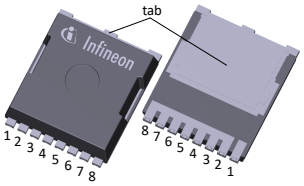
Automotive MOSFET

PG-HSOF-8

OptiMOS™ 7 Power-Transistor

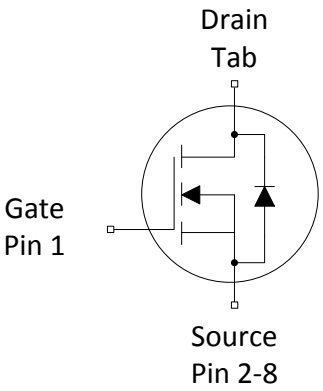


Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.



Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on)}$	0.24	mΩ
I_D(chip limited)	905	A

AEC Qualified
Extended quality
RoHS

Part number	Package	Marking	Related links
IAUTN04S7N003	PG-HSOF-8	7N04N003	see Appendix A

Table of contents

1 Maximum ratings

at Tj=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	905	A	Chip limitation, V_{GS} = 10 V [1) 2)]
				350		DC current, V_{GS} = 10 V
				107		R_{thJA} on 2s2p, V_{GS} = 10 V, T_a = 100 °C [1) 3)]
Pulsed drain current [1)]	$I_{D,pulse}$	-	-	3510	A	T_C = 25 °C, t_p = 100 µs
Avalanche energy, single pulse [1)]	E_{AS}	-	-	1064	mJ	I_D = 175 A
Avalanche current, single pulse	I_{AS}	-	-	350	A	-
Gate source voltage	V_{GS}	-20		20	V	
Power dissipation	P_{tot}	-	-	357	W	T_C = 25 °C
Operating temperature	T_j	-55	-	175	°C	-

1) The parameter is not subject to production testing - specified by design.

2) The current is limited by the overall system design, including the customer-specific PCB.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [4]	R_{thJC}	-	-	0.42	K/W	-
Thermal resistance, junction - ambient [5] [4]	R_{thJA}		14.8	-		

[4] The parameter is not subject to production testing - specified by design.

[5] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	I_D = 1 mA, V_{GS} = 0 V
Gate threshold voltage	$V_{GS(th)}$	2.2	2.6	3	V	V_{DS}=V_{GS}, I_D = 275 µA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS} = 40 V, T_J = 25 °C, V_{GS} = 0 V
				69		V_{DS} = 40 V, T_J = 100 °C, V_{GS} = 0 V [6]
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{DS} = 0 V, V_{GS} = 20 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.26	0.29	mΩ	I_D = 50 A, V_{GS} = 7 V
			0.22	0.24		I_D = 100 A, V_{GS} = 10 V
Gate resistance [6]	R_G	-	1.1	-	Ω	-

[6] The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	18460	24000	pF	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance [7]	C_{oss}		10730	13950		
Reverse transfer capacitance [7]	C_{rss}		340	505		
Turn-on delay time [7]	$t_{d(on)}$	-	45	-	ns	I_D = 100 A, V_{GS} = 10 V, V_{DD} = 20 V, R_G = 3.5 Ω
Rise time [7]	t_r		51			
Turn-off delay time [7]	$t_{d(off)}$		132			
Fall time [7]	t_f		84			

[7] The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge [8]	Q_{gs}	-	72	94	nC	I_D = 100 A, V_{DS} = 20 V, V_{GS} = 0 V to 10 V
Gate to drain charge [8]	Q_{gd}		52	78	nC	
Gate charge total [8]	Q_g		268	349	nC	
Gate plateau voltage [8]	$V_{plateau}$		3.9	-	V	

[8] The parameter is not subject to production testing - specified by design.

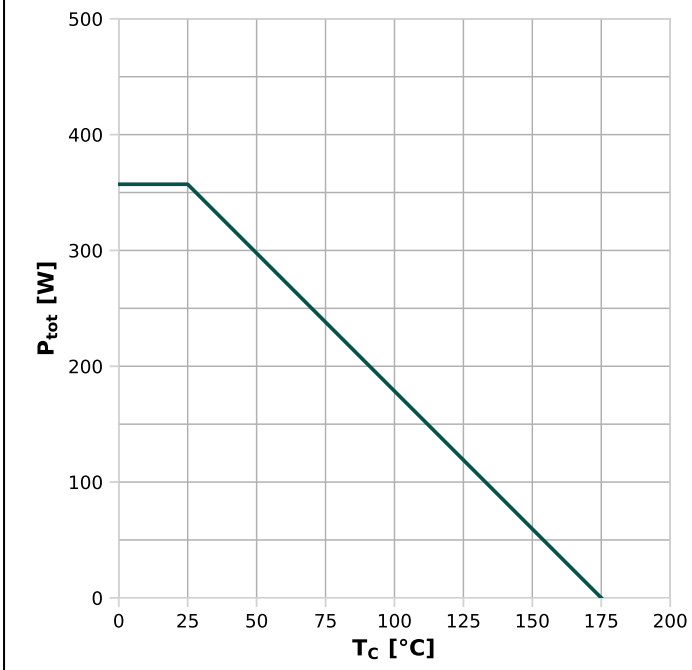
Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current [9]	I_S	-	-	350	A	T_C = 25 °C
Diode pulse current [9]	$I_{S,pulse}$	-	-	3510	A	T_C = 25 °C, t_p = 100 µs
Diode forward voltage	V_{SD}	-	0.8	0.95	V	T_J = 25 °C, V_{GS} = 0 V, I_F = 100 A
Reverse recovery time [9]	t_{rr}	-	83	125	ns	di_F/dt =100 A/µs, V_R = 20 V, I_F = 50 A
Reverse recovery charge [9]	Q_{rr}		126	252	nC	

[9] The parameter is not subject to production testing - specified by design.

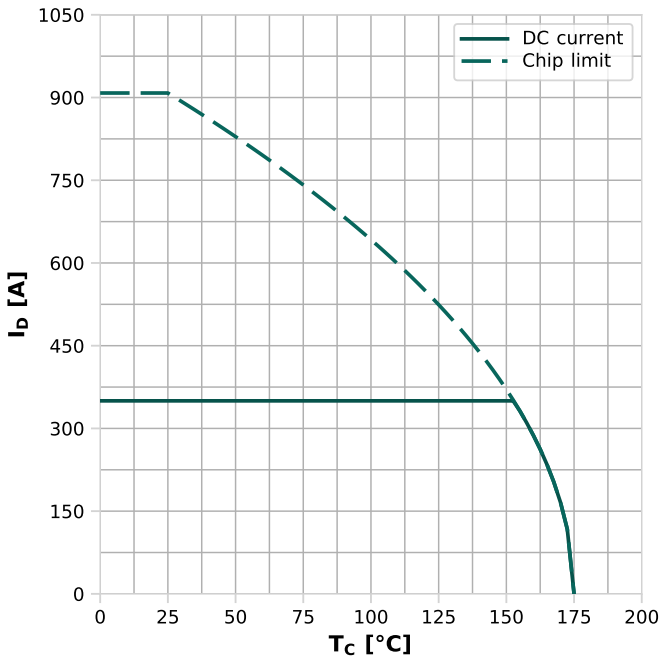
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



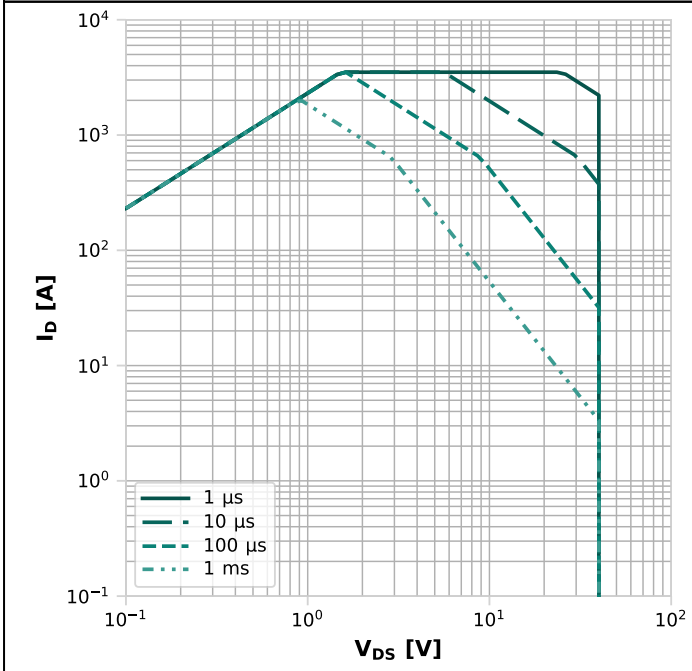
$P_{tot}=f(T_C)$; $V_{GS} \geq 6$ V

Diagram 2: Drain Current



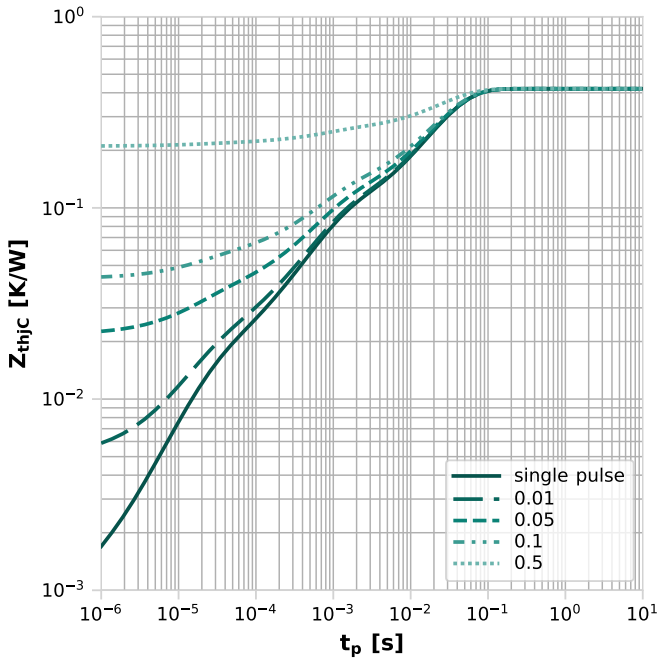
$I_D=f(T_C)$; $V_{GS} \geq 6$V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C= 25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



$Z_{thjC}=f(t_p)$; parameter: $D=t_p/T$

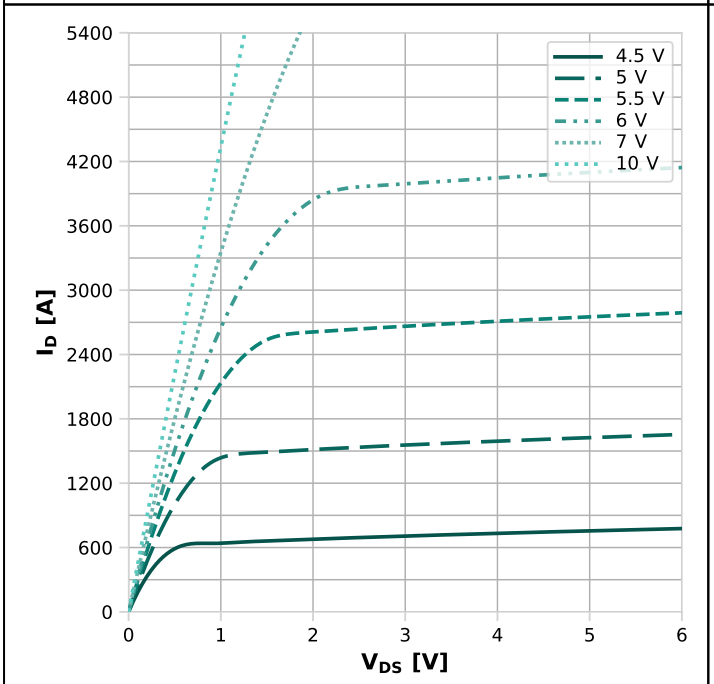
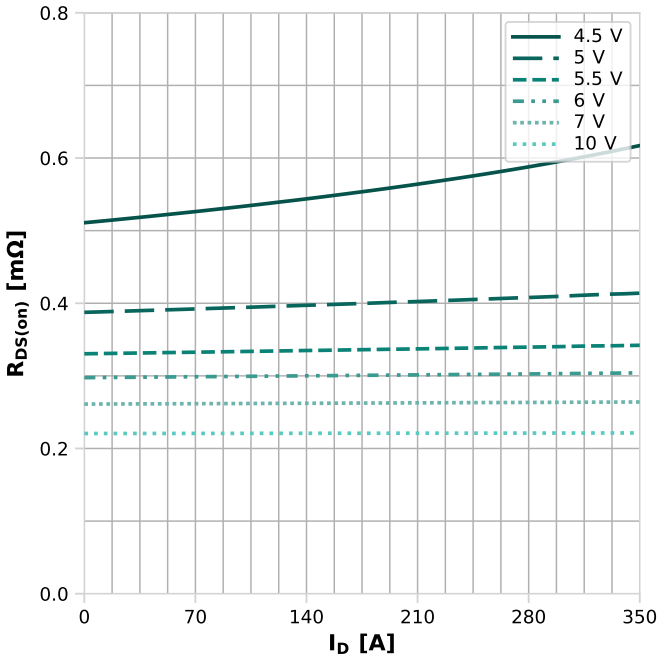
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on-state resistance
	
$I_D=f(V_{DS})$; T_j= 25 °C, parameter: V_{GS}	$R_{DS(on)}=f(I_D)$; T_j= 25 °C; parameter: V_{GS}

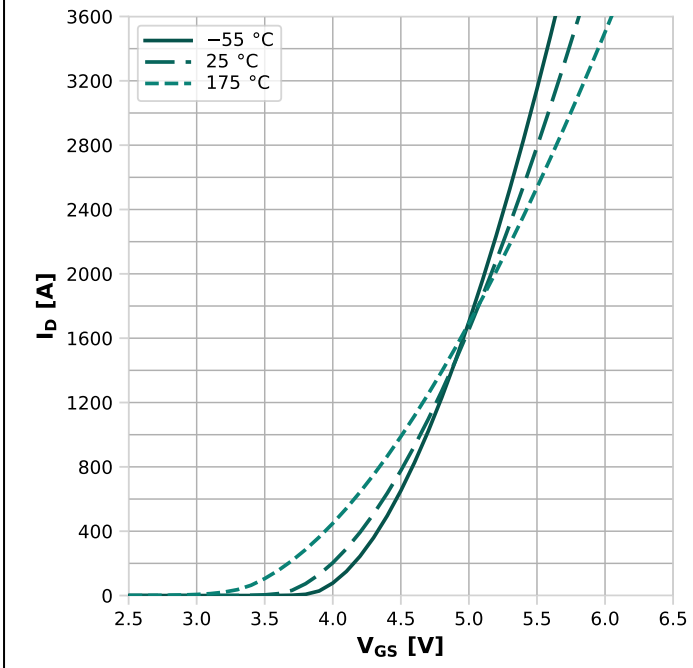
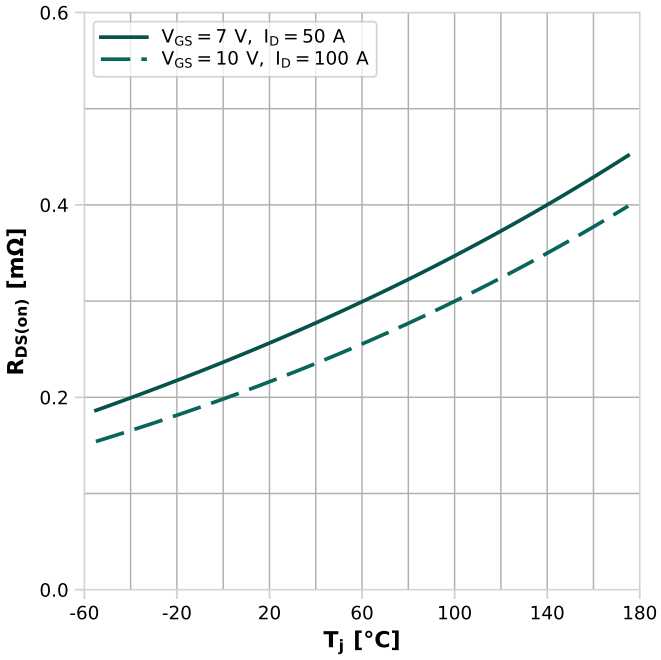
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on-state resistance
	
$I_D=f(V_{GS})$; V_{DS}= 6 V; parameter: T_j	$R_{DS(on)}=f(T_j)$; parameter: I_D, V_{GS}

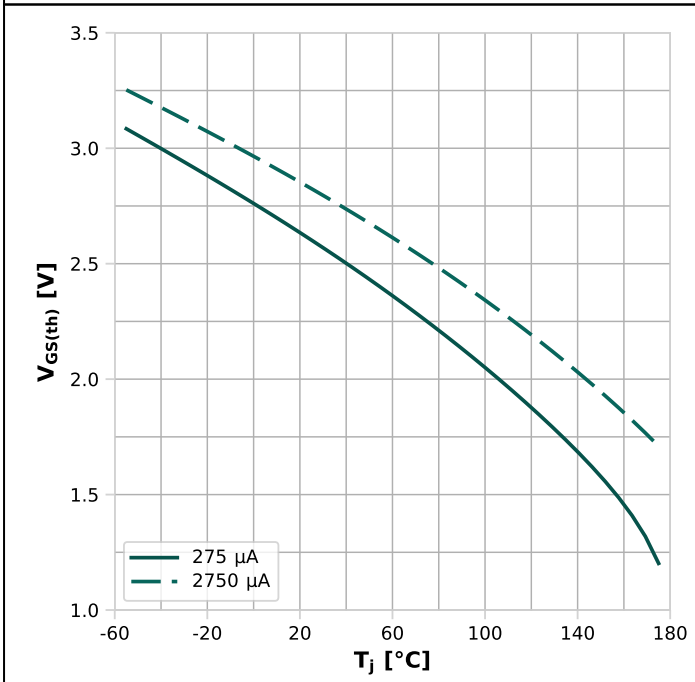
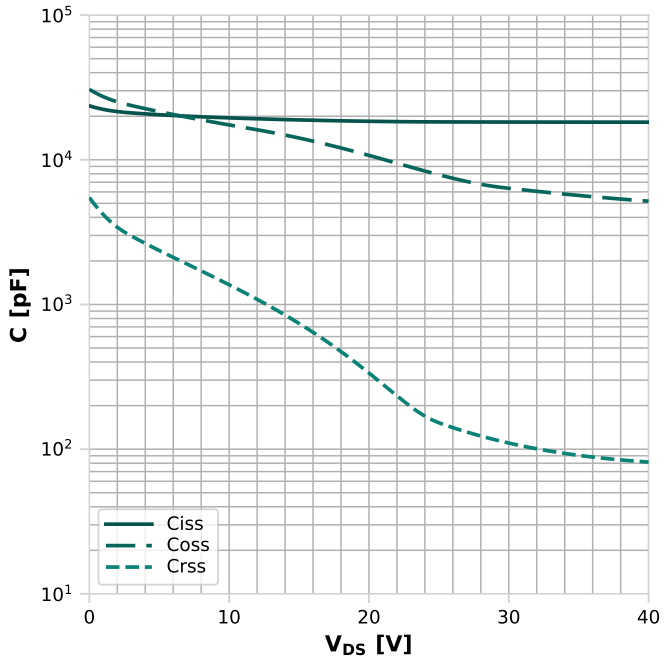
Diagram 9: Typ. gate threshold voltage	Diagram 10: Typ. capacitances
	
$V_{GS(th)}=f(T_j)$; $V_{GS}= V_{DS}$; parameter: I_D	$C=f(V_{DS})$; $V_{GS}= 0$ V; f=1 MHz

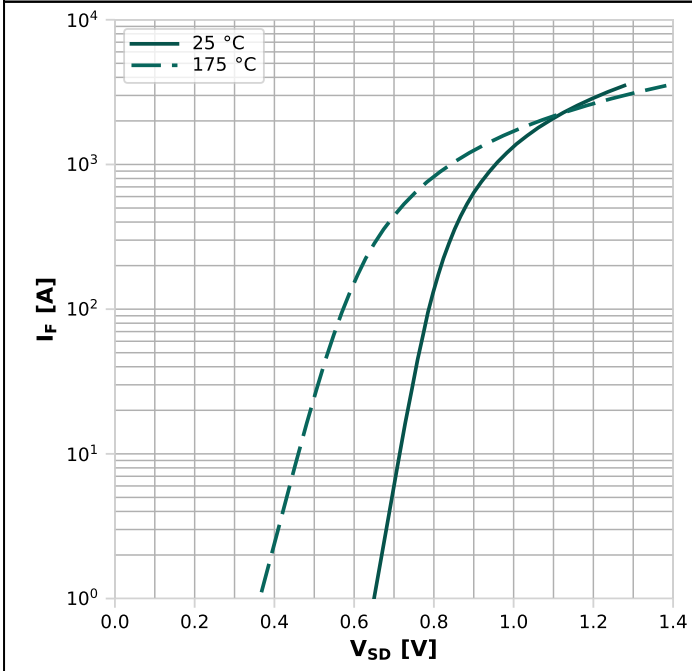
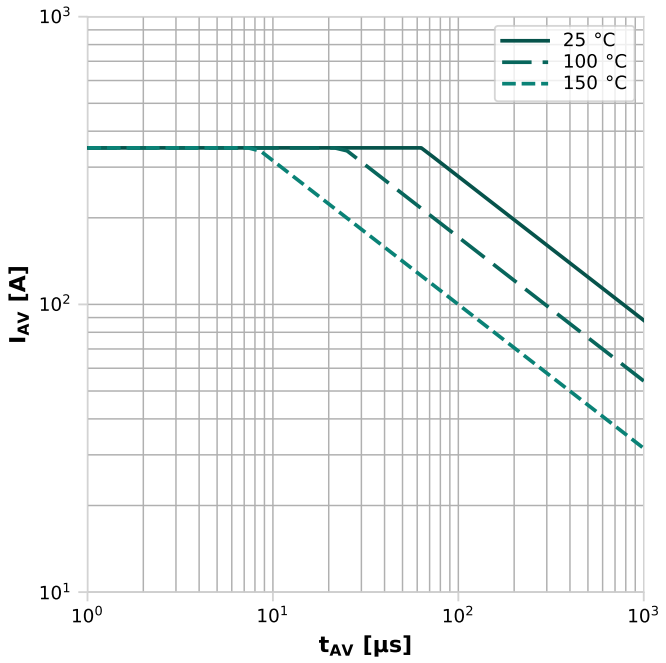
Diagram 11: Typ. forward diode characteristics	Diagram 12: Typ. avalanche characteristics
	
$I_F=f(V_{SD})$; parameter: T_j	$I_{AS}=f(t_{AV})$; parameter: $T_{j(start)}$

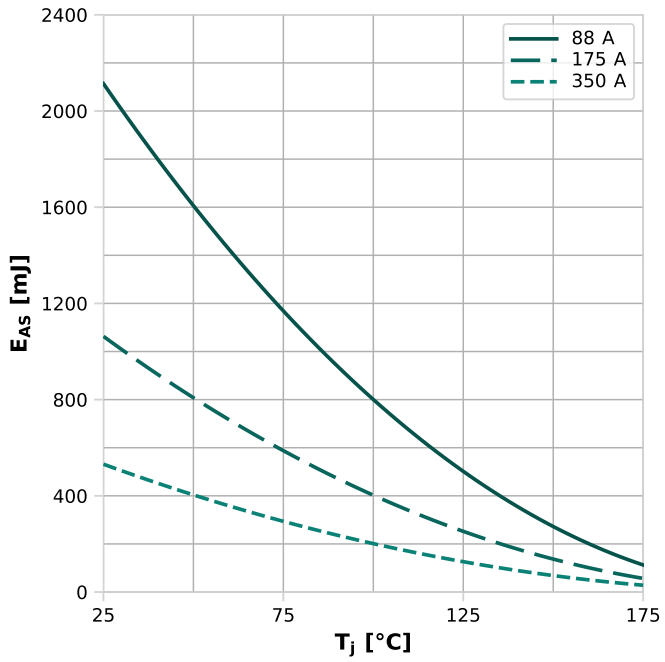
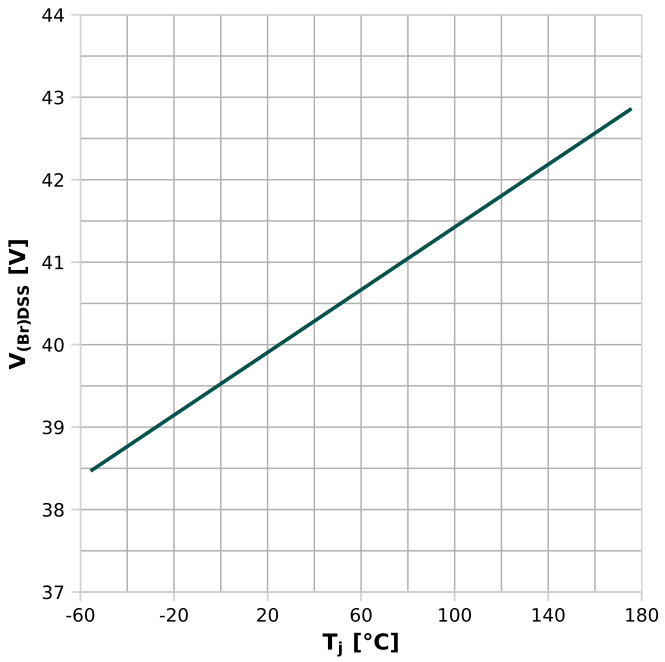
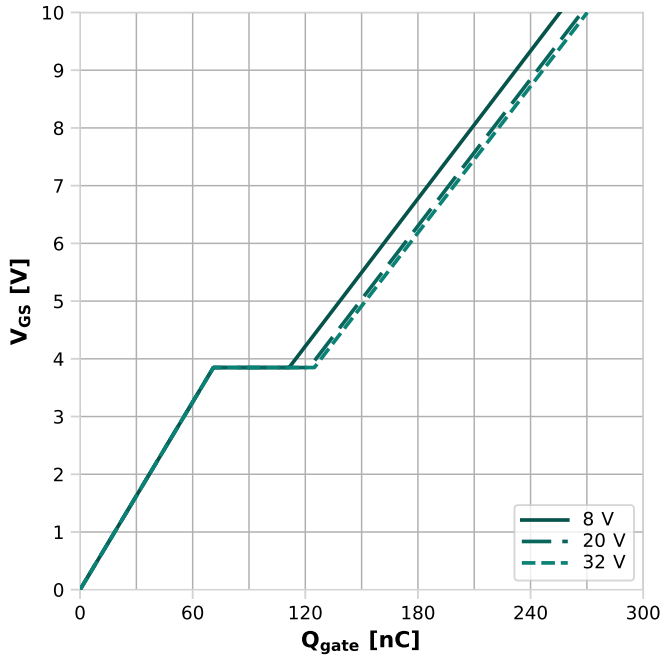
Diagram 13: Typical avalanche Energy	Diagram 14: Drain-source breakdown voltage
	
$E_{AS}=f(T_j)$; parameter: I_D	$V_{(Br)DSS}=f(T_j)$; I_D= 10 mA

Diagram 15: Typ. gate charge

$V_{GS}=f(Q_{gate})$; I_D= 100 A pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Diode characteristics

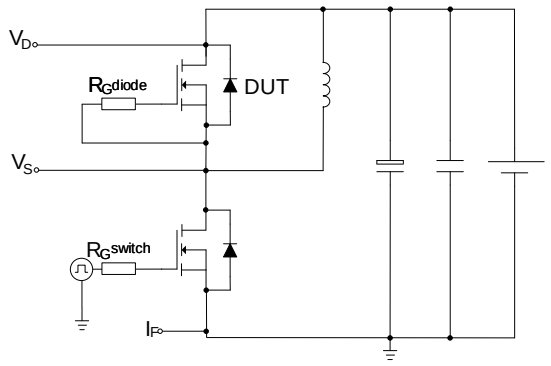
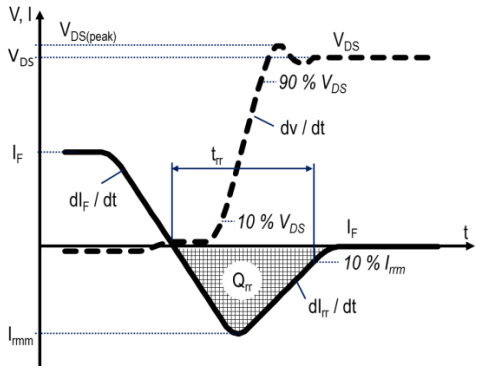
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Unclamped inductive load test circuit

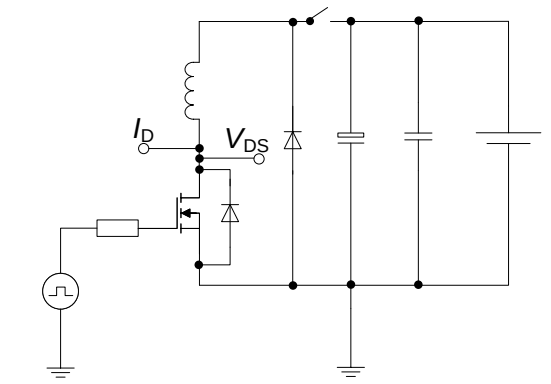
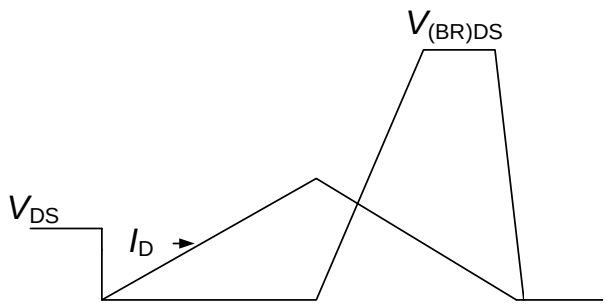
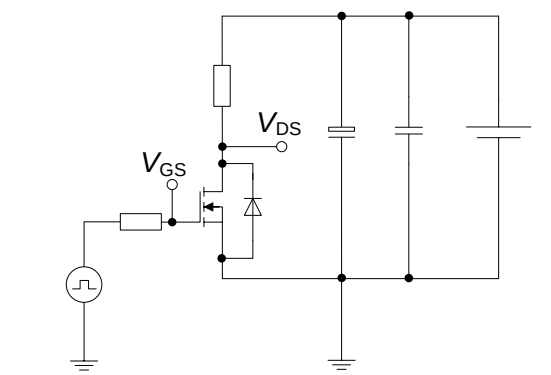
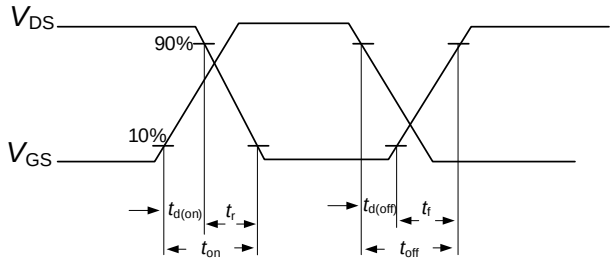
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 10 Switching times test circuit for resistive load

Switching times test circuit for resistive load	Switching times waveform
	

6 Package outlines

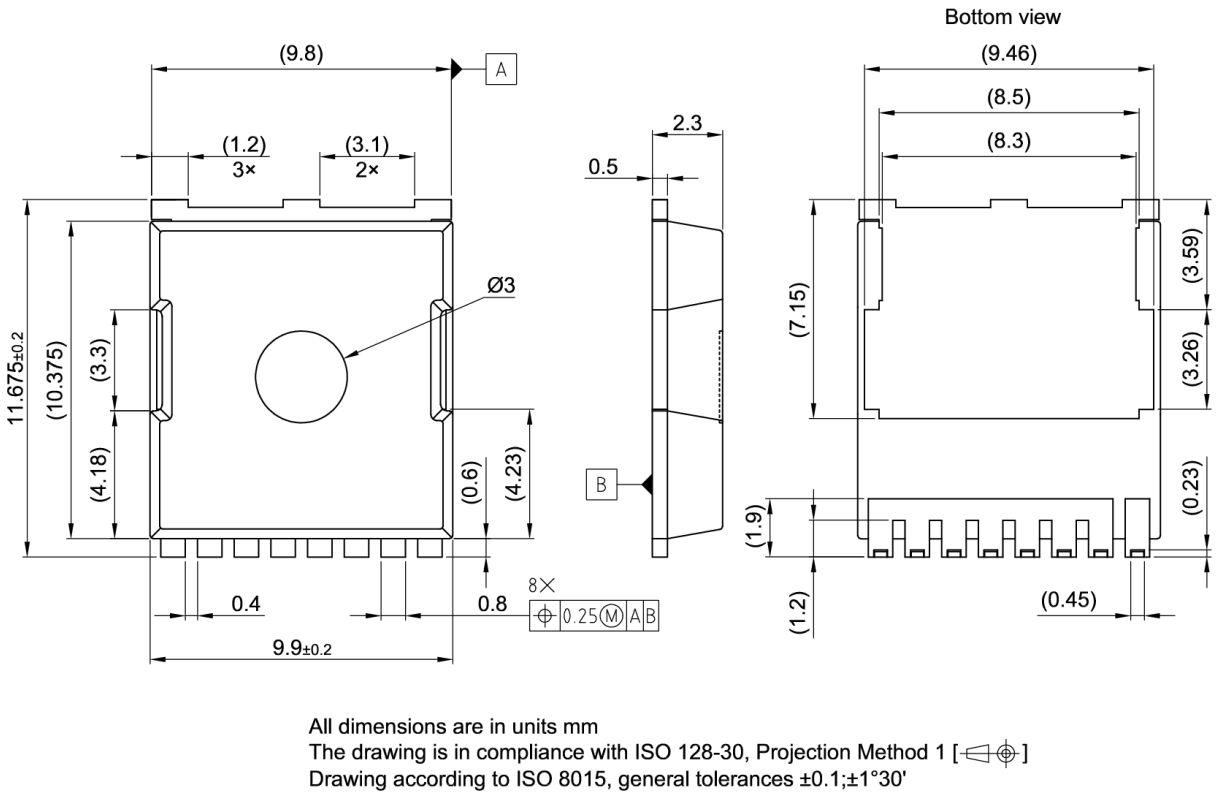


Figure 1 Outline PG-HSOF-8, dimensions in mm

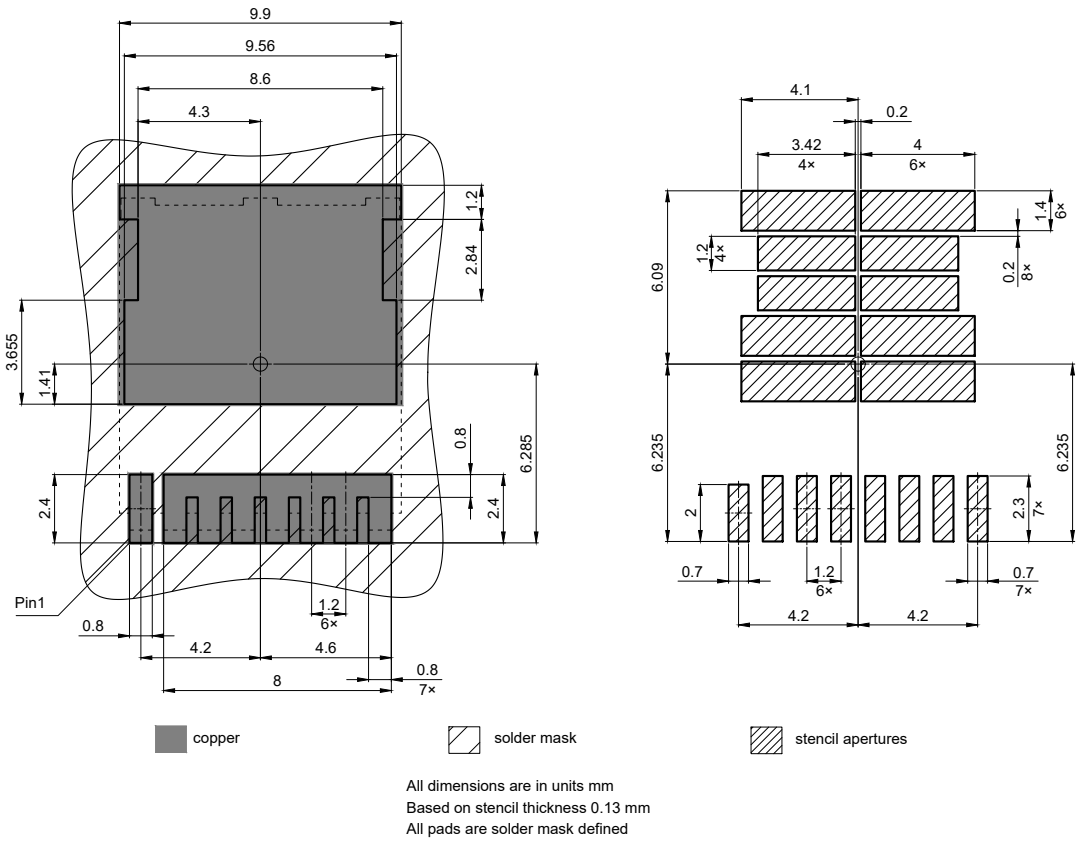
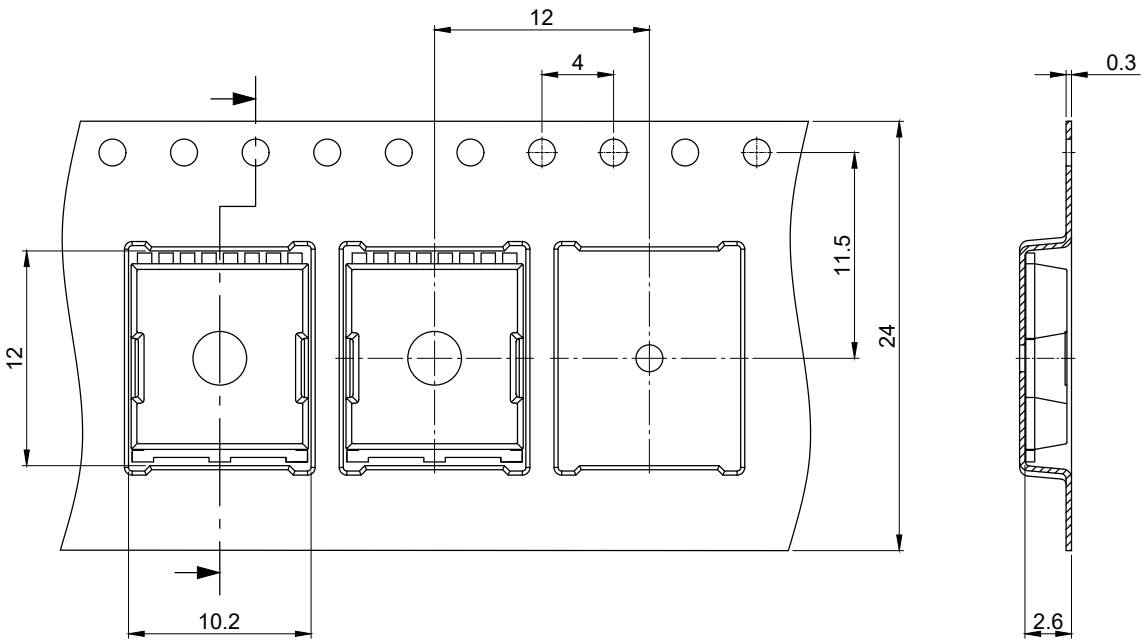


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUTN04S7N003

Revision 2026-03-23, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-03-23	Final Datasheet

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