

Automotive MOSFET

OptiMOS™ P2 Power-Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- P-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

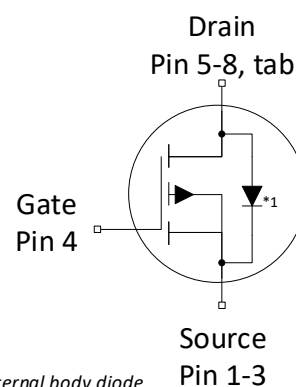
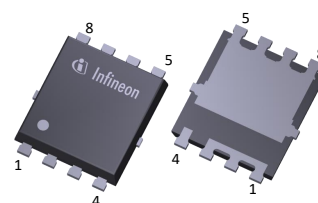
Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
$-V_{DS}$	40	V
$R_{DS(on)}$	12.5	mΩ
$-I_D$ (chip limited)	64	A

PG-TDSON-8



Part number	Package	Marking	Related links
IAUCP04P4N120	PG-TDSON-8	4P04N120	see Appendix A



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1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	$-I_D$	-	-	64	A	Chip limitation, $-V_{GS} = 10\text{ V}$ ^{1) 2)}
				60		DC current, $-V_{GS} = 10\text{ V}$
				11		R_{thJA} on 2s2p, $-V_{GS} = 10\text{ V}$, $T_a = 100\text{ °C}$ ^{1) 3)}
Pulsed drain current ¹⁾	$-I_{D,pulse}$	-	-	162	A	$T_C = 25\text{ °C}$, $t_p = 100\text{ }\mu\text{s}$
Avalanche energy, single pulse ¹⁾	E_{AS}	-	-	12	mJ	$-I_D = 30\text{ A}$
Avalanche current, single pulse	$-I_{AS}$	-	-	60	A	-
Gate source voltage	$-V_{GS}$	-20	-	20	V	
Power dissipation	P_{tot}	-	-	78	W	$T_C = 25\text{ °C}$
Operating temperature	T_j	-55	-	175	°C	-

¹⁾ The parameter is not subject to production testing - specified by design.

²⁾ The current is limited by the overall system design, including the customer-specific PCB.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case 4)	R_{thJC}	-	-	1.95	K/W	-
Thermal resistance, junction - ambient 5) 4)	R_{thJA}		28.0	-		

4) The parameter is not subject to production testing - specified by design.

5) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$-V_{(BR)DSS}$	40	-	-	V	$-I_D = 1\text{ mA}$, $-V_{GS} = 0\text{ V}$
Gate threshold voltage	$-V_{GS(th)}$	2	3	4	V	$V_{DS} = V_{GS}$, $-I_D = 75\text{ }\mu\text{A}$
Zero gate voltage drain current	$-I_{DSS}$	-	-	1	μA	$T_j = 25^\circ\text{C}$, $-V_{GS} = 0\text{ V}$, $-V_{DS} = 32\text{ V}$
				200		$-V_{GS} = 0\text{ V}$, $T_j = 125^\circ\text{C}$, $-V_{DS} = 32\text{ V}$ ⁶⁾
Gate-source leakage current	$-I_{GSS}$	-	-	100	nA	$-V_{DS} = 0\text{ V}$, $-V_{GS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	10.4	12.5	m Ω	$-I_D = 60\text{ A}$, $-V_{GS} = 10\text{ V}$

⁶⁾ The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	2540	3300	pF	$-V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$, $-V_{DS} = 25 \text{ V}$
Output capacitance ⁷⁾	C_{oss}		850	1280		
Reverse transfer capacitance ⁷⁾	C_{rss}		35	70		
Turn-on delay time ⁷⁾	$t_{d(on)}$	-	17	-	ns	$-I_D = 60 \text{ A}$, $-V_{GS} = 10 \text{ V}$, $R_G = 3.5 \Omega$, $-V_{DD} = 20 \text{ V}$
Rise time ⁷⁾	t_r		21			
Turn-off delay time ⁷⁾	$t_{d(off)}$		21			
Fall time ⁷⁾	t_f		20			

⁷⁾ The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁸⁾	Q_{gs}	-	15	20	nC	$-I_D = 60 \text{ A}$, $-V_{GS} = 0 \text{ V}$ to 10 V , $-V_{DS} = 32 \text{ V}$
Gate to drain charge ⁸⁾	Q_{gd}		5	10	nC	
Gate charge total ⁸⁾	Q_g		34	44	nC	
Gate plateau voltage ⁸⁾	$-V_{plateau}$		5.8	-	V	

⁸⁾ The parameter is not subject to production testing - specified by design.

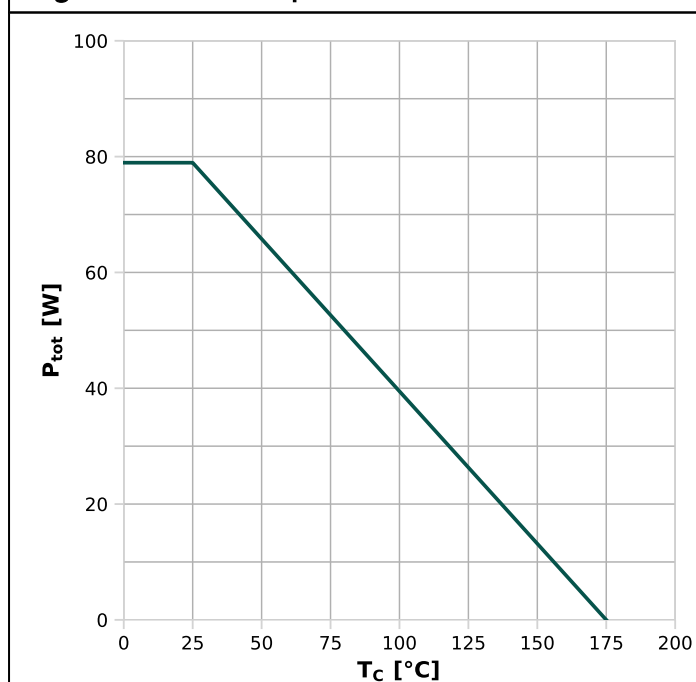
Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current ⁹⁾	$-I_S$	-	-	60	A	$T_C = 25 \text{ °C}$
Diode pulse current ⁹⁾	$-I_{S,pulse}$	-	-	162	A	$T_C = 25 \text{ °C}$, $t_p = 100 \text{ } \mu\text{s}$
Diode forward voltage	$-V_{SD}$	-	0.95	1.25	V	$T_J = 25 \text{ °C}$, $-V_{GS} = 0 \text{ V}$, $-I_F = 60 \text{ A}$
Reverse recovery time ⁹⁾	t_{rr}	-	31	-	ns	$di_F/dt = 100 \text{ A}/\mu\text{s}$, $-V_R = 20 \text{ V}$, $-I_F = 50 \text{ A}$
Reverse recovery charge ⁹⁾	Q_{rr}		19		nC	

⁹⁾ The parameter is not subject to production testing - specified by design.

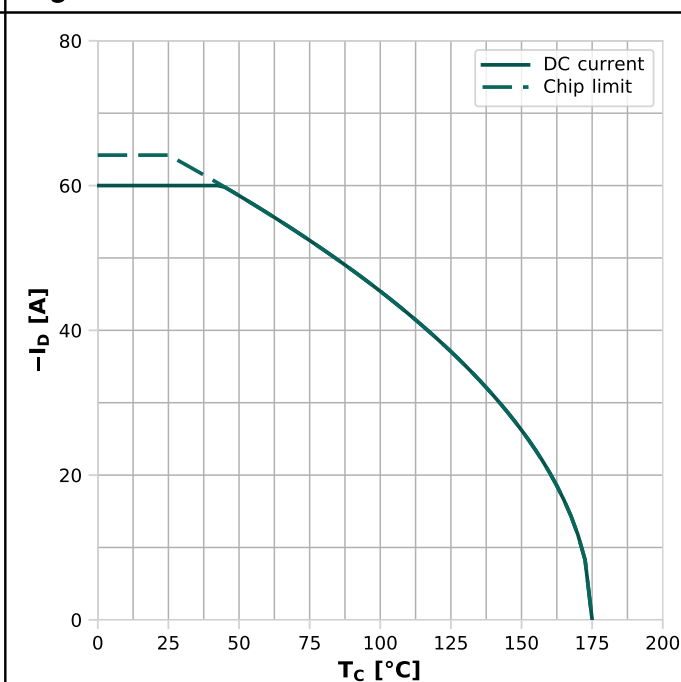
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



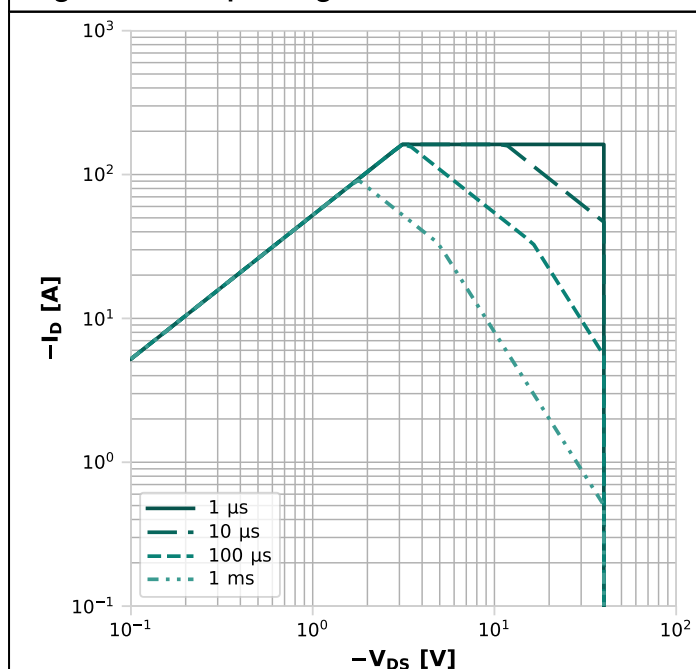
$$P_{tot}=f(T_c); -V_{GS} \geq 6 \text{ V}$$

Diagram 2: Drain Current



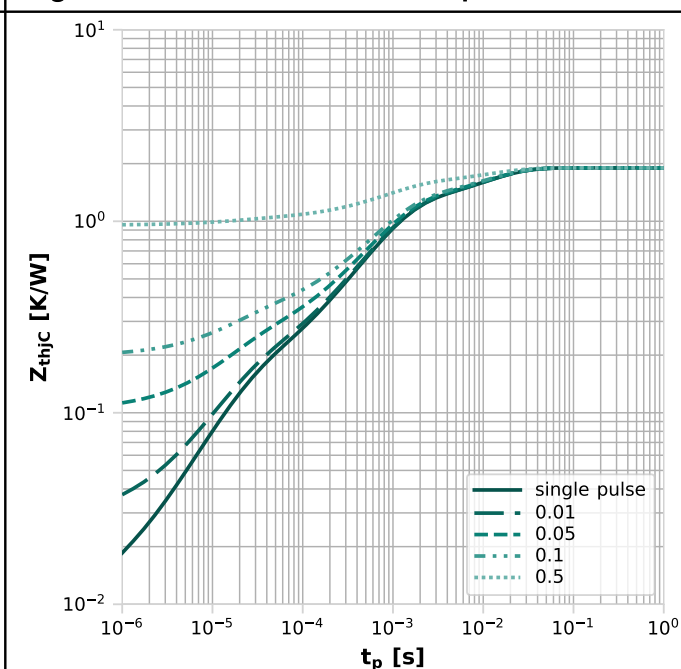
$$-I_D=f(T_c); -V_{GS} \geq 6 \text{ V}$$

Diagram 3: Safe operating area



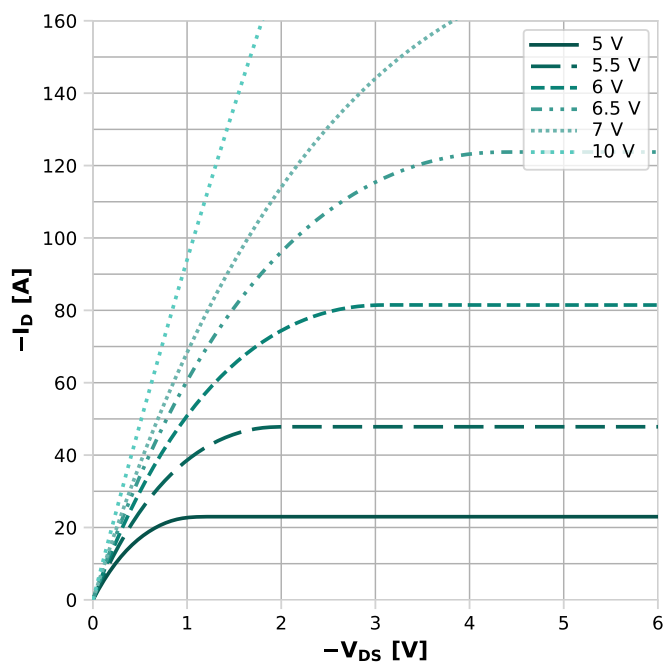
$$-I_D=f(-V_{DS}); T_c=25^\circ\text{C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



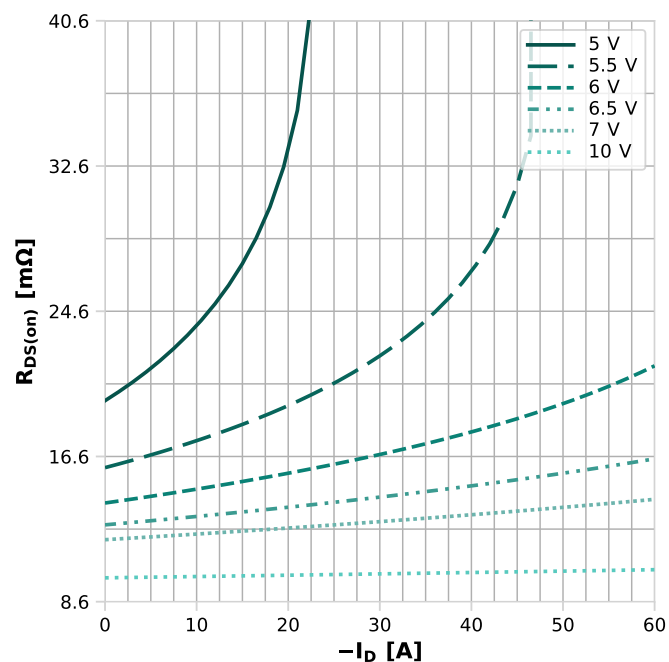
$$Z_{thjC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



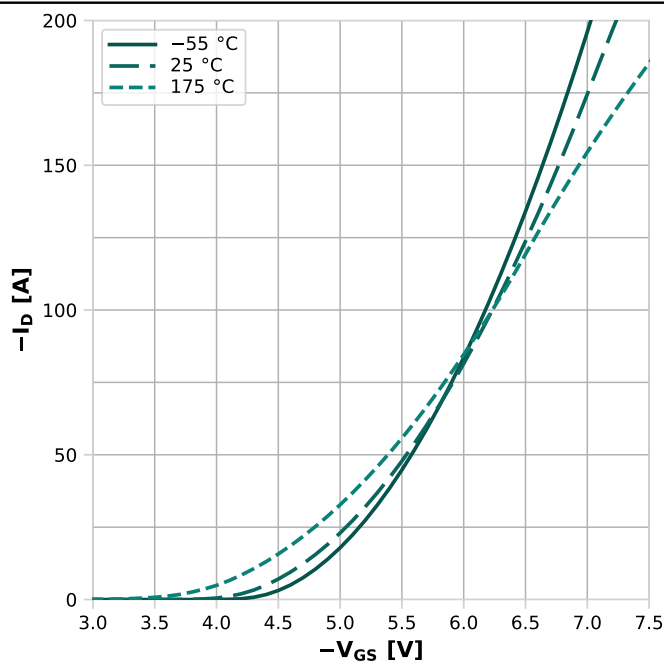
$-I_D = f(-V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: $-V_{GS}$

Diagram 6: Typ. drain-source on-state resistance



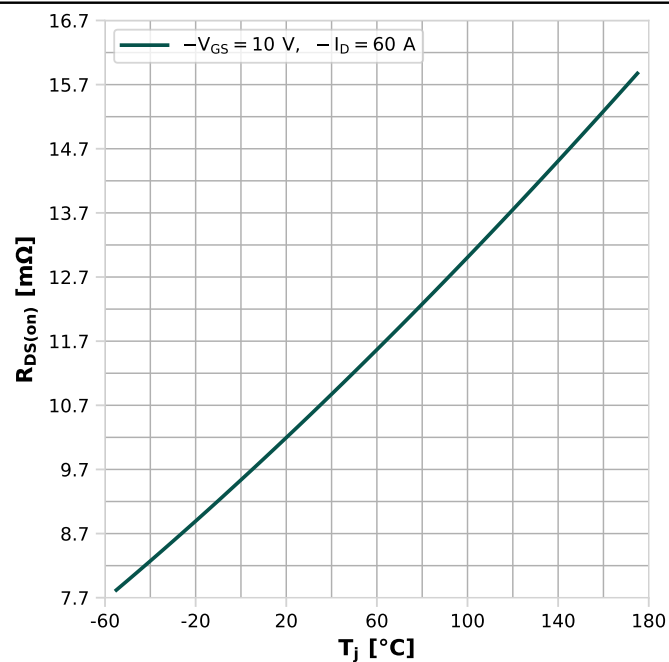
$R_{DS(on)} = f(-I_D)$; $T_j = 25^\circ\text{C}$; parameter: $-V_{GS}$

Diagram 7: Typ. transfer characteristics



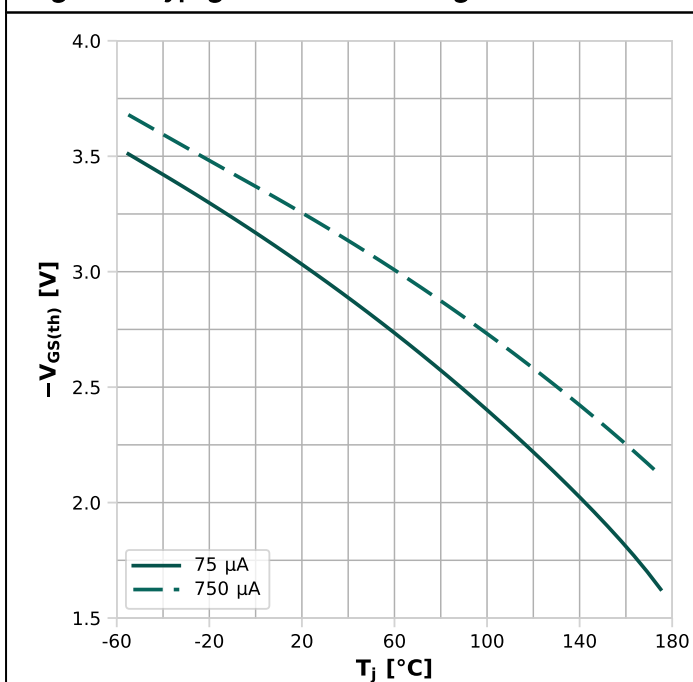
$-I_D = f(-V_{GS})$; $-V_{DS} = 6\text{ V}$; parameter: T_j

Diagram 8: Typ. drain-source on-state resistance



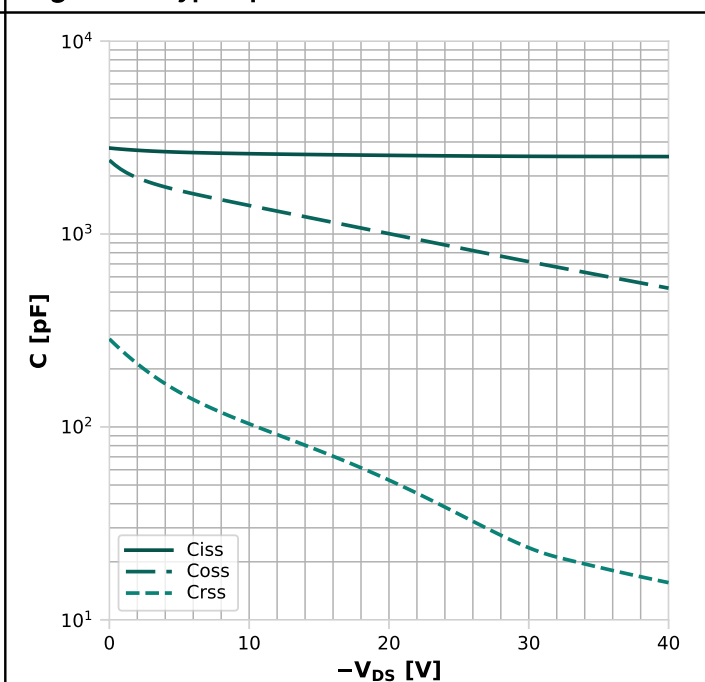
$R_{DS(on)} = f(T_j)$; parameter: $-I_D$, $-V_{GS}$

Diagram 9: Typ. gate threshold voltage



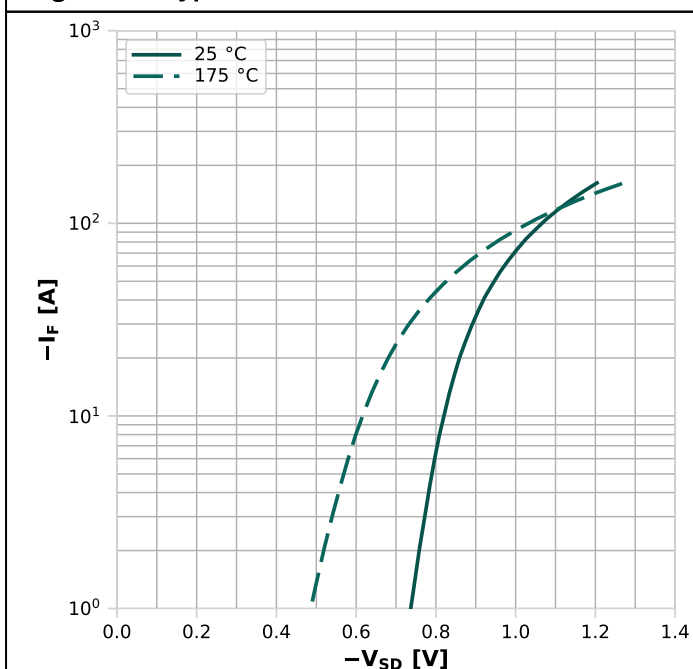
$-V_{GS(th)} = f(T_j)$; $-V_{GS} = -V_{DS}$; parameter: $-I_D$

Diagram 10: Typ. capacitances



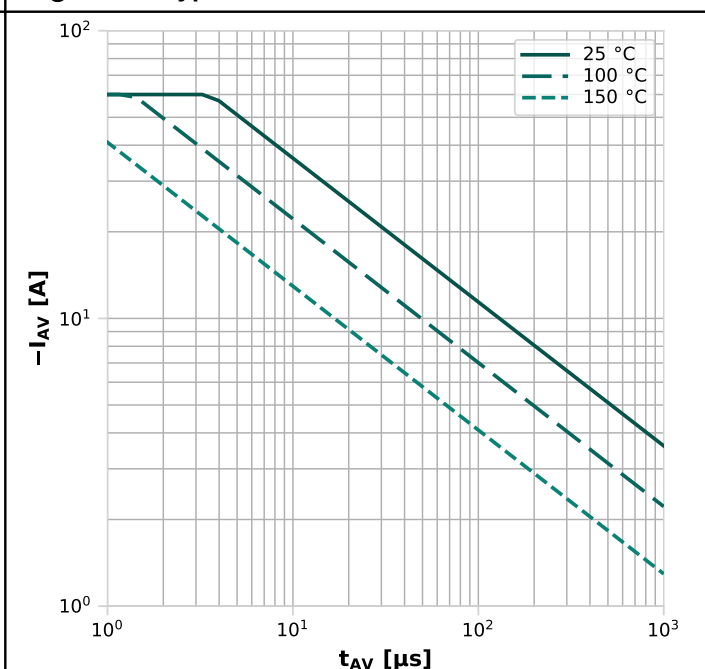
$C = f(-V_{DS})$; $-V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Diagram 11: Typ. forward diode characteristics



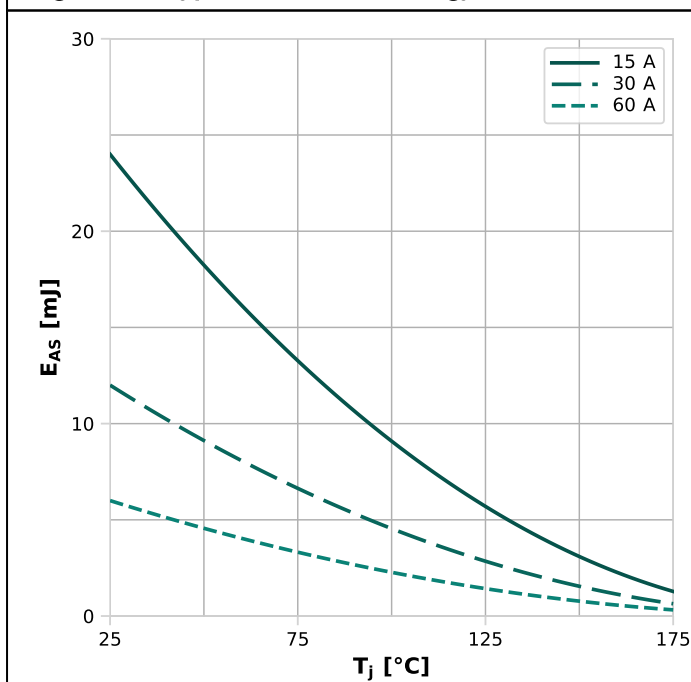
$-I_F = f(-V_{SD})$; parameter: T_j

Diagram 12: Typ. avalanche characteristics



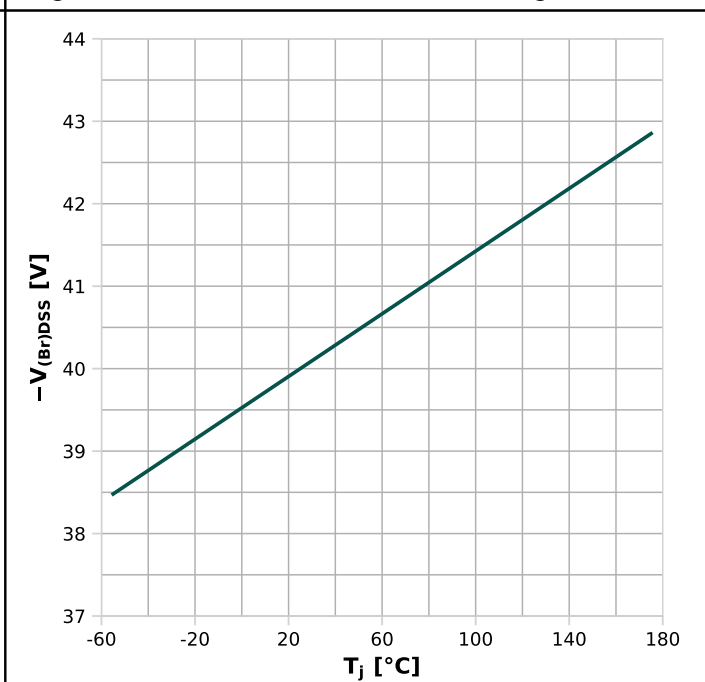
$-I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$

Diagram 13: Typical avalanche Energy



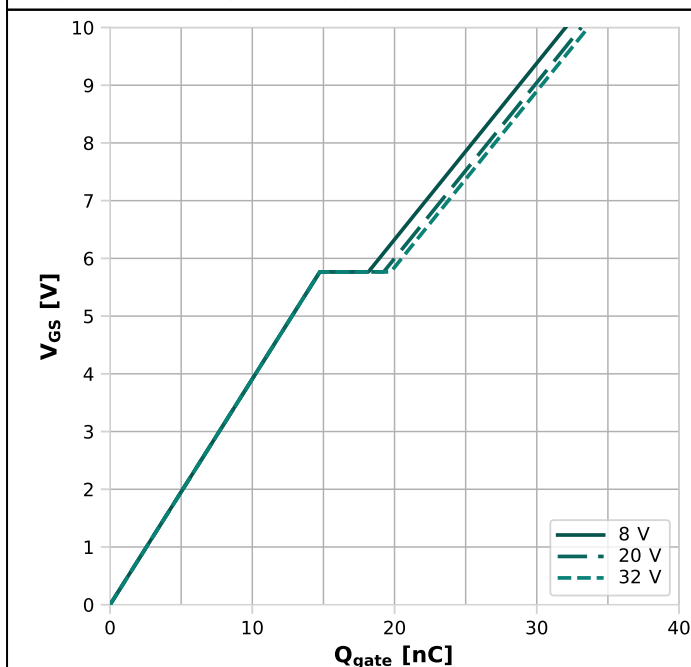
$E_{AS}=f(T_J)$; parameter: $-I_D$

Diagram 14: Drain-source breakdown voltage



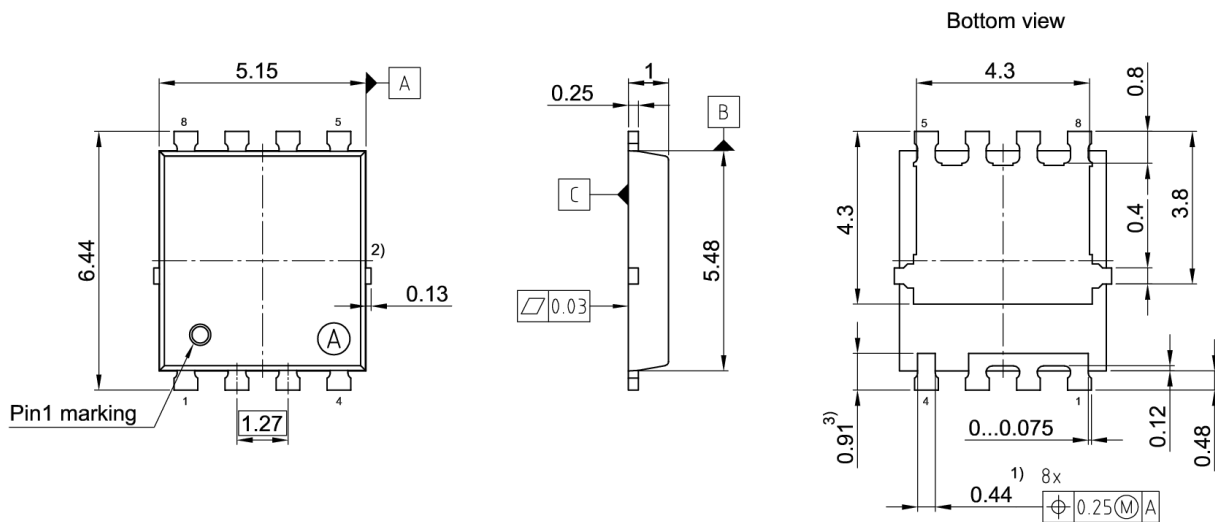
$-V_{(Br)DSS}=f(T_J)$; $-I_D=1\text{ mA}$

Diagram 15: Typ. gate charge



$-V_{GS}=f(Q_{gate})$; $-I_D=60\text{ A pulsed}$; parameter: $-V_{DS}$

5 Package outlines



- 1) Excluded mold flash.
- 2) Removal on mold gate:
Intrusion 0.1mm.
Protrusion 0.1mm.
- 3) Lead length up to anti flash line.
- 4) All metal surface are plated, except area of cut.

All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []
Drawing according to ISO 8015, general tolerances $\pm 0.1; \pm 1^\circ 30'$

Figure 1 Outline PG-TDSON-8, dimensions in mm

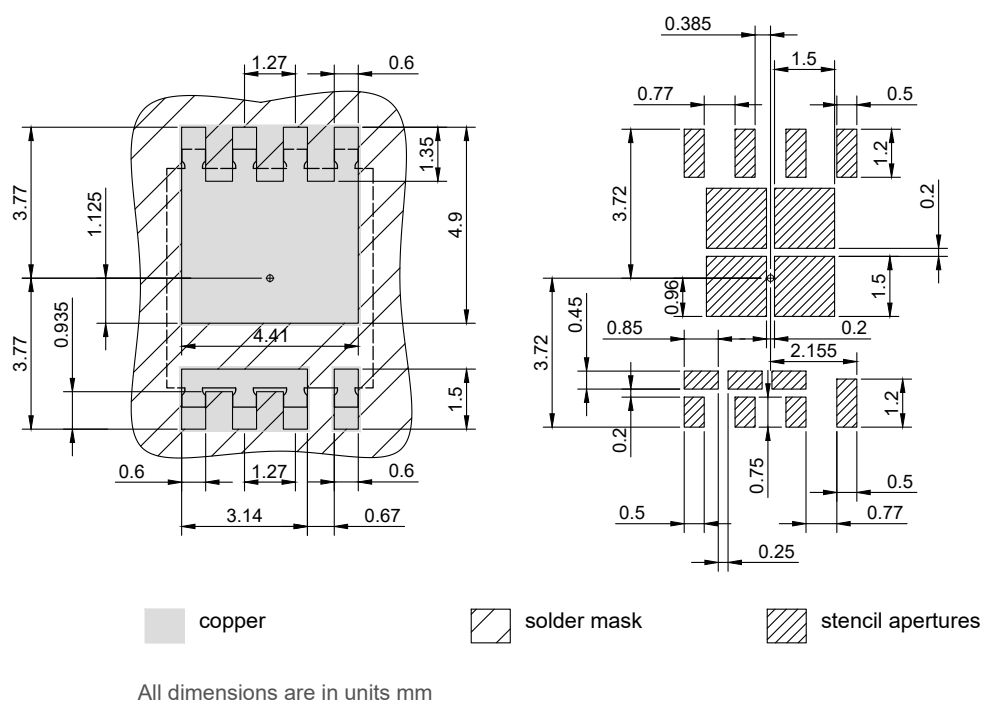


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

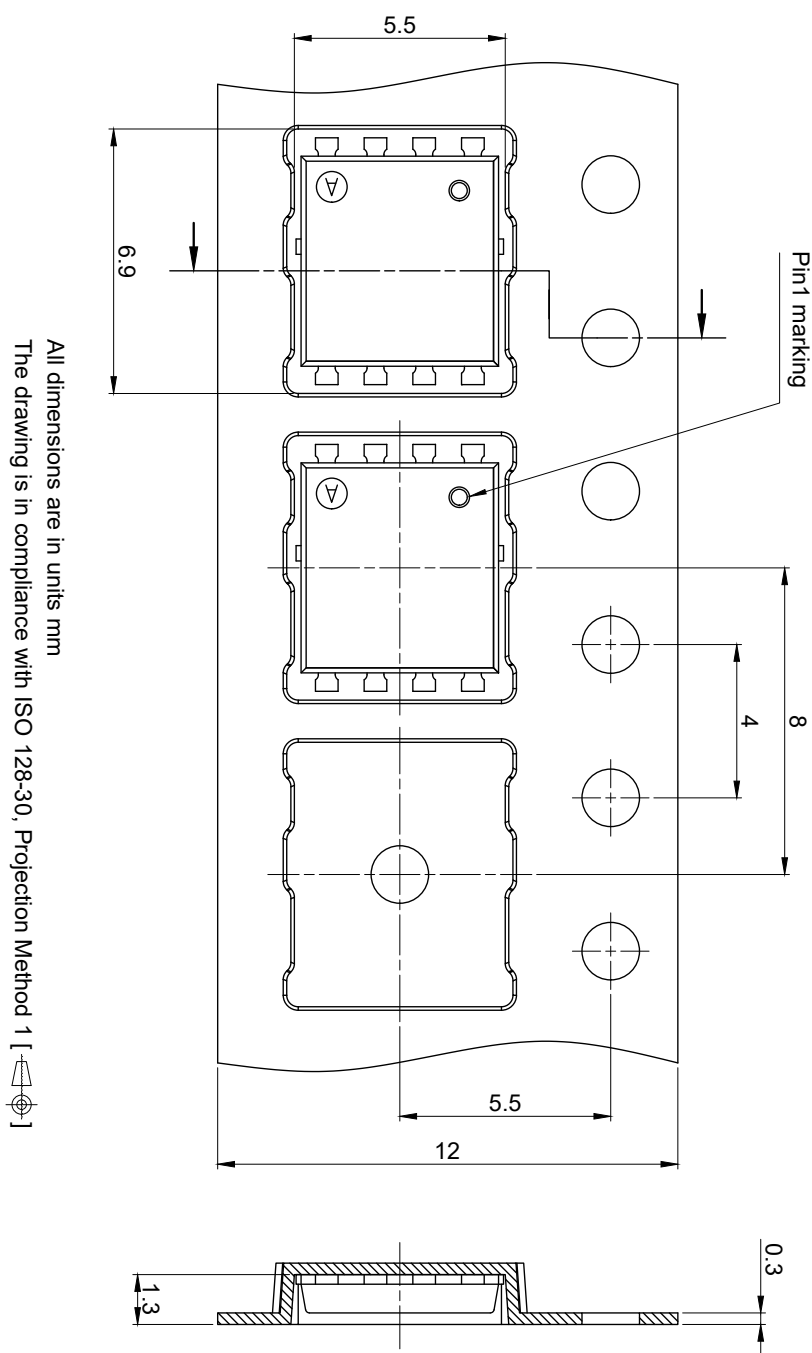


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

6 Appendix A

Table 8 Related links

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUCP04P4N120

Revision 2026-07-14, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-07-14	Release of Final Datasheet

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