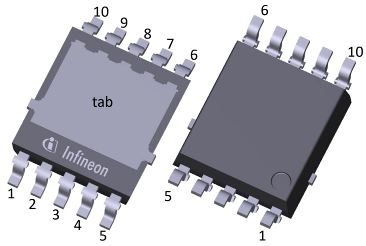
Automotive MOSFET

OptiMOS™ 7 Power-Transistor

PG-LHDSO-10



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.

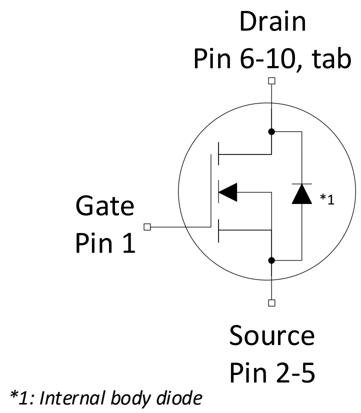


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	28.6	mΩ
I_D(chip limited)	27	A

Part number	Package	Marking	Related links
IAUCN10S7L290T	PG-LHDSO-10	7B1	see Appendix A

Table of contents

1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values Min.	Values Typ.	Values Max.	Unit	Note / Test condition
Continuous drain current	I_D	-	-	27	A	Chip limitation, V_{GS} = 10 V [1) 2)]
				27		DC current, V_{GS} = 10 V
				13		R_{thJH} on 2s2p, V_{GS} = 10 V, T_a = 100 °C [1) 3)]
Pulsed drain current [1)]	$I_{D,pulse}$	-	-	52	A	T_C = 25 °C, t_p = 100 µs
Avalanche energy, single pulse [1)]	E_{AS}	-	-	12	mJ	I_D = 9 A
Avalanche current, single pulse	I_{AS}	-	-	18	A	-
Gate source voltage	V_{GS}	-16		16	V	
Gate source voltage	V_{GS}	-	-	20	V	Limited to duty factor of 1%
Power dissipation	P_{tot}	-	-	45	W	T_C = 25 °C
Operating temperature	T_j	-55	-	175	°C	-

1) The parameter is not subject to production testing - specified by design.

2) The current is limited by the overall system design, including the customer-specific PCB.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [4]	R_{thJC}	-	-	3.34	K/W	-
Thermal characterization parameter, source pin [4] [5]	Ψ_{source}	-	14.2	-	K/W	-
Thermal characterization parameter, drain pin [4] [6]	Ψ_{drain}	-	11.4	-	K/W	-
Thermal resistance, junction - heatsink [4] [7]	R_{thJH}	-	10.1	-	K/W	-
Thermal resistance, junction - ambient [8] [4]	R_{thJA}	-	48.7	-	K/W	-

[4] The parameter is not subject to production testing - specified by design.

[5] Thermal characterization parameter, calculated as $\Psi_{source} = (T_{source} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at source pins for given power.

[6] Thermal characterization parameter, calculated as $\Psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at drain pins for given power.

[7] Device on 2s2p FR4 PCB defined in acc. with JEDEC standards (JESD51-5,-7) without thermal vias, heat sink of 71 x 110 x 2 mm is attached through TIM with 3.3 W/(m*K) and 400 µm thickness to tip side pad. Heatsink fixed to 85°C ambient temperature.

[8] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5,-7). PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	I_D = 1 mA, V_{GS} = 0 V
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	V_{DS}=V_{GS}, I_D = 10 µA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS} = 100 V, T_j = 25 °C, V_{GS} = 0 V
				3		V_{DS} = 100 V, T_j = 100 °C, V_{GS} = 0 V [9]
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{DS} = 0 V, V_{GS} = 16 V
Drain-source on-state resistance	$R_{DS(on)}$	-	31.3	38.2	mΩ	I_D = 14 A, V_{GS} = 4.5 V
			25.5	28.6		I_D = 14 A, V_{GS} = 10 V
Gate resistance [9]	R_G	-	1.5	-	Ω	-

[9] The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [10]	C_{iss}	-	430	560	pF	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance [10]	C_{oss}		180	240		
Reverse transfer capacitance [10]	C_{rss}		5	8		
Turn-on delay time [10]	$t_{d(on)}$	-	2	-	ns	I_D = 14 A, V_{GS} = 10 V, V_{DD} = 50 V, R_G = 3.5 Ω
Rise time [10]	t_r		2			
Turn-off delay time [10]	$t_{d(off)}$		8			
Fall time [10]	t_f		4			

[10] The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge [11]	Q_{gs}	-	1.4	1.8	nC	I_D = 14 A, V_{DS} = 50 V, V_{GS} = 0 V to 10 V
Gate to drain charge [11]	Q_{gd}		2	3	nC	
Gate charge total [11]	Q_g		9	11	nC	
Gate plateau voltage [11]	$V_{plateau}$		3.1	-	V	

[11] The parameter is not subject to production testing - specified by design.

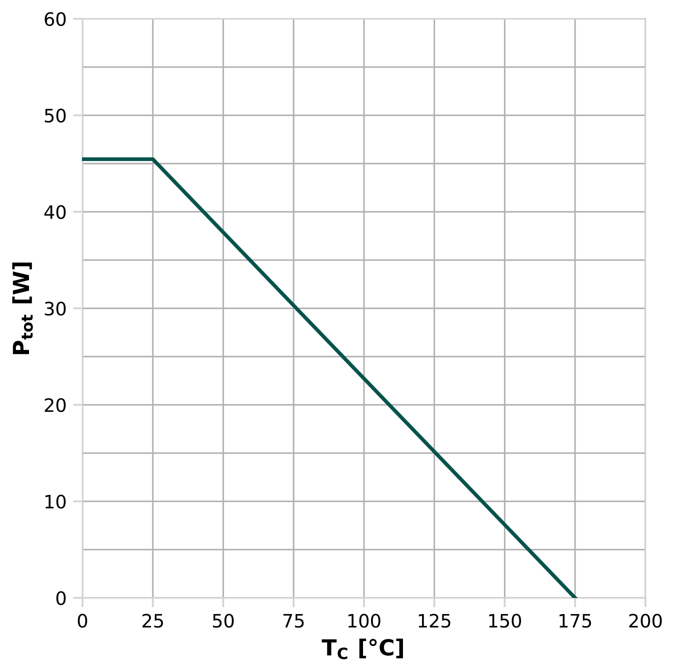
Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current [12]	I_S	-	-	27	A	T_C = 25 °C
Diode pulse current [12]	$I_{S,pulse}$	-	-	52	A	T_C = 25 °C, t_p = 100 µs
Diode forward voltage	V_{SD}	-	0.9	1	V	T_j = 25 °C, V_{GS} = 0 V, I_F = 14 A
Reverse recovery time [12]	t_{rr}	-	21	32	ns	di_F/dt =100 A/µs, V_R = 50 V, I_F = 27 A
Reverse recovery charge [12]	Q_{rr}		8	15	nC	

[12] The parameter is not subject to production testing - specified by design.

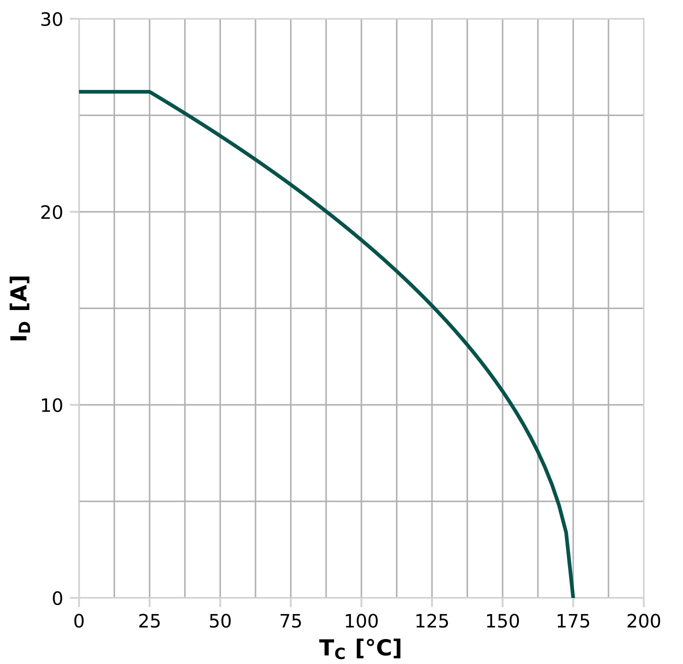
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



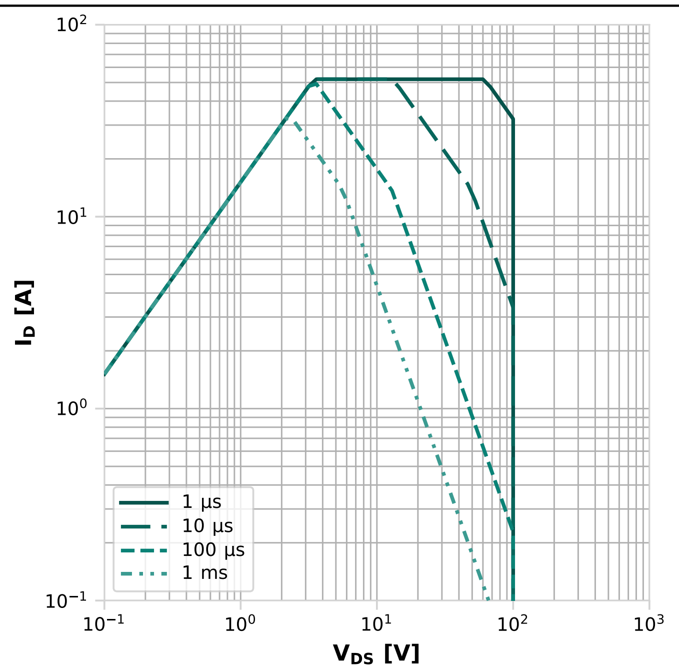
P_{tot}=f(T_C); $V_{GS} \geq 6$ V

Diagram 2: Drain Current



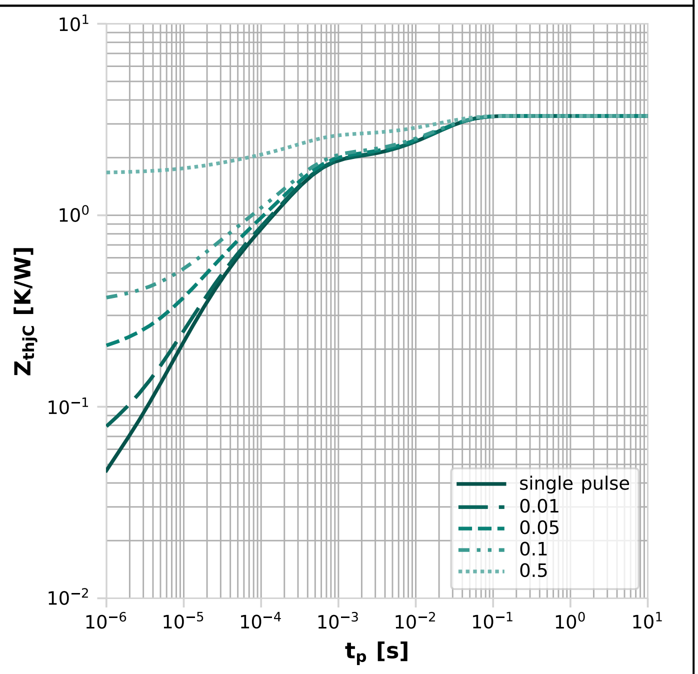
I_D=f(T_C); $V_{GS} \geq 6$V

Diagram 3: Safe operating area



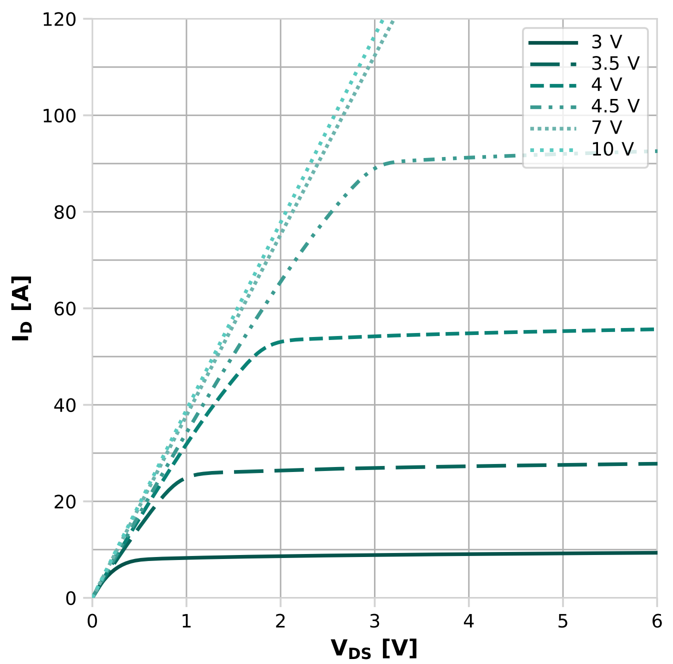
I_D=f(V_{DS}); T_C= 25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



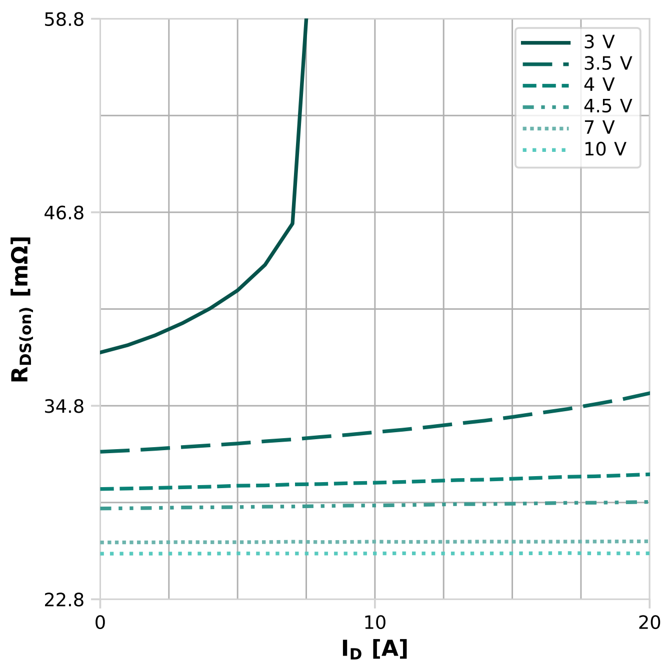
Z_{thjC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



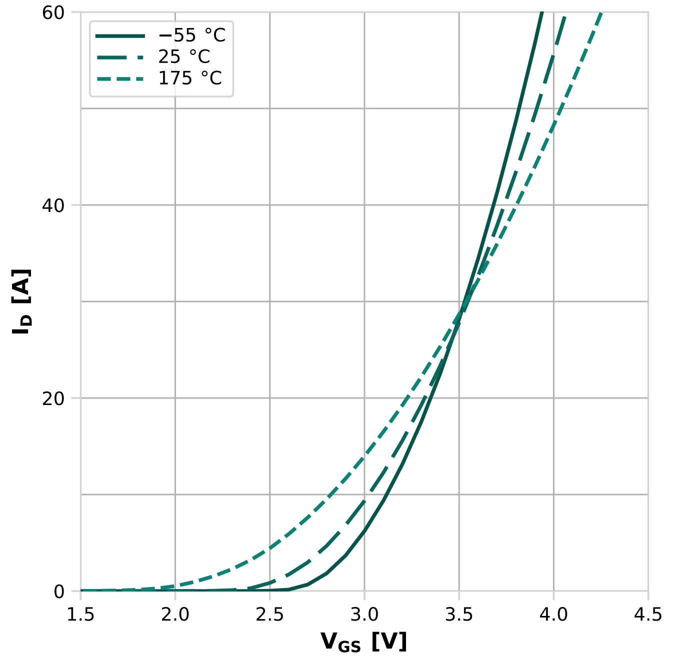
$I_D=f(V_{DS})$; T_j= 25 °C, parameter: V_{GS}

Diagram 6: Typ. drain-source on-state resistance



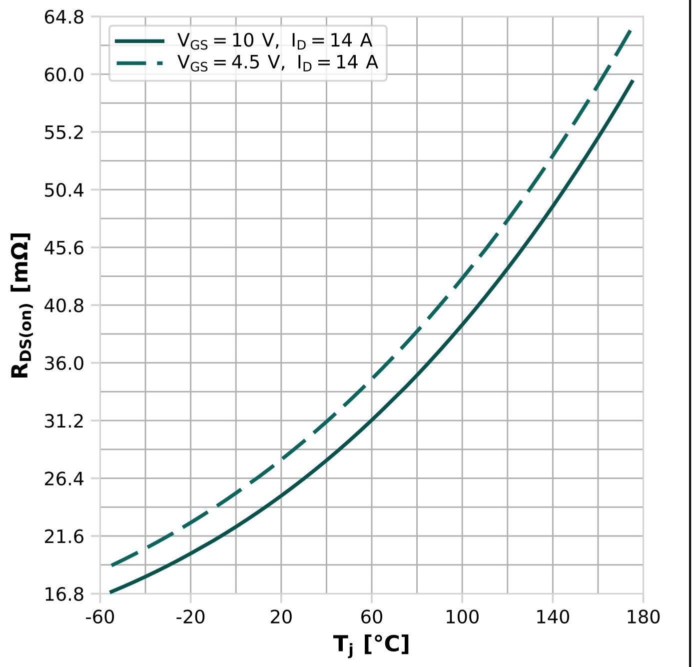
$R_{DS(on)}=f(I_D)$; T_j= 25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$; V_{DS}= 6 V; parameter: T_j

Diagram 8: Typ. drain-source on-state resistance



$R_{DS(on)}=f(T_j)$; parameter: I_D, V_{GS}

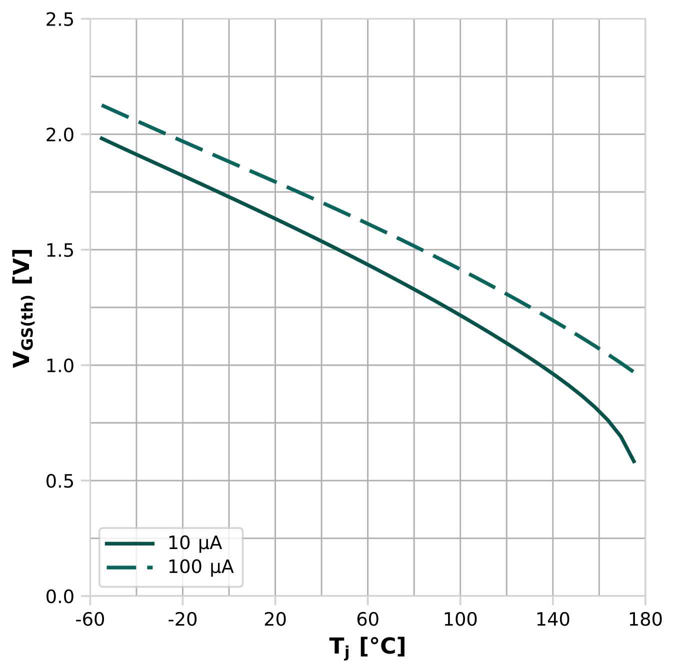
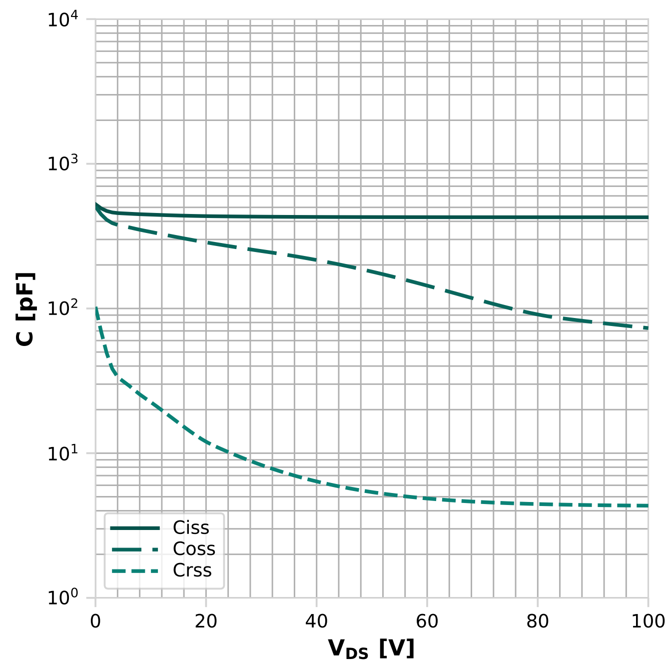
Diagram 9: Typ. gate threshold voltage	Diagram 10: Typ. capacitances
	
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D	$C=f(V_{DS})$; $V_{GS}=0$ V; f=1 MHz

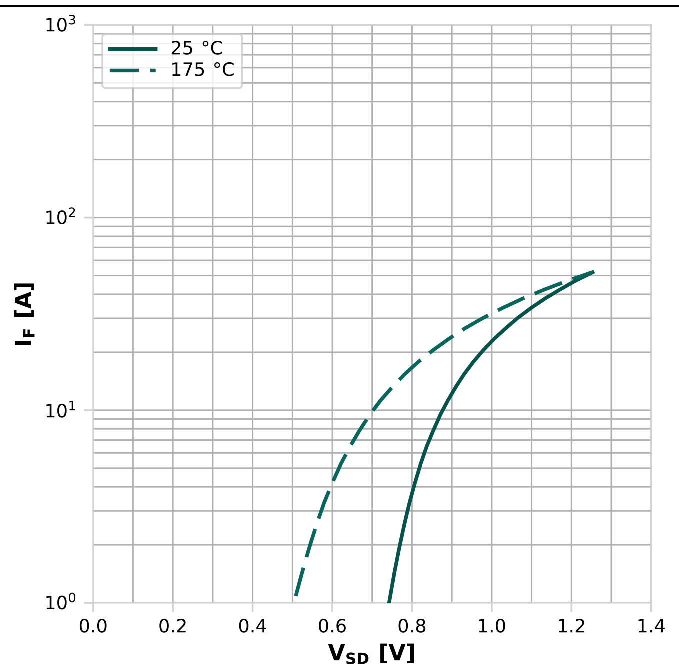
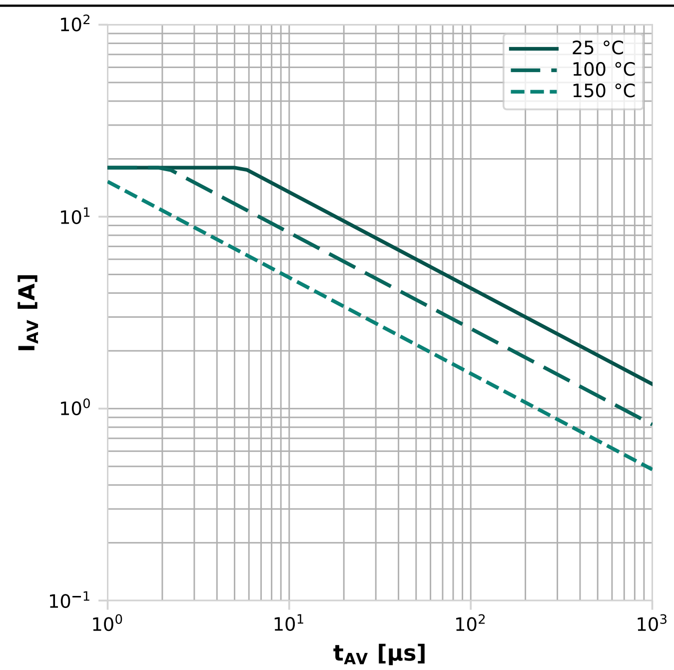
Diagram 11: Typ. forward diode characteristics	Diagram 12: Typ. avalanche characteristics
	
$I_F=f(V_{SD})$; parameter: T_j	$I_{AS}=f(t_{AV})$; parameter: $T_{j(start)}$

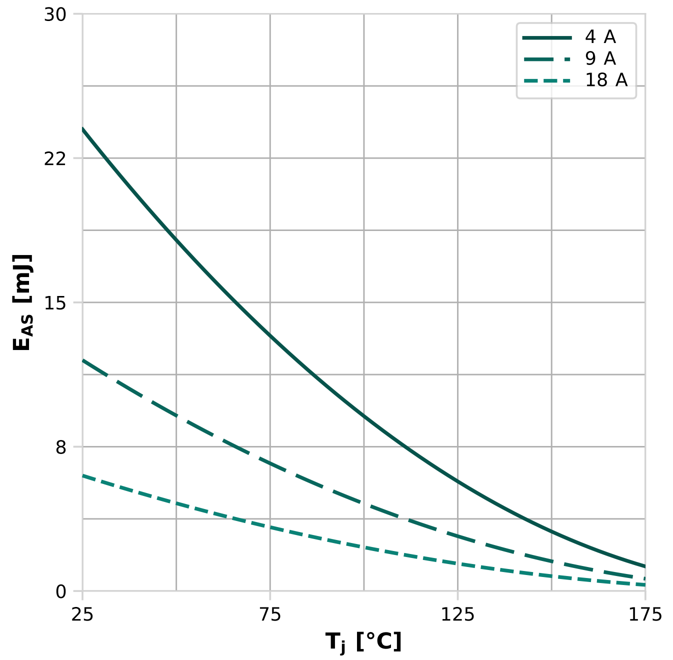
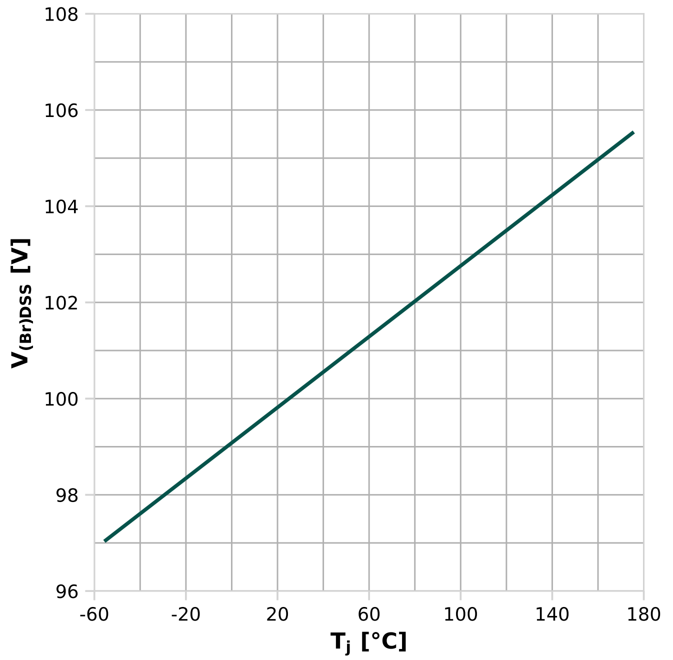
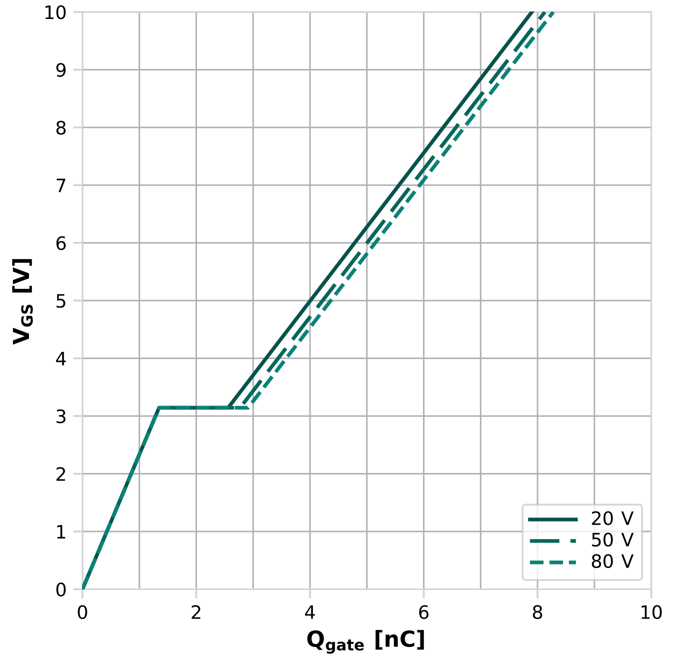
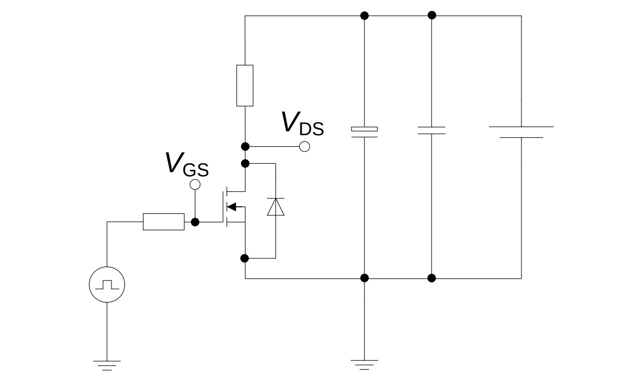
Diagram 13: Typical avalanche Energy	Diagram 14: Drain-source breakdown voltage
	
E_{AS}=f(T_j); parameter: I_D	$V_{(Br)DSS}$=f(T_j); I_D= 1 mA

Diagram 15: Typ. gate charge

V_{GS}=f(Q_{gate}); I_D= 14 A pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Switching times test circuit for resistive load

Switching times test circuit for resistive load



Switching times waveform

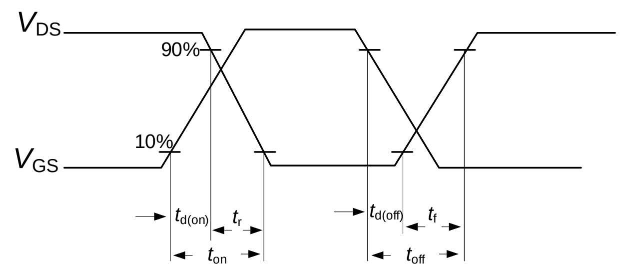
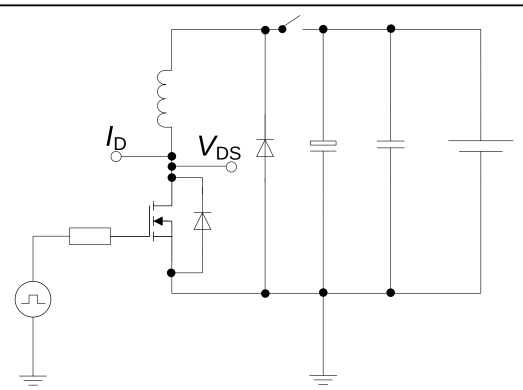


Table 9 Unclamped inductive load test circuit

Unclamped inductive load test circuit



Unclamped inductive waveform

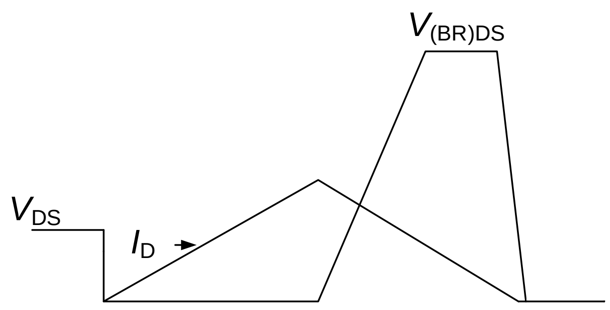
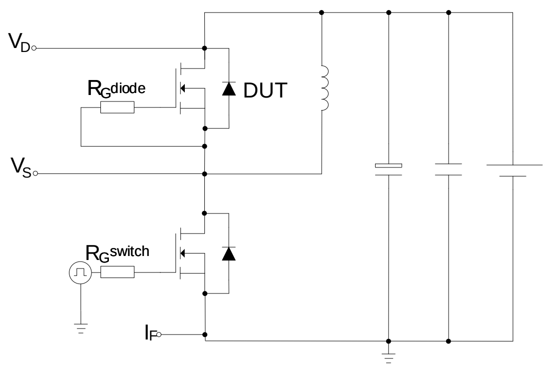
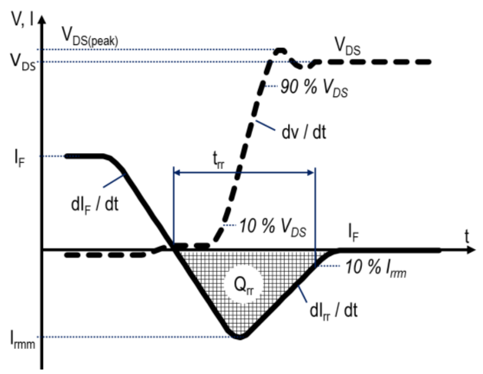


Table 10 Diode characteristics

Test circuit for diode characteristics



Diode recovery waveform



6 Package outlines

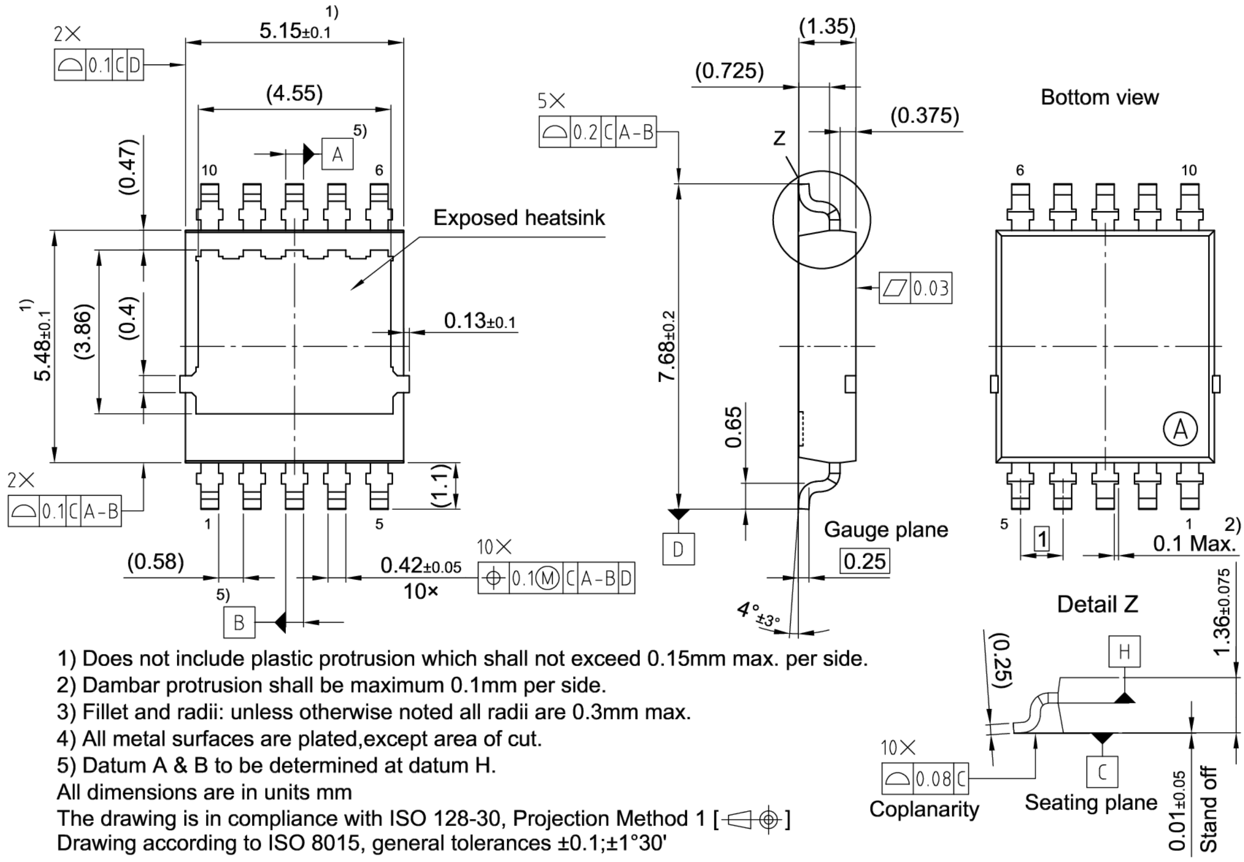


Figure 1 Outline PG-LHDSO-10, dimensions in mm

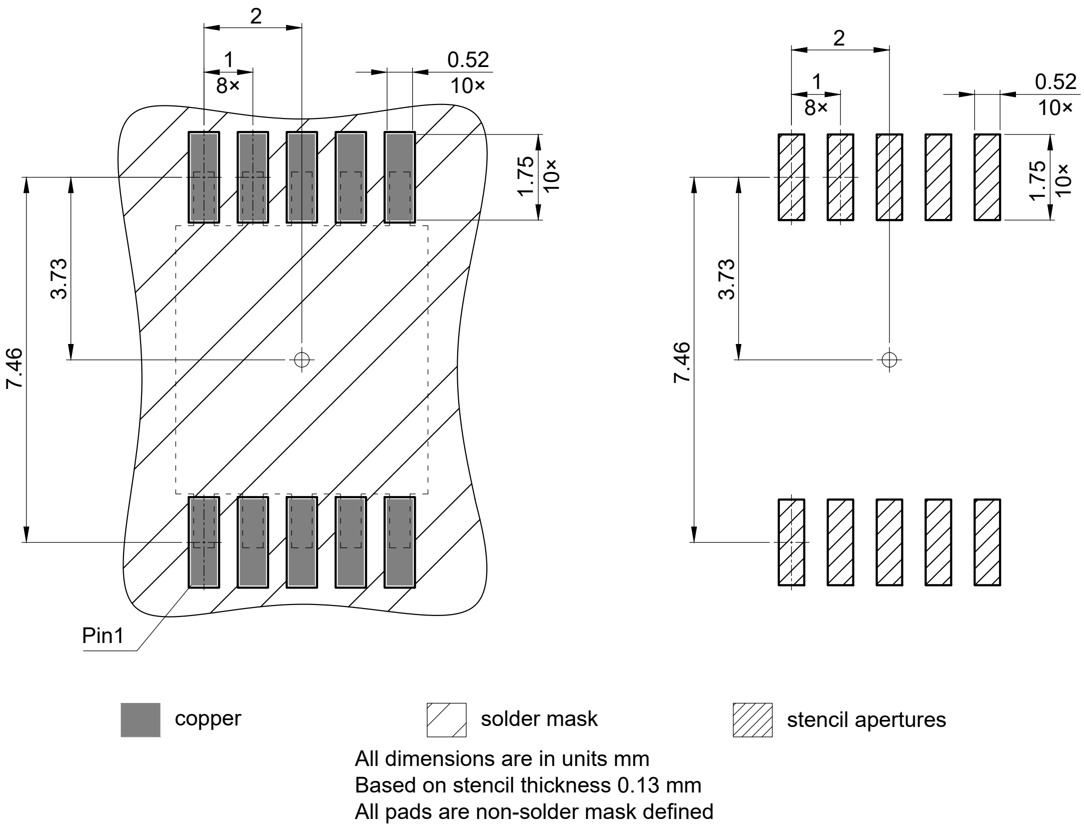
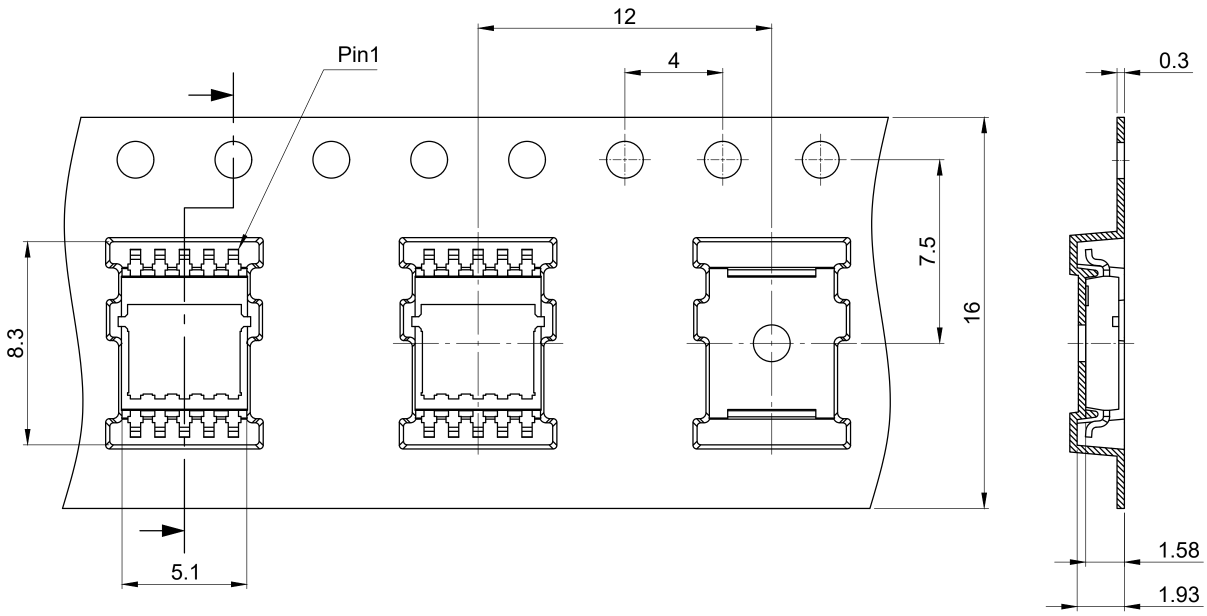


Figure 2 Footprint drawing PG-LHDSO-10, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Packaging variant PG-LHDSO-10, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUCN10S7L290T

Revision 2026-03-04, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-02-24	Final Data Sheet
1.1	2026-03-04	Corrected confidentiality level

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Published by Infineon Technologies AG, Am Campeon 1-15, 85579 Neubiberg, Germany

Important notice
Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features: Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit https://www.infineon.com.