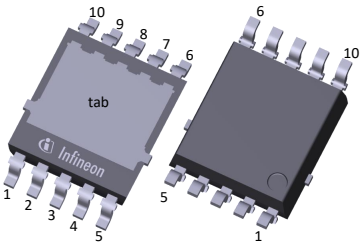
Automotive MOSFET

OptiMOS™ 5 Power-Transistor

PG-LHDSO-10



Features

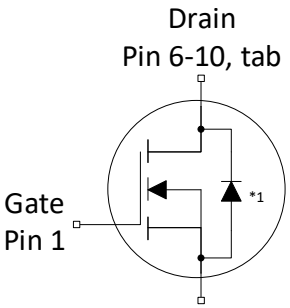
- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.



*1: Internal body diode

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	11.3	mΩ
I_D(chip limited)	61	A

AEC Qualified

Extended quality

RoHS

Part number	Package	Marking	Related links
IAUCN10S5L110T	PG-LHDSO-10	5A1	see Appendix A

Table of contents

1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	61	A	Chip limitation, V_{GS} = 10 V [1) 2)]
				61		DC current, V_{GS} = 10 V
				20		R_{thJA} on 2s2p, V_{GS} = 10 V, T_a = 100 °C [1) 3)]
Pulsed drain current [1)]	$I_{D,pulse}$	-	-	141	A	T_C = 25 °C, t_p = 100 µs
Avalanche energy, single pulse [1)]	E_{AS}	-	-	78	mJ	I_D = 12 A
Avalanche current, single pulse	I_{AS}	-	-	24	A	-
Gate source voltage	V_{GS}	-20		20	V	
Power dissipation	P_{tot}	-	-	88	W	T_C = 25 °C
Operating temperature	T_j	-55	-	175	°C	-

1) The parameter is not subject to production testing - specified by design.

2) The current is limited by the overall system design, including the customer-specific PCB.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [4]	R_{thJC}	-	-	1.69	K/W	-
Thermal characterization parameter, source pin [4] [5]	Ψ_{source}		13.5	-		
Thermal characterization parameter, drain pin [4] [6]	Ψ_{drain}		9.6	-		
Thermal resistance, junction - heatsink [4] [7]	R_{thJH}		8.2	-		
Thermal resistance, junction - ambient [4] [8]	R_{thJA}		47.2	-		

[4] The parameter is not subject to production testing - specified by design.

[5] Thermal characterization parameter, calculated as $\Psi_{source} = (T_{source} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at source pins for given power.

[6] Thermal characterization parameter, calculated as $\Psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at drain pins for given power.

[7] Device on 2s2p FR4 PCB defined in acc. with JEDEC standards (JESD51-5,-7) without thermal vias, heat sink of 71 x 110 x 2 mm is attached through TIM with 3.3 W/(m*K) and 400 µm thickness to top side pad. Heatsink fixed to 85°C ambient temperature.

[8] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	I_D = 1 mA, V_{GS} = 0 V
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.2	V	V_{DS}=V_{GS}, I_D = 30 µA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS} = 100 V, T_j = 25 °C, V_{GS} = 0 V
				20		V_{DS} = 100 V, T_j = 100 °C, V_{GS} = 0 V [9]
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{DS} = 0 V, V_{GS} = 20 V
Drain-source on-state resistance	$R_{DS(on)}$	-	14.6	17.8	mΩ	I_D = 31 A, V_{GS} = 4.5 V
			10.7	11.3		I_D = 31 A, V_{GS} = 10 V
Gate resistance [9]	R_G	-	1.1	-	Ω	-

[9] The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [10]	C_{iss}	-	1340	1740	pF	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance [10]	C_{oss}		230	300		
Reverse transfer capacitance [10]	C_{rss}		12	18		
Turn-on delay time [10]	$t_{d(on)}$	-	4	-	ns	I_D = 31 A, V_{GS} = 10 V, V_{DD} = 50 V, R_G = 3.5 Ω
Rise time [10]	t_r		6			
Turn-off delay time [10]	$t_{d(off)}$		12			
Fall time [10]	t_f		12			

[10] The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge [11]	Q_{gs}	-	4.4	6	nC	I_D = 31 A, V_{DS} = 50 V, V_{GS} = 0 V to 10 V
Gate to drain charge [11]	Q_{gd}		4	6	nC	
Gate charge total [11]	Q_g		20	25	nC	
Gate plateau voltage [11]	$V_{plateau}$		3.3	-	V	

[11] The parameter is not subject to production testing - specified by design.

Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current [12]	I_S	-	-	61	A	T_C = 25 °C
Diode pulse current [12]	$I_{S,pulse}$	-	-	141	A	T_C = 25 °C, t_p = 100 µs
Diode forward voltage	V_{SD}	-	0.9	1.1	V	T_j = 25 °C, V_{GS} = 0 V, I_F = 31 A
Reverse recovery time [12]	t_{rr}	-	28	42	ns	di_F/dt =100 A/µs, V_R = 50 V, I_F = 50 A
Reverse recovery charge [12]	Q_{rr}		19	38	nC	

[12] The parameter is not subject to production testing - specified by design.

4 Electrical characteristics diagrams

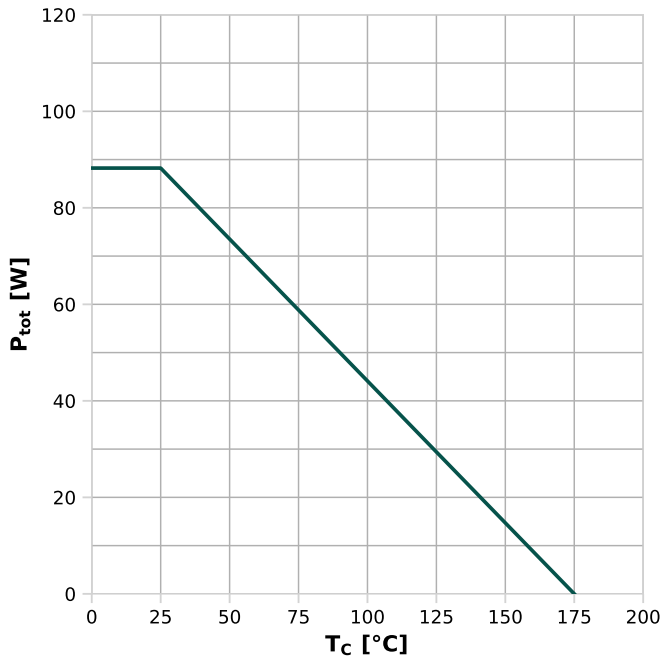
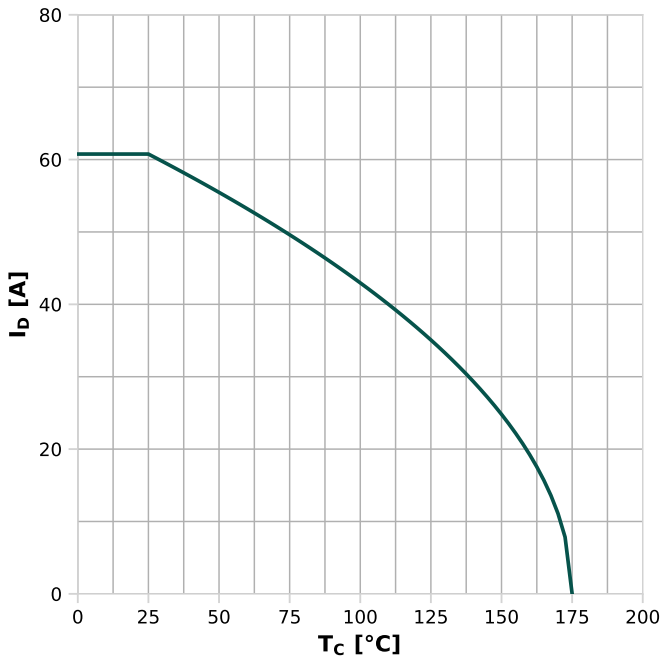
Diagram 1: Power dissipation	Diagram 2: Drain Current
	
$P_{tot}=f(T_C)$; $V_{GS} \geq 6$ V	$I_D=f(T_C)$; $V_{GS} \geq 6$V

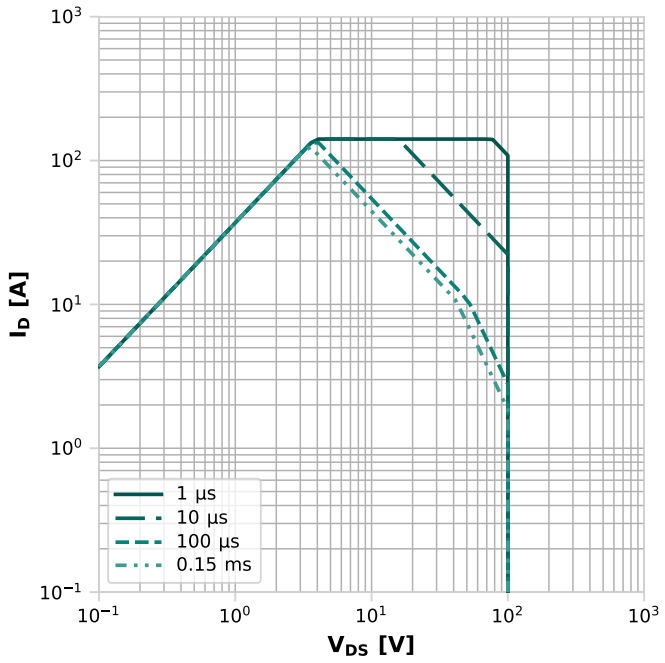
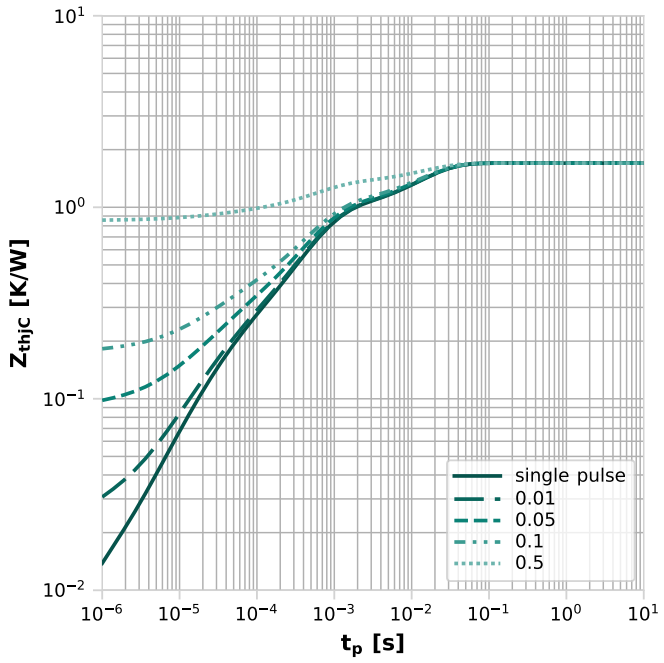
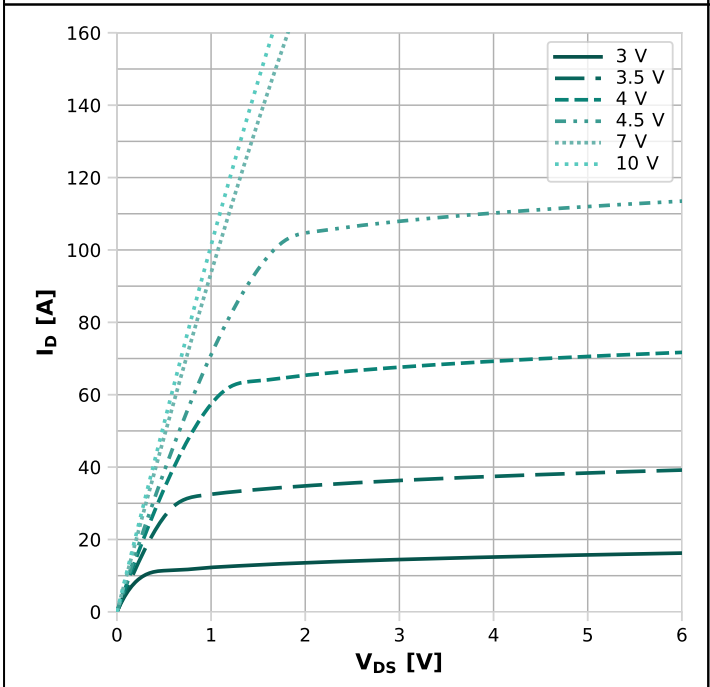
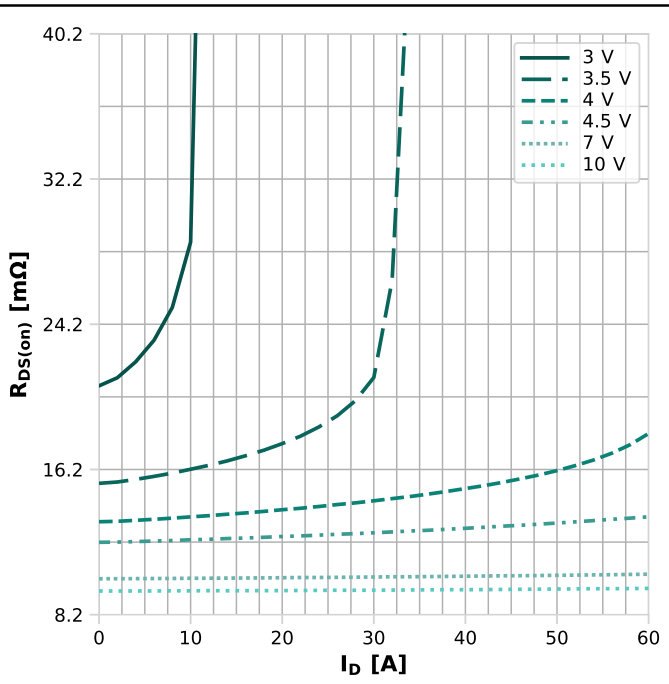
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
$I_D=f(V_{DS})$; T_C= 25 °C; D=0; parameter: t_p	$Z_{thjC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



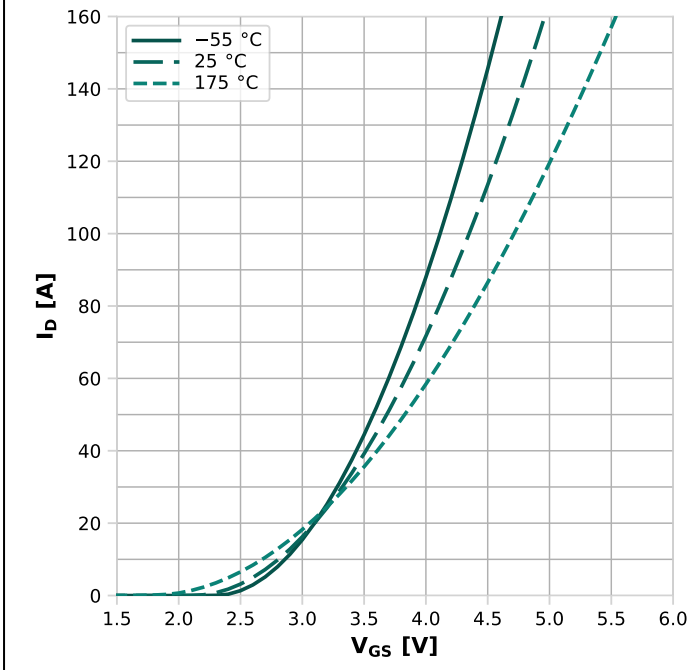
$I_D=f(V_{DS})$; T_j= 25 °C, parameter: V_{GS}

Diagram 6: Typ. drain-source on-state resistance



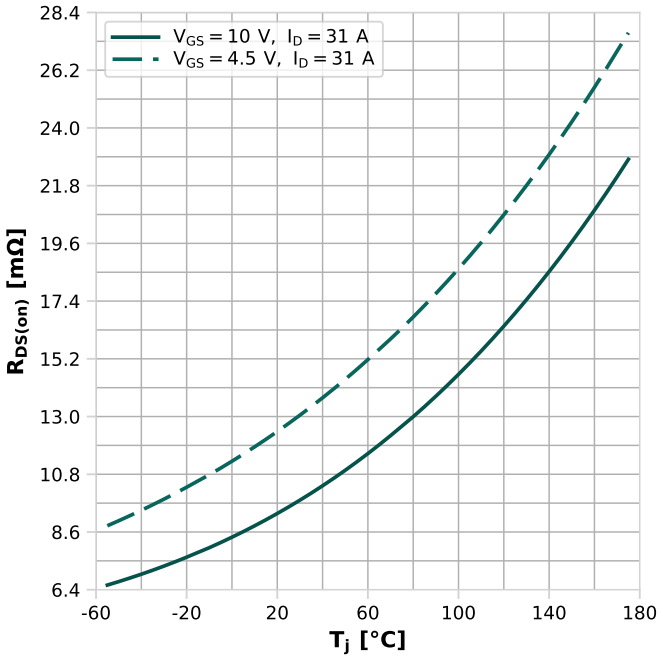
$R_{DS(on)}=f(I_D)$; T_j= 25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$; V_{DS}= 6 V; parameter: T_j

Diagram 8: Typ. drain-source on-state resistance



$R_{DS(on)}=f(T_j)$; parameter: I_D, V_{GS}

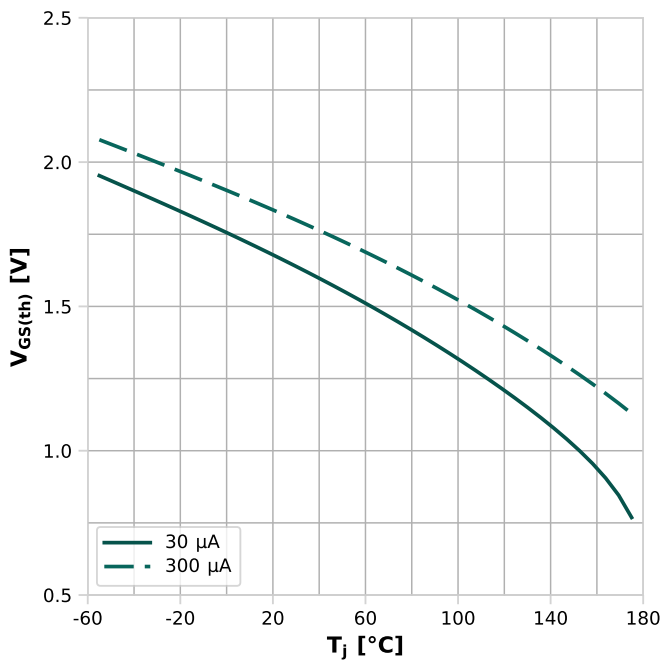
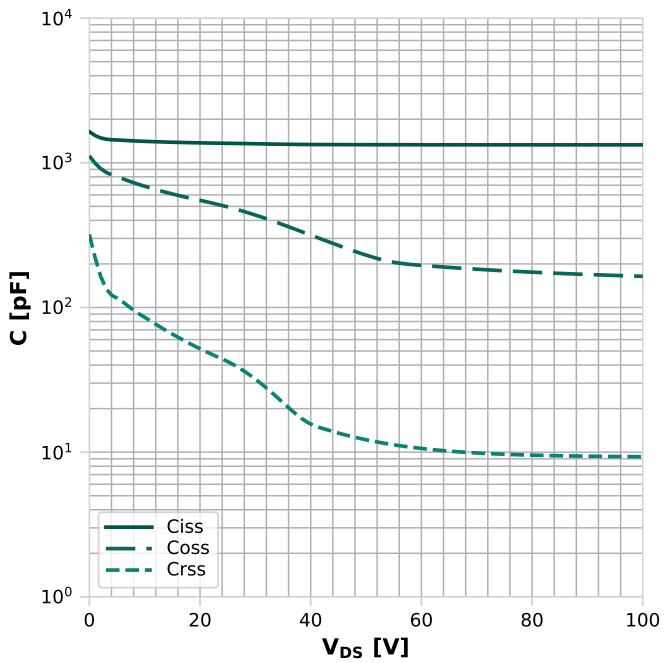
Diagram 9: Typ. gate threshold voltage	Diagram 10: Typ. capacitances
	
$V_{GS(th)}=f(T_j)$; $V_{GS}= V_{DS}$; parameter: I_D	$C=f(V_{DS})$; $V_{GS}= 0$ V; f=1 MHz

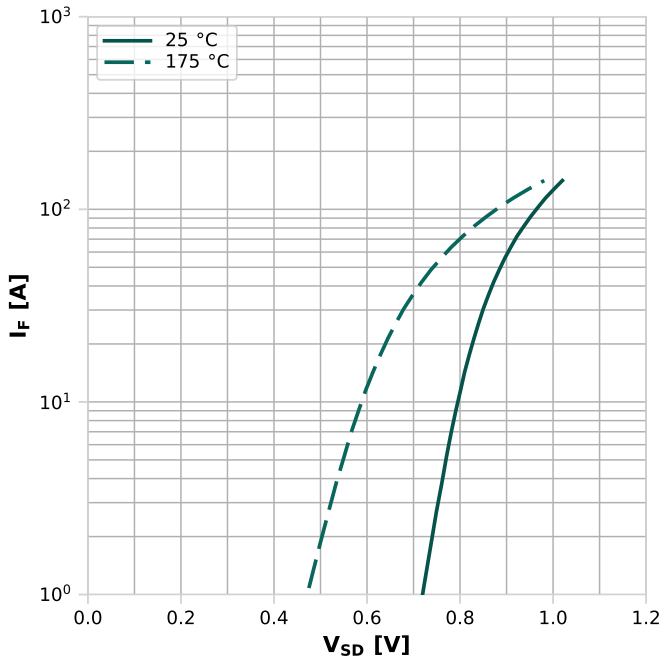
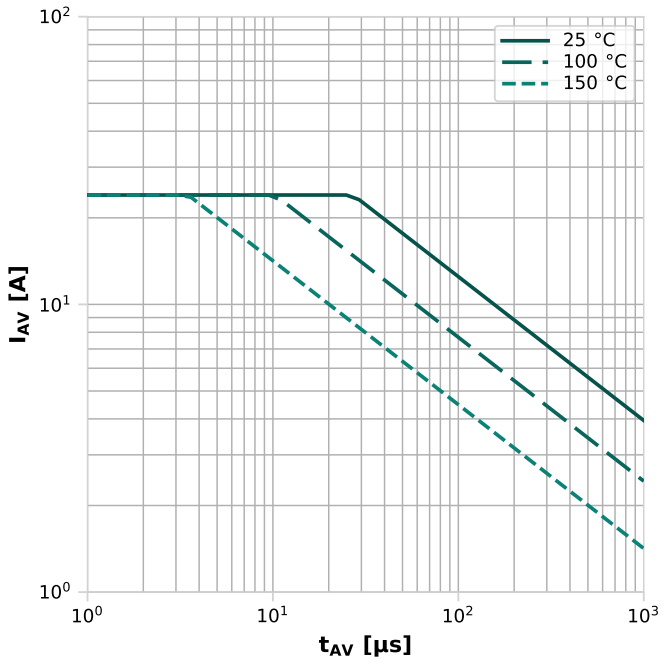
Diagram 11: Typ. forward diode characteristics	Diagram 12: Typ. avalanche characteristics
	
$I_F=f(V_{SD})$; parameter: T_j	$I_{AS}=f(t_{AV})$; parameter: $T_{j(start)}$

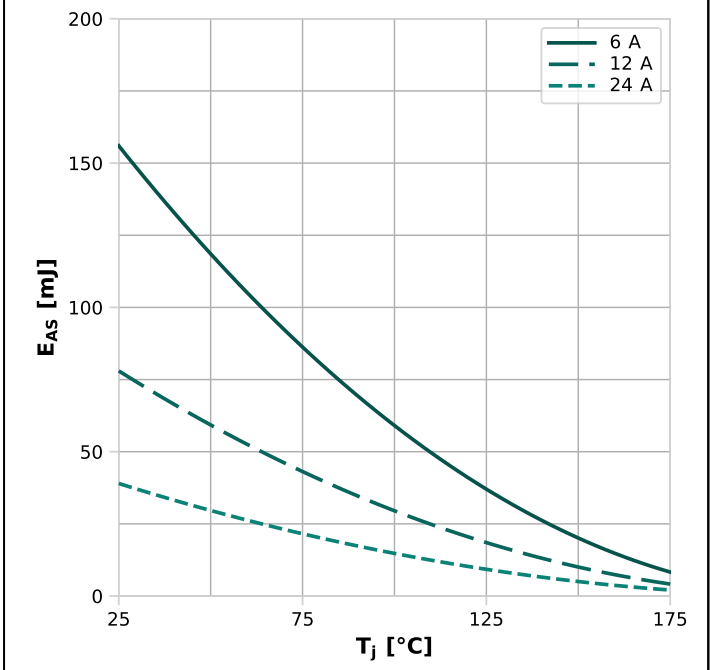
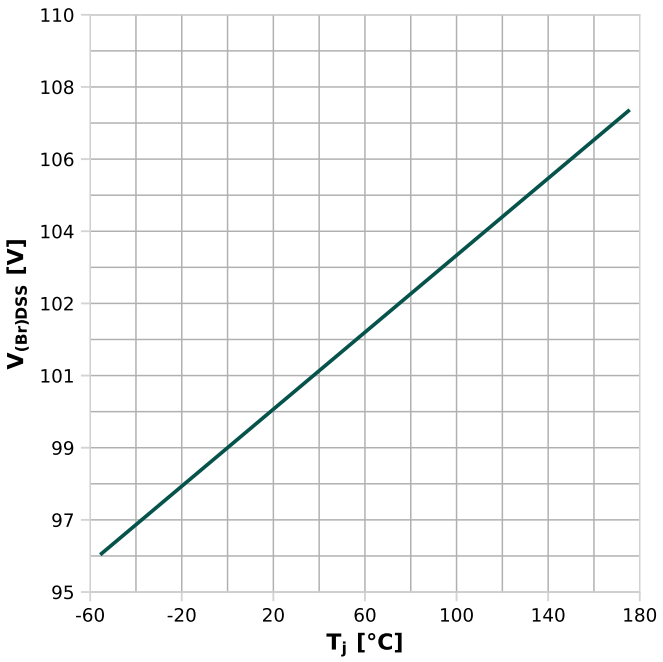
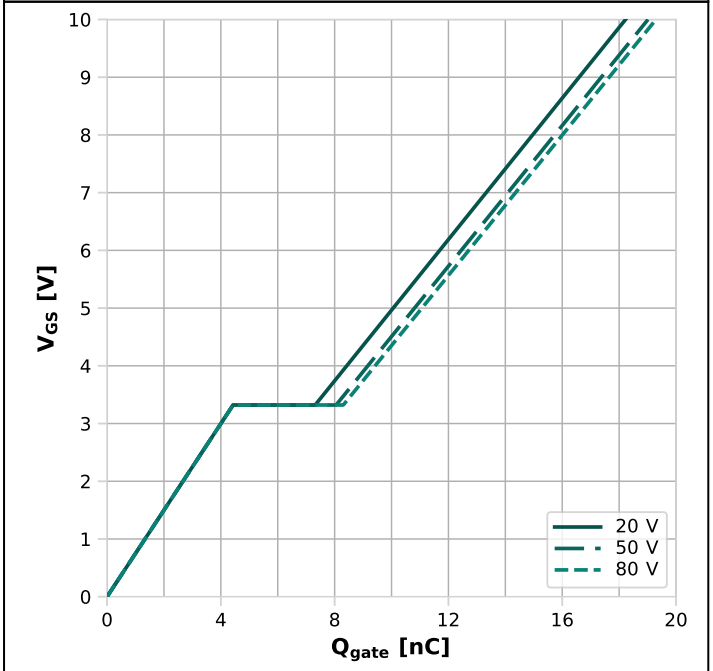
Diagram 13: Typical avalanche Energy	Diagram 14: Drain-source breakdown voltage
	
$E_{AS}=f(T_j)$; parameter: I_D	$V_{(Br)DSS}=f(T_j)$; I_D= 1 mA

Diagram 15: Typ. gate charge

$V_{GS}=f(Q_{gate})$; I_D= 31 A pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Switching times test circuit for resistive load

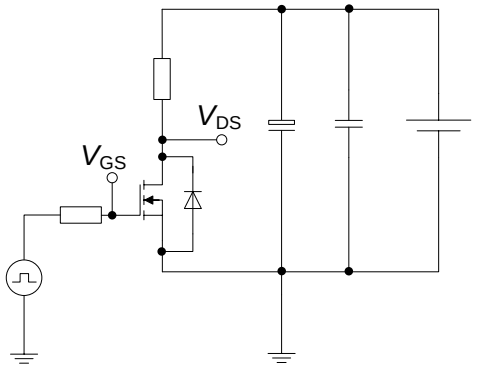
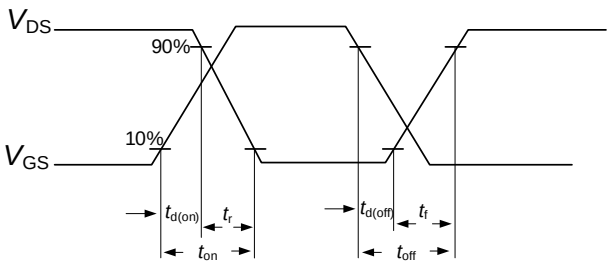
Switching times test circuit for resistive load	Switching times waveform
	

Table 9 Unclamped inductive load test circuit

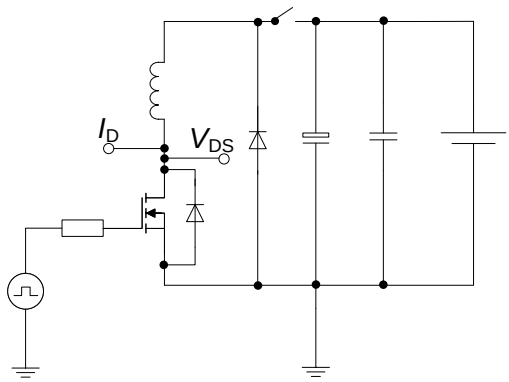
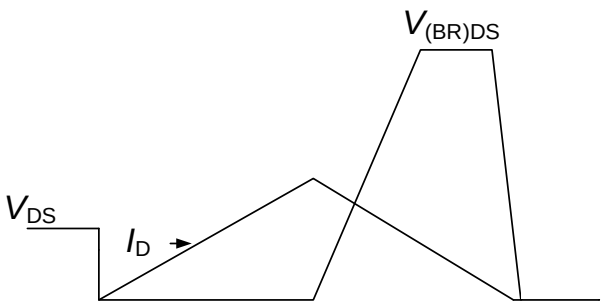
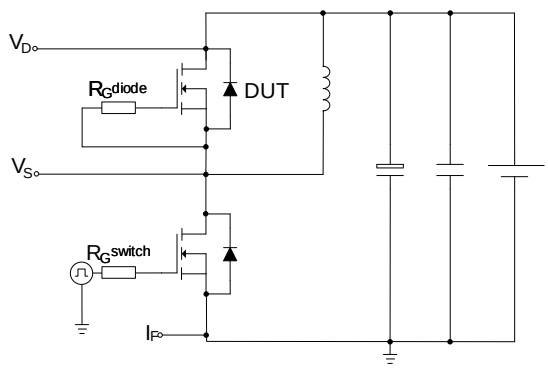
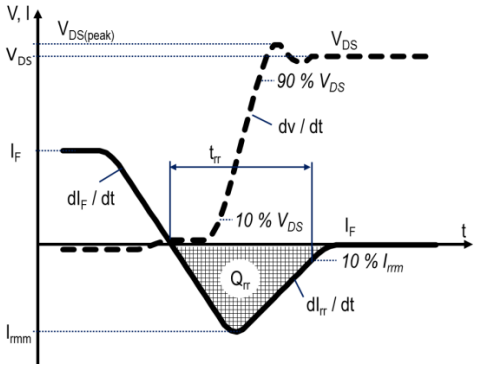
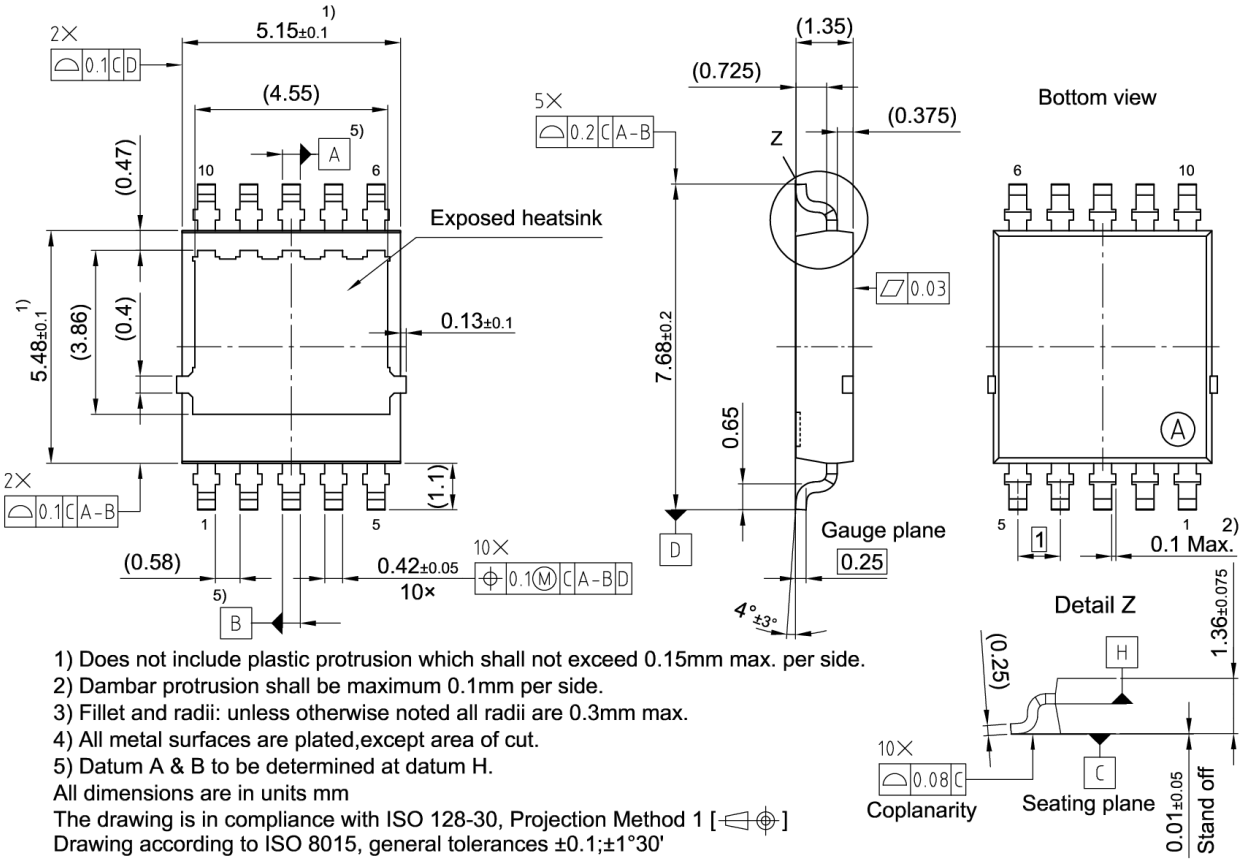
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 10 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

6 Package outlines



1) Does not include plastic protrusion which shall not exceed 0.15mm max. per side.
2) Dambar protrusion shall be maximum 0.1mm per side.
3) Fillet and radii: unless otherwise noted all radii are 0.3mm max.
4) All metal surfaces are plated,except area of cut.
5) Datum A & B to be determined at datum H.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]
Drawing according to ISO 8015, general tolerances ±0.1;±1°30'

Figure 1 Outline PG-LHDSO-10, dimensions in mm

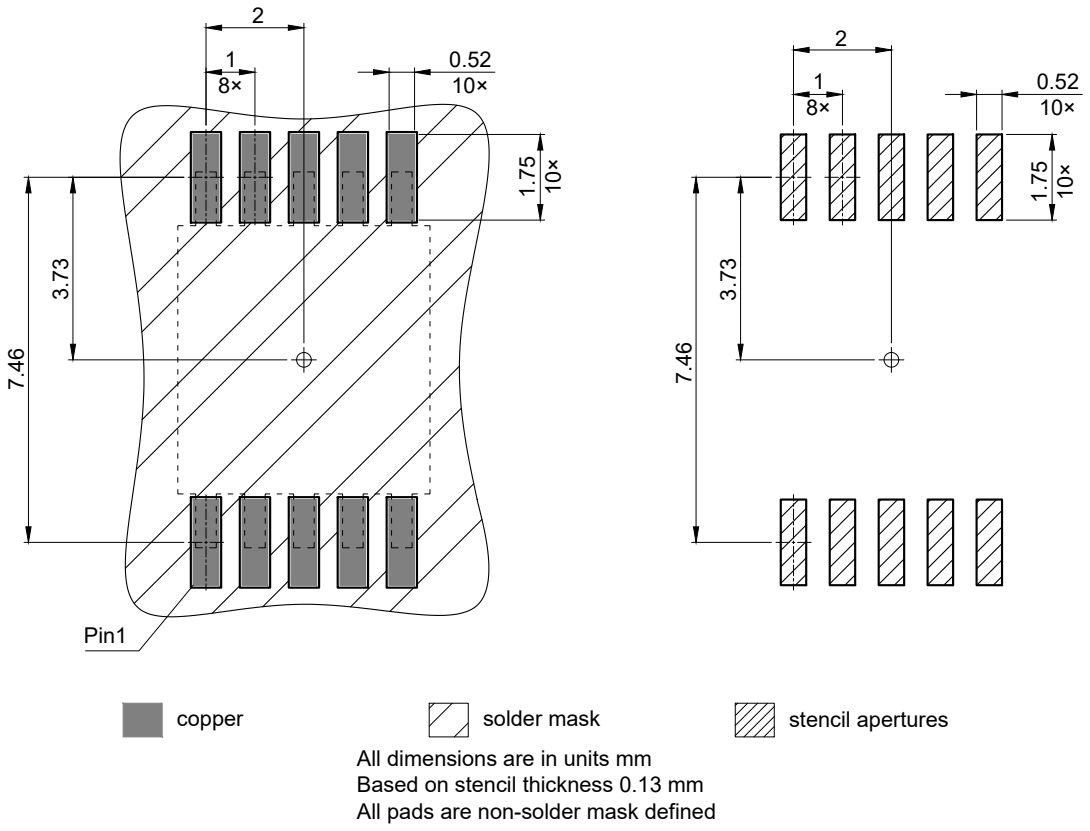


Figure 2 Footprint drawing PG-LHDSO-10, dimensions in mm

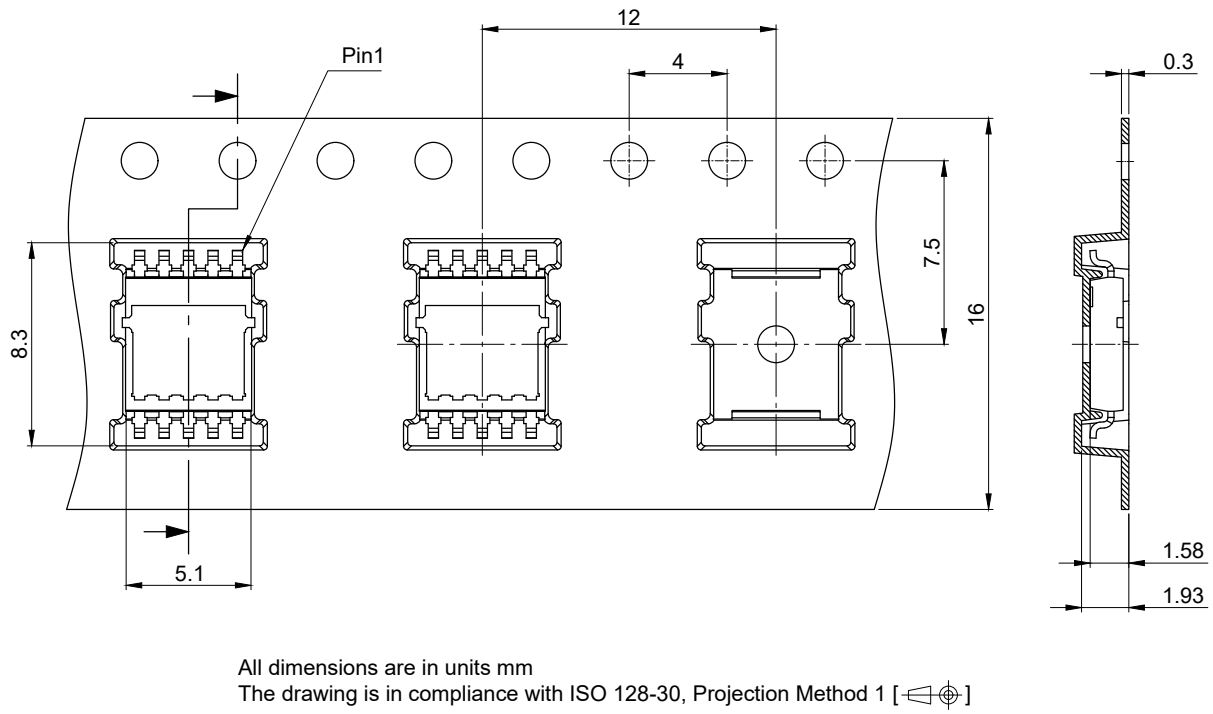


Figure 3 Packaging variant PG-LHDSO-10, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUCN10S5L110T

Revision 2026-03-04, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-02-24	Final Data Sheet
1.1	2026-03-04	Corrected confidentiality level

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