Automotive MOSFET

OptiMOS™ 7 Power-Transistor

RoHS

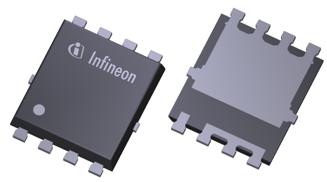
Infineon Automotive Quality

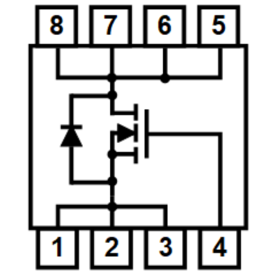
AEC Qualified

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

PG-TDSON-8-34





Potential Applications

General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	3.3	mΩ
I_D (chip limited)	130	A

Type	**Package**	**Marking**
IAUCN08S7L033	PG-TDSON-8-34	7N08L033

Table of Contents

Maximum Ratings

at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS} = 10 V, Chip limitation[1,2]	130	A
		V_{GS} = 10 V, DC current	120	
		T_a = 100°C, V_{GS} = 10 V, R_{thJA} on 2s2p[2,3]	20	
Pulsed drain current[2]	$I_{D,pulse}$	T_C = 25°C, t_p = 100 µs	356	
Avalanche energy, single pulse[2]	E_{AS}	I_D = 44 A	65.9	mJ
Avalanche current, single pulse	I_{AS}	–	87	A
Gate source voltage	V_{GS}	–	±16	V
		Limited to duty factor of 1%	+20	
Power dissipation	P_{tot}	T_C = 25°C	118	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal Characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	1.3	K/W
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	26.2	–	

Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static Characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 48 µA	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V, T_j = 25°C	–	–	1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_j = 100°C[2)]	–	–	12	
Gate-source leakage current	I_{GSS}	V_{GS} = 16 V, V_{DS} = 0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 60 A	–	3.6	4.6	mΩ
		V_{GS} = 10 V, I_D = 60 A	–	3.0	3.3	
Gate resistance[2)]	R_G	–	–	1.1	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics[2]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz	–	2708	3521	pF
Output capacitance	C_{oss}		–	1055	1372	
Reverse transfer capacitance	C_{rss}		–	15	23	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 40 V, V_{GS} = 10 V, I_D = 60 A, R_G = 3.5 Ω	–	6.1	–	ns
Rise time	t_r		–	5.9	–	
Turn-off delay time	$t_{d(off)}$		–	31.3	–	
Fall time	t_f		–	14.0	–	

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD} = 40 V, I_D = 60 A, V_{GS} = 0 to 10 V	–	8.1	10.6	nC
Gate to drain charge	Q_{gd}		–	6.5	9.9	
Gate charge total	Q_g		–	44.3	57.6	
Gate plateau voltage	$V_{plateau}$		–	3.0	–	V

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Reverse Diode						
Diode continuous forward current[2]	I_S	T_C = 25°C	–	–	120	A
Diode pulse current[2]	$I_{S,pulse}$	T_C = 25°C, t_p = 100 µs	–	–	356	
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 60 A, T_j = 25°C	–	0.9	1.0	V
Reverse recovery time[2]	t_{rr}	V_R = 40 V, I_F = 50 A, di_F/dt = 100 A/µs	–	26	39	ns
Reverse recovery charge[2]	Q_{rr}		–	11	22	nC

1) Practically the current is limited by the overall system design including the customer-specific PCB.

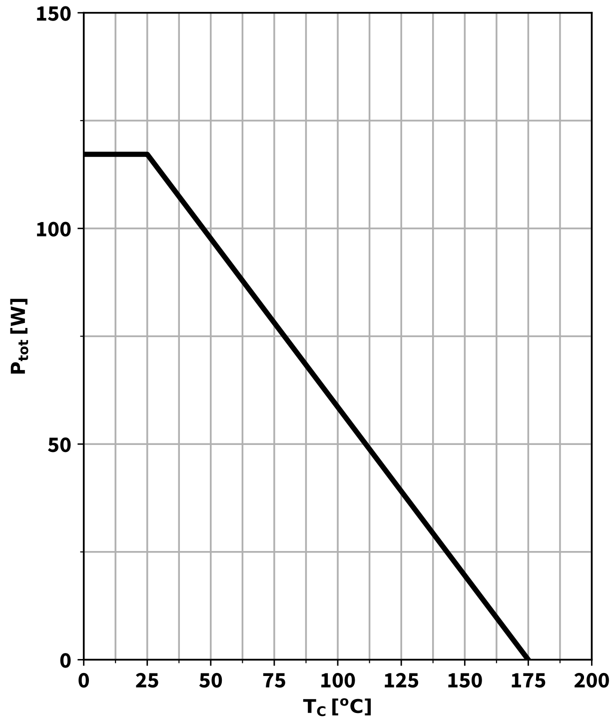
2) The parameter is not subject to production testing – specified by design.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

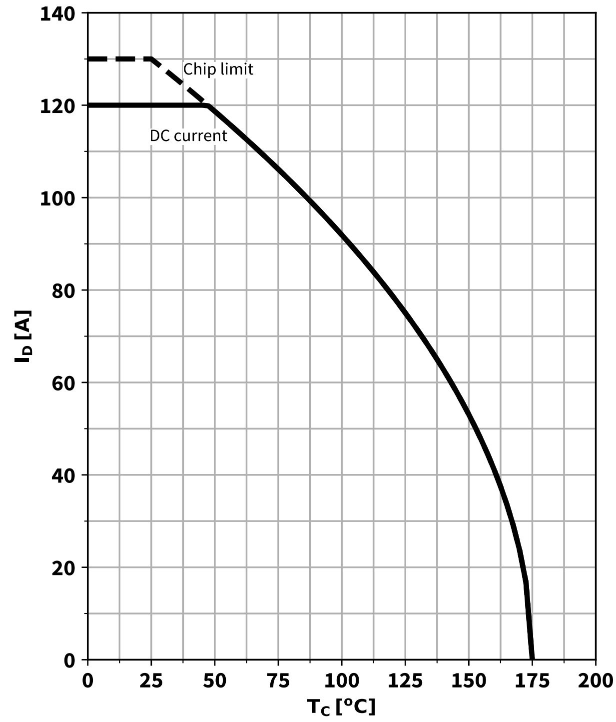
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



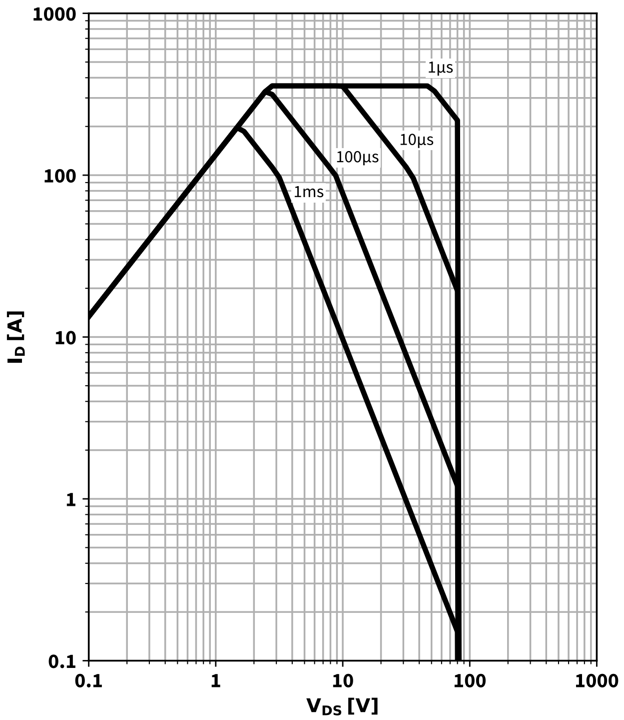
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



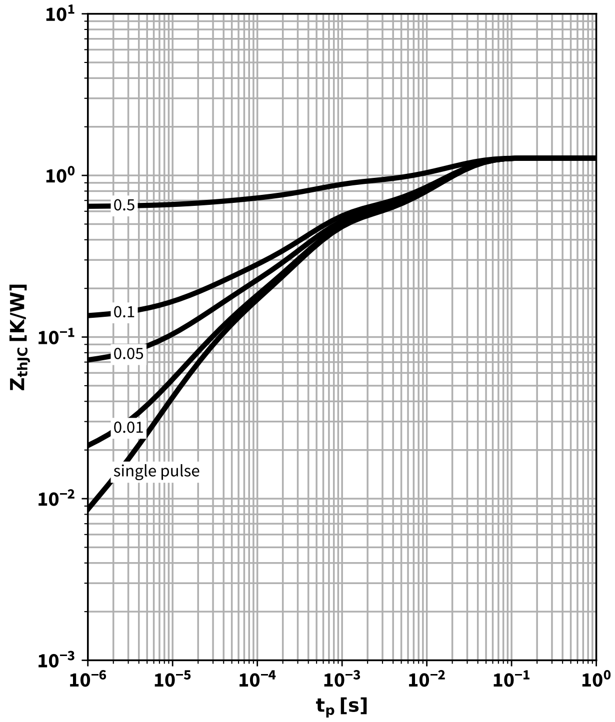
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



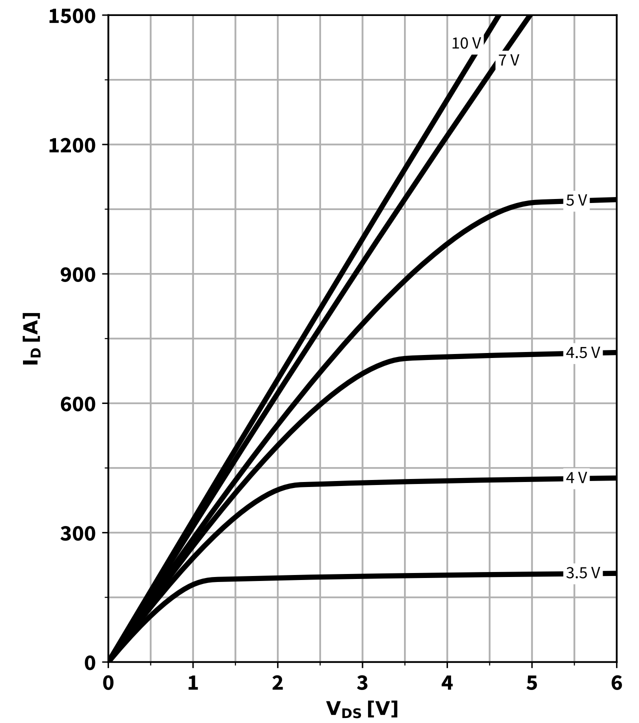
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



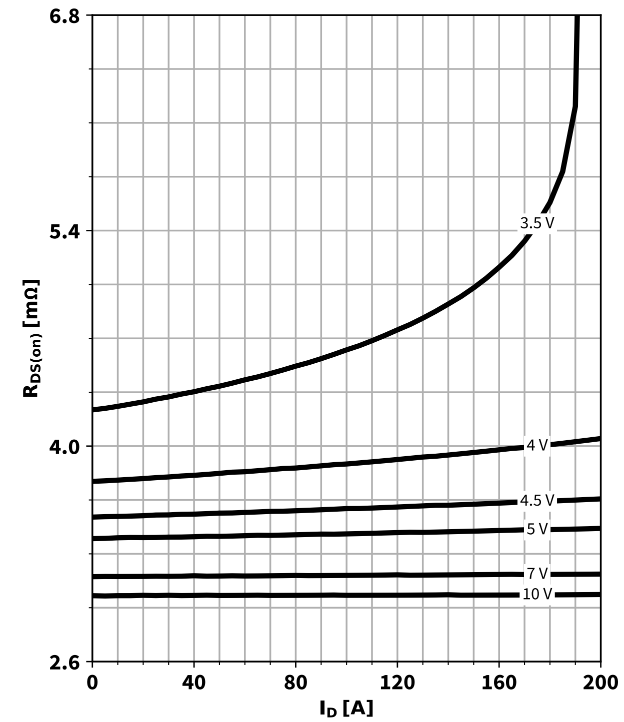
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



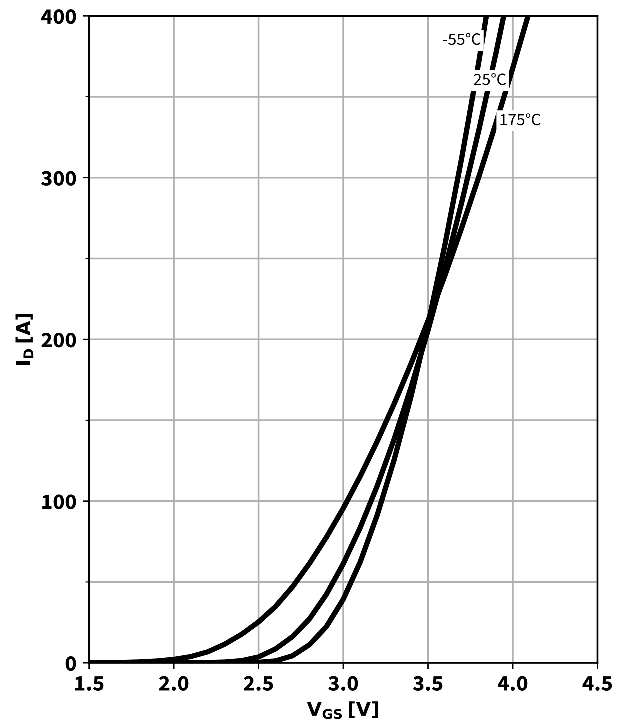
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



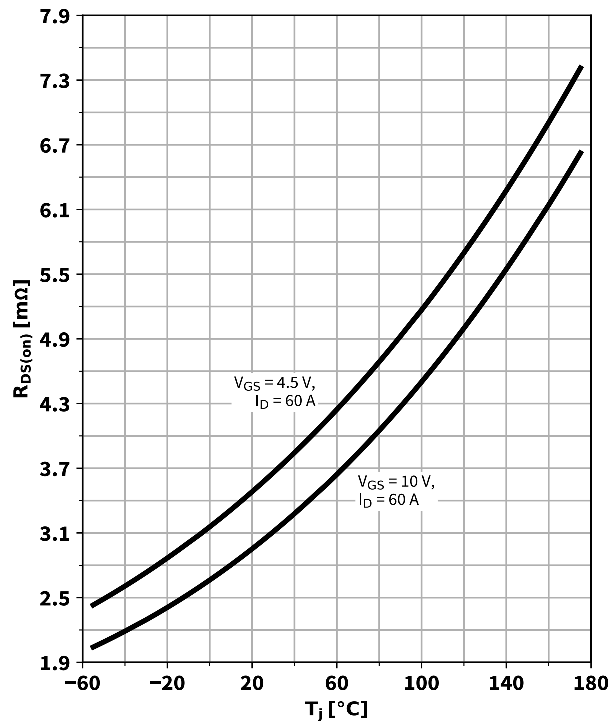
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$ V; parameter: T_j



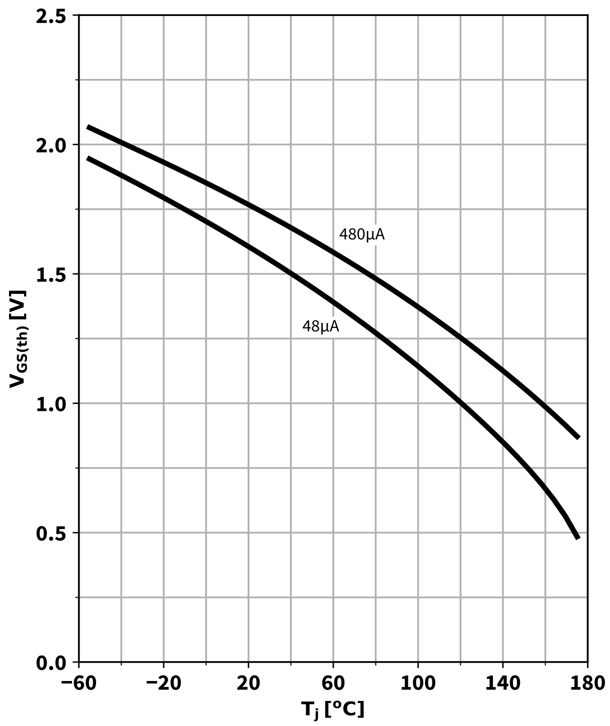
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



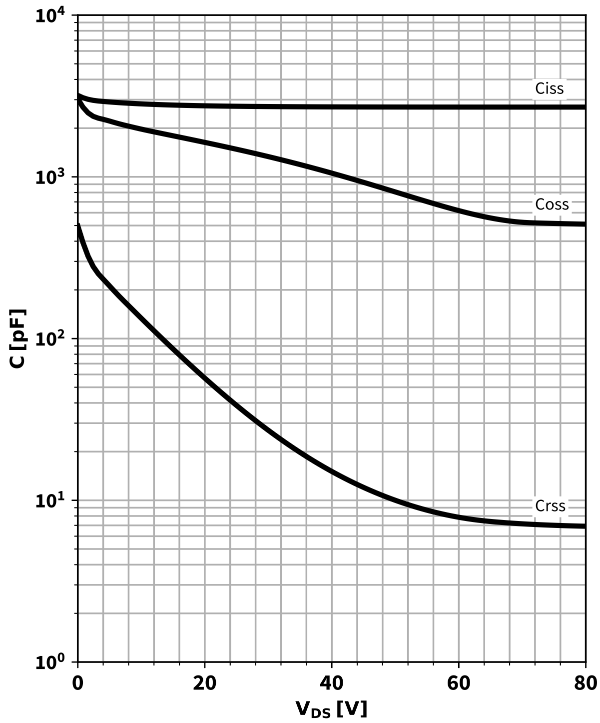
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



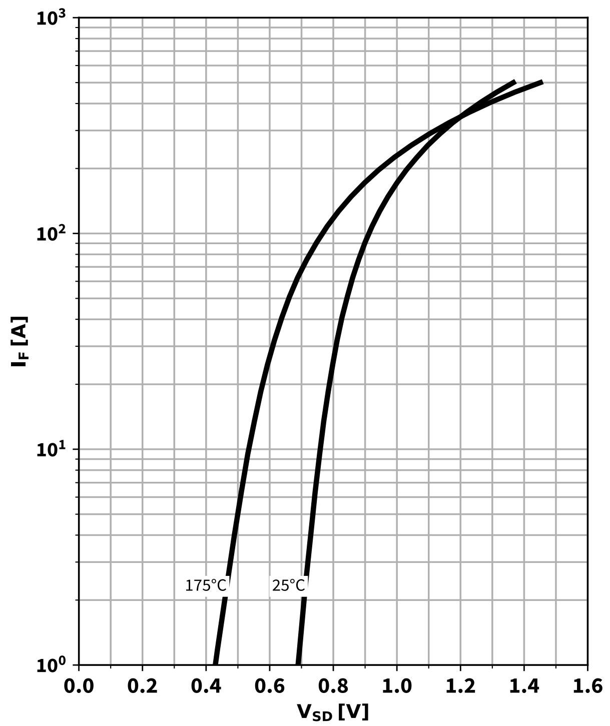
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



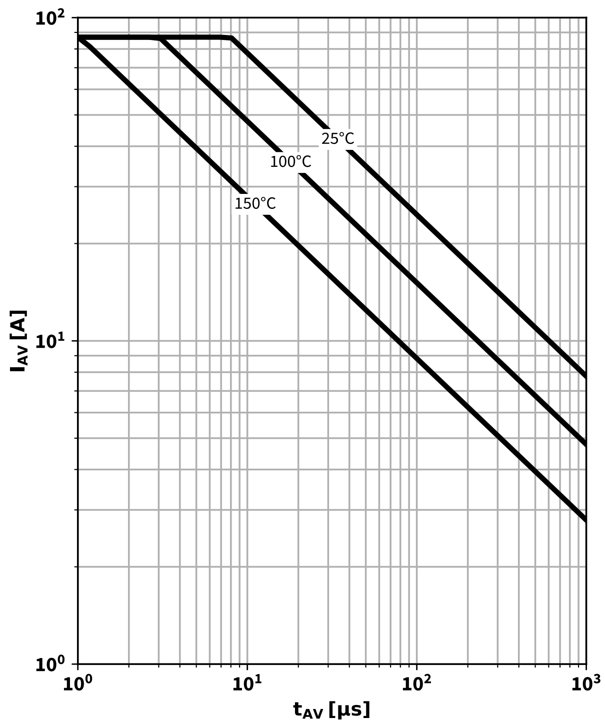
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



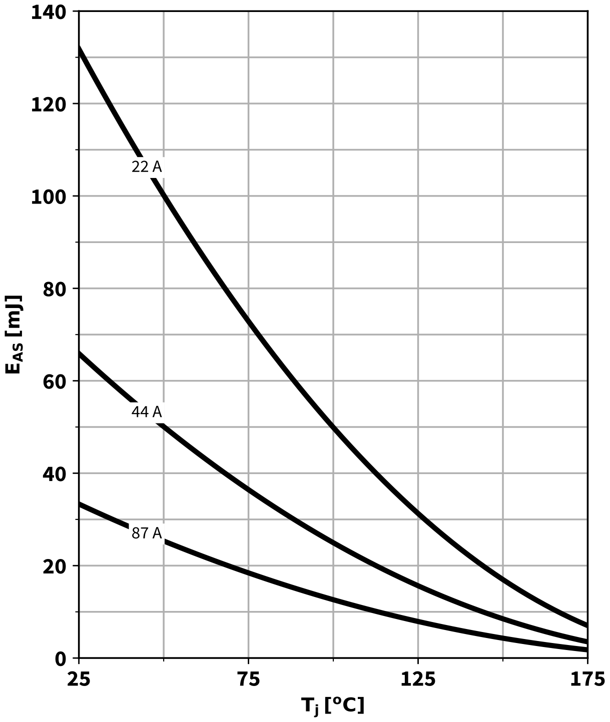
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



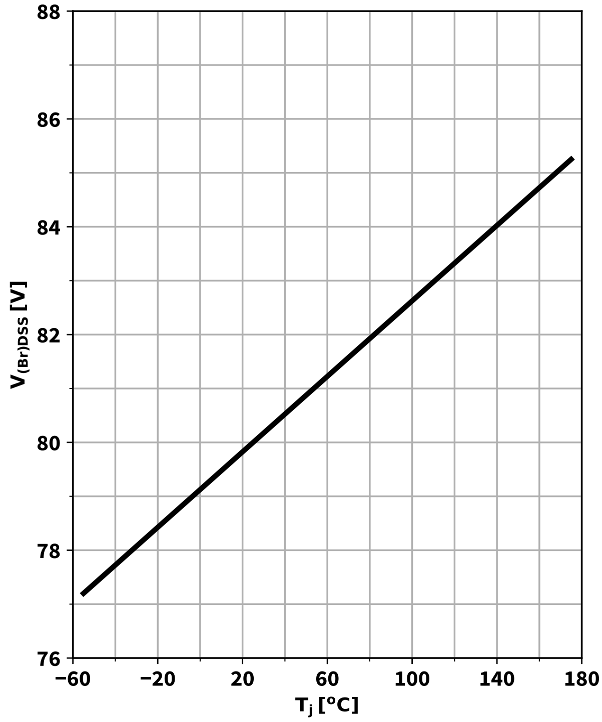
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



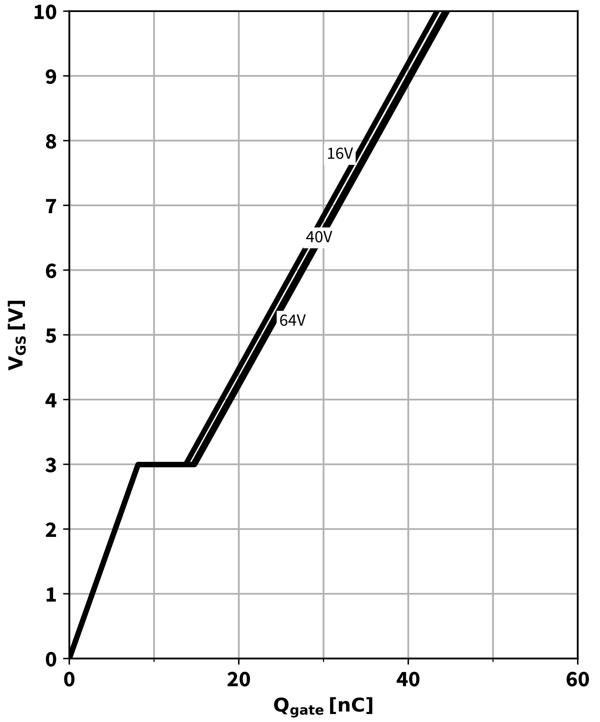
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; I_D = 1 mA

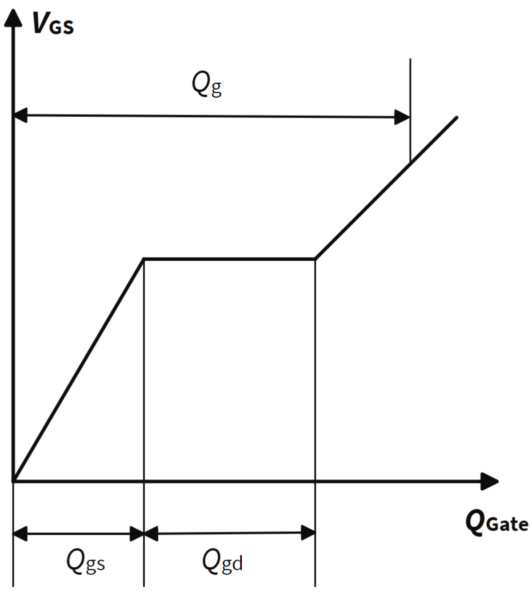


15 Typ. gate charge

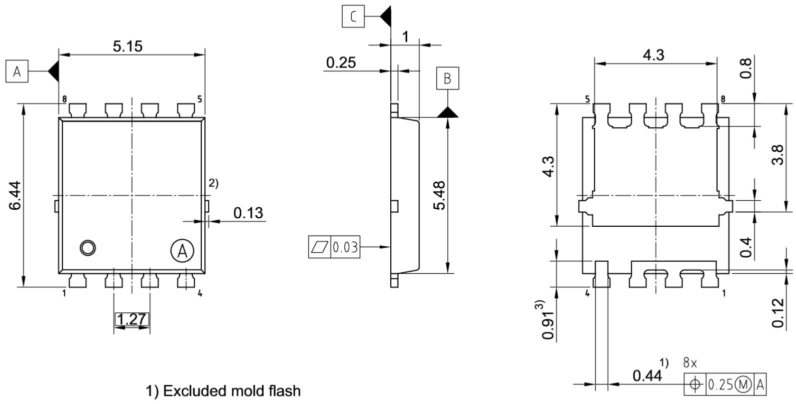
$V_{GS} = f(Q_{gate})$; I_D = 60 A pulsed; parameter: V_{DD}



16 Gate charge waveforms

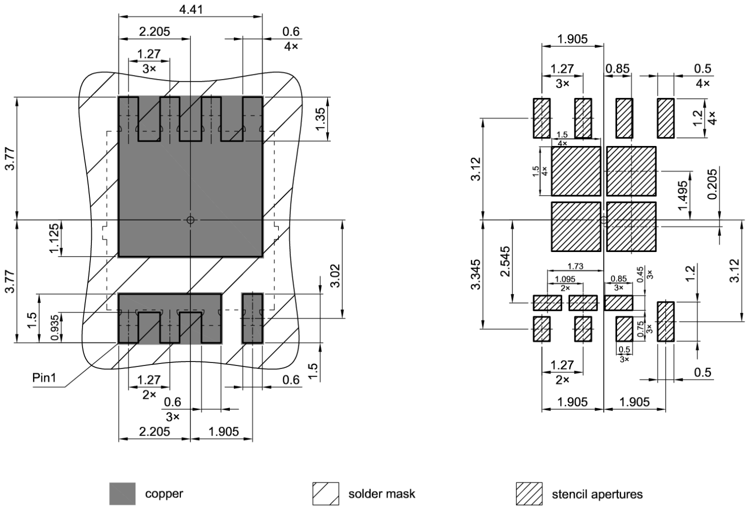


Package Outline



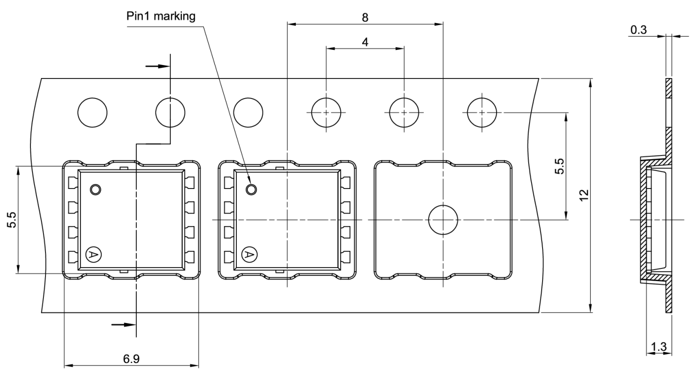
1) Excluded mold flash
2) Removal on mold gate:
Intrusion 0.1mm
Protrusion 0.1mm
3) Lead length up to anti flash line
4)All metal surface are plated, except area of cut
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ±0.1;±1°30'

Footprint



All dimensions are in units mm
All pads are solder mask defined

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Revision History

Revision	Date	Changes
Revision 1.0	2025-04-02	Final data sheet

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