

Automotive MOSFET

OptiMOS™ 5 Power-Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

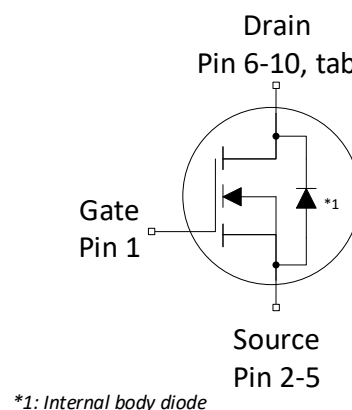
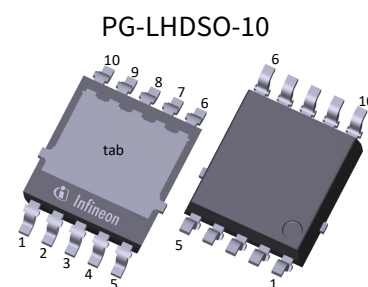
General automotive applications.

Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on)}$	6.9	mΩ
I_D (chip limited)	80	A



Part number	Package	Marking	Related links
IAUCN08S5N068T	PG-LHDSO-10	5A8	see Appendix A

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1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	80	A	Chip limitation, $V_{GS} = 10\text{ V}$ ^{1) 2)}
				80		DC current, $V_{GS} = 10\text{ V}$
				24		R_{thJA} on 2s2p, $V_{GS} = 10\text{ V}$, $T_a = 100\text{ °C}$ ^{1) 3)}
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	199	A	$T_C = 25\text{ °C}$, $t_p = 100\text{ }\mu\text{s}$
Avalanche energy, single pulse ¹⁾	E_{AS}	-	-	113	mJ	$I_D = 21\text{ A}$
Avalanche current, single pulse	I_{AS}	-	-	42	A	-
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	98	W	$T_C = 25\text{ °C}$
Operating temperature	T_j	-55	-	175	°C	-

¹⁾ The parameter is not subject to production testing - specified by design.

²⁾ The current is limited by the overall system design, including the customer-specific PCB.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case 4)	R_{thJC}	-	-	1.52	K/W	-
Thermal characterization parameter, source pin 4) 5)	ψ_{source}		5.4	-		
Thermal characterization parameter, drain pin 4) 6)	ψ_{drain}		5.3	-		
Thermal resistance, junction - heatsink 4) 7)	R_{thJH}		7.5	-		
Thermal resistance, junction - ambient 4) 8)	R_{thJA}		49	-		

4) The parameter is not subject to production testing - specified by design.

5) Thermal characterization parameter, calculated as $\psi_{source} = (T_{source} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at source pins for given power.

6) Thermal characterization parameter, calculated as $\psi_{drain} = (T_{drain} - T_{ambient})/P_{dis}$ in condition of 3). Used to determine PCB temperature at drain pins for given power.

7) Device on 2s2p FR4 PCB defined in acc. with JEDEC standards (JESD51-5,-7) without thermal vias, heat sink of 71 x 110 x 2 mm is attached through TIM with 3.3 W/(m*K) and 400 µm thickness to top side pad. Heatsink fixed to 85°C ambient temperature

8) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D = 36\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 80\text{ V}$, $T_j = 25^\circ\text{C}$, $V_{GS} = 0\text{ V}$
				20		$V_{DS} = 80\text{ V}$, $T_j = 100^\circ\text{C}$, $V_{GS} = 0\text{ V}$ 9)
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	8.3	10.7	mΩ	$I_D = 20\text{ A}$, $V_{GS} = 6\text{ V}$
			5.8	6.9		$I_D = 40\text{ A}$, $V_{GS} = 10\text{ V}$
Gate resistance 9)	R_G	-	1.2	-	Ω	-

9) The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ¹⁰⁾	C_{iss}	-	1600	2080	pF	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$
Output capacitance ¹⁰⁾	C_{oss}		296	385		
Reverse transfer capacitance ¹⁰⁾	C_{rss}		16	24		
Turn-on delay time ¹⁰⁾	$t_{d(on)}$	-	6.1	-	ns	$I_D = 40\text{ A}$, $V_{GS} = 10\text{ V}$, $V_{DD} = 40\text{ V}$, $R_G = 3.5\ \Omega$
Rise time ¹⁰⁾	t_r		8.9			
Turn-off delay time ¹⁰⁾	$t_{d(off)}$		11.7			
Fall time ¹⁰⁾	t_f		7.9			

¹⁰⁾ The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ¹¹⁾	Q_{gs}	-	8.1	10.6	nC	$I_D = 40\text{ A}$, $V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V to } 10\text{ V}$
Gate to drain charge ¹¹⁾	Q_{gd}		6.4	9.6	nC	
Gate charge total ¹¹⁾	Q_g		25.4	33.0	nC	
Gate plateau voltage ¹¹⁾	$V_{plateau}$		5.0	-	V	

¹¹⁾ The parameter is not subject to production testing - specified by design.

Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current ¹²⁾	I_S	-	-	80	A	$T_C = 25\text{ °C}$
Diode pulse current ¹²⁾	$I_{S,pulse}$	-	-	199	A	$T_C = 25\text{ °C}$, $t_p = 100\ \mu\text{s}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$T_j = 25\text{ °C}$, $V_{GS} = 0\text{ V}$, $I_F = 40\text{ A}$
Reverse recovery time ¹²⁾	t_{rr}	-	40	60	ns	$di_F/dt = 100\text{ A}/\mu\text{s}$, $V_R = 40\text{ V}$, $I_F = 50\text{ A}$
Reverse recovery charge ¹²⁾	Q_{rr}		61	122	nC	

¹²⁾ The parameter is not subject to production testing - specified by design.

4 Electrical characteristics diagrams

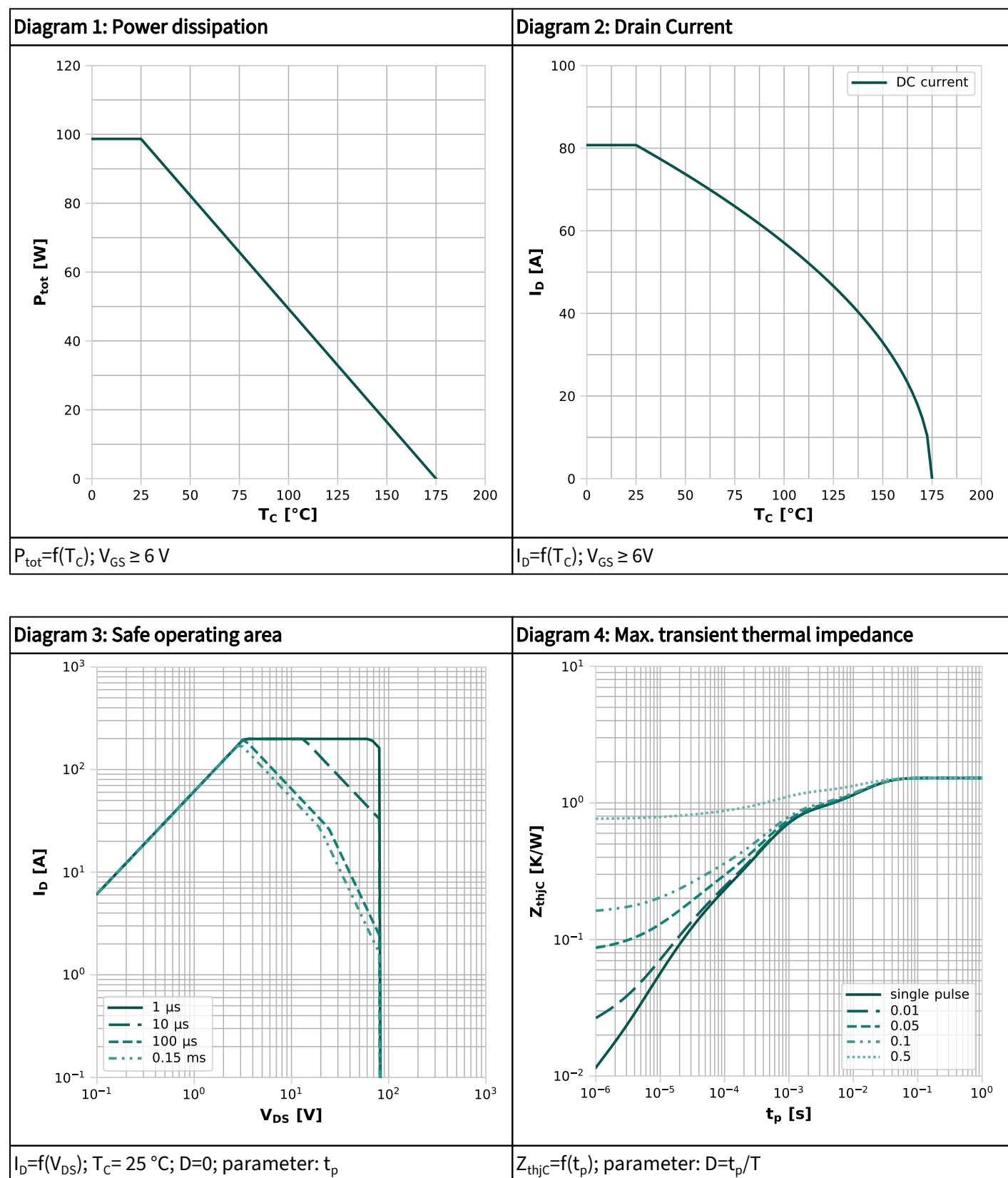
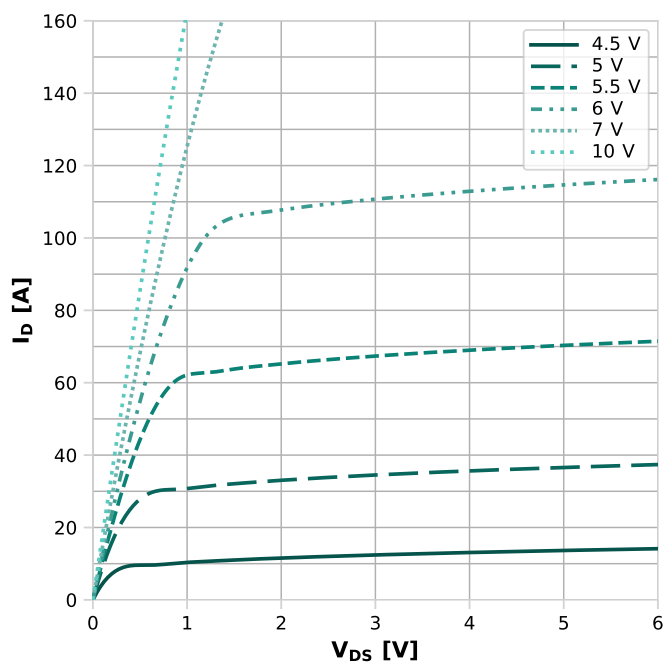
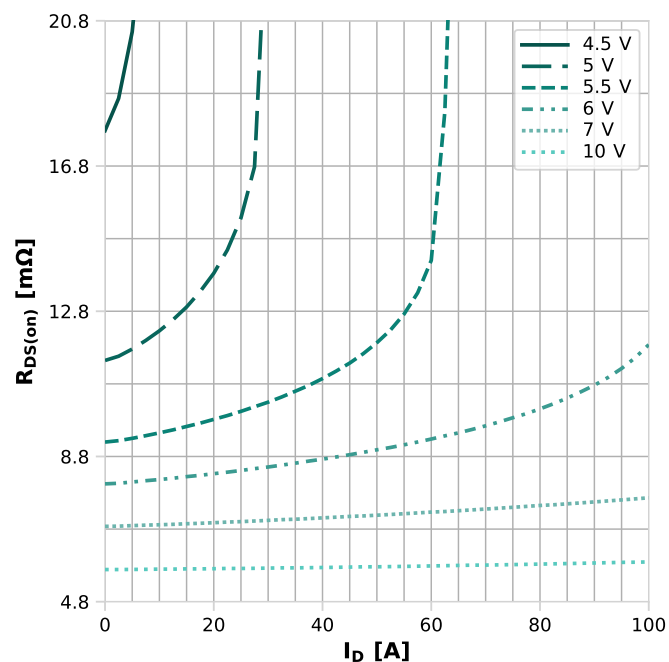


Diagram 5: Typ. output characteristics



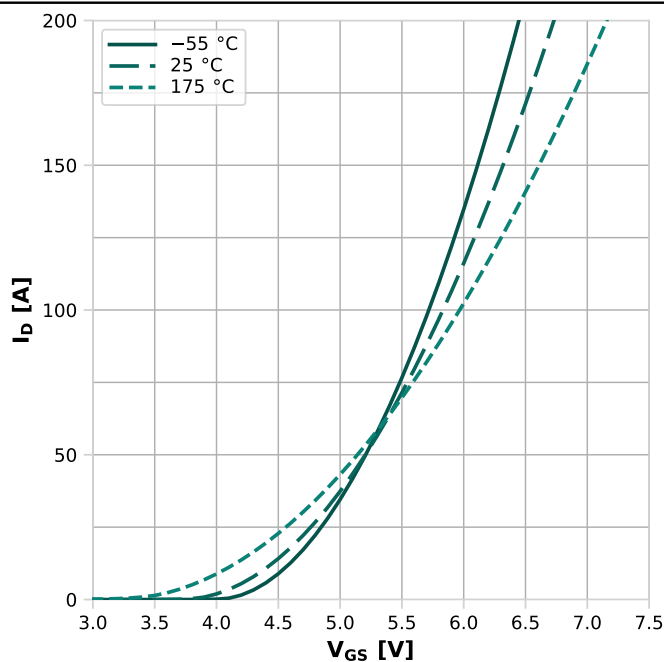
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on-state resistance



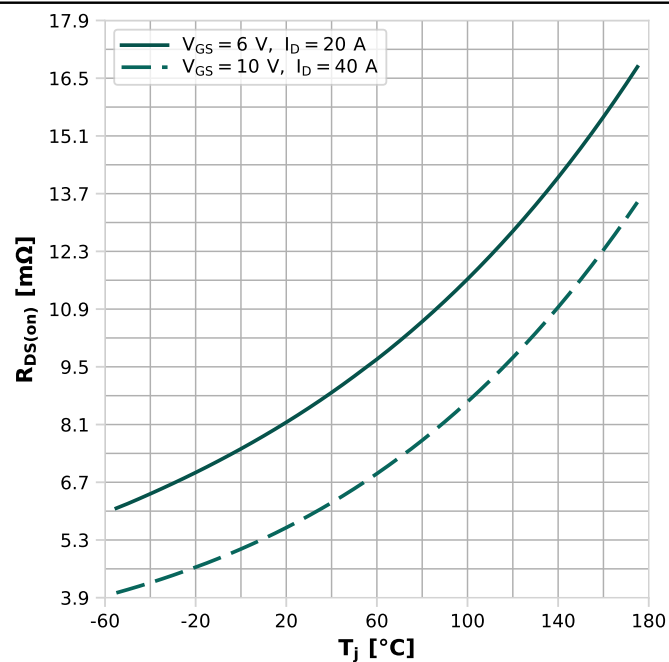
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



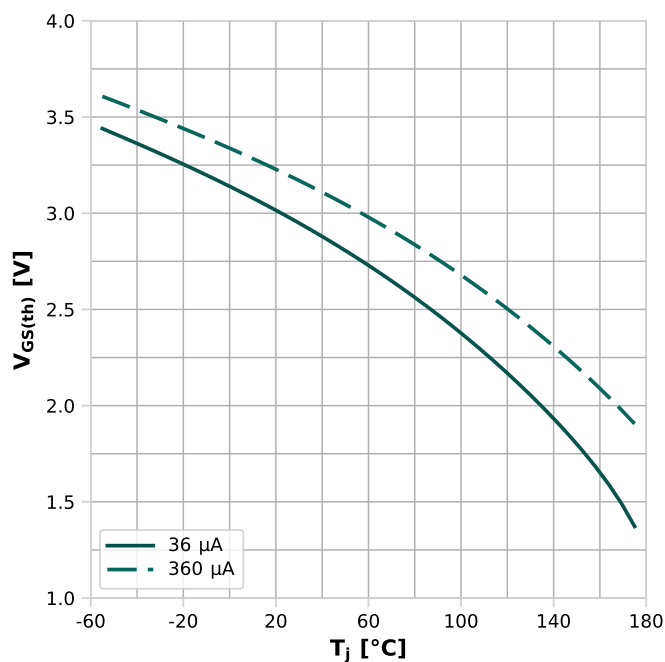
$I_D = f(V_{GS})$; $V_{DS} = 6\text{ V}$; parameter: T_j

Diagram 8: Typ. drain-source on-state resistance



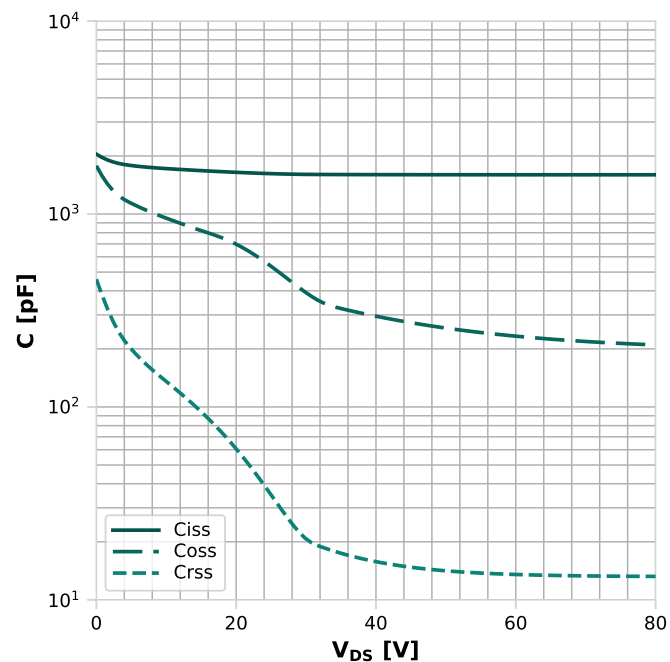
$R_{DS(on)} = f(T_j)$; parameter: I_D , V_{GS}

Diagram 9: Typ. gate threshold voltage



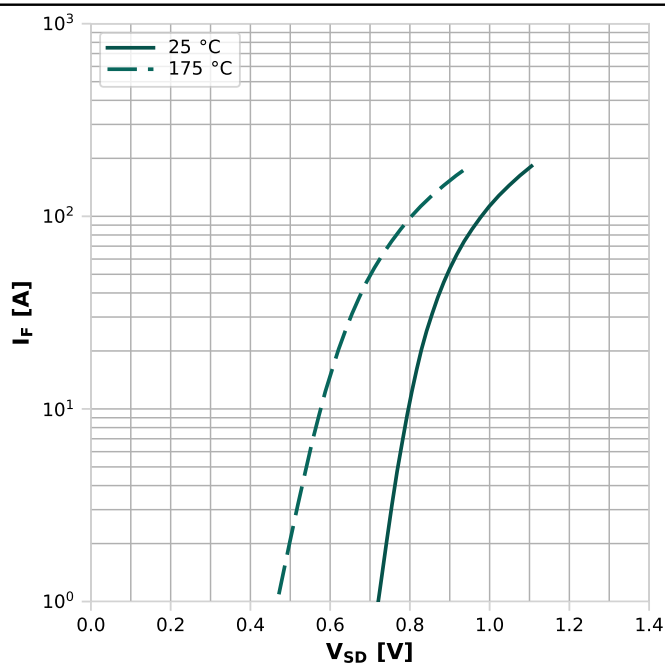
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D

Diagram 10: Typ. capacitances



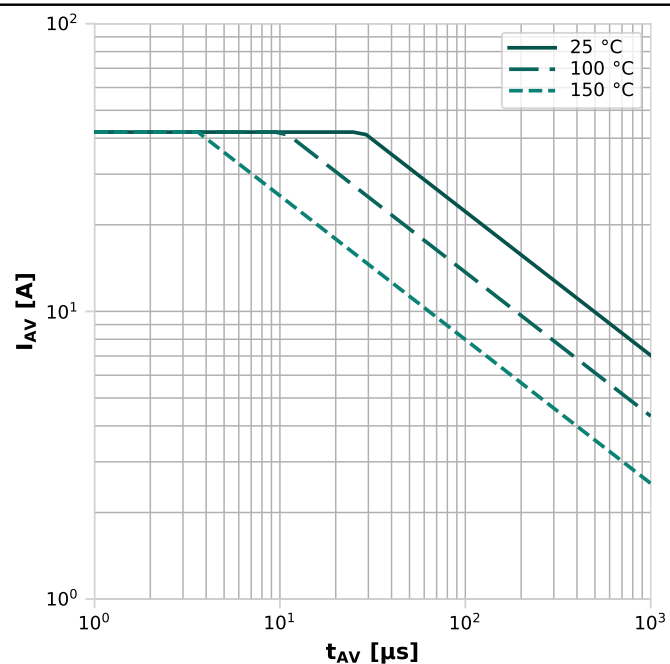
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 11: Typ. forward diode characteristics



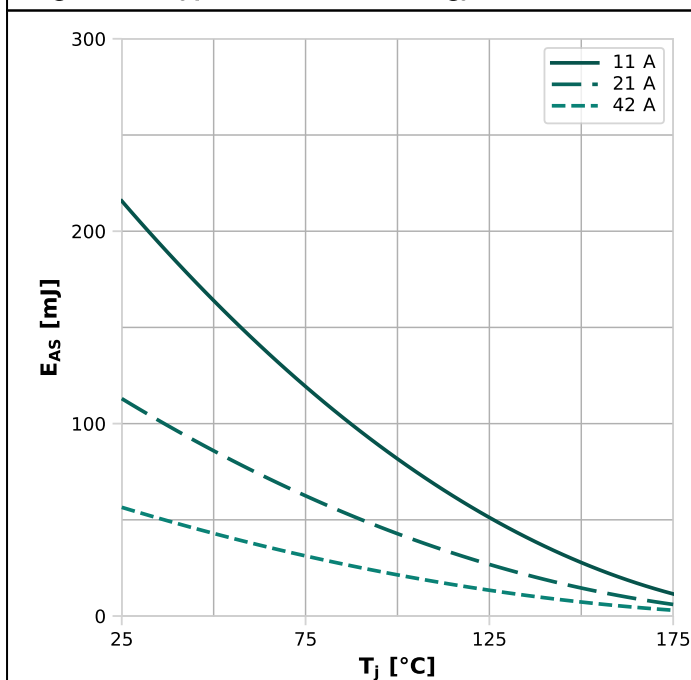
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Typ. avalanche characteristics



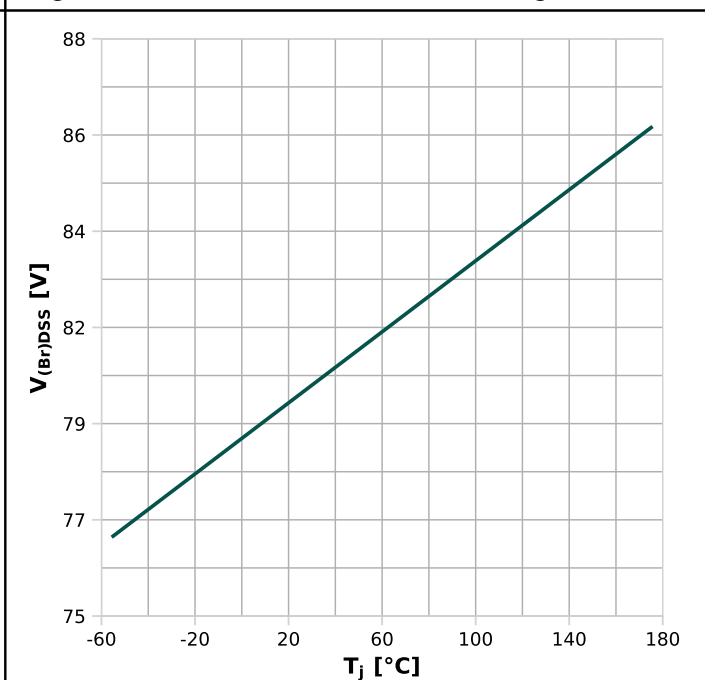
$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$

Diagram 13: Typical avalanche Energy



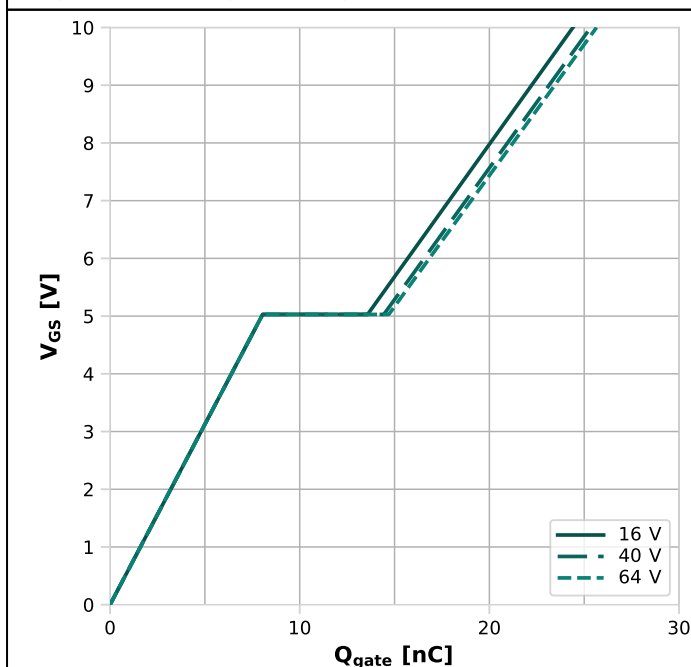
$E_{AS}=f(T_J)$; parameter: I_D

Diagram 14: Drain-source breakdown voltage



$V_{(Br)DSS}=f(T_J)$; $I_D = -1$ mA

Diagram 15: Typ. gate charge



$V_{GS}=f(Q_{gate})$; $I_D = -40$ A pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Diode characteristics

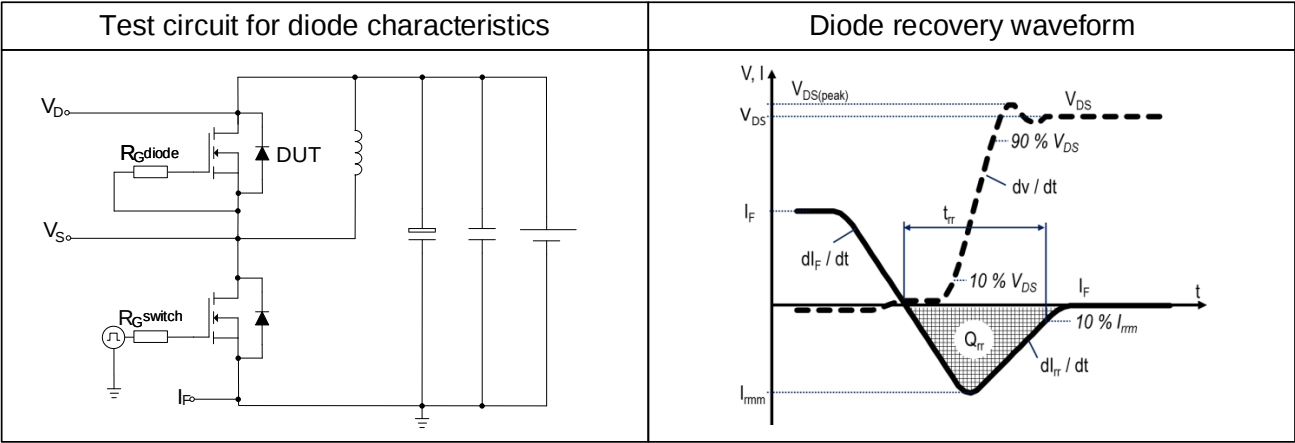


Table 9 Unclamped inductive load test circuit

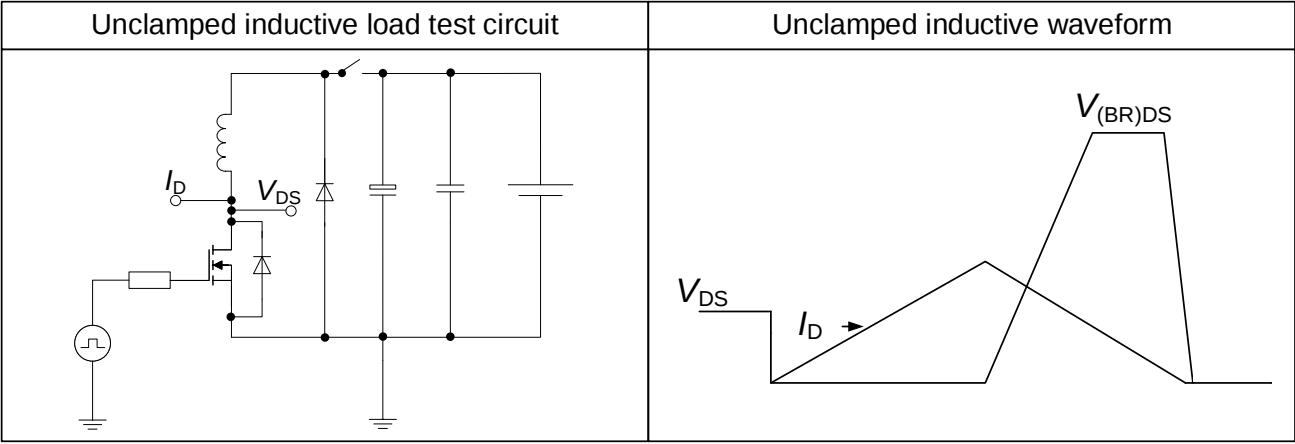
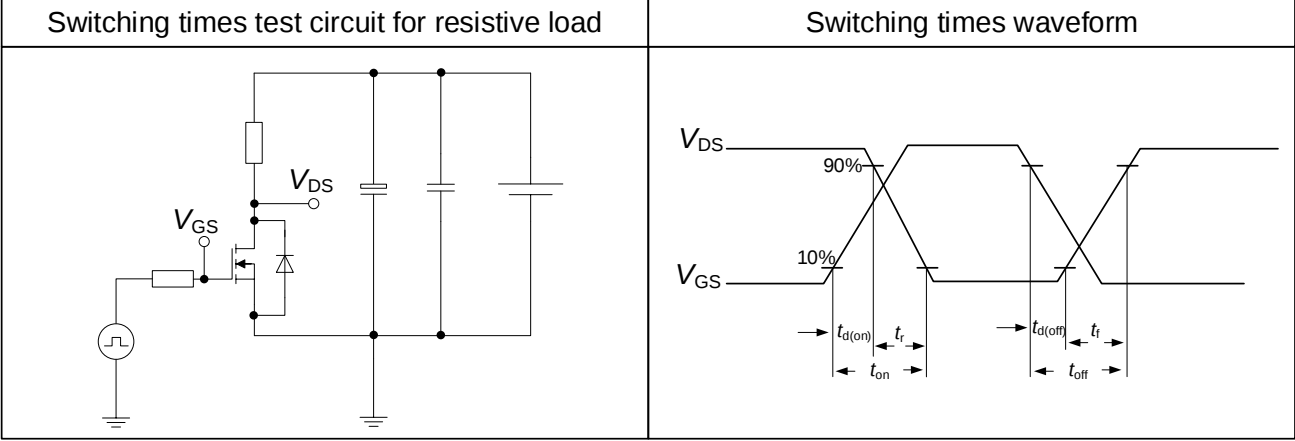


Table 10 Switching times test circuit for resistive load



6 Package outlines

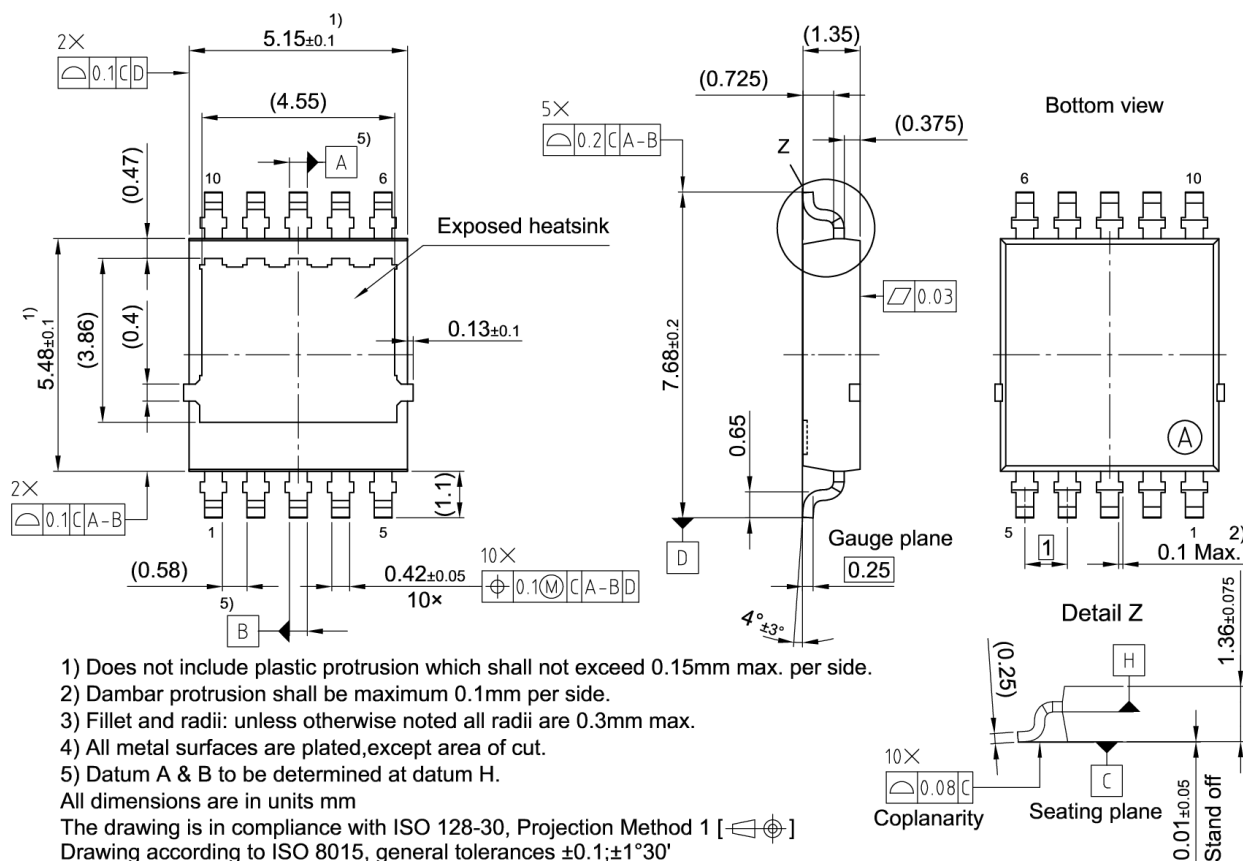


Figure 1 Outline PG-LHDSO-10, dimensions in mm

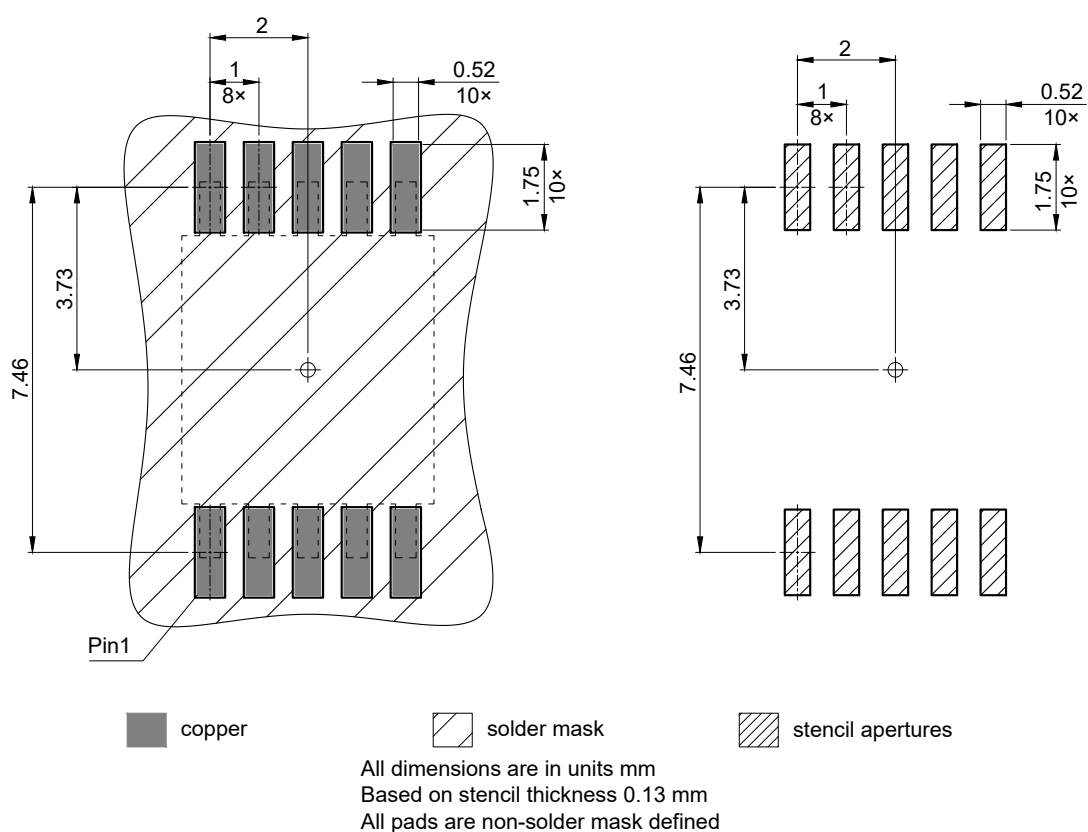
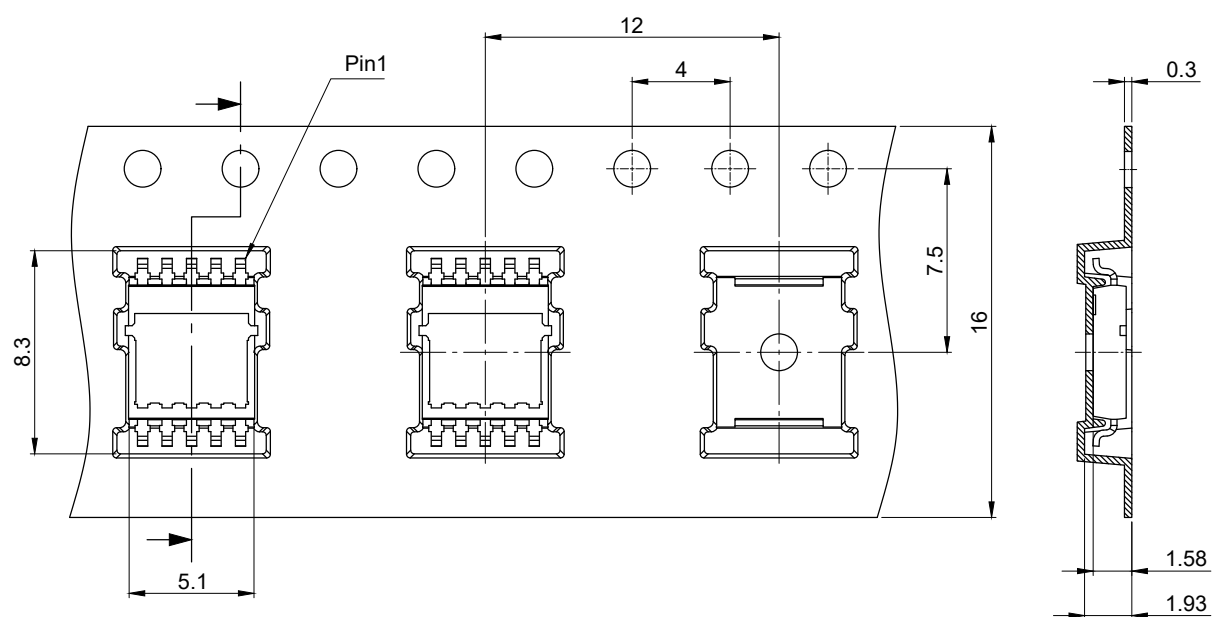


Figure 2 Footprint drawing PG-LHDSO-10, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-LHDSO-10, dimensions in mm

7 Appendix A

Table 11 **Related links**

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUCN08S5N068T

Revision 2026-07-10, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-07-10	Final Data Sheet

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