

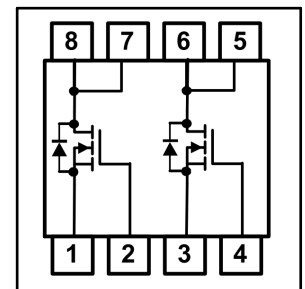
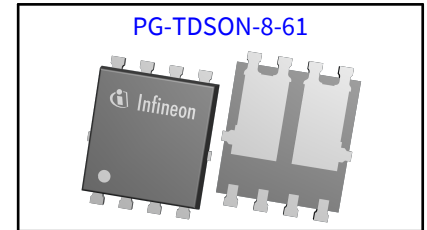
Automotive MOSFET

OptiMOS™ 7 Power-Transistor



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested



Potential Applications

General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

| | | |
|----------------------|------|----|
| V_{DS} | 40 | V |
| $R_{DS(on)}$ | 3.84 | mΩ |
| I_D (chip limited) | 84 | A |

| Type | Package | Marking |
|----------------|---------------|----------|
| IAUCN04S7L038D | PG-TDSON-8-61 | 7N4L038D |

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Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|---------------|---|--------------|------------------|
| Continuous drain current | I_D | $V_{GS} = 10\text{ V}$, Chip limitation ^{1,2)} | 84 | A |
| | | $V_{GS} = 10\text{ V}$, DC current | 60 | |
| | | $T_a = 100^\circ\text{C}$, $V_{GS} = 10\text{ V}$, R_{thJA} on 2s2p ^{2,3)} | 15 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C = 25^\circ\text{C}$, $t_p = 100\ \mu\text{s}$ | 200 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D = 20\text{ A}$ | 30 | mJ |
| Avalanche current, single pulse | I_{AS} | – | 40 | A |
| Gate source voltage | V_{GS} | – | ± 16 | V |
| | | Limited to duty factor of 1% | +20 | |
| Power dissipation | P_{tot} | $T_C = 25^\circ\text{C}$ | 51 | W |
| Operating temperature | T_j | – | -55 ... +175 | $^\circ\text{C}$ |

Thermal Characteristics²⁾

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal resistance, junction - case | R_{thJC} | – | – | – | 2.9 | K/W |
| Thermal resistance, junction - ambient ³⁾ | R_{thJA} | – | – | 48 | – | |

Electrical Characteristics

 at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Static Characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|------|------|---------------|
| Drain-source breakdown voltage | $V_{(Br)DSS}$ | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 40 | – | – | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 15\text{ }\mu\text{A}$ | 1.2 | 1.5 | 1.8 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25\text{ °C}$ | – | – | 1 | μA |
| | | $V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 100\text{ °C}^{2)}$ | – | – | 3 | |
| Gate-source leakage current | I_{GSS} | $V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ | – | – | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS} = 4.5\text{ V}$, $I_D = 30\text{ A}$ | – | 4.76 | 5.54 | m Ω |
| | | $V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$ | – | 3.44 | 3.84 | |
| Gate resistance ²⁾ | R_G | – | – | 2.7 | – | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|--------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Dynamic Characteristics²⁾ | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | - | 1031 | 1340 | pF |
| Output capacitance | C_{oss} | | - | 514 | 668 | |
| Reverse transfer capacitance | C_{rss} | | - | 21 | 32 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 30\text{ A}, R_G = 3.5\ \Omega$ | - | 3 | - | ns |
| Rise time | t_r | | - | 8 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 15 | - | |
| Fall time | t_f | | - | 19 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD} = 20\text{ V}, I_D = 30\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ | - | 2.9 | 3.8 | nC |
| Gate to drain charge | Q_{gd} | | - | 2.8 | 4.2 | |
| Gate charge total | Q_g | | - | 15 | 20 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 2.9 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|--|---|-----|------|----|
| Diode continuous forward current ²⁾ | I_S | $T_C = 25^\circ\text{C}$ | - | - | 60 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | $T_C = 25^\circ\text{C}, t_p = 100\ \mu\text{s}$ | - | - | 200 | |
| Diode forward voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_F = 30\text{ A}, T_j = 25^\circ\text{C}$ | - | 0.8 | 0.95 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R = 20\text{ V}, I_F = 50\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$ | - | 12 | 18 | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 2 | 4 | nC |

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

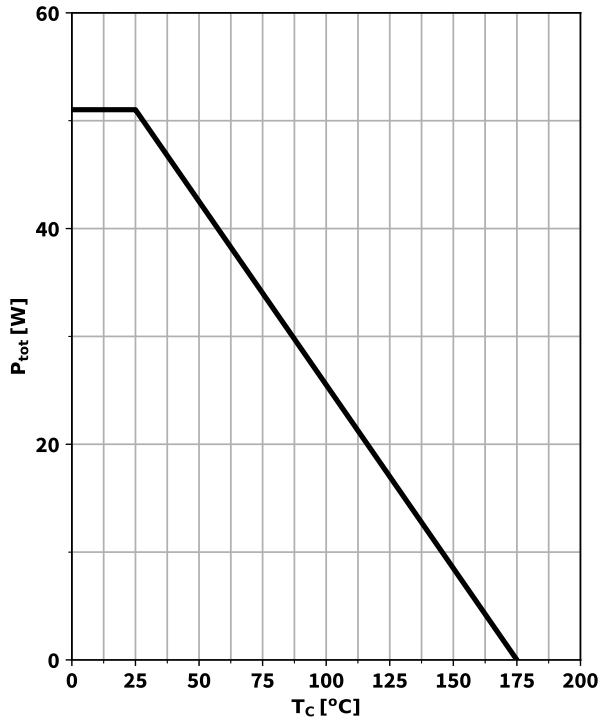
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

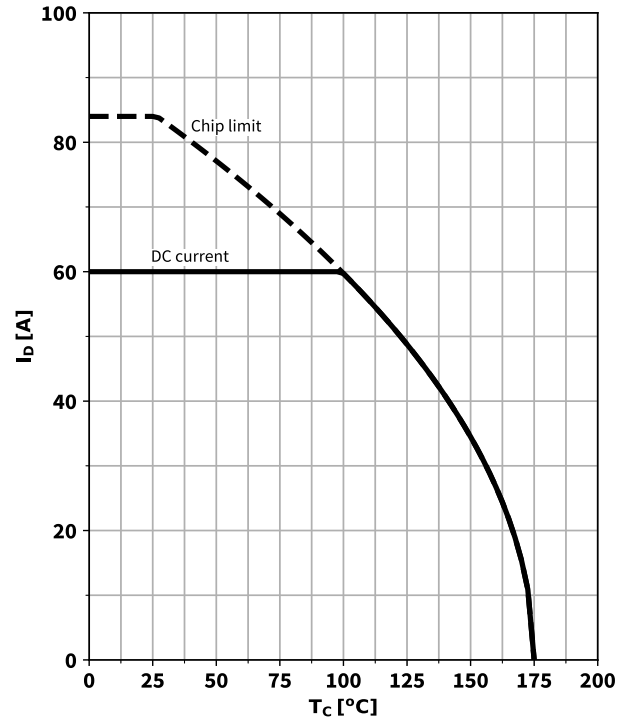
1 Power dissipation

$$P_{tot} = f(T_C); V_{GS} \geq 6 \text{ V}$$



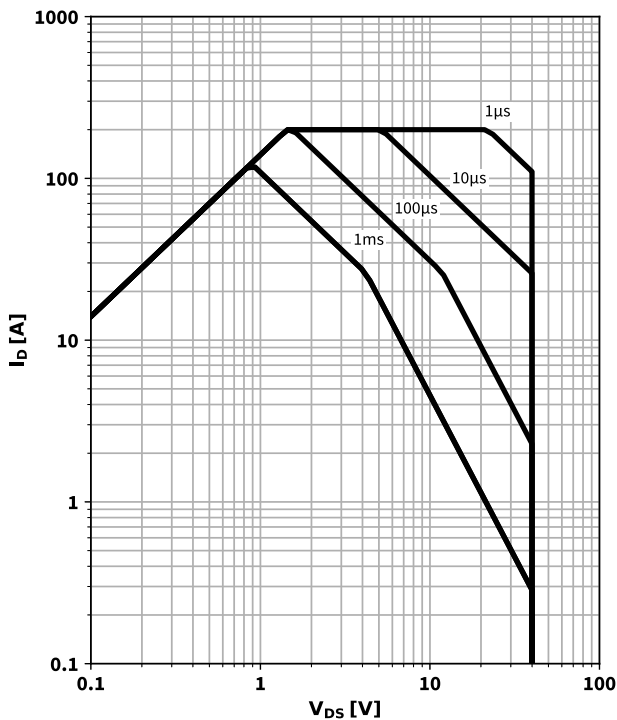
2 Drain current

$$I_D = f(T_C); V_{GS} \geq 6 \text{ V}$$



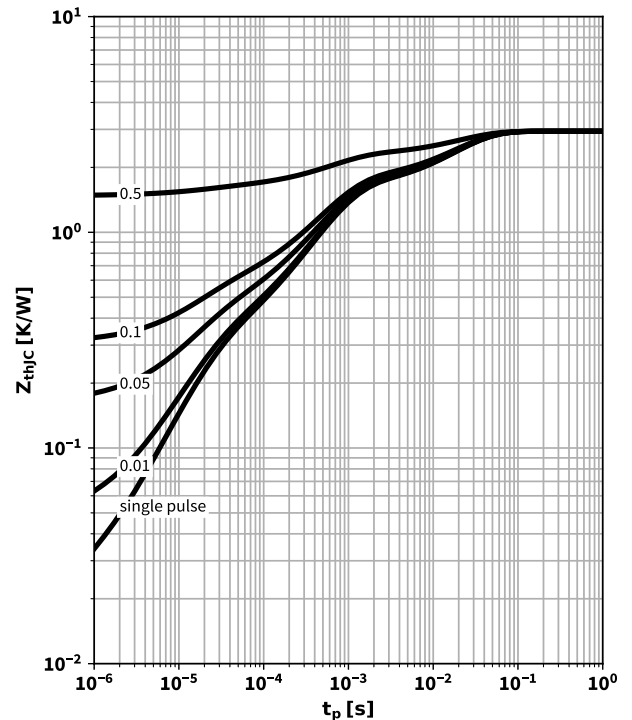
3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0; \text{ parameter: } t_p$$



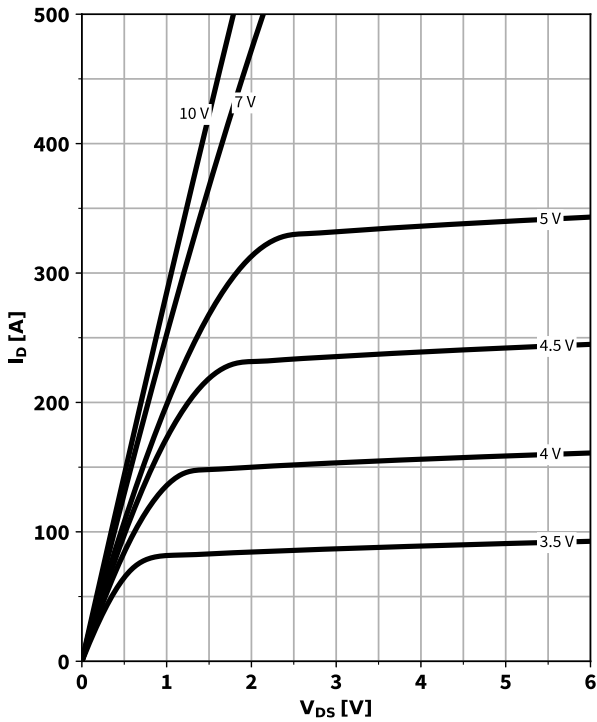
4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p); \text{ parameter: } D = t_p/T$$



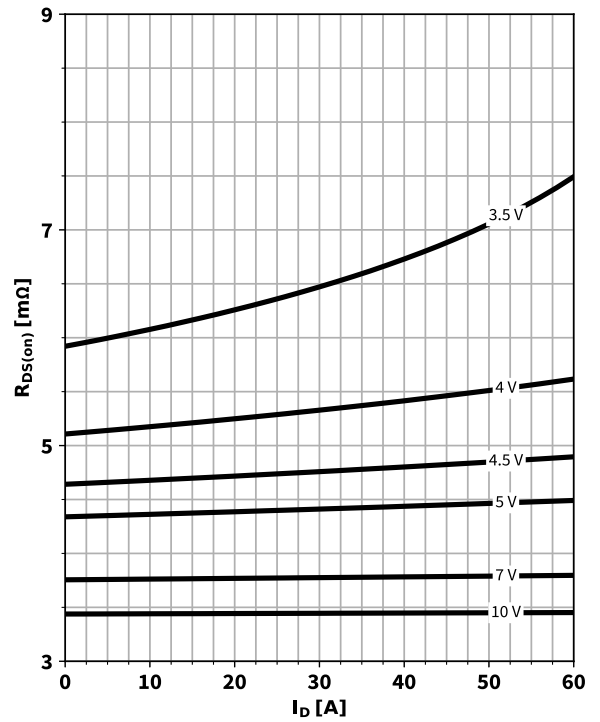
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C};$ parameter: V_{GS}



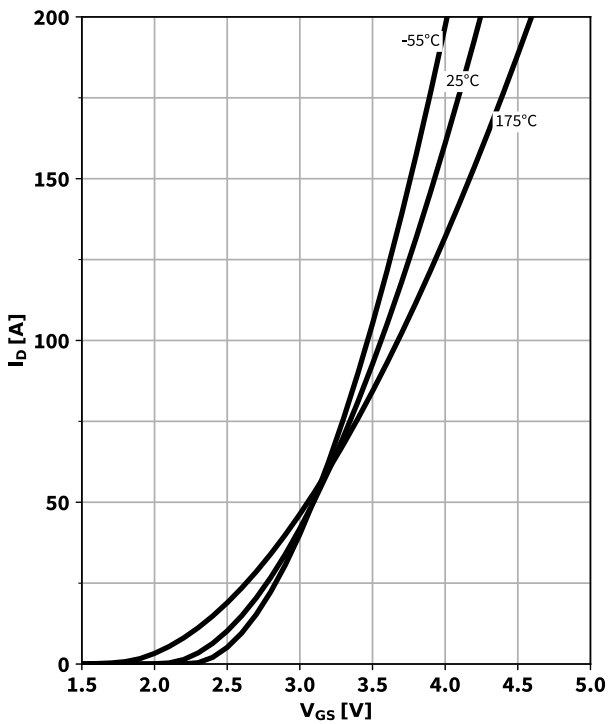
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C};$ parameter: V_{GS}



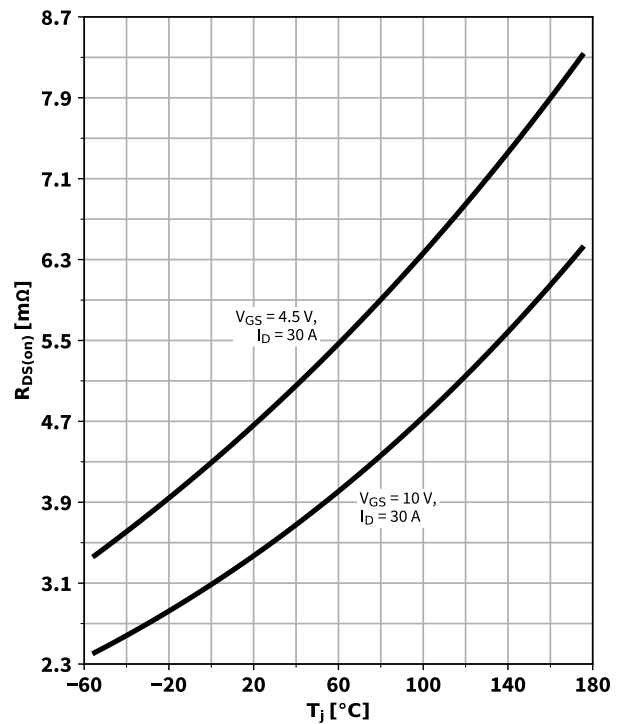
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V};$ parameter: T_j



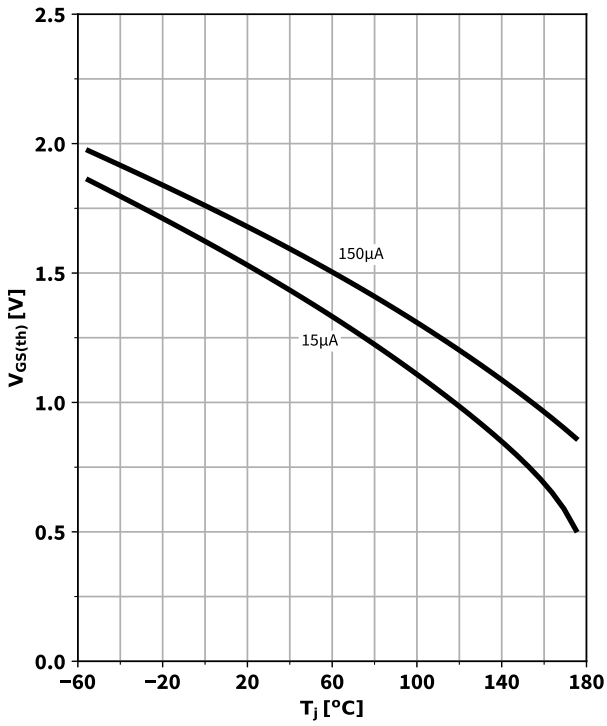
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j);$ parameter: I_D, V_{GS}



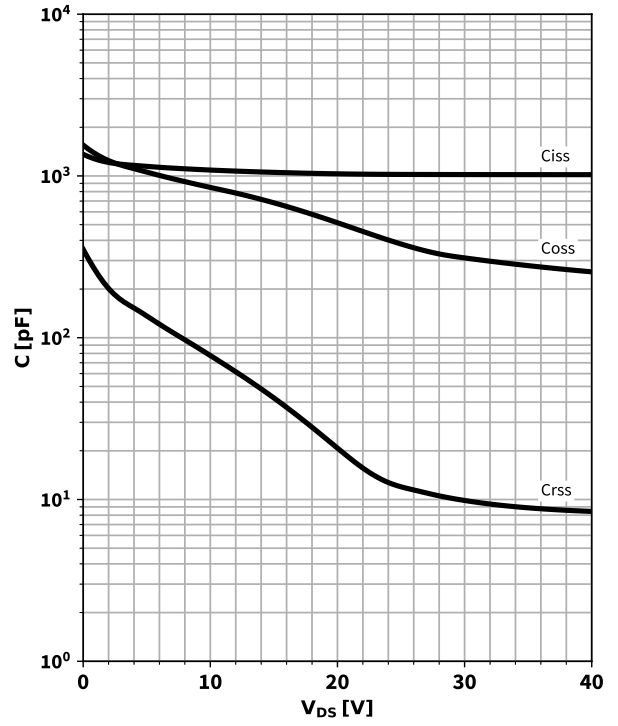
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



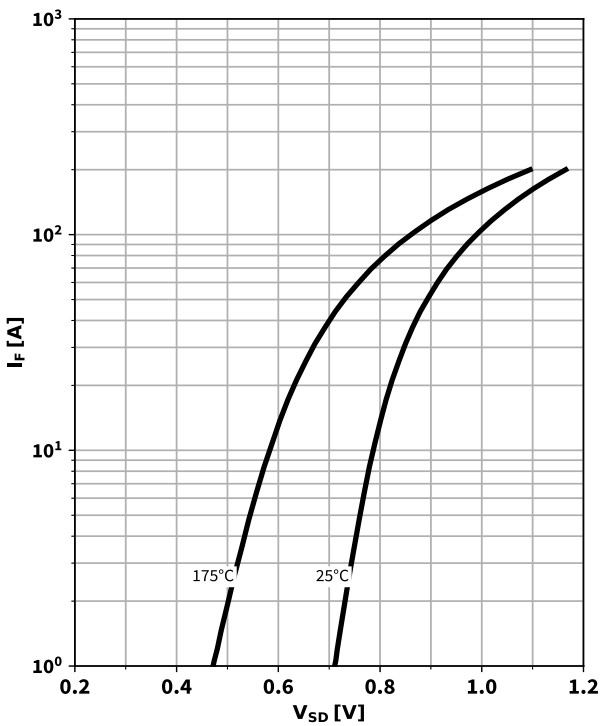
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0 V$; $f = 1 MHz$



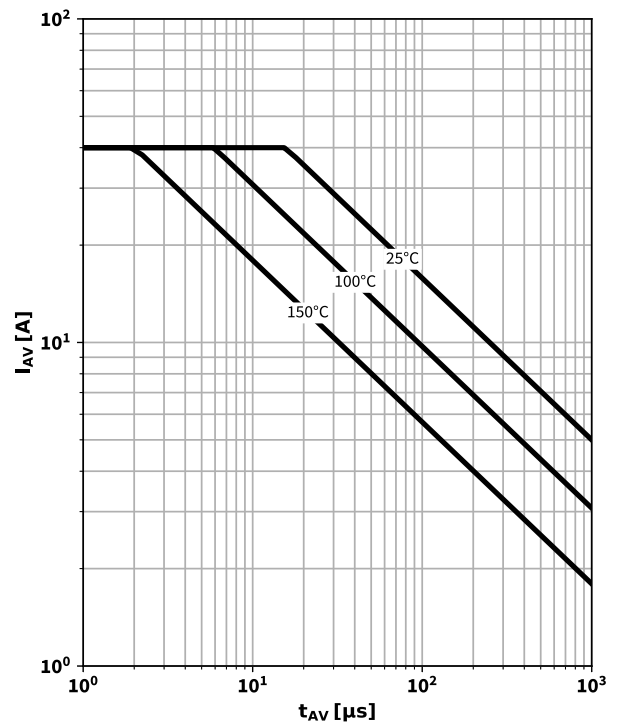
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



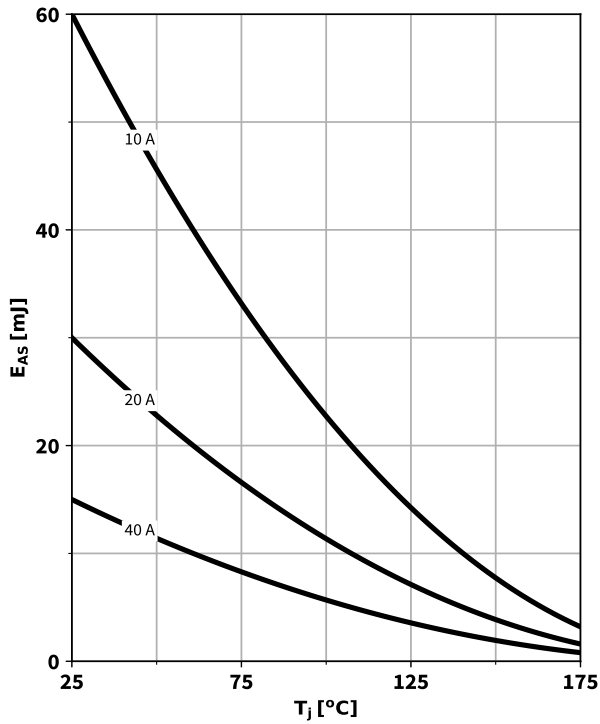
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



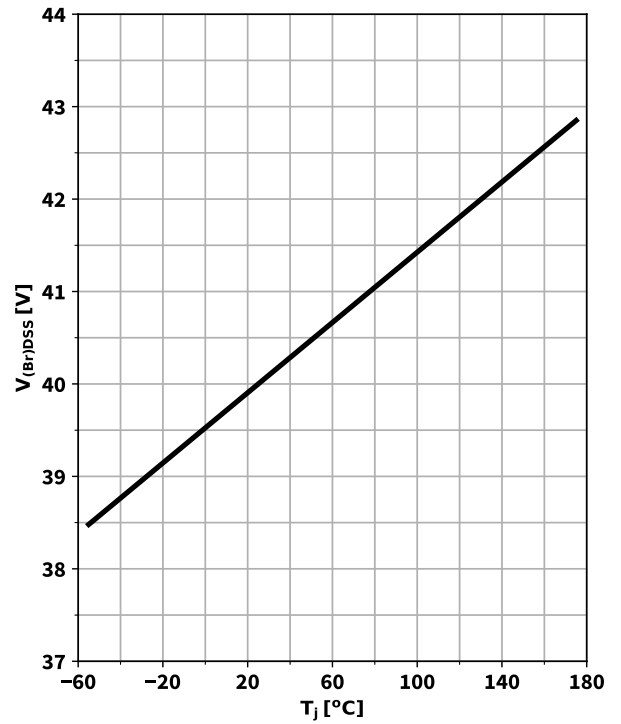
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



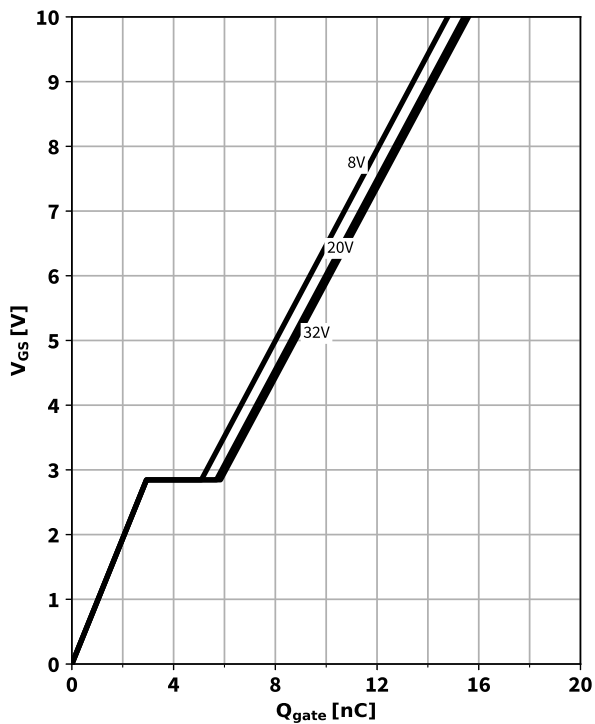
14 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$; $I_D = 1$ mA

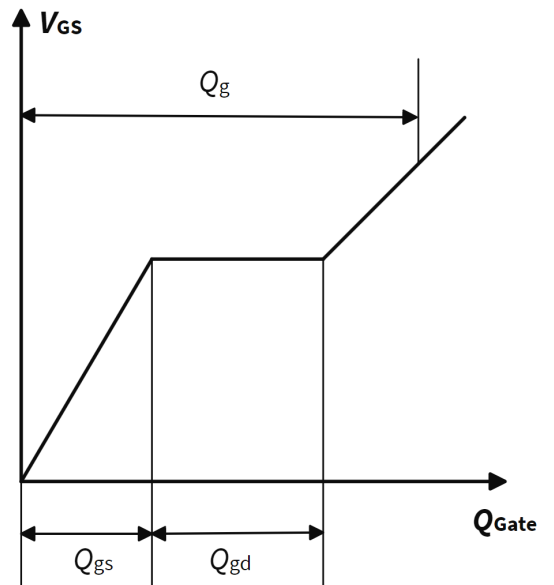


15 Typ. gate charge

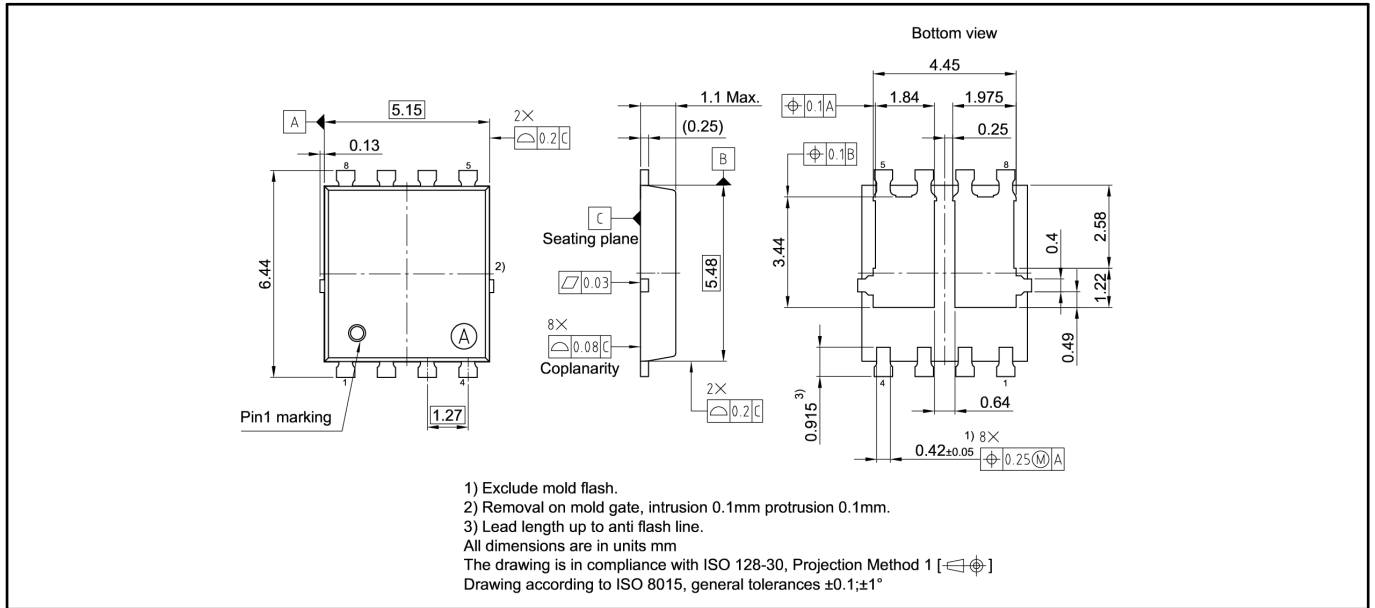
$V_{GS} = f(Q_{gate})$; $I_D = 30$ A pulsed; parameter: V_{DD}



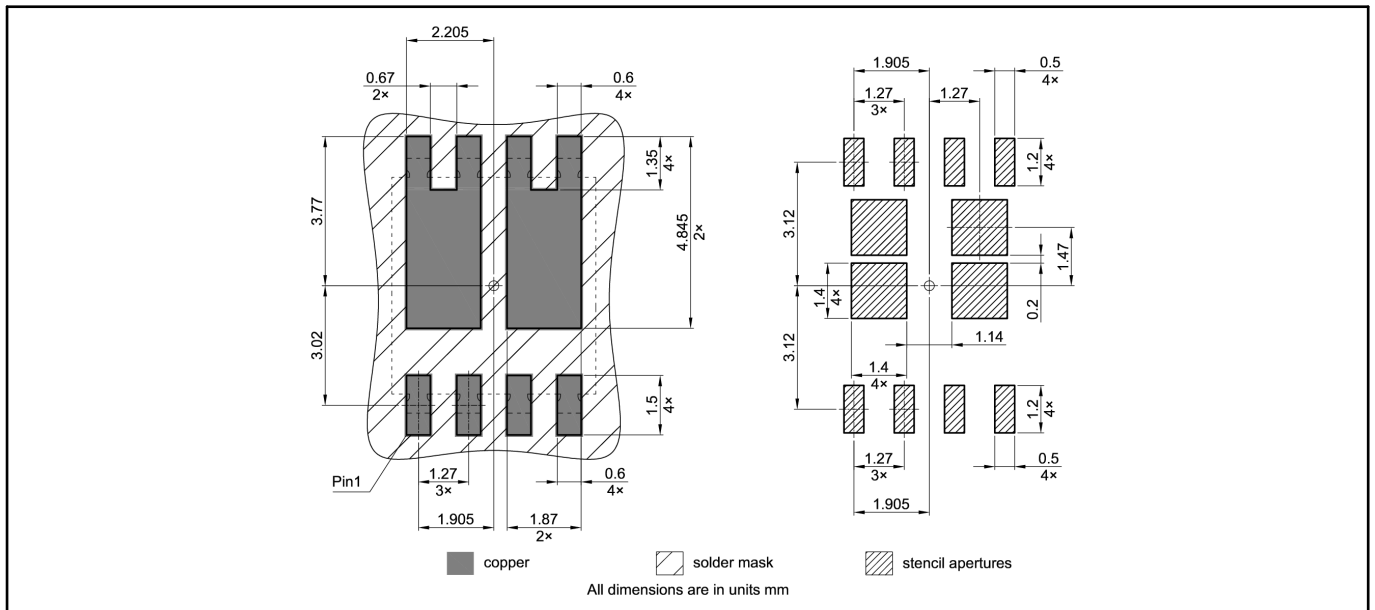
16 Gate charge waveforms



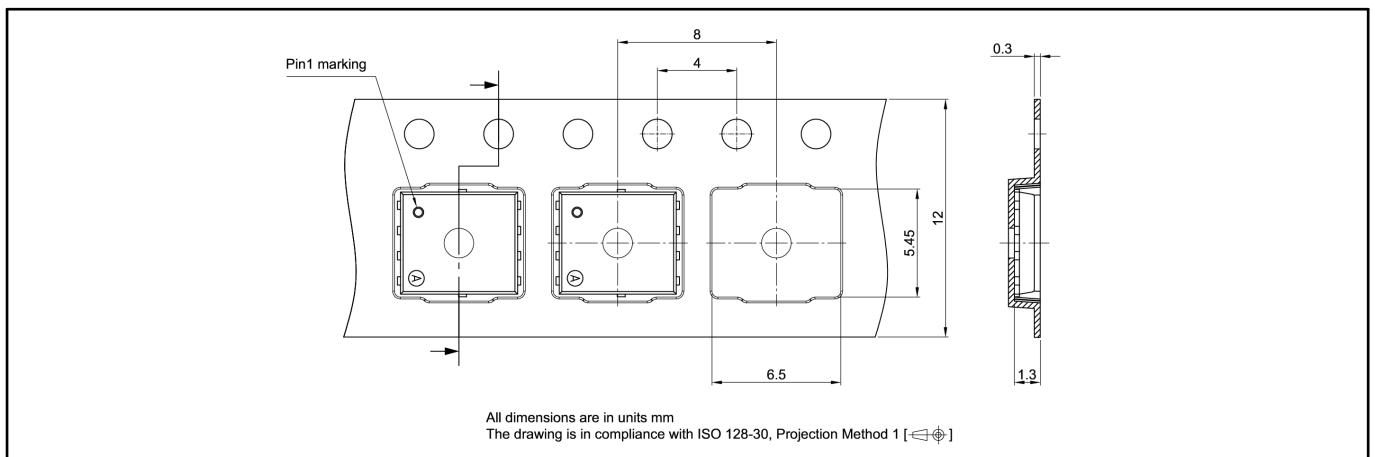
Package Outline



Footprint



Packaging



Revision History

| Revision | Date | Changes |
|--------------|------------|------------------|
| Revision 1.0 | 2025-04-09 | Final Data Sheet |

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