

Automotive MOSFET OptiMOS™ 7 Power-Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL2a up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

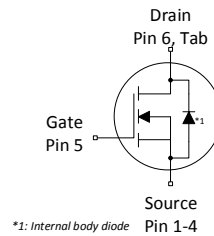
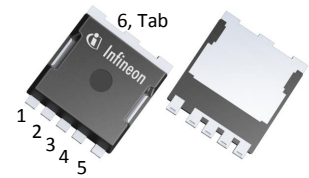
Product validation

Qualified according to Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on)}$	1.22	mΩ
I_D (chip limited)	208	A

PG-HSOF-5



Part number	Package	Marking	Related links
IAUAN04S7N012	PG-HSOF-5	7N04N012	see Appendix A

Table of contents

Description	1
Maximum ratings	3
Thermal characteristics	4
Electrical characteristics	4
Electrical characteristics diagrams	6
Test circuits	10
Package outlines	11
Appendix A	14
Revision history	15
Trademarks	16
Disclaimer	16

1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	208	A	Chip limitation, $V_{GS} = 10\text{ V}$ ^{1) 2)}
				180		DC current, $V_{GS} = 10\text{ V}$
				37		R_{thJA} on 2s2p, $V_{GS} = 10\text{ V}$, $T_a = 100\text{ °C}$ ¹⁾
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	610	A	$T_C = 25\text{ °C}$, $t_p = 100\text{ }\mu\text{s}$
Avalanche energy, single pulse ¹⁾	E_{AS}	-	-	88	mJ	$I_D = 55\text{ A}$
Avalanche current, single pulse	I_{AS}	-	-	110	A	-
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	101	W	$T_C = 25\text{ °C}$
Operating temperature	T_j	-55	-	175	°C	-

¹⁾ The parameter is not subject to production testing - specified by design.

²⁾ In practice, the current is limited by the overall system design, including the customer-specific PCB.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case 3)	R_{thJC}	-	-	1.48	K/W	-
Thermal resistance, junction - ambient ^{4) 3)}	R_{thJA}	-	24.0	-		

3) The parameter is not subject to production testing - specified by design.

4) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at $T_J=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$
Gate threshold voltage	$V_{GS(th)}$	2.2	2.6	3	V	$V_{DS}=V_{GS}$, $I_D = 40\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 40\text{ V}$, $T_J = 25\text{ °C}$, $V_{GS} = 0\text{ V}$
				11		$V_{DS} = 40\text{ V}$, $T_J = 100\text{ °C}$, $V_{GS} = 0\text{ V}$ ⁵⁾
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.33	1.57	m Ω	$I_D = 45\text{ A}$, $V_{GS} = 7\text{ V}$
			1.05	1.22		$I_D = 90\text{ A}$, $V_{GS} = 10\text{ V}$
Gate resistance ⁵⁾	R_G	-	1.6	-	Ω	-

5) The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	2730	3550	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}		1590	2070		
Reverse transfer capacitance ⁶⁾	C_{rss}		54	81		
Turn-on delay time ⁶⁾	$t_{d(on)}$	-	9	-	ns	$I_D = 90\text{ A}, V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}, R_G = 3.5\ \Omega$
Rise time ⁶⁾	t_r		4			
Turn-off delay time ⁶⁾	$t_{d(off)}$		16			
Fall time ⁶⁾	t_f		8			

⁶⁾ The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁷⁾	Q_{gs}	-	12	16	nC	$I_D = 90\text{ A}, V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V to } 10\text{ V}$
Gate to drain charge ⁷⁾	Q_{gd}		8	12	nC	
Gate charge total ⁷⁾	Q_g		40	52	nC	
Gate plateau voltage ⁷⁾	$V_{plateau}$		4.3	-	V	

⁷⁾ The parameter is not subject to production testing - specified by design.

Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current ⁸⁾	I_S	-	-	180	A	$T_C = 25\text{ }^\circ\text{C}$
Diode pulse current ⁸⁾	$I_{S,pulse}$	-	-	610	A	$T_C = 25\text{ }^\circ\text{C}, t_p = 100\ \mu\text{s}$
Diode forward voltage	V_{SD}	-	0.85	0.95	V	$T_J = 25\text{ }^\circ\text{C}, V_{GS} = 0\text{ V}, I_F = 90\text{ A}$
Reverse recovery time ⁸⁾	t_{rr}	-	36	54	ns	$di_F/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}, I_F = 50\text{ A}$
Reverse recovery charge ⁸⁾	Q_{rr}		21	42	nC	

⁸⁾ The parameter is not subject to production testing - specified by design.

4 Electrical characteristics diagrams

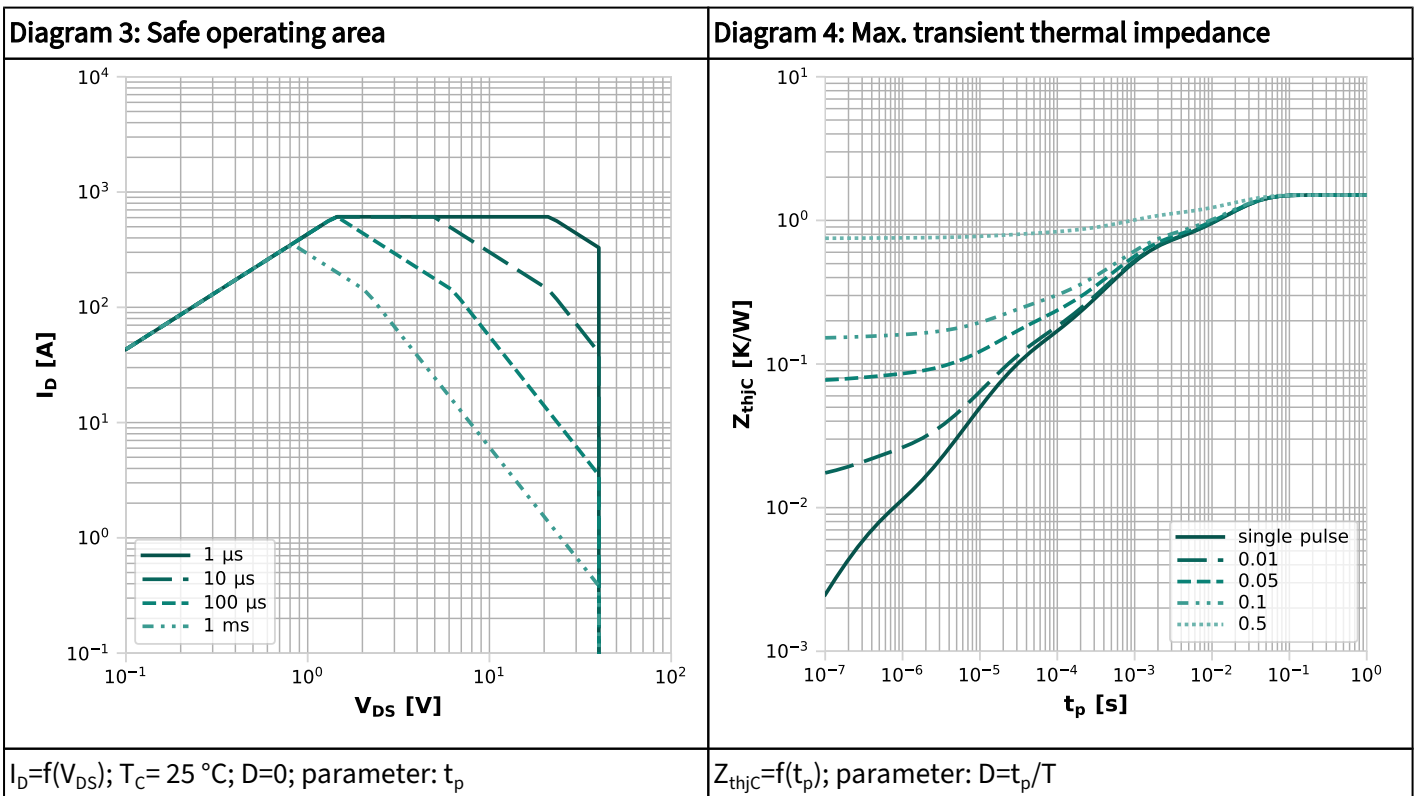
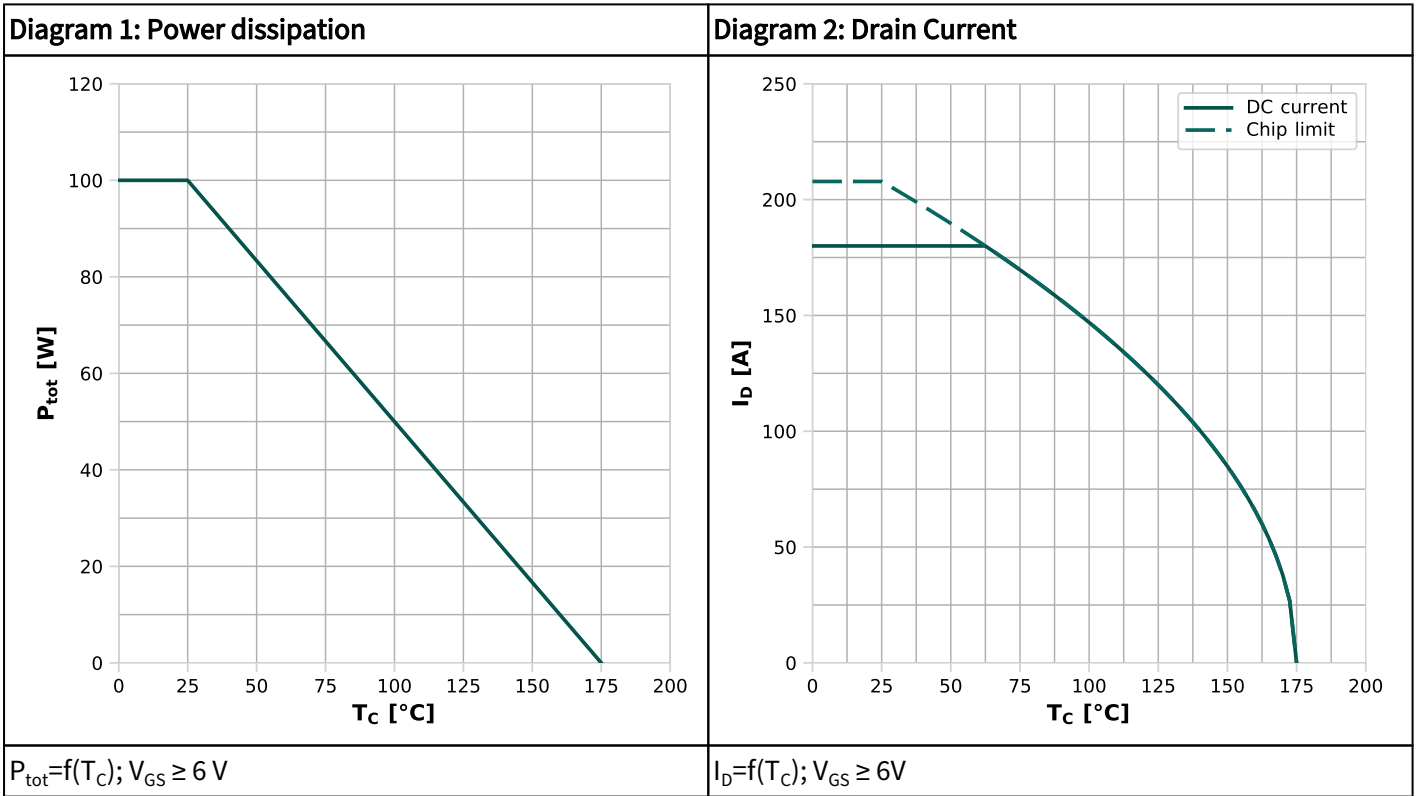
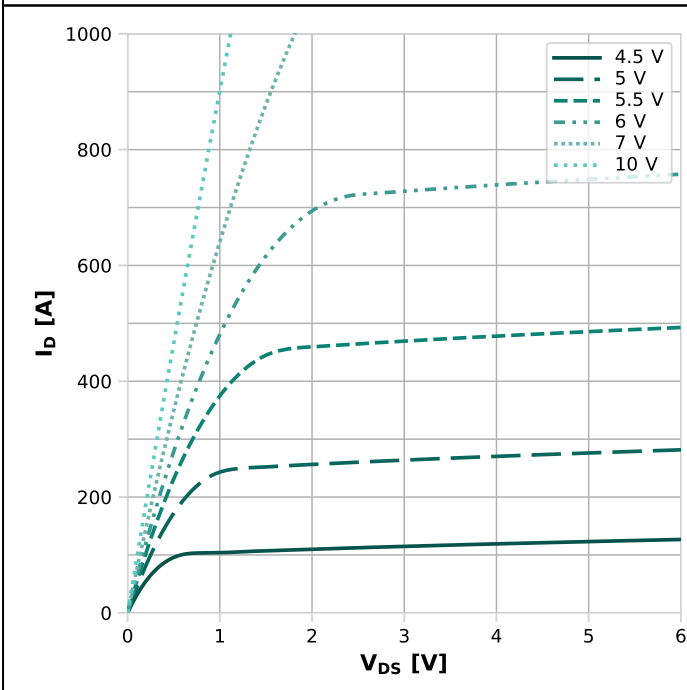
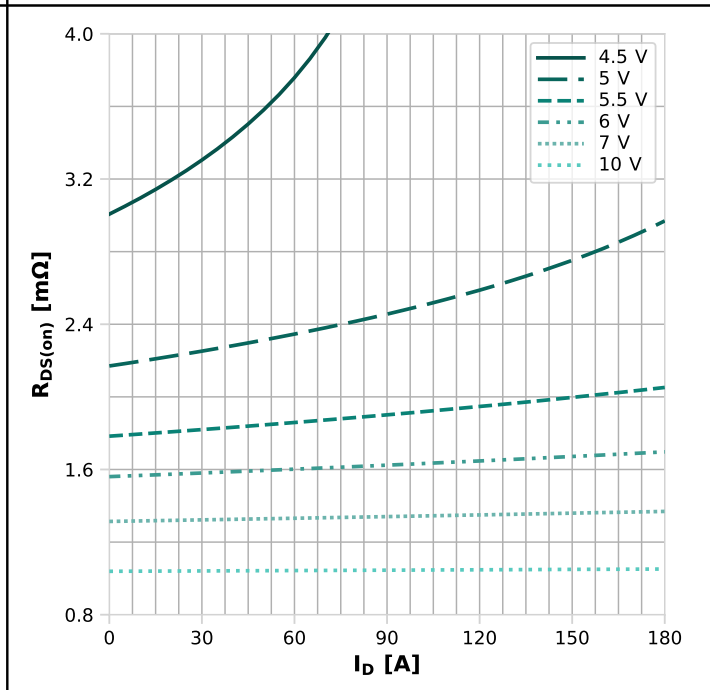


Diagram 5: Typ. output characteristics



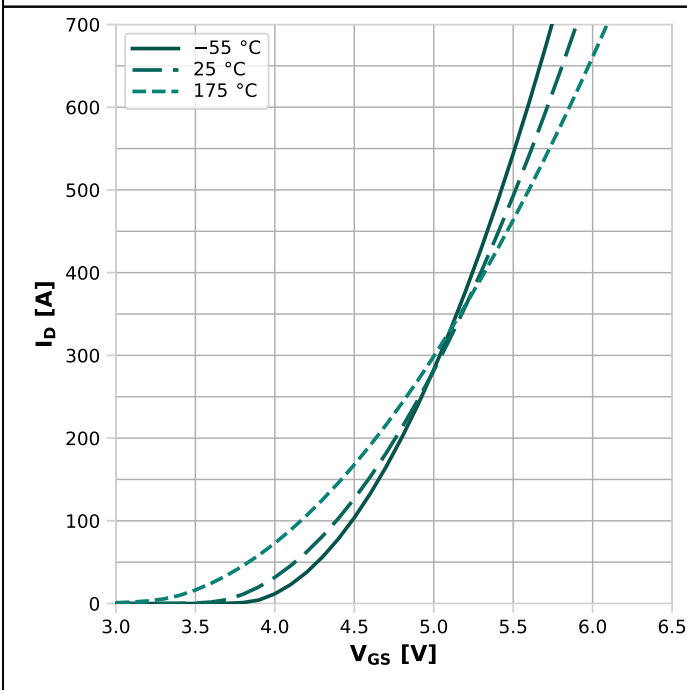
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on-state resistance



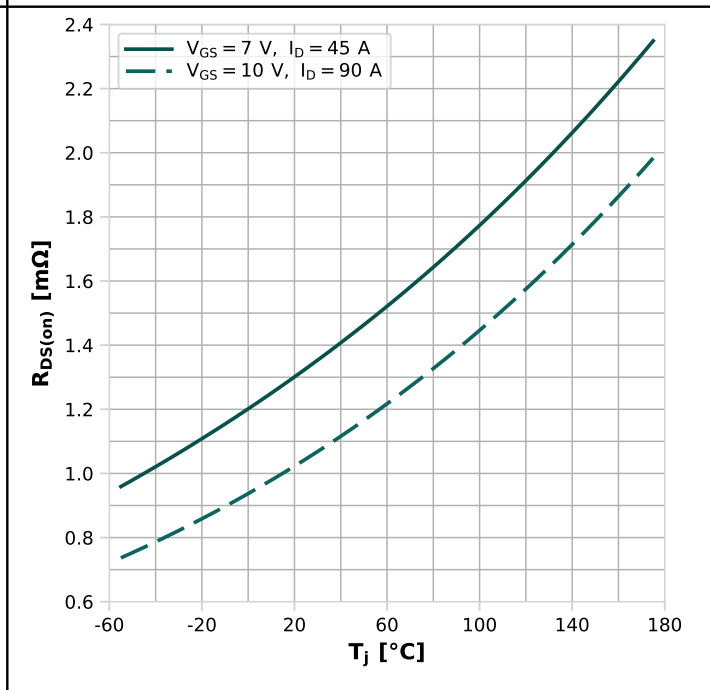
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



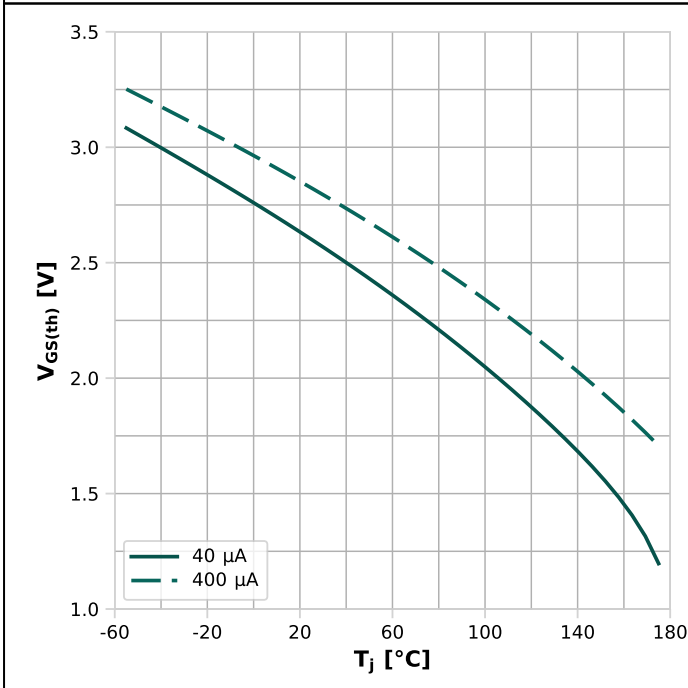
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$

Diagram 8: Typ. drain-source on-state resistance



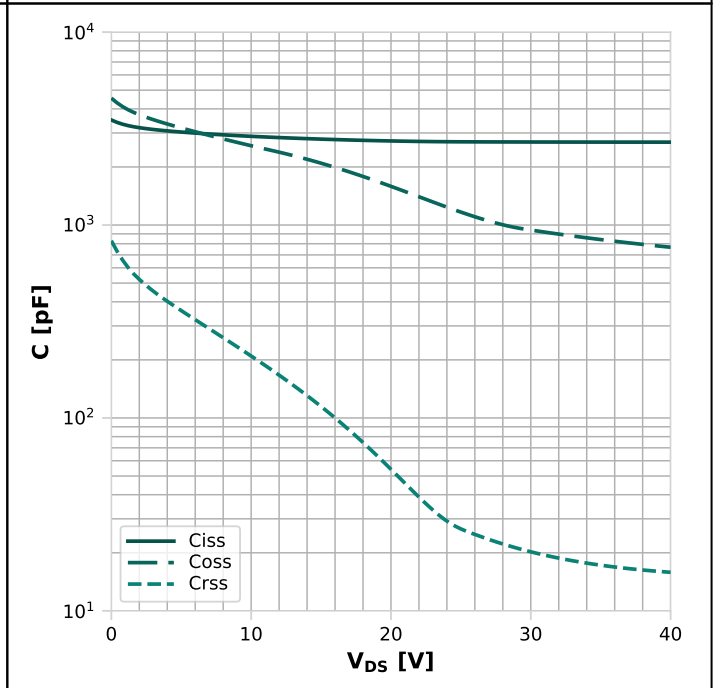
$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$

Diagram 9: Typ. gate threshold voltage



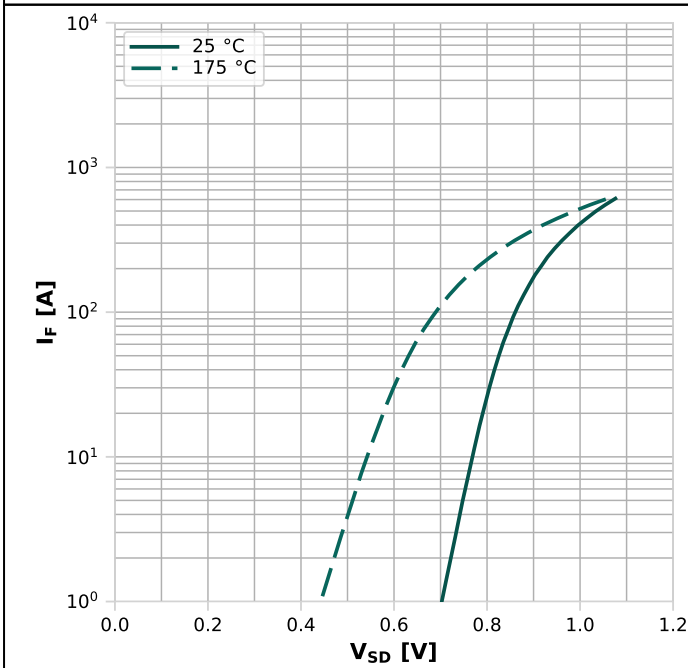
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS};$ parameter: I_D

Diagram 10: Typ. capacitances



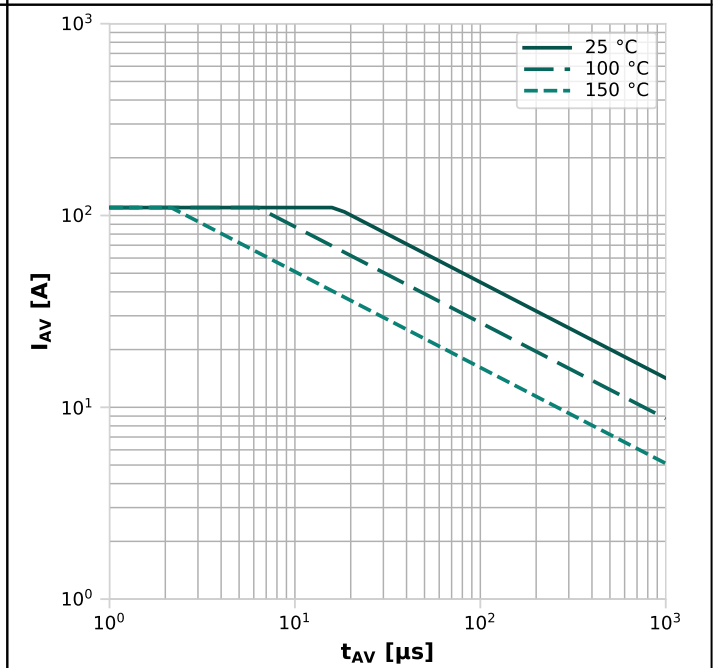
$C=f(V_{DS}); V_{GS}=0$ V; $f=1$ MHz

Diagram 11: Typ. forward diode characteristics



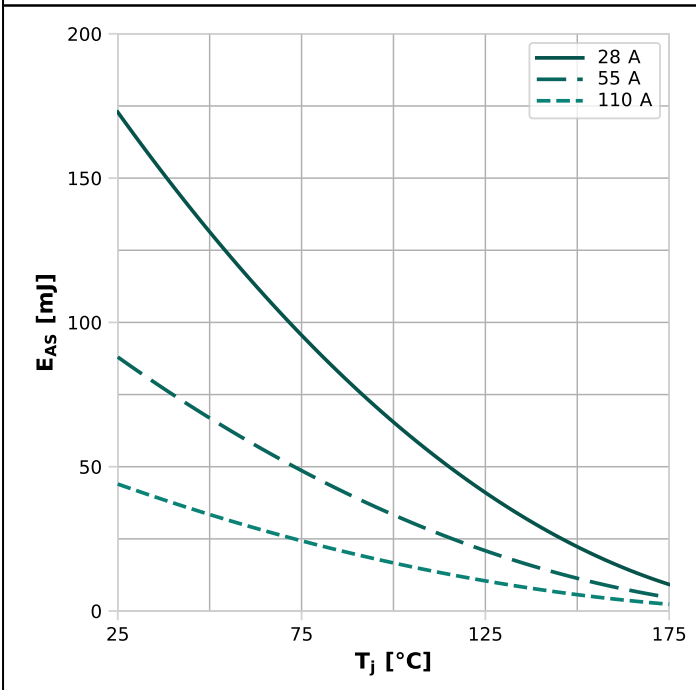
$I_F=f(V_{SD});$ parameter: T_j

Diagram 12: Typ. avalanche characteristics



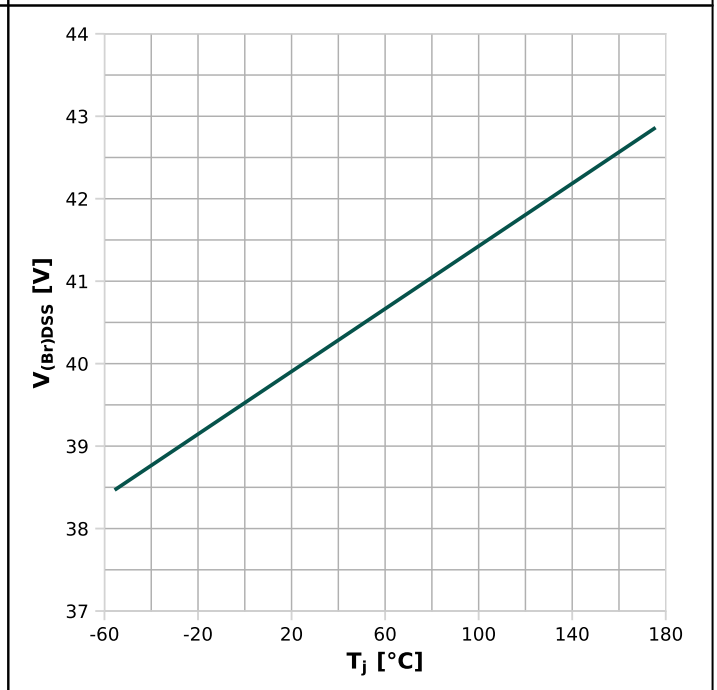
$I_{AS}=f(t_{AV});$ parameter: $T_{j(start)}$

Diagram 13: Typical avalanche Energy



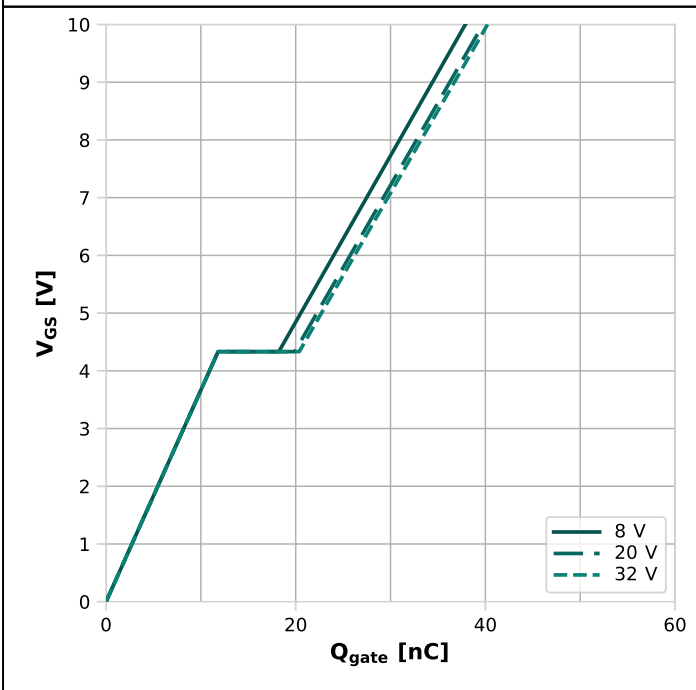
$E_{AS}=f(T_j)$; parameter: I_D

Diagram 14: Drain-source breakdown voltage



$V_{(Br)DSS}=f(T_j)$; $I_D=1\text{ mA}$

Diagram 15: Typ. gate charge



$V_{GS}=f(Q_{gate})$; $I_D=90\text{ A pulsed}$; parameter: V_{DD}

5 Test circuits

Table 8 Diode characteristics

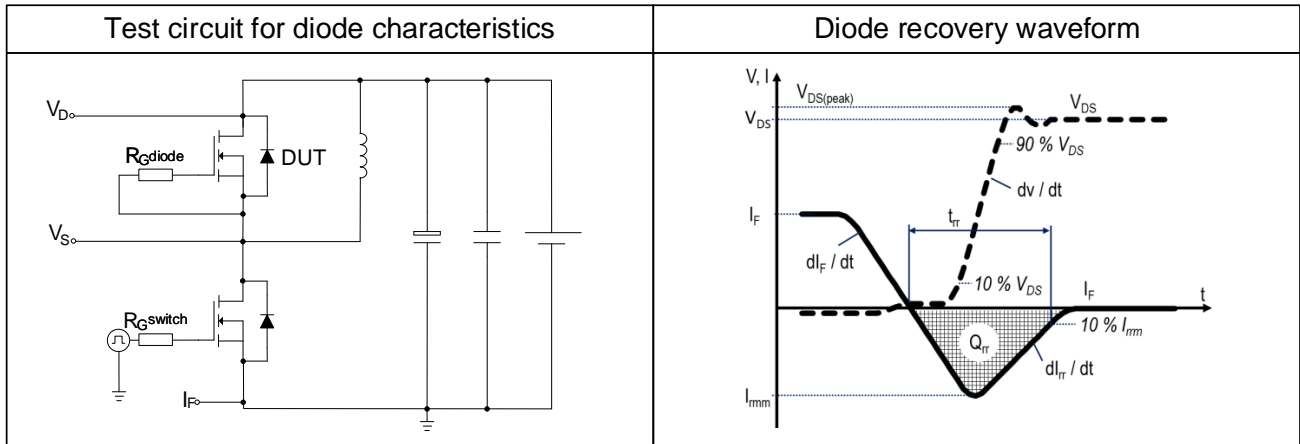


Table 9 Unclamped inductive load test circuit

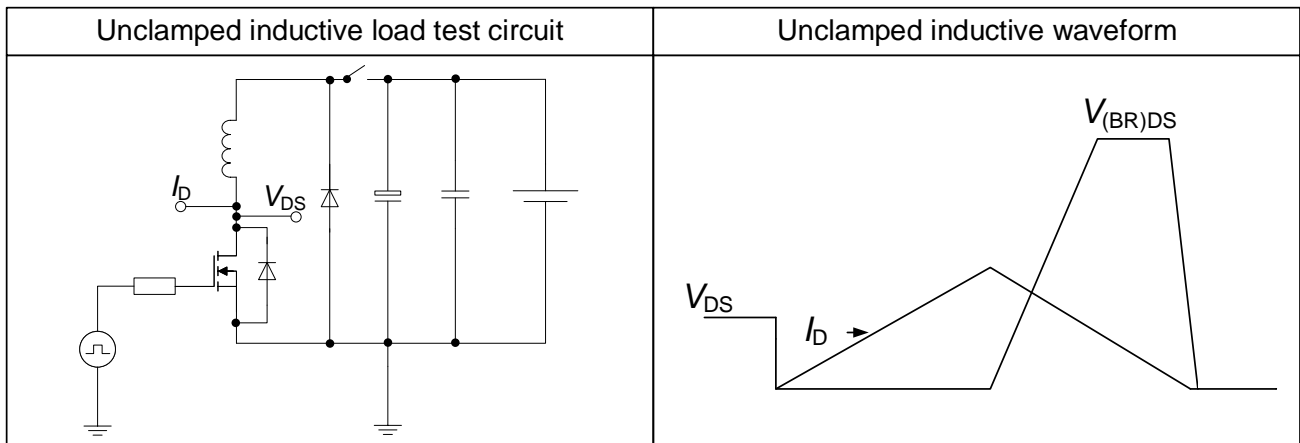
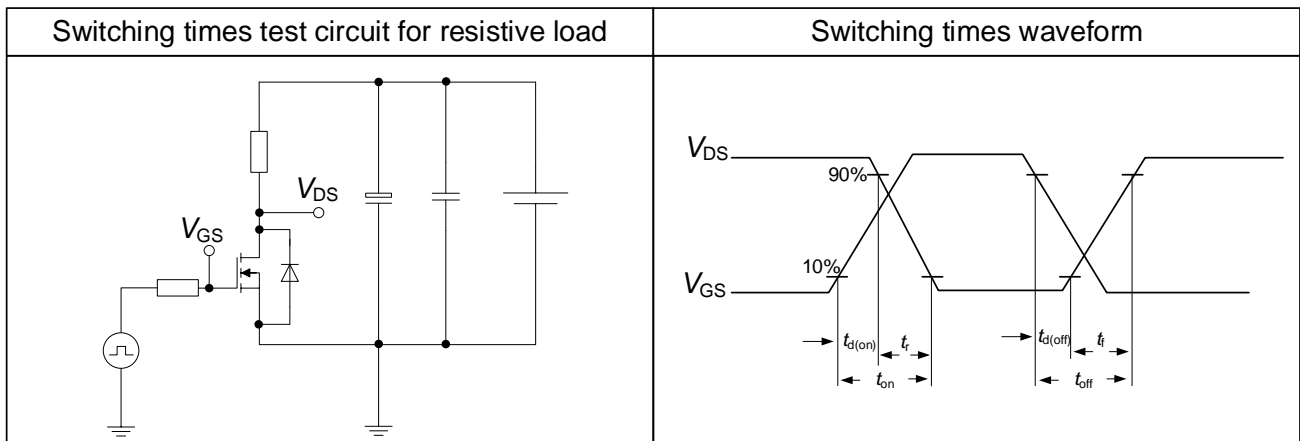
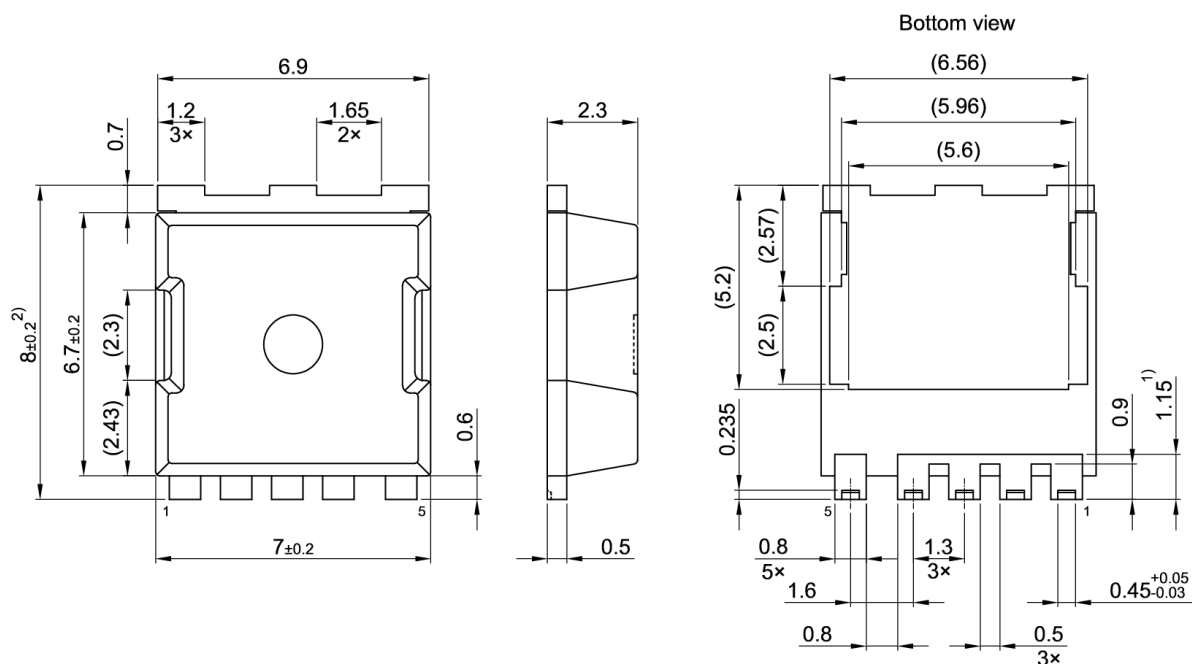


Table 10 Switching times test circuit for resistive load




6 Package outlines



1) Lead length up to anti flash profile; mold flashes excluded.

2) Excluding burr.

All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Drawing according to ISO 8015, general tolerances $\pm 0.1; \pm 1^\circ 30'$

Figure 1 Outline PG-HSOF-5, dimensions in mm

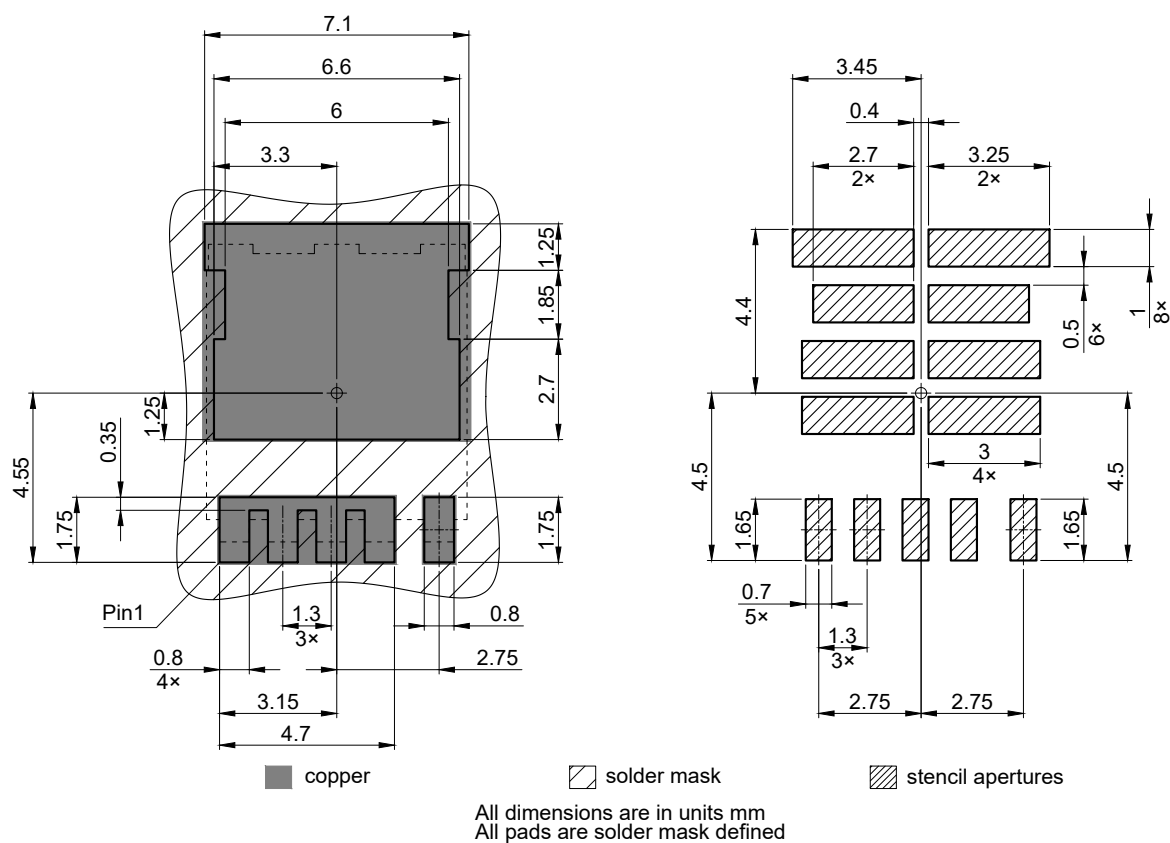
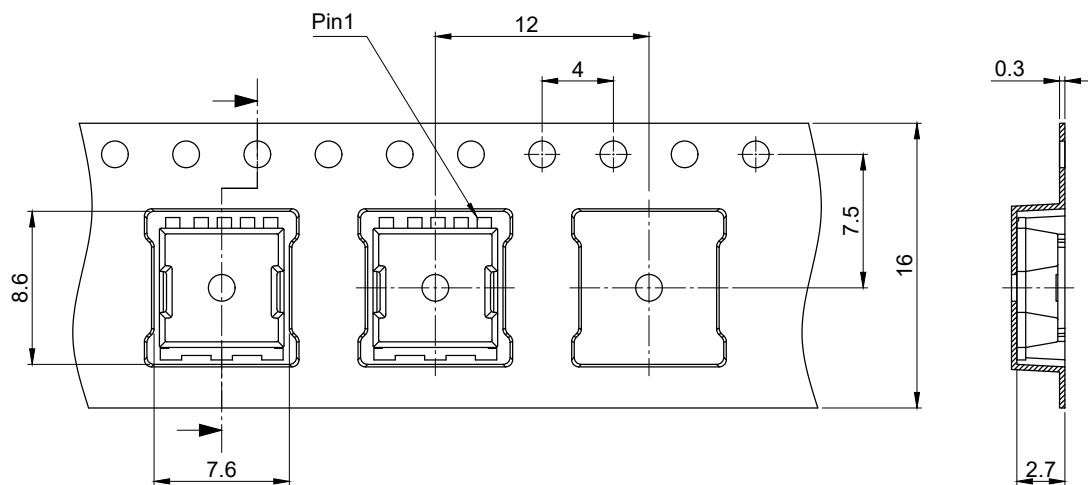


Figure 2 Footprint drawing PG-HSOF-5, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-5, dimensions in mm

7 Appendix A

Table 11 Related links

- [IFX Optimos™ Power-Transistor Webpage](#)



Revision history

IAUAN04S7N012

Revision 2026-01-14, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-01-14	Final Datasheet

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