

Automotive MOSFET

OptiMOS™ 7 Power-Transistor

PG-HSOF-8

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

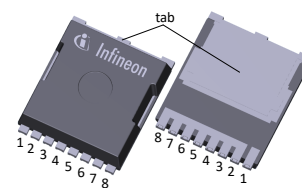
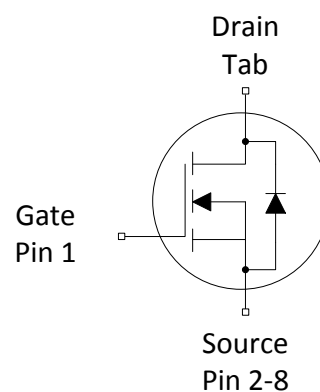
General automotive applications.

Product validation

Qualified for Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	1.26	mΩ
I_D (chip limited)	349	A



Part number	Package	Marking	Related links
IAUTN10S7N013	PG-HSOF-8	7N10N013	see Appendix A

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1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	349	A	Chip limitation, $V_{GS} = 10\text{ V}$ ^{1) 2)}
				349		DC current, $V_{GS} = 10\text{ V}$
				43		R_{thJA} on 2s2p, $V_{GS} = 10\text{ V}$, $T_a = 100\text{ °C}$ ^{1) 3)}
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	1282	A	$T_C = 25\text{ °C}$, $t_p = 100\text{ }\mu\text{s}$
Avalanche energy, single pulse ¹⁾	E_{AS}	-	-	355	mJ	$I_D = 100\text{ A}$
Avalanche current, single pulse	I_{AS}	-	-	200	A	-
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	333	W	$T_C = 25\text{ °C}$
Operating temperature	T_j	-55	-	175	°C	-

¹⁾ The parameter is not subject to production testing - specified by design.

²⁾ The current is limited by the overall system design, including the customer-specific PCB.

³⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case 4)	R_{thJC}	-	-	0.46	K/W	-
Thermal resistance, junction - ambient 5) 4)	R_{thJA}		14.9	-		

4) The parameter is not subject to production testing - specified by design.

5) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$
Gate threshold voltage	$V_{GS(th)}$	2.3	2.8	3.2	V	$V_{DS} = V_{GS}$, $I_D = 245\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 100\text{ V}$, $T_j = 25^\circ\text{C}$, $V_{GS} = 0\text{ V}$
				61		$V_{DS} = 100\text{ V}$, $T_j = 100^\circ\text{C}$, $V_{GS} = 0\text{ V}$ 6)
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.26	1.45	m Ω	$I_D = 50\text{ A}$, $V_{GS} = 7\text{ V}$
			1.15	1.26		$I_D = 100\text{ A}$, $V_{GS} = 10\text{ V}$
Gate resistance 6)	R_G	-	1.3	-	Ω	-

6) The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	10380	13490	pF	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		4340	5640		
Reverse transfer capacitance ⁷⁾	C_{rss}		41	61		
Turn-on delay time ⁷⁾	$t_{d(on)}$	-	26	-	ns	$I_D = 100\text{ A}$, $V_{GS} = 10\text{ V}$, $V_{DD} = 50\text{ V}$, $R_G = 3.5\ \Omega$
Rise time ⁷⁾	t_r		24			
Turn-off delay time ⁷⁾	$t_{d(off)}$		61			
Fall time ⁷⁾	t_f		31			

⁷⁾ The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁸⁾	Q_{gs}	-	47	60	nC	$I_D = 100\text{ A}$, $V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$ to 10 V
Gate to drain charge ⁸⁾	Q_{gd}		23	35	nC	
Gate charge total ⁸⁾	Q_g		144	187	nC	
Gate plateau voltage ⁸⁾	$V_{plateau}$		4.4	-	V	

⁸⁾ The parameter is not subject to production testing - specified by design.

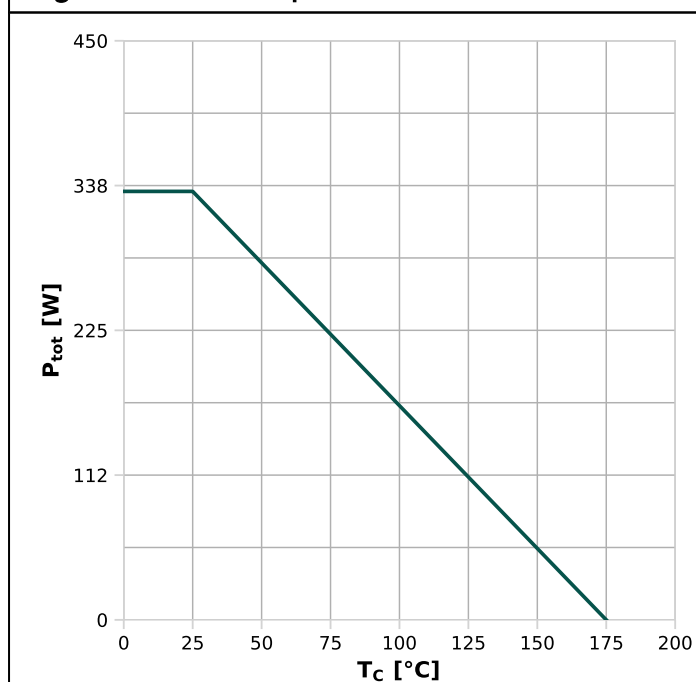
Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current ⁹⁾	I_S	-	-	349	A	$T_C = 25\text{ °C}$
Diode pulse current ⁹⁾	$I_{S,pulse}$	-	-	1282	A	$T_C = 25\text{ °C}$, $t_p = 100\ \mu\text{s}$
Diode forward voltage	V_{SD}	-	0.85	0.95	V	$T_J = 25\text{ °C}$, $V_{GS} = 0\text{ V}$, $I_F = 100\text{ A}$
Reverse recovery time ⁹⁾	t_{rr}	-	57	86	ns	$di_F/dt = 100\text{ A}/\mu\text{s}$, $V_R = 50\text{ V}$, $I_F = 50\text{ A}$
Reverse recovery charge ⁹⁾	Q_{rr}		57	114	nC	

⁹⁾ The parameter is not subject to production testing - specified by design.

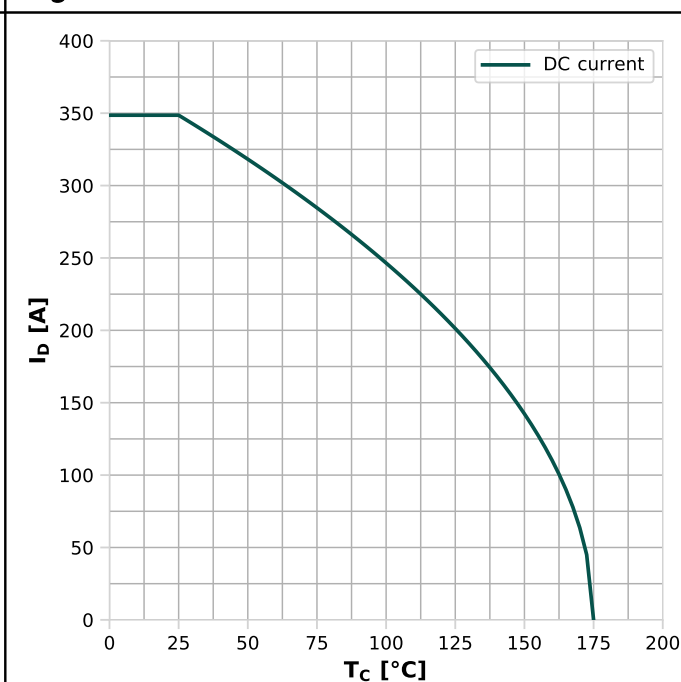
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



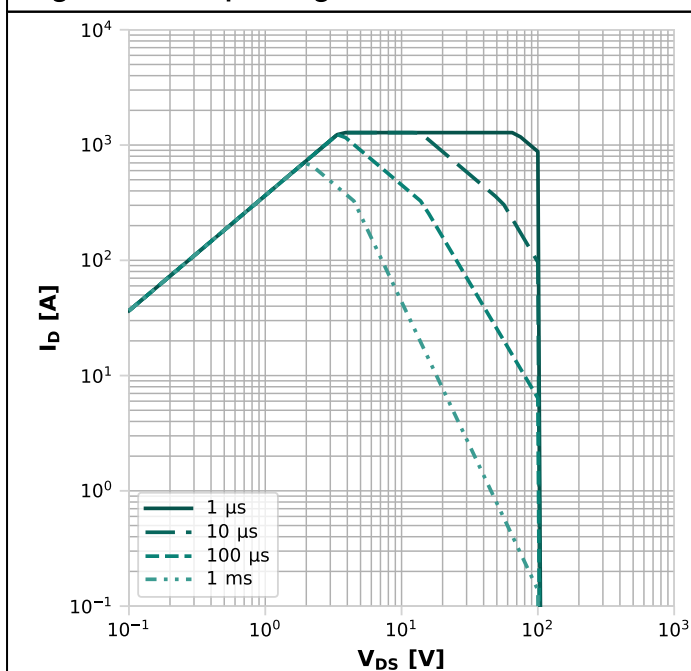
$$P_{tot}=f(T_c); V_{GS} \geq 6 V$$

Diagram 2: Drain Current



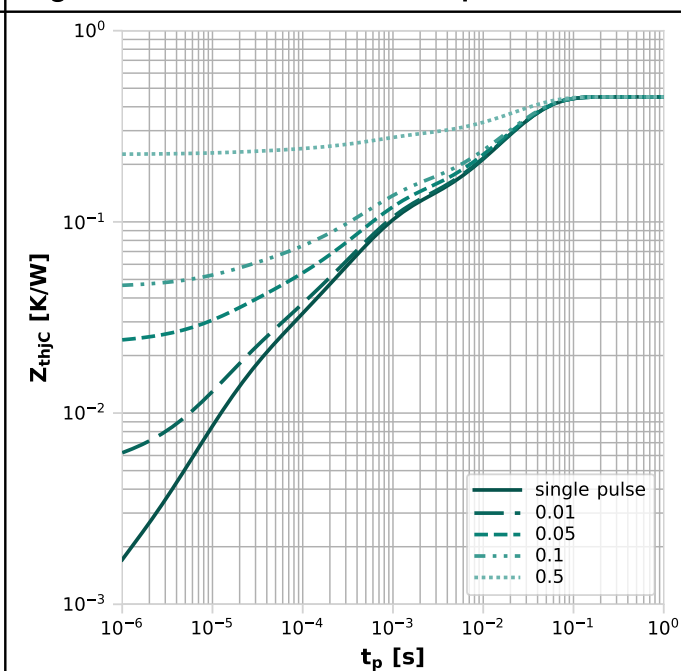
$$I_D=f(T_c); V_{GS} \geq 6 V$$

Diagram 3: Safe operating area



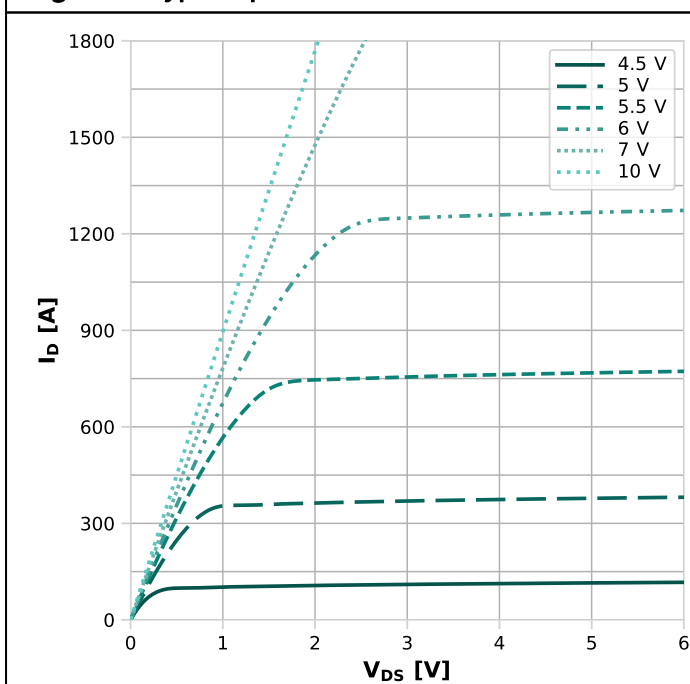
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



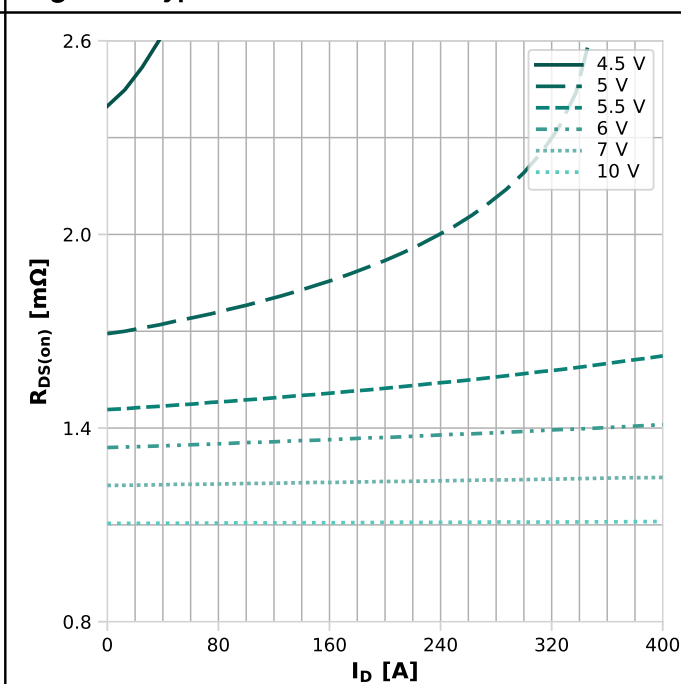
$$Z_{thjC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



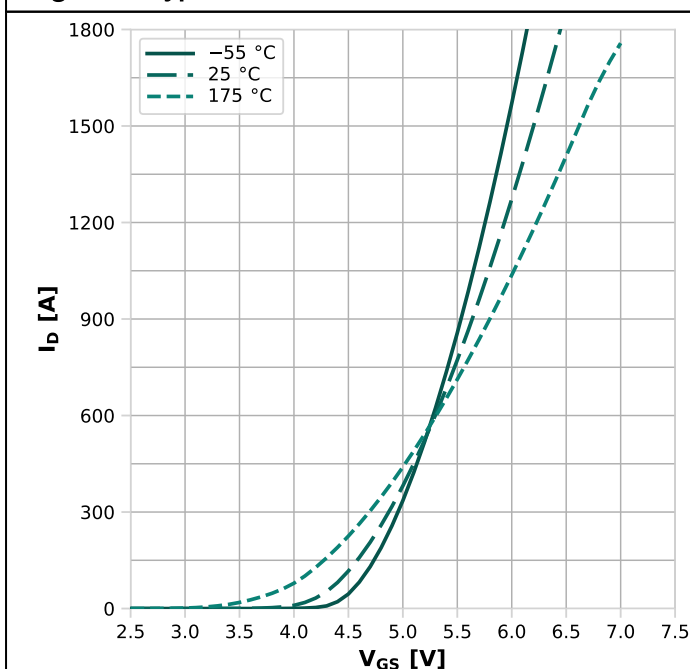
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on-state resistance



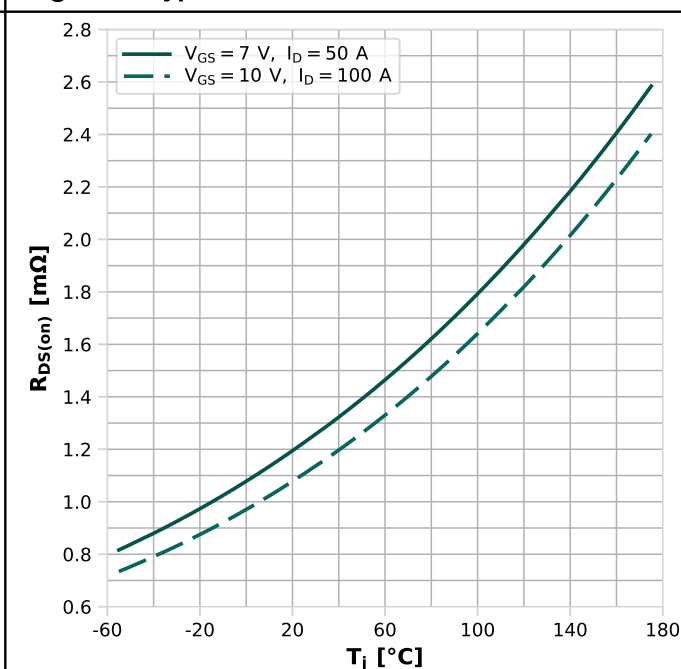
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



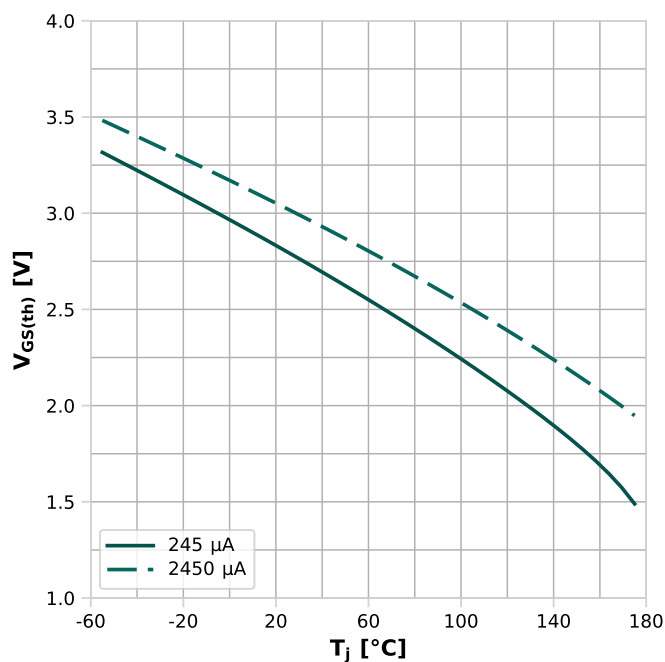
$I_D = f(V_{GS})$; $V_{DS} = 6\text{ V}$; parameter: T_j

Diagram 8: Typ. drain-source on-state resistance



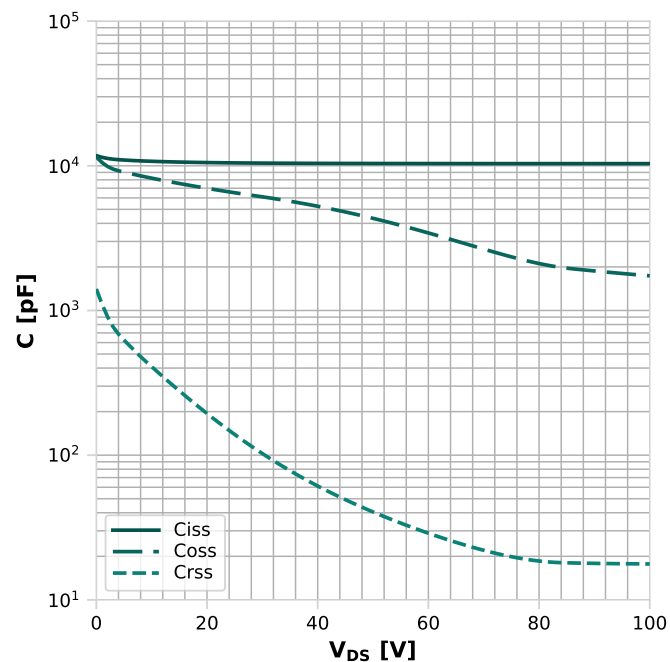
$R_{DS(on)} = f(T_j)$; parameter: I_D , V_{GS}

Diagram 9: Typ. gate threshold voltage



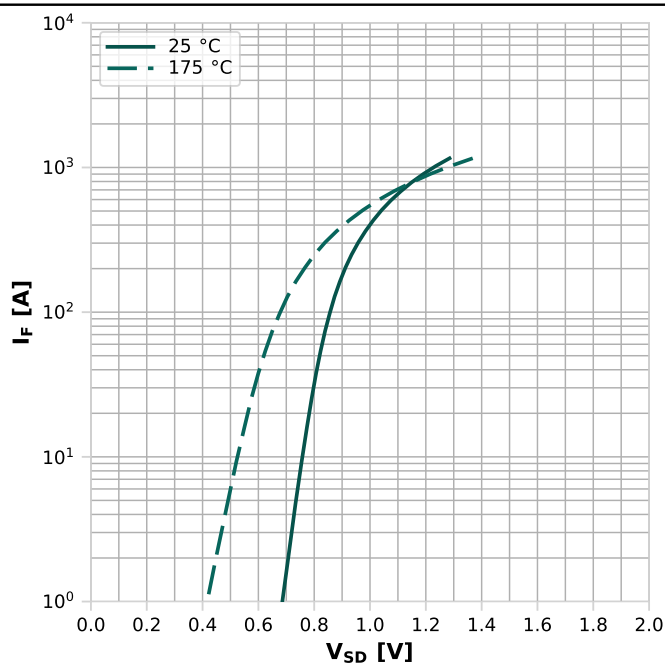
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D

Diagram 10: Typ. capacitances



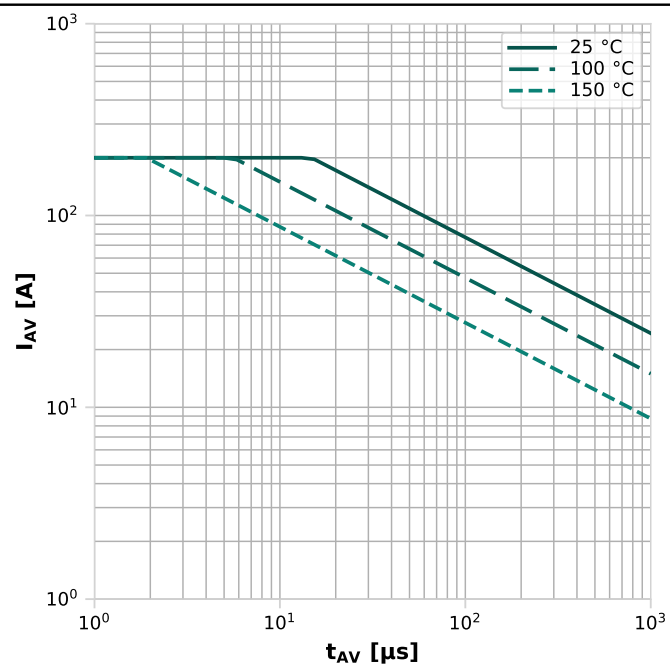
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 11: Typ. forward diode characteristics



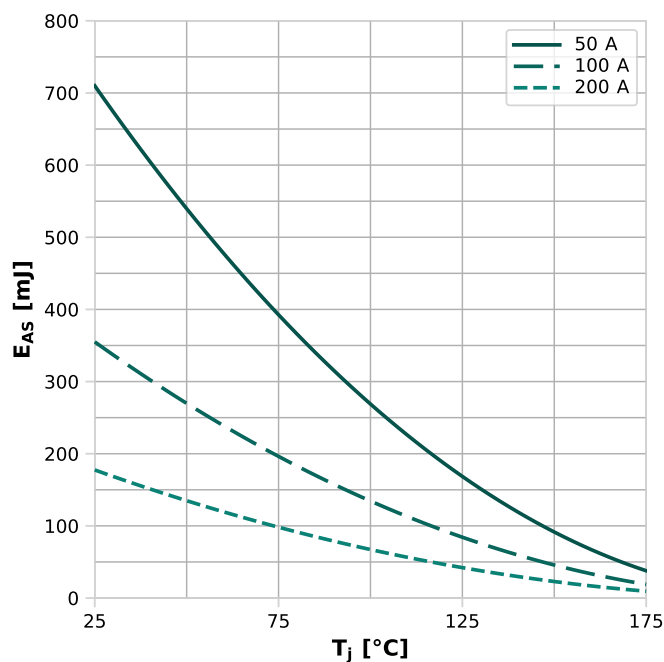
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Typ. avalanche characteristics



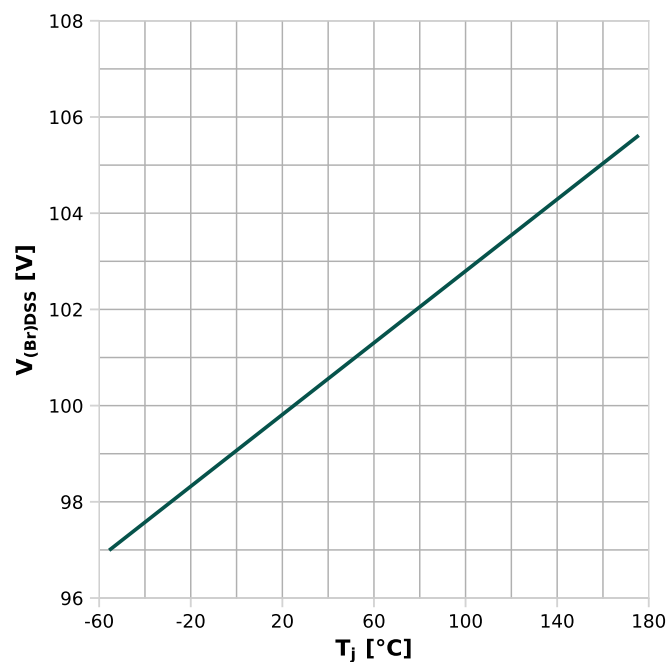
$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$

Diagram 13: Typical avalanche Energy



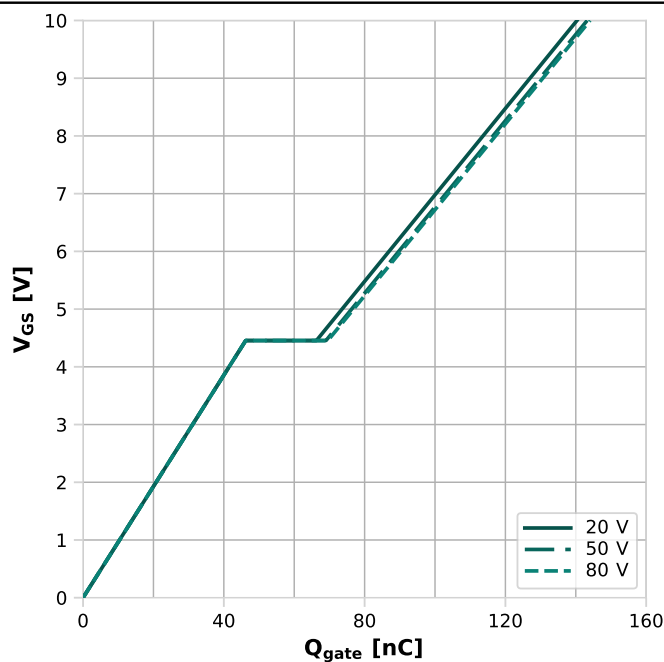
$E_{AS}=f(T_J)$; parameter: I_D

Diagram 14: Drain-source breakdown voltage



$V_{(BR)DSS}=f(T_J)$; $I_D=1\text{ mA}$

Diagram 15: Typ. gate charge



$V_{GS}=f(Q_{gate})$; $I_D=100\text{ A}$ pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Diode characteristics

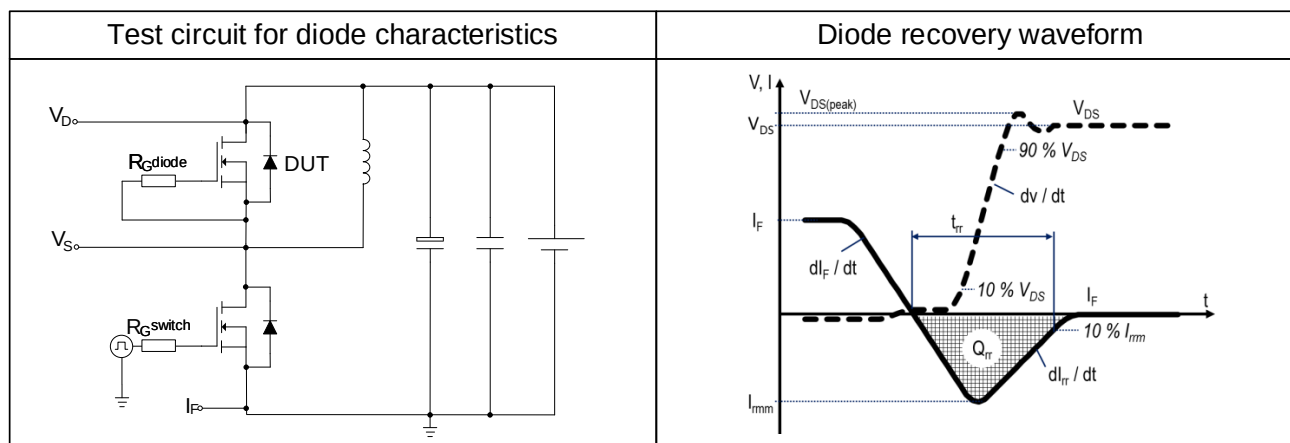


Table 9 Unclamped inductive load test circuit

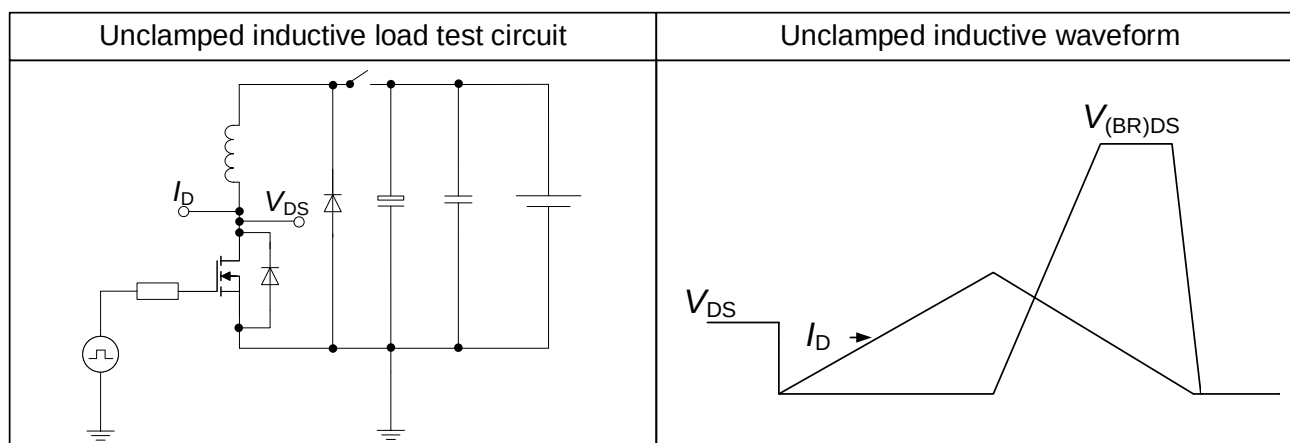
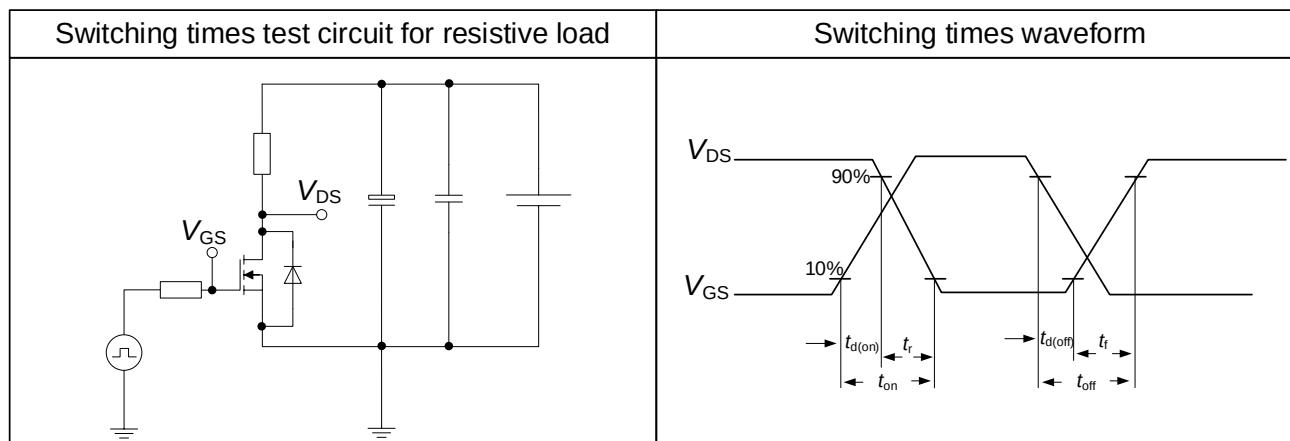
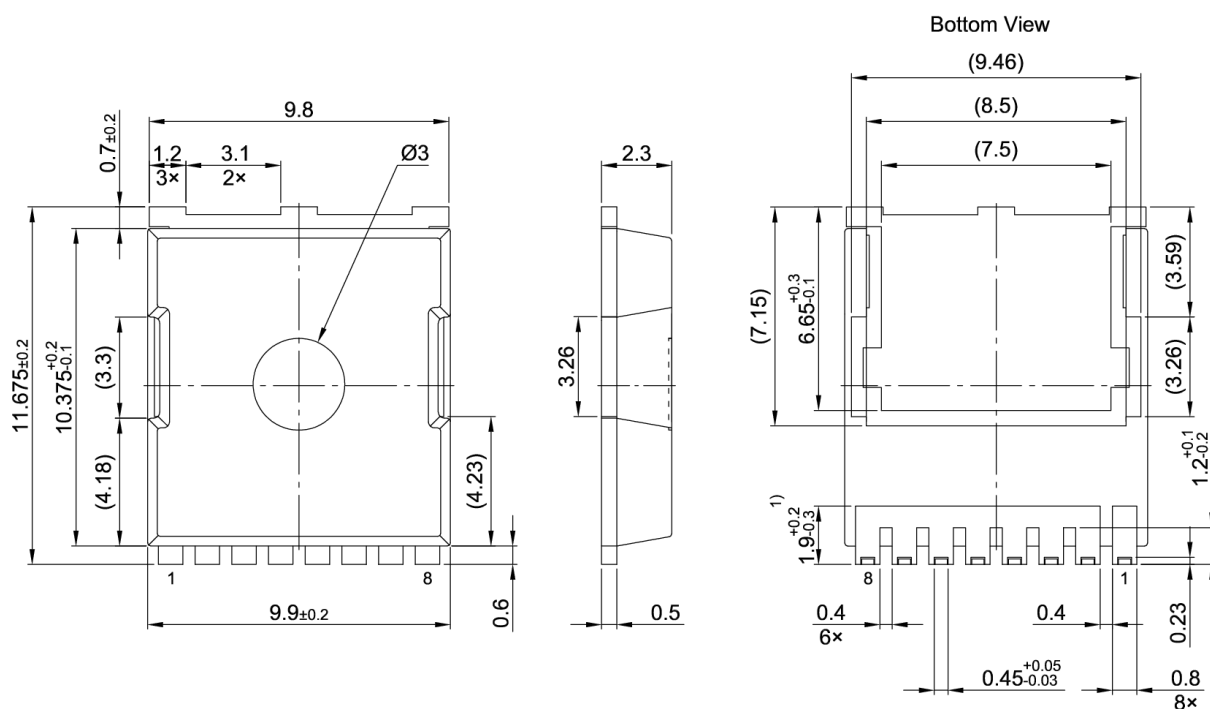


Table 10 Switching times test circuit for resistive load



6 Package outlines



1) Lead length up to anti flash profile; mold flashes excluded.

All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Drawing according to ISO 8015, general tolerances $\pm 0,1$; $\pm 1^\circ 30'$

Figure 1 Outline PG-HSOF-8, dimensions in mm

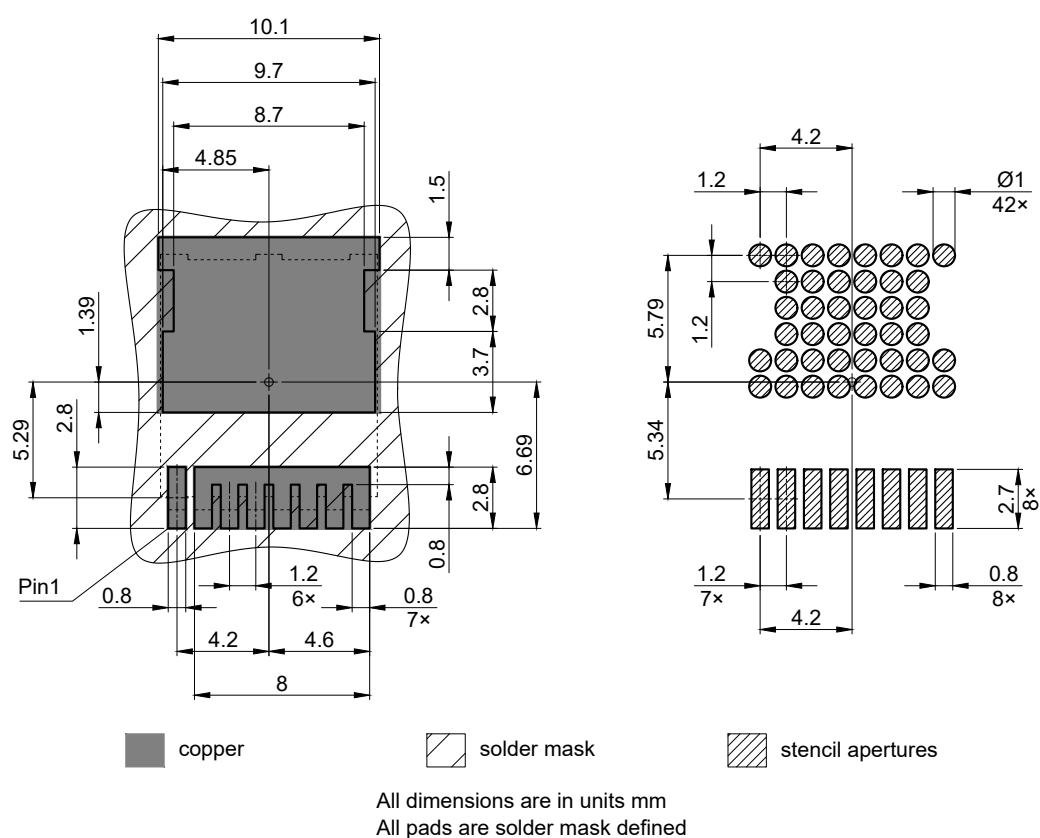
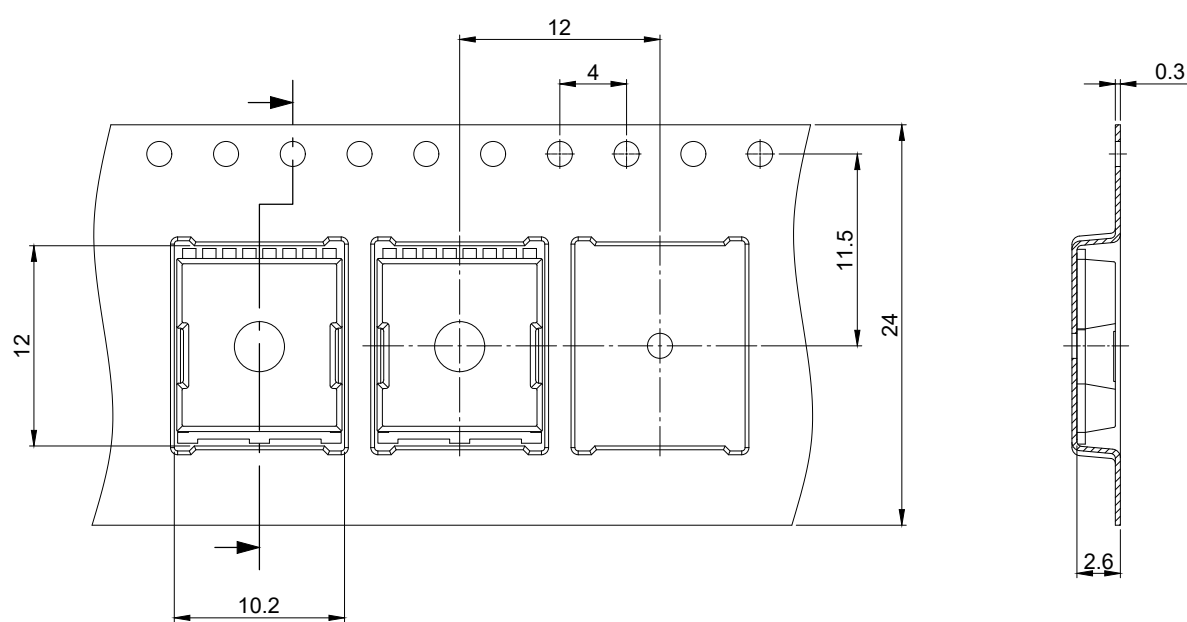


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 **Related links**

- IFX Optimos™ Power-Transistor Webpage

Revision history

IAUTN10S7N013

Revision 2026-09-28, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-09-28	Final datasheet

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