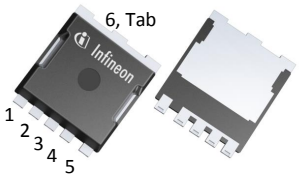
Automotive MOSFET

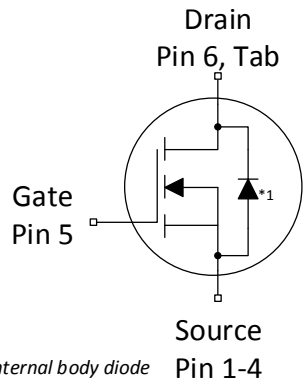
OptiMOS™ 7 LinearFET 40 V

PG-HSOF-5



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL2a up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- 100% Safe Operating Area tested
- Enhanced Safe Operating Area
- High current precision enabling paralleling in linear operation



*1: Internal body diode

Potential applications

- Battery main switch, e-fuse switch, backup-supply switch
- In-rush current limitation (e.g. capacitor charging)
- Slow-switching to minimize voltage discontinuities
- Active clamping (over-voltage limitation)

Product validation

Qualified for Automotive applications.
Product validation according to AEC-Q101.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on)}$ at V_{GS} = 12 V	0.93	mΩ
I_D(chip limited)	281	A

AEC Qualified

Extended quality

RoHS

Part number	Package	Marking	Related links
IAUAN04S7S009	PG-HSOF-5	7N04S009	-

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1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	281	A	Chip limitation, V_{GS} = 12 V [1) 2)]
				180		DC current, V_{GS} = 12 V
				43		R_{thJA} on 2s2p, V_{GS} = 12 V, T_a = 100 °C [1) 3)]
Pulsed drain current [1)]	$I_{D,pulse}$	-	-	860	A	T_C = 25 °C, t_p = 100 µs
Avalanche energy, single pulse [1)]	E_{AS}	-	-	152	mJ	I_D = 70 A
Avalanche current, single pulse	I_{AS}	-	-	140	A	-
Gate source voltage	V_{GS}	-20		20	V	
Power dissipation	P_{tot}	-	-	133	W	T_C = 25 °C
Operating temperature	T_j	-55	-	175	°C	-

1) The parameter is not subject to production testing - specified by design.

2) The current is limited by the overall system design, including the customer-specific PCB.

3) Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [4]	R_{thJC}	-	-	1.12	K/W	-
Thermal resistance, junction - ambient [4] [5]	R_{thJA}		23.6	-		

[4] The parameter is not subject to production testing - specified by design.

[5] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	I_D = 1 mA, V_{GS} = 0 V
Gate threshold voltage	$V_{GS(th)}$	2.3	2.6	2.9	V	V_{DS}=V_{GS}, I_D = 1.9 µA
Current limit precision	$I_{D,lim}$	11	17	29	A	V_{DS} = 14 V, V_{GS} = 5.1 V
		27	38	58		V_{DS} = 14 V, V_{GS} = 6.0 V
		38	54	96		V_{DS} = 14 V, V_{GS} = 6.5 V
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS} = 40 V, T_J = 25 °C, V_{GS} = 0 V
				16		V_{DS} = 40 V, T_J = 100 °C, V_{GS} = 0 V [6]
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{DS} = 0 V, V_{GS} = 20 V
Drain-source on-state resistance	$R_{DS(on)}$	-	11.8	24.1	mΩ	I_D = 21 A, V_{GS} = 7 V
			0.96	1.36		I_D = 41 A, V_{GS} = 10 V
			0.83	0.93		I_D = 41 A, V_{GS} = 12 V
			0.79	0.88		I_D = 41 A, V_{GS} = 14 V
Gate resistance [6]	R_G	-	1	-	Ω	-

[6] The parameter is not subject to production testing - specified by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	4130	5370	pF	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance [7]	C_{oss}		2150	2800		
Reverse transfer capacitance [7]	C_{rss}		65	117		
Turn-on delay time [7]	$t_{d(on)}$	-	13	-	ns	I_D = 41 A, V_{GS} = 10 V, V_{DD} = 20 V, R_G = 3.5 Ω
Rise time [7]	t_r		24			
Turn-off delay time [7]	$t_{d(off)}$		15			
Fall time [7]	t_f		20			

[7] The parameter is not subject to production testing - specified by design.

Table 6 Gate Charge Characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge [8]	Q_{gs}	-	26	33	nC	I_D = 41 A, V_{DS} = 20 V, V_{GS} = 0 V to 10 V
Gate to drain charge [8]	Q_{gd}		13	19	nC	
Gate charge total [8]	Q_g		61	79	nC	
Gate plateau voltage [8]	$V_{plateau}$		6.2	-	V	

[8] The parameter is not subject to production testing - specified by design.

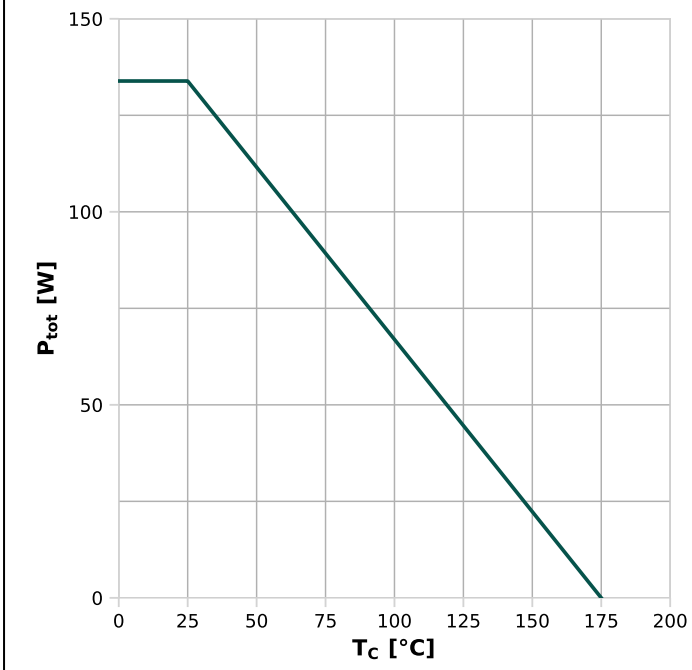
Table 7 Reverse Diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	180	A	T_C = 25 °C
Diode pulse current [9]	$I_{S,pulse}$	-	-	860	A	T_C = 25 °C, t_p = 100 µs
Diode forward voltage	V_{SD}	-	0.8	0.95	V	T_J = 25 °C, V_{GS} = 0 V, I_F = 41 A
Reverse recovery time [9]	t_{rr}	-	41	62	ns	di_F/dt =100 A/µs, V_R = 20 V, I_F = 50 A
Reverse recovery charge [9]	Q_{rr}		33	66	nC	

[9] The parameter is not subject to production testing - specified by design.

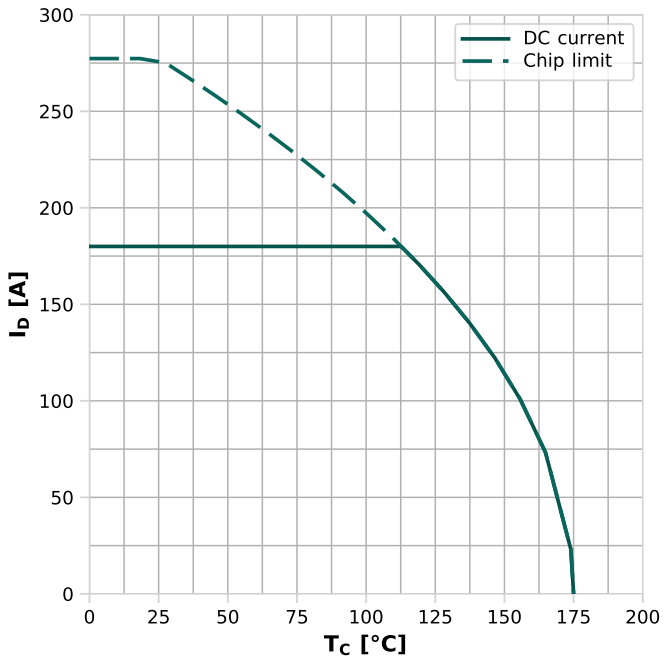
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



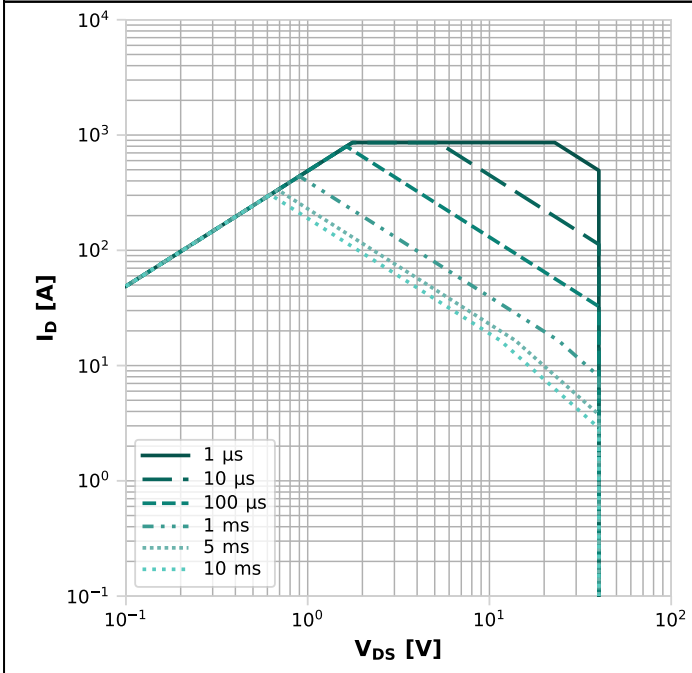
$P_{tot}=f(T_C)$; $V_{GS} \geq 12$ V

Diagram 2: Drain Current



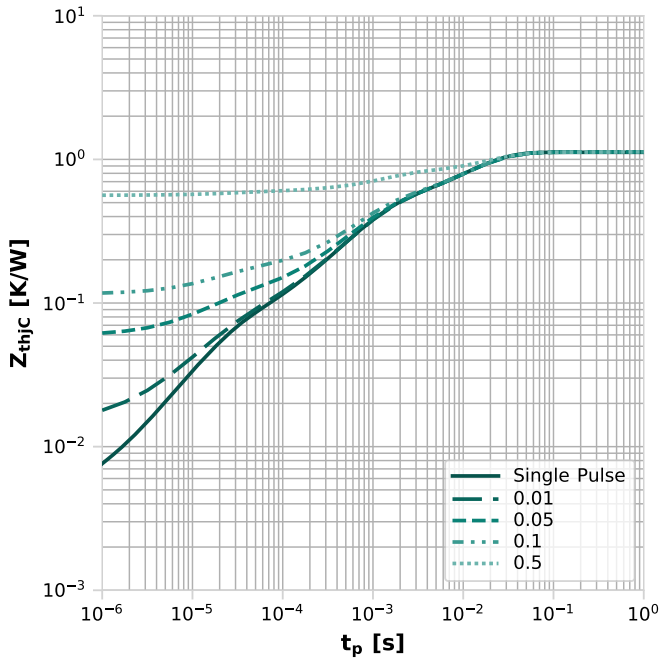
$I_D=f(T_C)$; $V_{GS} \geq 12$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C= 25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



$Z_{thjC}=f(t_p)$; parameter: $D=t_p/T$

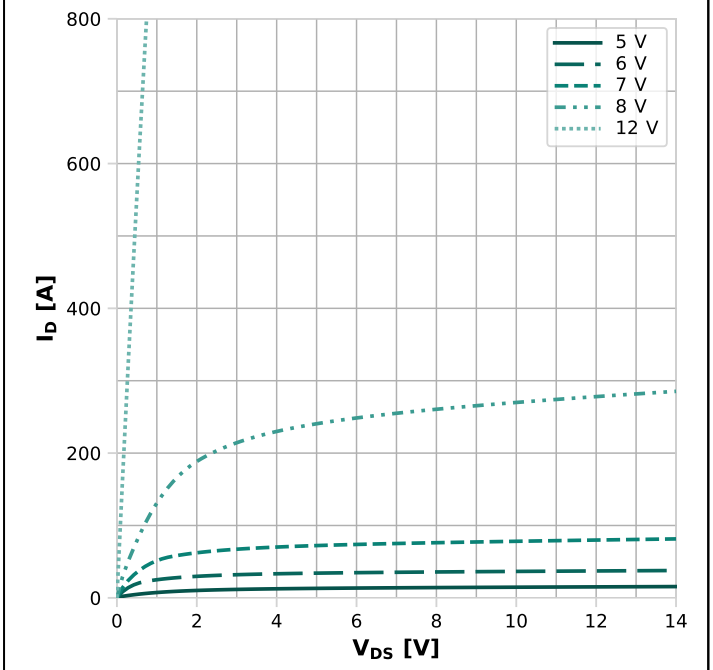
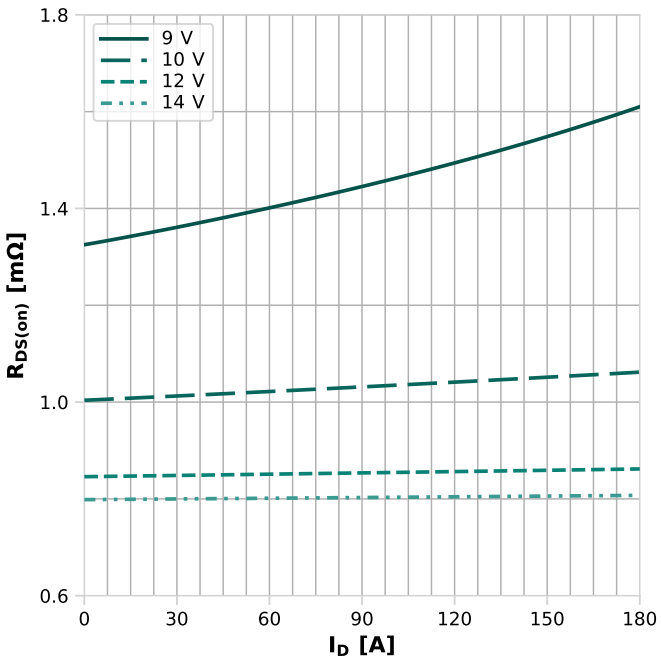
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on-state resistance
	
$I_D=f(V_{DS})$; T_j= 25 °C, parameter: V_{GS}	$R_{DS(on)}=f(I_D)$; T_j= 25 °C; parameter: V_{GS}

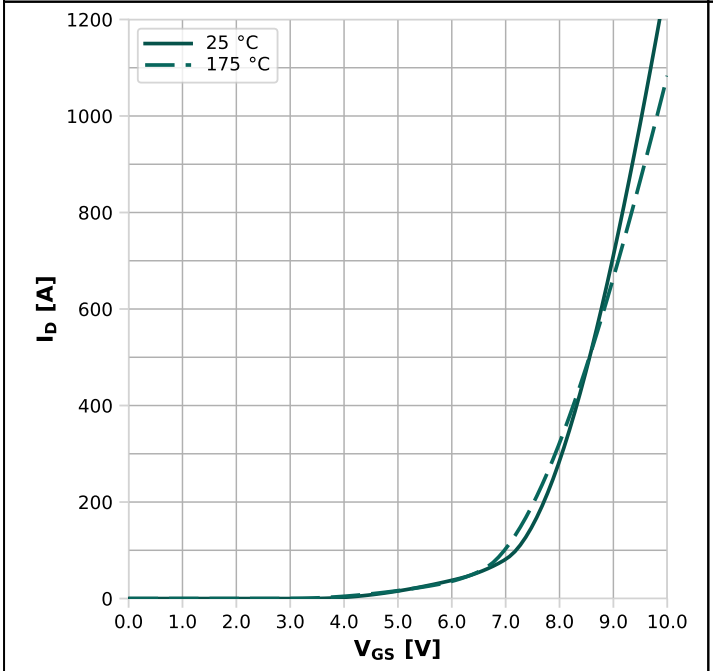
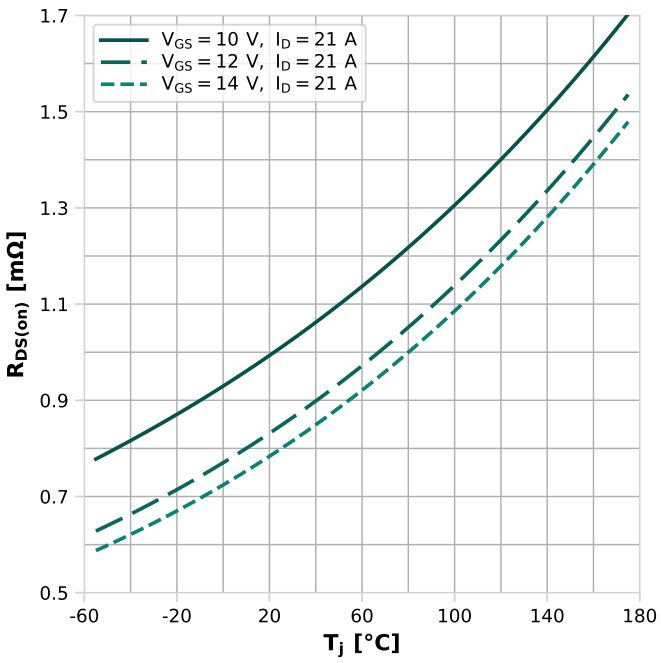
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on-state resistance
	
$I_D=f(V_{GS})$; V_{DS}= 14 V; parameter: T_j	$R_{DS(on)}=f(T_j)$; parameter: I_D, V_{GS}

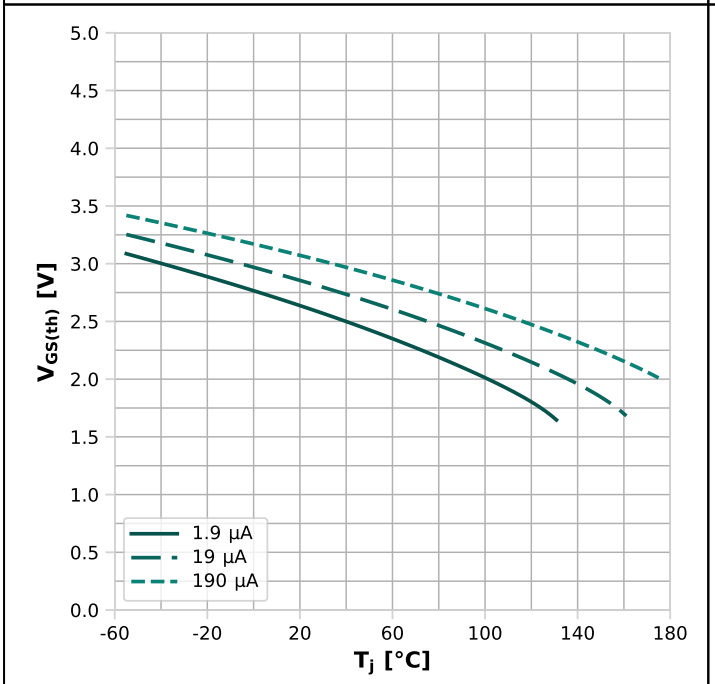
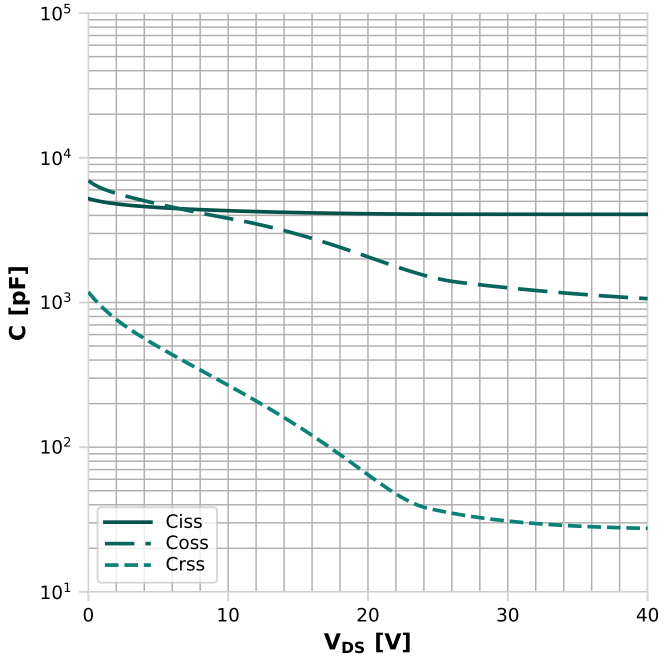
Diagram 9: Typ. gate threshold voltage	Diagram 10: Typ. capacitances
	
$V_{GS(th)}=f(T_j)$; $V_{GS}= V_{DS}$; parameter: I_D	$C=f(V_{DS})$; $V_{GS}= 0$ V; f=1 MHz

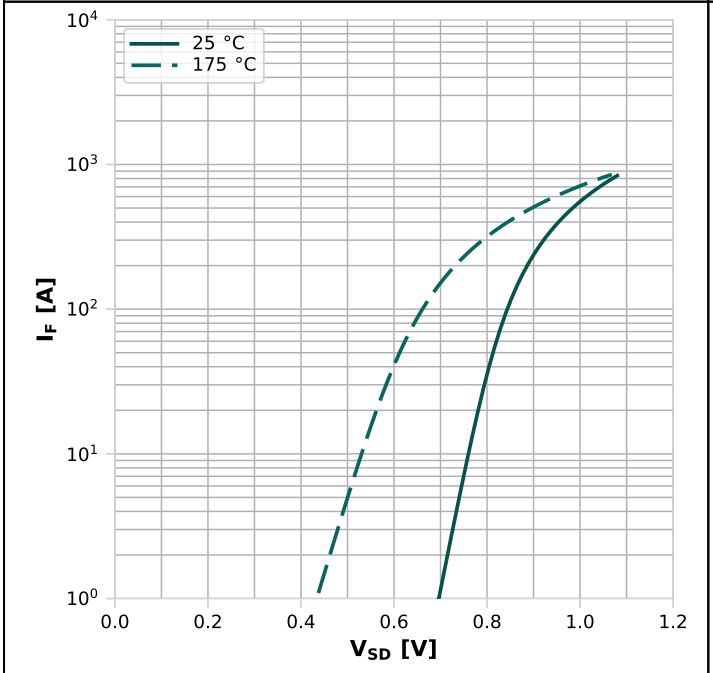
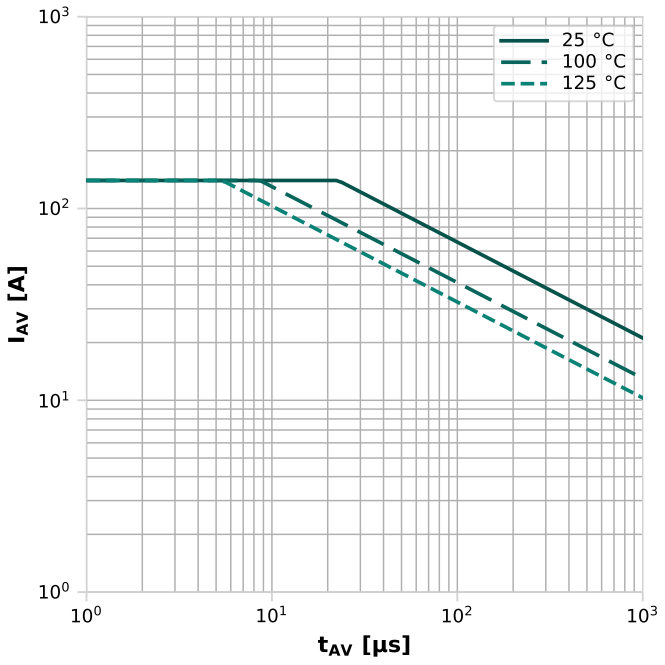
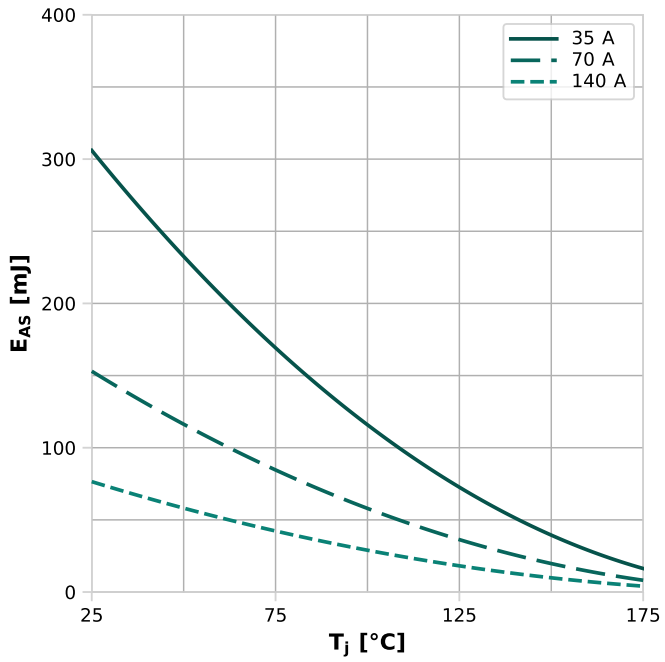
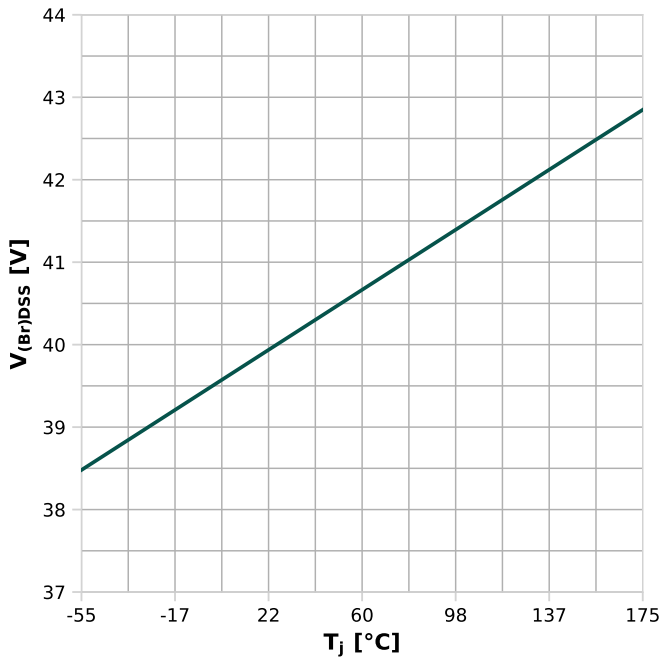
Diagram 11: Typ. forward diode characteristics	Diagram 12: Typ. avalanche characteristics
	
$I_F=f(V_{SD})$; parameter: T_j	$I_{AS}=f(t_{AV})$; parameter: $T_{j(start)}$

Diagram 13: Typical avalanche Energy



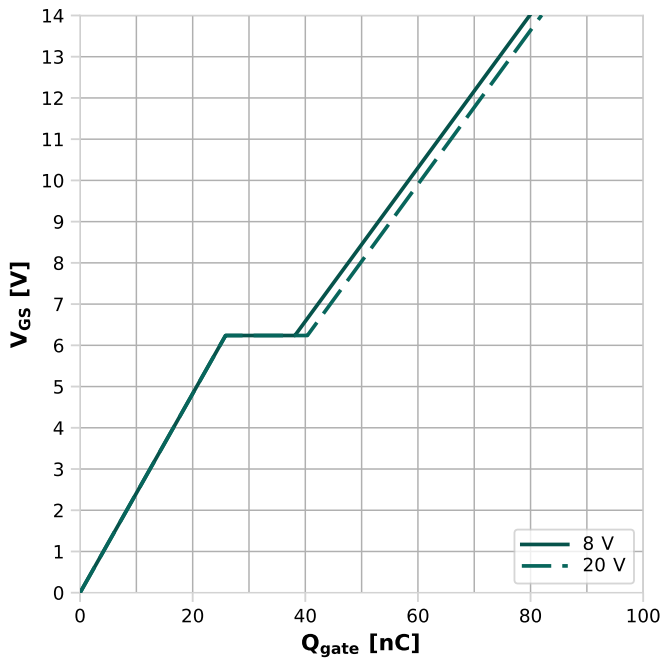
$E_{AS}=f(T_j)$; parameter: I_D

Diagram 14: Drain-source breakdown voltage



$V_{(Br)DSS}=f(T_j)$; I_D= 10 mA

Diagram 15: Typ. gate charge



$V_{GS}=f(Q_{gate})$; I_D= 41 A pulsed; parameter: V_{DD}

5 Test circuits

Table 8 Diode characteristics

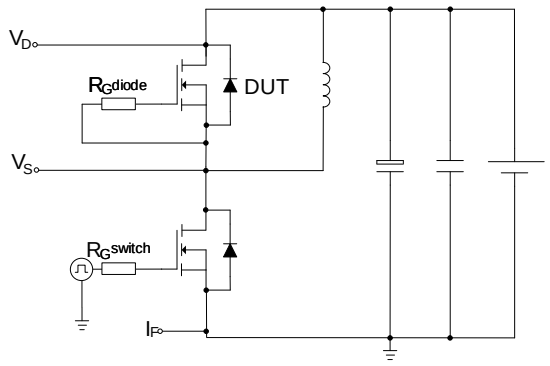
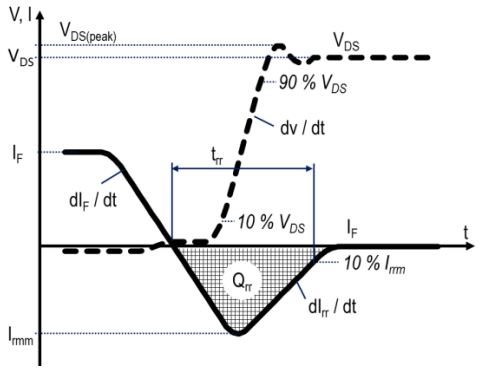
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Unclamped inductive load test circuit

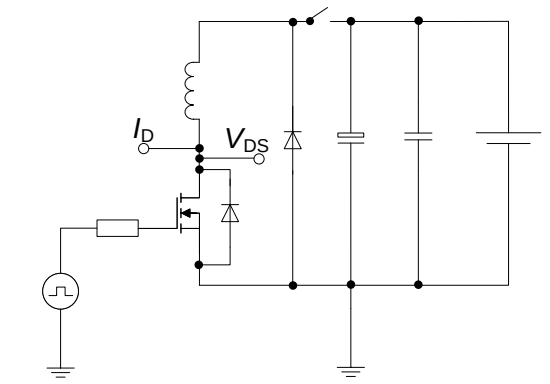
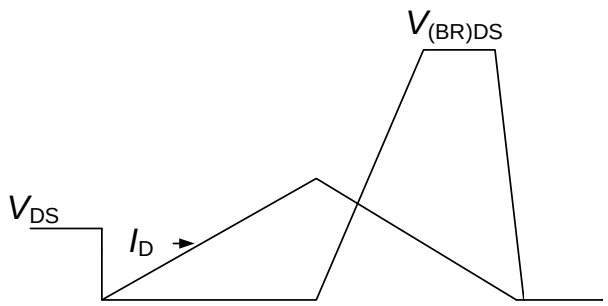
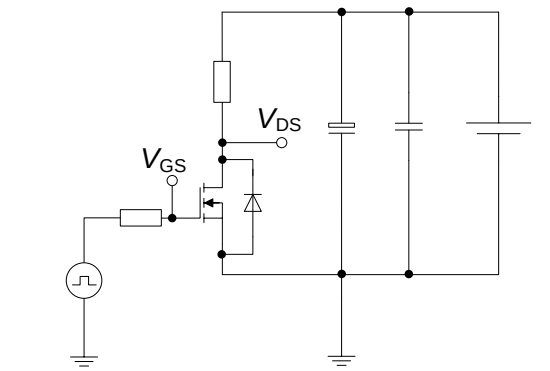
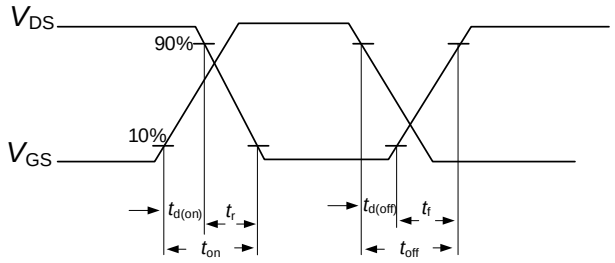
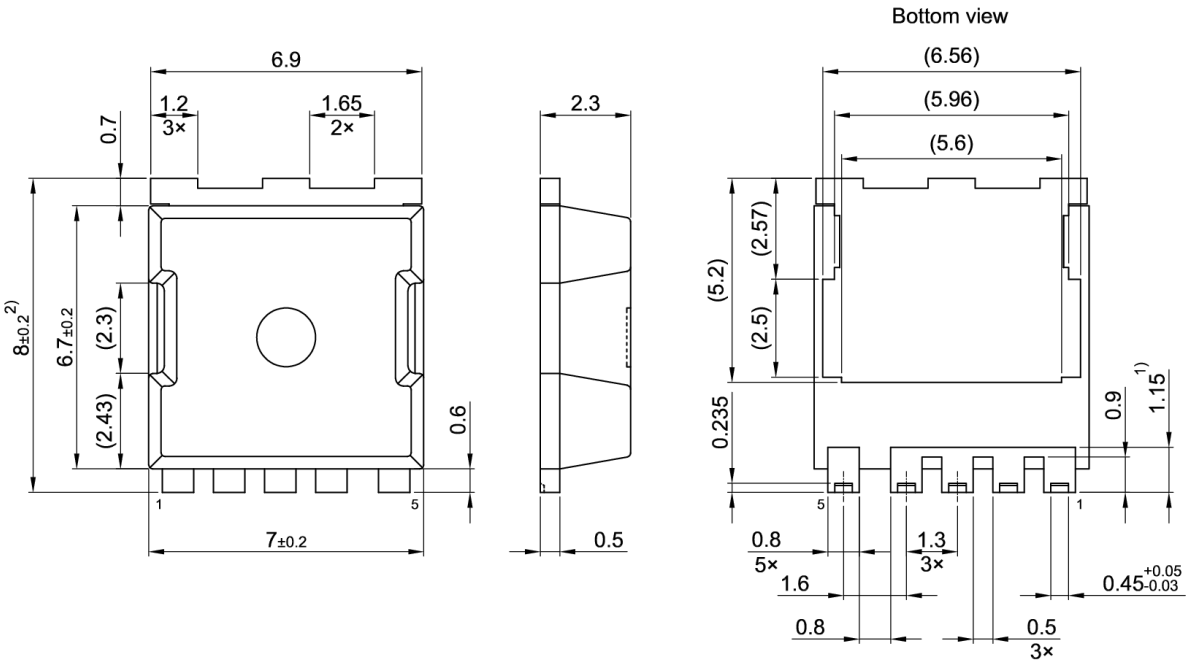
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 10 Switching times test circuit for resistive load

Switching times test circuit for resistive load	Switching times waveform
	

6 Package outlines



1) Lead length up to anti flash profile; mold flashes excluded.
2) Excluding burr.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ±0.1;±1°30'

Figure 1 Outline PG-HSOF-5, dimensions in mm

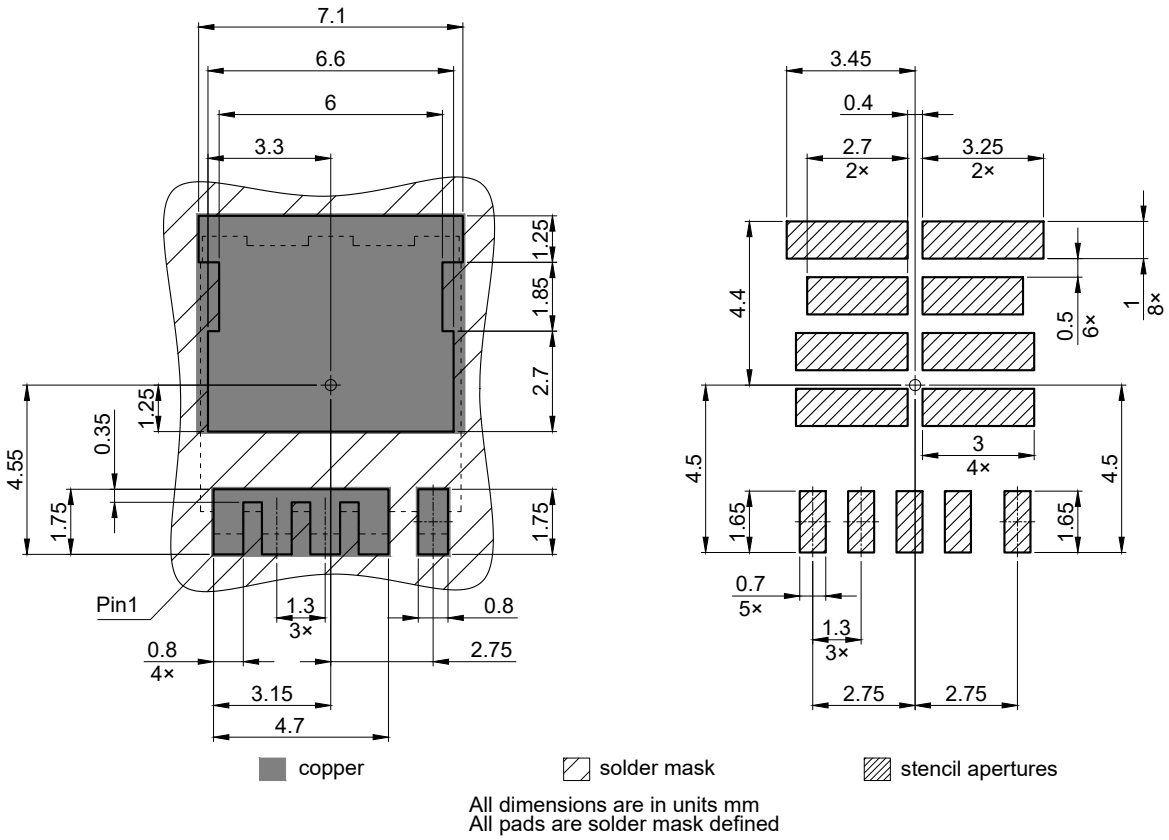


Figure 2 Footprint drawing PG-HSOF-5, dimensions in mm

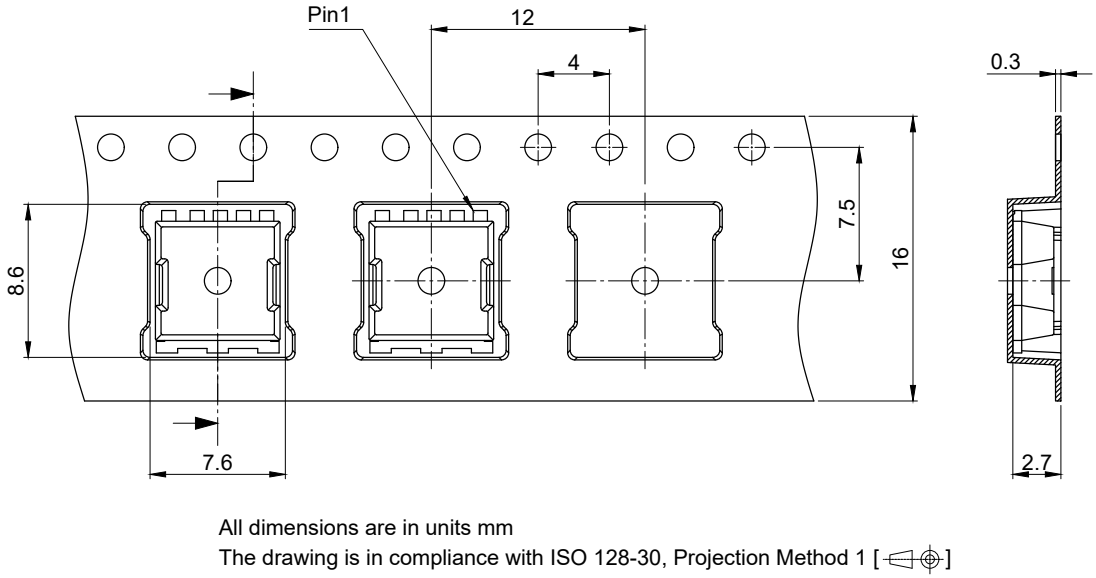


Figure 3 Packaging variant PG-HSOF-5, dimensions in mm

Revision history

IAUAN04S7S009

Revision 2026-09-23, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-09-23	Final Datasheet

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