

英飞凌 TRAVEO™ T2G 32 位车规级 MCU

基于 Arm® Cortex®-M7 单核

描述

英飞凌 TRAVEO™ T2G 32 位车规级 MCU 是一款专为汽车应用设计的高性能、低功耗控制器，符合功能安全标准 ISO 26262 和网络安全标准 ISO 21434。CYT3DL 是一款 TRAVEO™ T2G 微控制器系列，主要面向仪表盘和抬头显示器（HUD）等汽车系统。CYT3DL 配备 2D 图形引擎、音频处理功能，以及用于主处理的 Arm® Cortex®-M7 CPU，以及用于外设和安全处理的 Arm® Cortex®-M0+ CPU。这些器件内置了支持灵活数据速率控制器局域网（CAN FD）、本地互连网络（LIN）、时钟扩展外设接口（CXPI）以及以太网的嵌入式外设。TRAVEO™ T2G 系列器件采用先进的 40 nm 工艺制造。CYT3DL 集成了英飞凌的低功耗闪存以及多种高性能模拟和数字外设，可构建安全的计算平台。

特性

• 图形子系统

- 支持 2D 和 2.5D（透视扭曲、3D 效果）图形渲染
- 内部色彩分辨率
 - 40 位 RGBA（4 × 10 位）
 - 24 位 RGB（3 × 8 位）
- 2048 KB 嵌入式视频 RAM 内存 (VRAM)
- 两个视频输出接口，支持以下显示输出：
 - 并行 RGB（最大显示尺寸：800 × 600，40 MHz）
 - FPD-link 单通道（最大显示尺寸：1920 × 720，110 MHz）
- 一个采集引擎，用于 ITU 656 或并行 RGB/YUV 或 MIPI CSI-2 输入的视频输入处理
 - ITU656（标准摄像头采集：最高 800 × 480），与 RGB 接口复用
 - RGB（最大采集尺寸 1600 × 600，80 MHz）或
 - 双通道/四通道 MIPI CSI-2 接口（最大采集尺寸：双通道，110 MHz 时为 1920 × 720；四通道，220 MHz 时为 2880 × 1080）
- HUD 应用的实时显示变形处理
- 从采集到显示接口的直接传输，支持图形叠加
- 用于通过显示层进行场景合成的合成引擎
- 用于视频时序生成和显示功能的显示引擎
- 用于加速矢量图形渲染的绘图引擎
- 用于设置和控制渲染过程的指令序列器
- 支持无帧缓冲（即时）图形渲染
- 单通道 FPD-Link/LVDS 接口，最高可输出高清分辨率视频

• 声音子系统

- 四个时分复用（TDM）接口
- 两种脉冲编码调制-脉冲宽度调制（PCM - PWM）接口
- 最多五个声音发生器（SG）接口
- 两个具有五个输入流的 PCM 音频流混频器
- 一个音频数模转换器 (DAC)

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

特性

• CPU 子系统

- 240 MHz（最大）32 位 Arm® Cortex®-M7 CPU，带有
 - 单周期乘法
 - 单/双精度浮点运算单元（FPU）
 - 16 KB 数据缓存、16 KB 指令缓存
 - 存储器保护单元（MPU）
 - 64 KB 指令和 64 KB 数据紧耦合存储器 (TCM)
- 100 MHz 32 位 Arm® Cortex®-M0+ CPU，带有
 - 单周期乘法
 - 存储器保护单元
- 处理器间硬件通信
- 四个 DMA 控制器
 - 外设 DMA 控制器 #0 (P-DMA0) 带有 76 个通道
 - 外设 DMA 控制器 #1 (P-DMA1) 带有 84 个通道
 - 内存 DMA (AHB) 控制器 (M-DMA0) 带 8 个通道
 - 内存 DMA (AXI) 控制器 (M-DMA1) 带 4 个通道

• 集成存储器

- 4160 KB 代码闪存，另加 128 KB 工作闪存
 - 边读边写 (RWW) 允许在执行代码时对代码闪存/工作闪存进行更新
 - 单组和双组模式（专门用于无线固件更新 [FOTA]）
 - 通过 SWD/JTAG 接口对闪存进行编程
- 384 KB SRAM，具有可选保留粒度

• 符合 ISO 21434 标准/[EVITA Full^{1\)}](#)

- 支持增强安全硬件扩展（eSHE）和硬件安全模块（HSM）
- 安全启动和身份验证
 - 使用数字签名验证¹⁾
 - 使用快速安全启动
- AES：128 位块，128/192/256 位密钥
- 3DES¹⁾：64 位块，64 位密钥
- 向量单元¹⁾支持非对称密钥加密算法（如 Rivest-Shamir-Adleman (RSA) 和 Elliptic curve (ECC)）
- SHA-1/2/3[1]：SHA-512、SHA-256、SHA-160，可变长度输入数据
- CRC¹⁾：支持 CCITT CRC16 和 IEEE-802.3 CRC32
- 真随机数生成器（TRNG）和伪随机数生成器（PRNG）
- 伽罗瓦/计数器模式（GCM）

• 符合 ISO 26262 功能安全标准，达到 ASIL-B 等级

- 存储器保护单元（MPU）
- 共享存储器保护单元（SMPU）
- 外设保护单元（PPU）
- 看门狗计时器（WDT）
- 多计数器看门狗定时器（MCWDT）
- 低电压检测器（LVD）
- 电压欠压检测（BOD）

¹⁾ 加密引擎功能仅在部分 MPN 上提供。

特性

- 过压检测 (OVD)
- 过流检测 (OCD)
- 时钟监视器 (CSV)
 - 支持除休眠模式外的所有电源模式
- 硬件纠错 (SECCDED ECC) 在所有安全关键存储器 (SRAM, Flash, TCM)
- **低功耗 2.7 V 至 5.5 V 工作电压**
 - 低功耗运行、睡眠、低功耗睡眠、深度睡眠和休眠模式，可实现精细的电源管理
 - 可配置选项以实现稳健的电压欠压检测 (BOD)
 - 两个阈值电平 (2.7 V 和 3.0 V) 用于 BOD 在 V_{DD} 和 V_{DDA_ADC}
 - 一个阈值电平 (1.1 V) 用于 BOD 在 V_{CCD}
- **唤醒支持**
 - 最多四个引脚可唤醒休眠模式
 - 最多 61 个 GPIO 引脚可唤醒深度睡眠模式
 - 事件发生器、SCB、看门狗计时器、RTC 警报可从深度睡眠模式中唤醒
- **时钟**
 - 内部主振荡器 (IMO)
 - 内部低速振荡器 (ILO)
 - 外部晶体振荡器 (ECO)
 - 时钟晶体振荡器 (WCO)
 - 锁相环 (PLL)
 - 锁频环 (FLL)
 - 低功耗外部晶体振荡器 (LPECO)
- **通信接口**
 - 最多四个 CAN FD 通道
 - 与传统 CAN 相比，数据速率有所提高 (高达 8 Mbps)，但受物理层拓扑和收发器的限制
 - 符合 ISO 11898-1:2015 标准
 - 支持 Bosch CAN FD 规格 V1.0 对非 ISO CAN FD 的所有要求
 - ISO 16845:2015 证书可用
 - 最多 12 个运行时可配置的串行通讯功能块 (SCB) 通道，每个功能块可配置为 I2C, SPI, 或 UART
 - 最多两个独立 LIN 通道
 - LIN 协议符合 ISO 17987 标准
 - 多达两个 CXPI 通道，数据传输速率高达 20 kbps
 - 符合 IEEE-802.3bw 的 10/100 Mbps 以太网 MAC 接口
 - 支持以下 PHY 接口：
 - 介质独立接口 (MII)
 - 精简媒体独立接口 (RMII)
 - 符合 IEEE-802.1BA 音频视频桥接 (AVB)
 - 符合 IEEE-1588 精确时间协议 (PTP)
- **串行存储器接口 (SMIF)**
 - 两个 SPI (单线、双线、四线或八线)、xSPI 接口
 - 即时加密和解密
 - 从外部存储器就地执行 (XIP)

特性

• 定时器

- 最多 50 个 16 位和 32 个 32 位定时器/计数器脉冲宽度调制器 (TCPWM) 模块，用于常规操作
 - 最多 12 个 16 位计数器，针对电机控制操作进行了优化（相当于六个具有 ZPD 和斜率控制功能的步进电机控制 [SMC] 通道）
 - 支持定时器、捕获、正交解码、脉冲宽度调制 (PWM)、带死区时间的 PWM (PWM_DT)、伪随机 PWM (PWM_PR) 和移位寄存器 (SR) 模式
- 最多 16 个事件生成 (EVTGEN) 定时器，支持从深度睡眠模式循环唤醒
 - 事件触发特定的设备操作（例如执行中断处理程序、SAR ADC 转换等）

• 实时时钟 (RTC)

- 年/月/日、星期、小时：分钟：秒字段
- 12 小时和 24 小时格式
- 自动闰年校正

• I/O

- 最多 135 个可编程 I/O
- 四个 I/O 类型
 - GPIO 标准 (GPIO_STD)
 - GPIO 增强 (GPIO_ENH)
 - 通用 I/O 步进电机控制 (GPIO_SMC)
 - 高速 I/O 标准低噪声 (HSIO_STDLN)

• 功率

- 稳压器
 - 从 2.7 V 至 5.5 V 输入电源生成标称 1.1 V 内核电源
 - 两个稳压器：深度睡眠和核芯内部
- PMIC 控制模块

• 可编程的模拟资源

- 一个 SAR 模数转换器
 - 每个 ADC 支持 32 个逻辑通道，有 48 个外部通道，任何外部通道都可以连接到 SAR 中的任何逻辑通道
 - 12 位分辨率和高达 1 Msps 的采样率
- 每个 ADC 还支持六个内部模拟输入，如：
 - 带隙基准电压源用于提供绝对电压值
 - 用于结温计算的校准二极管
 - 两个 AMUXBUS 输入和两个用于监测电源电平的直接连接
- ADC 支持外部多路复用器的寻址
- ADC 有一个序列器，支持对已配置通道进行自主扫描

• 智能 I/O

- 一个智能 I/O 模块，可对进出 I/O 的信号执行布尔运算
- 支持最多 8 个 I/O (GPIO_STD)

• 调试接口

- 符合 IEEE-1149.1-2001 的 JTAG 控制器和接口

特性

- Arm® SWD（串行线调试）端口
- 支持 Arm® 嵌入式跟踪宏单元（ETM）跟踪
 - 使用 SWD 进行数据跟踪
 - 使用 JTAG 进行指令和数据跟踪
- 与行业标准工具兼容
 - GHS MULTI 或 IAR EWARM 用于代码开发和调试
- 封装
 - 272-BGA, 16 × 16 × 1.7 mm（最大），0.8 mm 球距
 - 216-TEQFP, 24 × 24 × 1.6 mm（最大），0.4 mm 球距

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1 特性列表
1 特性列表
表 1 CYT3DL 特性列表

Features	Packages	
	216-TEQFP	272-BGA
CPU		
Core	32-bit Arm® Cortex®-M7 CPU and 32-bit Arm® Cortex®-M0+ CPU	
Functional safety	ISO 26262 ASIL-B compliant	
Operation voltage for GPIO_STD	2.7 V to 5.5 V	
Operation voltage for GPIO_ENH	2.7 V to 5.5 V	
Operation voltage for GPIO_SMC	2.7 V to 5.5 V	
Operation voltage for HSIO_STDLN	3.0 V to 3.6 V	
Core voltage VCCD	1.09 V to 1.21 V	
Operation frequency	Arm® Cortex®-M7 240 MHz (max) and Arm® Cortex®-M0+ 100 MHz (max)	
MPU, PPU	Supported	
FPU	Supports both single (32-bit) and double (64-bit) precision	
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M7 CPU	
TCM	64-KB instruction and 64-KB data for Cortex®-M7 CPU	
Memory		
Code flash	4160 KB (4032 KB + 128 KB)	
Work flash	128 KB (96 KB + 32 KB)	
SRAM (configurable for retention)	384 KB	
ROM	64 KB	
Communication interfaces		
CAN0 (CAN FD: Up to 8 Mbps)	2 ch	
CAN1 (CAN FD: Up to 8 Mbps)	2 ch	
CAN RAM	16 KB per instance (2 ch), 32 KB in total	
Serial communication block (SCB/UART)	9 ch	12 ch
Serial communication block (SCB/I2C)	9 ch	11 ch
Serial communication block (SCB/SPI)	8 ch	11 ch
LIN0	2 ch	
CXPI controller	2 ch	
Ethernet MAC	1 ch × 10/100	
Memory interfaces		
SMIF (Single SPI / Dual SPI / Quad SPI / Octal SPI / xSPI)	2 ch (HSIO_STDLN at 133 MHz)	

(表格续下页...)

1 特性列表
表 1 (续) CYT3DL 特性列表

Features	Packages	
	216-TEQFP	272-BGA
Timers		
RTC	1 ch	
TCPWM (16-bit)	38 ch	
TCPWM (16-bit) SMC	12 ch (Equivalent to 6 ch SMC with ZPD and slew rate control)	
TCPWM (32-bit)	32 ch	
External interrupts	108	135
Analog		
12-bit, 1 Msps SAR ADC	1 Unit (SAR#0, 32 logical channels)	
	48 external channels	
	6 ch for Internal sampling	
Security – ISO 21434 compliant		
Flash security (program/work read protection)	Supported	
Flash Chip erase enable	Configurable	
eSHE / HSM	By separate firmware ¹⁾	
Sound		
Mixer	2 ch (5 mixer sources)	
PCM-PWM	2 ch	
TDM/I2S	4 TDM structures (each support 32 channels)	
TDM/RX	3 ch	4 ch
TDM/TX	2 ch	4 ch
Audio DAC	1 ch	
Sound generator (SG)	5 ch	
Graphics		
2/2.5 D Engine	Supported	
Embedded Video RAM	2048 KB (with protection)	
Vector Drawing	Supported	
Warping	Supported (on the fly)	
Scale/Rotate/Blend	Supported (on the fly)	
Graphics Engine Clock	200 MHz (max)	
Timing Control	One output	
Video Capture	One Capture (1× RGB or 1× MIPI CSI-2, up to 4 lanes)	One Capture(1× RGB or 1× MIPI CSI-2, up to 4 lanes)
Video Capture Formats	TTL: ITU656 (8-/10-bit, RGB/YUV interlaced or progressive)	

(表格续下页...)

1 特性列表

表 1 (续) **CYT3DL 特性列表**

Features	Packages	
	216-TEQFP	272-BGA
	–	TTL: Parallel RGB (1 to 24 bpp), YUV444, YUV422
	MIPI CSI-2: Table 79	
Number of Displays	Up to two (1× LVDS single and/or 1× RGB)	
RGB888/TTL Output	1 ch at 40 MHz (max)	
FPD-link/LVDS Output	Single channel LVDS at 80 MHz pixel clock (max)	Single channel LVDS at 110 MHz pixel clock (max)
MIPI CSI-2 Input	4 or 2 lane MIPI CSI-2 at 80 MHz pixel clock (max)	4 or 2 lane MIPI CSI-2 at 110 MHz pixel clock (max)
System		
DMA Controller	P-DMA0 with 76 channels (32 general purpose), P-DMA1 with 84 channels (16 general purpose), M-DMA0 with 8 channels, and AXI M-DMA1 with 4 channels	
Internal Main Oscillator	8 MHz	
Internal Low speed Oscillator	32.768 kHz (nominal)	
PLL	Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 240 MHz	
FLL	Input frequency: 0.25 to 100 MHz, FLL output frequency: up to 100 MHz	
Watchdog timer and multi-counter watchdog timer	Supported (WDT + 2× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM7_0	
Clock supervisor	Supported	
Cyclic wakeup from DeepSleep	Supported	
GPIO standard (GPIO_STD)	20	29
GPIO enhanced (GPIO_ENH)	8	
GPIO SMC (GPIO_SMC) ²⁾	24	
HSIO Standard Low Noise (HSIO_STDLN)	55	74
Smart I/O (Blocks)	1 block, mapped through 8 I/Os	
Low-voltage detect	Two, 26 selectable levels	
Maximum ambient temperature	105°C for S-grade, 125°C for E-grade	
Debug interface	SWD/JTAG	
Debug Trace	Arm® Cortex®-M7 ETB size of 8 KB, Arm® Cortex®-M0+ MTB size of 4 KB	

1) 增强安全硬件扩展 (eSHE) 和硬件安全模块 (HSM) 支持由第三方固件实现。

2) 高电流 SMC I/O, 用于直接连接指针式仪器的步进电机线圈。

1 特性列表

1.1 外设实例列表

下表列出了通讯外设在每个封装下支持的实例，根据实现功能所需的最少和完整引脚数。

表 2 最小外设实例列表

Module	216-TEQFP	272-BGA	Minimum pin functions
CAN0	0-1	0-1	TX, RX
CAN1	0-1	0-1	TX, RX
LIN0	0-1	0-1	TX, RX
CXPI	0-1	0-1	TX, RX
SCB/UART	0-4, 8-11	0-11	TX, RX
SCB/I2C	1-4, 7-11	1-11	SCL, SDA
SCB/SPI	1-4, 8-11	1-11	MISO, MOSI, SCK, SELECT0
TDM/RX	0-2	0-3	MCK, FSYNC, SCK, SD
TDM/TX	2-3	0-3	MCK, FSYNC, SCK, SD
SG	0-4	0-4	TONE, AMPL
ETHERNET	0	0	RMII
SMIF	0-1	0-1	DATA, CLK, RWDS, SELECT0-1
PWM	0-1	0-1	LINE1_P/N, LINE2_P/N
TCPWM (32-bit)	0-31	0-31	PWM, PWM_N
TCPWM (16-bit) ¹⁾	32-35, 256-267, 520-533, 536-543	32-37, 256-267, 512-543	PWM, PWM_N

1) 通道 522-524 的引脚功能复用至同一引脚。

表 3 完整外设实例列表

Module	216-TEQFP	272-BGA	Full pin functions
CAN0	0-1	0-1	TX, RX
CAN1	0-1	0-1	TX, RX
LIN0	0-1	0-1	TX, RX, EN
CXPI	0-1	0-1	TX, RX, EN
SCB/UART	0-4, 8-11	0-11	TX, RX, RTS, CTS
SCB/I2C	1-4, 7-11	1-11	SCL, SDA
SCB/SPI	1-4, 8	1-11	MISO, MOSI, SCK, SELECT0-1
TDM/RX	0-2	0-3	MCK, FSYNC, SCK, SD
TDM/TX	2-3	0-3	MCK, FSYNC, SCK, SD
SG	4	0-4	TONE, AMPL, MCK
ETHERNET	–	0	MII

(表格续下页.....)



1 特性列表

表 3 (续) 完整外设实例列表

Module	216-TEQFP	272-BGA	Full pin functions
SMIF	0-1	0-1	DATA, CLK, RWDS, SELECT0-1
PWM	0-1	0-1	LINE1_P/N, LINE2_P/N, MCK
TCPWM (32-bit)	0-31	0-31	PWM, PWM_N, TC_TR
TCPWM (16-bit) ¹⁾	32-33, 36-37, 518-519, 522-541	32-37, 512-543	PWM, PWM_N, TC_TR

1) 通道 522-524 的引脚功能复用至同一引脚。

2 模块和功能

2 模块和功能

框图

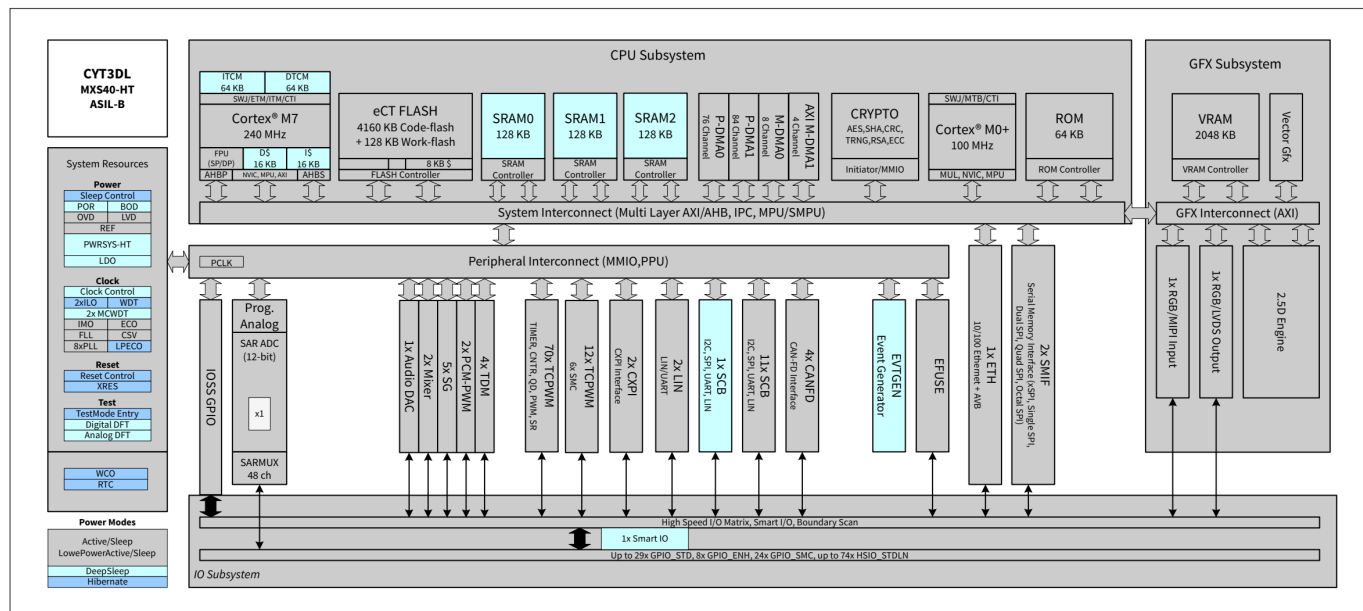


图 1 架构框图

图 1 简要展示了各子系统与模块之间的相互连接。CYT3DL 拥有五个主要子系统：CPU、系统资源、外设、图形和 I/O^{[2], [3], [4], [5]}。颜色标记表示该模块在仍能正常工作时的最低功耗模式。

CYT3DL 广泛支持硬件和固件的编程、测试、调试和跟踪。

片上调试功能支持使用生产器件进行系统调试。它不需要特殊的接口、调试转接板、模拟器或仿真器。

JTAG 接口与 I-jet、J-Link 和 GHS 等行业标准的第三方探测器完全兼容。调试电路默认启用。

CYT3DL 提供高级的安全性，具有强大的闪存保护以及调试等禁用功能。

此外，如果某些应用担心网络钓鱼攻击会通过器件恶意重新编程或试图启动和中断闪存编程序列来击败安全设定，所有器件接口都可以被永久禁用。当器件的最大安全级别被使能时，将禁用所有编程、调试和测试接口。

² GPIO STD 支持 2.7 V 至 5.5 V VDDIO GPIO 范围。

³ GPIO_ENH支持2.7V至5.5V VDDIO_GPIO范围, 在较低电压下具有较高的电流。

⁴ GPIO_SMC 支持 2.7V 至 5.5V VDDIO_SMC 范围, 电流高于 GPIO_ENH。

⁵ HSIO_STPLN 支持 3.0V 至 3.6V VDDIO_HSIO 范围，支持高速信号和可编程驱动强度。

3 功能描述

3 功能描述

3.1 CPU 子系统

3.1.1 CPU

CYT3DL CPU 子系统包含一个 32 位 Arm®Cortex®-M0+ CPU 带有 MPU，以及一个 32 位 Arm®Cortex®-M7 CPU，带有 MPU、单/双精度 FPU 以及 16 KB 数据和指令缓存。该子系统还包括 P-/M-DMA 控制器、加密加速器、4160 KB 代码闪存、128 KB 工作闪存、384 KB SRAM 和 64 KB ROM。

Cortex®-M0+ CPU 提供了安全、不可中断的启动功能。这保证了启动功能完成后，系统完整性有效且权限得到强制执行。共享资源（闪存、SRAM、外设等）可以通过总线仲裁进行访问，并且使用硬件信号量的处理器间通讯（IPC）机制来支持独占访问。

每个 Cortex®-M7 CPU 具有 64 KB 指令和 64 KB 数据 TCM，并带有可编程读取等待状态。每个 TCM 时钟均由相关的 Cortex®-M7 CPU 时钟提供。

3.1.2 DMA 控制器

CYT3DL 有四个 DMA 控制器：具有 32 个通用通道和 44 个专用通道的 P-DMA0、具有 16 个通用通道和 68 个专用通道的 P-DMA1、具有 8 个通道的 M-DMA0，以及具有四个通道的 AXI M-DMA1。P-DMA 用于外设到存储器和存储器到外设的数据传输，并为大量通道提供低延迟。每个 P-DMA 控制器使用单个数据传输引擎，并由相关通道共享。通用通道具有丰富的互连矩阵，包括 P-DMA 交叉触发，可满足苛刻的数据传输场景的要求。专用通道具有单个触发输入（例如 ADC 通道）来处理常见的传输需求。M-DMA 用于存储器到存储器的数据传输，并为少量通道提供高内存带宽。M-DMA 为每个通道使用专用的数据传输引擎。它们支持使用 AHB 多层总线去独立访问外设。AXI M-DMA 用于提供对 AXI 从设备（如 VRAM）的访问。

3.1.3 闪存

CYT3DL 具有 4160 KB（4032 KB 的扇区大小为 32 KB，128 KB 的扇区大小为 8 KB）的代码闪存，以及额外 128 KB（96 KB 的扇区大小为 2 KB，32 KB 的扇区大小为 128 B）的工作闪存。工作闪存经过了优化，可以比代码闪存进行更多次重新编程。代码闪存支持边读边写（RWW）操作，以便在 CPU 工作模式时更新闪存。代码闪存和工作闪存区域均支持远程升级（OTA）编程的双区操作。

3.1.4 SRAM

CYT3DL 具有 384 KB 的 SRAM 和两个独立的控制器。SRAM0 以 32 KB 的增量提供在深度睡眠模式保留，而 SRAM1/2 可在完全保留或不保留之间选择。

3.1.5 ROM

CYT3DL 具有 64 KB 的 ROM，其中包含启动和配置例程。该 ROM 可实现安全启动和用户的闪存验证，以保证系统的安全。

3 功能描述

3.1.6 安全加密加速器

密码加速器实现 (3) DES 分组密码、AES 分组密码、SHA 散列、循环冗余校验、伪随机数生成、真随机数生成、伽罗瓦/计数器模式和向量单元以支持 RSA 和 ECC 等非对称密钥密码。

根据部件编号的不同，此功能块可能完全可用、部分可用或完全不可用。详情参见[订购信息](#)。

3.2 系统资源

3.2.1 电源系统

电源系统确保电源电压水平满足每种电源模式的要求，并在这些水平无效时提供全系统复位。内部上电复位 (POR) 保证初始电源上升期间的全芯片复位。

三个 BOD 电路用于监控外部电源电压 (V_{DD} , V_{DDA_ADC} , V_{CCD})。 V_{DD} 和 V_{CCD} 上的 BOD 初始状态为使能，无法禁用。 V_{DDA_ADC} 上的 BOD 初始状态为禁用，用户可以启用。对于外部电源 V_{DD} 和 V_{DDA_ADC} ，BOD 电路可通过软件配置两种设置：2.7 V 最小电压，对所有内部信号具有稳健性；以及 3.0 V 最小电压，对所有 I/O 规格同样具有稳健性（保证电压为 2.7 V）。 V_{CCD} 上的 BOD 是一种安全措施，并非可靠的检测器。

提供三个过压检测 (OVD) 电路用于监控外部电源 (V_{DD} 、 V_{DDA_ADC} 、 V_{CCD})，以及过流检测电路 (OCD) 用于监控内部和外部稳压器。 V_{DD} 和 V_{DDA_ADC} 上的 OVD 阈值可配置为两种设置：5.0 V 和 5.5 V 最大电压。

提供了两个电压检测电路来监控外部电源电压 (V_{DD}) 的下降和上升电平，每个电路均可配置为 26 个可选电平之一。

V_{DD} 和 V_{CCD} 上的所有 BOD、OVD 和 OCD 电路都会产生复位，因为它们用于保护 CPU 和故障逻辑。 V_{DDA_ADC} 上的 BOD 和 OVD 电路可以配置为产生复位或故障。

3.2.2 稳压器

CYT3DL 包含两个稳压器，为低压核晶体管提供电源：深度睡眠和核内稳压器。这些稳压器接受 2.7 V 至 5.5 V V_{DD} 供电，并为器件的各个部分提供低噪声的 1.1 V 供电。这些稳压器在切换电源模式时由硬件和固件自动启用和禁用。核内稳压器在工作模式下工作，为 CPU 子系统及相关外设供电。

3.2.2.1 深度睡眠

深度睡眠稳压器用于在深度睡眠模式下维持供电给少数模块。这些模块包括 ILO 和 WDT 定时器、BOD 检测器、SCB0、SRAM 存储器、智能 I/O 和其他配置存储器。深度睡眠稳压器在深度睡眠模式下启用，此时核内稳压器被禁用。当 XRES_L 有效（低电平）并且核内稳压器被禁用时，它被禁用。

3.2.2.2 核心内部

核内稳压器支持高达 300 mA 的负载电流，并且在器件启动（启动过程）期间以及在工作/睡眠模式下运行。（不支持图形子系统）

3 功能描述

3.2.3 PMIC 控制模块

内部 PMIC 模块可用于控制外部 PMIC。PMIC 控制模块管理仅用于启动的内部有源稳压器与外部 PMIC 之间的切换。

核内部稳压器和核外部 PMIC 都需要外部大容量存储电容并连接到 V_{CCD} 引脚。该电容在低压核晶体管的动态负载下提供充电。

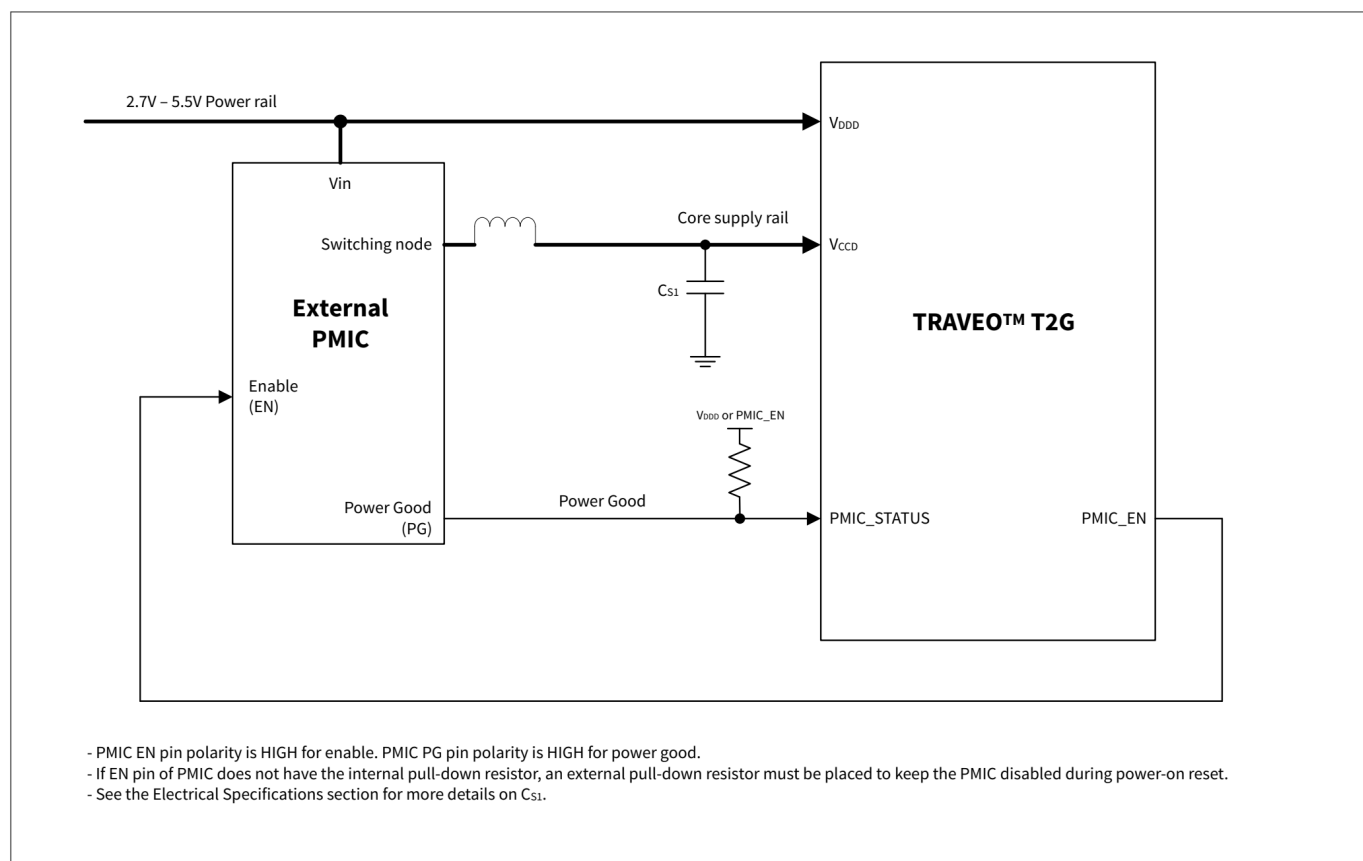


图 2 PMIC 控制接口示例

3.2.4 时钟系统

CYT3DL 时钟系统为所有需要时钟的子系统提供时钟，并在不同时钟源之间实现无缝切换。此外，它还确保不发生亚稳态。

CYT3DL 的时钟系统由 8 MHz IMO、两个 ILO、四个看门狗定时器、八个 PLL、一个 FLL、五个时钟监视器 (CSV)、一个 7.2 至 33.34 MHz ECO、一个 3.99 至 8.01 MHz LPECO 和一个 32.768 kHz WCO 组成。

时钟系统支持三个主时钟域：CLK_HF、CLK_SLOW、CLK_LF。

- CLK_HF_x 是工作模式时钟。每个都可以使用任何高频时钟源，包括 IMO、EXT_CLK、ECO、LPECO、FLL 或 PLL。
- CLK_SLOW 为 Cortex®-CM0+ CPU、Crypto、P-/M-DMA 和 CPU 子系统的其他慢速基础模块提供基准时钟
- CLK_LF 是深度睡眠域时钟，为 MCWDT 或 RTC 模块提供基准时钟。CLK_LF 域的基准时钟可以禁用，也可以从 ILO0、ILO1 或 WCO 中选择。

3 功能描述

表 4 CLK_HF 目标

Name	Description
CLK_HF0	CPUSS (Memories, CLK_SLOW, Peripherals)
CLK_HF1	CPUSS (Cortex®-M7 CPU)
CLK_HF2	CAN FD, CXPI, LIN, SCB, SAR
CLK_HF3	Event generator, Clock output (CLK_EXT)
CLK_HF4	Ethernet Internal Clock
CLK_HF5	Sound Subsystem #0 (TDM, SG, PWM, MIXER, DAC), Ethernet TSU
CLK_HF6	Sound Subsystem #1 (TDM, SG, PWM, MIXER)
CLK_HF7	Sound Subsystem #2 (TDM, SG, PWM)
CLK_HF8	SMIF #0
CLK_HF9	SMIF #1
CLK_HF10	Video Subsystem
CLK_HF11	Video Display #0
CLK_HF12	Video Display #1

3.2.4.1 IMO 时钟源

IMO 是 CYT3DL 的频率基准，当没有外部基准可用或被使能时。IMO 的运行频率约为 8 MHz。

3.2.4.2 ILO 时钟源

ILO 是一种低功耗振荡器，标称频率为 32.768 kHz，在深度睡眠模式下为看门狗定时器产生时钟。有两个 ILO 可确保深度睡眠模式下的时钟监控器 (CSV) 功能。可以根据 IMO、WCO 或 ECO 来校准 ILO 驱动的计数器，以提高其精度。ILO1 也用于时钟监控。

3.2.4.3 PLL 和 FLL

可以使用 PLL（三个 200 MHz 和五个 400 MHz）或 FLL 来从 IMO、ECO 或 EXT_CLK 生成高速时钟。与锁相环相比，FLL 提供的锁定速度要快得多（5 μ s 而不是 35 μ s），但会引入少量（ $\pm 1\%$ ）频率误差⁶以及较低的最大输出频率（100 MHz，而不是高达 400 MHz）。400 MHz PLL 支持具有向下扩展的展频时钟生成（SSCG）。

3.2.4.4 时钟监控器

每个时钟监控器 (CSV) 允许一个时钟（基准）监控另一个时钟（被监控）的行为。每个 CSV 都有用于监控和参考时钟的计数器。每个计数器的参数决定基准时钟的频率以及受监控时钟的频率上限和下限。如果频率范围比较器检测到停止的时钟或指定频率范围之外的时钟，则会发出异常状态信号并产生复位或中断。

⁶ 由于频率误差，不建议使用基于 FLL 的参考源来操作参考定时外设（例如 UART）。

3 功能描述

3.2.4.5 EXT_CLK

三个 GPIO_STD I/O 中的一个可用于提供高达 100 MHz 的外部时钟输入。该时钟可以用作 PLL 或 FLL 的源时钟，也可以直接由 CLK_HF 域使用。

3.2.4.6 ECO

ECO 使用连接到 ECO_IN 和 ECO_OUT 引脚的外部晶体提供高频时钟。它支持基模（非泛音）石英晶体，范围为 7.2 至 33.34 MHz。与 PLL 结合使用时，它能生成 CPU 和外设所需的器件最大时钟。ECO 精度取决于所选的晶体。如果 ECO 被禁用，则相关引脚可用于任何可用的 I/O 功能。

3.2.4.7 LPECO

LPECO 使用连接到 LPECO_IN 和 LPECO_OUT 引脚的外部晶体提供高频时钟。它支持基模（非泛音）石英晶体，范围为 3.99 至 8.01 MHz。LPECO 可以在深度睡眠和休眠模式下运行，电流损耗显著降低。它还可用于实时时钟应用。与 PLL 结合使用时，它能生成 CPU 和外设所需的器件最大时钟。

3.2.4.8 WCO

WCO 是一款低功耗时钟晶振振荡器，适用于实时时钟应用。它需要一个外部 32.768-kHz 晶振连接到 WCO_IN 和 WCO_OUT 引脚。WCO 还可以配置为 CLK_LF 的时钟基准，CLK_LF 是 MCWDT 和 RTC 的时钟源。

3.2.5 复位

CYT3DL 可以从多种来源复位，包括软件。大多数复位事件是异步的，并能够确保器件恢复到已知状态。复位原因（POR、BOD、OVD、过流、XRES_L、WDT、MCWDT、软件复位、故障、CSV、休眠唤醒、调试）记录在一个寄存器中，该寄存器在复位时保持不变，并允许软件确定复位的原因。XRES_L 引脚可用于外部复位。

3.2.6 看门狗定时器

CYT3DL 具有一个看门狗定时器（WDT）和两个多计数器看门狗定时器（MCWDT）。

WDT 是一个自由运行的计数器，仅由 ILO0 提供时钟，因此可以将其用作休眠模式的唤醒源。在所有电源模式下都可以进行看门狗操作。为了防止因 WDT 超时而导致器件复位，必须在配置的窗口期间对 WDT 进行喂狗。看门狗复位被记录在复位原因寄存器中。

每个 CPU 核都有一个 MCWDT。这些定时器提供比 WDT 更多的功能，并且仅在运行、睡眠和深度睡眠模式下可用。这些计时器有多个计数器，可以单独使用或级联使用来触发中断和/或复位。它们由 ILO0 或 WCO 提供时钟。

3.2.7 功耗模式

CYT3DL 具有六种功耗模式，适用于核心功能、Cortex®-M0+ 内核以及不带电源开关的外设。Cortex®-M7 内核和 VIDEOSS 的电源模式则单独控制。

- 工作模式 – 所有外围设备均可用
- 低功耗工作（LPACTIVE） – 工作模式低功耗配置，其中所有外设和 CPU 均可用，但功能有限

3 功能描述

- 睡眠 – 除 CPU 外的所有外设均可用
- 低功耗睡眠 (LPSLEEP) – 睡眠模式的低功耗配置，其中除 CPU 外所有外设均可用，但功能有限
- 深度睡眠 – 仅可使用与 CLK_LF 配合使用的外设
- 休眠 – 器件和 I/O 状态被冻结，器件在唤醒时会复位

3.3 外设

3.3.1 外设时钟分频器

提供整数和小数时钟分频器用于外设和定时目的。

表 5 时钟分频器 - CPUSS 组 (0号)

Divider type	Instances	Description
div_8	9	Integer divider, 8 bits
div_16	16	Integer divider, 16 bits
div_16_5	7	Fractional divider, 16.5 bits (16 integer bits, 5 fractional bits)
div_24_5	3	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

表 6 时钟分频器 - CPUSS 组 (1 号)

Divider type	Instances	Description
div_8	3	Integer divider, 8 bits
div_16	4	Integer divider, 16 bits
div_24_5	7	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 外设保护单元

外设保护单元 (PPU) 控制和监视从所有主设备 (CPU、P-/M-DMA、加密和任何启用的调试接口) 到外设的未经授权的访问。它允许或限制总线基础设施上的数据传输。访问规则是根据传输的特定属性来强制执行的，例如传输的地址范围和访问属性 (例如读/写、用户/特殊权限和安全/非安全)。

3.3.3 12 位 SAR ADC

CYT3DL 包含一个 1-Msps SAR ADC。该 ADC 的时钟频率高达 26.67 MHz，可在 26 个时钟周期内提供 12 位结果。

SAR ADC 的参考信号来自一对专用输入：VREFH 和 VREFL ⁷。

CYT3DL 支持 32 个逻辑 ADC 通道，可从 54 个输入源中选择一个。信号源包括来自 I/O 的 48 个外部输入，以及用于诊断和监测的六个内部连接。

表 1 中列出了 ADC 通道数 (每个 ADC 和封装类型)。

⁷ VREF_L 可防止 VSSIO 和 VSSA_ADC 路径中的 IR 压降影响测量。当 VREF_L 正确连接时，可以降低或消除 VSSIO 和 VSSA_ADC 路径中的 IR 压降对测量的影响。

3 功能描述

SAR ADC 具有一个序列器，能够自主循环配置的通道（序列扫描），并且没有切换开销（也就是说，当时钟频率为 26.67 MHz 时，无论用于单个通道还是分布在多个通道上，总采样率都等于 1 Msps）。序列器切换通过状态机或固件控制。序列器对触发请求进行优先级排序，启用适当的模拟通道，控制 ADC 采样，启动 ADC 数据转换，管理结果，并启动后续的重复转换或组转换，而无需 CPU 干预。

SAR ADC 具有两个模拟多路复用器，用于将待测信号连接到 ADC。其中一个 SARMUX0，它有 24 个 GPIO_STD 输入（ADC[0]_0 至 ADC[0]_23），以及六个额外的输入，用于测量内部信号，例如带隙基准、温度传感器、 V_{CCD} 、 V_{DDA_ADC} 电源和 AMUXBUSA/B 信号。另一个多路复用器是 SARMUX1，它有 24 个 GPIO_SMC 输入（ADC[1]_0 至 ADC[1]_23）。

CYT3DL 有一个温度传感器。需要软件后处理将温度传感器读数转换为开尔文或摄氏度值。

为了适应各种源阻抗和频率的信号，每个通道可以编程不同的采样时间。ADC 还支持范围比较功能，无需等待定序器扫描完成，也无需等待 CPU 固件评估测量值是否超出量程，即可快速检测出超出范围的数值。

ADC 不能用于深度睡眠和休眠模式，因为 ADC 需要高速时钟（而这些模式下高速时钟不可用）。ADC 输入基准电压 (V_{REFH}) 范围为 2.7 V 至 V_{DDA_ADC} ， V_{REFL} 为 V_{SSA_ADC0} 。

3.3.4 定时器/计数器/脉宽调制器模块 (TCPWM)

TCPWM 功能块由 16 位（50 个通道）和 32 位（32 个通道）计数器组成，具有用户可编程周期。

每个 TCPWM 计数器包含一个捕获寄存器，用于记录发生事件时的计数值；一个周期寄存器（用于在计数值等于周期寄存器值时停止或自动重新加载计数器）；以及比较寄存器，用于生成作为 PWM 占空比输出的信号。

TCPWM 模块内的每个计数器都支持多种功能模式，例如定时器、捕获、正交、PWM、带死区插入的 PWM（PWM_DT，8 位）、伪随机 PWM（PWM_PR）和移位寄存器。

TCPWM 模块还提供了正向输出和互补输出，它们之间偏移可编程控制，以允许它们用作死区互补 PWM 输出。TCPWM 模块还具有 Kill 输入（仅适用于 PWM 模式）用于强制输出进入预定状态；例如，在马达驱动系统中，当出现过流状态时，需要立即使用它来关闭驱动 FET 的 PWM（没有时间用于软件干预）。

十二个 16 位计数器针对 DC 和步进电机控制操作进行了优化，还具有 ZPD（零点检测）和斜率控制功能。这两个 TCPWM 通道构成一个 SMC 通道。

3.3.5 串行通信模块 (SCB)

CYT3DL 包含最多 12 个串行通信模块，每个模块可配置为 I²C、UART 或 SPI。

3.3.5.1 I²C 接口

SCB 可配置为实现完整的 I²C 主设备（支持多主仲裁）或从设备接口。每个配置为 I²C 的 SCB 最高工作速率可达 1 Mbps（快速模式 Plus），并提供灵活的缓冲选项，以减少 CPU 的中断开销和延迟。此外，每个 SCB 均支持对收发数据进行 FIFO 缓冲，通过延长 CPU 读取数据的时间，从而减少对时钟拉伸的需求。该 I²C 接口与 NXP I²C 总线规格及用户手册（UM10204）中规定的标准模式、快速模式和快速模式 Plus 设备兼容。

I²C 总线 I/O 通过处于开漏模式的 GPIO 实现⁸⁾，⁹⁾。

3 功能描述

3.3.5.2 UART 接口

当配置为 UART，每个 SCB 提供全功能 UART，其最大速率由配置的外设时钟频率和过采样率确定。它支持红外接口 (IrDA) 和智能卡 (ISO 7816) 协议，这些协议是 UART 协议的小变种。此外，它还支持 9 位多处理器模式，此模式允许寻址连接到通用 RX 和 TX 线的外设。

支持通用 UART 功能，如奇偶校验、停止位的数量、断帧检测和帧错误。发送和接收数据的 FIFO 缓冲允许容忍更大的 CPU 服务延迟。

LIN 协议由 UART 支持。LIN 基于单主多从拓扑结构。LIN 总线上有一个主节点和多个从机节点。SCB UART 仅支持 LIN 从机功能。

与专用 LIN 模块相比，以 SCB/UART 用作 LIN 需要更高水平的软件交互和增加 CPU 负载。

3.3.5.3 SPI 接口

SPI 配置支持完整的 Motorola SPI、TI 同步串行协议 (SSP，本质上是添加启动脉冲用于同步基于 SPI 的编解码) 和 National Microwire (SPI 的半双工形式)。SPI 接口可以使用 FIFO。SPI 接口以高达 12.5 MHz 的 SPI 时钟运行。SCB 还支持 EZSPI 10) 模式。

SCB0 支持以下附加特性：

- 在深度睡眠模式下可作为从机操作
- I2C 从机 EZ (EZI2C ¹¹⁾) 模式，最多可容纳 256 B 数据缓冲，无需 CPU 干预即可实现多字节通讯
- I2C 从机外部时钟操作
- 具有 512 B 数据缓冲区的命令/响应模式，可进行多字节通信，无需 CPU 干预

3.3.6 控制器区域网络灵活数据速率 (CAN FD)

CYT3DL 包含两个 CAN FD 控制器模块，每个模块支持两个 CAN FD 通道。所有 CAN FD 控制器均符合 ISO 11898-1:2015 标准；可提供 ISO 16845:2015 证书。它还在硬件中完全实现了 ISO 11898-4 (TTCAN 协议级别 1 和 2) 中指定的时间触发 CAN (TTCAN) 协议。所有与信息处理有关的功能均由 Rx 和 Tx 处理程序实现。Rx 处理程序管理消息接受过滤、将接收到的消息从 CAN 核心传输到消息 RAM，并提供接收消息状态。Tx 处理程序负责将发送消息从消息 RAM 传输到 CAN 核心，并提供发送消息状态。

3.3.7 本地互连网络 (LIN)

CYT3DL 含有多达两个 LIN 通道。每个功能块都支持按照 ISO 标准 17987 的 LIN 协议传输/接收数据。每个 LIN 功能块通过 3 引脚接口 (包括使能功能) 连接到外部收发器，并支持主机和从机功能。每个功能块还支持经典和增强的检验和，以及消息接收和唤醒信令期间的断帧检测。断帧检测、同步场、校验和计算以及错误中断均由硬件处理。

⁸ 这不 100% 符合 I2C 总线规格；I/O 不耐受过压，不支持快速模式 Plus 的 20 mA 灌电流要求，并且在未施加电源时违反漏电流规格。

⁹ 参见表 39 "串行通信模块 (SCB) 规格"，了解支持的 I/O 单元和 I2C 模式。

¹⁰ Easy SPI (EZSPI) 协议基于摩托罗拉 SPI 协议可在任何模式 (0、1、2 或 3) 下运行。它允许主机和从机之间进行通信，同时减少 CPU 干预的需要。

¹¹ Easy I2C (EZI2C) 协议是英飞凌在 I2C 协议基础上开发的一种独特通信方案。它使用围绕标准 I2C 协议的元协议，通过索引式内存传输与 I2C 从机进行通信。这减少了对 CPU 干预的需求。

3 功能描述

3.3.8 时钟扩展外设接口 (CXPI)

CYT3DL 包含多达四个符合 JASO D015 和 ISO 标准 20794 (包括控制器规格) 的 CXPI 通道。

每个通道支持：

- 主机和从机功能
- 针对正常帧和长帧的轮询和事件触发方法
- 非归零编码 (NRZ) 和 PWM 信号模式
- 碰撞解析以及载波监听多路访问机制
- 唤醒脉冲的生成和检测
- 正常帧和长帧的 CRC8 和 CRC16
- 错误检测
- 用于发送和接收的专用 FIFO (16 B)

3.3.9 以太网 MAC

CYT3DL 支持一个传输速率为 10 或 100 Mbps 的以太网通道。兼容 IEEE 802.3 标准。支持 IEEE 802AS 和 1588 精确时钟同步协议。支持 MII 和 RMII PHY 接口。支持使用外部 PHY 设备进行全双工数据传输。仅在 RMII 模式下使用外部 PHY 设备支持半双工数据传输。该设备还支持音频-视频桥接 (AVB)。MAC 支持标准 6 字节可编程地址。模块使用 AXI 接口进行 DMA 访问。

3.3.10 串行存储器接口 (SMIF)

除了内部闪存外，CYT3DL 还支持直接连接多达两个 512 MB 的外部快闪式存储器或 RAM 存储器。此连接通过 xSPI 或串行外设接口 (SPI) 建立。xSPI 允许连接 HYPERFLASH™ 和 HYPERRAM™ 设备，而 SPI (单、双、四或八进制 SPI) 可以连接串行闪存。通过该接口连接的内存中存储的代码允许就地执行 (XIP) 操作，该操作不需要先将指令复制到内部内存，并且对于需要安全外部数据和代码的环境可以进行即时加密和解密。

3.3.11 声音子系统

CYT3DL 支持以下功能，

- 最多四个时分复用 (TDM) 接口
 - 全双工发射器和接收器操作
 - 独立发送或接收操作，每个支持主模式或从模式
 - 最多 32 个通道，每个通道可单独启用或禁用
- 最多两个脉冲编码调制-脉冲宽度调制 (PCM - PWM) 接口
 - 将 PCM 音频流转换为 PWM 信号
 - 最高 32 位输出采样分辨率
 - 支持 E 桥和 H 桥格式
 - 死区时间插入
- 最多五个声音发生器 (SG) 接口
 - PWM 调制 (振幅、音调) 声音生成
 - 单独的音量和频率控制 (两个信号) 以及音量和频率组合控制 (一个信号) 格式

3 功能描述

- 最多五个混音器
 - 将多个 PCM 源流合并为一个 PCM 目标流
 - PCM 音源流可以进行增益/音量控制
 - 固定 PCM 采样格式（16 位成对）
 - 通过 FIR 滤波器支持 LPF
 - 对源 PCM 流和目标 PCM 流进行淡入淡出控制
- 一个音频数模转换器 (DAC)
 - 可编程采样率和频率控制
 - 支持立体声（左声道和右声道）
 - 支持 CIC 滤波器、FIR 滤波器、插值滤波器和 Delta-Sigma 调制器
 - 多级 DAC

3.3.12 一次性可编程（OTP）eFuse

CYT3DL 包含一个 1024 位 OTP eFuse 存储器，可用于存储和访问每个器件的唯一且不可更改的标识符或序列号。eFuse 还用于控制设备生命周期（制造、编程、正常运行、寿命终止等）和安全状态。在 1024 位中，有 192 位可供用户使用。

3.3.13 事件发生器

事件发生器支持在工作模式下产生中断和触发，以及在深度睡眠模式下产生中断。事件发生器用于触发特定的器件操作（执行中断处理程序、SAR ADC 转换等）并提供从深度睡眠模式的循环唤醒机制。它们为器件功能提供无需 CPU 的触发器，减少 CPU 在触发器件功能时的参与，从而降低总体功率消耗和处理开销。

3.3.14 触发多路复用器

CYT3DL 支持使用触发信号连接各种外设。触发器用于通知外设事件的发生或状态的改变。这些触发器用于影响或启动其他外设的某些操作。触发多路复用器用于将触发器从来源外设路由到目的地。

触发器提供主动的逻辑功能，并且通常在工作模式下支持。

3.4 图形

CYT3DL 支持一个图形子系统实例，其中包括 2048 KB 嵌入式视频 RAM、一个 2D 图形内核以及用于视频输入和输出处理的接口。

CYT3DL 支持 4 通道 MIPI CSI-2 接口，最高支持高清 (1920 × 720) 分辨率视频输入；支持单通道 FPD-link 接口，最高支持高清 (1920 × 720) 分辨率视频输出。2D 图形核心支持一个块图像传输 (BLIT) 引擎，用于更快的图形渲染至内存或实时显示；支持一个绘图引擎，用于加速矢量图形渲染；还支持一个命令序列器，用于设置和控制渲染过程。视频输入/输出支持一个用于将显示层合成为场景的合成引擎、一个用于视频时序生成和显示功能的显示引擎，以及一个用于视频输入处理的捕捉引擎。该设备还支持透视校正 3D 效果 ("2.5D")。其中一层，如抬头显示器，可进行实时变形处理。

3.5 I/Os

CYT3DL 具有多达 135 个可编程 I/O。

3 功能描述

I/O 被组织为称为端口的逻辑实体，其最大宽度为 8 位。在上电和复位期间，I/O 被强制进入 High-Z 状态。在休眠模式期间，I/O 被冻结。

每个 I/O 引脚都能生成一个中断（如果被启用），并且每个 I/O 端口都有一个与其相关的中断请求（IRQ）和中断服务程序（ISR）。

I/O 端口的电源映射如 [CROSS-REF] 所示。当配置为 CMOS 和汽车级阈值时，相应的电源决定了 V_{OH} 、 V_{OL} 、 V_{IH} 和 V_{IL} 的电平。

表 7 I/O 端口电源

Supply pins	Ports
VDDD ¹⁾	P0
VDDIO_GPIO_1 ¹⁾	P1, P2, P3
VDDIO_GPIO_2 ¹⁾	P4, P5, P6
VDDIO_SMC ¹⁾	P7, P8, P9
VDDIO_HSIO	P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21

1) 确保 $V_{DDD} \geq (V_{DDIO_GPIO_1} - 0.3 \text{ V}) \geq (V_{DDIO_GPIO_2} - 0.3 \text{ V})$ 。

所有 I/O 均支持以下可编程驱动模式：

- 高阻态
- 电阻上拉
- 电阻下拉
- 开漏和强下拉
- 开漏和强上拉
- 强上拉或下拉
- 弱上拉或下拉

CYT3DL 有四种类型的可编程 GPIO：GPIO 标准、GPIO 增强、GPIO SMC、HSIO 标准低噪声。只有 GPIO_STD、GPIO_ENH 和 GPIO_SMC 能够将器件从深度睡眠模式中唤醒。所有这些 I/O 都具有 GPIO 输入/输出功能，其中一些可能需要特殊配置¹²⁾。

3.5.1 GPIO

支持三种类型的 GPIO：

- GPIO_STD, GPIO_ENH, 和 GPIO_SMC

这些 GPIO 类型实现以下功能：

- 可配置输入阈值（CMOS、TTL 或汽车）
- 保持模式，用于锁存先前状态（即保持 I/O 状态处于深度睡眠模式）
- 模拟输入模式（输入和输出缓冲器禁用）
- 基于引脚，可配置为上升沿、下降沿或双边沿触发的中断

3.5.1.1 GPIO 标准 (GPIO_STD)

支持 2.7 V 至 5.5 V V_{DDIO} 范围内的标准汽车信号。GPIO_STD I/O 具有多种可配置的驱动级别、驱动模式和可选的输入电平。

¹²⁾ 有关 I/O 配置的更多信息，请参阅特定系列的架构 TRM（002-25800，TRAVEO™ T2G Automotive MCU cluster 2D 架构技术参考手册）。

3 功能描述

3.5.1.2 GPIO 增强 (GPIO_ENH)

GPIO 支持 2.7 V 至 5.5 V V_{DDIO} 范围内的扩展功能汽车信号传输，在较低电压下具有较高的电流（完全 I2C 时序支持、斜率控制）。

3.5.1.3 GPIO SMC (GPIO_SMC)

与 GPIO_STD 和 GPIO_ENH 相比，此 GPIO 可提供更强的驱动力（支持 30 mA 驱动）。

3.5.2 HSIO

这些 I/O 专门针对高速信号传输进行了优化，不支持斜率控制、深度睡眠模式操作、POR 模式控制、模拟连接或非 CMOS 信号传输级别。HSIO 还支持可编程驱动强度。它们仅在工作模式下可用。

3.5.2.1 HSIO 标准低噪声 (HSIO_STDLN)

对于 BGA 封装和 TEQFP 封装，I/O 支持高达 133 MHz 和 100 MHz 的时钟和信号。支持高速外设，如图形输入/输出和以太网。还支持在深度睡眠模式下保持状态。低噪音版通过为每个接口支持特定的模式来优化产生的噪音。

3.5.3 端口命名规则

Px.y 描述 I/O 端口“x”内可用的特定位“y”。

例如，P4.2 读取“端口 4，位 2”。

3.5.4 智能 I/O

智能 I/O 允许对从芯片子系统发送到 I/O 的信号或进入芯片的信号进行布尔运算。CYT3DL 有一个智能 I/O 功能块。操作可以是同步或异步，并且块可以在除休眠之外的所有器件功耗模式下操作。

4 CYT3DL 地址映射**4 CYT3DL 地址映射**

CYT3DL 微控制器支持所示的存储空间如 [图 3](#)：

- 4160 KB (4032 KB + 128 KB) 代码闪存，根据闪存控制寄存器中的相关位，用于单组或双组模式
 - 单组模式：4160 KB
 - 双组模式：每组 2080 KB
- 128 KB (92 KB + 32 KB) 工作闪存，根据闪存控制寄存器中的相关位，用于单组或双组模式
 - 单组模式：128 KB
 - 双组模式：每组 64 KB
- 64 KB 安全 ROM
- 384 KB SRAM (前 2 KB 保留供内部使用)
- 每个 Cortex®-M7 CPU 有 64 KB 的指令 TCM
- 每个 Cortex®-M7 CPU 有 64 KB 的数据 TCM
- 512 MB SMIF XIP1
- 512 MB SMIF XIP2
- 2048 KB VRAM

4 CYT3DL 地址映射

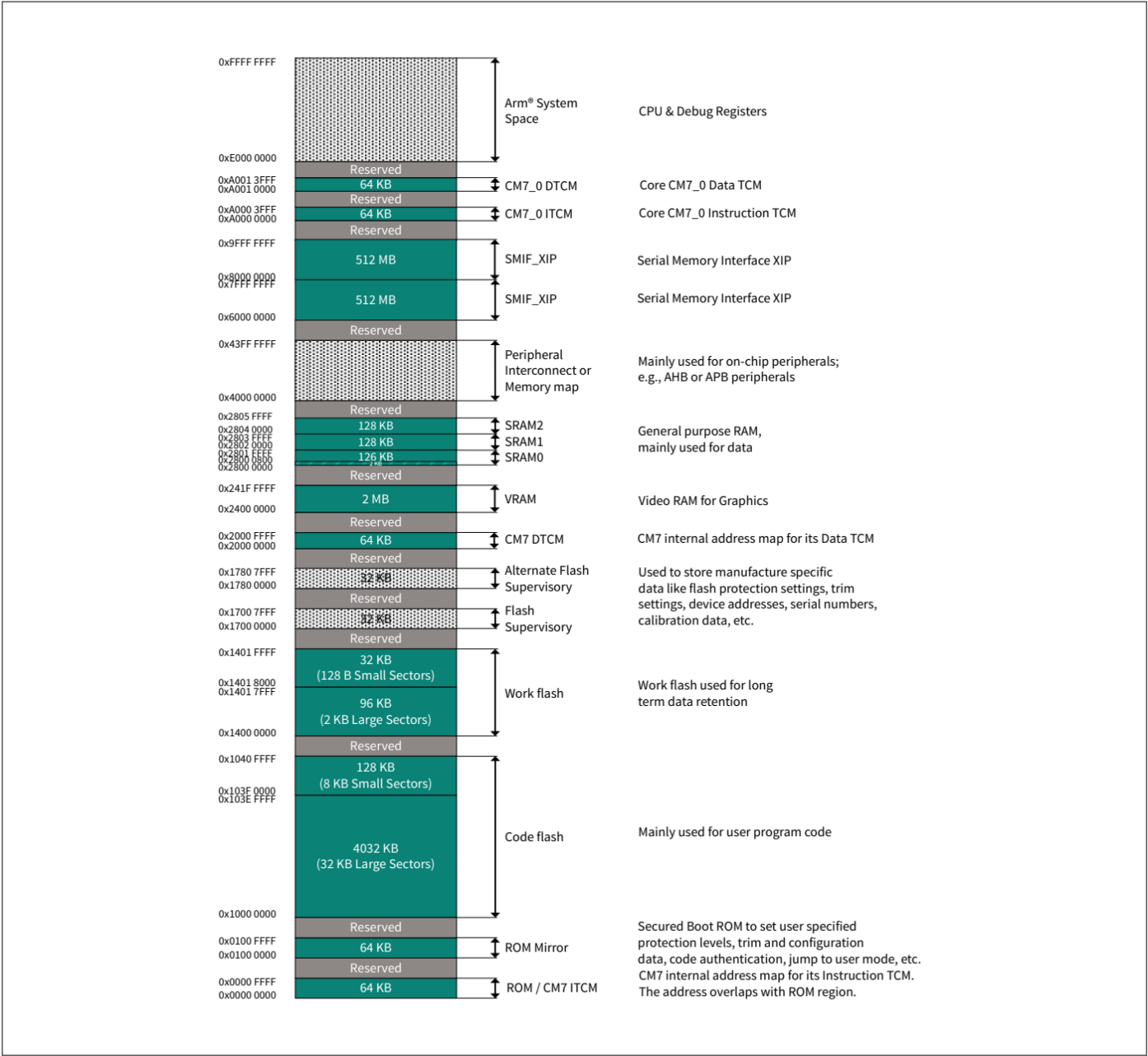


图 3 CYT3DL 地址映射¹³⁾, ¹⁴⁾

¹³⁾ 尺寸不是等比例缩放。

¹⁴⁾ SRAM 的前 2 KB 被保留, 不供用户使用。用户必须在所有工作、低功耗工作、睡眠、低功耗睡眠、深度睡眠模式下, 将 SRAM0 前 32 KB 功能块的电源保持在使能或保留状态。

5 闪存基地址映射

5 闪存基地址映射

表 8 至表 13 提供有关代码和工作闪存区域的扇区映射及其各自基地址的信息。

表 8 单组模式下代码闪存地址映射

Code-flash Size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large Sector Base Address	Small Sector Base Address
4160	32 KB × 126	8 KB × 16	0x1000 0000	0x103F 0000

表 9 单组模式下工作闪存地址映射

Work-flash Size (KB)	Large Sectors	Small Sectors	Large Sector Base Address	Small Sector Base Address
128	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000

表 10 双组模式下的代码闪存地址映射（映射 A）

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1000 0000	0x101F 8000	0x1200 0000	0x121F 8000

表 11 双组模式下的代码闪存地址映射（映射 B）

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1200 0000	0x121F 8000	0x1000 0000	0x101F 8000

表 12 双组模式下工作闪存地址映射（映射 A）

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1400 0000	0x1400 C000	0x1500 0000	0x1500 C000

表 13 双组模式下的工作闪存地址映射（映射 B）

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1500 0000	0x1500 C000	0x1400 0000	0x1401 8000

6 外设 I/O 映射

6 外设 I/O 映射

表 14 CYT3DL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	Group	Slave
PERI	Peripheral interconnect	0x4000 0000			0	0
	Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9, 10)	0x4000 4000	10	0x40		
	Peripheral trigger group	0x4000 8000	13	0x400		
	Peripheral 1:1 trigger group	0x4000 C000	8	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4002 0000			0	1
	PERI Programmable PPU	0x4002 0000	101)	0x40		
	PERI Fixed PPU	0x4002 0800	582	0x40		
PERI_PCLK	Peripheral Clock Groups	0x4004 0000	2	0x2000	0	2
Crypto	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000			2	2
	IPC structures	0x4022 0000	8	0x20		
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000			2	3
	Shared memory protection unit structures	0x4023 2000	16	0x40		
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	Flash controller	0x4024 0000			2	4
SRSS	System Resources Subsystem Core Registers	0x4026 0000			2	5
	Clock Supervision High Frequency	0x4026 1400	14	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Clock PLL 400 MHz	0x4026 1900	5	0x10		
	Multi Counter WDT	0x4026 8000	2	0x100		
	Free Running WDT	0x4026 C000	1			
BACKUP	SRSS Backup Domain/RTC	0x4027 0000			2	6

(表格续下页.....)

6 外设 I/O 映射
表 14 (续) CYT3DL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	Group	Slave
	Backup Register	0x4027 1000	4	0x04		
P-DMA	P-DMA 0 Controller	0x4028 0000			2	7
	P-DMA 0 channel structures	0x4028 8000	76	0x40		
	P-DMA 1 Controller	0x4029 0000			2	8
	P-DMA 1 channel structures	0x4029 8000	84	0x40		
M-DMA	M-DMA0 Controller (AHB Bus)	0x402A 0000			2	9
	M-DMA0 channels	0x402A 1000	8	0x100		
	M-DMA1 Controller (AXI Bus)	0x402B 0000			2	10
	M-DMA1 channels	0x402B 1000	8	0x100		
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	11
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	21	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	21	0x80	3	1
SMARTIO	Programmable I/O configuration	0x4032 0000			3	2
	SMARTIO port configuration	0x4032 0C00	1	0x100		
TCPWM	Timer/Counter/PWM 0 (TCPWM0)	0x4038 0000			3	3
	TCPWM0 Group #0 (16-bit)	0x4038 0000	38	0x80		
	TCPWM0 Group #1 (16-bit, Motor control)	0x4038 8000	12	0x80		
	TCPWM0 Group #2 (32-bit)	0x4039 0000	32	0x80		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	4
	Event generator 0 comparator structures	0x403F 0800	16	0x20		
SMIF	Serial Memory Interface 0 (SMIF0)	0x4042 0000			4	0
	SMIF0 Devices	0x4042 0800	2	0x80		
	Serial Memory Interface 1 (SMIF1)	0x4043 0000			4	1
	SMIF1 Devices	0x4043 0800	2	0x80		
ETH	Ethernet 0 (ETH0)	0x4048 0000	1		4	2
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	2	0x100		
CXPI	Clock Extension Peripheral Interface 0 (CXPI0)	0x4051 0000			5	1
	CXPI0 Channels	0x4051 8000	2	0x100		
CAN	CAN0 controller	0x4052 0000	2	0x200	5	2
	Message RAM CAN0	0x4053 0000	2	0x4000		

(表格续下页.....)

6 外设 I/O 映射
表 14 (续) CYT3DL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	Group	Slave
	CAN1 controller	0x4054 0000		0x200	5	3
	Message RAM CAN1	0x4055 0000	2	0x4000		
SCB	Serial Communications Block (SPI/UART/I2C)	0x4060 0000	12	0x10000	6	0-11
Sound	Time Division Multiplexer 0 (TDM0)	0x4081 0000			8	0
	TDM0 Structures	0x4081 8000	2	0x200		
	Sound Generator 0 (SG0)	0x4082 0000			8	1
	SG0 Structures	0x4082 8000	5	0x100		
	Pulse Width Modulation 0 (PWM0)	0x4083 0000			8	2
	PWM0 Structures	0x4083 8000	2	0x100		
	Audio DAC0	0x4084 0000	1		8	3
	Mixer0	0x4088 0000			8	4
	Mixer0 Source Structures	0x4088 8000	5	0x100		
	Mixer0 Destination Structures	0x4088 C000	1			
	Mixer1	0x4089 0000			8	5
	Mixer1 Source Structures	0x4089 8000	5	0x100		
	Mixer1 Destination Structures	0x4089 C000	1			
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR0 channel structures	0x4090 0800	24 ²⁾	0x40		
	SAR1 channel structures	0x4090 1800	24	0x40		
Graphics	Video Subsystem (VIDEOSS0)	0x40A0 0000			10	0
	Display Engine	0x40AA 0000	2	0x4000		
	FPD-Link	0x40AC 0000	2	0x8000		
	MIPI CSI0	0x40AD 0000	1			

- 1) 这些可编程 PPU 由 Boot ROM 配置，并根据访问权限供用户使用。请参阅特定于设备的 TRM 以了解有关这些可编程 PPU 的配置的更多信息。
- 2) 其余 24 个外部通道通过 SAR1 多路复用器访问。(SAR0 使用 SARMUX1)。

7 CYT3DL clock diagram

7 CYT3DL clock diagram

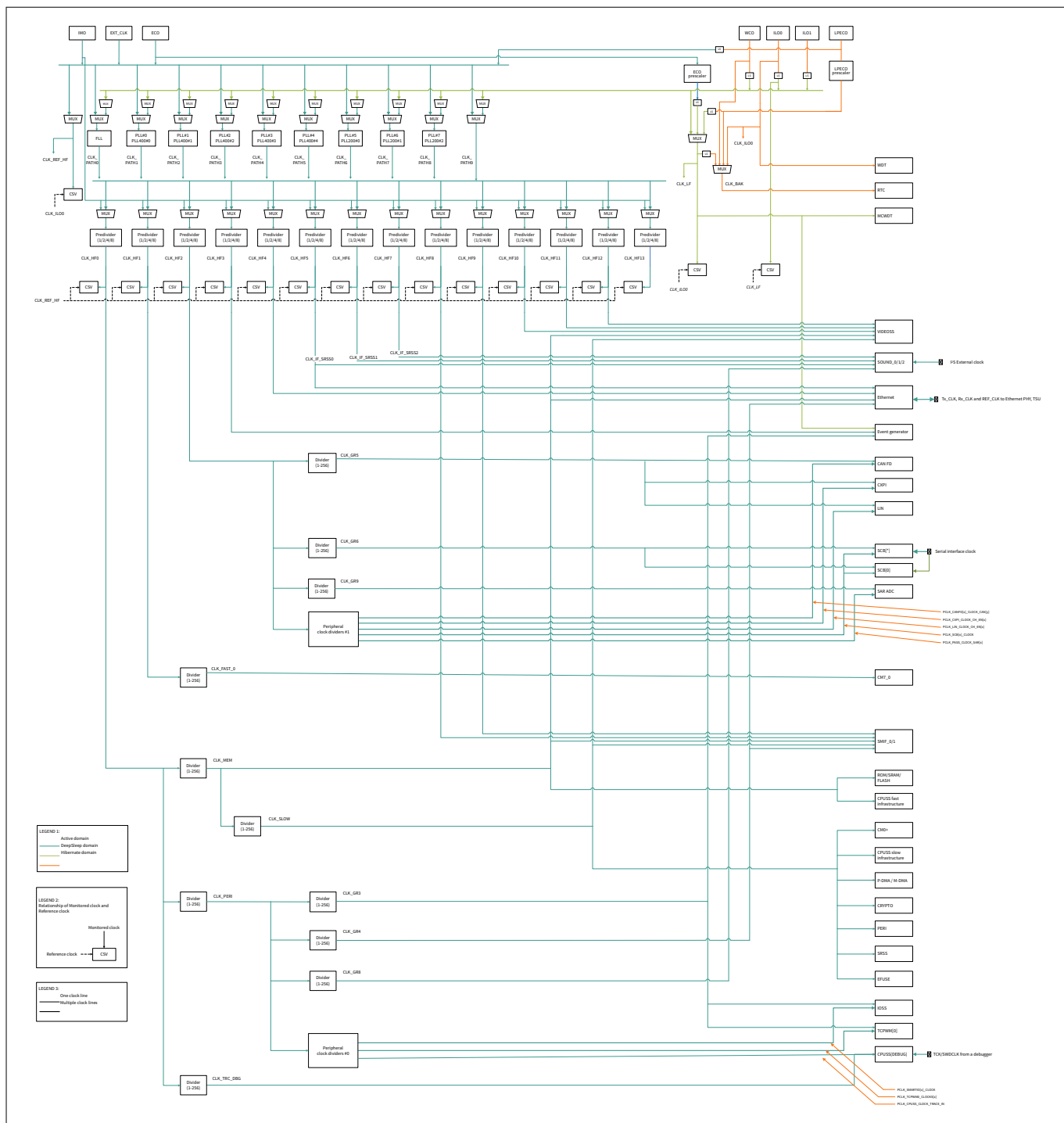


Figure 4 **CYT3DL clock diagram**

8 CTY3DL CPU 启动序列

8 CYT3DL CPU 启动序列

启动顺序按以下步骤描述：

1. 系统复位 (@0x0000 0000)
2. CM0+ 执行 ROM 启动 (@0x0000 0004)
 - a. 应用微调值
 - b. 应用调试访问端口 (DAP) 访问限制，以及来自 eFuse 和监督闪存的系统保护
 - c. 验证闪存启动 (仅在安全生命周期阶段) 并将控制权转移给闪存启动
3. CM0+ 执行闪存启动 (来自监控闪存 @0x1700 2000)
 - a. 调试引脚根据 SWD/JTAG 规格配置 ¹⁵⁾
 - b. 将 CM0+ 向量偏移寄存器 (Arm® 系统空间的 CM0_VTOR 部分) 设置为闪存的起始地址 (@0x1000 0000)
 - c. CM0+ 分支到其复位处理程序
4. CM0+ 开始执行
 - a. 将 CM0+ 向量表移至 SRAM (更新 CM0+ 向量表基址)
 - b. 为不同的存储器子系统设置等待状态
 - c. 设置根时钟、启用内核外部电源 (PMIC)、图形子系统等。
 - d. 为 CM7_0 设置时钟 (CLK_HF1)
 - e. 将 CM7_0 (CM7_0_VECTOR_TABLE_BASE @0x4020 0200) 向量表设置到相应位置，该位置也在闪存中指定 (在链接器定义文件中指定)。
 - f. 为 CPU 核心 CM7_0 启用电源
 - g. 禁用 CPU_WAIT，以便调试器能够访问它
 - h. 从复位状态释放 CM7_0
 - i. 继续执行 CM0+ 用户应用程序
5. CM7_0 直接从代码闪存或 SRAM 执行
 - a. CM7_0 分支到其复位处理程序
 - b. 继续执行用户应用程序

¹⁵⁾ SWD/JTAG 引脚的端口配置将从默认的 GPIO 模式更改，以支持启动过程后的调试，参见表 16 获取引脚分配相关信息。

9 引脚分配

9 引脚分配

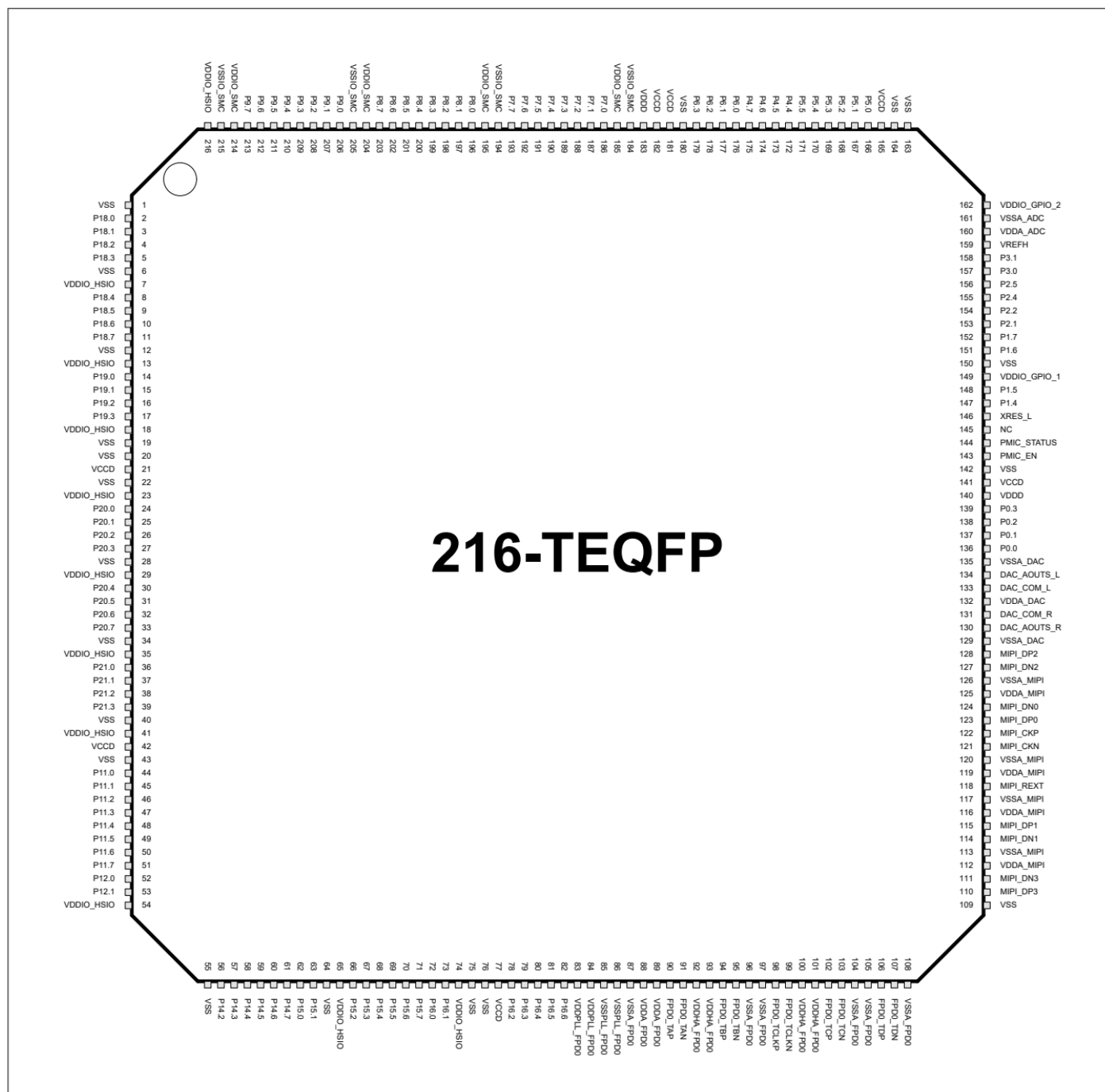


图 5 216-TEQFP 引脚分配¹⁶⁾

¹⁶⁾ 将 TEQFP 器件的裸露焊垫连接到接地。

9 Pin assignment

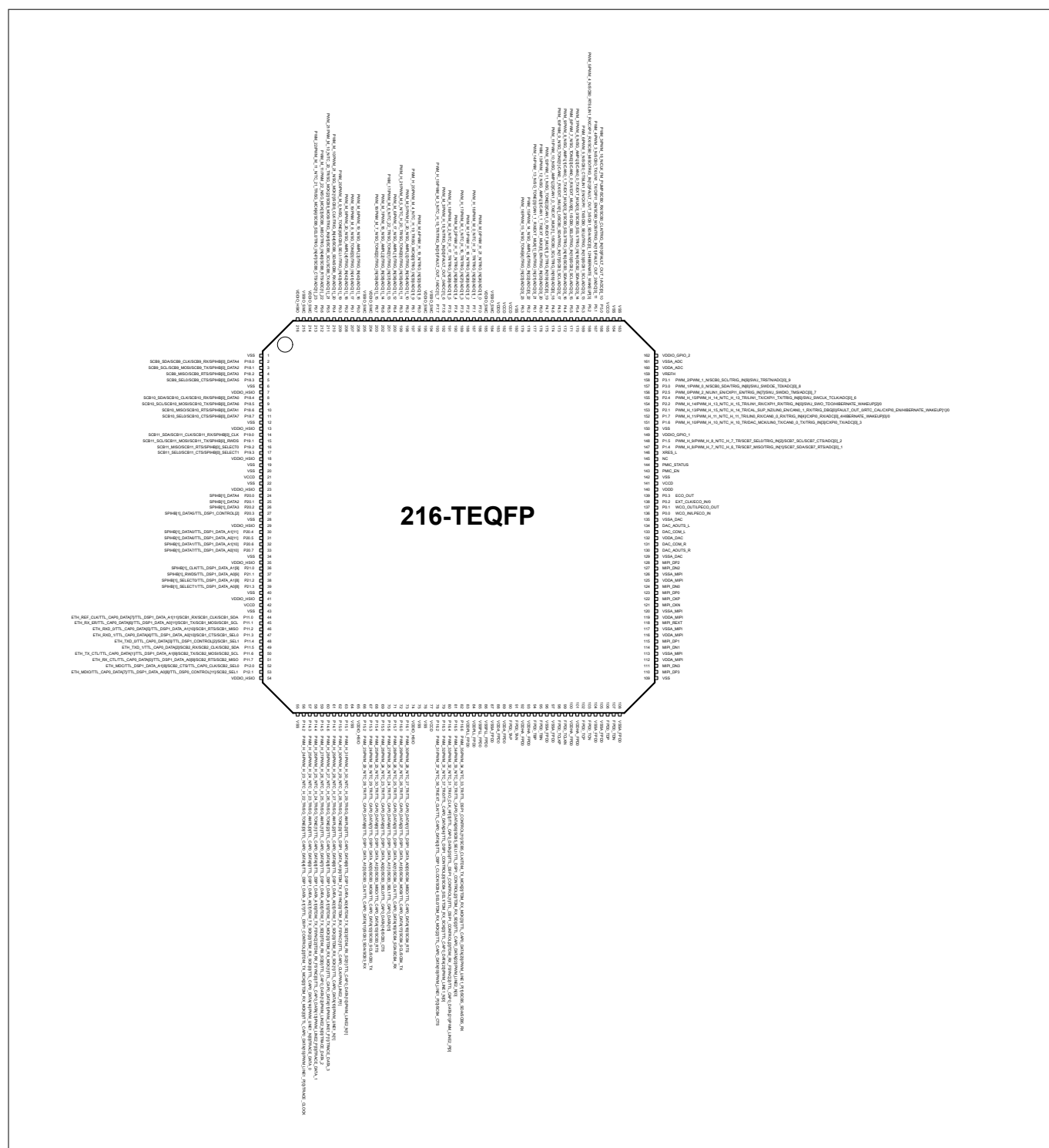


Figure 6 216-TEQFP pin assignment with alternate functions¹⁶⁾

¹⁶⁾ Connect exposure pad of TEQFP devices to the ground.

9 引脚分配

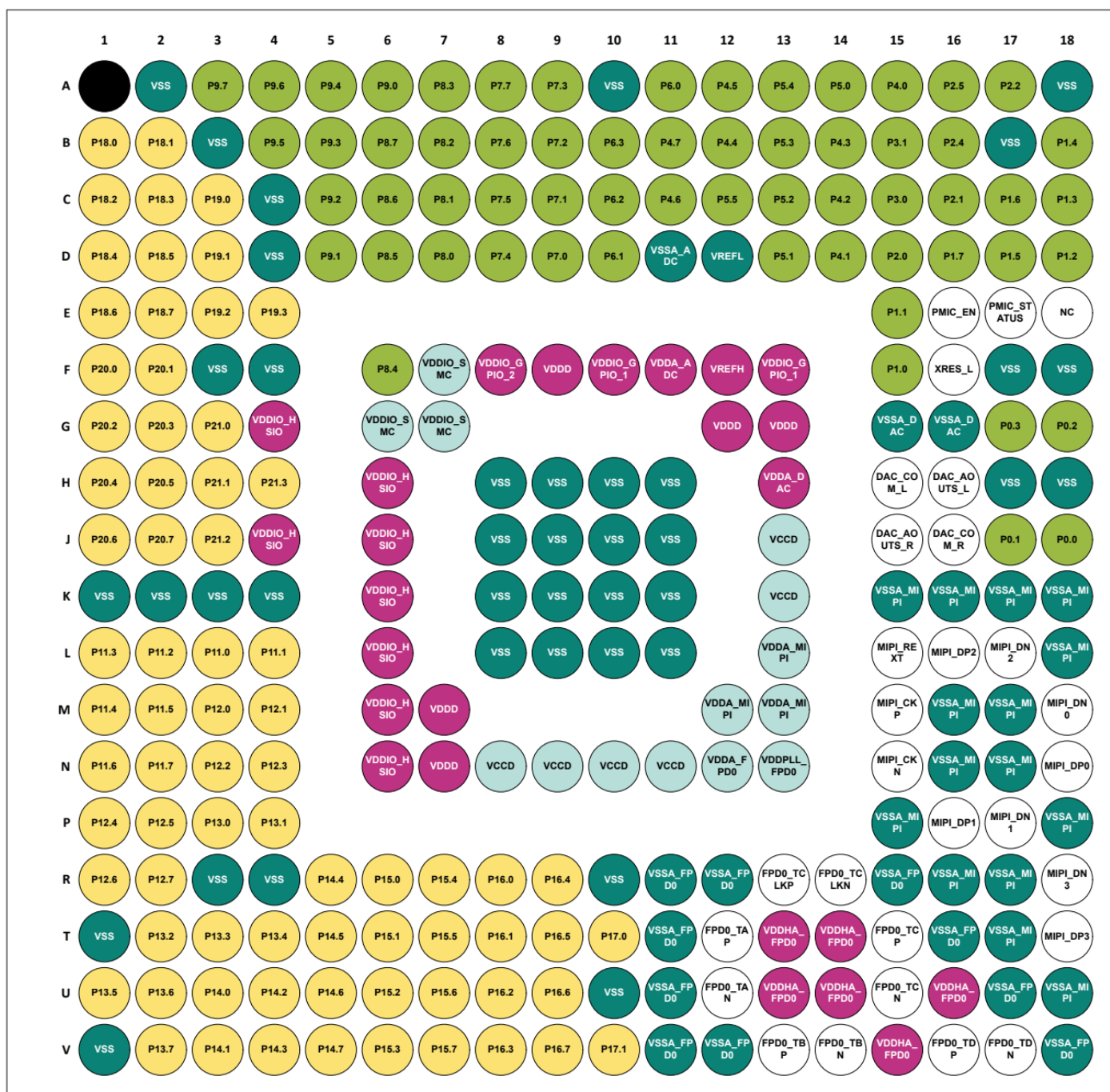


图 7 272-BGA 球图

10 高速 I/O 矩阵连接

10 高速 I/O 矩阵连接

表 15 HSIOM 连接参考

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7

11 封装引脚列表和备用功能
11 封装引脚列表和备用功能

大多数引脚具有备用功能，如表 16 所示。

表 16 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ³⁾ , ⁴⁾	DS #6			
P0.0	J18	136	GPIO_STD			Not supported	WCO_IN, LPECO_IN ⁵⁾	
P0.1	J17	137	GPIO_STD				WCO_OUT, LPECO_OUT ⁵⁾	
P0.2	G18	138	GPIO_STD				ECO_IN ⁵⁾	
P0.3	G17	139	GPIO_STD				ECO_OUT ⁵⁾	
P1.0	F15	NA	GPIO_STD			Supported		
P1.1	E15	NA	GPIO_STD					
P1.2	D18	NA	GPIO_STD					
P1.3	C18	NA	GPIO_STD				ADC[0]_0	
P1.4	B18	147	GPIO_STD				ADC[0]_1	
P1.5	D17	148	GPIO_STD				ADC[0]_2	
P1.6	C17	151	GPIO_STD			Not supported	ADC[0]_3	
P1.7	D16	152	GPIO_STD			Supported	ADC[0]_4, HIBERNATE_WAKEUP[0]	
P2.0	D15	NA	GPIO_STD				ADC[0]_5	
P2.1 ⁶⁾	C16	153	GPIO_STD	RTC_CAL		Not supported	HIBERNATE_WAKEUP[1]	
P2.2	A17	154	GPIO_STD	SWJ_SWO_TDO			HIBERNATE_WAKEUP[2]	
P2.4	B16	155	GPIO_STD	SWJ_SWCLK_TCLK		Supported	ADC[0]_6	
P2.5	A16	156	GPIO_STD	SWJ_SWDIO_TMS			ADC[0]_7	
P3.0	C15	157	GPIO_ENH	SWJ_SWDOE_TDI	SCB0_SDA		ADC[0]_8	
P3.1	B15	158	GPIO_ENH	SWJ_TRSTN	SCB0_SCL		ADC[0]_9	
P4.0	A15	NA	GPIO_STD			Supported		

(表格续下页.....)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ^{3), 4)}	DS #6			
P4.1	D14	NA	GPIO_STD					
P4.2	C14	NA	GPIO_STD					
P4.3	B14	NA	GPIO_STD			Supported		
P4.4	B12	172	GPIO_STD		SCB0_SE L3	Not supported	ADC[0]_16	
P4.5	A12	173	GPIO_STD		SCB0_SD A ⁷⁾		ADC[0]_17	
P4.6	C11	174	GPIO_STD		SCB0_SCL ⁷⁾		ADC[0]_18	
P4.7	B11	175	GPIO_STD				ADC[0]_19	
P5.0	A14	166	GPIO_ENH		SCB0_CLK		ADC[0]_10	
P5.1	D13	167	GPIO_ENH		SCB0_MOSI		ADC[0]_11	
P5.2	C13	168	GPIO_ENH		SCB0_MISO		ADC[0]_12, HIBERNATE_WAKEUP[3]	
P5.3	B13	169	GPIO_ENH		SCB0_SE L0		ADC[0]_13	
P5.4	A13	170	GPIO_ENH		SCB0_SE L1		ADC[0]_14	
P5.5	C12	171	GPIO_ENH		SCB0_SE L2		ADC[0]_15	
P6.0	A11	176	GPIO_STD				ADC[0]_20	
P6.1	D10	177	GPIO_STD				ADC[0]_21	
P6.2	C10	178	GPIO_STD				ADC[0]_22	
P6.3	B10	179	GPIO_STD				ADC[0]_23	
P7.0	D9	186	GPIO_SMC			Supported	ADC[1]_0	
P7.1	C9	187	GPIO_SMC				ADC[1]_1	
P7.2	B9	188	GPIO_SMC				ADC[1]_2	
P7.3	A9	189	GPIO_SMC				ADC[1]_3	
P7.4	D8	190	GPIO_SMC				ADC[1]_4	

(表格续下页...)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ^{3), 4)}	DS #6			
P7.5	C8	191	GPIO_SMC				ADC[1]_5	
P7.6	B8	192	GPIO_SMC				ADC[1]_6	
P7.7	A8	193	GPIO_SMC				ADC[1]_7	
P8.0	D7	196	GPIO_SMC				ADC[1]_8	
P8.1	C7	197	GPIO_SMC				ADC[1]_9	
P8.2	B7	198	GPIO_SMC			Supported	ADC[1]_10	
P8.3	A7	199	GPIO_SMC				ADC[1]_11	
P8.4	F6	200	GPIO_SMC				ADC[1]_12	
P8.5	D6	201	GPIO_SMC				ADC[1]_13	
P8.6	C6	202	GPIO_SMC				ADC[1]_14	
P8.7	B6	203	GPIO_SMC				ADC[1]_15	
P9.0	A6	206	GPIO_SMC				ADC[1]_16	SMART IO9_0
P9.1	D5	207	GPIO_SMC				ADC[1]_17	SMART IO9_1
P9.2	C5	208	GPIO_SMC				ADC[1]_18	SMART IO9_2
P9.3	B5	209	GPIO_SMC				ADC[1]_19	SMART IO9_3
P9.4	A5	210	GPIO_SMC			Supported	ADC[1]_20	SMART IO9_4
P9.5	B4	211	GPIO_SMC				ADC[1]_21	SMART IO9_5
P9.6	A4	212	GPIO_SMC				ADC[1]_22	SMART IO9_6
P9.7	A3	213	GPIO_SMC				ADC[1]_23	SMART IO9_7
P11.0	L3	44	HSIO_STDLN			Not supported		
P11.1	L4	45	HSIO_STDLN					
P11.2	L2	46	HSIO_STDLN					

(表格续下页...)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ^{3), 4)}	DS #6			
P11.3	L1	47	HSIO_STDLN					
P11.4	M1	48	HSIO_STDLN					
P11.5	M2	49	HSIO_STDLN					
P11.6	N1	50	HSIO_STDLN					
P11.7	N2	51	HSIO_STDLN					
P12.0	M3	52	HSIO_STDLN					
P12.1	M4	53	HSIO_STDLN					
P12.2	N3	NA	HSIO_STDLN					
P12.3	N4	NA	HSIO_STDLN					
P12.4	P1	NA	HSIO_STDLN					
P12.5	P2	NA	HSIO_STDLN					
P12.6	R1	NA	HSIO_STDLN					
P12.7	R2	NA	HSIO_STDLN					
P13.0	P3	NA	HSIO_STDLN			Not supported		
P13.1	P4	NA	HSIO_STDLN					
P13.2	T2	NA	HSIO_STDLN					
P13.3	T3	NA	HSIO_STDLN					

(表格续下页.....)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin			DS #5 ³⁾ , ⁴⁾			
P13.4	T4	NA	HSIO_STDLN					
P13.5	U1	NA	HSIO_STDLN					
P13.6	U2	NA	HSIO_STDLN					
P13.7	V2	NA	HSIO_STDLN					
P14.0	U3	NA	HSIO_STDLN					
P14.1	V3	NA	HSIO_STDLN					
P14.2	U4	56	HSIO_STDLN					
P14.3	V4	57	HSIO_STDLN					
P14.4	R5	58	HSIO_STDLN					
P14.5	T5	59	HSIO_STDLN					
P14.6	U5	60	HSIO_STDLN					
P14.7	V5	61	HSIO_STDLN					
P15.0	R6	62	HSIO_STDLN					
P15.1	T6	63	HSIO_STDLN					
P15.2	U6	66	HSIO_STDLN					
P15.3	V6	67	HSIO_STDLN					
P15.4	R7	68	HSIO_STDLN					

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11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ^{3), 4)}	DS #6			
P15.5	T7	69	HSIO_STDLN			Not supported		
P15.6	U7	70	HSIO_STDLN					
P15.7	V7	71	HSIO_STDLN					
P16.0	R8	72	HSIO_STDLN					
P16.1	T8	73	HSIO_STDLN					
P16.2	U8	78	HSIO_STDLN					
P16.3	V8	79	HSIO_STDLN					
P16.4	R9	80	HSIO_STDLN					
P16.5	T9	81	HSIO_STDLN					
P16.6	U9	82	HSIO_STDLN					
P16.7	V9	NA	HSIO_STDLN					
P17.0	T10	NA	HSIO_STDLN					
P17.1	V10	NA	HSIO_STDLN					
P18.0	B1	2	HSIO_STDLN					
P18.1	B2	3	HSIO_STDLN					
P18.2	C1	4	HSIO_STDLN					
P18.3	C2	5	HSIO_STDLN					

(表格续下页.....)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ³⁾ , ⁴⁾	DS #6			
P18.4	D1	8	HSIO_STDLN					
P18.5	D2	9	HSIO_STDLN					
P18.6	E1	10	HSIO_STDLN					
P18.7	E2	11	HSIO_STDLN					
P19.0	C3	14	HSIO_STDLN					
P19.1	D3	15	HSIO_STDLN					
P19.2	E3	16	HSIO_STDLN			Not supported		
P19.3	E4	17	HSIO_STDLN					
P20.0	F1	24	HSIO_STDLN					
P20.1	F2	25	HSIO_STDLN					
P20.2	G1	26	HSIO_STDLN					
P20.3	G2	27	HSIO_STDLN					
P20.4	H1	30	HSIO_STDLN					
P20.5	H2	31	HSIO_STDLN					
P20.6	J1	32	HSIO_STDLN					
P20.7	J2	33	HSIO_STDLN					
P21.0	G3	36	HSIO_STDLN					

(表格续下页.....)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping		+B input ¹⁾	Analog/HV	SMART IO
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾			
	Pin	Pin		DS #5 ³⁾ , ⁴⁾	DS #6			
P21.1	H3	37	HSIO_STDLN					
P21.2	J3	38	HSIO_STDLN					
P21.3	H4	39	HSIO_STDLN					
FPD0_TAP	T12	90						
FPD0_TAN	U12	91						
FPD0_TBP	V13	94						
FPD0_TBN	V14	95						
FPD0_TCLKP	R13	98						
FPD0_TCLKN	R14	99						
FPD0_TCP	T15	102						
FPD0_TCN	U15	103				Not supported		
FPD0_TDP	V16	106						
FPD0_TD N	V17	107						
MIPI_DP3	T18	110						
MIPI_DN3	R18	111						
MIPI_DN1	P17	114						
MIPI_DP1	P16	115						
MIPI_REXT	L15	118						
MIPI_CKN	N15	121						
MIPI_CKP	M15	122						
MIPI_DP0	N18	123						
MIPI_DN0	M18	124						
MIPI_DN2	L17	127						
MIPI_DP2	L16	128						

(表格续下页.....)

11 封装引脚列表和备用功能
表 16 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping			+B input ¹⁾	Analog/HV	SMART I/O
	272-BGA	216-TEQFP		HCon#0	HCon#29 ²⁾	HCon#30			
	Pin	Pin		DS #5 ³⁾ , ⁴⁾	DS #6				
DAC_AOU TS_R	J15	130							
DAC_COM _R	J16	131							
DAC_COM _L	H15	133							
DAC_AOU TS_L	H16	134							
PMIC_EN	E16	143							
PMIC_STA TUS	E17	144							
XRES_L	F16	146							

1) 有关 +B 条件和钳位电流规格，请参阅[绝对最大额定值](#)章节。

2) 高速 I/O 矩阵连接 (HCON) 基准可参见[表 15](#)。

3) 深度睡眠排序 (DS#0、DS#1、DS#2) 对选择任何备用功能没有任何影响；HSIOM 模块负责处理各个备用功能的分配。

4) 所有在深度睡眠模式下可用的端口引脚功能在工作模式下也可用。

5) 如果振荡器已启用，则支持振荡器功能 (WCO 或 ECO) 的 I/O 引脚必须配置为高阻抗。

6) 当 VDDD 低于 POR 阈值时，此 I/O 将出现增大的对地漏电流。

7) 参见[表 39](#)“串行通信模块 (SCB) 规格”，了解支持的 I/O 单元和 I2C 模式。

12 电源引脚分配

12 电源引脚分配

表 17 电源引脚分配

Name	Package		Remarks
	272-BGA	216-TEQFP	
VDDD	M7, N7, G12, G13, F9	140, 183	Main supply for SRSS
VSS	A2, B3, C4, D4, F3, F4, K1, K2, K3, K4, R3, R4, T1, V1, R10, U10, H17, H18, F17, F18, A18, B17, A10, H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11	1, 6, 12, 19, 20, 22, 28, 34, 40, 43, 55, 64, 75, 76, 109, 142, 150, 163, 164, 180	Main digital ground
VDDIO_HSIO	G4, J4, H6, J6, K6, L6, M6, N6	7, 13, 18, 23, 29, 35, 41, 54, 65, 74, 216	Supply for HSIO (3.0 V - 5.5 V)
VDDIO_GPIO_1	F10, F13	149	Supply for GPIO 1 (2.7V - 5.5V)
VDDIO_GPIO_2	F8	162	Supply for GPIO 2 (2.7V - 5.5V)
VDDIO_SMC	F7, G6, G7	185, 195, 204, 214	GPIO SMC supply (2.7 V - 5.5 V)
VSSIO_SMC	NA	184, 194, 205, 215	GPIO SMC ground
VDDPLL_FPD0	N13	83, 84	Dedicated supplies for FPD0 1.15 V
VSSPLL_FPD0	NA	85, 86	Dedicated ground for FPD0
VDDHA_FPD0	T13, T14, U13, U14, V15, U16	92, 93, 100, 101	Dedicated supplies for FPD0 (3.0 V - 3.6 V)
VDDA_FPD0	N12	88, 89	Dedicated supplies for FPD0 1.15 V
VSSA_FPD0	V18, U17, T16, R15, V12, R12, V11, U11, T11, R11	87, 96, 97, 104, 105, 108	Dedicated ground for FPD0
VDDA_MIPI	M12, M13, L13	112, 116, 119, 125	Dedicated supplies for MIPI 1.15 V
VSSA_MIPI	U18, T17, R16, P15, R17, P18, N16, N17, M16, M17, L18, K18, K17, K16, K15	113, 117, 120, 126	Dedicated ground for MIPI
VCCD ¹⁾	J13, K13, N8, N9, N10, N11	21, 42, 77, 141, 165, 181, 182	Main regulated supply. Driven by external PMIC.
VREFH	F12	159	High reference voltage for SAR
VREFL	D12	161	Low reference voltage for SAR
VDDA_ADC	F11	160	Main analog supply (for PASS/ SAR, 2.7 V - 5.5 V)
VSSA_ADC	D11	161	Main analog ground
VDDA_DAC	H13	132	Supply for DAC (3.0 V - 3.6 V)
VSSA_DAC	G15, G16	129, 135	Ground for DAC

 1) V_{CCD} 引脚必须连接在一起，以确保低阻抗连接。（参见图 11 中的要求）。

13 备用功能引脚分配

13 备用功能引脚分配

表 18 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P0.0													
P0.1													
P0.2										EXT_CLK			
P0.3													
P1.0	PWM0_H_4	PWM0_H_3_N	TC0_H_2_TR										SCB6_MISO
P1.1	PWM0_H_5	PWM0_H_4_N	TC0_H_3_TR										SCB6_CTS
P1.2	PWM0_H_6	PWM0_H_5_N	TC0_H_4_TR										SCB7_C_LK
P1.3	PWM0_H_7	PWM0_H_6_N	TC0_H_5_TR						TRIG_D_BG[1]				SCB7_TX
P1.4	PWM0_H_8	PWM0_H_7_N	TC0_H_6_TR						TRIG_I_N[1]				SCB7_RTSDA ⁶⁾
P1.5	PWM0_H_9	PWM0_H_8_N	TC0_H_7_TR						TRIG_I_N[2]				SCB7_CTS
P1.6	PWM0_H_10	PWM0_H_10_N	TC0_H_10_TR						TRIG_I_N[3]		DAC_MCK	LIN0_TX	CAN0_0_TX
P1.7	PWM0_H_11	PWM0_H_11_N	TC0_H_11_TR						TRIG_I_N[4]			LIN0_RX	CAN0_0_RX
P2.0	PWM0_H_12	PWM0_H_12_N	TC0_H_12_TR						TRIG_I_N[5]			LIN0_EN	CAN0_1_TX

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P2.1	PWM0_H_13	PWM0_H_15_N	TC0_H_14_TR						TRIG_DBG[0]		CAL_SU_P_NZ	LIN0_EN	CAN0_1_RX
P2.2	PWM0_H_14	PWM0_H_13_N	TC0_H_15_TR						TRIG_I_N[0]			LIN1_RX	CXPI1_RX
P2.4	PWM0_H_15	PWM0_H_14_N	TC0_H_13_TR						TRIG_I_N[6]			LIN1_TX	CXPI1_TX
P2.5	PWM0_0	PWM0_2_N							TRIG_I_N[7]			LIN1_EN	CXPI1_EN
P3.0	PWM0_1	PWM0_0_N							TRIG_I_N[8]				
P3.1	PWM0_2	PWM0_1_N							TRIG_I_N[9]				
P4.0	PWM0_H_2	PWM0_H_1_N	TC0_H_0_TR										SCB6_C_LK
P4.1	PWM0_H_3	PWM0_H_2_N	TC0_H_1_TR										SCB6_RX
P4.2	PWM0_H_0	PWM0_H_9_N	TC0_H_8_TR										SCB6_TX
P4.3	PWM0_H_1	PWM0_H_0_N	TC0_H_9_TR										SCB6_MOSI
P4.4	PWM0_9	PWM0_8_N											SCB6_EL1
													SCB7_EL1
													CAN0_1_TX
													SCB3_S_DA ⁶⁾
													SCB6_S_DA ⁶⁾

(表格续下页.....)

表 18

Active mapping															
	HCon# 8 ⁴⁾	HCon#9	HCon#0	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P4.5	PWM0_10	PWM0_9_N			EXT_M UX[1]_0				TRIG_I N[17]	SG_TON E[1](2)			CAN0_1_RX		SCB3_SC L ⁶⁾
P4.6	PWM0_11	PWM0_10_N			EXT_M UX[1]_1				TRIG_I N[18]	SG_AMP L2			CAN1_0_TX		
P4.7	PWM0_12	PWM0_11_N			EXT_M UX[1]_2				TRIG_I N[19]	SG_TON E2			CAN1_0_RX		
P5.0	PWM0_3	PWM0_16_N							TRIG_I N[10]	CLK_FM_PUMP	SCB0_RX				FAULT_OUT_1
P5.1	PWM0_4	PWM0_3_N							TRIG_I N[11]		SCB0_TX	LIN1_TX	CXPI1_EN		FAULT_OUT_2
P5.2	PWM0_5	PWM0_4_N							TRIG_I N[12]		SCB0_TS	LIN1_RX	CXPI1_RX	SCB1_SDA	FAULT_OUT_3
P5.3	PWM0_6	PWM0_5_N							TRIG_I N[13]		SCB0_CTS	LIN1_EN	CXPI1_TX	SCB1_SCL	
P5.4	PWM0_7	PWM0_6_N			EXT_M UX[0]_0				TRIG_I N[14]	SG_AMP L[0](2)			CAN0_0_TX	SCB2_SDA	
P5.5	PWM0_8	PWM0_7_N			EXT_M UX[0]_1				TRIG_I N[15]	SG_TON E[0](2)			CAN0_0_RX	SCB2_SCL	

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P6.0	PWM0_13	PWM0_12_N			EXT_M UX[0]_ EN				TRIG_I N[20]	SG_AMP L[3](2)			CAN1_1 _TX
P6.1	PWM0_14	PWM0_13_N			EXT_M UX[1]_ EN				TRIG_I N[21]	SG_TON E[3](2)			CAN1_1 _RX
P6.2	PWM0_15	PWM0_14_N							TRIG_I N[22]	SG_AMP L[4](0)			
P6.3	PWM0_16	PWM0_15_N							TRIG_I N[23]	SG_TON E[4](0)			
P7.0	PWM0_M_0	PWM0_H_21_N							TRIG_I N[24]				
P7.1	PWM0_H_16	PWM0_M_0_N	TC0_H_2 1_TR						TRIG_I N[25]				
P7.2	PWM0_M_1	PWM0_H_16_N							TRIG_I N[26]				
P7.3	PWM0_H_17	PWM0_M_1_N	TC0_H_1 6_TR						TRIG_I N[27]				
P7.4	PWM0_M_2	PWM0_H_17_N							TRIG_I N[28]				
P7.5	PWM0_H_18	PWM0_M_2_N	TC0_H_1 7_TR						TRIG_I N[29]				
P7.6	PWM0_M_3	PWM0_H_18_N							TRIG_I N[30]				FAULT_ OUT_0

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping																
	HPin	HCon# 8 ⁴⁾	HCon#9	HCon#1 0	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# #20	HCon# 21	HCon#2 2	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon#2 7
	Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT# 8	ACT#9	ACT#10	ACT#11	ACT# 12	ACT#13	ACT#1 4	ACT#15
	P7.7	PWM0_H_19	PWM0_M_3_N	TC0_H_18_TR						TRIG_I_N[31]						FAULT_OUT_1
	P8.0	PWM0_M_4	PWM0_H_19_N							TRIG_I_N[32]						
	P8.1	PWM0_H_20	PWM0_M_4_N	TC0_H_19_TR						TRIG_I_N[33]	SG_MC_K[0]					
	P8.2	PWM0_M_5	PWM0_H_20_N							TRIG_I_N[34]	SG_AMP_L[0](3)					
	P8.3	PWM0_H_21	PWM0_M_5_N	TC0_H_20_TR						TRIG_I_N[35]	SG_TON_E[0](3)					
	P8.4	PWM0_M_6	PWM0_17_N							TRIG_I_N[36]	SG_AMP_L[1](3)					
	P8.5	PWM0_17	PWM0_M_6_N	TC0_22_TR						TRIG_I_N[37]	SG_TON_E[1](3)					
	P8.6	PWM0_M_7	PWM0_18_N							TRIG_I_N[38]	SG_AMP_L[2](3)					
	P8.7	PWM0_18	PWM0_M_7_N							TRIG_I_N[39]	SG_TON_E[2](3)					
	P9.0	PWM0_M_8	PWM0_19_N							TRIG_I_N[40]	SG_AMP_L3					
	P9.1	PWM0_19	PWM0_M_8_N							TRIG_I_N[41]	SG_TON_E3					

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping															
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1 0	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon#2 2	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon#2 7
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT# 8	ACT#9	ACT#10	ACT#11	ACT# 12	ACT#13	ACT#1 4	ACT#15
P9.2	PWM0_M_9	PWM0_20_N							TRIG_I N[42]	SG_AMP L[4](1)					
P9.3	PWM0_20	PWM0_M_9_N							TRIG_I N[43]	SG_TON E[4](1)			SCB8_S EL1		
P9.4	PWM0_M_10	PWM0_21_N							TRIG_I N[44]	SG_MC K[1]			SCB8_C LK	SCB8_RX DA ⁶⁾	SCB8_S
P9.5	PWM0_21	PWM0_M_10_N	TC0_20_TR						TRIG_I N[45]	SG_MC K[2]			SCB8_MOSI	SCB8_TX	SCB8_SC L ⁶⁾
P9.6	PWM0_M_11	PWM0_22_N							TRIG_I N[46]	SG_MC K[3]			SCB8_MISO	SCB8_RTS	
P9.7	PWM0_22	PWM0_M_11_N	TC0_21_TR						TRIG_I N[47]	SG_MC K[4]			SCB8_S ELO	SCB8_CTS	
P11.0				ETH_R EF_CL K								TTL_DSP1_DAT_A_A1[11]	SCB1_RX SDA ⁶⁾		SCB1_CL K
P11.1				ETH_R X_ER								TTL_DSP1_DAT_A_A0[11]	SCB1_TX SCL ⁶⁾		SCB1_M OSI

(表格续下页.....)

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping																				
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon#2	HCon# 23	HCon# #24	HCon# 25	HCon#	HCon# 26	HCon#2				
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#1	ACT#15					
P11.2				ETH_R XD_0								TTL_ DSP1 _DAT _A_A1[10]	SCB1_R TS			SCB1_MI SO				
P11.3				ETH_R XD_1								TTL_ DSP1 _DAT _A_A0[10]	SCB1_C TS			SCB1_SE L0				
P11.4				ETH_T XD_0									TTL_DS P1_CO NTROL[2]			SCB1_SE L1				
P11.5				ETH_T XD_1									SCB2_R X	SCB2_C SDA ⁶⁾ L K		SCB2_C L K				
P11.6				ETH_T X_CTL								TTL_ DSP1 _DAT _A_A1[9]	SCB2_T X	SCB2_ SCL ⁶⁾	SCB2_ OSI	SCB2_M OSI				
P11.7				ETH_R X_CTL								TTL_ DSP1 _DAT _A_A0[9]	SCB2_R TS			SCB2_MI SO				

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P12. 0				ETH_ MDC								TTL_ DSP1 _DAT _A_A1[8]	SCB2_C TS
P12. 1				ETH_ MDIO								TTL_ DSP1 _DAT _A_A0[8]	TTL_DS P0_CO NTROL[11]
P12. 2				ETH_T X_CLK	TDM_T X_MC K0	TDM_ RX_MC K1			PWM_LI NE1_P0	SG_TON E0		TTL_ DSP1 _CON TRO L[10]	TTL_DS P0_CO NTROL[10]
P12. 3				ETH_R X_CLK	TDM_T X_SC K0	TDM_ RX_SC K1			PWM_LI NE1_N0	SG_AMP L0		TTL_ DSP1 _CON TRO L[9]	TTL_DS P0_CO NTROL[9]
P12. 4				ETH_R XD_2	TDM_T X_FSY NC[0] (0)	TDM_ RX_FS YNC[1] (1)			PWM_LI NE2_P0	SG_TON E[1](0)		TTL_ DSP1 _CON TRO L[8]	TTL_DS P0_CO NTROL[8]

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能^{1), 2), 3)}

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P12. 5				ETH_R XD_3	TDM_T X_SD0	TDM_ RX_S D1			PWM_LI NE2_N0	SG_AMP L[1](0)		TTL_ DSP1 _CON TRO L[7]	TTL_DS P0_CO NTROL[7]
P12. 6				ETH_T XD_2	TDM_T X_MC K[1](0)	TDM_ RX_MC K[0](1)			PWM_LI NE1_P[1](0)	SG_TON E[2](0)		TTL_ DSP1 _CON TRO L[6]	TTL_DS P0_CO NTROL[6]
P12. 7				ETH_T XD_3	TDM_T X_SC K[1](0)	TDM_ RX_SC K[0](1)			PWM_LI NE1_N[1](0)	SG_AMP L[2](0)		TTL_ DSP1 _CON TRO L[5]	TTL_DS P0_CO NTROL[5]
P13. 0				ETH_T X_ER	TDM_T X_FSY NC[1] (0)	TDM_ RX_FS YNC[0] (1)			PWM_LI NE2_P[1](0)	SG_TON E[3](0)		TTL_ DSP1 _CON TRO L[4]	TTL_DS P0_CO NTROL[4]
P13. 1				ETH_T SU_TI MER_C MP_VA L	TDM_T X_SD[1](0)	TDM_ RX_S D[0](1)			PWM_LI NE2_N[1](0)	SG_AMP L[3](0)		TTL_ DSP1 _CON TRO L[3]	TTL_DS P0_CO NTROL[3]

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能^{1), 2), 3)}

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P13. 2							TTL_C AP0_D ATA[23]		PWM_M CK[0]			TTL_ DSP1 _DAT A_A1[11]	
P13. 3							TTL_C AP0_D ATA[22]		PWM_M CK[1]		TTL_CA P0_DA T A[26]	TTL_ DSP1 _DAT A_A0[11]	
P13. 4							TTL_C AP0_D ATA[21]				TTL_CA P0_DA T A[25]	TTL_ DSP1 _DAT A_A1[10]	
P13. 5							TTL_C AP0_D ATA[20]				TTL_CA P0_DA T A[24]	TTL_ DSP1 _DAT A_A0[10]	
P13. 6							TTL_C AP0_D ATA[19]				TTL_CA P0_DA T A[0]	TTL_ DSP1 _DAT A_A1[9]	

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13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P13. 7							TTL_C AP0_D ATA[18]]				TTL_CA P0_DA TA[1]]	TTL_ DSP1 _DAT A_A0[9]	
P14. 0	PWM0 _H_22	PWM0_H _31_N	TC0_H_3 0_TR				TTL_C AP0_D ATA[17]]				TTL_CA P0_DA TA[2]]	TTL_ DSP1 _DAT A_A1[8]	
P14. 1	PWM0 _H_23	PWM0_H _22_N	TC0_H_3 1_TR				TTL_C AP0_D ATA[16]]				TTL_CA P0_DA TA[3]]	TTL_ DSP1 _DAT A_A0[8]	
P14. 2	PWM0 _H_24	PWM0_H _23_N	TC0_H_2 2_TR			TDM_T X_MC K[2](0)	TTL_C AP0_D ATA[15]]		PWM_LI NE1_P[0](1)	SG_TON E[0](1)	TTL_CA P0_DA TA[4]]	TTL_ DSP1 _DAT A_A1[7]	TTL_DS P1_CO NTROL[2]
P14. 3	PWM0 _H_25	PWM0_H _24_N	TC0_H_2 3_TR			TDM_T X_SC K[2](0)	TTL_C AP0_D ATA[14]]		PWM_LI NE1_N[0](1)	SG_AMP L[0](1)	TTL_CA P0_DA TA[5]]	TTL_ DSP1 _DAT A_A0[7]	TRACE _DATA _0(0)

(表格续下页.....)

13 备用功能引脚分配
表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping															
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1 0	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon #20	HCon# 21	HCon#2 2	HCon# 23	HCon #24	HCon# 25	HCon# 26	HCon#2 7
Na me	ACT#0 5)	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT# 8	ACT#9	ACT#10	ACT#11	ACT# 12	ACT#13	ACT#1 4	ACT#15
P14. 4	PWM0 _H_26	PWM0_H _25_N	TC0_H_2 4_TR		TDM_T X_FSY NC[2] (0)	TDM_ RX_FS YNC[0] (0)	TTL_C AP0_D ATA[13]]		PWM_LI NE2_P[0](1)	SG_TON E1	TTL_CA P0_DA TA[6]	TTL_ DSP1 _DAT A_A1[6]		TRACE _DATA _1(0)	
P14. 5	PWM0 _H_27	PWM0_H _26_N	TC0_H_2 5_TR		TDM_T X_SD[2](0)	TDM_ RX_S D0	TTL_C AP0_D ATA[12]]		PWM_LI NE2_N[0](1)	SG_AMP L1	TTL_CA P0_DA TA[7]	TTL_ DSP1 _DAT A_A0[6]		TRACE _DATA _2(0)	
P14. 6	PWM0 _H_28	PWM0_H _27_N	TC0_H_2 6_TR		TDM_T X_MC K[3](0)	TDM_ RX_MC K[1](0)	TTL_C AP0_D ATA[11]]		PWM_LI NE1_P1	SG_TON E[2](1)	TTL_CA P0_DA TA[8]	TTL_ DSP1 _DAT A_A1[5]		TRACE _DATA _3(0)	
P14. 7	PWM0 _H_29	PWM0_H _28_N	TC0_H_2 7_TR		TDM_T X_SC K[3](0)	TDM_ RX_SC K[1](0)	TTL_C AP0_D ATA[10]]		PWM_LI NE1_N1	SG_AMP L[2](1)	TTL_CA P0_DA TA[9]	TTL_ DSP1 _DAT A_A0[5]			
P15. 0	PWM0 _H_30	PWM0_H _29_N	TC0_H_2 8_TR		TDM_T X_FSY NC[3] (0)	TDM_ RX_FS YNC[1] (0)	TTL_C AP0_C LK		PWM_LI NE2_P1	SG_TON E[3](1)		TTL_ DSP1 _DAT A_A1[4]			

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping															
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1 0	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon #20	HCon# 21	HCon#2 2	HCon# 23	HCon #24	HCon# 25	HCon# 26	HCon#2 7
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT# 8	ACT#9	ACT#10	ACT#11	ACT# 12	ACT#13	ACT#1 4	ACT#15
P15. 1	PWM0 _H_31	PWM0_H _30_N	TC0_H_2 9_TR		TDM_T X_SD[3](0)	TDM_ RX_S D[1](0)	TTL_C AP0_D ATA[10]		PWM_LI NE2_N1	SG_AMP L[3](1)	TTL_CA P0_DA TA[9]	TTL_ DSP1 _DAT A_A0[4]			
P15. 2	PWM0 _23	PWM0_29 _N	TC0_28_ TR				TTL_C AP0_D ATA[11]				TTL_CA P0_DA TA[8]	TTL_ DSP1 _DAT A_A1[3]	SCB3_C LK	SCB3_ RX	SCB3_S DA ⁶⁾
P15. 3	PWM0 _24	PWM0_30 _N	TC0_29_ TR				TTL_C AP0_D ATA[12]				TTL_CA P0_DA TA[7]	TTL_ DSP1 _DAT A_A0[3]	SCB3_ MOSI	SCB3_ TX	SCB3_SC L ⁶⁾
P15. 4	PWM0 _25	PWM0_23 _N	TC0_30_ TR				TTL_C AP0_D ATA[13]				TTL_CA P0_DA TA[6]	TTL_ DSP1 _DAT A_A1[2]	SCB3_ MISO	SCB3_ RTS	
P15. 5	PWM0 _26	PWM0_24 _N	TC0_23_ TR				TTL_C AP0_D ATA[14]				TTL_CA P0_DA TA[5]	TTL_ DSP1 _DAT A_A0[2]	SCB3_S ELO	SCB3_ CTS	

(表格续下页.....)

13 备用功能引脚分配
表 18 (续) 工作模式下的备用引脚功能^{1), 2), 3)}

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P15. 6	PWM0 _27	PWM0_25 _N	TC0_24_ TR				TTL_C AP0_D ATA[15]]				TTL_CA P0_DA TA[4]	TTL_ DSP1 _DAT A_A1[1]	SCB3_S EL1
P15. 7	PWM0 _28	PWM0_26 _N	TC0_25_ TR				TTL_C AP0_D ATA[16]]				TTL_CA P0_DA TA[3]	TTL_ DSP1 _DAT A_A0[1]	SCB4_C LK
P16. 0	PWM0 _29	PWM0_27 _N	TC0_26_ TR				TTL_C AP0_D ATA[17]]				TTL_CA P0_DA TA[2]	TTL_ DSP1 _DAT A_A1[0]	SCB4_ MOSI
P16. 1	PWM0 _30	PWM0_28 _N	TC0_27_ TR				TTL_C AP0_D ATA[18]]				TTL_CA P0_DA TA[1]	TTL_ DSP1 _DAT A_A0[0]	SCB4_ MISO
P16. 2	PWM0 _31	PWM0_37 _N	TC0_36_ TR			TDM_ RX_MC K[2](0)	TTL_C AP0_D ATA[19]]		PWM_LI NE1_P[0](2)	EXT_CLK	TTL_CA P0_DA TA[0]	TTL_ DSP1 _CLO CK	SCB4_S ELO
													SCB4_ RTS
													SCB4_ CTS

(表格续下页.....)

13 备用功能引脚分配
表 18 (续) 工作模式下的备用引脚功能^{1), 2), 3)}

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P16. 3	PWM0_32	PWM0_31_N	TC0_37_TR			TDM_RX_SC K[2](0)	TTL_C AP0_D ATA[20]		PWM_LI NE1_N[0](2)		TTL_CA P0_DA TA[24]	TTL_DSP1_CON TRO L[0]	SCB4_S EL1
P16. 4	PWM0_33	PWM0_32_N	TC0_31_TR			TDM_RX_FS YNC[2](0)	TTL_C AP0_D ATA[21]		PWM_LI NE2_P[0](2)	IO_CLK_HF[5]	TTL_CA P0_DA TA[25]	TTL_DSP1_CON TRO L[1]	TTL_DS P1_CO NTROL[2]
P16. 5	PWM0_34	PWM0_33_N	TC0_32_TR			TDM_RX_S D[2](0)	TTL_C AP0_D ATA[22]		PWM_LI NE2_N[0](2)		TTL_CA P0_DA TA[26]	SCB5_SEL 1	TTL_DS P1_CO NTROL[2]
P16. 6	PWM0_35	PWM0_34_N	TC0_33_TR		TDM_T X_MC K[2](1)	TDM_RX_MC K[3](0)	TTL_C AP0_D ATA[23]		PWM_LI NE1_P[1](2)			TTL_DSP1_CON TRO L[11]	SCB5_C LK
P16. 7	PWM0_36	PWM0_35_N	TC0_34_TR		TDM_T X_SC K[2](1)	TDM_RX_SC K[3](0)			PWM_LI NE1_N[1](2)			TTL_DSP1_CON TRO L[2]	SCB5_C MOSI
													SCB5_RX
													SCB5_TX
													SCB5_S DA ⁶⁾
													SCB5_S L ⁶⁾

(表格续下页.....)

表 18

Active mapping															
	HCon# 8 ⁴⁾	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P17.0	PWM0_37	PWM0_36_N	TC0_35_TR	ETH_MDC	TDM_TX_FSVNC[2](1)	TDM_RX_FSYNC[3](0)			PWM_LI_NE2_P[1](2)			TTL_DSP0_CON_TROL[1]	SCB5_MISO	SCB5_RTS	
P17.1				ETH_MDIO	TDM_TX_SD[2](1)	TDM_RX_S D[3](0)			PWM_LI_NE2_N[1](2)			TTL_DSP0_CON_TROL[0]	SCB5_EL0	SCB5_CTS	
P18.0								SCB9_CLK_X	SCB9_RX_X	SCB9_S DA ⁶⁾					SPIHB[0]_DATA4
P18.1								SCB9_MI_I	SCB9_TX_X	SCB9_SC L ⁶⁾					SPIHB[0]_DATA2
P18.2								SCB9_MI_O	SCB9_RX_TS						SPIHB[0]_DATA3
P18.3								SCB9_SEL_0	SCB9_C TS						SPIHB[0]_DATA5
P18.4								SCB10_CL_K	SCB10_RX	SCB10_S DA ⁶⁾					SPIHB[0]_DATA0

(表格续下页.....)

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

[illegible]

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 5)	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P20. 1				SPIHB[1]_DA TA2									
P20. 2				SPIHB[1]_DA TA3									
P20. 3				SPIHB[1]_DA TA5									TTL_DS P1_CO NTROL[2]
P20. 4				SPIHB[1]_DA TA0								TTL_ DSP1 _DAT _A_A1[11]	
P20. 5				SPIHB[1]_DA TA6								TTL_ DSP1 _DAT _A_A0[11]	
P20. 6				SPIHB[1]_DA TA1								TTL_ DSP1 _DAT _A_A1[10]	

(表格续下页.....)

13 备用功能引脚分配

表 18 (续) 工作模式下的备用引脚功能¹⁾, ²⁾, ³⁾

Active mapping													
Pin	HCon# 8 ⁴⁾	HCon#9	HCon#1	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#2	HCon#23	HCon#24	HCon#25
Na me	ACT#0 ⁵⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13
P20. 7				SPIHB[1]_DA TA7								TTL_ DSP1 _DAT _A_A0[10]	
P21. 0				SPIHB[1]_CL K								TTL_ DSP1 _DAT _A_A1[9]	
P21. 1				SPIHB[1]_RW DS								TTL_ DSP1 _DAT _A_A0[9]	
P21. 2				SPIHB[1]_SEL ECT0								TTL_ DSP1 _DAT _A_A1[8]	
P21. 3				SPIHB[1]_SEL ECT1								TTL_ DSP1 _DAT _A_A0[8]	

1) 所有在深度睡眠模式下可用的端口引脚功能在工作模式下也可用。

2) 有关使用的引脚多路复用器缩写更多信息, 可参见表 19。

13 备用功能引脚分配

- 3) 对于任何标有标识符 (n) 的函数, 交流时序仅在相应的组“n”内得到保证。
- 4) 高速 I/O 矩阵连接 (HCON) 基址可参见表 15。
- 5) 工作模式顺序 (ACT #0、ACT #1 等) 对配置备用功能没有任何影响; HSIOM 模块处理替换功能分配。
- 6) 参见表 39 “串行通信模块 (SCB) 规格”, 了解支持的 I/O 单元和 I2C 模式。

13 备用功能引脚分配
13.1 引脚功能
表 19 引脚功能描述

Sl No	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y ¹⁾	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N ¹⁾	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
9	SCBx_RX	SCB	UART Receive, x-SCB block
10	SCBx_TX	SCB	UART Transmit, x-SCB block
11	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
12	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
13	SCBx_SDA	SCB	I2C Data line, x-SCB block
14	SCBx_SCL	SCB	I2C Clock line, x-SCB block
15	SCBx_MISO	SCB	SPI Master Input Slave Output, x-SCB block
16	SCBx_MOSI	SCB	SPI Master Output Slave Input, x-SCB block
17	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
18	SCBx_SELy	SCB	SPI Slave Select, x-SCB block, y-select line
19	LINx_RX	LIN	LIN Receive line, x-LIN block
20	LINx_TX	LIN	LIN Transmit line, x-LIN block
21	LINx_EN	LIN	LIN Enable line, x-LIN block
22	CXPIx_RX	CXPI	CXPI Receive line, x-CXPI block
23	CXPIx_TX	CXPI	CXPI Transmit line, x-CXPI block
24	CXPIx_EN	CXPI	CXPI Enable line, x-CXPI block
25	CANx_y_TX	CAN FD	CAN Transmit line, x-CAN block, y-channel number
26	CANx_y_RX	CAN FD	CAN Receive line, x-CAN block, y-channel number
27	SPIHB_CLK	SMIF	SMIF interface clock

(表格续下页.....)

13 备用功能引脚分配
表 19 (续) 引脚功能描述

SI No	Pin	Module	Description
28	SPIHB_RWDS	SMIF	SMIF (SPI/xSPI) read-write-data-strobe line
29	SPIHB_SELx	SMIF	SMIF (SPI/xSPI) memory select line, x-select line number
30	SPIHB_DATAx	SMIF	SMIF (SPI/xSPI) memory data read and write line, x-0 to 7 data lines
31	ETHx_RX_ER	Ethernet	Ethernet receive error indication line, x-ETH module number
32	ETHx_ETH_TSU_TIM ER_CMP_VAL	Ethernet	Ethernet time stamp unit timer compare indication line, x-ETH module number
33	ETHx_MDIO	Ethernet	Ethernet management data input/output (MDIO) interface to PHY, x-ETH module number
34	ETHx_MDC	Ethernet	Ethernet management data clock (MDC) line, x-ETH module number
35	ETHx_REF_CLK	Ethernet	Ethernet reference clock line, x-ETH module number
36	ETHx_TX_CTL	Ethernet	Ethernet transmit control line, x-ETH module number
37	ETHx_TX_ER	Ethernet	Ethernet transmit error indication line, x-ETH module number
38	ETHx_TX_CLK	Ethernet	Ethernet transmit clock line, x-ETH module number
39	ETHx_TXD_y	Ethernet	Ethernet transmit data line, x-ETH module number, y-transmit channel number
40	ETHx_RXD_y	Ethernet	Ethernet receive data line, x-ETH module number, y-receive channel number
41	ETHx_RX_CTL	Ethernet	Ethernet receive control line, x-ETH module number
42	ETHx_RX_CLK	Ethernet	Ethernet receive clock line, x-ETH module number
43	CAL_SUP_NZ	System	ETAS Calibration support line
44	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
45	TRACE_DATA_x	SRSS	Trace dataout line x-0 to 3
46	TRACE_CLOCK	SRSS	Trace clock line
47	RTC_CAL	SRSS RTC	RTC calibration clock input
48	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
49	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
50	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
51	SWJ_SWDIO_TMS	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/Output)
52	SWJ_SWDOE_TDI	SRSS	JTAG Test data input
53	HIBERNATE_WAKEUP P[x]	SRSS	Hibernate wakeup line x-0 to N (Check Table 16)
54	EXT_CLK	SRSS	External clock input
55	IO_CLK_HF[5]	SRSS	CLK_HF5 clock output
56	PMIC_EN	SRSS PMIC	PMIC control line, Enable output for PMIC

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13 备用功能引脚分配
表 19 (续) 引脚功能描述

SI No	Pin	Module	Description
57	PMIC_STATUS	SRSS PMIC	PMIC status line, Power good input from PMIC
58	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
59	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
60	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
61	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
62	PWM_LINEx_N[y]	PCM PWM	Audio PWM complementary output line, x-PWM module instance
63	PWM_LINEx_P[y]	PCM PWM	Audio PWM output line, x-PWM module instance
64	PWM_MCK[x]	PCM PWM	Audio PWM master clock input, x-PWM module instance
65	SG_AMPL[x]	SG	Sound generator (SG) amplitude output, x-SG module number
66	SG_MCK[x]	SG	Sound generator (SG) master clock input, x-SG module number
67	SG_TONE[x]	SG	Sound generator (SG) tone output, x-SG module number
68	TDM_RX_FSYNC[x]	TDM	TDM receive frame sync, x-TDM module number
69	TDM_RX_MCK[x]	TDM	TDM receive master clock input, x-TDM module number
70	TDM_RX_SCK[x]	TDM	TDM receive bit clock, x-TDM module number
71	TDM_RX_SD[x]	TDM	TDM receive serial data, x-TDM module number
72	TDM_TX_FSYNC[x]	TDM	TDM transmit frame sync, x-TDM module number
73	TDM_TX_MCK[x]	TDM	TDM transmit master clock input, x-TDM module number
74	TDM_TX_SCK[x]	TDM	TDM transmit bit clock, x-TDM module number
75	TDM_TX_SD[x]	TDM	TDM transmit serial data, x-TDM module number
76	TTL_CAPx_CLK	VIDEO	Capture clock, x-capture module number
77	TTL_CAPx_DATA[y]	VIDEO	Capture data lines, x-capture module number, y- (0-26) data line
78	TTL_DSPx_CONTRO L[y]	VIDEO	Display control line, x-display number, y-0/invalid, 1/vertical sync signal, 2/display enable (DE)
79	TTL_DSPx_CLOCK	VIDEO	Display clock line (PCLK), x-display number
80	TTL_DSPx_DATA_A0[y]	VIDEO	Display data (A0/1 used in pairs), x-display number, y- (0-11) color data
81	TTL_DSPx_DATA_A1[y]	VIDEO	Display data (A0/1 used in pairs), x-display number, y- (0-11) color data
82	DAC_MCK	AUDIODA C	DAC external master clock input
83	DAC_AOUTS_x	AUDIODA C	DAC output signal, x-left (L) or right (R) signal

(表格续下页.....)

13 备用功能引脚分配
表 19 (续) 引脚功能描述

SI No	Pin	Module	Description
84	DAC_COM_x	AUDIODAC	DAC common signal, x-left (L) or right (R) signal
85	MIPI_DPx	VIDEO	MIPI CSI-2 positive Data-Y input signal
86	MIPI_DNx	VIDEO	MIPI CSI-2 negative Data-Y input signal
87	MIPI_CKP	VIDEO	MIPI CSI-2 positive clock input signal
88	MIPI_CKN	VIDEO	MIPI CSI-2 negative clock input signal
89	MIPI_REXT	VIDEO	MIPI CSI-2 external reference resistor pin for auto-calibration
90	FPDx_TyP	VIDEO	FPD-link positive transmit signal, x-FPD instance, y-(0-3/A-C) output signal
91	FPDx_TyN	VIDEO	FPD-link negative transmit signal, x-FPD instance, y-(0-3/A-C) output signal
92	FPDx_TCLKP	VIDEO	FPD-link positive clock signal, x-FPD instance
93	FPDx_TCLKN	VIDEO	FPD-link negative clock signal, x-FPD instance

1) 该引脚/线路用于直接连接指针式仪器的步进电机线圈。

14 中断和唤醒分配

14 中断和唤醒分配

表 20 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS Fault Structure #0 Interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS Fault Structure #1 Interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS Fault Structure #2 Interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS Fault Structure #3 Interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain Interrupt
13	srss_interrupt_mcwtdt_0_IRQn	DeepSleep	Multi Counter Watchdog Timer#0 interrupt
14	srss_interrupt_mcwtdt_1_IRQn	DeepSleep	Multi Counter Watchdog Timer#1 interrupt
17	srss_interrupt_wdt_IRQn	DeepSleep	Hardware Watchdog Timer interrupt
18	srss_interrupt_IRQn	DeepSleep	Other combined Interrupts for SRSS (LVD, CLKCAL)
19	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event gen DeepSleep domain interrupt
20	scb_0_interrupt_IRQn	DeepSleep	SCB0 interrupt (DeepSleep capable)
22	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Supply (VDDIO, VDDA_ADC, VDDD) state change Interrupt
23	ioss_interrupt_gpio_dpslp_IRQn	DeepSleep	Consolidated Interrupt for GPIO*, All Ports
24	ioss_interrupts_gpio_dpslp_0_IRQn	DeepSleep	GPIO_STD Port #0 Interrupt
25	ioss_interrupts_gpio_dpslp_1_IRQn	DeepSleep	GPIO_STD Port #1 Interrupt
26	ioss_interrupts_gpio_dpslp_2_IRQn	DeepSleep	GPIO_STD Port #2 Interrupt
27	ioss_interrupts_gpio_dpslp_3_IRQn	DeepSleep	GPIO_STD Port #3 Interrupt
28	ioss_interrupts_gpio_dpslp_4_IRQn	DeepSleep	GPIO_STD Port #4 Interrupt

(表格续下页.....)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
29	ioss_interrupts_gpio_dpslp_5_I RQn	DeepSleep	GPIO_STD Port #5 Interrupt
30	ioss_interrupts_gpio_dpslp_6_I RQn	DeepSleep	GPIO_STD Port #6 Interrupt
31	ioss_interrupts_gpio_dpslp_7_I RQn	DeepSleep	GPIO_SMC Port #7 Interrupt
32	ioss_interrupts_gpio_dpslp_8_I RQn	DeepSleep	GPIO_SMC Port #8 Interrupt
33	ioss_interrupts_gpio_dpslp_9_I RQn	DeepSleep	GPIO_SMC Port #9 Interrupt
50	ioss_interrupt_gpio_act_IRQn	Active	Consolidated Interrupt for HSIO*, All Ports
52	ioss_interrupts_gpio_act_11_IR Qn	Active	HSIO_STDLN Port Interrupt #11 Interrupt
53	ioss_interrupts_gpio_act_12_IR Qn	Active	HSIO_STDLN Port Interrupt #12 Interrupt
54	ioss_interrupts_gpio_act_13_IR Qn	Active	HSIO_STDLN Port Interrupt #13 Interrupt
55	ioss_interrupts_gpio_act_14_IR Qn	Active	HSIO_STDLN Port Interrupt #14 Interrupt
56	ioss_interrupts_gpio_act_15_IR Qn	Active	HSIO_STDLN Port Interrupt #15 Interrupt
57	ioss_interrupts_gpio_act_16_IR Qn	Active	HSIO_STDLN Port Interrupt #16 Interrupt
58	ioss_interrupts_gpio_act_17_IR Qn	Active	HSIO_STDLN Port Interrupt #17 Interrupt
59	ioss_interrupts_gpio_act_18_IR Qn	Active	HSIO_STDLN Port Interrupt #18 Interrupt
60	ioss_interrupts_gpio_act_19_IR Qn	Active	HSIO_STDLN Port Interrupt #19 Interrupt
61	ioss_interrupts_gpio_act_20_IR Qn	Active	HSIO_STDLN Port Interrupt #20 Interrupt
62	ioss_interrupts_gpio_act_21_IR Qn	Active	HSIO_STDLN Port Interrupt #21 Interrupt
70	cpuss_interrupt_crypto_IRQn	Active	Crypto Accelerator Interrupt
71	cpuss_interrupt_fm_IRQn	Active	FLASH Macro Interrupt
72	cpuss_interrupts_cm7_0_fp_IR Qn	Active	CM7_0 Floating Point operation fault

(表格续下页.....)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
74	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross Trigger Interface) #0
75	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI #1
76	cpuss_interrupts_cm7_0_cti_0_IRQn	Active	CM7_0 CTI #0
77	cpuss_interrupts_cm7_0_cti_1_IRQn	Active	CM7_0 CTI #1
80	evtgen_0_interrupt_IRQn	Active	Event gen Active domain interrupt
81	smif_0_interrupt_IRQn	Active	SMIF #0 (QSPI) interrupt
82	smif_1_interrupt_IRQn	Active	SMIF #1 (QSPI) interrupt
83	eth_0_interrupt_eth_0_IRQn	Active	Ethernet #0 priority queue[0]
84	eth_0_interrupt_eth_1_IRQn	Active	Ethernet #0 priority queue[1]
85	eth_0_interrupt_eth_2_IRQn	Active	Ethernet #0 priority queue[2]
86	CAN FD_0_interrupt0_IRQn	Active	CAN0, Consolidated interrupt #0 for all channels
87	CAN FD_0_interrupt1_IRQn	Active	CAN0, Consolidated interrupt #1 for all channels
88	CAN FD_1_interrupt0_IRQn	Active	CAN1, Consolidated interrupt #0 for all channels
89	CAN FD_1_interrupt1_IRQn	Active	CAN1, Consolidated interrupt #1 for all channels
90	CAN FD_0_interrupts0_0_IRQn	Active	CAN0, Interrupt #0, Channel #0
91	CAN FD_0_interrupts0_1_IRQn	Active	CAN0, Interrupt #0, Channel #1
96	CAN FD_0_interrupts1_0_IRQn	Active	CAN0, Interrupt #1, Channel #0
97	CAN FD_0_interrupts1_1_IRQn	Active	CAN0, Interrupt #1, Channel #1
102	CAN FD_1_interrupts0_0_IRQn	Active	CAN1, Interrupt #0, Channel #0
103	CAN FD_1_interrupts0_1_IRQn	Active	CAN1, Interrupt #0, Channel #1
108	CAN FD_1_interrupts1_0_IRQn	Active	CAN1, Interrupt #1, Channel #0
109	CAN FD_1_interrupts1_1_IRQn	Active	CAN1, Interrupt #1, Channel #1
114	lin_0_interrupts_0_IRQn	Active	LIN0 Channel #0 Interrupt
115	lin_0_interrupts_1_IRQn	Active	LIN0 Channel #1 Interrupt
130	cxpi_0_interrupts_0_IRQn	Active	CXPIO Channel #0 Interrupt
131	cxpi_0_interrupts_1_IRQn	Active	CXPIO Channel #1 Interrupt
135	scb_1_interrupt_IRQn	Active	SCB1 Interrupt
136	scb_2_interrupt_IRQn	Active	SCB2 Interrupt
137	scb_3_interrupt_IRQn	Active	SCB3 Interrupt
138	scb_4_interrupt_IRQn	Active	SCB4 Interrupt

(表格续下页.....)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
139	scb_5_interrupt_IRQn	Active	SCB5 Interrupt
140	scb_6_interrupt_IRQn	Active	SCB6 Interrupt
141	scb_7_interrupt_IRQn	Active	SCB7 Interrupt
142	scb_8_interrupt_IRQn	Active	SCB8 Interrupt
143	scb_9_interrupt_IRQn	Active	SCB9 Interrupt
144	scb_10_interrupt_IRQn	Active	SCB10 Interrupt
145	scb_11_interrupt_IRQn	Active	SCB11 Interrupt
150	videoss_0_interrupt_gfx2d_IRQn	Active	GFX2D Interrupt
151	videoss_0_interrupt_mipicsi_IRQn	Active	MIPICSI Interrupt
152	videoss_0_interrupt_videoio0_IRQn	Active	VIDEOSS I/O Interrupt #0
153	videoss_0_interrupt_videoio1_IRQn	Active	VIDEOSS I/O Interrupt #1
154	videoss_0_interrupt_videoio0_safety	Active	VIDEOSS I/O Safety Interrupt #0
155	videoss_0_interrupt_videoio1_safety	Active	VIDEOSS I/O Safety Interrupt #1
160	pass_0_interrupts_sar_0_IRQn	Active	SAR0, Logical Channel #0 Interrupt
161	pass_0_interrupts_sar_1_IRQn	Active	SAR0, Logical Channel #1 Interrupt
162	pass_0_interrupts_sar_2_IRQn	Active	SAR0, Logical Channel #2 Interrupt
163	pass_0_interrupts_sar_3_IRQn	Active	SAR0, Logical Channel #3 Interrupt
164	pass_0_interrupts_sar_4_IRQn	Active	SAR0, Logical Channel #4 Interrupt
165	pass_0_interrupts_sar_5_IRQn	Active	SAR0, Logical Channel #5 Interrupt
166	pass_0_interrupts_sar_6_IRQn	Active	SAR0, Logical Channel #6 Interrupt
167	pass_0_interrupts_sar_7_IRQn	Active	SAR0, Logical Channel #7 Interrupt
168	pass_0_interrupts_sar_8_IRQn	Active	SAR0, Logical Channel #8 Interrupt
169	pass_0_interrupts_sar_9_IRQn	Active	SAR0, Logical Channel #9 Interrupt
170	pass_0_interrupts_sar_10_IRQn	Active	SAR0, Logical Channel #10 Interrupt
171	pass_0_interrupts_sar_11_IRQn	Active	SAR0, Logical Channel #11 Interrupt
172	pass_0_interrupts_sar_12_IRQn	Active	SAR0, Logical Channel #12 Interrupt
173	pass_0_interrupts_sar_13_IRQn	Active	SAR0, Logical Channel #13 Interrupt
174	pass_0_interrupts_sar_14_IRQn	Active	SAR0, Logical Channel #14 Interrupt
175	pass_0_interrupts_sar_15_IRQn	Active	SAR0, Logical Channel #15 Interrupt

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14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
176	pass_0_interrupts_sar_16_IRQn	Active	SAR0, Logical Channel #16 Interrupt
177	pass_0_interrupts_sar_17_IRQn	Active	SAR0, Logical Channel #17 Interrupt
178	pass_0_interrupts_sar_18_IRQn	Active	SAR0, Logical Channel #18 Interrupt
179	pass_0_interrupts_sar_19_IRQn	Active	SAR0, Logical Channel #19 Interrupt
180	pass_0_interrupts_sar_20_IRQn	Active	SAR0, Logical Channel #20 Interrupt
181	pass_0_interrupts_sar_21_IRQn	Active	SAR0, Logical Channel #21 Interrupt
182	pass_0_interrupts_sar_22_IRQn	Active	SAR0, Logical Channel #22 Interrupt
183	pass_0_interrupts_sar_23_IRQn	Active	SAR0, Logical Channel #23 Interrupt
184	pass_0_interrupts_sar_24_IRQn	Active	SAR0, Logical Channel #24 Interrupt
185	pass_0_interrupts_sar_25_IRQn	Active	SAR0, Logical Channel #25 Interrupt
186	pass_0_interrupts_sar_26_IRQn	Active	SAR0, Logical Channel #26 Interrupt
187	pass_0_interrupts_sar_27_IRQn	Active	SAR0, Logical Channel #27 Interrupt
188	pass_0_interrupts_sar_28_IRQn	Active	SAR0, Logical Channel #28 Interrupt
189	pass_0_interrupts_sar_29_IRQn	Active	SAR0, Logical Channel #29 Interrupt
190	pass_0_interrupts_sar_30_IRQn	Active	SAR0, Logical Channel #30 Interrupt
191	pass_0_interrupts_sar_31_IRQn	Active	SAR0, Logical Channel #31 Interrupt
280	axi_dmac_0_interrupts_0_IRQn	Active	AXI M-DMA1, Channel#0 Interrupt
281	axi_dmac_0_interrupts_1_IRQn	Active	AXI M-DMA1, Channel#1 Interrupt
282	axi_dmac_0_interrupts_2_IRQn	Active	AXI M-DMA1, Channel#2 Interrupt
283	axi_dmac_0_interrupts_3_IRQn	Active	AXI M-DMA1, Channel#3 Interrupt
288	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA0, Channel #0 Interrupt
289	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA0, Channel #1 Interrupt
290	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA0, Channel #2 Interrupt
291	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA0, Channel #3 Interrupt
292	cpuss_interrupts_dmac_4_IRQn	Active	CPUSS M-DMA0, Channel #4 Interrupt
293	cpuss_interrupts_dmac_5_IRQn	Active	CPUSS M-DMA0, Channel #5 Interrupt
294	cpuss_interrupts_dmac_6_IRQn	Active	CPUSS M-DMA0, Channel #6 Interrupt
295	cpuss_interrupts_dmac_7_IRQn	Active	CPUSS M-DMA0, Channel #7 Interrupt
296	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA0, Channel #0 Interrupt
297	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA0, Channel #1 Interrupt
298	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA0, Channel #2 Interrupt
299	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA0, Channel #3 Interrupt
300	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA0, Channel #4 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
301	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA0, Channel #5 Interrupt
302	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA0, Channel #6 Interrupt
303	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA0, Channel #7 Interrupt
304	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA0, Channel #8 Interrupt
305	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA0, Channel #9 Interrupt
306	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA0, Channel #10 Interrupt
307	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA0, Channel #11 Interrupt
308	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA0, Channel #12 Interrupt
309	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA0, Channel #13 Interrupt
310	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA0, Channel #14 Interrupt
311	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA0, Channel #15 Interrupt
312	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA0, Channel #16 Interrupt
313	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA0, Channel #17 Interrupt
314	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA0, Channel #18 Interrupt
315	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA0, Channel #19 Interrupt
316	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA0, Channel #20 Interrupt
317	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA0, Channel #21 Interrupt
318	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA0, Channel #22 Interrupt
319	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA0, Channel #23 Interrupt
320	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA0, Channel #24 Interrupt
321	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA0, Channel #25 Interrupt
322	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA0, Channel #26 Interrupt
323	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA0, Channel #27 Interrupt
324	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA0, Channel #28 Interrupt
325	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA0, Channel #29 Interrupt
326	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA0, Channel #30 Interrupt
327	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA0, Channel #31 Interrupt
328	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA0, Channel #32 Interrupt
329	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA0, Channel #33 Interrupt
330	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA0, Channel #34 Interrupt
331	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA0, Channel #35 Interrupt
332	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA0, Channel #36 Interrupt
333	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA0, Channel #37 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
334	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA0, Channel #38 Interrupt
335	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA0, Channel #39 Interrupt
336	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA0, Channel #40 Interrupt
337	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA0, Channel #41 Interrupt
338	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA0, Channel #42 Interrupt
339	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA0, Channel #43 Interrupt
340	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA0, Channel #44 Interrupt
341	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA0, Channel #45 Interrupt
342	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA0, Channel #46 Interrupt
343	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA0, Channel #47 Interrupt
344	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA0, Channel #48 Interrupt
345	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA0, Channel #49 Interrupt
346	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA0, Channel #50 Interrupt
347	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA0, Channel #51 Interrupt
348	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA0, Channel #52 Interrupt
349	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA0, Channel #53 Interrupt
350	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA0, Channel #54 Interrupt
351	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA0, Channel #55 Interrupt
352	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA0, Channel #56 Interrupt
353	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA0, Channel #57 Interrupt
354	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA0, Channel #58 Interrupt
355	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA0, Channel #59 Interrupt
356	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA0, Channel #60 Interrupt
357	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA0, Channel #61 Interrupt
358	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA0, Channel #62 Interrupt
359	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA0, Channel #63 Interrupt
360	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA0, Channel #64 Interrupt
361	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA0, Channel #65 Interrupt
362	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA0, Channel #66 Interrupt
363	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA0, Channel #67 Interrupt
364	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA0, Channel #68 Interrupt
365	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA0, Channel #69 Interrupt
366	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA0, Channel #70 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
367	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA0, Channel #71 Interrupt
368	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA0, Channel #72 Interrupt
369	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA0, Channel #73 Interrupt
370	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA0, Channel #74 Interrupt
371	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA0, Channel #75 Interrupt
424	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA1, Channel #0 Interrupt
425	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA1, Channel #1 Interrupt
426	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA1, Channel #2 Interrupt
427	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA1, Channel #3 Interrupt
428	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA1, Channel #4 Interrupt
429	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA1, Channel #5 Interrupt
430	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA1, Channel #6 Interrupt
431	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA1, Channel #7 Interrupt
432	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA1, Channel #8 Interrupt
433	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA1, Channel #9 Interrupt
434	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA1, Channel #10 Interrupt
435	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA1, Channel #11 Interrupt
436	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA1, Channel #12 Interrupt
437	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA1, Channel #13 Interrupt
438	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA1, Channel #14 Interrupt
439	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA1, Channel #15 Interrupt
440	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA1, Channel #16 Interrupt
441	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA1, Channel #17 Interrupt
442	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA1, Channel #18 Interrupt
443	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA1, Channel #19 Interrupt
444	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA1, Channel #20 Interrupt
445	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA1, Channel #21 Interrupt
446	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA1, Channel #22 Interrupt
447	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA1, Channel #23 Interrupt
448	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA1, Channel #24 Interrupt
449	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA1, Channel #25 Interrupt
450	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA1, Channel #26 Interrupt
451	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA1, Channel #27 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
452	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA1, Channel #28 Interrupt
453	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA1, Channel #29 Interrupt
454	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA1, Channel #30 Interrupt
455	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA1, Channel #31 Interrupt
456	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA1, Channel #32 Interrupt
457	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA1, Channel #33 Interrupt
458	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA1, Channel #34 Interrupt
459	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA1, Channel #35 Interrupt
460	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA1, Channel #36 Interrupt
461	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA1, Channel #37 Interrupt
462	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA1, Channel #38 Interrupt
463	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA1, Channel #39 Interrupt
464	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA1, Channel #40 Interrupt
465	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA1, Channel #41 Interrupt
466	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA1, Channel #42 Interrupt
467	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA1, Channel #43 Interrupt
468	cpuss_interrupts_dw1_44_IRQn	Active	CPUSS P-DMA1, Channel #44 Interrupt
469	cpuss_interrupts_dw1_45_IRQn	Active	CPUSS P-DMA1, Channel #45 Interrupt
470	cpuss_interrupts_dw1_46_IRQn	Active	CPUSS P-DMA1, Channel #46 Interrupt
471	cpuss_interrupts_dw1_47_IRQn	Active	CPUSS P-DMA1, Channel #47 Interrupt
472	cpuss_interrupts_dw1_48_IRQn	Active	CPUSS P-DMA1, Channel #48 Interrupt
473	cpuss_interrupts_dw1_49_IRQn	Active	CPUSS P-DMA1, Channel #49 Interrupt
474	cpuss_interrupts_dw1_50_IRQn	Active	CPUSS P-DMA1, Channel #50 Interrupt
475	cpuss_interrupts_dw1_51_IRQn	Active	CPUSS P-DMA1, Channel #51 Interrupt
476	cpuss_interrupts_dw1_52_IRQn	Active	CPUSS P-DMA1, Channel #52 Interrupt
477	cpuss_interrupts_dw1_53_IRQn	Active	CPUSS P-DMA1, Channel #53 Interrupt
478	cpuss_interrupts_dw1_54_IRQn	Active	CPUSS P-DMA1, Channel #54 Interrupt
479	cpuss_interrupts_dw1_55_IRQn	Active	CPUSS P-DMA1, Channel #55 Interrupt
480	cpuss_interrupts_dw1_56_IRQn	Active	CPUSS P-DMA1, Channel #56 Interrupt
481	cpuss_interrupts_dw1_57_IRQn	Active	CPUSS P-DMA1, Channel #57 Interrupt
482	cpuss_interrupts_dw1_58_IRQn	Active	CPUSS P-DMA1, Channel #58 Interrupt
483	cpuss_interrupts_dw1_59_IRQn	Active	CPUSS P-DMA1, Channel #59 Interrupt
484	cpuss_interrupts_dw1_60_IRQn	Active	CPUSS P-DMA1, Channel #60 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
485	cpuss_interrupts_dw1_61_IRQn	Active	CPUSS P-DMA1, Channel #61 Interrupt
486	cpuss_interrupts_dw1_62_IRQn	Active	CPUSS P-DMA1, Channel #62 Interrupt
487	cpuss_interrupts_dw1_63_IRQn	Active	CPUSS P-DMA1, Channel #63 Interrupt
488	cpuss_interrupts_dw1_64_IRQn	Active	CPUSS P-DMA1, Channel #64 Interrupt
489	cpuss_interrupts_dw1_65_IRQn	Active	CPUSS P-DMA1, Channel #65 Interrupt
490	cpuss_interrupts_dw1_66_IRQn	Active	CPUSS P-DMA1, Channel #66 Interrupt
491	cpuss_interrupts_dw1_67_IRQn	Active	CPUSS P-DMA1, Channel #67 Interrupt
492	cpuss_interrupts_dw1_68_IRQn	Active	CPUSS P-DMA1, Channel #68 Interrupt
493	cpuss_interrupts_dw1_69_IRQn	Active	CPUSS P-DMA1, Channel #69 Interrupt
494	cpuss_interrupts_dw1_70_IRQn	Active	CPUSS P-DMA1, Channel #70 Interrupt
495	cpuss_interrupts_dw1_71_IRQn	Active	CPUSS P-DMA1, Channel #71 Interrupt
496	cpuss_interrupts_dw1_72_IRQn	Active	CPUSS P-DMA1, Channel #72 Interrupt
497	cpuss_interrupts_dw1_73_IRQn	Active	CPUSS P-DMA1, Channel #73 Interrupt
498	cpuss_interrupts_dw1_74_IRQn	Active	CPUSS P-DMA1, Channel #74 Interrupt
499	cpuss_interrupts_dw1_75_IRQn	Active	CPUSS P-DMA1, Channel #75 Interrupt
500	cpuss_interrupts_dw1_76_IRQn	Active	CPUSS P-DMA1, Channel #76 Interrupt
501	cpuss_interrupts_dw1_77_IRQn	Active	CPUSS P-DMA1, Channel #77 Interrupt
502	cpuss_interrupts_dw1_78_IRQn	Active	CPUSS P-DMA1, Channel #78 Interrupt
503	cpuss_interrupts_dw1_79_IRQn	Active	CPUSS P-DMA1, Channel #79 Interrupt
504	cpuss_interrupts_dw1_80_IRQn	Active	CPUSS P-DMA1, Channel #80 Interrupt
505	cpuss_interrupts_dw1_81_IRQn	Active	CPUSS P-DMA1, Channel #81 Interrupt
506	cpuss_interrupts_dw1_82_IRQn	Active	CPUSS P-DMA1, Channel #82 Interrupt
507	cpuss_interrupts_dw1_83_IRQn	Active	CPUSS P-DMA1, Channel #83 Interrupt
552	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 Group #0, Counter #0 Interrupt
553	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 Group #0, Counter #1 Interrupt
554	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 Group #0, Counter #2 Interrupt
555	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 Group #0, Counter #3 Interrupt
556	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 Group #0, Counter #4 Interrupt
557	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 Group #0, Counter #5 Interrupt
558	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 Group #0, Counter #6 Interrupt
559	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 Group #0, Counter #7 Interrupt
560	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 Group #0, Counter #8 Interrupt
561	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 Group #0, Counter #9 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
562	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 Group #0, Counter #10 Interrupt
563	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 Group #0, Counter #11 Interrupt
564	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 Group #0, Counter #12 Interrupt
565	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 Group #0, Counter #13 Interrupt
566	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 Group #0, Counter #14 Interrupt
567	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 Group #0, Counter #15 Interrupt
568	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 Group #0, Counter #16 Interrupt
569	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 Group #0, Counter #17 Interrupt
570	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 Group #0, Counter #18 Interrupt
571	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 Group #0, Counter #19 Interrupt
572	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 Group #0, Counter #20 Interrupt
573	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 Group #0, Counter #21 Interrupt
574	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 Group #0, Counter #22 Interrupt
575	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 Group #0, Counter #23 Interrupt
576	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 Group #0, Counter #24 Interrupt
577	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 Group #0, Counter #25 Interrupt
578	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 Group #0, Counter #26 Interrupt
579	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 Group #0, Counter #27 Interrupt
580	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 Group #0, Counter #28 Interrupt
581	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 Group #0, Counter #29 Interrupt
582	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 Group #0, Counter #30 Interrupt
583	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 Group #0, Counter #31 Interrupt
584	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 Group #0, Counter #32 Interrupt
585	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 Group #0, Counter #33 Interrupt
586	tcpwm_0_interrupts_34_IRQn	Active	TCPWM0 Group #0, Counter #34 Interrupt
587	tcpwm_0_interrupts_35_IRQn	Active	TCPWM0 Group #0, Counter #35 Interrupt
588	tcpwm_0_interrupts_36_IRQn	Active	TCPWM0 Group #0, Counter #36 Interrupt
589	tcpwm_0_interrupts_37_IRQn	Active	TCPWM0 Group #0, Counter #37 Interrupt
616	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 Group #1, Counter #0 Interrupt
617	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 Group #1, Counter #1 Interrupt
618	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 Group #1, Counter #2 Interrupt
619	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 Group #1, Counter #3 Interrupt
620	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 Group #1, Counter #4 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
621	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 Group #1, Counter #5 Interrupt
622	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 Group #1, Counter #6 Interrupt
623	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 Group #1, Counter #7 Interrupt
624	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 Group #1, Counter #8 Interrupt
625	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 Group #1, Counter #9 Interrupt
626	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 Group #1, Counter #10 Interrupt
627	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 Group #1, Counter #11 Interrupt
680	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 Group #2, Counter #0 Interrupt
681	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 Group #2, Counter #1 Interrupt
682	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 Group #2, Counter #2 Interrupt
683	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 Group #2, Counter #3 Interrupt
684	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 Group #2, Counter #4 Interrupt
685	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 Group #2, Counter #5 Interrupt
686	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 Group #2, Counter #6 Interrupt
687	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 Group #2, Counter #7 Interrupt
688	tcpwm_0_interrupts_520_IRQn	Active	TCPWM0 Group #2, Counter #8 Interrupt
689	tcpwm_0_interrupts_521_IRQn	Active	TCPWM0 Group #2, Counter #9 Interrupt
690	tcpwm_0_interrupts_522_IRQn	Active	TCPWM0 Group #2, Counter #10 Interrupt
691	tcpwm_0_interrupts_523_IRQn	Active	TCPWM0 Group #2, Counter #11 Interrupt
692	tcpwm_0_interrupts_524_IRQn	Active	TCPWM0 Group #2, Counter #12 Interrupt
693	tcpwm_0_interrupts_525_IRQn	Active	TCPWM0 Group #2, Counter #13 Interrupt
694	tcpwm_0_interrupts_526_IRQn	Active	TCPWM0 Group #2, Counter #14 Interrupt
695	tcpwm_0_interrupts_527_IRQn	Active	TCPWM0 Group #2, Counter #15 Interrupt
696	tcpwm_0_interrupts_528_IRQn	Active	TCPWM0 Group #2, Counter #16 Interrupt
697	tcpwm_0_interrupts_529_IRQn	Active	TCPWM0 Group #2, Counter #17 Interrupt
698	tcpwm_0_interrupts_530_IRQn	Active	TCPWM0 Group #2, Counter #18 Interrupt
699	tcpwm_0_interrupts_531_IRQn	Active	TCPWM0 Group #2, Counter #19 Interrupt
700	tcpwm_0_interrupts_532_IRQn	Active	TCPWM0 Group #2, Counter #20 Interrupt
701	tcpwm_0_interrupts_533_IRQn	Active	TCPWM0 Group #2, Counter #21 Interrupt
702	tcpwm_0_interrupts_534_IRQn	Active	TCPWM0 Group #2, Counter #22 Interrupt
703	tcpwm_0_interrupts_535_IRQn	Active	TCPWM0 Group #2, Counter #23 Interrupt
704	tcpwm_0_interrupts_536_IRQn	Active	TCPWM0 Group #2, Counter #24 Interrupt
705	tcpwm_0_interrupts_537_IRQn	Active	TCPWM0 Group #2, Counter #25 Interrupt

(表格续下页...)

14 中断和唤醒分配
表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
706	tcpwm_0_interrupts_538_IRQn	Active	TCPWM0 Group #2, Counter #26 Interrupt
707	tcpwm_0_interrupts_539_IRQn	Active	TCPWM0 Group #2, Counter #27 Interrupt
708	tcpwm_0_interrupts_540_IRQn	Active	TCPWM0 Group #2, Counter #28 Interrupt
709	tcpwm_0_interrupts_541_IRQn	Active	TCPWM0 Group #2, Counter #29 Interrupt
710	tcpwm_0_interrupts_542_IRQn	Active	TCPWM0 Group #2, Counter #30 Interrupt
711	tcpwm_0_interrupts_543_IRQn	Active	TCPWM0 Group #2, Counter #31 Interrupt
752	tdm_0_interrupts_tx_0_IRQn	Active	TDM0 TX #0 Interrupt
753	tdm_0_interrupts_rx_0_IRQn	Active	TDM0 RX #0 Interrupt
754	tdm_0_interrupts_tx_1_IRQn	Active	TDM0 TX #1 Interrupt
755	tdm_0_interrupts_rx_1_IRQn	Active	TDM0 RX #1 Interrupt
756	tdm_0_interrupts_tx_2_IRQn	Active	TDM0 TX #2 Interrupt
757	tdm_0_interrupts_rx_2_IRQn	Active	TDM0 RX #2 Interrupt
758	tdm_0_interrupts_tx_3_IRQn	Active	TDM0 TX #3 Interrupt
759	tdm_0_interrupts_rx_3_IRQn	Active	TDM0 RX #3 Interrupt
760	sg_0_interrupts_0_IRQn	Active	SG0 #0 Interrupt
761	sg_0_interrupts_1_IRQn	Active	SG0 #1 Interrupt
762	sg_0_interrupts_2_IRQn	Active	SG0 #2 Interrupt
763	sg_0_interrupts_3_IRQn	Active	SG0 #3 Interrupt
764	sg_0_interrupts_4_IRQn	Active	SG0 #4 Interrupt
768	pwm_0_interrupts_0_IRQn	Active	PCM-PWM0 #0 Interrupt
769	pwm_0_interrupts_1_IRQn	Active	PCM-PWM0 #1 Interrupt
776	dac_0_interrupt_IRQn	Active	Audio DAC interrupt
780	mixer_0_interrupt_dst_IRQn	Active	MIXER0 Destination interrupt
781	mixer_0_interrupts_src_0_IRQn	Active	MIXER0 Source #0 Interrupt
782	mixer_0_interrupts_src_1_IRQn	Active	MIXER0 Source #1 Interrupt
783	mixer_0_interrupts_src_2_IRQn	Active	MIXER0 Source #2 Interrupt
784	mixer_0_interrupts_src_3_IRQn	Active	MIXER0 Source #3 Interrupt
785	mixer_0_interrupts_src_4_IRQn	Active	MIXER0 Source #4 Interrupt
789	mixer_1_interrupt_dst_IRQn	Active	MIXER1 Destination interrupt
790	mixer_1_interrupts_src_0_IRQn	Active	MIXER1 Source #0 Interrupt
791	mixer_1_interrupts_src_1_IRQn	Active	MIXER1 Source #1 Interrupt
792	mixer_1_interrupts_src_2_IRQn	Active	MIXER1 Source #2 Interrupt
793	mixer_1_interrupts_src_3_IRQn	Active	MIXER1 Source #3 Interrupt

(表格续下页...)

14 中断和唤醒分配

表 20 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
794	mixer_1_interrupts_src_4_IRQn	Active	MIXER1 Source #4 Interrupt

15 核心中断类型

15 核心中断类型

表 21 核心中断类型

Interrupt	Source	Power mode	Description
0	CPUIntIdx0_IRQn ¹⁾	DeepSleep	CPU User Interrupt #0
1	CPUIntIdx1_IRQn ¹⁾	DeepSleep	CPU User Interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU User Interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU User Interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU User Interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU User Interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU User Interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU User Interrupt #7
8	Internal0_IRQn	Active	Internal Software Interrupt #0
9	Internal1_IRQn	Active	Internal Software Interrupt #1
10	Internal2_IRQn	Active	Internal Software Interrupt #2
11	Internal3_IRQn	Active	Internal Software Interrupt #3
12	Internal4_IRQn	Active	Internal Software Interrupt #4
13	Internal5_IRQn	Active	Internal Software Interrupt #5
14	Internal6_IRQn	Active	Internal Software Interrupt #6
15	Internal7_IRQn	Active	Internal Software Interrupt #7

1) 用户中断不能用于 Cortex®-M0+ 应用程序，因为它由系统调用内部使用。请注意，这不会影响 Cortex®-M7 应用程序。

16 Trigger multiplexer

Figure 8 **Trigger multiplexer¹⁷⁾**

17 触发组输入
17 触发组输入
表 22 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
MUX group 0: P-DMA0_0_15 trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	Allow P-DMA0 to chain to itself. Channels 0 - 32 are general purpose channels available for chaining
33:48	PDMA1_TR_OUT[0:15]	Cross connections from P-DMA1 to P-DMA0, Channels 0-15 are used
49:56	MDMA_TR_OUT[0:7]	Cross connections from M-DMA0 to P-DMA0
57:58	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
59:60	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
61:84	HSIOM_IO_INPUT[0:23]	I/O Inputs
85:88	FAULT_TR_OUT[0:3]	Fault events
MUX group 1: P-DMA0_16_31 trigger multiplexer		
1:38	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
39:50	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
51:82	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
83:84	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
85:86	CTI_TR_OUT[0:1]	Trace events
87:90	EVTGEN_TR_OUT[0:3]	Event generator triggers
MUX group 2: P-DMA1_0_15 trigger multiplexer		
1:16	PDMA1_TR_OUT[0:15]	Allow P-DMA1 to chain to itself. Channels 0 - 15 are dedicated for chaining
17:48	PDMA0_TR_OUT[0:31]	Cross connections from P-DMA0 to P-DMA1, channels 0-31 are used.
49:72	HSIOM_IO_INPUT[24:47]	I/O Inputs
MUX Group 3: M-DMA0 trigger multiplexer		
1:8	TCPWM0_16_TR_OUT0[0:7]	16-bit TCPWM0 counters
9:16	TCPWM0_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
17:20	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
MUX group 4: TCPWM0 Trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA0 triggers
33:48	PDMA1_TR_OUT[0:15]	General purpose P-DMA1 triggers
49:56	MDMA_TR_OUT[0:7]	M-DMA0 triggers

(表格续下页.....)

¹⁷ 该图仅显示 TRIG_LABEL；最终触发形成基于公式 TRIG_{PREFIX(IN/OUT)}_{MUX_x}_{TRIG_LABEL} 和表 22 和表 23 中提供的信息。

17 触发组输入
表 22 (续) 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
57:94	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
95:106	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
107:138	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
139	SMIF0_TX_TR_OUT	SMIF0 TX trigger
140	SMIF0_RX_TR_OUT	SMIF0 RX trigger
141	SMIF1_TX_TR_OUT	SMIF1 TX trigger
142	SMIF1_RX_TR_OUT	SMIF1 RX trigger
143:146	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
151:154	TDM0_TX_TR_OUT[0:3]	TDM0 TX trigger
155:158	TDM0_RX_TR_OUT[0:3]	TDM0 RX trigger
159:163	SG0_TR_COMPLETE[0:4]	SG0 TX complete trigger
164:165	PWM0_TX_TR_OUT[0:1]	PCM-PWM0 TX trigger
166:170	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER0 SRC trigger
171	MIXER0_TR_DST_REQ_OUT	MIXER0 DST trigger
172:176	MIXER1_TR_SRC_REQ_OUT[0:4]	MIXER1 SRC trigger
177	MIXER1_TR_DST_REQ_OUT	MIXER1 DST trigger
178	AUDIODAC0_TX_TR_OUT	AUDIO DAC0 TX trigger
MUX group 5: TCPWM0_20_31 Trigger multiplexer		
1:2	CAN0_DBG_TR_OUT[0:1]	CAN0 DMA events
3:4	CAN0_FIFO0_TR_OUT[0:1]	CAN0 FIFO0 events
5:6	CAN0_FIFO1_TR_OUT[0:1]	CAN0 FIFO1 events
7:8	CAN1_DBG_TR_OUT[0:1]	CAN1 DMA events
9:10	CAN1_FIFO0_TR_OUT[0:1]	CAN1 FIFO0 events
11:12	CAN1_FIFO1_TR_OUT[0:1]	CAN1 FIFO1 events
13:14	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
15:16	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
17:24	EVTGEN_TR_OUT[4:11]	Event generator triggers
MUX group 6: TCPWM0_32_59 Trigger Multiplexer		
1:16	TCPWM0_16_TR_OUT1[0:15]	16-bit TCPWM0 counters
17	SCB_TX_TR_OUT[0]	SCB0 TX trigger
18	SCB_RX_TR_OUT[0]	SCB0 RX trigger

(表格续下页.....)

17 触发组输入
表 22 (续) 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
19	SCB_I2C_SCL_TR_OUT[0]	SCB0 I2C trigger
20	SCB_TX_TR_OUT[1]	SCB1 TX trigger
21	SCB_RX_TR_OUT[1]	SCB1 RX trigger
22	SCB_I2C_SCL_TR_OUT[1]	SCB1 I2C trigger
23	SCB_TX_TR_OUT[2]	SCB2 TX trigger
24	SCB_RX_TR_OUT[2]	SCB2 RX trigger
25	SCB_I2C_SCL_TR_OUT[2]	SCB2 I2C trigger
26	SCB_TX_TR_OUT[3]	SCB3 TX trigger
27	SCB_RX_TR_OUT[3]	SCB3 RX trigger
28	SCB_I2C_SCL_TR_OUT[3]	SCB3 I2C trigger
29	SCB_TX_TR_OUT[4]	SCB4 TX trigger
30	SCB_RX_TR_OUT[4]	SCB4 RX trigger
31	SCB_I2C_SCL_TR_OUT[4]	SCB4 I2C trigger
32	SCB_TX_TR_OUT[5]	SCB5 TX trigger
33	SCB_RX_TR_OUT[5]	SCB5 RX trigger
34	SCB_I2C_SCL_TR_OUT[5]	SCB5 I2C trigger
35	SCB_TX_TR_OUT[6]	SCB6 TX trigger
36	SCB_RX_TR_OUT[6]	SCB6 RX trigger
37	SCB_I2C_SCL_TR_OUT[6]	SCB6 I2C trigger
38	SCB_TX_TR_OUT[7]	SCB7 TX trigger
39	SCB_RX_TR_OUT[7]	SCB7 RX trigger
40	SCB_I2C_SCL_TR_OUT[7]	SCB7 I2C trigger
41	SCB_TX_TR_OUT[8]	SCB8 TX trigger
42	SCB_RX_TR_OUT[8]	SCB8 RX trigger
43	SCB_I2C_SCL_TR_OUT[8]	SCB8 I2C trigger
44	SCB_TX_TR_OUT[9]	SCB9 TX trigger
45	CB_RX_TR_OUT[9]	SCB9 RX trigger
46	SCB_I2C_SCL_TR_OUT[9]	SCB9 I2C trigger
47	SCB_TX_TR_OUT[10]	SCB10 TX trigger
48	SCB_RX_TR_OUT[10]	SCB10 RX trigger
49	SCB_I2C_SCL_TR_OUT[10]	SCB10 I2C trigger
50	SCB_TX_TR_OUT[11]	SCB11 TX trigger
51	SCB_RX_TR_OUT[11]	SCB11 RX trigger

(表格续下页.....)

17 触发组输入
表 22 (续) 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
52	SCB_I2C_SCL_TR_OUT[11]	SCB11 I2C trigger
53:54	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
55:102	HSIOM_IO_INPUT[0:47]	I/O Inputs
103:104	CTI_TR_OUT[0:1]	Trace events
105:108	FAULT_TR_OUT[0:3]	Fault events
109:110	CXPI_TX_TR_OUT[0:1]	CXPI0 events
111:112	CXPI_RX_TR_OUT[0:1]	CXPI0 events

MUX group 7: PASS0 SAR trigger multiplexer

1:32	PDMA0_TR_OUT[0:31]	General-purpose P-DMA0 triggers
33:70	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
71:82	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
83:114	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
115:122	HSIOM_IO_INPUT[0:7]	I/O Inputs
123	EVTGEN_TR_OUT[12]	Event generator triggers

MUX group 8: CAN TT Sync trigger multiplexer

1:2	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
3:4	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs

MUX group 9: Debug trigger multiplexer

1:5	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP11_OUTPUT[0:4]	Output from debug reduction multiplexer #2
11:15	TR_GROUP12_OUTPUT[0:4]	Output from debug reduction multiplexer #3

MUX Group 10: Debug Reduction #1

1:76	PDMA0_TR_OUT[0:75]	General purpose P-DMA0 triggers
77:88	SCB_TX_TR_OUT[0:11]	SCB TX triggers
89:100	SCB_RX_TR_OUT[0:11]	SCB RX triggers
101:112	SCB_I2C_SCL_TR_OUT[0:11]	SCB I2C triggers
113:114	CAN0_DBG_TR_OUT[0:1]	CAN0 DMA
115:116	CAN0_FIFO0_TR_OUT[0:1]	CAN0 FIFO0
117:118	CAN0_FIFO1_TR_OUT[0:1]	CAN0 FIFO1
119:120	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
121:122	CAN1_DBG_TR_OUT[0:1]	CAN1 DMA
123:124	CAN1_FIFO0_TR_OUT[0:1]	CAN1 FIFO0
125:126	CAN1_FIFO1_TR_OUT[0:1]	CAN1 FIFO1

(表格续下页...)

17 触发组输入
表 22 (续) 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
127:128	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
129:130	CTI_TR_OUT[0:1]	Trace events
131:134	FAULT_TR_OUT[0:3]	Fault events
135:150	EVTGEN_TR_OUT[0:15]	EVTGEN Triggers

MUX Group 11: Debug Reduction #2

1:32	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
33:44	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
45:82	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
83	SMIF0_TX_TR_OUT	SMIF0 TX trigger
84	SMIF0_RX_TR_OUT	SMIF0 RX trigger
85	SMIF1_TX_TR_OUT	SMIF1 TX trigger
86	SMIF1_RX_TR_OUT	SMIF1 RX trigger
87:90	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
95:98	TDM0_TX_TR_OUT[0:3]	TDM0 TX trigger
99:102	TDM0_RX_TR_OUT[0:3]	TDM0 RX trigger
103:107	SG0_TX_TR_OUT[0:4]	SG0 TX trigger
108:109	PWM0_TX_TR_OUT[0:1]	PCM-PWM0 TX trigger
110	AUDIODAC0_TX_TR_OUT	AUDIO DAC0 TX trigger
111:115	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER0 SRC trigger
116	MIXER0_TR_DST_REQ_OUT	MIXER0 DST trigger
117:121	MIXER1_TR_SRC_REQ_OUT[0:4]	MIXER1 SRC trigger
122	MIXER1_TR_DST_REQ_OUT	MIXER1 DST trigger
123:170	HSIOM_IO_INPUT[0:47]	I/O inputs
171:172	CXPI_TX_TR_OUT[0:1]	CXPI0 TX trigger
173:174	CXPI_RX_TR_OUT[0:1]	CXPI0 RX trigger

MUX Group 12: Debug Reduction #3

1:84	PDMA1_TR_OUT[0:83]	General purpose P-DMA1 triggers
85:92	MDMA_TR_OUT[0:7]	M-DMA0 triggers
93:124	TCPWM0_32_TR_OUT1[0:31]	32-bit TCPWM0 counters
125:136	TCPWM0_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM0 counters
137:174	TCPWM0_16_TR_OUT1[0:37]	16-bit TCPWM0 counters

(表格续下页...)

17 触发组输入
表 22 (续) 触发输入

Input	Trigger Label (TRIG_LABEL)	Description
175:176	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
MUX group 13: AXI M-DMA trigger multiplexer		
1:4	TCPWM0_16_TR_OUT0[0:3]	16-bit TCPWM0 counters
5:8	TCPWM0_32_TR_OUT0[0:3]	32-bit TCPWM0 counters
9:12	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers

18 触发组输出

18 触发组输出

表 23 触发输出

Output	Trigger	Description
MUX group 0: P-DMA0_0_15 trigger multiplexer MUX		
0:15	PDMA0_TR_IN[0:15]	Triggers to P-DMA0[0:15]
group 1: P-DMA0_16_31 trigger multiplexer MUX		
0:15	PDMA0_TR_IN[16:31]	Triggers to P-DMA0[16:31]
group 2: P-DMA1_0_15 trigger multiplexer MUX		
0:15	PDMA1_TR_IN[0:15]	Triggers to P-DMA1
group 3: M-DMA0 trigger multiplexer		
0:7	MDMA_TR_IN[0:7]	Triggers to M-DMA0
MUX group 4: TCPWM0 Trigger multiplexer		
0:19	TCPWM0_ALL_CNT_TR_IN[0:19]	Triggers to TCPWM0
MUX group 5: TCPWM0_20_31 Trigger multiplexer		
0:11	TCPWM0_ALL_CNT_TR_IN[20:31]	Triggers to TCPWM0
MUX group 6: TCPWM0_32_59 Trigger multiplexer		
0:27	TCPWM0_ALL_CNT_TR_IN[32:59]	Triggers to TCPWM0
MUX group 7: PASS0 SAR trigger multiplexer		
0:3	PASS_GEN_TR_IN[0:3]	Triggers to PASS0 SAR
MUX group 8: CAN TT Sync trigger multiplexer		
0:1	CAN0_TT_TR_IN[0:1]	CAN0 TT Sync Inputs
2:3	CAN1_TT_TR_IN[0:1]	CAN1 TT Sync Inputs
MUX group 9: Debug trigger multiplexer		
0	HSIOM_IO_OUTPUT[0]	To HSIOM as an output
1	HSIOM_IO_OUTPUT[1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To the Cross Trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze PASS0 SAR operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
7	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[2]	Signal to Freeze MCWDT2 operation
8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1]	Signal to Freeze MCWDT1 operation
9	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0]	Signal to Freeze MCWDT0 operation

(表格续下页.....)

18 触发组输出
表 23 (续) 触发输出

Output	Trigger	Description
10	TCPWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM0 operation
12	TDM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TDM0 operation
13	SG0_DEBUG_FREEZE_TR_IN	Signal to Freeze SG0 operation
14	PWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze PWM0 operation
15	MIXER0_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER0 operation
16	MIXER1_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER1 operation
17	AUDIODAC0_DEBUG_FREEZE_TR_IN	Signal to Freeze AUDIO DAC0 operation
MUX Group 10: Debug Reduction #1		
0:4	TR_GROUP9_INPUT[1:5]	To main debug multiplexer
MUX Group 11: Debug Reduction #2		
0:4	TR_GROUP9_INPUT[6:10]	To main debug multiplexer
MUX Group 12: Debug Reduction #3		
0:4	TR_GROUP9_INPUT[11:15]	To main debug multiplexer
MUX group 13: AXI-DMA trigger multiplexer		
0:3	AXIDMA_TR_IN[0:3]	Triggers to AXI M-DMA1

19 一对一触发器

19 一对一触发器

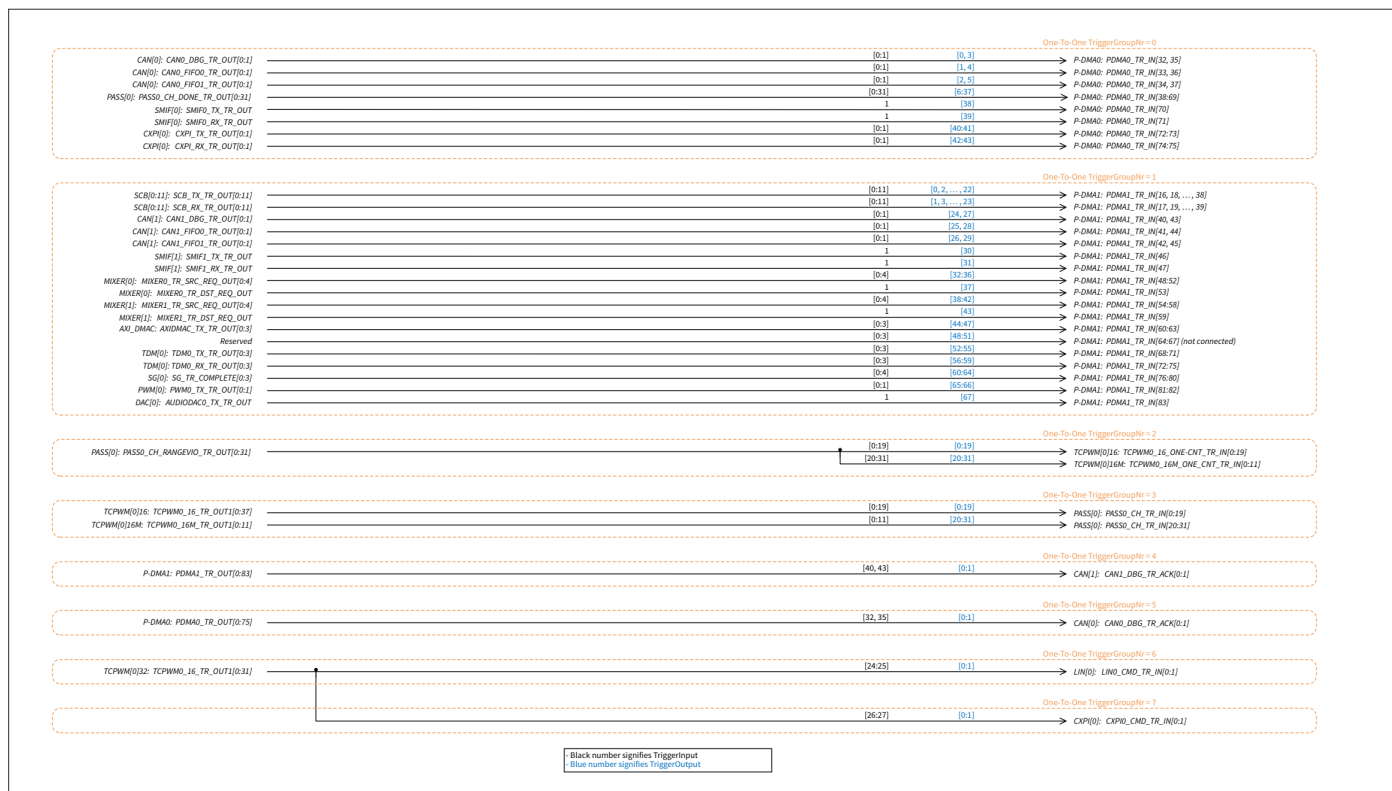


图 9 一对一触发器¹⁸⁾

表 24 触发器 1:1

Input	Trigger In	Trigger Out	Description
MUX Group 0: CAN0 to P-DMA0 Triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[32]	CAN0, Channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[33]	CAN0, Channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[34]	CAN0, Channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[35]	CAN0, Channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[36]	CAN0, Channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[37]	CAN0, Channel #1 FIFO1 trigger
6:37	PASS0_CH_DONE_TR_OUT[0:31]	PDMA0_TR_IN[38:69]	PASS0 SAR0 to P-DMA0 direct connect
38	SMIF0_TX_TR_OUT	PDMA0_TR_IN[70]	SMIF TX to P-DMA0 Trigger
39	SMIF0_RX_TR_OUT	PDMA0_TR_IN[71]	SMIF RX to P-DMA0 Trigger
40:41	CXPI0_TX_TR_OUT[0:1]	PDMA0_TR_IN[72:73]	CXPI 0 TX P-DMA0 Triggers
42:43	CXPI0_RX_TR_OUT[0:1]	PDMA0_TR_IN[74:75]	CXPI 0 RX P-DMA0 Triggers

MUX group 1: SCBx to P-DMA1 Triggers

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¹⁸⁾ 该图仅显示 TRIG_LABEL；最终触发形成基于公式 $TRIG_{\{PREFIX(IN_1TO1/OUT_1TO1)\}_{x}}\{TRIG_LABEL\}$ 和表 24 中提供的信息。

19 一对一触发器
表 24 (续) 触发器 1:1

Input	Trigger In	Trigger Out	Description
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[16]	SCB0 to P-DMA1 Trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[17]	SCB0 to P-DMA1 Trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[18]	SCB1 to P-DMA1 Trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[19]	SCB1 to P-DMA1 Trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[20]	SCB2 to P-DMA1 Trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[21]	SCB2 to P-DMA1 Trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[22]	SCB3 to P-DMA1 Trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[23]	SCB3 to P-DMA1 Trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[24]	SCB4 to P-DMA1 Trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[25]	SCB4 to P-DMA1 Trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[26]	SCB5 to P-DMA1 Trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[27]	SCB5 to P-DMA1 Trigger
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[28]	SCB6 to P-DMA1 Trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[29]	SCB6 to P-DMA1 Trigger
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[30]	SCB7 to P-DMA1 Trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[31]	SCB7 to P-DMA1 Trigger
16	SCB8_TX_TR_OUT	PDMA1_TR_IN[32]	SCB8 to P-DMA1 Trigger
17	SCB8_RX_TR_OUT	PDMA1_TR_IN[33]	SCB8 to P-DMA1 Trigger
18	SCB9_TX_TR_OUT	PDMA1_TR_IN[34]	SCB9 to P-DMA1 Trigger
19	SCB9_RX_TR_OUT	PDMA1_TR_IN[35]	SCB9 to P-DMA1 Trigger
20	SCB10_TX_TR_OUT	PDMA1_TR_IN[36]	SCB10 to P-DMA1 Trigger
21	SCB10_RX_TR_OUT	PDMA1_TR_IN[37]	SCB10 to P-DMA1 Trigger
22	SCB11_TX_TR_OUT	PDMA1_TR_IN[38]	SCB11 to P-DMA1 Trigger
23	SCB11_RX_TR_OUT	PDMA1_TR_IN[39]	SCB11 to P-DMA1 Trigger
24	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[40]	CAN1 Channel #0 P-DMA1 trigger
25	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[41]	CAN1 Channel #0 FIFO0 trigger
26	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[42]	CAN1 Channel #0 FIFO1 trigger
27	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[43]	CAN1 Channel #1 P-DMA1 trigger
28	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[44]	CAN1 Channel #1 FIFO0 trigger
29	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[45]	CAN1 Channel #1 FIFO1 trigger
30	SMIF1_TX_TR_OUT	PDMA1_TR_IN[46]	SMIF1 TX to P-DMA1 trigger
31	SMIF1_RX_TR_OUT	PDMA1_TR_IN[47]	SMIF1 RX to P-DMA1 trigger
32:36	MIXER0_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[48:52]	MIXER0 to P-DMA1 trigger

(表格续下页.....)

19 一对一触发器
表 24 (续) 触发器 1:1

Input	Trigger In	Trigger Out	Description
37	MIXER0_TR_DST_REQ_OUT	PDMA1_TR_IN[53]	MIXER0 to P-DMA1 trigger
38:42	MIXER1_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[54:58]	MIXER1 to P-DMA1 trigger
43	MIXER1_TR_DST_REQ_OUT	PDMA1_TR_IN[59]	MIXER1 to P-DMA1 trigger
44:47	AXIDMA_TR_OUT[0:3]	PDMA1_TR_IN[60:63]	AXI M-DMA1 to P-DMA1 trigger
52:55	TDM0_TX_TR_OUT[0:3]	PDMA1_TR_IN[68:71]	TDM0 TX to P-DMA1 trigger
56:59	TDM0_RX_TR_OUT[0:3]	PDMA1_TR_IN[72:75]	TDM0 RX to P-DMA1 trigger
60:64	SG0_TX_TR_OUT[0:4]	PDMA1_TR_IN[76:80]	SG0 TX to P-DMA1 trigger
65:66	PWM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[81:82]	PWM0 TX to P-DMA1 trigger
67	AUDIODAC0_TX_TR_OUT	PDMA1_TR_IN[83]	AUDIODAC0 to P-DMA1 trigger

MUX group 2: PASS SARx to TCPWM1 direct connect

0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16_ONE_CNT_TR_IN[0]	SAR0 ch#0, range violation to TCPWM0 Group#0 Counter#00 trig=2
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16_ONE_CNT_TR_IN[1]	SAR0 ch#1, range violation to TCPWM0 Group#0 Counter#01 trig=2
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16_ONE_CNT_TR_IN[2]	SAR0 ch#2, range violation to TCPWM0 Group#0 Counter#02 trig=2
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16_ONE_CNT_TR_IN[3]	SAR0 ch#3, range violation to TCPWM0 Group#0 Counter#03 trig=2
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16_ONE_CNT_TR_IN[4]	SAR0 ch#4, range violation to TCPWM0 Group#0 Counter#04 trig=2
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16_ONE_CNT_TR_IN[5]	SAR0 ch#5, range violation to TCPWM0 Group#0 Counter#05 trig=2
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16_ONE_CNT_TR_IN[6]	SAR0 ch#6, range violation to TCPWM0 Group#0 Counter#06 trig=2
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16_ONE_CNT_TR_IN[7]	SAR0 ch#7, range violation to TCPWM0 Group#0 Counter#07 trig=2
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16_ONE_CNT_TR_IN[8]	SAR0 ch#8, range violation to TCPWM0 Group#0 Counter#08 trig=2
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16_ONE_CNT_TR_IN[9]	SAR0 ch#9, range violation to TCPWM0 Group#0 Counter#09 trig=2
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16_ONE_CNT_TR_IN[10]	SAR0 ch#10, range violation to TCPWM0 Group#0 Counter#10 trig=2
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16_ONE_CNT_TR_IN[11]	SAR0 ch#11, range violation to TCPWM0 Group#0 Counter#11 trig=2
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16_ONE_CNT_TR_IN[12]	SAR0 ch#12, range violation to TCPWM0 Group#0 Counter#12 trig=2

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19 一对一触发器
表 24 (续) 触发器 1:1

Input	Trigger In	Trigger Out	Description
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16_ONE_CNT_TR_IN[13]	SAR0 ch#13, range violation to TCPWM0 Group#0 Counter#13 trig=2
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16_ONE_CNT_TR_IN[14]	SAR0 ch#14, range violation to TCPWM0 Group#0 Counter#14 trig=2
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16_ONE_CNT_TR_IN[15]	SAR0 ch#15, range violation to TCPWM0 Group#0 Counter#15 trig=2
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16_ONE_CNT_TR_IN[16]	SAR0 ch#16, range violation to TCPWM0 Group#0 Counter#16 trig=2
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16_ONE_CNT_TR_IN[17]	SAR0 ch#17, range violation to TCPWM0 Group#0 Counter#17 trig=2
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#18, range violation to TCPWM0 Group#0 Counter#18 trig=2
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#19, range violation to TCPWM0 Group#0 Counter#19 trig=2
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#20, range violation to TCPWM0 Group#1 Counter#00 trig=2
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR0 ch#21, range violation to TCPWM0 Group#1 Counter#01 trig=2
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR0 ch#22, range violation to TCPWM0 Group#1 Counter#02 trig=2
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#23, range violation to TCPWM0 Group#1 Counter#03 trig=2
24	PASS0_CH_RANGEVIO_TR_OUT[24]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR0 ch#24, range violation to TCPWM0 Group#1 Counter#04 trig=2
25	PASS0_CH_RANGEVIO_TR_OUT[25]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR0 ch#25, range violation to TCPWM0 Group#1 Counter#05 trig=2
26	PASS0_CH_RANGEVIO_TR_OUT[26]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#26, range violation to TCPWM0 Group#1 Counter#06 trig=2
27	PASS0_CH_RANGEVIO_TR_OUT[27]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR0 ch#27, range violation to TCPWM0 Group#1 Counter#07 trig=2
28	PASS0_CH_RANGEVIO_TR_OUT[28]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR0 ch#28, range violation to TCPWM0 Group#1 Counter#08 trig=2
29	PASS0_CH_RANGEVIO_TR_OUT[29]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#29, range violation to TCPWM0 Group#1 Counter#09 trig=2
30	PASS0_CH_RANGEVIO_TR_OUT[30]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR0 ch#30, range violation to TCPWM0 Group#1 Counter#10 trig=2
31	PASS0_CH_RANGEVIO_TR_OUT[31]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR0 ch#31, range violation to TCPWM0 Group#1 Counter#11 trig=2

MUX group 3: TCPWM0 to PASS SARx

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19 一对一触发器
表 24 (续) 触发器 1:1

Input	Trigger In	Trigger Out	Description
0:19	TCPWM0_16_TR_OUT1[0:19]	PASS0_CH_TR_IN[0:19]	TCPWM0 Group #0 Counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#0 through SAR0 ch#19
20:31	TCPWM0_16M_TR_OUT1[0:11]	PASS0_CH_TR_IN[20:31]	TCPWM0 Group #1 Counter #00 through 11 (PWM0_M_0 to PWM0_M_11) to SAR0 ch#20 through SAR0 ch#31

MUX group 4: Acknowledge triggers from P-DMA1 to CAN1

0	PDMA1_TR_OUT[40]	CAN1_DBG_TR_ACK[0]	CAN1 Channel#0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[43]	CAN1_DBG_TR_ACK[1]	CAN1 Channel#1 P-DMA1 acknowledge

MUX group 5: Acknowledge triggers from P-DMA0 to CAN0

0	PDMA0_TR_OUT[32]	CAN0_DBG_TR_ACK[0]	CAN0 Channel#0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[35]	CAN0_DBG_TR_ACK[1]	CAN0 Channel#1 P-DMA0 acknowledge

MUX group 6: TCPWM0 to LIN0 triggers

0:1	TCPWM0_16_TR_OUT1[24:25]	LIN0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to LIN0
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MUX group 7: TCPWM0_TO_CXPI (TCPWM0 to CXPI)

0:1	TCPWM0_16_TR_OUT1[26:27]	CXPI0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to CXPI0
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1) SAR ADC[x] 的每个逻辑通道都可以连接到任意 SAR ADC[x]_y 外部引脚。(x = 0, or 1, or 2 and y=0 to max 31)

20 外设时钟

20 外设时钟

表 25 外设时钟分配

Output	Destination	Description
CPUSS root clocks (Group 0)		
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO9_CLOCK	Smart I/O #9
2	PCLK_TCPWM0_CLOCKS0	TCPWM0 Group #0, Counter #0
3	PCLK_TCPWM0_CLOCKS1	TCPWM0 Group #0, Counter #1
4	PCLK_TCPWM0_CLOCKS2	TCPWM0 Group #0, Counter #2
5	PCLK_TCPWM0_CLOCKS3	TCPWM0 Group #0, Counter #3
6	PCLK_TCPWM0_CLOCKS4	TCPWM0 Group #0, Counter #4
7	PCLK_TCPWM0_CLOCKS5	TCPWM0 Group #0, Counter #5
8	PCLK_TCPWM0_CLOCKS6	TCPWM0 Group #0, Counter #6
9	PCLK_TCPWM0_CLOCKS7	TCPWM0 Group #0, Counter #7
10	PCLK_TCPWM0_CLOCKS8	TCPWM0 Group #0, Counter #8
11	PCLK_TCPWM0_CLOCKS9	TCPWM0 Group #0, Counter #9
12	PCLK_TCPWM0_CLOCKS10	TCPWM0 Group #0, Counter #10
13	PCLK_TCPWM0_CLOCKS11	TCPWM0 Group #0, Counter #11
14	PCLK_TCPWM0_CLOCKS12	TCPWM0 Group #0, Counter #12
15	PCLK_TCPWM0_CLOCKS13	TCPWM0 Group #0, Counter #13
16	PCLK_TCPWM0_CLOCKS14	TCPWM0 Group #0, Counter #14
17	PCLK_TCPWM0_CLOCKS15	TCPWM0 Group #0, Counter #15
18	PCLK_TCPWM0_CLOCKS16	TCPWM0 Group #0, Counter #16
19	PCLK_TCPWM0_CLOCKS17	TCPWM0 Group #0, Counter #17
20	PCLK_TCPWM0_CLOCKS18	TCPWM0 Group #0, Counter #18
21	PCLK_TCPWM0_CLOCKS19	TCPWM0 Group #0, Counter #19
22	PCLK_TCPWM0_CLOCKS20	TCPWM0 Group #0, Counter #20
23	PCLK_TCPWM0_CLOCKS21	TCPWM0 Group #0, Counter #21
24	PCLK_TCPWM0_CLOCKS22	TCPWM0 Group #0, Counter #22
25	PCLK_TCPWM0_CLOCKS23	TCPWM0 Group #0, Counter #23
26	PCLK_TCPWM0_CLOCKS24	TCPWM0 Group #0, Counter #24
27	PCLK_TCPWM0_CLOCKS25	TCPWM0 Group #0, Counter #25
28	PCLK_TCPWM0_CLOCKS26	TCPWM0 Group #0, Counter #26
29	PCLK_TCPWM0_CLOCKS27	TCPWM0 Group #0, Counter #27
30	PCLK_TCPWM0_CLOCKS28	TCPWM0 Group #0, Counter #28

(表格续下页.....)

20 外设时钟
表 25 (续) 外设时钟分配

Output	Destination	Description
31	PCLK_TCPWM0_CLOCKS29	TCPWM0 Group #0, Counter #29
32	PCLK_TCPWM0_CLOCKS30	TCPWM0 Group #0, Counter #30
33	PCLK_TCPWM0_CLOCKS31	TCPWM0 Group #0, Counter #31
34	PCLK_TCPWM0_CLOCKS32	TCPWM0 Group #0, Counter #32
35	PCLK_TCPWM0_CLOCKS33	TCPWM0 Group #0, Counter #33
36	PCLK_TCPWM0_CLOCKS34	TCPWM0 Group #0, Counter #34
37	PCLK_TCPWM0_CLOCKS35	TCPWM0 Group #0, Counter #35
38	PCLK_TCPWM0_CLOCKS36	TCPWM0 Group #0, Counter #36
39	PCLK_TCPWM0_CLOCKS37	TCPWM0 Group #0, Counter #37
40	PCLK_TCPWM0_CLOCKS256	TCPWM0 Group #1, Counter #0
41	PCLK_TCPWM0_CLOCKS257	TCPWM0 Group #1, Counter #1
42	PCLK_TCPWM0_CLOCKS258	TCPWM0 Group #1, Counter #2
43	PCLK_TCPWM0_CLOCKS259	TCPWM0 Group #1, Counter #3
44	PCLK_TCPWM0_CLOCKS260	TCPWM0 Group #1, Counter #4
45	PCLK_TCPWM0_CLOCKS261	TCPWM0 Group #1, Counter #5
46	PCLK_TCPWM0_CLOCKS262	TCPWM0 Group #1, Counter #6
47	PCLK_TCPWM0_CLOCKS263	TCPWM0 Group #1, Counter #7
48	PCLK_TCPWM0_CLOCKS264	TCPWM0 Group #1, Counter #8
49	PCLK_TCPWM0_CLOCKS265	TCPWM0 Group #1, Counter #9
50	PCLK_TCPWM0_CLOCKS266	TCPWM0 Group #1, Counter #10
51	PCLK_TCPWM0_CLOCKS267	TCPWM0 Group #1, Counter #11
52	PCLK_TCPWM0_CLOCKS512	TCPWM0 Group #2, Counter #0
53	PCLK_TCPWM0_CLOCKS513	TCPWM0 Group #2, Counter #1
54	PCLK_TCPWM0_CLOCKS514	TCPWM0 Group #2, Counter #2
55	PCLK_TCPWM0_CLOCKS515	TCPWM0 Group #2, Counter #3
56	PCLK_TCPWM0_CLOCKS516	TCPWM0 Group #2, Counter #4
57	PCLK_TCPWM0_CLOCKS517	TCPWM0 Group #2, Counter #5
58	PCLK_TCPWM0_CLOCKS518	TCPWM0 Group #2, Counter #6
59	PCLK_TCPWM0_CLOCKS519	TCPWM0 Group #2, Counter #7
60	PCLK_TCPWM0_CLOCKS520	TCPWM0 Group #2, Counter #8
61	PCLK_TCPWM0_CLOCKS521	TCPWM0 Group #2, Counter #9
62	PCLK_TCPWM0_CLOCKS522	TCPWM0 Group #2, Counter #10
63	PCLK_TCPWM0_CLOCKS523	TCPWM0 Group #2, Counter #11

(表格续下页.....)

20 外设时钟
表 25 (续) 外设时钟分配

Output	Destination	Description
64	PCLK_TCPWM0_CLOCKS524	TCPWM0 Group #2, Counter #12
65	PCLK_TCPWM0_CLOCKS525	TCPWM0 Group #2, Counter #13
66	PCLK_TCPWM0_CLOCKS526	TCPWM0 Group #2, Counter #14
67	PCLK_TCPWM0_CLOCKS527	TCPWM0 Group #2, Counter #15
68	PCLK_TCPWM0_CLOCKS528	TCPWM0 Group #2, Counter #16
69	PCLK_TCPWM0_CLOCKS529	TCPWM0 Group #2, Counter #17
70	PCLK_TCPWM0_CLOCKS530	TCPWM0 Group #2, Counter #18
71	PCLK_TCPWM0_CLOCKS531	TCPWM0 Group #2, Counter #19
72	PCLK_TCPWM0_CLOCKS532	TCPWM0 Group #2, Counter #20
73	PCLK_TCPWM0_CLOCKS533	TCPWM0 Group #2, Counter #21
74	PCLK_TCPWM0_CLOCKS534	TCPWM0 Group #2, Counter #22
75	PCLK_TCPWM0_CLOCKS535	TCPWM0 Group #2, Counter #23
76	PCLK_TCPWM0_CLOCKS536	TCPWM0 Group #2, Counter #24
77	PCLK_TCPWM0_CLOCKS537	TCPWM0 Group #2, Counter #25
78	PCLK_TCPWM0_CLOCKS538	TCPWM0 Group #2, Counter #26
79	PCLK_TCPWM0_CLOCKS539	TCPWM0 Group #2, Counter #27
80	PCLK_TCPWM0_CLOCKS540	TCPWM0 Group #2, Counter #28
81	PCLK_TCPWM0_CLOCKS541	TCPWM0 Group #2, Counter #29
82	PCLK_TCPWM0_CLOCKS542	TCPWM0 Group #2, Counter #30
83	PCLK_TCPWM0_CLOCKS543	TCPWM0 Group #2, Counter #31

COMM root clocks (Group 1)

0	PCLK_CAN FD0_CLOCK_CAN0	CAN0, Channel #0
1	PCLK_CAN FD0_CLOCK_CAN1	CAN0, Channel #1
2	PCLK_CAN FD1_CLOCK_CAN0	CAN1, Channel #0
3	PCLK_CAN FD1_CLOCK_CAN1	CAN1, Channel #1
4	PCLK_LIN0_CLOCK_CH_EN0	LIN0, Channel #0
5	PCLK_LIN0_CLOCK_CH_EN1	LIN0, Channel #1
6	PCLK_CXPI0_CLOCK_CH_EN0	CXPI0, Channel #0
7	PCLK_CXPI0_CLOCK_CH_EN1	CXPI0, Channel #1
8	PCLK_SCB0_CLOCK	SCB0
9	PCLK_SCB1_CLOCK	SCB1
10	PCLK_SCB2_CLOCK	SCB2
11	PCLK_SCB3_CLOCK	SCB3

(表格续下页.....)

20 外设时钟

表 25 (续) 外设时钟分配

Output	Destination	Description
12	PCLK_SCB4_CLOCK	SCB4
13	PCLK_SCB5_CLOCK	SCB5
14	PCLK_SCB6_CLOCK	SCB6
15	PCLK_SCB7_CLOCK	SCB7
16	PCLK_SCB8_CLOCK	SCB8
17	PCLK_SCB9_CLOCK	SCB9
18	PCLK_SCB10_CLOCK	SCB10
19	PCLK_SCB11_CLOCK	SCB11
20	PCLK_PASS0_CLOCK_SAR0	SAR0

21 故障
21 故障
表 26 故障分配

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ S MPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': S MPU violation.
1	CPUSS_MPU_VIO_1	Crypto S MPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA1 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
9	CPUSS_MPU_VIO_9	ETH0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
11	CPUSS_MPU_VIO_11	AXI M-DMA1 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
12	CPUSS_MPU_VIO_12	VIDEOSS0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
14	CPUSS_MPU_VIO_14	CM7_0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test Controller MPU/S MPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_CM7_0_CACHE_C_ECC	Correctable ECC error in CM7_0 Cache memories DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details. DATA0[31]: 0=Instruction cache, 1= Data cache
17	CPUSS_CM7_0_CACHE_NC_ECC	Non-correctable ECC error in CM7_0 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description
18	CPUSS_CM7_0_TCM_C_ECC	Correctable ECC error in CM7_0 TCM memory DATA0[23:2]: Violating address. DATA1[7:0]: Syndrome of code word (at address offset 0x0). DATA1[31:30]: 0= ITCM, 2=D0TCM, 3=D1TCM
19	CPUSS_CM7_0_TCM_NC_ECC	Non-correctable ECC error in CM7_0 TCM memory. See CPUSS_CM7_0_TCM_C_ECC description.

(表格续下页.....)

21 故障
表 26 (续) 故障分配

Fault	Source	Description
24	PERI_PERI_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
25	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation
26	PERI_MS_VIO_0	CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: master interface, PPU violation, “1”: timeout detected, “2”: bus error, other: undefined.
27	PERI_MS_VIO_1	CM7_0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
29	PERI_MS_VIO_3	P-DMA0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_4	P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
32	PERI_GROUP_VIO_0	Peripheral Group #0 violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.

(表格续下页.....)

21 故障
表 26 (续) 故障分配

Fault	Source	Description
36	PERI_GROUP_VIO_4	Peripheral Group #4 violation. See PERI_GROUP_VIO_0 description.
37	PERI_GROUP_VIO_5	Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.
40	PERI_GROUP_VIO_8	Peripheral Group #8 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.
42	PERI_GROUP_VIO_10	Peripheral Group #10 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERR	Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERR	Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.

(表格续下页.....)

21 故障
表 26 (续) 故障分配

Fault	Source	Description
56	CPUSS_FM_SRAMC_C_ECC	Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
57	CPUSS_FM_SRAMC_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
62	CPUSS_RAMC2_C_ECC	System memory controller 2 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
63	CPUSS_RAMC2_NC_ECC	System memory controller 2 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
64	CPUSS_CRYPT0_C_ECC	Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.
65	CPUSS_CRYPT0_NC_ECC	Crypto memory non-correctable ECC violation. See CPUSS_CRYPT0_C_ECC description.
66	CPUSS_DW0_C_ECC	P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
67	CPUSS_DW0_NC_ECC	P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
68	CPUSS_DW1_C_ECC	P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
69	CPUSS_DW1_NC_ECC	P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.

(表格续下页.....)

21 故障
表 26 (续) 故障分配

Fault	Source	Description
70	CAN FD_0_CAN_C_ECC	CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttCAN FD cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.
71	CAN FD_0_CAN_NC_ECC	CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttCAN FD cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
72	CAN FD_1_CAN_C_ECC	CAN1 message buffer correctable ECC violation. See CAN FD_0_CAN_C_ECC description.
73	CAN FD_1_CAN_NC_ECC	CAN1 message buffer non-correctable ECC violation. See CAN FD_0_CAN_NC_ECC description.
82	VIDEOSS_0_VRPU_RD_0	VIDEOSS Fault Reporting VRPU read 0: DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined.
83	VIDEOSS_0_VRPU_RD_1	VIDEOSS Fault Reporting VRPU read 1. See VIDEOSS_0_VRPU_RD_0 description.
84	VIDEOSS_0_VRPU_RD_2	VIDEOSS Fault Reporting VRPU read 2. See VIDEOSS_0_VRPU_RD_0 description.
85	VIDEOSS_0_VRPU_RD_3	VIDEOSS Fault Reporting VRPU read 3. See VIDEOSS_0_VRPU_RD_0 description.

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21 故障
表 26 (续) 故障分配

Fault	Source	Description
86	VIDEOSS_0_VRPU_RD_4	VIDEOSS Fault Reporting VRPU read 4. See VIDEOSS_0_VRPU_RD_0 description.
87	VIDEOSS_0_VRPU_WR_0	VIDEOSS Fault Reporting VRPU write 0. See VIDEOSS_0_VRPU_RD_0 description.
88	VIDEOSS_0_VRPU_WR_1	VIDEOSS Fault Reporting VRPU write 1. See VIDEOSS_0_VRPU_RD_0 description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDDA_ADC DATA[1]: OVD on VDDA_ADC DATA[16]: LVD/HVD #1 DATA0[17]: LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description.

23 总线主控器

22 外设保护单元固定结构配对

保护配对由一对 PPU 结构组成，包括一个主结构和一个从结构。主结构保护从结构，从结构保护外设寄存器等资源，或外设本身。

有关 FX PPU 基地址，请参阅表 14。

表 27 PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
0	PERI_MAIN	0x40000200	0x00000040	Peripheral Interconnect main
1	PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral Group #0 main
3	PERI_GR1_GROUP	0x40004050	0x00000004	Peripheral Group #1 main
4	PERI_GR2_GROUP	0x40004090	0x00000004	Peripheral Group #2 main
5	PERI_GR3_GROUP	0x400040C0	0x00000020	Peripheral Group #3 main
6	PERI_GR4_GROUP	0x40004100	0x00000020	Peripheral Group #4 main
7	PERI_GR5_GROUP	0x40004140	0x00000020	Peripheral Group #5 main
8	PERI_GR6_GROUP	0x40004180	0x00000020	Peripheral Group #6 main
9	PERI_GR8_GROUP	0x40004200	0x00000020	Peripheral Group #8 main
10	PERI_GR9_GROUP	0x40004240	0x00000020	Peripheral Group #9 main
11	PERI_GR10_GROUP	0x40004280	0x00000020	Peripheral Group #10 main
12	PERI_GR0_BOOT	0x40004020	0x00000004	Peripheral Group #0 boot
13	PERI_GR1_BOOT	0x40004060	0x00000004	Peripheral Group #1 boot
14	PERI_GR2_BOOT	0x400040A0	0x00000004	Peripheral Group #2 boot
15	PERI_GR3_BOOT	0x400040E0	0x00000004	Peripheral Group #3 boot
16	PERI_GR4_BOOT	0x40004120	0x00000004	Peripheral Group #4 boot
17	PERI_GR5_BOOT	0x40004160	0x00000004	Peripheral Group #5 boot
18	PERI_GR6_BOOT	0x400041A0	0x00000004	Peripheral Group #6 boot
19	PERI_GR8_BOOT	0x40004220	0x00000004	Peripheral Group #8 boot
20	PERI_GR9_BOOT	0x40004260	0x00000004	Peripheral Group #9 boot
21	PERI_GR10_BOOT	0x400042A0	0x00000004	Peripheral Group #10 boot
22	PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
23	PERI_MS_BOOT	0x40030000	0x00001000	Peripheral master slave boot
24	PERI_PCLK_MAIN	0x40040000	0x00004000	Peripheral clock main
25	CRYPTO_MAIN	0x40100000	0x00000400	Crypto main
26	CRYPTO_CRYPT0	0x40101000	0x00000800	Crypto MMIO (Memory Mapped I/O)
27	CRYPTO_BOOT	0x40102000	0x00000100	Crypto boot
28	CRYPTO_KEY0	0x40102100	0x00000004	Crypto Key #0

(表格续下页...)

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
29	CRYPTO_KEY1	0x40102120	0x00000004	Crypto Key #1
30	CRYPTO_BUF	0x40108000	0x00002000	Crypto buffer
31	CPUSS_CM7_0	0x40200000	0x00000400	CM7_0 CPU core
32	Reserved	0x40200500	0x00000020	
33	CPUSS_CM0	0x40201000	0x00001000	CM0+ CPU core
34	CPUSS_BOOT ¹⁾	0x40202000	0x00000200	CPUSS boot
35	CPUSS_CM0_INT	0x40208000	0x00001000	CPUSS CM0+ interrupts
36	CPUSS_CM7_0_INT	0x4020A000	0x00001000	CPUSS CM7_0 interrupts
37	Reserved	0x4020C000	0x00001000	
38	FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUSS Fault Structure #0 main
39	FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUSS Fault Structure #1 main
40	FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS Fault Structure #2 main
41	FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS Fault Structure #3 main
42	IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC Structure #0
43	IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC Structure #1
44	IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC Structure #2
45	IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC Structure #3
46	IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC Structure #4
47	IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC Structure #5
48	IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC Structure #6
49	IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC Structure #7
50	IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC Interrupt Structure #0
51	IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC Interrupt Structure #1
52	IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC Interrupt Structure #2
53	IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC Interrupt Structure #3
54	IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC Interrupt Structure #4
55	IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC Interrupt Structure #5
56	IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC Interrupt Structure #6
57	IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC Interrupt Structure #7
58	PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection SMPU main
59	PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
60	PROT_MPU9_MAIN	0x40236400	0x00000400	Peripheral protection MPU #9 main
61	PROT_MPU11_MAIN	0x40236C00	0x00000004	Peripheral protection MPU #11 main

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
62	PROT_MPU12_MAIN	0x40237000	0x00000400	Peripheral protection MPU #12 main
63	PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
64	PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
65	FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
66	FLASHC_CMD	0x40240008	0x00000004	Flash controller command
67	FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
68	FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
69	FLASHC_CM7_0	0x402404E0	0x00000004	Flash controller CM7_0
70	FLASHC_CRYPT0	0x40240580	0x00000004	Flash controller Crypto
71	FLASHC_DW0	0x40240600	0x00000004	Flash controller P-DMA0
72	FLASHC_DW1	0x40240680	0x00000004	Flash controller P-DMA1
73	FLASHC_DM0	0x40240700	0x00000004	Flash controller M-DMA0
74	FLASHC_FlashMgmt	0x4024F000	0x00000080	Flash management
75	FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller main safety
76	FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work safety
77	SRSS_GENERAL	0x40260000	0x00000400	SRSS General
78	SRSS_MAIN	0x40261000	0x00001000	SRSS main
79	SRSS_SECURE	0x40262000	0x00002000	SRSS secure
80	MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
81	MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
82	MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
83	MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
84	WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
85	WDT_MAIN	0x4026C040	0x00000020	System WDT main
86	BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
87	DW0_DW	0x40280000	0x00000100	P-DMA0 main
88	DW1_DW	0x40290000	0x00000100	P-DMA1 main
89	DW0_DW_CRC	0x40280100	0x00000080	P-DMA0 CRC
90	DW1_DW_CRC	0x40290100	0x00000080	P-DMA1 CRC
91	DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA0 Channel #0
92	DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA0 Channel #1
93	DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA0 Channel #2
94	DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA0 Channel #3

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
95	DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA0 Channel #4
96	DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA0 Channel #5
97	DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA0 Channel #6
98	DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA0 Channel #7
99	DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA0 Channel #8
100	DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA0 Channel #9
101	DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA0 Channel #10
102	DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA0 Channel #11
103	DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA0 Channel #12
104	DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA0 Channel #13
105	DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA0 Channel #14
106	DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA0 Channel #15
107	DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA0 Channel #16
108	DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA0 Channel #17
109	DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA0 Channel #18
110	DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA0 Channel #19
111	DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA0 Channel #20
112	DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA0 Channel #21
113	DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA0 Channel #22
114	DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA0 Channel #23
115	DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA0 Channel #24
116	DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA0 Channel #25
117	DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA0 Channel #26
118	DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA0 Channel #27
119	DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA0 Channel #28
120	DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA0 Channel #29
121	DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA0 Channel #30
122	DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA0 Channel #31
123	DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA0 Channel #32
124	DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA0 Channel #33
125	DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA0 Channel #34
126	DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA0 Channel #35
127	DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA0 Channel #36

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
128	DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA0 Channel #37
129	DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA0 Channel #38
130	DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA0 Channel #39
131	DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA0 Channel #40
132	DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA0 Channel #41
133	DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA0 Channel #42
134	DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA0 Channel #43
135	DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA0 Channel #44
136	DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA0 Channel #45
137	DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA0 Channel #46
138	DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA0 Channel #47
139	DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA0 Channel #48
140	DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA0 Channel #49
141	DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA0 Channel #50
142	DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA0 Channel #51
143	DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA0 Channel #52
144	DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA0 Channel #53
145	DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA0 Channel #54
146	DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA0 Channel #55
147	DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA0 Channel #56
148	DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA0 Channel #57
149	DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA0 Channel #58
150	DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA0 Channel #59
151	DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA0 Channel #60
152	DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA0 Channel #61
153	DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA0 Channel #62
154	DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA0 Channel #63
155	DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA0 Channel #64
156	DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA0 Channel #65
157	DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA0 Channel #66
158	DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA0 Channel #67
159	DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA0 Channel #68
160	DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA0 Channel #69

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
161	DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA0 Channel #70
162	DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA0 Channel #71
163	DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA0 Channel #72
164	DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA0 Channel #73
165	DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA0 Channel #74
166	DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA0 Channel #75
167	DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA1 Channel #0
168	DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA1 Channel #1
169	DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA1 Channel #2
170	DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA1 Channel #3
171	DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA1 Channel #4
172	DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA1 Channel #5
173	DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA1 Channel #6
174	DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA1 Channel #7
175	DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA1 Channel #8
176	DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA1 Channel #9
177	DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA1 Channel #10
178	DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA1 Channel #11
179	DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA1 Channel #12
180	DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA1 Channel #13
181	DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA1 Channel #14
182	DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA1 Channel #15
183	DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA1 Channel #16
184	DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA1 Channel #17
185	DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA1 Channel #18
186	DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA1 Channel #19
187	DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA1 Channel #20
188	DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA1 Channel #21
189	DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA1 Channel #22
190	DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA1 Channel #23
191	DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA1 Channel #24
192	DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA1 Channel #25
193	DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA1 Channel #26

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
194	DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA1 Channel #27
195	DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA1 Channel #28
196	DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA1 Channel #29
197	DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA1 Channel #30
198	DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA1 Channel #31
199	DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA1 Channel #32
200	DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA1 Channel #33
201	DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA1 Channel #34
202	DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA1 Channel #35
203	DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA1 Channel #36
204	DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA1 Channel #37
205	DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA1 Channel #38
206	DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA1 Channel #39
207	DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA1 Channel #40
208	DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA1 Channel #41
209	DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA1 Channel #42
210	DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA1 Channel #43
211	DW1_CH_STRUCT44_CH	0x40298B00	0x00000040	P-DMA1 Channel #44
212	DW1_CH_STRUCT45_CH	0x40298B40	0x00000040	P-DMA1 Channel #45
213	DW1_CH_STRUCT46_CH	0x40298B80	0x00000040	P-DMA1 Channel #46
214	DW1_CH_STRUCT47_CH	0x40298BC0	0x00000040	P-DMA1 Channel #47
215	DW1_CH_STRUCT48_CH	0x40298C00	0x00000040	P-DMA1 Channel #48
216	DW1_CH_STRUCT49_CH	0x40298C40	0x00000040	P-DMA1 Channel #49
217	DW1_CH_STRUCT50_CH	0x40298C80	0x00000040	P-DMA1 Channel #50
218	DW1_CH_STRUCT51_CH	0x40298CC0	0x00000040	P-DMA1 Channel #51
219	DW1_CH_STRUCT52_CH	0x40298D00	0x00000040	P-DMA1 Channel #52
220	DW1_CH_STRUCT53_CH	0x40298D40	0x00000040	P-DMA1 Channel #53
221	DW1_CH_STRUCT54_CH	0x40298D80	0x00000040	P-DMA1 Channel #54
222	DW1_CH_STRUCT55_CH	0x40298DC0	0x00000040	P-DMA1 Channel #55
223	DW1_CH_STRUCT56_CH	0x40298E00	0x00000040	P-DMA1 Channel #56
224	DW1_CH_STRUCT57_CH	0x40298E40	0x00000040	P-DMA1 Channel #57
225	DW1_CH_STRUCT58_CH	0x40298E80	0x00000040	P-DMA1 Channel #58
226	DW1_CH_STRUCT59_CH	0x40298EC0	0x00000040	P-DMA1 Channel #59

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
227	DW1_CH_STRUCT60_CH	0x40298F00	0x00000040	P-DMA1 Channel #60
228	DW1_CH_STRUCT61_CH	0x40298F40	0x00000040	P-DMA1 Channel #61
229	DW1_CH_STRUCT62_CH	0x40298F80	0x00000040	P-DMA1 Channel #62
230	DW1_CH_STRUCT63_CH	0x40298FC0	0x00000040	P-DMA1 Channel #63
231	DW1_CH_STRUCT64_CH	0x40299000	0x00000040	P-DMA1 Channel #64
232	DW1_CH_STRUCT65_CH	0x40299040	0x00000040	P-DMA1 Channel #65
233	DW1_CH_STRUCT66_CH	0x40299080	0x00000040	P-DMA1 Channel #66
234	DW1_CH_STRUCT67_CH	0x402990C0	0x00000040	P-DMA1 Channel #67
235	DW1_CH_STRUCT68_CH	0x40299100	0x00000040	P-DMA1 Channel #68
236	DW1_CH_STRUCT69_CH	0x40299140	0x00000040	P-DMA1 Channel #69
237	DW1_CH_STRUCT70_CH	0x40299180	0x00000040	P-DMA1 Channel #70
238	DW1_CH_STRUCT71_CH	0x402991C0	0x00000040	P-DMA1 Channel #71
239	DW1_CH_STRUCT72_CH	0x40299200	0x00000040	P-DMA1 Channel #72
240	DW1_CH_STRUCT73_CH	0x40299240	0x00000040	P-DMA1 Channel #73
241	DW1_CH_STRUCT74_CH	0x40299280	0x00000040	P-DMA1 Channel #74
242	DW1_CH_STRUCT75_CH	0x402992C0	0x00000040	P-DMA1 Channel #75
243	DW1_CH_STRUCT76_CH	0x40299300	0x00000040	P-DMA1 Channel #76
244	DW1_CH_STRUCT77_CH	0x40299340	0x00000040	P-DMA1 Channel #77
245	DW1_CH_STRUCT78_CH	0x40299380	0x00000040	P-DMA1 Channel #78
246	DW1_CH_STRUCT79_CH	0x402993C0	0x00000040	P-DMA1 Channel #79
247	DW1_CH_STRUCT80_CH	0x40299400	0x00000040	P-DMA1 Channel #80
248	DW1_CH_STRUCT81_CH	0x40299440	0x00000040	P-DMA1 Channel #81
249	DW1_CH_STRUCT82_CH	0x40299480	0x00000040	P-DMA1 Channel #82
250	DW1_CH_STRUCT83_CH	0x402994C0	0x00000040	P-DMA1 Channel #83
251	DMAC_TOP	0x402A0000	0x00000010	M-DMA0 main
252	DMAC_CH0_CH	0x402A1000	0x00000100	M-DMA0 Channel #0
253	DMAC_CH1_CH	0x402A1100	0x00000100	M-DMA0 Channel #1
254	DMAC_CH2_CH	0x402A1200	0x00000100	M-DMA0 Channel #2
255	DMAC_CH3_CH	0x402A1300	0x00000100	M-DMA0 Channel #3
256	DMAC_CH4_CH	0x402A1400	0x00000100	M-DMA0 Channel #4
257	DMAC_CH5_CH	0x402A1500	0x00000100	M-DMA0 Channel #5
258	DMAC_CH6_CH	0x402A1600	0x00000100	M-DMA0 Channel #6
259	DMAC_CH7_CH	0x402A1700	0x00000100	M-DMA0 Channel #7

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
260	AXI_DMAC_TOP	0x402B0000	0x00000008	AXI M-DMA1 main
261	AXI_DMAC_SEC	0x402B0008	0x00000004	AXI M-DMA1 active secure channels
262	AXI_DMAC_NONSEC	0x402B000C	0x00000004	AXI M-DMA1 active non-secure channels
263	AXI_DMAC_CH0_CH	0x402B1000	0x00000100	AXI M-DMA1 Channel #0
264	AXI_DMAC_CH1_CH	0x402B1100	0x00000100	AXI M-DMA1 Channel #1
265	AXI_DMAC_CH2_CH	0x402B1200	0x00000100	AXI M-DMA1 Channel #2
266	AXI_DMAC_CH3_CH	0x402B1300	0x00000100	AXI M-DMA1 Channel #3
267	EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
268	EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
269	Reserved	0x402F0000	0x00001000	
270	HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOM Port #0
271	HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOM Port #1
272	HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOM Port #2
273	HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOM Port #3
274	HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOM Port #4
275	HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOM Port #5
276	HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOM Port #6
277	HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOM Port #7
278	HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOM Port #8
279	HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOM Port #9
280	HSIOM_PRT10_PRT	0x403000A0	0x00000008	HSIOM Port #10
281	HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOM Port #11
282	HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOM Port #12
283	HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOM Port #13
284	HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOM Port #14
285	HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOM Port #15
286	HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOM Port #16
287	HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOM Port #17
288	HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOM Port #18
289	HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOM Port #19
290	HSIOM_PRT20_PRT	0x40300140	0x00000008	HSIOM Port #20
291	HSIOM_PRT21_PRT	0x40300150	0x00000008	HSIOM Port #21
292	HSIOM_AMUX	0x40302000	0x00000020	HSIOM Analog multiplexer

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
293	HSIOM_MON	0x40302200	0x00000010	HSIOM monitor
294	GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_STD Port #0
295	GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD Port #1
296	GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD Port #2
297	GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_ENH Port #3
298	GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD Port #4
299	GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_ENH Port #5
300	GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_STD Port #6
301	GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_STD Port #7
302	GPIO_PRT8_PRT	0x40310400	0x00000040	GPIO_STD Port #8
303	GPIO_PRT9_PRT	0x40310480	0x00000040	GPIO_SMC Port #9
304	GPIO_PRT10_PRT	0x40310500	0x00000040	GPIO_SMC Port #10
305	GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_SMC Port #11
306	GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_SMC Port #12
307	GPIO_PRT13_PRT	0x40310680	0x00000040	HSIO_STDLN Port #13
308	GPIO_PRT14_PRT	0x40310700	0x00000040	HSIO_STDLN Port #14
309	GPIO_PRT15_PRT	0x40310780	0x00000040	HSIO_STDLN Port #15
310	GPIO_PRT16_PRT	0x40310800	0x00000040	HSIO_STDLN Port #16
311	GPIO_PRT17_PRT	0x40310880	0x00000040	HSIO_STDLN Port #17
312	GPIO_PRT18_PRT	0x40310900	0x00000040	HSIO_STDLN Port #18
313	GPIO_PRT19_PRT	0x40310980	0x00000040	HSIO_STDLN Port #19
314	GPIO_PRT20_PRT	0x40310A00	0x00000040	HSIO_STDLN Port #20
315	GPIO_PRT21_PRT	0x40310A80	0x00000040	HSIO_STDLN Port #21
316	GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_STD Port #0 Configuration
317	GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD Port #1 Configuration
318	GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD Port #2 Configuration
319	GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_ENH Port #3 Configuration
320	GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD Port #4 Configuration
321	GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_ENH Port #5 Configuration
322	GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_STD Port #6 Configuration
323	GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_STD Port #7 Configuration
324	GPIO_PRT8_CFG	0x40310440	0x00000020	GPIO_STD Port #8 Configuration
325	GPIO_PRT9_CFG	0x403104C0	0x00000020	GPIO_SMC Port #9 Configuration

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
326	GPIO_PRT10_CFG	0x40310540	0x00000008	GPIO_SMC Port #10 Configuration
327	GPIO_PRT11_CFG	0x403105C0	0x00000040	GPIO_SMC Port #11 Configuration
328	GPIO_PRT12_CFG	0x40310640	0x00000040	GPIO_SMC Port #12 Configuration
329	GPIO_PRT13_CFG	0x403106C0	0x00000040	HSIO_STDLN Port #13 Configuration
330	GPIO_PRT14_CFG	0x40310740	0x00000040	HSIO_STDLN Port #14 Configuration
331	GPIO_PRT15_CFG	0x403107C0	0x00000040	HSIO_STDLN Port #15 Configuration
332	GPIO_PRT16_CFG	0x40310840	0x00000040	HSIO_STDLN Port #16 Configuration
333	GPIO_PRT17_CFG	0x403108C0	0x00000040	HSIO_STDLN Port #17 Configuration
334	GPIO_PRT18_CFG	0x40310940	0x00000040	HSIO_STDLN Port #18 Configuration
335	GPIO_PRT19_CFG	0x403109C0	0x00000040	HSIO_STDLN Port #19 Configuration
336	GPIO_PRT20_CFG	0x40310A40	0x00000040	HSIO_STDLN Port #20 Configuration
337	GPIO_PRT21_CFG	0x40310AC0	0x00000040	HSIO_STDLN Port #21 Configuration
338	GPIO_GPIO	0x40314000	0x00000040	GPIO main
339	GPIO_TEST	0x40315000	0x00000008	GPIO test
340	SMARTIO_PRT9_PRT	0x40320900	0x00000100	SMART I/O #9
341	TCPWM0_GRP0_CNT0_CNT T	0x40380000	0x00000080	TCPWM0 Group #0, Counter #0
342	TCPWM0_GRP0_CNT1_CNT T	0x40380080	0x00000080	TCPWM0 Group #0, Counter #1
343	TCPWM0_GRP0_CNT2_CNT T	0x40380100	0x00000080	TCPWM0 Group #0, Counter #2
344	TCPWM0_GRP0_CNT3_CNT T	0x40380180	0x00000080	TCPWM0 Group #0, Counter #3
345	TCPWM0_GRP0_CNT4_CNT T	0x40380200	0x00000080	TCPWM0 Group #0, Counter #4
346	TCPWM0_GRP0_CNT5_CNT T	0x40380280	0x00000080	TCPWM0 Group #0, Counter #5
347	TCPWM0_GRP0_CNT6_CNT T	0x40380300	0x00000080	TCPWM0 Group #0, Counter #6
348	TCPWM0_GRP0_CNT7_CNT T	0x40380380	0x00000080	TCPWM0 Group #0, Counter #7
349	TCPWM0_GRP0_CNT8_CNT T	0x40380400	0x00000080	TCPWM0 Group #0, Counter #8
350	TCPWM0_GRP0_CNT9_CNT T	0x40380480	0x00000080	TCPWM0 Group #0, Counter #9

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
351	TCPWM0_GRP0_CNT10_CNT	0x40380500	0x00000080	TCPWM0 Group #0, Counter #10
352	TCPWM0_GRP0_CNT11_CNT	0x40380580	0x00000080	TCPWM0 Group #0, Counter #11
353	TCPWM0_GRP0_CNT12_CNT	0x40380600	0x00000080	TCPWM0 Group #0, Counter #12
354	TCPWM0_GRP0_CNT13_CNT	0x40380680	0x00000080	TCPWM0 Group #0, Counter #13
355	TCPWM0_GRP0_CNT14_CNT	0x40380700	0x00000080	TCPWM0 Group #0, Counter #14
356	TCPWM0_GRP0_CNT15_CNT	0x40380780	0x00000080	TCPWM0 Group #0, Counter #15
357	TCPWM0_GRP0_CNT16_CNT	0x40380800	0x00000080	TCPWM0 Group #0, Counter #16
358	TCPWM0_GRP0_CNT17_CNT	0x40380880	0x00000080	TCPWM0 Group #0, Counter #17
359	TCPWM0_GRP0_CNT18_CNT	0x40380900	0x00000080	TCPWM0 Group #0, Counter #18
360	TCPWM0_GRP0_CNT19_CNT	0x40380980	0x00000080	TCPWM0 Group #0, Counter #19
361	TCPWM0_GRP0_CNT20_CNT	0x40380A00	0x00000080	TCPWM0 Group #0, Counter #20
362	TCPWM0_GRP0_CNT21_CNT	0x40380A80	0x00000080	TCPWM0 Group #0, Counter #21
363	TCPWM0_GRP0_CNT22_CNT	0x40380B00	0x00000080	TCPWM0 Group #0, Counter #22
364	TCPWM0_GRP0_CNT23_CNT	0x40380B80	0x00000080	TCPWM0 Group #0, Counter #23
365	TCPWM0_GRP0_CNT24_CNT	0x40380C00	0x00000080	TCPWM0 Group #0, Counter #24
366	TCPWM0_GRP0_CNT25_CNT	0x40380C80	0x00000080	TCPWM0 Group #0, Counter #25
367	TCPWM0_GRP0_CNT26_CNT	0x40380D00	0x00000080	TCPWM0 Group #0, Counter #26
368	TCPWM0_GRP0_CNT27_CNT	0x40380D80	0x00000080	TCPWM0 Group #0, Counter #27
369	TCPWM0_GRP0_CNT28_CNT	0x40380E00	0x00000080	TCPWM0 Group #0, Counter #28

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
370	TCPWM0_GRP0_CNT29_CNT	0x40380E80	0x00000080	TCPWM0 Group #0, Counter #29
371	TCPWM0_GRP0_CNT30_CNT	0x40380F00	0x00000080	TCPWM0 Group #0, Counter #30
372	TCPWM0_GRP0_CNT31_CNT	0x40380F80	0x00000080	TCPWM0 Group #0, Counter #31
373	TCPWM0_GRP0_CNT32_CNT	0x40381000	0x00000080	TCPWM0 Group #0, Counter #32
374	TCPWM0_GRP0_CNT33_CNT	0x40381080	0x00000080	TCPWM0 Group #0, Counter #33
375	TCPWM0_GRP0_CNT34_CNT	0x40381100	0x00000080	TCPWM0 Group #0, Counter #34
376	TCPWM0_GRP0_CNT35_CNT	0x40381180	0x00000080	TCPWM0 Group #0, Counter #35
377	TCPWM0_GRP0_CNT36_CNT	0x40381200	0x00000080	TCPWM0 Group #0, Counter #36
378	TCPWM0_GRP0_CNT37_CNT	0x40381280	0x00000080	TCPWM0 Group #0, Counter #37
379	TCPWM0_GRP1_CNT0_CNT	0x40388000	0x00000080	TCPWM0 Group #1, Counter #0
380	TCPWM0_GRP1_CNT1_CNT	0x40388080	0x00000080	TCPWM0 Group #1, Counter #1
381	TCPWM0_GRP1_CNT2_CNT	0x40388100	0x00000080	TCPWM0 Group #1, Counter #2
382	TCPWM0_GRP1_CNT3_CNT	0x40388180	0x00000080	TCPWM0 Group #1, Counter #3
383	TCPWM0_GRP1_CNT4_CNT	0x40388200	0x00000080	TCPWM0 Group #1, Counter #4
384	TCPWM0_GRP1_CNT5_CNT	0x40388280	0x00000080	TCPWM0 Group #1, Counter #5
385	TCPWM0_GRP1_CNT6_CNT	0x40388300	0x00000080	TCPWM0 Group #1, Counter #6
386	TCPWM0_GRP1_CNT7_CNT	0x40388380	0x00000080	TCPWM0 Group #1, Counter #7
387	TCPWM0_GRP1_CNT8_CNT	0x40388400	0x00000080	TCPWM0 Group #1, Counter #8
388	TCPWM0_GRP1_CNT9_CNT	0x40388480	0x00000080	TCPWM0 Group #1, Counter #9

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
389	TCPWM0_GRP1_CNT10_CNT	0x40388500	0x00000080	TCPWM0 Group #1, Counter #10
390	TCPWM0_GRP1_CNT11_CNT	0x40388580	0x00000080	TCPWM0 Group #1, Counter #11
391	TCPWM0_GRP2_CNT0_CNT	0x40390000	0x00000080	TCPWM0 Group #2, Counter #0
392	TCPWM0_GRP2_CNT1_CNT	0x40390080	0x00000080	TCPWM0 Group #2, Counter #1
393	TCPWM0_GRP2_CNT2_CNT	0x40390100	0x00000080	TCPWM0 Group #2, Counter #2
394	TCPWM0_GRP2_CNT3_CNT	0x40390180	0x00000080	TCPWM0 Group #2, Counter #3
395	TCPWM0_GRP2_CNT4_CNT	0x40390200	0x00000080	TCPWM0 Group #2, Counter #4
396	TCPWM0_GRP2_CNT5_CNT	0x40390280	0x00000080	TCPWM0 Group #2, Counter #5
397	TCPWM0_GRP2_CNT6_CNT	0x40390300	0x00000080	TCPWM0 Group #2, Counter #6
398	TCPWM0_GRP2_CNT7_CNT	0x40390380	0x00000080	TCPWM0 Group #2, Counter #7
399	TCPWM0_GRP2_CNT8_CNT	0x40390400	0x00000080	TCPWM0 Group #2, Counter #8
400	TCPWM0_GRP2_CNT9_CNT	0x40390480	0x00000080	TCPWM0 Group #2, Counter #9
401	TCPWM0_GRP2_CNT10_CNT	0x40390500	0x00000080	TCPWM0 Group #2, Counter #10
402	TCPWM0_GRP2_CNT11_CNT	0x40390580	0x00000080	TCPWM0 Group #2, Counter #11
403	TCPWM0_GRP2_CNT12_CNT	0x40390600	0x00000080	TCPWM0 Group #2, Counter #12
404	TCPWM0_GRP2_CNT13_CNT	0x40390680	0x00000080	TCPWM0 Group #2, Counter #13
405	TCPWM0_GRP2_CNT14_CNT	0x40390700	0x00000080	TCPWM0 Group #2, Counter #14
406	TCPWM0_GRP2_CNT15_CNT	0x40390780	0x00000080	TCPWM0 Group #2, Counter #15
407	TCPWM0_GRP2_CNT16_CNT	0x40390800	0x00000080	TCPWM0 Group #2, Counter #16

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
408	TCPWM0_GRP2_CNT17_CNT	0x40390880	0x00000080	TCPWM0 Group #2, Counter #17
409	TCPWM0_GRP2_CNT18_CNT	0x40390900	0x00000080	TCPWM0 Group #2, Counter #18
410	TCPWM0_GRP2_CNT19_CNT	0x40390980	0x00000080	TCPWM0 Group #2, Counter #19
411	TCPWM0_GRP2_CNT20_CNT	0x40390A00	0x00000080	TCPWM0 Group #2, Counter #20
412	TCPWM0_GRP2_CNT21_CNT	0x40390A80	0x00000080	TCPWM0 Group #2, Counter #21
413	TCPWM0_GRP2_CNT22_CNT	0x40390B00	0x00000080	TCPWM0 Group #2, Counter #22
414	TCPWM0_GRP2_CNT23_CNT	0x40390B80	0x00000080	TCPWM0 Group #2, Counter #23
415	TCPWM0_GRP2_CNT24_CNT	0x40390C00	0x00000080	TCPWM0 Group #2, Counter #24
416	TCPWM0_GRP2_CNT25_CNT	0x40390C80	0x00000080	TCPWM0 Group #2, Counter #25
417	TCPWM0_GRP2_CNT26_CNT	0x40390D00	0x00000080	TCPWM0 Group #2, Counter #26
418	TCPWM0_GRP2_CNT27_CNT	0x40390D80	0x00000080	TCPWM0 Group #2, Counter #27
419	TCPWM0_GRP2_CNT28_CNT	0x40390E00	0x00000080	TCPWM0 Group #2, Counter #28
420	TCPWM0_GRP2_CNT29_CNT	0x40390E80	0x00000080	TCPWM0 Group #2, Counter #29
421	TCPWM0_GRP2_CNT30_CNT	0x40390F00	0x00000080	TCPWM0 Group #2, Counter #30
422	TCPWM0_GRP2_CNT31_CNT	0x40390F80	0x00000080	TCPWM0 Group #2, Counter #31
423	EVTGEN0	0x403F0000	0x00001000	Event generator #0
424	SMIF0	0x40420000	0x00001000	Serial Memory Interface #0
425	SMIF1	0x40430000	0x00001000	Serial Memory Interface #1
426	ETH0	0x40480000	0x00010000	Ethernet0
427	LIN0_MAIN	0x40500000	0x00000008	LIN0, main
428	LIN0_CH0_CH	0x40508000	0x00000100	LIN0, Channel #0
429	LIN0_CH1_CH	0x40508100	0x00000100	LIN0, Channel #1

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
430	CXPIO_MAIN	0x40510000	0x00000008	CXPIO, main
431	CXPIO_CH0_CH	0x40518000	0x00000100	CXPIO, Channel #0
432	CXPIO_CH1_CH	0x40518100	0x00000100	CXPIO, Channel #1
433	CAN FD0_CH0_CH	0x40520000	0x00000200	CAN0, Channel #0
434	CAN FD0_CH1_CH	0x40520200	0x00000200	CAN0, Channel #1
435	CAN FD1_CH0_CH	0x40540000	0x00000200	CAN1, Channel #0
436	CAN FD1_CH1_CH	0x40540200	0x00000200	CAN1, Channel #1
437	CAN FD0_MAIN	0x40521000	0x00000100	CAN0 main
438	CAN FD1_MAIN	0x40541000	0x00000100	CAN1 main
439	CAN FD0_BUF	0x40530000	0x00010000	CAN0 buffer
440	CAN FD1_BUF	0x40550000	0x00010000	CAN1 buffer
441	SCB0	0x40600000	0x00010000	SCB0
442	SCB1	0x40610000	0x00010000	SCB1
443	SCB2	0x40620000	0x00010000	SCB2
444	SCB3	0x40630000	0x00010000	SCB3
445	SCB4	0x40640000	0x00010000	SCB4
446	SCB5	0x40650000	0x00010000	SCB5
447	SCB6	0x40660000	0x00010000	SCB6
448	SCB7	0x40670000	0x00010000	SCB7
449	SCB8	0x40680000	0x00010000	SCB8
450	SCB9	0x40690000	0x00010000	SCB9
451	SCB10	0x406A0000	0x00010000	SCB10
452	SCB11	0x406B0000	0x00010000	SCB11
453	TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX	0x40818000	0x00000100	TDM0 TX Structure #0
454	TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX	0x40818200	0x00000100	TDM0 TX Structure #1
455	TDM0_TDM_STRUCT2_TDM_TX_STRUCT_TX	0x40818400	0x00000100	TDM0 TX Structure #2
456	TDM0_TDM_STRUCT3_TDM_TX_STRUCT_TX	0x40818600	0x00000100	TDM0 TX Structure #3
457	TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX	0x40818100	0x00000100	TDM0 RX Structure #0
458	TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX	0x40818300	0x00000100	TDM0 RX Structure #1

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表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
459	TDM0_TDM_STRUCT2_TDM_RX_STRUCT_RX	0x40818500	0x00000100	TDM0 RX Structure #2
460	TDM0_TDM_STRUCT3_TDM_RX_STRUCT_RX	0x40818700	0x00000100	TDM0 RX Structure #3
461	SG0_SG_STRUCT0_TX	0x40828000	0x00000100	SG0 TX Structure #0
462	SG0_SG_STRUCT1_TX	0x40828100	0x00000100	SG0 TX Structure #1
463	SG0_SG_STRUCT2_TX	0x40828200	0x00000100	SG0 TX Structure #2
464	SG0_SG_STRUCT3_TX	0x40828300	0x00000100	SG0 TX Structure #3
465	SG0_SG_STRUCT4_TX	0x40828400	0x00000100	SG0 TX Structure #4
466	PWM0_MAIN	0x40830000	0x00000010	PW0 Main
467	PWM0_TX0_TX	0x40838000	0x00000100	PWM0 TX0
468	PWM0_TX1_TX	0x40838100	0x00000100	PWM0 TX1
469	DAC0_MAIN	0x40840000	0x00000100	DAC0 Main
470	MIXER0_MIXER_SRC_STRUCT0_SRC	0x40888000	0x00000100	MIXER0 Source Structure #0
471	MIXER0_MIXER_SRC_STRUCT1_SRC	0x40888100	0x00000100	MIXER0 Source Structure #1
472	MIXER0_MIXER_SRC_STRUCT2_SRC	0x40888200	0x00000100	MIXER0 Source Structure #2
473	MIXER0_MIXER_SRC_STRUCT3_SRC	0x40888300	0x00000100	MIXER0 Source Structure #3
474	MIXER0_MIXER_SRC_STRUCT4_SRC	0x40888400	0x00000100	MIXER0 Source Structure #4
475	MIXER1_MIXER_SRC_STRUCT0_SRC	0x40898000	0x00000100	MIXER1 Source Structure #0
476	MIXER1_MIXER_SRC_STRUCT1_SRC	0x40898100	0x00000100	MIXER1 Source Structure #1
477	MIXER1_MIXER_SRC_STRUCT2_SRC	0x40898200	0x00000100	MIXER1 Source Structure #2
478	MIXER1_MIXER_SRC_STRUCT3_SRC	0x40898300	0x00000100	MIXER1 Source Structure #3
479	MIXER1_MIXER_SRC_STRUCT4_SRC	0x40898400	0x00000100	MIXER1 Source Structure #4
480	MIXER0_MIXER_DST_STRUCT_DST	0x4088C000	0x00000100	MIXER0 Destination Structure
481	MIXER1_MIXER_DST_STRUCT_DST	0x4089C000	0x00000100	MIXER1 Destination Structure

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
482	PASS0_SAR0_SAR	0x40900000	0x00000400	PASS SAR0
483	PASS0_SAR1_SAR	0x40901000	0x00000008	PASS SAR1
484	PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR0, Channel #0
485	PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR0, Channel #1
486	PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR0, Channel #2
487	PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR0, Channel #3
488	PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR0, Channel #4
489	PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR0, Channel #5
490	PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR0, Channel #6
491	PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR0, Channel #7
492	PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR0, Channel #8
493	PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR0, Channel #9
494	PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR0, Channel #10
495	PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR0, Channel #11
496	PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR0, Channel #12
497	PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR0, Channel #13
498	PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR0, Channel #14
499	PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR0, Channel #15
500	PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR0, Channel #16
501	PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR0, Channel #17
502	PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR0, Channel #18
503	PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR0, Channel #19
504	PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR0, Channel #20
505	PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR0, Channel #21
506	PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR0, Channel #22
507	PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR0, Channel #23
508	PASS0_SAR0_CH24_CH	0x40900E00	0x00000040	SAR0, Channel #24
509	PASS0_SAR0_CH25_CH	0x40900E40	0x00000040	SAR0, Channel #25
510	PASS0_SAR0_CH26_CH	0x40900E80	0x00000040	SAR0, Channel #26
511	PASS0_SAR0_CH27_CH	0x40900EC0	0x00000040	SAR0, Channel #27
512	PASS0_SAR0_CH28_CH	0x40900F00	0x00000040	SAR0, Channel #28
513	PASS0_SAR0_CH29_CH	0x40900F40	0x00000040	SAR0, Channel #29
514	PASS0_SAR0_CH30_CH	0x40900F80	0x00000040	SAR0, Channel #30

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
515	PASS0_SAR0_CH31_CH	0x40900FC0	0x00000040	SAR0, Channel #31
516	PASS0_TOP	0x409F0000	0x00001000	PASS0 SAR main
517	VIDEOSS0_VCFG_VIDEOSS CFG	0x40A00000	0x00000400	VIDEOSS#0 Configuration
518	VIDEOSS0_VCFG_VRAM	0x40A00400	0x00000400	VIDEOSS#0 VRAM Configuration
519	VIDEOSS0_GPU_GFX2D	0x40A40000	0x00040000	VIDEOSS#0 Graphics 2D Core
520	VIDEOSS0_VIDEOIOCFG_VI RQ_VIDEOIOCFG	0x40A80020	0x00000020	VIDEOSS#0 I/O Configuration
521	VIDEOSS0_CAPIFC0_FRAM EDUMP	0x40A80400	0x00000400	VIDEOSS#0 Frame Dump Unit
522	VIDEOSS0_CAPIFC0_CAPE NG0	0x40A81000	0x00001000	VIDEOSS#0 Capture Engine#0
523	VIDEOSS0_DSPCFG_COMP ENGCFG	0x40A90000	0x00002000	VIDEOSS#0 Composition Engine Configuration
524	VIDEOSS0_DSPSEC0_CON STFRAME0	0x40A92000	0x00000400	VIDEOSS#0 Constant Frame#0 (Content)
525	VIDEOSS0_DSPSEC0_EXT DST0	0x40A92400	0x00000400	VIDEOSS#0 ExtDst#0 (Content)
526	VIDEOSS0_DSPPRIM0_CO NSTFRAME4	0x40A92800	0x00000400	VIDEOSS#0 Constant Frame#4 (Content)
527	VIDEOSS0_DSPPRIM0_EXT DST4	0x40A92C00	0x00000400	VIDEOSS#0 ExtDst#4 (Safety)
528	VIDEOSS0_DSPSEC1_CON STFRAME1	0x40A93000	0x00000400	VIDEOSS#0 Constant Frame#1 (Content)
529	VIDEOSS0_DSPSEC1_EXT DST1	0x40A93400	0x00000400	VIDEOSS#0 ExtDst#1 (Safety)
530	VIDEOSS0_DSPPRIM1_CO NSTFRAME5	0x40A93800	0x00000400	VIDEOSS#0 Constant Frame#5 (Safety)
531	VIDEOSS0_DSPPRIM1_EXT DST5	0x40A93C00	0x00000400	VIDEOSS#0 ExtDst#5 (Safety)
532	VIDEOSS0_CAPIFC0_EXTS RC4	0x40A94000	0x00000400	VIDEOSS#0 ExtSrc#4 (Capture)
533	VIDEOSS0_CAPIFC0_STOR E4	0x40A94400	0x00000400	VIDEOSS#0 Store#4 (Capture)
534	VIDEOSS0_DSPLAYER1_FE TCHLAYER0	0x40A94800	0x00000400	VIDEOSS#0 Fetch Layer#0 (Display)
535	VIDEOSS0_DSPLAYER2_FE TCHDECODE4	0x40A94C00	0x00000400	VIDEOSS#0 Fetch Decode#4 (Capture)

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
536	VIDEOSS0_DSPLAYER2_FE TCHECO4	0x40A95000	0x00000400	VIDEOSS#0 Fetch Eco#4 (Capture)
537	VIDEOSS0_DSPLAYER3_FE TCHWARP1	0x40A95800	0x00000400	VIDEOSS#0 Fetch Warp#1 (Display)
538	VIDEOSS0_DSPLAYER3_FE TCHECO1	0x40A95C00	0x00000400	VIDEOSS#0 Fetch Eco#1 (Display)
539	VIDEOSS0_DSPLAYER4_FE TCHLAYER1	0x40A96000	0x00000400	VIDEOSS#0 Fetch Layer#1 (Display)
540	VIDEOSS0_DSPLAYER5_FE TCHDECODE0	0x40A96400	0x00000400	VIDEOSS#0 Fetch Decode#0 (Display)
541	VIDEOSS0_DSPVPB_GAM MACOR4	0x40A96800	0x00000400	Video Processing Block #0 GammaCor (Capture)
542	VIDEOSS0_DSPVPB_MATR IX4	0x40A96C00	0x00000400	Video Processing Block #0 Matrix (Capture)
543	VIDEOSS0_DSPVPB_GPSC ALER4	0x40A97000	0x00000400	GPscaler #4 (Capture)
544	VIDEOSS0_DSPVPB_HIST OGRAM4	0x40A97400	0x00000400	Video Processing Block #0 Histogram (Capture)
545	VIDEOSS0_DSPBLEND1_L AYERBLEND1	0x40A97800	0x00000400	LayerBlend #1 (Display, Alpha Plane 1)
546	VIDEOSS0_DSPBLEND2_L AYERBLEND2	0x40A97C00	0x00000400	LayerBlend #2 (Display, Alpha Plane 2)
547	VIDEOSS0_DSPBLEND3_L AYERBLEND3	0x40A98000	0x00000400	LayerBlend #3 (Display, Alpha Plane 3)
548	VIDEOSS0_DSPBLEND4_L AYERBLEND4	0x40A98400	0x00000400	LayerBlend #4 (Display, Alpha Plane 4)
549	VIDEOSS0_DSPBLEND5_L AYERBLEND5	0x40A98800	0x00000400	LayerBlend #5 (Display, Alpha Plane 5)
550	VIDEOSS0_CAPIFC0_EXT SRC8	0x40A98C00	0x00000400	ExtSrc #8 (Display)
551	VIDEOSS0_DSPCFG0_DISE NGCFG0	0x40AA0000	0x00000400	VIDEOSS#0 Display Engine#0 Configuration
552	VIDEOSS0_DSPMON0_SIG 0	0x40AA1000	0x00000400	VIDEOSS#0 Display Engine#0 Signature Unit#0
553	VIDEOSS0_DSPCFG0_FRA MEGEN0	0x40AA2000	0x00000400	VIDEOSS#0 Display Engine#0 Frame Generator#0
554	VIDEOSS0_DSPCOL0_GAM MACOR0	0x40AA2400	0x00000400	VIDEOSS#0 Display Engine#0 Gamma Correction Unit#0

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
555	VIDEOSS0_DSPCOL0_DITHER0	0x40AA2800	0x00000400	VIDEOSS#0 Display Engine#0 Dither Unit#0
556	VIDEOSS0_DSPIFC0_TCON0	0x40AA3000	0x00000800	VIDEOSS#0 Display Engine#0 Timing Controller#0
557	VIDEOSS0_DSPCFG1_DISENGCFG1	0x40AA4000	0x00000400	VIDEOSS#0 Display Engine#1 Configuration
558	VIDEOSS0_DSPMON1_SIGNATURE1	0x40AA5000	0x00000400	VIDEOSS#0 Display Engine#1 Signature Unit#1
559	VIDEOSS0_DSPCFG1_FRAMEGEN1	0x40AA6000	0x00000400	VIDEOSS#0 Display Engine#1 Frame Generator
560	VIDEOSS0_DSPCOL1_GAMMACOR1	0x40AA6400	0x00000400	VIDEOSS#0 Display Engine#1 Gamma Correction Unit#1
561	VIDEOSS0_DSPCOL1_DITHER1	0x40AA6800	0x00000400	VIDEOSS#0 Display Engine#1 Dither Unit#1
562	VIDEOSS0_DSPIFC1_TCON1	0x40AA7000	0x00000800	VIDEOSS#0 Display Engine#1 Timing Controller#1
563	VIDEOSS0_DSPIFC0_FPDLINK0	0x40AC0000	0x00000400	VIDEOSS#0 Display interface0 FPD-Link#0
564	VIDEOSS0_MIPICSI0_MIPI CSI_STRUCT_MIPICSI_WRAPPER_MAIN	0x40AD0000	0x00000100	VIDEOSS#0 MIPICSI#0 D-PHY wrapper configuration and status
565	VIDEOSS0_MIPICSI0_MIPI CSI_STRUCT_MIPICSI_CORE_3PIP	0x40AD0200	0x00000080	VIDEOSS#0 MIPICSI#0 RX Core through APB interface
566	VIDEOSS0_VRPU_MAIN	0x40AF0000	0x00000080	VIDEOSS#0 VRPU Configuration
567	VIDEOSS0_GFX_MPU_RD0_MAIN	0x40AF4000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
568	VIDEOSS0_GFX_MPU_RD1_MAIN	0x40AF4400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
569	VIDEOSS0_GFX_MPU_RD2_MAIN	0x40AF4800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
570	VIDEOSS0_GFX_MPU_RD3_MAIN	0x40AF4C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
571	VIDEOSS0_GFX_MPU_RD4_MAIN	0x40AF5000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
572	VIDEOSS0_GFX_MPU_RD5_MAIN	0x40AF5400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
573	VIDEOSS0_GFX_MPU_RD6_MAIN	0x40AF5800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
574	VIDEOSS0_GFX_MPU_RD7_MAIN	0x40AF5C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
575	VIDEOSS0_GFX_MPU_RD8_MAIN	0x40AF6000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
576	VIDEOSS0_GFX_MPU_RD9_MAIN	0x40AF6400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
577	VIDEOSS0_GFX_MPU_RD10_MAIN	0x40AF6800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
578	VIDEOSS0_GFX_MPU_RD11_MAIN	0x40AF6C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
579	VIDEOSS0_GFX_MPU_RD12_MAIN	0x40AF7000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
580	VIDEOSS0_GFX_MPU_RD13_MAIN	0x40AF7400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
581	VIDEOSS0_GFX_MPU_RD14_MAIN	0x40AF7800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
582	VIDEOSS0_GFX_MPU_RD15_MAIN	0x40AF7C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
583	VIDEOSS0_GFX_MPU_WR0_MAIN	0x40AF8000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
584	VIDEOSS0_GFX_MPU_WR1_MAIN	0x40AF8400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
585	VIDEOSS0_GFX_MPU_WR2_MAIN	0x40AF8800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
586	VIDEOSS0_GFX_MPU_WR3_MAIN	0x40AF8C00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
587	VIDEOSS0_GFX_MPU_WR4_MAIN	0x40AF9000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
588	VIDEOSS0_GFX_MPU_WR5_MAIN	0x40AF9400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
589	VIDEOSS0_GFX_MPU_WR6_MAIN	0x40AF9800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
590	VIDEOSS0_GFX_MPU_WR7_MAIN	0x40AF9C00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
591	VIDEOSS0_GFX_MPU_WR8_MAIN	0x40AFA000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
592	VIDEOSS0_GFX_MPU_WR9_MAIN	0x40AFA400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters

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23 总线主控器
表 27 (续) PPU 固定结构配对

Pair number	PPU fixed structure pair	Address	Size	Description
593	VIDEOSS0_GFX_MPU_WR10_MAIN	0x40AFA800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
594	VIDEOSS0_GFX_MPU_WR11_MAIN	0x40AFAC00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
595	VIDEOSS0_GFX_MPU_WR12_MAIN	0x40AFB000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
596	VIDEOSS0_GFX_MPU_WR13_MAIN	0x40AFB400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
597	VIDEOSS0_GFX_MPU_WR14_MAIN	0x40AFB800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
598	VIDEOSS0_GFX_MPU_WR15_MAIN	0x40AFBC00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
599	PD_PD	0x40B00000	0x00000100	VIDEOSS#0 Power Domain Control

1) 固定 PPU 在启动 (Boot) 过程中完成配置, 用户不得更改此 PPU 的属性。

23 总线主控器

23 总线主控器

仲裁器（闪存控制器的一部分）根据主控标识符执行基于优先级的仲裁。每个总线主控都有一个专用的 4 位主控标识符。该主控标识符用于总线仲裁和 IPC 功能。

表 28 用于访问和保护控制的总线主控器

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for CM0+
1	CPUSS_MS_ID_CRYPT0	Master ID for Crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA0
9	CPUSS_MS_ID_FAST0	Master ID for External AXI Master 0 (Ethernet#0)
11	CPUSS_MS_ID_FAST2	Master ID for M-DMA1 (AXI DMA)
12	CPUSS_MS_ID_FAST3	Master ID for VIDEO Subsystem
14	CPUSS_MS_ID_CM7_0	Master ID for CM7_0
15	CPUSS_MS_ID_TC	Master ID for DAP Tap Controller

24 杂项配置
24 杂项配置
表 29 CYT3DL 器件的杂项配置

Sl. No.	Configuration	Number/ Instances	Description
0	SRSS_NUM_CLKPATH	11	Number of clock paths. One for each of FLL, PLL, Direct, and CSV
1	SRSS_NUM_HFROOT	14	Number of CLK_HFs present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_PERI_PCLK_PCLK_GROUP_NR	2	Number of asynchronous PCLK groups
4	PERI_PERI_PCLK_PCLK_GROUP_NR0_ GR_DIV_8_VECT	9	Group 0, Number of divide-by-8 clock dividers
5	PERI_PERI_PCLK_PCLK_GROUP_NR0_ GR_DIV_16_VECT	16	Group 0, Number of divide-by-16 clock dividers
6	PERI_PERI_PCLK_PCLK_GROUP_NR0_ GR_DIV_16_5_VECT	7	Group 0, Number of divide-by-16.5 clock dividers
7	PERI_PERI_PCLK_PCLK_GROUP_NR0_ GR_DIV_24_5_VECT	3	Group 0, Number of divide-by-24.5 clock dividers
8	PERI_PERI_PCLK_PCLK_GROUP_NR0_ GR_CLOCK_VECT	84	Group 0, Number of programmable clocks [1, 256]
9	PERI_PERI_PCLK_PCLK_GROUP_NR1_ GR_DIV_8_VECT	3	Group 1, Number of divide-by-8 clock dividers
10	PERI_PERI_PCLK_PCLK_GROUP_NR1_ GR_DIV_16_VECT	4	Group 1, Number of divide-by-16 clock dividers
11	PERI_PERI_PCLK_PCLK_GROUP_NR1_ GR_DIV_24_5_VECT	7	Group 1, Number of divide-by-24.5 clock dividers
12	PERI_PERI_PCLK_PCLK_GROUP_NR1_ GR_CLOCK_VECT	21	Group 1, Number of programmable clocks [1, 256]
13	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
14	CPUSS_CM7_0_FPU_LVL	2	CM7_0 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU
15	CPUSS_CM7_0_MPU_NR	16	Number of MPU regions in CM7_0
16	CPUSS_CM7_0_ICACHE_SIZE	16	CM7_0 Instruction cache (ICACHE) size in KB
17	CPUSS_CM7_0_DCACHE_SIZE	16	CM7_0 Data cache size (DCACHE) in KB
18	CPUSS_CM7_0_ITCM_SIZE	64	CM7_0 Instruction TCM (ITCM) size in KB
19	CPUSS_CM7_0_DTCM_SIZE	64	CM7_0 Data TCM (DTCM) size in KB
26	CPUSS_DW0_CH_NR	76	Number of P-DMA0 channels
27	CPUSS_DW1_CH_NR	84	Number of P-DMA1 channels

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24 杂项配置
表 29 (续) CYT3DL 器件的杂项配置

Sl. No.	Configuration	Number/ Instances	Description
28	CPUSS_DMACH_CH_NR	8	Number of M-DMA0 controller channels
29	CPUSS_CRYPTOBUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
30	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
31	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM7_0 access 2 - Reserved for DAP access Remaining for user purposes
32	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of SMPU protection structures
33	SCB0_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode
34	TCPWM_TR_ONE_CNT_NR	1	Number of input triggers per counter, routed to one counter
35	TCPWM_TR_ALL_CNT_NR	60	Number of input triggers routed to all counters, based on the pin package
36	TCPWM_GRP_NR	3	Number of TCPWM0 counter groups
37	TCPWM_GRP_NR0_GRP_GRP_CNT_NR	38	Number of counters per TCPWM0 Group #0
38	TCPWM_GRP_NR0_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #0
39	TCPWM_GRP_NR1_GRP_GRP_CNT_NR	12	Number of counters per TCPWM0 Group #1
40	TCPWM_GRP_NR1_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #1
41	TCPWM_GRP_NR2_GRP_GRP_CNT_NR	32	Number of counters per TCPWM0 Group #2
42	TCPWM_GRP_NR2_CNT_GRP_CNT_WIDTH	32	Counter width in number of bits per TCPWM0 Group #2
43	CAN FD0_MRAM_SIZE / CAN FD1_MRAM_SIZE	16	Message RAM size in KB shared by all the channels
44	EVTGEN_COMP_STRUCT_NR	16	Number of Event generator comparator structures

25 开发支持

CYT3DL 拥有丰富的文档、编程工具和在线资源来协助开发过程。可访问 www.infineon.cn 了解更多信息。

25.1 文档

一系列文档支持 CYT3DL，确保您能够快速找到问题的答案。本节列出了一些关键文档。

25.1.1 软件用户指南

使用示例驱动程序库以及第三方 IDE（例如 IAR EWARM 和 GHS Multi）的分步指南。

25.1.2 参考手册

技术参考手册 (TRM) 包含使用 CYT3DL 器件所需的所有技术细节，包括所有寄存器的完整描述。TRM 可在 www.infineon.cn 的文档部分找到。

25.2 工具

CYT3DL 受第三方开发工具生态系统（如 IAR 和 GHS）支持。英飞凌的编程工具也支持该器件，可使用英飞凌的 MiniProg4 或 Segger J-link 进行编程、擦除或读取。更多详细信息请参阅 www.infineon.cn 中的文档部分。

26 电气规格

26 电气规格

26.1 绝对最大额定值

如果在超出表 30 所列最小值和最大值限值范围的条件下使用该器件，可能会导致器件永久性损坏。即使在表 30 限值范围内，但长期处于超出正常工作条件的状态下，也可能影响器件的可靠性。根据 JEDEC 标准 JESD22-A103 《高温存储寿命》的规定，最大存储温度为 150 °C。当在表 30 规定的范围内但超出正常工作条件的情况下运行时，该器件可能无法达到规格要求。

功率考虑因素

芯片结温 (T_J) 的平均值 (单位: °C) 可通过公式 1 计算得出: $T_J = T_A + (P_D \times \theta_{JA})$

其中:

T_A 是环境温度, 单位为 °C。

θ_{JA} 是封装结点至环境的热阻, 单位为 °C/W。

P_D 是 P_{INT} 与 P_{IO} 之和 ($P_D = P_{INT} + P_{IO}$)。

P_{INT} 为芯片内部电源。 ($P_{INT} = V_{DDD} \times I_{DD} + V_{CCD} \times I_{CC} + V_{DDA} \times I_{VDDA}$)

P_{IO} 表示输入和输出引脚上的功耗; 由用户确定。

对于大多数应用, $P_{IO} < P_{INT}$ 可以被忽略。

另一方面, 如果器件配置为连续驱动外部模块和/或存储器, 则 P_{IO} 可能很重要。

- 警告:**
- 需要遵循推荐的工作条件来确保半导体器件的正常运行。当器件在这些条件下运行时, 器件的所有电气特性均得到保证。
 - 在这些条件之外的任何条件下运行, 都可能对设备的可靠性产生不利影响, 并可能导致设备故障。
 - 对于本数据表中未提及的任何使用、工作条件或组合, 不提供任何保证。如果您想在列出的条件以外的任何条件下运行器件, 请联系销售代表。

表 30 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID10	VDDD_ABS	Power supply voltage (VDDD) ^{1), 2)}	V _{SS} – 0.3	–	V _{SS} + 6.0	V	See Table 7 for assignment of ports to supply domains
SID10A	VDDIO_GPIO_ABS	Power supply voltage (VDDIO_GPIO) ²⁾	V _{SS} – 0.3	–	V _{SS} + 6.0	V	Applies to all VDDIO_GPIO sources (VDDIO_GPIO_1/2). See Table 7 for assignment of ports to supply domains

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID10B	VDDIO_SMC_ABS	Power supply voltage (VDDIO_SMC) ²⁾	$V_{SS} - 0.3$	–	$V_{SS} + 6.0$	V	See Table 7 for assignment of ports to supply domains
SID10C	VDDIO_HSIO_ABS	Power supply voltage (VDDIO_HSIO) ²⁾	$V_{SS} - 0.3$	–	$V_{SS} + 6.0$	V	See Table 7 for assignment of ports to supply domains
SID10F	VDDPLL_FPD0_ABS	Power supply voltage (VDDPLL_FPD0) ²⁾ . Supply for FPD-Link PLLs	$V_{SSA_FPD0} - 0.3$	–	$V_{SSA_FPD0} + 1.21$	V	
SID10G	VDDHA_FPD0_ABS	Power supply voltage (VDDHA_FPD0) ²⁾ . Supply for FPD-Link Drivers	$V_{SSA_FPD0} - 0.3$	–	$V_{SSA_FPD0} + 4.0$	V	
SID10H	VDDA_FPD0_ABS	Power supply voltage (VDDA_FPD0) ²⁾ . Core-supply for FPD-Link	$V_{SSA_FPD0} - 0.3$	–	$V_{SSA_FPD0} + 1.21$	V	
SID10J	VDDA_MIPI_ABS	Power supply voltage (VDDA_MIPI) ²⁾ . Supply for MIPI D-PHY	$V_{SSA_MIPI} - 0.3$	–	$V_{SSA_MIPI} + 1.21$	V	
SID45	VDDA_DAC_ABS	Power supply voltage (VDDA_DAC) ²⁾ . Supply for Audio DAC	$V_{SSA_DAC} - 0.3$	–	$V_{SSA_DAC} + 4.0$	V	
SID11	VDDA_ADC_ABS	Analog power supply voltage (VDDA_ADC) ²⁾ . Supply for SAR ADC	$V_{SSA_ADC} - 0.3$	–	$V_{SSA_ADC} + 6.0$	V	
SID12	VREFH_ABS	SAR Analog reference voltage, high ²⁾	$V_{SSA_ADC} - 0.3$	–	$V_{SSA_ADC} + 6.0$	V	$V_{REFH} \leq (V_{DDA_ADC} + 0.3 \text{ V})$
SID12A	VREFL_ABS	SAR Analog reference voltage, low ²⁾	$V_{SSA_ADC} - 0.3$	–	$V_{SSA_ADC} + 0.3$	V	
SID13	VCCD_ABS	Power supply voltage (VCCD)	$V_{SS} - 0.3$	–	$V_{SS} + 1.21$	V	
SID15A	VI_GPIO_ABS	Input voltage ²⁾	$V_{SS} - 0.5$	–	$V_{DDIO_GPIO} + 0.5$	V	See Table 7 for assignment of ports to supply domains
SID15B	VI_SMC_ABS	Input voltage ²⁾	$V_{SS} - 0.5$	–	$V_{DDIO_SMC} + 0.5$	V	See Table 7 for assignment of ports to supply domains
SID15C	VI_HSIO_ABS	Input voltage ²⁾	$V_{SS} - 0.5$	–	$V_{DDIO_HSIO} + 0.5$	V	See Table 7 for assignment of ports to supply domains
SID15F	VI_MIPI_ABS	Input voltage ²⁾	$V_{SSA_MIPI} - 0.3$	–	$V_{DDA_MIPI} + 0.3$	V	

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID16	$V_{I_ADC_ABS}$	Analog input voltage to ADC ²⁾	$V_{SSA_ADC} - 0.3$	–	$V_{DDA_ADC} + 0.3$	V	See Table 7 for assignment of ports to supply domains
SID17A	$V_{O_GPIO_ABS}$	Output voltage ²⁾	$V_{SS} - 0.3$	–	$V_{DDIO_GPIO} + 0.3$	V	See Table 7 for assignment of ports to supply domains
SID17B	$V_{O_SMC_ABS}$	Output voltage ²⁾	$V_{SS} - 0.3$	–	$V_{DDIO_SMC} + 0.3$	V	See Table 7 for assignment of ports to supply domains
SID17C	$V_{O_HSIO_ABS}$	Output voltage ²⁾	$V_{SS} - 0.3$	–	$V_{DDIO_HS} + 0.3$	V	See Table 7 for assignment of ports to supply domains
SID17G	$V_{O_FPD0_ABS}$	Output voltage ²⁾	$V_{SSA_FPD0} - 0.3$	–	$V_{DDA_FPD0} + 0.3$	V	
SID17H	$V_{O_PMIC_EN_ABS}$	Output voltage ²⁾	$V_{SS} - 0.3$	–	$V_{DDD} + 0.3$	V	For the pin PMIC_EN
SID18	$ I_{CLAMP_ABS} $	Maximum clamp current ^{3), 4), 5), 6)}	–5	–	5	mA	Applicable to general purpose I/O pins
SID18A	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to I/O pins in total for $V_{DDIO_GPIO_X}$
SID18B	$ I_{CLAMP_ABS} $	Maximum clamp current ^{3), 4), 5), 6)}	–52	–	52	mA	Applicable to SMC I/O pins
SID18C	ΣI_{CLAMP_ABS}	Total maximum clamp current	–624	–	624	mA	Applicable to SMC I/O pins clamping current occurred by sudden switching-off of inductive load (stepper motor coil) in total for V_{DDIO_SMC}
SID18D	$ I_{CLAMP_ABS} $	Maximum clamp current ^{3), 4), 5), 6)}	–5	–	5	mA	Applicable to HSIO_STDLN
SID18E	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to I/O pins in total for V_{DDIO_HSIO}
SID20	$I_{OL1_GPIO_ABS}$	LOW-level maximum output current for GPIO ⁷⁾	–	–	3.5	mA	Setting is 1 mA
SID21	$I_{OL2_GPIO_ABS}$	LOW-level maximum output current for GPIO ⁷⁾	–	–	7	mA	Setting is 2 mA
SID22	$I_{OL3_GPIO_ABS}$	LOW-level maximum output current for GPIO ⁷⁾	–	–	10	mA	Setting is 5 mA

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID22A	IOL4_GPIO_ABS	LOW-level maximum output current for GPIO ⁷⁾	–	–	10	mA	Setting is 6 mA
SID23A	IOL_PMIC_EN_ABS	Sink maximum current	–	–	4	mA	For the pin PMIC_EN. Required to add a current limiting series resistor of 1.25 kΩ –5 kΩ to the PMIC_EN output.
SID23B	Σ IOL_PMIC_EN_ABS	Sink average current	–	–	1	mA	For the pin PMIC_EN. The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio. The operation current period over the average current spec should be less than 100 ns. Required to add a current limiting series resistor of 1.25 kΩ –5 kΩ to the PMIC_EN output.
SID26	Σ IOL_GPIO_ABS	LOW-level total output current for GPIO ⁸⁾	–	–	50	mA	
SID26A	IOL_SMC_ABS	LOW-level maximum output current for SMC ⁹⁾	–	–	52	mA	Setting is 30 mA at –40°C
SID26B	Σ IOL_SMC_ABS	LOW-level total output current for SMC ¹⁰⁾	–	–	300	mA	25°C < T _A ≤ 105°C For S-grade devices
SID26B_125	Σ IOL_SMC_ABS	LOW-level total output current for SMC ¹⁰⁾	–	–	300	mA	25°C < T _A ≤ 125°C For E-grade devices

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID26I	Σ IOL_SMC_ABS	LOW-level total output current for SMC ⁽¹⁰⁾	–	–	450	mA	–40°C ≤ T _A ≤ 25°C
SID26E	IOL_FPD_ABS	LOW-level maximum output current for FPD-link ⁽¹¹⁾	–	–	24	mA	
SID26F	Σ IOL_FPD_ABS	LOW-level total output current for FPD-link ⁽¹²⁾	–	–	120	mA	
SID26G	IOL_HSIO_ABS	LOW-level maximum output current for HSIO ⁽¹³⁾	–	–	15	mA	
SID26H	Σ IOL_HSIO_ABS	LOW-level total output current for HSIO ⁽¹⁴⁾	–	–	150	mA	
SID27	IOH1_GPIO_ABS	HIGH-level maximum output current for GPIO ⁽⁷⁾	–	–	–3.5	mA	Setting is 1 mA
SID28	IOH2_GPIO_ABS	HIGH-level maximum output current for GPIO ⁽⁷⁾	–	–	–7	mA	Setting is 2 mA
SID29	IOH3_GPIO_ABS	HIGH-level maximum output current for GPIO ⁽⁷⁾	–	–	–10	mA	Setting is 5 mA
SID29A	IOH4_GPIO_ABS	HIGH-level maximum output current for GPIO ⁽⁷⁾	–	–	–10	mA	Setting is 6 mA
SID30A	IOH_PMIC_EN_ABS	Source maximum current	–	–	–4	mA	For the pin PMIC_EN. Required to add a current limiting series resistor of 1.25 kΩ - 5 kΩ to the PMIC_EN output.

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID30B	Σ IOH_PMIC_EN_ABS	Source average current	–	–	–1	mA	For the pin PMIC_EN. The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current $\times$ the operation ratio. The operation current period over the average current spec should be less than 100 ns. Required to add a current limiting series resistor of 1.25 k Ω - 5 k Ω to the PMIC_EN output.
SID33	Σ IOH1_GPIO_ABS	HIGH-level total output current for GPIO ⁽¹⁰⁾	–	–	–50	mA	
SID33A	IOH_SMC_ABS	HIGH-level maximum output current for SMC ⁽⁹⁾	–	–	–52	mA	Setting is 30 mA at –40°C
SID33B	Σ IOH_SMC_ABS	HIGH-level total output current for SMC ⁽¹⁰⁾	–	–	–300	mA	25°C < T _A ≤ 105°C For S-grade devices
SID33B_125	Σ IOH_SMC_ABS	HIGH-level total output current for SMC ⁽¹⁰⁾	–	–	–300	mA	25°C < T _A ≤ 125°C For E-grade devices
SID33I	Σ IOH_SMC_ABS	HIGH-level total output current for SMC	–	–	–450	mA	–40°C ≤ T _A ≤ 25°C
SID33E	IOH_FPD_ABS	HIGH-level maximum output current for FPD-link ⁽¹¹⁾	–	–	–24	mA	
SID33F	Σ IOH_FPD_ABS	HIGH-level total output current for FPDlink ⁽¹²⁾	–	–	–120	mA	

(表格续下页.....)

26 电气规格
表 30 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID33G	IOH_HSIO_AB S	HIGH-level maximum output current for HSIO ¹⁾	–	–	–15	mA	
SID33H	Σ IOH_HSIO_AB S	HIGH-level total output current for HSIO ¹⁴⁾	–	–	–150	mA	
SID34_2	P _D	Power dissipation	–	–	2500	mW	25°C < T _A ≤ 105°C For S-grade devices
SID34_2_125	P _D	Power dissipation	–	–	1400	mW	25°C < T _A ≤ 125°C (for E-grade devices) BGA-272: 1400 mW; TEQFP-216: 1600 mW, based on R _{th}
SID36	T _A	Operating ambient temperature	–40	–	105	°C	For S-grade devices
SID36_125	T _A	Operating ambient temperature	–40	–	125	°C	For E-grade devices
SID38	T _{STG}	Storage temperature	–55	–	150	°C	
SID39	T _J	Operating junction temperature	–40	–	150	°C	
SID39A	V _{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	
SID39B1	V _{ESD_CDM1}	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B2	V _{ESD_CDM2}	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	I _{LU}	The maximum pin current the device can tolerate before triggering a latch-up	–100	–	100	mA	

- 1) SAR ADC[x] 的每个逻辑通道都可以连接到任意 SAR ADC[x]_y 外部引脚。(x = 0, or 1, or 2 and y=0 to max 31)
- 2) 固定 PPU 在启动 (Boot) 过程中完成配置, 用户不得更改此 PPU 的属性。
- 3) 必须设置限流电阻, 确保 I/O 引脚的电流在任何时候 (包括电源瞬变期间) 都不会超过额定值。有关推荐电路的更多信息, 可参见图 10。
- 4) V_{DDD} 和 V_{DDIO} 必须有足够的负载或受到保护, 以防止它们被钳位电流拉出建议的工作范围。
- 5) 钳位电流可施加于表 16 所列引脚, 且只能在部件通电时施加。
- 6) 当满足条件²⁾, 1, 2. 以及 SID18/A/B/C/D/E 时, |ICLAMP_ABS| 将取代 V_{IA_ABS} 和 V_{I_ABS0}
- 7) 最大输出电流是流过任何一个 GPIO I/O 的峰值电流。
- 8) 总输出电流是流过所有 GPIO I/O (GPIO_STD 和 GPIO_ENH) 的最大电流。
- 9) 最大输出电流是流过任何一个 SMC I/O 的峰值电流。
- 10) 总输出电流是流过所有 SMC I/O (GPIO_SMC) 的最大电流。

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- 11) 最大输出电流是流过任何一个 FPD-link I/O 输出的峰值电流。
- 12) 总输出电流是流过所有 FPD-link I/O 输出的最大电流。
- 13) 最大输出电流是流过任何一个 HSIO I/O 的峰值电流。
- 14) 总输出电流是流过所有 HSIO I/O (HSIO_STDLN) 的最大电流。

注：

1. 确保 $V_{DDD} \geq (V_{DDIO_GPIO_1} - 0.3 V) \geq (V_{DDIO_GPIO_2} - 0.3 V)$ 。
2. 这些参数基于条件： $V_{SS} = V_{SSA_ADC} = V_{SSA_DAC} = V_{SSA_MIPI} = V_{SSA_FPD} = 0.0 V$ 。

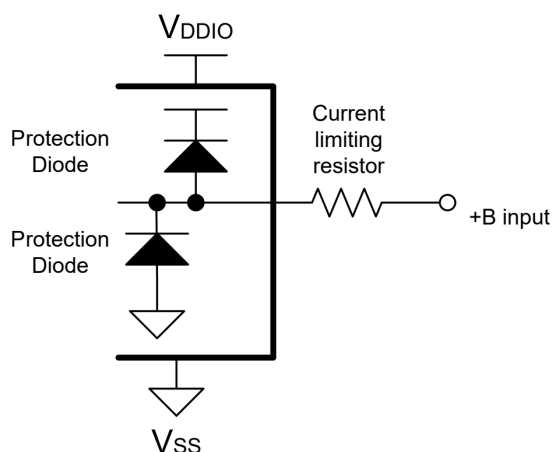


图 10 推荐电路示例¹⁹⁾

警告： 半导体器件可能因施加超过绝对最大额定值的压力（包括但不限于电压、电流或温度）而导致永久损坏。不要超过任何这些额定值。

26.2 推荐工作条件

表 31 器件级规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended operating conditions							
SID40	V_{DDD} , V_{DDA_ADC} , V_{DDIO_GPIO} , V_{DDIO_SMC} ,	Power supply voltage ¹⁾	2.7 ²⁾	–	5.5 ³⁾	V	V_{DDIO_GPIO} ($V_{DDIO_GPIO_1/2}$)
SID40A	V_{DDIO_EFP}	Power supply voltage for eFuse programming ⁴⁾	3.0	–	5.5	V	$V_{DDIO_GPIO_1}$ for this product, when programming eFuses
SID40B	V_{DDIO_HSIO}	Power supply voltage	3.0	3.3	3.6	V	

(表格续下页.....)

¹⁹⁾ +B 是电池正极电压，约为 45 V。

26 电气规格
表 31 (续) 器件级规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID40E	VDDPLL_FPD0 5)	Power supply voltage (V _{DDPLL_FPD0}). Supply for FPD-link PLLs.	1.09	1.15	1.21	V	
SID40F	VDDHA_FPD0	Power supply voltage (V _{DDHA_FPD0}). Supply for FPD-link line drivers.	3.0	3.3	3.6	V	
SID40G	VDDA_FPD0 5)	Power supply voltage (V _{DDA_FPD0}). Core-supply for FPD-link.	1.09	1.15	1.21	V	
SID40H	VDDA_MIPI 5)	Power supply voltage (V _{DDA_MIPI}). Supply for D-PHY.	1.09	1.15	1.21	V	
SID40J	VCCD 5)	External V _{CCD} power supply	1.09	1.15	1.21	V	External V _{CCD} power supply range when externally supplied at V _{CCD} . V _{CCD} must not be driven by an external supply at startup. See related application note for correct startup sequence.
SID41	CS1	Smoothing capacitor 6), 7)	30.8	94	103.4	μF	
SID43	VDDA_DAC	High voltage supply	3.0	3.3	3.6	V	

- 1) 当 SARMUX0 启用时, 确保 $V_{DDIO_GPIO_1} \geq 0.8 \times V_{DDA_ADC0}$
- 2) 支持 3.0 V $\pm 10\%$ 的电压范围, 提供较低的 BOD 设置选项。此设置可为内部时序提供稳健的保护, 但 BOD 复位会在电压低于指定工作条件时发生。可提供更高的 BOD 设置选项 (与低至 3.0 V 的电压一致), 确保满足所有运行条件。
- 3) 支持 5.0 V $\pm 10\%$ 的电压范围, 提供较高的 OVD 设置选项。此设置可为内部和接口时序提供稳健的保护, 但 OVD 复位会在电压高于指定工作条件时发生。可选择较低的 OVD 设置 (最高 5.0 V), 确保满足所有运行条件。允许 VDDDD 和 VDDA_ADC 电压过冲至更高的 OVD 设置范围, 但累计持续时间不得超过 2 小时。请注意, 在过冲电压条件下, 电气参数无法得到保证。
- 4) eFuse 编程必须在部件处于“安静”状态时进行, 尽量减少活动 (最好只有 JTAG 或单个 LIN/CAN 通道在 V_{DDDD} 域)。
- 5) 在 PCB 上短接的模拟和数字电源轨 (V_{DDPLL_FPD0} = V_{DDA_FPD0} = V_{DDA_MIPI} = V_{CCD})。这些电源轨必须连接到 V_{CCD} 的同一电源上。需要对该电源电压进行滤波, 以消除任何 PLL 抖动。建议使用噪声滤波器来降低 FPD-LINK 和 MIPI-PHY 电源的噪声纹波。
- 6) 每个芯片 (而非每个 VCCD 引脚) 都需要一个平滑电容器 CS1。VCCD 引脚必须连接在一起, 以确保低阻抗连接。(参见图 11 中的要求)。
- 7) 用于电源去耦或滤波的电容器在连续直流偏置下运行。许多使用直流电源的电容器提供的电容小于其目标电容, 并且其电容在其工作电压范围内不是恒定的。选择用于此设备的电容器时, 请确保所选组件在设计中使用的特定温度和电压工作条件下提供所需的电容。虽然温度系数通常可以在零件目录中找到 (例如 X7R、C0G、Y5V), 但匹配的电压系数可能仅在组件数据表上提供或直接从制造商处获得。在实际运行条件下使用不能提供所需电容的组件可能会导致器件运行不符合数据表规格。

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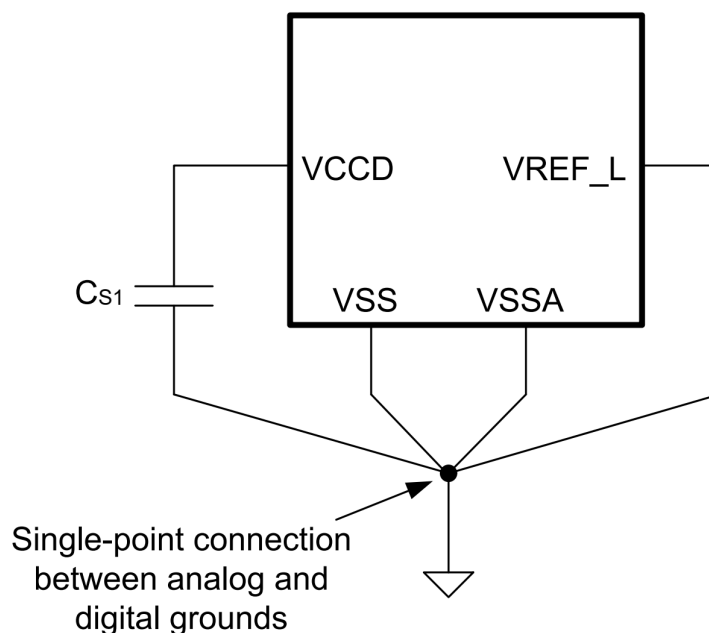


图 11 平滑电容器

注：平滑电容器应尽可能靠近VCCD 引脚放置。

表 32 直流规格、CPU电流和转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Execute with Flash							
SID51C	Icc1	V _{CCD} current in external PMIC mode	–	450	950	mA	Typ: T _A = 25°C, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 105°C, T _J = 150°C, V _{CCD} = 1.21 V, process worst (FF) (Maximum expected V _{CCD} when T _J = 150°C is reached due to self-heating) For S-grade devices

(表格续下页.....)

26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID51C_125	I _{CC1}	V _{CCD} current in external PMIC mode	–	450	950	mA	Typ: T _A = 25°C, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125°C, T _J = 150°C, V _{CCD} = 1.21 V, process worst (FF) (Maximum expected V _{CCD} when T _J = 150°C is reached due to self-heating); For E-grade devices
SID52C	I _{DD1}	V _{DDD} current in external PMIC mode, Use case with VIDEOSS (V _{DDD} current for SID51C use case)	–	7	10	mA	Cortex®-M7 at 240 MHz generated by PLL with ECO reference, executing Dhrystone from flash with cache enabled. Cortex®-M0+ is sleeping at 100 MHz. Graphics Engine at 200 MHz, operating 2D rendering, drawing, capture, output on 2 displays. All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are enabled. No I/O toggling. Typ: T _A = 25°C, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 105°C, V _{CCD} = 1.21 V, process worst (FF); For S-grade devices

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID52C_125	I _{DD1}	V _{DDD} current in external PMIC mode, Use case with VIDEOSS (V _{DDD} current for SID51C use case)	–	7	10	mA	Cortex®-M7 at 240 MHz generated by PLL with ECO reference, executing Dhrystone from flash with cache enabled. Cortex®-M0+ is sleeping at 100 MHz. Graphics Engine at 200 MHz, operating 2D rendering, drawing, capture, output on 2 displays. All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are enabled. No I/O toggling. Typ: T _A = 25°C, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125°C, V _{CCD} = 1.21 V, process worst (FF); For E-grade devices
SID56	I _{DD1}	V _{DDD} current in internal regulator mode, Execute from flash; Cortex®-M7 CPU in Active mode	–	8	38	mA	Cortex®-M7 at 8 MHz generated by IMO reference, executing Dhrystone from flash with cache enabled. Cortex®-M0+ is sleeping at 8 MHz. All clocks at 8MHz generated by IMO. VIDEOSS power switched off. All other peripherals, peripheral clocks, interrupts, CSV, DMA, PLL, ECO are disabled. No IO toggling. Typ: T _A = 25°C, V _{DDD} = 5.0 V, process typ (TT) Max: T _A = 85°C, V _{DDD} = 5.5 V, process worst (FF)

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明, 所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件, 以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID50A	I _{DD1}	V _{DDD} current in internal regulator mode. Cortex®-M7/M0+ CPUs in Sleep mode	–	28	70	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS power switched off. All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T _A = 25°C, V _{DDD} = 5.0 V, process typ (TT) Max: T _A = 85°C, V _{DDD} = 5.5 V, process worst (FF)
SID50C	I _{DD1}	V _{DDD} current in internal regulator mode. Cortex®-M7/M0+ CPUs in Sleep mode (room temp)	–	–	40	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS power switched off All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Max: T _A = 25°C, V _{DDD} = 5.5 V, process worst (FF)
SID50B	I _{CC1}	V _{CCD} current in external PMIC mode. Cortex®-M7/M0+ CPUs in Sleep mode. VIDEOSS in sleep mode (clocks off)	–	30	500	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS in sleep mode All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T _A = 25°C, V _{DDD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 105°C, V _{DDD} = 5.5 V, V _{CCD} = 1.21 V, process worst (FF); For S-grade devices

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID50B_125	I _{CC1}	V _{CCD} current in external PMIC mode. Cortex®-M7/M0+ CPUs in Sleep mode. VIDEOSS in sleep mode (clocks off)	–	30	500	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS in sleep mode All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T _A = 25°C, V _{DD} = 5.0 V, V _{CCD} = 1.15 V, process typ (TT) Max: T _A = 125°C, V _{DD} = 5.5 V, V _{CCD} = 1.21 V, process worst (FF); For E-grade devices

DeepSleep Mode

SID59_3	I _{DD_DS32A}	V _{DD} current in internal regulator mode. 32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode.	–	150	–	μA	DeepSleep Mode (RTC and EVTGEN operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain, CM7_1 power switched OFF Typ: T _A = 25°C, V _{DD} = 5.0 V, V _{CCD} = 1.1 V, process typ (TT) FPD-Link/MIPI Standby currents not included
SID59A_3	I _{DD_DS32A}	V _{DD} current in internal regulator mode. 32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode.	–	–	250	μA	DeepSleep Mode (RTC at 32kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain Max: V _{DD} = 5.5 V, T _A = 25°C, process worst (FF) FPD-Link/MIPI Standby currents not included

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID60_3	I _{DD_DS32B}	V _{DDD} current in internal regulator mode. 32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode.	–	–	2500	μA	DeepSleep Mode (RTC and Event generator operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain, CM7_1 power switched OFF Max: V _{DDD} = 5.5 V, T _A = 85°C, process worst (FF) FPD-Link/MIPI Standby currents not included
SID64_3	I _{DD_DS32C}	V _{DDD} current in internal regulator mode. 32 KB SRAM retention, ILO operation in DeepSleep mode.	–	50	2500	μA	DeepSleep Mode (RTC and Event generator operating, all other peripherals off, CAN MRAM disabled) CM0+ and CM7_0 retain, CM7_1 power switched OFF Typ: T _A = 25°C, V _{DDD} = 5.0 V, process typ (TT) Max: T _A = 85°C, V _{DDD} = 5.5 V, process worst (FF) FPD-Link/MIPI Standby currents not included
SID64A_3	I _{DD_DS32D}	32 KB SRAM retention, ILO operation in DeepSleep mode	–	–	150	μA	DeepSleep Mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) CM0+ and CM7_0 retain Max: T _A = 25°C, V _{DDD} = 5.5 V, process worst (FF) FPD-Link/MIPI Standby currents not included

Hibernate mode

SID66	I _{DD_HIB1}	V _{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	20	μA	T _A = 25°C using ILO, V _{DDD} = 5.0 V
SID66A	I _{DD_HIB2}	V _{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	40	μA	T _A = 25°C, using WCO, V _{DDD} = 5.0 V

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID66B	I _{DD_HIB3}	V _{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	75	μA	T _A = 85°C, using WCO, V _{DDD} = 5.5 V
SID66C	I _{DD_HIB4}	V _{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	150	μA	T _A = 25°C using LPECO 4 MHz, 20 pF load of LPECO V _{DDD} = 5.0 V
SID66D	I _{DD_HIB5}	V _{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	215	μA	T _A = 85°C, using LPECO 4 MHz, 20 pF load of LPECO V _{DDD} = 5.5 V
SID69_1	t _{ACT_DS}	Power down time from ACTIVE to DEEPSLEEP (using the internal regulator)	–	–	2.8	μs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID69A	t _{ACT_DS}	Power down time from ACTIVE to DeepSleep (using external PMIC)	–	–	6.5	μs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off. The time for the PMIC to deassert its power good signal is not included.
SID67	t _{DS_ACT}	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	26	μs	When using 8 MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T _A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID67A	t _{DS_ACT_FLL}	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	26	μs	When using FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. $T_A \geq -5^{\circ}\text{C}$ Note: At temperatures below -5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs
SID67B	t _{DS_ACT_PLL}	DeepSleep to Active transition time (PLL clock)	–	–	60	μs	When using PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until PLL locks. $T_A \geq -5^{\circ}\text{C}$ Note: At temperatures below -5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs
SID68C	t _{HIB_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	650	μs	Without boot runtime with max. 103.4 μF smoothing capacitor per SID41, no FPD/MIPI filter connected Guaranteed by Design
SID68D	t _{HIB_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	1040	μs	Without boot runtime with max. 103.4 μF smoothing capacitor per SID41 + max. 5x11 μF FPD/MIPI filter caps Guaranteed by Design
SID68A	t _{LVR_ACT}	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot	8	–	10	μs	Without boot runtime. Guaranteed by design

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID68B	tLVR_DS	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	μs	Without boot runtime. Guaranteed by design
SID79	tHIBWAKEUP_PW	Pulse width for wakeup from Hibernate mode on HIBERANTE_WAKEUP pins	90	–	–	ns	Guaranteed by design
SID80A	tRB_N	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	1700	μs	FAST_BOOT = 1, CM0+ clocked at 100 MHz
SID80B	tRB_S	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	2300	μs	FAST_BOOT = 1, CM0+ clocked at 100 MHz
SID81A	tFB	Flash boot startup time or wakeup time from hibernate in NORMAL/ SECURE protection state	–	–	190	μs	FAST_BOOT = 1, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms
SID81B	tFB_A	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	5000	μs	FAST_BOOT = 1, TOC2_FLAGS = 0x24F, CM0+ clocked at 100 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, APP size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K.

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26 电气规格
表 32 (续) DC 规格、CPU 电流及转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 的 S 级器件和 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 的 E 级器件，以及 2.7 V 至 5.5 V 的电压。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID81C	t _{FB_B}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	8150	μs	FAST_BOOT = 1, TOC2_FLAGS = 0x24F, CM0+ clocked at 100 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, APP size is 64 KB with the last 384 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA3K.

Regulator Specifications

SID600	V _{CCD}	Internal regulator core supply voltage (transient range)	1.05	1.1	1.15	V	
SID600A	V _{CCD_S}	Internal regulator core supply voltage (static range, no load)	1.07 5	1.1	1.12 5	V	Guaranteed by design
SID601	I _{DDD_ACT}	Regulator operating current in Active/Sleep mode	–	900	1500	μA	Guaranteed by design
SID602	I _{DDD_DPSLP}	Regulator operating current in DeepSleep mode	–	1.5	20	μA	Guaranteed by design
SID603	I _{RUSH}	In-rush current	–	–	850	mA	
SID604	I _{ILDOUT}	Internal regulator output current for operation	–	–	300	mA	
SID606	V _{IL}	PMIC digital input LOW voltage (%V _{DDD})	–	–	0.3 × V _{DDD}	V	
SID606A	V _{IH}	PMIC digital input HIGH voltage (%V _{DDD})	0.7 × V _{DDD}	–	–	V	
SID606B	V _{HYST}	PMIC digital input hysteresis (%V _{DDD})	0.05 × V _{DDD}	–	–	V	
SID607	V _{OL}	PMIC digital output LOW voltage	–	–	0.5	V	I _{OL} = 1 mA
SID607A	V _{OH}	PMIC digital output HIGH voltage	V _{DDD} – 0.5	–	–	V	I _{OH} = –1 mA

26 电气规格
26.3 复位规格
表 33 XRES_L 复位

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
XRES_L DC specifications							
SID73	I _{IDD_XRES}	I _{DD} when XRES_L asserted	–	–	1.7	mA	Max: T _A = 105°C, V _{DDD} = 5.5 V, process worst (FF); For S-grade devices
SID73_12 5	I _{IDD_XRES}	I _{DD} when XRES_L asserted	–	–	1.7	mA	Max: T _A = 125°C, V _{DDD} = 5.5 V, process worst (FF); For E-grade devices
SID74	V _{IH}	Input voltage high threshold	0.7 × V _{DDD}	–	–	V	CMOS Input
SID75	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DDD}	V	CMOS Input
SID76	R _{PULLUP}	Pull-up resistor	7	–	20	kΩ	
SID77	C _{IN}	Input capacitance	–	–	5	pF	
SID78	V _{HYSXRES}	Input voltage hysteresis	0.05 × V _{DDD}	–	–	V	
SID82	I _{DDIO_HSIO}	I _{DDIO_HSIO} when XRES_L is asserted	–	1.5	300	μA	Typ: T _A = 25°C, V _{DDIO_HSIO} = 3.3 V, process typ (TT) Max: T _A = 105°C, V _{DDIO_HSIO} = 3.6 V, process worst (FF); For S-grade devices
SID82_12 5	I _{DDIO_HSIO}	I _{DDIO_HSIO} when XRES_L is asserted	–	1.5	300	μA	Typ: T _A = 25°C, V _{DDIO_HSIO} = 3.3 V, process typ (TT) Max: T _A = 125°C, V _{DDIO_HSIO} = 3.6 V, process worst (FF); For E-grade devices
SID82_1	I _{DDIO_HSIO_1}	I _{DDIO_HSIO} when XRES_L is asserted	–	–	4.5	μA	Max: T _A = 25°C, V _{DDIO_HSIO} = 3.6 V, process worst (FF)
SID82_2	I _{DDIO_HSIO_2}	I _{DDIO_HSIO} when XRES_L is asserted	–	–	36	μA	Max: T _A = 85°C, V _{DDIO_HSIO} = 3.6 V, process worst (FF)

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26 电气规格
表 33 (续) XRES_L 复位

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID83	IDDIO_SMC	IDDIO_SMC when XRES_L is asserted	–	0.0 6	90	μA	Typ: T _A = 25°C, V _{DDIO_SMC} = 5.0 V, process typ (TT) Max: T _A = 105°C, V _{DDIO_SMC} = 5.5 V, process worst (FF); For S-grade devices
SID83_12 5	IDDIO_SMC	IDDIO_SMC when XRES_L is asserted	–	0.0 6	90	μA	Typ: T _A = 25°C, V _{DDIO_SMC} = 5.0 V, process typ (TT) Max: T _A = 125°C, V _{DDIO_SMC} = 5.5 V, process worst (FF); For E-grade devices
SID83_1	IDDIO_SMC_1	IDDIO_SMC when XRES_L is asserted	–	–	0.2	μA	Max: T _A = 25°C, V _{DDIO_SMC} = 5.5 V, process worst (FF)
SID83_2	IDDIO_SMC_2	IDDIO_SMC when XRES_L is asserted	–	–	3	μA	Max: T _A = 85°C, V _{DDIO_SMC} = 5.5 V, process worst (FF)
SID84	IDDIO_GPIO_1	IDDIO_GPIO_1 when XRES_L is asserted	–	0.0 5	40	μA	Typ: T _A = 25°C, V _{DDIO_GPIO_1} = 5.0 V, process typ (TT) Max: T _A = 105°C, V _{DDIO_GPIO_1} = 5.5 V, process worst (FF); For S-grade devices
SID84_12 5	IDDIO_GPIO_1	IDDIO_GPIO_1 when XRES_L is asserted	–	0.0 5	40	μA	Typ: T _A = 25°C, V _{DDIO_GPIO_1} = 5.0 V, process typ (TT) Max: T _A = 125°C, V _{DDIO_GPIO_1} = 5.5 V, process worst (FF); For E-grade devices
SID84_1	IDDIO_GPIO_1 _1	IDDIO_GPIO_1 when XRES_L is asserted	–	–	0.15	μA	Max: T _A = 25°C, V _{DDIO_GPIO_1} = 5.5 V, process worst (FF)
SID84_2	IDDIO_GPIO_1 _2	IDDIO_GPIO_1 when XRES_L is asserted	–	–	1.2	μA	Max: T _A = 85°C, V _{DDIO_GPIO_1} = 5.5 V, process worst (FF)

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26 电气规格
表 33 (续) XRES_L 复位

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID85	IDDIO_GPIO_2	IDDIO_GPIO_2 when XRES_L is asserted	–	0.05	50	μA	Typ: T _A = 25°C, V _{DDIO_GPIO_2} = 5.0 V, process typ (TT) Max: T _A = 105°C, V _{DDIO_GPIO_2} = 5.5 V, process worst (FF); For S-grade devices
SID85_125	IDDIO_GPIO_2	IDDIO_GPIO_2 when XRES_L is asserted	–	0.05	50	μA	Typ: T _A = 25°C, V _{DDIO_GPIO_2} = 5.0 V, process typ (TT) Max: T _A = 125°C, V _{DDIO_GPIO_2} = 5.5 V, process worst (FF); For E-grade devices
SID85_1	IDDIO_GPIO_2_1	IDDIO_GPIO_2 when XRES_L is asserted	–	–	0.15	μA	Max: T _A = 25°C, V _{DDIO_GPIO_2} = 5.5 V, process worst (FF)
SID85_2	IDDIO_GPIO_2_2	IDDIO_GPIO_2 when XRES_L is asserted	–	–	1.2	μA	Max: T _A = 85°C, V _{DDIO_GPIO_2} = 5.5 V, process worst (FF)

XRES_L AC specifications

SID70	txRES_ACT	XRES_L deasserted to Active transition time	–	–	265	μs	Without boot runtime. Guaranteed by design
SID71	txRES_PW	XRES_L pulse width	5	–	–	μs	
SID72	txRES_FT	Pulse suppression width	100	–	–	ns	

26 电气规格

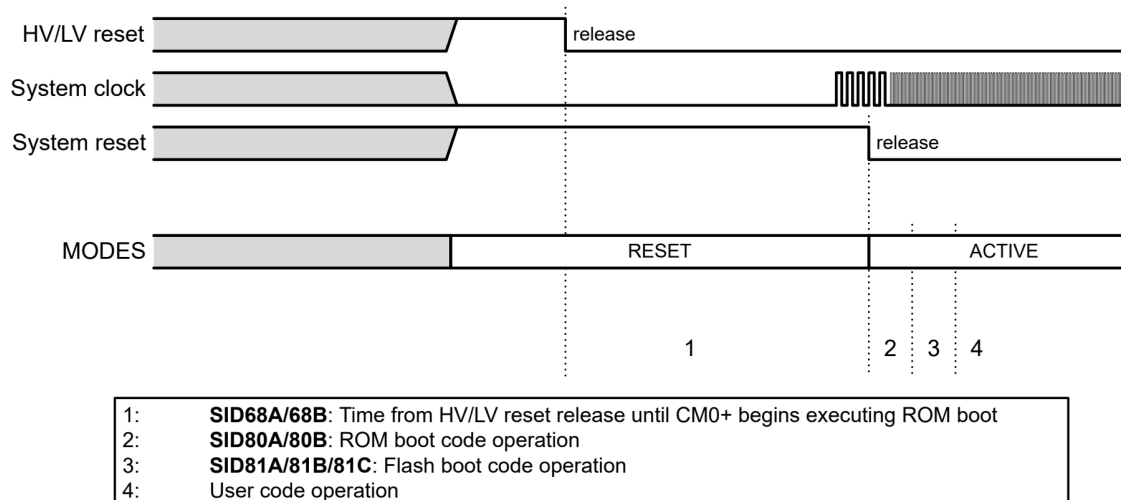


图 12 复位序列

26.4 I/O 规格

表 34 I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
GPIO_STD specifications (5-V I/Os, except GPIO_ENH)							
SID650	VOL1	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 V _{DDIO_GPIO} ≥ 4.5 V
SID651	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X V _{DDIO_GPIO} ≥ 4.5 V
SID651D	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID652	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 V _{DDIO_GPIO} ≥ 4.5 V

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26 电气规格
表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID652D	VoL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID653	VoL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 V _{DDIO_GPIO} ≥ 4.5 V
SID653D	VoL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID654	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 V _{DDIO_GPIO} ≥ 4.5 V
SID654D	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID655	VoH2	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b01 V _{DDIO_GPIO} ≥ 4.5 V
SID655D	VoH2	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b01 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID656	VOH3	Output voltage HIGH level	$V_{DDIO_GPIO} - 0.5$	–	–	V	$I_{OH} = -2 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b10 $V_{DDIO_GPIO} \geq 4.5 \text{ V}$
SID656D	VOH3	Output voltage HIGH level	$V_{DDIO_GPIO} - 0.5$	–	–	V	$I_{OH} = -1 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b10 $2.7 \text{ V} \leq V_{DDIO_GPIO} < 4.5 \text{ V}$
SID657	VOH4	Output voltage HIGH level	$V_{DDIO_GPIO} - 0.5$	–	–	V	$I_{OH} = -1 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b11 $V_{DDIO_GPIO} \geq 4.5 \text{ V}$
SID657D	VOH4	Output voltage HIGH level	$V_{DDIO_GPIO} - 0.5$	–	–	V	$I_{OH} = -0.5 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b11 $2.7 \text{ V} \leq V_{DDIO_GPIO} < 4.5 \text{ V}$
SID658	R _{PD}	Pull-down resistance	25	50	100	kΩ	–
SID659	R _{PU}	Pull-up resistance	25	50	100	kΩ	–
SID660	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	$0.7 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/ VTRIP_SEL<0:0> = 0b0
SID661	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/ VTRIP_SEL<0:0> = 0b1
SID662	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	$0.8 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b1 CFG_IN/ VTRIP_SEL<0:0> = 0b0 $4.5 \text{ V} \leq V_{DDIO_GPIO} \leq 5.5 \text{ V}$

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID663	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V _{DDIO_GPIO}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID664	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID665	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V _{DDIO_GPIO}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V
SID666	V _{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID668	V _{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V
SID669	C _{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670	I _{IL}	Input leakage current	–1	–	1	μA	V _{DDIO_GPIO_x} = V _{DDD} = V _{DDA_ADC} = 5.5 V, V _{SS} < V _I < V _{DDIO_GPIO_x} –40°C ≤ T _A ≤ 105°C This is valid for the pin which do not have ADC input functionality; For S-grade devices.

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID670_125	IIL	Input leakage current	-1	-	1	μA	$V_{DDIO_GPIO_x} = V_{DDD} = V_{DDA_ADC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{DDIO_GPIO_x}$ $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ This is valid for the pin which do not have ADC input functionality; For E-grade devices.
SID671	tr_F_FAST	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	-	10	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 20-pF load, entire V_{DDIO_GPIO} range
SID672	tr_F_FAST	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	-	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 50-pF load, entire V_{DDIO_GPIO} range, guaranteed by design
SID673	tr_F_FAST	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	-	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b01, 20-pF load, entire V_{DDIO_GPIO} range, guaranteed by design
SID674	tr_F_FAST	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	-	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b10, 10-pF load, entire V_{DDIO_GPIO} range, guaranteed by design
SID675	tr_F_FAST	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	-	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b11, 6-pF load, entire V_{DDIO_GPIO} range, guaranteed by design

GPIO_SMC specifications (Stepper Motor Control, 5-V I/Os)

SID650A	VOL2	Output voltage LOW level	-	-	0.6	V	$I_{OL} = 6\text{ mA}$ CFG_OUT/DRIVE_SEL<1:0> = 0b01 $V_{DDIO_SMC} \geq 4.5\text{ V}$
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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID651A	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b01 V _{DDIO_SMC} ≥ 4.5 V
SID651E	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b01 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID652A	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 V _{DDIO_SMC} ≥ 4.5 V
SID652E	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID653A	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 V _{DDIO_SMC} ≥ 4.5 V
SID653E	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 2.7 V ≤ V _{DDIO_SMC} < 4.5 V

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID653B	VOL5	Output voltage LOW level	–	–	0.5	V	$I_{OL} = 30 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 $25^{\circ}\text{C} < T_A \leq 105^{\circ}\text{C}$ $V_{DDIO_SMC} \geq 4.5 \text{ V}$ For S-grade devices
SID653B_1 25	VOL5	Output voltage LOW level	–	–	0.5	V	$I_{OL} = 30 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 $25^{\circ}\text{C} < T_A \leq 125^{\circ}\text{C}$ $V_{DDIO_SMC} \geq 4.5 \text{ V}$ For E-grade devices
SID653C	VOL5	Output voltage LOW level	–	–	0.5	V	$I_{OL} = 40 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 $-30^{\circ}\text{C} < T_A \leq 25^{\circ}\text{C}$ $V_{DDIO_SMC} \geq 4.5 \text{ V}$
SID653H	VOL5	Output voltage LOW level	–	–	0.5	V	$I_{OL} = 52 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 $-40^{\circ}\text{C} \leq T_A \leq -30^{\circ}\text{C}$ $V_{DDIO_SMC} \geq 4.5 \text{ V}$
SID654A	VOH2	Output voltage HIGH level	$V_{DDIO_SMC} - 0.5$	–	–	V	$I_{OH} = -5 \text{ mA}$ CFG_OUT/ DRIVE_SEL<1:0> = 0b01 $V_{DDIO_SMC} \geq 4.5 \text{ V}$

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID654E	VOH2	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOH = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b01 2.7 V ≤ VDDIO_SMC < 4.5 V
SID656A	VOH3	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOH = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 VDDIO_SMC ≥ 4.5 V
SID656E	VOH3	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOH = –1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 2.7 V ≤ VDDIO_SMC < 4.5 V
SID657A	VOH4	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOH = –1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 VDDIO_SMC ≥ 4.5 V
SID657E	VOH4	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOH = –0.5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 2.7 V ≤ VDDIO_SMC < 4.5 V
SID657B	VOH5	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	IOL = –30 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 25°C < TA ≤ 105°C VDDIO_SMC ≥ 4.5 V For S-grade devices

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID657B_1 25	VOH5	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	I _{OL} = –30 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 25°C < T _A ≤ 125°C VDDIO_SMC ≥ 4.5 V For E-grade devices
SID657C	VOH5	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	I _{OL} = –40 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –30°C < T _A ≤ 25°C VDDIO_SMC ≥ 4.5 V
SID657I	VOH5	Output voltage HIGH level	VDDIO_SMC – 0.5	–	–	V	I _{OL} = –52 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –40°C ≤ T _A ≤ –30°C VDDIO_SMC ≥ 4.5 V
SID658A	R _{PD}	Pull-down resistance	25	50	100	kΩ	
SID659A	R _{PU}	Pull-up resistance	25	50	100	kΩ	
SID659B	V _{OUT}	Mid range voltage level	2.45	–	2.55	V	CFG/ DRIVE_MODE<2:0> = 0b001
SID660A	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × VDDIO_SMC	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/ VTRIP_SEL<0:0> = 0b0
SID661A	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/ VTRIP_SEL<0:0> = 0b1

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID662A	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	$0.8 \times V_{DDIO_SMC}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_SMC} \leq 5.5\text{ V}$
SID663A	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	$0.3 \times V_{DDIO_SMC}$	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID664A	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID665A	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	$0.5 \times V_{DDIO_SMC}$	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_SMC} \leq 5.5\text{ V}$
SID666A	V _{HYST_CMOS}	Hysteresis in CMOS mode	$0.05 \times V_{DDIO_SMC}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID668A	V _{HYST_AUTO}	Hysteresis in AUTO mode	$0.05 \times V_{DDIO_SMC}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_SMC} \leq 5.5\text{ V}$
SID669A	C _{IN}	Input pin capacitance	–	–	7	pF	Test condition: 10/100MHz
SID670A	I _{IL}	Input leakage current	–2	–	2	μA	$V_{DDIO_SMC} = V_{DDD} = 5.5\text{ V}$, $V_{SS} < V_I < V_{DDIO_SMC}$ $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ This is valid for the pin which do not have ADC input functionality; For S-grade devices

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID670A_1 25	I _{IL}	Input leakage current	-2	-	2	μA	V _{DDIO_SMC} = V _{DDD} = 5.5 V, V _{SS} < V _I < V _{DDIO_SMC} -40°C ≤ T _A ≤ 125°C This is valid for the pin which do not have ADC input functionality; For E-grade devices
SID673A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	-	20	ns	5 mA drive strength 20-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b01, CFG_OUT/ SLOW<0:0> = 0b0, guaranteed by design
SID674A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	-	20	ns	2 mA drive strength 10-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b10, CFG_OUT/ SLOW<0:0> = 0b0, guaranteed by design
SID675A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	-	20	ns	1 mA drive strength 6-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b11, CFG_OUT/ SLOW<0:0> = 0b0, guaranteed by design
SID676A	t _{R_F_SMC_SLOW}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	15	-	80	ns	30 mA drive strength No load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676B	t _{R_F_SMC_SLOW}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	25	-	100	ns	30 mA drive strength 85-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/ SLOW<0:0> = 0b1

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID676C	tr_F_SMC_SLOW	Rise time or fall time (10% to 90% of VDDIO_SMC)	100	–	200	ns	30 mA drive strength 2.7-nF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/ SLOW<0:0> = 0b1

GPIO_ENH Specifications

SID650C	VOL1	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X VDDIO_GPIO ≥ 4.5 V
SID650D	VOL1	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X VDDIO_GPIO ≥ 4.5 V
SID651C	VOL1	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X 2.7 V ≤ VDDIO_GPIO < 4.5 V
SID652C	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 VDDIO_GPIO ≥ 4.5 V
SID652F	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 2.7 V ≤ VDDIO_GPIO < 4.5 V
SID653F	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 VDDIO_GPIO ≥ 4.5 V

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID653G	Vol4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID654C	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X V _{DDIO_GPIO} ≥ 4.5 V
SID654G	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b0X 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID655C	VoH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 V _{DDIO_GPIO} ≥ 4.5 V
SID656C	VoH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b10 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID657G	VoH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 V _{DDIO_GPIO} ≥ 4.5 V
SID657H	VoH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –0.5 mA CFG_OUT/ DRIVE_SEL<1:0> = 0b11 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID658C	R _{PD}	Pull-down resistance	25	50	100	kΩ	

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Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID659C	RPU	Pull-up resistance	25	50	100	kΩ	
SID660C	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	$0.7 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID661C	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID662C	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	$0.8 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_GPIO} \leq 5.5\text{ V}$
SID663C	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	$0.3 \times V_{DDIO_GPIO}$	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID664C	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID665C	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	$0.5 \times V_{DDIO_GPIO}$	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_GPIO} \leq 5.5\text{ V}$
SID666C	V _{HYST_CMOS}	Hysteresis in CMOS mode	$0.05 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID668C	V _{HYST_AUTO}	Hysteresis in AUTO mode	$0.05 \times V_{DDIO_GPIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b0 $4.5\text{ V} \leq V_{DDIO_GPIO} \leq 5.5\text{ V}$

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表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID669C	C _{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670C	I _{IL}	Input leakage current	–1	–	1	μA	V _{DDIO_GPIO} = V _{DDD} = 5.5 V, V _{SS} < V _I < V _{DDIO_GPIO} –40°C ≤ T _A ≤ 105°C For S-grade devices
SID670C_1 25	I _{IL}	Input leakage current	–1	–	1	μA	V _{DDIO_GPIO} = V _{DDD} = 5.5 V, V _{SS} < V _I < V _{DDIO_GPIO} –40°C ≤ T _A ≤ 125°C For E-grade devices
SID671C	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	10	ns	20-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/ SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range
SID672C	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	50-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range, guaranteed by design
SID673C	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	20-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b01, CFG_OUT/ SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range, guaranteed by design
SID674C	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	10-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b10, CFG_OUT/ SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range, guaranteed by design

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26 电气规格
表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID675C	tr_F_FAST	Rise time or fall time (10% to 90% of VDDIO_GPIO)	1	–	20	ns	6-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b11, CFG_OUT/ SLOW<0:0> = 0b0, entire VDDIO_GPIO range, guaranteed by design
SID676E	tf_I2C_SLOW	Fall time (30% to 70% of VDDIO_GPIO)	20 × (VDDIO_GPIO / 5.5)	–	250	ns	10-pF to 400-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, minimum R _{PU} = 400 Ω
SID677C	tr_F_SLOW	Rise time or fall time (10% to 90% of VDDIO_GPIO)	20 × (VDDIO_GPIO / 5.5)	–	160	ns	20-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/ SLOW<0:0> = 0b1, output frequency = 1 MHz
SID678C	tr_F_SLOW	Rise time or fall time (10% to 90% of VDDIO_GPIO)	20 × (VDDIO_GPIO / 5.5)	–	250	ns	400-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/ SLOW<0:0> = 0b1, output frequency = 400 kHz guaranteed by design

HSIO_STDLN Specifications (3 V I/Os)

SID650E	Vol0	Output LOW voltage level	–	–	0.4	V	I _{OL} = 10 mA CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b000
SID651F	Vol0	Output LOW voltage level	–	–	0.2	V	I _{OL} = 0.1 mA CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b000

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26 电气规格
表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID654I	VOL1	Output LOW voltage level	–	–	0.4	V	$I_{OL} = 10 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b001 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID655G	VOL2	Output LOW voltage level	–	–	0.4	V	$I_{OL} = 2 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b010 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID656G	VOL3	Output LOW voltage level	–	–	0.4	V	$I_{OL} = 1 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b011 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID656H	VOL4	Output LOW voltage level	–	–	0.4	V	$I_{OL} = 0.5 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b100 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID657J	VOH0	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -10 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b000
SID658D	VOH0	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.2$	–	–	V	$I_{OH} = -0.1 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b000
SID661F	VOH1	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -10 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b001 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$

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26 电气规格
表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID662F	VOH2	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -2 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b010 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID663E	VOH3	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -1 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b011 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID663F	VOH4	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -0.5 \text{ mA}$ CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b100 $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID664D	RPD	Pull-down resistance	25	50	100	kΩ	
SID665F	RPU	Pull-up resistance	25	50	100	kΩ	
SID665H	VIH3	Input Voltage HIGH threshold	1.7	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID667G	VIH0	Input Voltage HIGH threshold	$0.7 \times V_{DDIO_HSIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID667I	VIH1	Input Voltage HIGH threshold	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID667H	VIL3	Input Voltage LOW threshold	–	–	0.9	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/ VTRIP_SEL<0:0>= 0b1

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26 电气规格
表 34 (续) I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID671F	V _{IL0}	Input Voltage LOW threshold	–	–	0.3 × V _{DDIO_HSIO}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID671G	V _{IL1}	Input Voltage LOW threshold	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b1
SID674D	V _{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V _{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/ VTRIP_SEL<0:0>= 0b0
SID675D	C _{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID676H	I _{IL12}	Input leakage current	–1	–	1	μA	V _{DDIO_HSIO} = 3.6 V, V _{SS} < V _I < V _{DDIO_HSIO} –40°C ≤ T _A ≤ 105°C For S-grade devices
SID676H_1 25	I _{IL12}	Input leakage current	–1	–	1	μA	V _{DDIO_HSIO} = 3.6 V, V _{SS} < V _I < V _{DDIO_HSIO} –40°C ≤ T _A ≤ 125°C For E-grade devices

GPIO 输入规格

SID98	t _{FT}	Analog glitch filter (pulse suppression width)	–	–	50 ¹⁾	ns	One filter per port group (required for some I ² C speeds)
SID99	t _{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

1) 如果需要更长的脉冲抑制宽度，请使用智能 I/O。

26 电气规格

26.5 模拟外设

26.5.1 SAR ADC

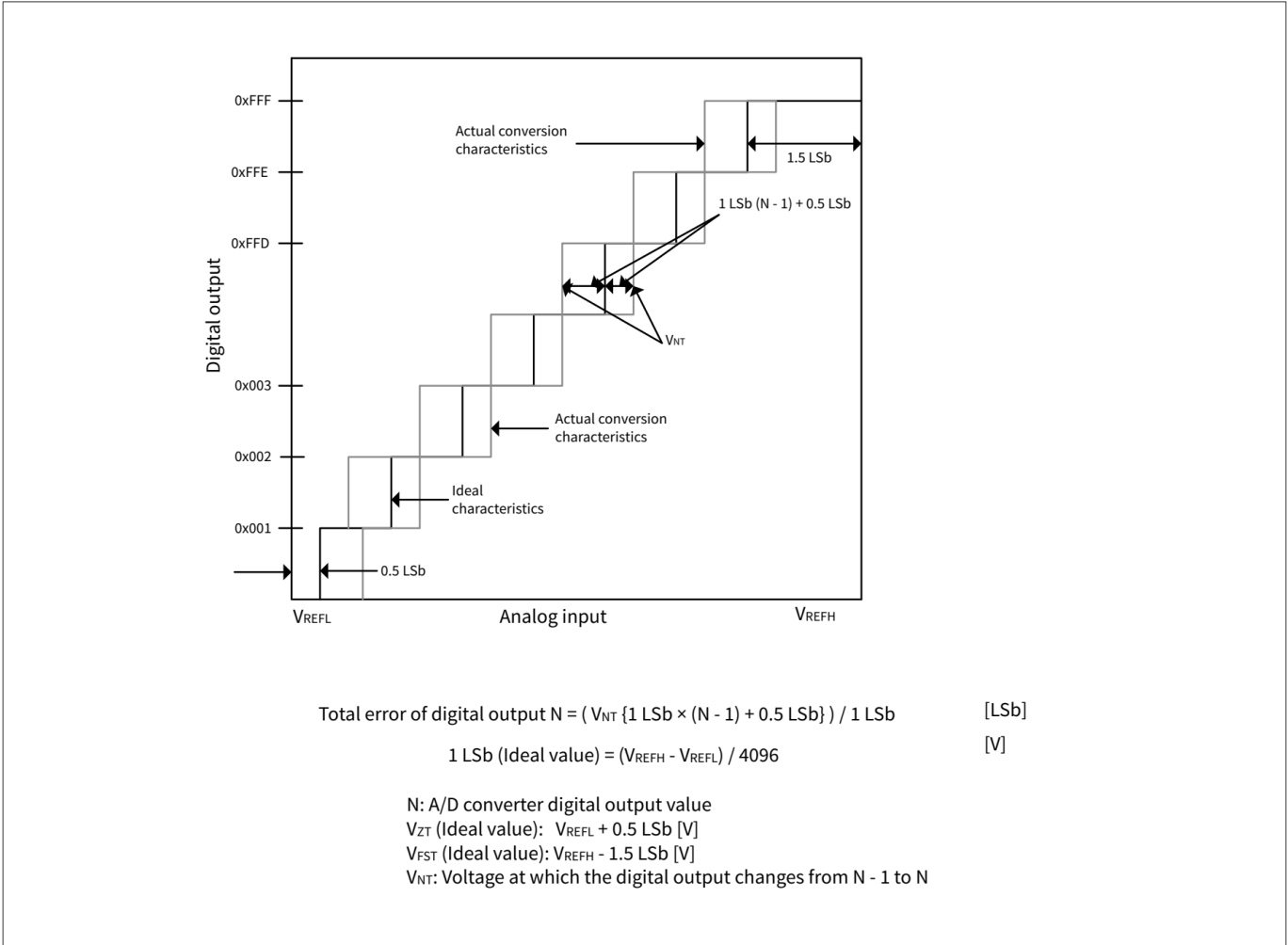
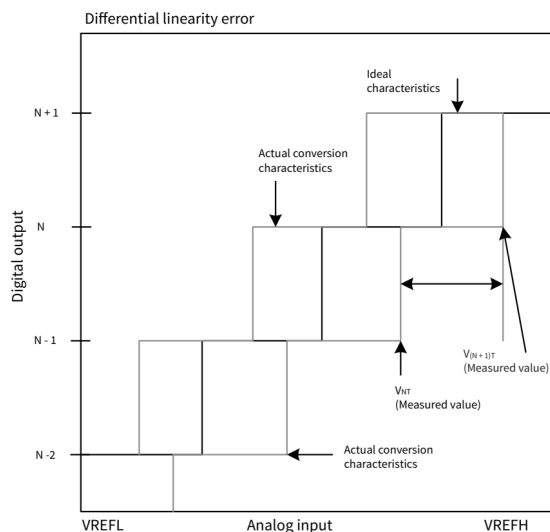
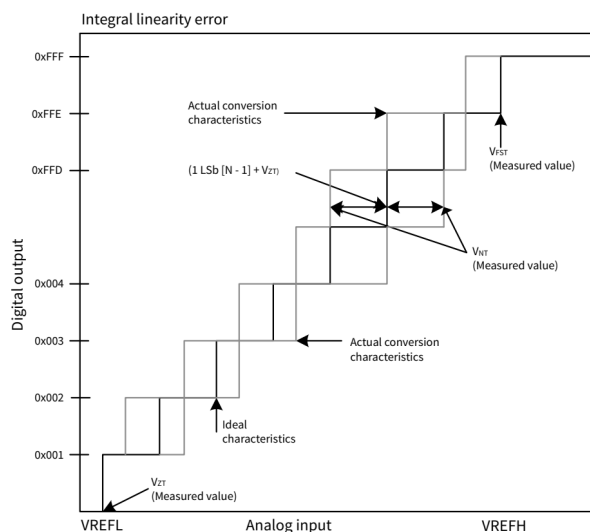


图 13 ADC 特性和误差描述

表 35 12 位 SAR ADC DC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	–	–	12	bits	
SID101	VA_INV	Input voltage range	V _{REFL}	–	V _{REFH}	V	
SID102	VREFH	SAR ADC HIGH reference voltage range	2.7	–	V _{DDA_ADC}	V	ADC performance degrades when high reference is higher than supply
SID103	VREFL	SAR ADC LOW reference voltage range	V _{VSSA_ADC}	–	V _{VSSA_ADC}	V	ADC performance degrades when low reference is lower than ground
SID103A	VBAND_GAP	Internal band gap reference voltage	0.882	0.9	0.918	V	

26 电气规格



$$\text{Integral linearity error of digital output } N = (V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{ZT}\}) / 1 \text{ LSB} \quad [\text{LSb}]$$

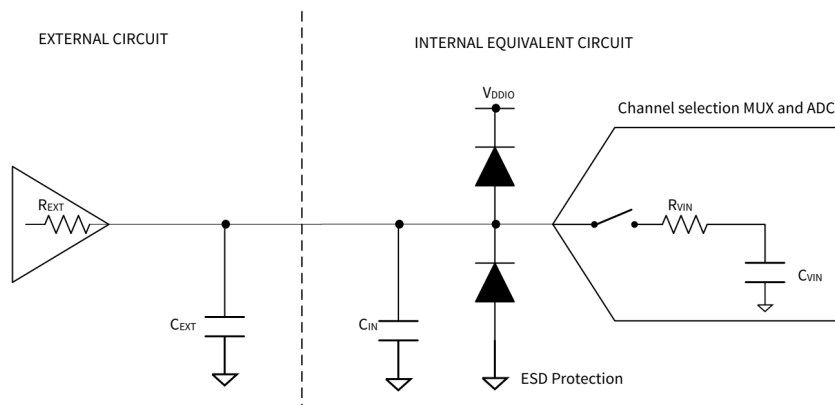
$$\text{Differential linearity error of digital output } N = (V_{(N+1)T} - V_{NT} - 1 \text{ LSB}) / 1 \text{ LSB} \quad [\text{LSb}]$$

$$1 \text{ LSB} = (V_{FST} - V_{ZT}) / 4094 \quad [\text{V}]$$

V_{ZT} : Voltage for which digital output changes from 0x000 to 0x001

V_{FST} : Voltage for which digital output changes from 0xFFE to 0xFFFF

图 14 积分和微分线性误差



R_{EXT} : Source impedance
 C_{EXT} : On-PCB capacitance
 C_{IN} : I/O pad or Input capacitance
 R_{VIN} : ADC equivalent input resistance
 C_{VIN} : ADC equivalent input capacitance
 K : Constant for sampling accuracy, $K = \ln(\text{abs}(4096/\text{LSb}_{\text{SAMPLE}}))$

Sampling Time (t_{SAMPLE}) requirement is shown in the following equation
 $t_{\text{SAMPLE}} > K \times \{ C_{VIN} \times (R_{VIN} + R_{EXT}) + (C_{IN} + C_{EXT}) \times (R_{EXT}) \}$ [seconds]

$K = 9.0$ is recommended to get ± 0.5 LSB sampling accuracy at 12-bit ($\text{LSb}_{\text{SAMPLE}} = \pm 0.5$)

图 15 ADC模拟输入等效电路

26 电气规格

表 36 SAR ADC 交流规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V _{ZT}	Zero transition voltage	-20	–	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T _A ≤ 105°C before offset adjustment; For S-grade devices
SID104_125	V _{ZT}	Zero transition voltage	-20	–	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T _A ≤ 125°C before offset adjustment; For E-grade devices
SID105	V _{FST}	Full-scale transition voltage	-20	–	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T _A ≤ 105°C before offset adjustment; For S-grade devices
SID105_125	V _{FST}	Full-scale transition voltage	-20	–	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T _A ≤ 125°C before offset adjustment; For E-grade devices
SID114	f _{ADC}	ADC operating frequency	2	–	26.67	MHz	
SID113	ts_4P5	Analog input sample time (4.5 V ≤ V _{DDA_ADC}) for channels of SARMUX0	412	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113A	ts_2P7	Analog input sample time (2.7 V ≤ V _{DDA_ADC}) for channels of SARMUX0	824	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113B	ts_DR_4P5	Analog input sample time when input is from diagnostic reference (4.5 V ≤ V _{DDA_ADC})	2	–	–	μs	Guaranteed by design
SID113C	ts_DR_2P7	Analog input sample time when input is from diagnostic reference (2.7 V ≤ V _{DDA_ADC})	2.5	–	–	μs	Guaranteed by design
SID113D	ts_TS	Analog input sample time for temperature sensor	7	–	–	μs	Guaranteed by design

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26 电气规格
表 36 (续) SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID106	t _{ST1}	Max throughput (sample per second) for channels of SARMUX0	–	–	1	Msp/s	4.5 V ≤ V _{DDA_ADC} ≤ 5.5 V, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles
SID106A	t _{ST2}	Max throughput (sample per second) for channels of SARMUX0	–	–	0.5	Msp/s	2.7 V ≤ V _{DDA_ADC} < 4.5 V 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID107	C _{VIN}	ADC input sampling capacitance	–	–	4.8	pF	Guaranteed by design
SID108	R _{VIN1}	Input path ON resistance (4.5 V to 5.5 V)	–	–	9.4	kΩ	Guaranteed by design
SID108A	R _{VIN2}	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	R _{DREF1}	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	R _{DREF2}	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	
SID109	A _{TE}	Total error	–5	–	5	LSb	V _{DDA_ADC} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA_ADC} –40°C ≤ T _A ≤ 105°C Total error after offset and gain adjustment at 12-bit resolution mode; For S-grade devices
SID109_125	A _{TE}	Total error	–5	–	5	LSb	V _{DDA_ADC} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA_ADC} –40°C ≤ T _A ≤ 125°C Total error after offset and gain adjustment at 12-bit resolution mode; For E-grade devices

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26 电气规格
表 36 (续) SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID109A	A_TEB	Total error	-12	-	12	LSb	$V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $V_{REFL} = V_{SSA_ADC}$ $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ Total Error before offset and gain adjustment at 12-bit resolution mode; For S-grade devices
SID109A_125	A_TEB	Total error	-12	-	12	LSb	$V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $V_{REFL} = V_{SSA_ADC}$ $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ Total Error before offset and gain adjustment at 12-bit resolution mode; For E-grade devices
SID110	A_INL	Integral nonlinearity	-2.5	-	2.5	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$; For S-grade devices
SID110_125	A_INL	Integral nonlinearity	-2.5	-	2.5	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; For E-grade devices
SID111	A_DNL	Differential nonlinearity	-0.99	-	1.9	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID111_125	A_DNL	Differential nonlinearity	-0.99	-	1.9	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID112	A_GE	Measure the ADC output with input switching through all input channels of one ADC	-7	-	7	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID112_125	A_GE	Measure the ADC output with input switching through all input channels of one ADC	-7	-	7	LSb	$V_{DDA_ADC} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115	I _{AIC}	Analog input leakage current (GPIO_STD)	-350	-	350	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices

(表格续下页.....)

26 电气规格
表 36 (续) SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID115_125	IAIC	Analog input leakage current (GPIO_STD)	-350	-	350	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115B	IAIC	Analog input leakage current (GPIO_ENH)	-700	-	700	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID115B_125	IAIC	Analog input leakage current (GPIO_ENH)	-700	-	700	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115D	IAIC	Analog input leakage current (GPIO_SMC)	-1075	-	1075	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID115D_125	IAIC	Analog input leakage current (GPIO_SMC)	-1075	-	1075	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115A	IAIC2	Analog input leakage current (GPIO_STD)	-	-	165	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID115A_125	IAIC2	Analog input leakage current (GPIO_STD)	-	-	165	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115C	IAIC2	Analog input leakage current (GPIO_ENH)	-	-	515	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices

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26 电气规格
表 36 (续) SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID115C_125	IAIC2	Analog input leakage current (GPIO_ENH)	–	–	515	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID115E	IAIC2	Analog input leakage current (GPIO_SMC)	–	–	1015	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ For S-grade devices
SID115E_125	IAIC2	Analog input leakage current (GPIO_SMC)	–	–	1015	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ For E-grade devices
SID116	IDIAGREF	Diagnostic reference current	–	–	70	μA	
SID117	IVDDA	Analog power supply current while ADC is operating	–	360	550	μA	Per enabled ADC, without diagnosis
SID117A	IVDDA_DS	Analog power supply current while ADC is not operating	–	1	21	μA	Per enabled ADC
SID118	IVREF	Analog reference voltage current while ADC is operating	–	360	550	μA	Per enabled ADC, without diagnosis
SID118A	IVREF_LEAK	Analog reference voltage current while ADC is not operating	–	1.8	5	μA	Per enabled ADC
SID118B	ts_4P5_1	Analog input sample time ($4.5\text{ V} \leq V_{DDA_ADC}$) for channels of SARMUX1	824	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID118C	ts_2P7_1	Analog input sample time ($2.7\text{ V} \leq V_{DDA_ADC}$) for channels of SARMUX1	1648	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design

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26 电气规格
表 36 (续) SAR ADC AC 规格

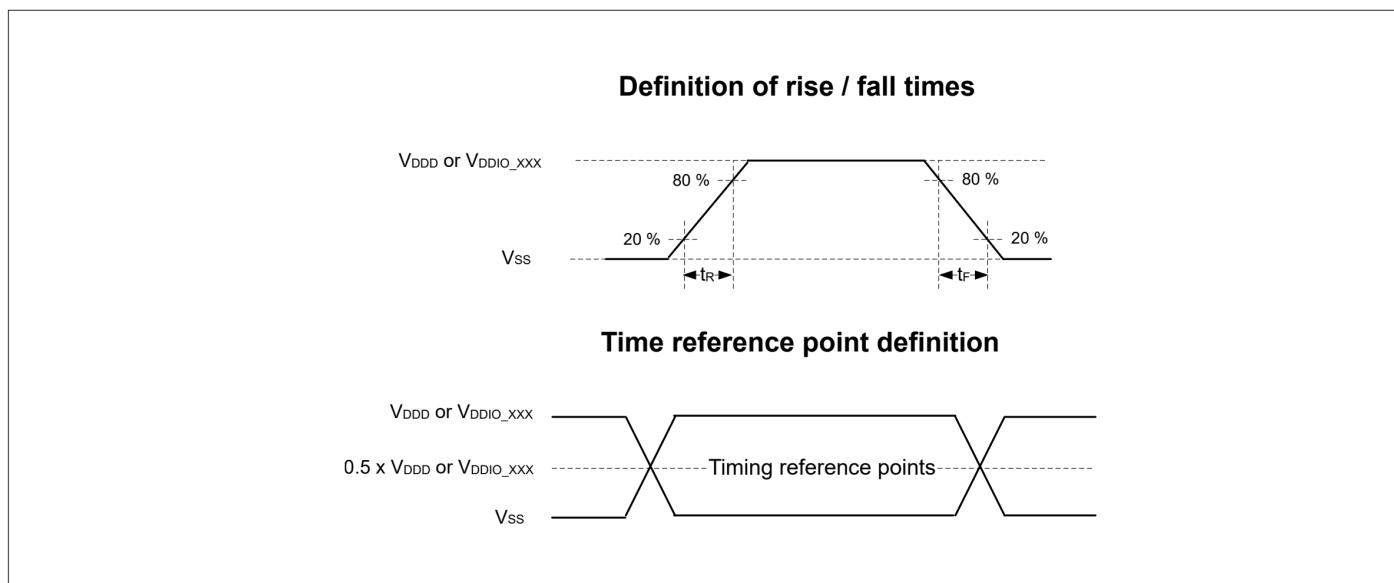
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID119A	t _{ST3}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.5	Msps	4.5 V ≤ V _{DDA_ADC} ≤ 5.5 V 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID119B	t _{ST4}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.25	Msps	2.7 V ≤ V _{DDA_ADC} < 4.5 V 80 MHz / 12 = 6.67 MHz, 11 sampling cycles, 15 conversion cycles

表 37 温度传感器规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201	TSENSACC_TR	Temperature sensor accuracy trimmed	–5	–	5	°C	This spec is valid for the following two conditions: 1. 3.0 V ≤ V _{DDA_ADC} = V _{REFH} ≤ 3.6 V and 3.0 V ≤ V _{DDD} ≤ 3.6 V 2. 4.5 V ≤ V _{DDA_ADC} = V _{REFH} ≤ 5.5 V and 4.5 V ≤ V _{DDD} ≤ 5.5 V (Calibrated accuracy by factory trimming)
SID202	TSENSACC_STD	Temperature sensor accuracy standard	–10	–	10	°C	This spec applies to all valid combinations for V _{DDA_ADC} = V _{REFH} and V _{DDD} , which are not covered by SID201 (Uncalibrated accuracy)

26.6 AC 规格

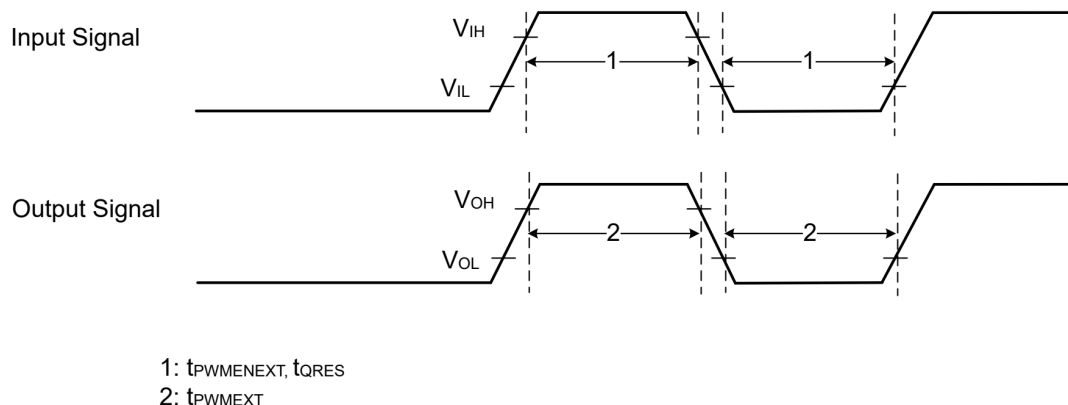
除非另有说明，时序均按照图 16 中提到的指导原则定义。

26 电气规格

图 16 AC 时序规格
26.7 数字外设
表 38 TCPWM 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID120	f_c	TCPWM operating frequency	–	–	100	MHz	f_c = peripheral clock
SID121	t_{PWMENT}	Input trigger pulse width for all trigger events	$2 / f_c$	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMENT}	Output trigger pulse widths	$2 / f_c$	–	–	ns	Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs
SID123	t_{CRES}	Resolution of counter	$1 / f_c$	–	–	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	$1 / f_c$	–	–	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	$2 / f_c$	–	–	ns	Minimum pulse width between Quadrature phase inputs.

26 电气规格

TCPWM Timing Diagrams


图 17 TCPWM 时序图
表 39 SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID129	f_{SCB}	SCB operating frequency	–	–	100	MHz	
SID129_2	$t_{\text{SPI_TRANS}}$	SCB input transition in SPI mode	–	–	4	ns	
SID129_3	$t_{\text{SPI_TRANS}}$	SCB output transition in SPI mode	–	–	10	ns	Valid for HSIO_STDLN
SID129_4	$t_{\text{SPI_TRANS}}$	SCB output transition in SPI mode	–	–	20	ns	Valid for GPIO_STD, GPIO_ENH, GPIO_SMC

I²C Interface-Standard-mode
建议 I/O 配置:

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_SLEW_EXT/SLEW<2:0> = 0b000

(
注: SID138 对于 HSIO_STDLN 无效
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SID130	f_{SCL}	SCL clock frequency	–	–	100	kHz	
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(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID131	t _{HD;STA}	Hold time, START condition	4000	–	–	ns	
SID132	t _{LOW}	Low period of SCL	4700	–	–	ns	
SID133	t _{HIGH}	High period of SCL	4000	–	–	ns	
SID134	t _{SU;STA}	Setup time for a repeated START	4700	–	–	ns	
SID135	t _{HD;DAT}	Data hold time, for receiver	0	–	–	ns	
SID136	t _{SU;DAT}	Data setup time	250	–	–	ns	
SID138	t _F	Fall time of SCL and SDA	–	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC, GPIO_STD
SID139	t _{SU;STO}	Setup time for STOP	4000	–	–	ns	
SID140	t _{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C _B	Capacitive load for each bus line	–	–	400	pF	
SID142	t _{VD;DAT}	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	t _{VD;ACK}	Data valid acknowledge time	–	–	3450	ns	

I²C Interface-Fast-mode
建议 I/O 配置:

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_SLEW_EXT/SLEW<2:0> = 0b000

(

注: SID158 对于 GPIO_STD 和 HSIO_STDLN 无效

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SID150	f _{SCL}	SCL clock frequency	–	–	400 ¹⁾	kHz	
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(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID151	t _{HD;STA}	Hold time, START condition	600	–	–	ns	
SID152	t _{LOW}	Low period of SCL	1300	–	–	ns	
SID153	t _{HIGH}	High period of SCL	600	–	–	ns	
SID154	t _{SU;STA}	Setup time for a repeated START	600	–	–	ns	
SID155	t _{HD;DAT}	Data hold time, for receiver	0	–	–	ns	
SID156	t _{SU;DAT}	Data setup time	100	–	–	ns	
SID158	t _F	Fall time of SCL and SDA	20 × (V _{DDIO_G} PIO/5.5 V)	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC
SID159	t _{SU;STO}	Setup time for STOP	600	–	–	ns	
SID160	t _{BUF}	Bus free time between START and STOP	1300	–	–	ns	
SID161	C _B	Capacitive load for each bus line	–	–	400	pF	
SID162	t _{VD;DAT}	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	t _{VD;ACK}	Data valid acknowledge time	–	–	900	ns	
SID164	t _{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	

I²C Interface-Fast-Plus mode

(表格续下页...)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
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建议 I/O 配置

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_SLEW_EXT/SLEW<2:0>=0b000

(

注: *SID178 对于 GPIO_STD, GPIO_SMC 和 HSIO_STDLN 无效*

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SID170	fSCL	SCL clock frequency	–	–	12)	MHz	
SID171	tHD;STA	Hold time, START condition	260	–	–	ns	
SID172	tLOW	Low period of SCL	500	–	–	ns	
SID173	tHIGH	High period of SCL	260	–	–	ns	
SID174	tSU;STA	Setup time for a repeated START	260	–	–	ns	
SID175	tHD;DAT	Data hold time, for receiver	0	–	–	ns	
SID176	tSU;DAT	Data setup time	50	–	–	ns	
SID178	t _F	Fall time of SCL and SDA	20 × (V _{DDIO_G} PIO/5.5 V)	–	160	ns	Input and output, 20pF load Output: Only for GPIO_ENH
SID179	tSU;STO	Setup time for STOP	260	–	–	ns	
SID180	tBUF	Bus free time between START and STOP	500	–	–	ns	
SID181	C _B	Capacitive load for each bus line	–	–	20	pF	
SID182	tVD;DAT	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	tVD;ACK	Data valid acknowledge time	–	–	450	ns	

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID184	tSP	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	

SPI Interface
建议 I/O 配置：（适用于以下所有模式）

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0

对于 SPI 速度 ≤ 12.5 MHz

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, GPIO)

SID190	fSPI	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID191	tDMO	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID192	tDSI	SPI Master: MISO valid before SCLK capturing edge	40	–	–	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC

（表格续下页.....）

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID193	tHMO	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID194	tw_SCLK_H_L	SPI SCLK pulse width HIGH or LOW	$0.4 \times (1/f_{SPI})$	$0.5 \times (1/f_{SPI})$	$0.6 \times (1/f_{SPI})$	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID195	tvss	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID196	tDHI	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID198	tEN_SETUP	SSEL valid, before the first SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID199	tEN_HOLD	SSEL hold, after the last SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID197	CSPIM_MS	SPI Capacitive Load	–	–	20	pF	

SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, HSIO)

(表格续下页...)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID190A	f _{SPI}	SPI operating frequency	–	–	20	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) - 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz. for instances on HSIO_STDLN
SID191A	t _{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	9	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID192A	t _{DSI}	SPI Master: MISO valid before SCLK capturing edge	25	–	–	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID193A	thMO	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID194A	tw_SCLK_H_L	SPI SCLK pulse width HIGH or LOW	$0.4 \times (1/f_{SPI})$	$0.5 \times (1/f_{SPI})$	$0.6 \times (1/f_{SPI})$	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID195A	tvss	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID196A	tdHI	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode): LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID197A	CSPIM_MS	SPI Capacitive Load	–	–	20	pF	
SID198A	tEN_SETUP	SSEL valid, before the first SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID199A	tEN_SHOLD	SSEL hold, after the last SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SPI Interface Slave (internally clocked, GPIO and HSIO)							
SID205	fSPI_INT	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206	tDMI_INT	SPI Slave: MOSI Valid before Scklock capturing edge	5	–	–	ns	SPI Slave, internally clocked
SID207	tDSO_INT	SPI Slave: MISO Valid after Scklock driving edge, in the internal-clocked mode	–	–	60	ns	SPI Slave, internally clocked
SID208	tHSO_INT	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209	tEN_SETUP_INT	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210	tEN_HOLD_INT	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked
SID211	tEN_SETUP_PRE	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID212	tEN_HOLD_PRE	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213	tEN_SETUP_CO	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214	tEN_HOLD_CO	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215	tw_DIS_INT	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216	tw_SCLKH_INT	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, internally clocked
SID217	tw_SCLKL_INT	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, internally clocked
SID218	tSIH_INT	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID219	CSPIS_INT	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked

SPI Interface Slave (externally clocked, GPIO and HSIO)

SID220	fSPI_EXT	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps
SID221	tDMI_EXT	SPI Slave: MOSI Valid before Sclock capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID222	tDSO_EXT	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	30	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223	tHSO_EXT	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224	tEN_SETUP_EXT	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID225	tEN_HOLD_EXT	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226	tw_DIS_EXT	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227	tw_SCLKH_EXT	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228	tw_SCLKL_EXT	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230	CSPIS_EXT	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231	tvSS_EXT	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	SPI Slave, externally clocked: 12.5 Mbps

SPI Interface Slave (internally clocked, SMC I/O)

SID205_2	fSPI_INT	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206_2	tDMI_INT	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI Slave, internally clocked

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID207_2	tDSO_INT	SPI Slave: MISO Valid after Scklock driving edge, in the internal-clocked mode	–	–	64	ns	SPI Slave, internally clocked
SID208_2	tHSO_INT	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209_2	tEN_SETUP_INT	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210_2	tEN_HOLD_INT	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked
SID211_2	tEN_SETUP_PRE	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID212_2	tEN_HOLD_PRE	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213_2	tEN_SETUP_CO	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214_2	tEN_HOLD_CO	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215_2	tW_DIS_INT	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216_2	tW_SCLKH_INT	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, internally clocked
SID217_2	tW_SCLKL_INT	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, internally clocked
SID218_2	tSIH_INT	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked
SID219_2	CSPIS_INT	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked

SPI Interface Slave (externally clocked, SMC I/O)

SID220_2	fSPI_EXT	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps
SID221_2	tDMI_EXT	SPI Slave: MOSI Valid before Scklock capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID222_2	tDSO_EXT	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	34	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223_2	tHSO_EXT	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224_2	tEN_SETUP_EXT	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID225_2	tEN_HOLD_EXT	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226_2	tW_DIS_EXT	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227_2	tW_SCLKH_EXT	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228_2	tW_SCLKL_EXT	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229_2	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230_2	CSPIS_EXT	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231_2	tVSS_EXT	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	37	ns	SPI Slave, externally clocked: 12.5 Mbps

SPI Interface Slave (externally clocked, 20 MHz)

SID220A	fSPI_EXT	SPI operating frequency	–	–	20	MHz	SPI Slave, externally clocked: 20 Mbps
SID221A	tDMI_EXT	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID222A	tDSO_EXT	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	18	ns	SPI Slave, externally clocked: 20 Mbps
SID223A	tHSO_EXT	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID224A	tEN_SETUP_EXT	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps

(表格续下页.....)

26 电气规格
表 39 (续) SCB 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID225A	tEN_HOLD_EXT	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID226A	tw_DIS_EXT	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID227A	tw_SCLKH_EXT	SPI SCLK pulse width HIGH	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID228A	tw_SCLKL_EXT	SPI SCLK pulse width LOW	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID229A	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID230A	CSPIS_EXT	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 20 Mbps
SID231A	tvSS_EXT	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	23	ns	SPI Slave, externally clocked: 20 Mbps

UART Interface
建议 I/O 配置:

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0

SID240	fBPS	Signaling rate	–	–	10	Mbps	
SID240A	fBPS_TX	Signaling rate for TX on P16_0 for SCB#4 and P15_3 for SCB#3	–	–	25	Mbps	Valid only for TX at 20 pF load
SID241	fACC	Frequency accuracy of TX bit time on P16_0 for SCB#4 and P15_3 for SCB#3	–0.5	–	0.5	ns	With PLL 200 MHz ≤ f _{VCO} ≤ 400 MHz at 20 pF load
SID242	fJIT	Jitter of TX on P16.0 for SCB#4 and P15.3 for SCB#3	–4.5	–	4.5	ns	at 20 pF load

1) 为了以 400 kHz 的频率驱动满总线负载, 在 0.6 V_{VOL} 时需要 6 mA I_{OLo}

2) 为了以 1 MHz 的频率驱动满总线负载, 在 0.4 V_{VOL} 时需要 20 mA I_{OLo}

26 电气规格

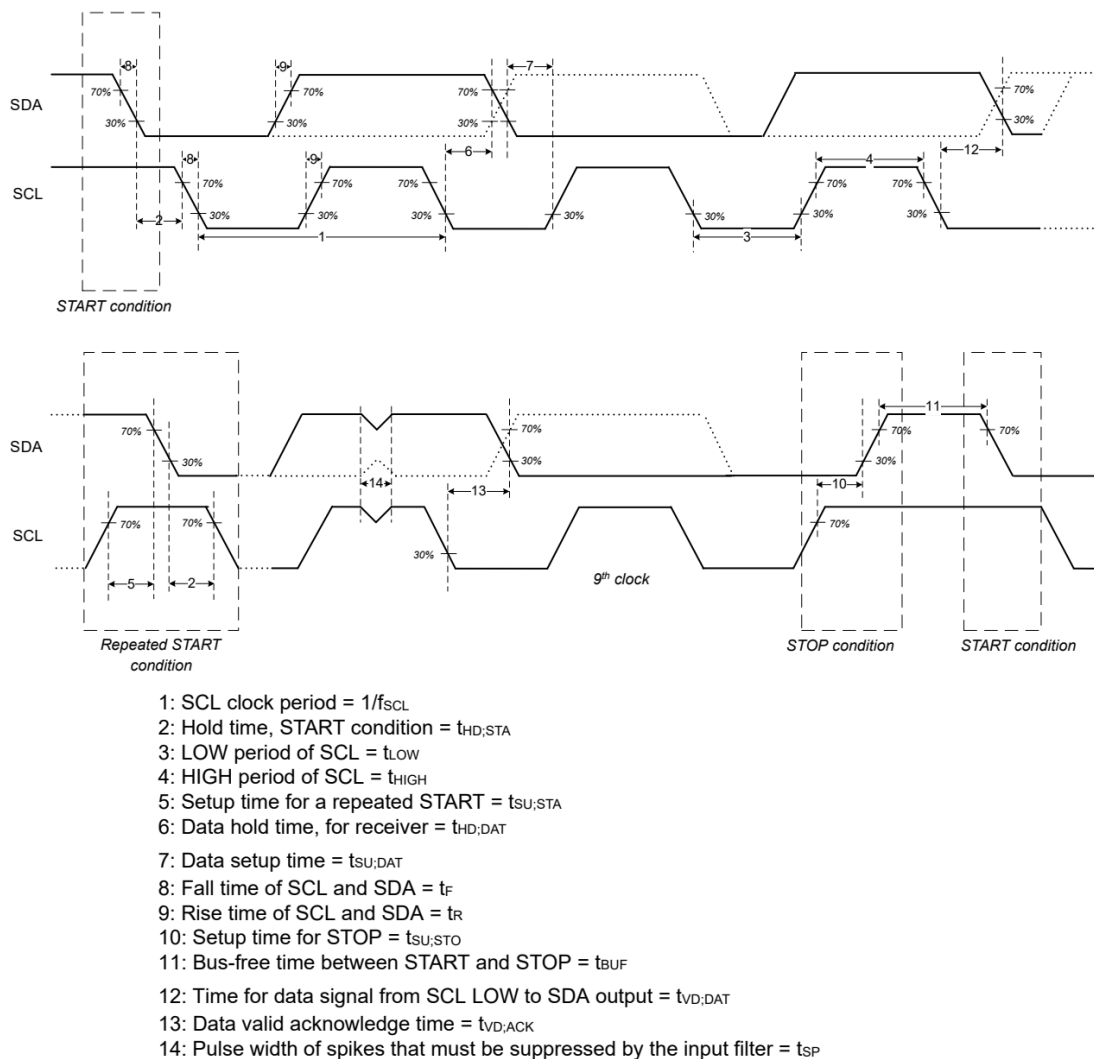
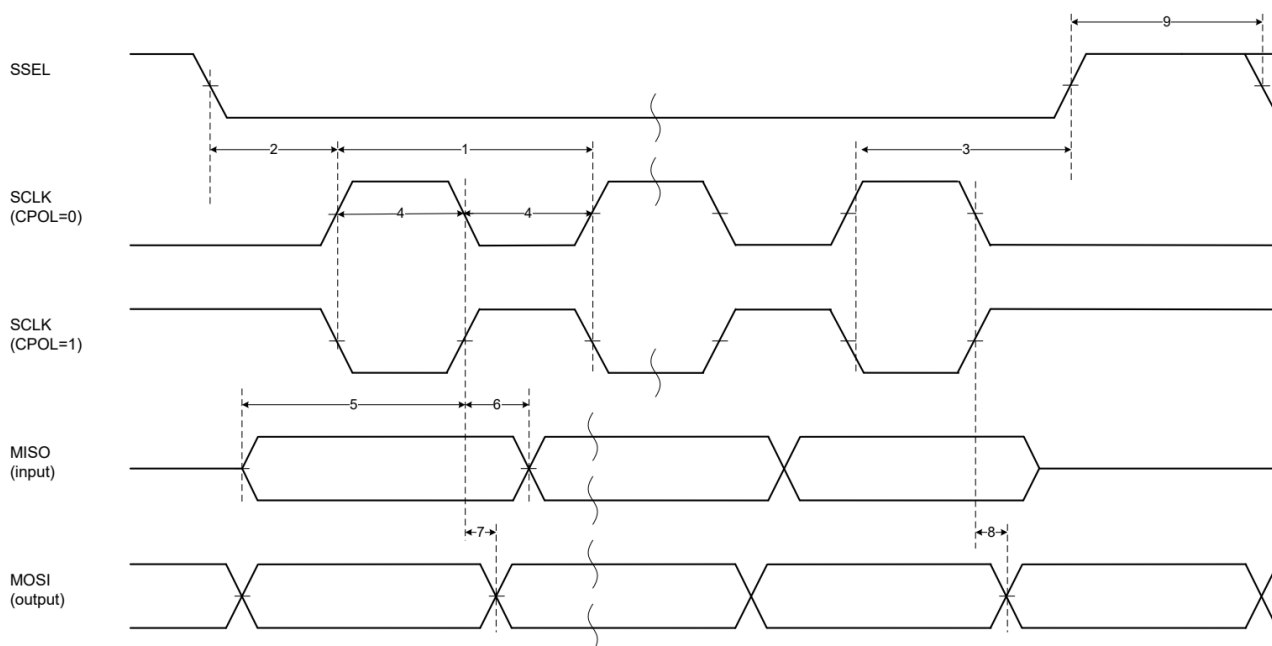


图 18

I²C 时序图

26 电气规格

SPI Master Timing Diagrams (LATE_MISO_SAMPLE=1)
CPHA=0



- 1: SCLK period = $1 / f_{SPI}$
- 2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
- 3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
- 4: SCLK high or low time = $t_{W_SCLK_H_L}$
- 5: Input data setup time = t_{DSI}
- 6: Input data hold time = t_{DHI}
- 7: Output data valid after SCLK driving edge = t_{DMO}
- 8: Output data hold time = t_{HMO}
- 9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

图 19 SPI 主机时序图（低时钟相位）

26 电气规格

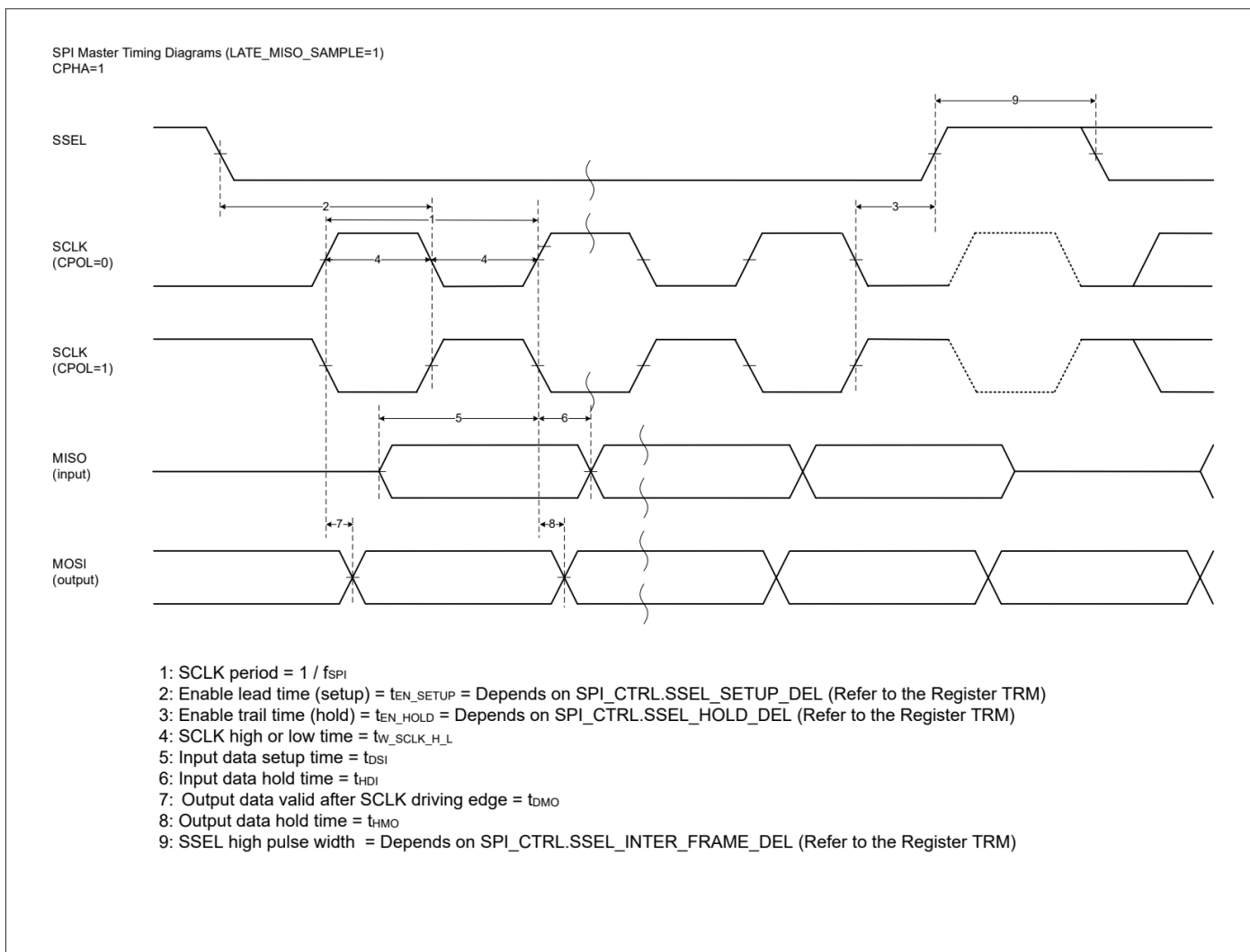


图 20 SPI 主机时序图（高时钟相位）

26 电气规格

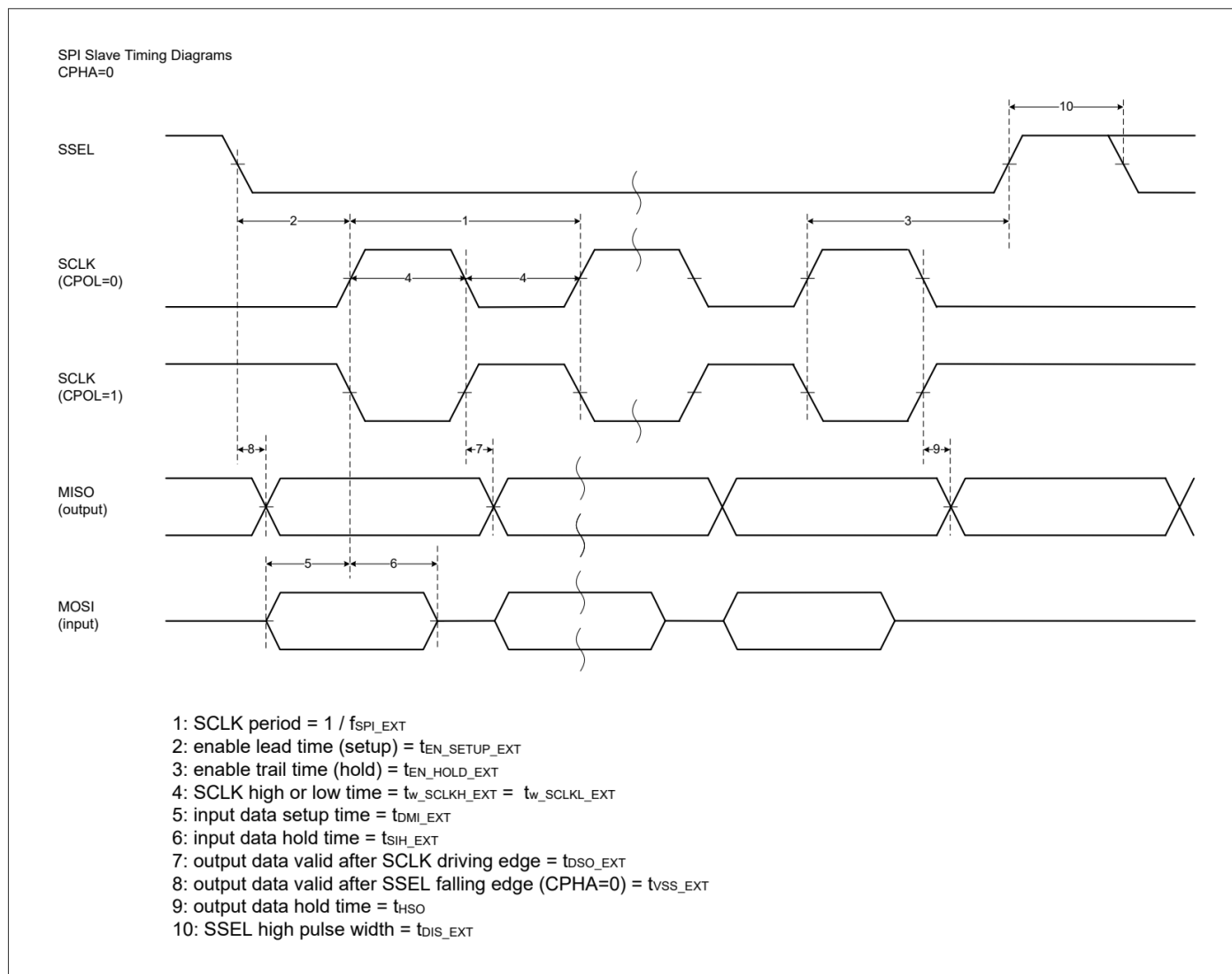


图 21 SPI 从机时序图（低时钟相位）

26 电气规格

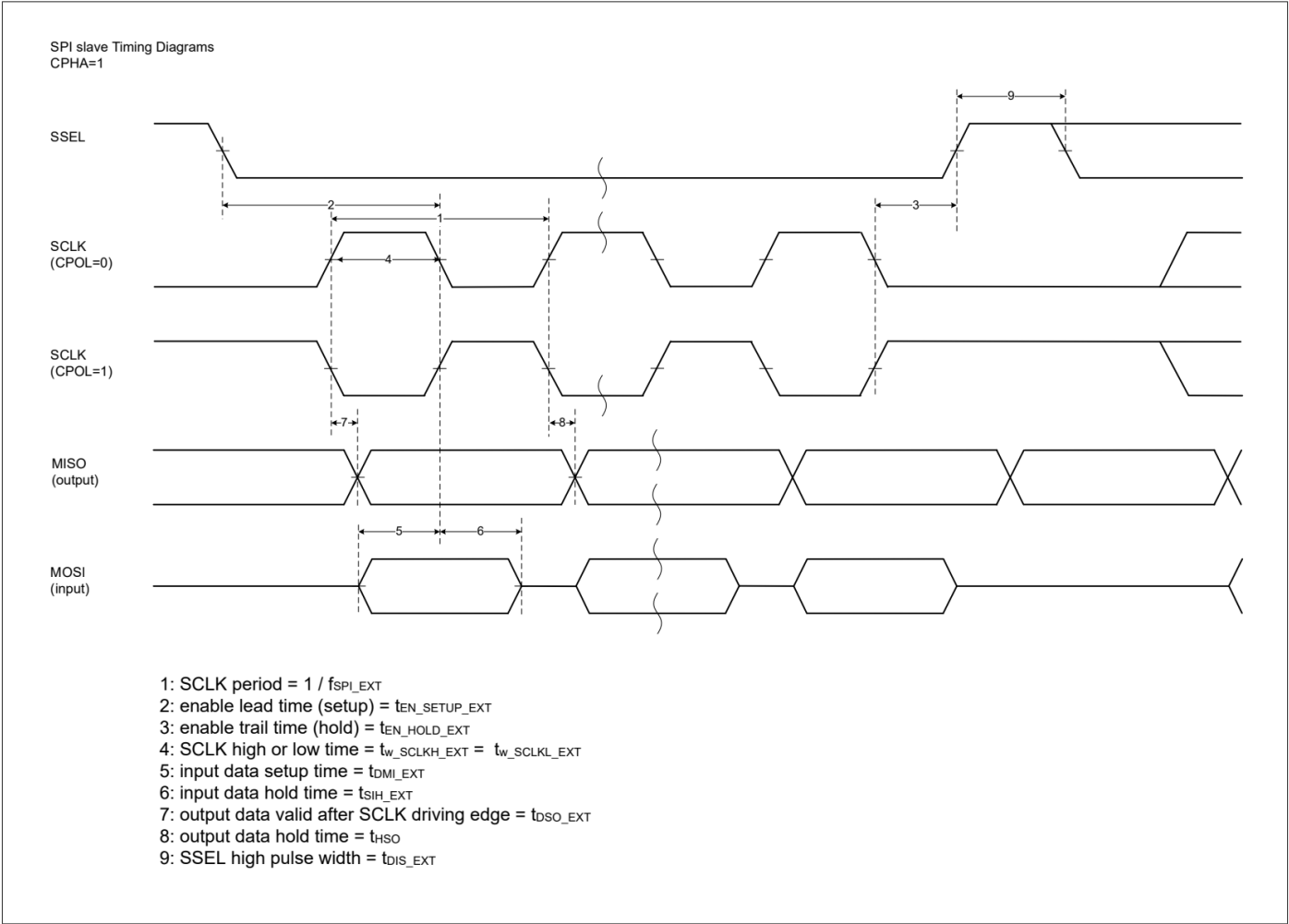


图 22 SPI 从机时序图（高时钟相位）

表 40 CAN FD 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID630	f_{HCLK}	System clock (HCLK) frequency	–	–	100	MHz	$f_{CCLK} \leq f_{HCLK}$, guaranteed by design
SID631	f_{CCLK}	CAN clock (CCLK) frequency	–	–	100	MHz	$f_{CCLK} \leq f_{HCLK}$, guaranteed by design

26 电气规格
表 41 LIN 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID249	f _{LIN}	Internal clock frequency to the LIN block	–	–	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	Guaranteed by design

26.8 存储器
表 42 Flash DC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257A	V _{PE}	Erase and program voltage	2.7	–	5.5	V	

表 43 Flash AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257	f _{FO}	Maximum operation frequency	–	–	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 320 MHz
SID254	t _{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	–	–	37.5	μs	
SID255	t _{ERS_RES_SUS}	Minimum time allowed from erase resume to erase suspend	250	–	–	μs	Guaranteed by design
SID258	t _{BC_WF}	Blank Check time for Work Flash N-byte	–	–	10 + 0.3 × N	μs	At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time

(表格续下页.....)

26 电气规格
表 43 (续) Flash AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID258A	tAA_BC_ENTRY	Time to enter Blank Check mode	–	5	–	µs	
SID258B	tAA_BC_EXIT	Time to exit Blank Check mode	–	5	–	µs	
SID259	tSECTORERASE1	Sector erase time (code-flash: 32 KB)	–	45	90	ms	Includes internal preprogramming time
SID260	tSECTORERASE2	Sector erase time (code-flash: 8 KB)	–	15	30	ms	Includes internal preprogramming time
SID261	tSECTORERASE3	Sector erase time (work-flash, 2 KB)	–	80	160	ms	Includes internal preprogramming time
SID262	tSECTORERASE4	Sector erase time (work-flash, 128 B)	–	5	15	ms	Includes internal preprogramming time
SID263	tWRITE1	64-bit write time (code-flash)	–	30	60	µs	Excludes system overhead time
SID264	tWRITE2	256-bit write time (code-flash)	–	40	70	µs	Excludes system overhead time
SID265	tWRITE3	4096-bit write time (code-flash)	–	320	1200	µs	Excludes system overhead time
SID266	tWRITE4	32-bit write time (work-flash)	–	30	60	µs	Excludes system overhead time
SID267	tFRET1	Code-flash retention. 1000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85^\circ\text{C}$ average
SID182T1	tFRET2	Code-flash retention. 100 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30^\circ\text{C}$ average
SID268	tFRET3	Work-flash retention. 125,000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85^\circ\text{C}$ average
SID269	tFRET4	Work-flash retention. 250,000 program/erase cycles	10	–	–	years	Temperature at write/erase time. $T_A \leq +85^\circ\text{C}$ average
SID182T2	tFRET5	Work-flash retention. 1000 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30^\circ\text{C}$ average

(表格续下页.....)

26 电气规格
表 43 (续) Flash AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID612	ICC_ACT2	Program operating current (code or work-flash)	–	15	62	mA	$V_{DD} = 5\text{ V}$, $V_{CCD} = 1.1\text{ V}$ guaranteed by design
SID613	ICC_ACT3	Erase operating current (code- or work-flash)	–	15	62	mA	$V_{DD} = 5\text{ V}$, $V_{CCD} = 1.1\text{ V}$ guaranteed by design

26.9 系统资源
表 44 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Power-on Reset Specifications							
SID270	VPOR_R	POR rising trip voltage	1.5	–	2.35	V	Guaranteed by design
SID276	VPOR_F	POR falling trip voltage	1.45	–	2.1	V	
SID271	VPOR_H	Level detection hysteresis	20	–	300	mV	
SID272	tdLY_POR	Delay between V_{DD} rising through 2.3 V and POR reset output rising through $V_{DD} / 2$	–	–	3	μs	Guaranteed by design
SID273	tPOFF	Power off time	350	–	–	μs	$V_{DD} < 1.45\text{ V}$ Does not apply to SID274A and SID274B
SID274 A	POR_RR1	V_{DD} power ramp rate with robust BOD - XRES_L asserted (BOD operation is guaranteed)	–	–	100	mV/μs	Applies to ramp up and ramp down
SID274 B	POR_RR1	V_{DD} power ramp rate with robust BOD - XRES_L de-asserted (BOD operation is guaranteed)	1	–	100	mV/μs	Applies to ramp up and ramp down
SID275	POR_RR2	V_{DD} power ramp rate without robust BOD	100	–	1000	mV/μs	This ramp does not support robust BOD t_{POFF} must be satisfied. Applies to ramp up and ramp down

High-voltage BOD (HV BOD) Specifications

(表格续下页...)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID500	VTR_2P7_R	HV BOD 2.7 V trimmed rising trip point for V_{DD} and V_{DDA_ADC} (default)	2.474	2.55	2.627	V	
SID501	VTR_2P7_F	HV BOD 2.7 V trimmed falling trip point for V_{DD} and V_{DDA_ADC} (default)	2.449	2.525	2.601	V	
SID502	VTR_3P0_R	HV BOD 3.0 V trimmed rising trip point for V_{DD} and V_{DDA_ADC}	2.765	2.85	2.936	V	
SID503	VTR_3P0_F	HV BOD 3.0 V trimmed falling trip point for V_{DD} and V_{DDA_ADC}	2.74	2.825	2.91	V	
SID505	HVBOD_RR_A	Power ramp rate: V_{DD} and V_{DDA_ADC} (Active)	–	–	100	mV/μs	
SID506	HVBOD_RR_DS	Power ramp rate: V_{DD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/μs	
SID507	tdLY_ACT_HVBOD	Active mode delay between V_{DD} falling/rising through VTR_2P7_F/R or VTR_3P0_F/R and an internal HV BOD output transitioning through $V_{DD}/2$	–	–	0.5	μs	Guaranteed by design
SID507 A	tdLY_ACT_HVBOD_A	Active mode delay between V_{DDA_ADC} falling/rising through VTR_2P7_F/R or VTR_3P0_F/R and internal HV BOD output transitioning through $V_{DD}/2$	–	–	1	μs	Guaranteed by design
SID507 B	tdLY_DS_HVBOD	DeepSleep mode delay between V_{DD}/V_{DDA_ADC} falling/rising through VTR_2P7_F/R or VTR_3P0_F/R and an internal HV BOD output transitioning through $V_{DD}/2$	–	–	4	μs	Guaranteed by design
SID508	tRES_HVBOD	Response time of HV BOD, V_{DD}/V_{DDA_ADC} supply. HV BOD guaranteed to generate pulse for V_{DD}/V_{DDA_ADC} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below VTR_2P7_F or VTR_3P0_F)	100	–	–	ns	Guaranteed by design

Low-voltage BOD (LV BOD) Specifications

SID510	VTR_R_LVBOD	LV BOD trimmed rising trip point for V_{CCD}	0.917	0.945	0.973	V	
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26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID511	VTR_F_LVBOD	LV BOD trimmed falling trip point for V _{CCD}	0.892	0.92	0.948	V	
SID515	tdLY_ACT_LVBOD	Active delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V _{DD} / 2	–	–	1	μs	Guaranteed by design
SID515 A	tdLY_DS_LVBOD	DeepSleep mode delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V _{DD} / 2	–	–	12	μs	Guaranteed by design
SID516	tRES_LVBOD	Response time of LV BOD. LV BOD guaranteed to generate pulse for V _{CCD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below V _{TR_F_LVBOD})	100	–	–	ns	Guaranteed by design

Low-voltage Detector (LVD) DC Specifications

SID520	VTR_2P8_F	LVD 2.8 V trimmed falling trip point for V _{DD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	VTR_2P9_F	LVD 2.9 V trimmed falling trip point for V _{DD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	VTR_3P0_F	LVD 3.0 V trimmed falling trip point for V _{DD}	Typ – 4%	3000	Typ + 4%	mV	
SID523	VTR_3P1_F	LVD 3.1 V trimmed falling trip point for V _{DD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	VTR_3P2_F	LVD 3.2 V trimmed falling trip point for V _{DD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	VTR_3P3_F	LVD 3.3 V trimmed falling trip point for V _{DD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	VTR_3P4_F	LVD 3.4 V trimmed falling trip point for V _{DD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	VTR_3P5_F	LVD 3.5 V trimmed falling trip point for V _{DD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	VTR_3P6_F	LVD 3.6 V trimmed falling trip point for V _{DD}	Typ – 4%	3600	Typ + 4%	mV	
SID529	VTR_3P7_F	LVD 3.7 V trimmed falling trip point for V _{DD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	VTR_3P8_F	LVD 3.8 V trimmed falling trip point for V _{DD}	Typ – 4%	3800	Typ + 4%	mV	

(表格续下页.....)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID531	VTR_3P9_F	LVD 3.9 V trimmed falling trip point for V _{DD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	VTR_4P0_F	LVD 4.0 V trimmed falling trip point for V _{DD}	Typ – 4%	4000	Typ + 4%	mV	
SID533	VTR_4P1_F	LVD 4.1 V trimmed falling trip point for V _{DD}	Typ – 4%	4100	Typ + 4%	mV	
SID534	VTR_4P2_F	LVD 4.2 V trimmed falling trip point for V _{DD}	Typ – 4%	4200	Typ + 4%	mV	
SID535	VTR_4P3_F	LVD 4.3 V trimmed falling trip point for V _{DD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	VTR_4P4_F	LVD 4.4 V trimmed falling trip point for V _{DD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	VTR_4P5_F	LVD 4.5 V trimmed falling trip point for V _{DD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	VTR_4P6_F	LVD 4.6 V trimmed falling trip point for V _{DD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	VTR_4P7_F	LVD 4.7 V trimmed falling trip point for V _{DD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	VTR_4P8_F	LVD 4.8 V trimmed falling trip point for V _{DD}	Typ – 4%	4800	Typ + 4%	mV	
SID541	VTR_4P9_F	LVD 4.9 V trimmed falling trip point for V _{DD}	Typ – 4%	4900	Typ + 4%	mV	
SID542	VTR_5P0_F	LVD 5.0 V trimmed falling trip point for V _{DD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	VTR_5P1_F	LVD 5.1 V trimmed falling trip point for V _{DD}	Typ – 4%	5100	Typ + 4%	mV	
SID544	VTR_5P2_F	LVD 5.2 V trimmed falling trip point for V _{DD}	Typ – 4%	5200	Typ + 4%	mV	
SID545	VTR_5P3_F	LVD 5.3 V trimmed falling trip point for V _{DD}	Typ – 4%	5300	Typ + 4%	mV	
SID546	VTR_2P8_R	LVD 2.8 V trimmed rising trip point for V _{DD}	Typ – 4%	2825	Typ + 4%	mV	Same as VTR_2P8_F + 25 mV
SID547	VTR_2P9_R	LVD 2.9 V trimmed rising trip point for V _{DD}	Typ – 4%	2925	Typ + 4%	mV	Same as VTR_2P9_F + 25 mV
SID548	VTR_3P0_R	LVD 3.0 V trimmed rising trip point for V _{DD}	Typ – 4%	3025	Typ + 4%	mV	Same as VTR_3P0_F + 25 mV

(表格续下页.....)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID549	VTR_3P1_R	LVD 3.1 V trimmed rising trip point for V _{DD}	Typ – 4%	3125	Typ + 4%	mV	Same as VTR_3P1_F + 25 mV
SID550	VTR_3P2_R	LVD 3.2 V trimmed rising trip point for V _{DD}	Typ – 4%	3225	Typ + 4%	mV	Same as VTR_3P2_F + 25 mV
SID551	VTR_3P3_R	LVD 3.3 V trimmed rising trip point for V _{DD}	Typ – 4%	3325	Typ + 4%	mV	Same as VTR_3P3_F + 25 mV
SID552	VTR_3P4_R	LVD 3.4 V trimmed rising trip point for V _{DD}	Typ – 4%	3425	Typ + 4%	mV	Same as VTR_3P4_F + 25 mV
SID553	VTR_3P5_R	LVD 3.5 V trimmed rising trip point for V _{DD}	Typ – 4%	3525	Typ + 4%	mV	Same as VTR_3P5_F + 25 mV
SID554	VTR_3P6_R	LVD 3.6 V trimmed rising trip point for V _{DD}	Typ – 4%	3625	Typ + 4%	mV	Same as VTR_3P6_F + 25 mV
SID555	VTR_3P7_R	LVD 3.7 V trimmed rising trip point for V _{DD}	Typ – 4%	3725	Typ + 4%	mV	Same as VTR_3P7_F + 25 mV
SID556	VTR_3P8_R	LVD 3.8 V trimmed rising trip point for V _{DD}	Typ – 4%	3825	Typ + 4%	mV	Same as VTR_3P8_F + 25 mV
SID557	VTR_3P9_R	LVD 3.9 V trimmed rising trip point for V _{DD}	Typ – 4%	3925	Typ + 4%	mV	Same as VTR_3P9_F + 25 mV
SID558	VTR_4P0_R	LVD 4.0 V trimmed rising trip point for V _{DD}	Typ – 4%	4025	Typ + 4%	mV	Same as VTR_4P0_F + 25 mV
SID559	VTR_4P1_R	LVD 4.1 V trimmed rising trip point for V _{DD}	Typ – 4%	4125	Typ + 4%	mV	Same as VTR_4P1_F + 25 mV
SID560	VTR_4P2_R	LVD 4.2 V trimmed rising trip point for V _{DD}	Typ – 4%	4225	Typ + 4%	mV	Same as VTR_4P2_F + 25 mV
SID561	VTR_4P3_R	LVD 4.3 V trimmed rising trip point for V _{DD}	Typ – 4%	4325	Typ + 4%	mV	Same as VTR_4P3_F + 25 mV

(表格续下页.....)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID562	VTR_4P4_R	LVD 4.4 V trimmed rising trip point for V _{DD}	Typ – 4%	4425	Typ + 4%	mV	Same as VTR_4P4_F + 25 mV
SID563	VTR_4P5_R	LVD 4.5 V trimmed rising trip point for V _{DD}	Typ – 4%	4525	Typ + 4%	mV	Same as VTR_4P5_F + 25 mV
SID564	VTR_4P6_R	LVD 4.6 V trimmed rising trip point for V _{DD}	Typ – 4%	4625	Typ + 4%	mV	Same as VTR_4P6_F + 25 mV
SID565	VTR_4P7_R	LVD 4.7 V trimmed rising trip point for V _{DD}	Typ – 4%	4725	Typ + 4%	mV	Same as VTR_4P7_F + 25 mV
SID566	VTR_4P8_R	LVD 4.8 V trimmed rising trip point for V _{DD}	Typ – 4%	4825	Typ + 4%	mV	Same as VTR_4P8_F + 25 mV
SID567	VTR_4P9_R	LVD 4.9 V trimmed rising trip point for V _{DD}	Typ – 4%	4925	Typ + 4%	mV	Same as VTR_4P9_F + 25 mV
SID568	VTR_5P0_R	LVD 5.0 V trimmed rising trip point for V _{DD}	Typ – 4%	5025	Typ + 4%	mV	Same as VTR_5P0_F + 25 mV
SID569	VTR_5P1_R	LVD 5.1 V trimmed rising trip point for V _{DD}	Typ – 4%	5125	Typ + 4%	mV	Same as VTR_5P1_F + 25 mV
SID570	VTR_5P2_R	LVD 5.2 V trimmed rising trip point for V _{DD}	Typ – 4%	5225	Typ + 4%	mV	Same as VTR_5P2_F + 25 mV
SID571	VTR_5P3_R	LVD 5.3 V trimmed rising trip point for V _{DD}	Typ – 4%	5325	Typ + 4%	mV	Same as VTR_5P3_F + 25 mV
SID573	LVD_RR_A	Power ramp rate: V _{DD} (Active)	–	–	100	mV/μs	
SID574	LVD_RR_DS	Power ramp rate: V _{DD} (DeepSleep)	–	–	10	mV/μs	
SID575	tdLY_ACT_LVD	Active mode delay between V _{DD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through V _{DD} / 2	–	–	1	μs	Guaranteed by design

(表格续下页.....)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID575 A	tdLY_DS_LVD	DeepSleep mode delay between V_{DD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through $V_{DD} / 2$	–	–	4	μs	Guaranteed by design
SID576	tRES_LVD	Response time of LVD, V_{DD} supply. LVD guaranteed to generate pulse for V_{DD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling trip point.)	100	–	–	ns	Guaranteed by design

High-voltage OVD Specifications

SID580	VTR_5P0_R	High-voltage OVD 5.0-V trimmed rising trip point for V_{DD} and V_{DDA_ADC}	5.049	5.205	5.361	V	
SID581	VTR_5P0_F	High-voltage OVD 5.0-V trimmed falling trip point for V_{DD} and V_{DDA_ADC}	5.025	5.18	5.335	V	
SID582	VTR_5P5_R	High-voltage OVD 5.5-V trimmed rising trip point for V_{DD} and V_{DDA_ADC} (default)	5.548	5.72	5.892	V	
SID583	VTR_5P5_F	High-voltage OVD 5.5-V trimmed falling trip point for V_{DD} and V_{DDA_ADC} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V_{DD} and V_{DDA_ADC} (Active)	–	–	100	mV/μs	
SID586	HVOVD_RR_DS	Power ramp rate: V_{DD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/μs	
SID587	tdLY_ACT_HVOVD	Active mode delay between V_{DD} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD output transitioning through $V_{DD} / 2$	–	–	1	μs	Guaranteed by design
SID587 A	tdLY_ACT_HVOVD_A	Active mode delay between V_{DDA_ADC} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD output transitioning through $V_{DD} / 2$	–	–	1.5	μs	Guaranteed by design

(表格续下页.....)

26 电气规格
表 44 (续) 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID587 B	tdLY_DS_HVOVD	DeepSleep mode delay between V_{DD}/V_{DDA_ADC} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD output transitioning through $V_{DD}/2$	–	–	4	µs	Guaranteed by design
SID588	tRES_HVOVD	Response time of HV OVD HV OVD guaranteed to generate pulse for V_{DD}/V_{DDA_ADC} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR_5P0_R}$ or $V_{TR_5P5_R}$)	100	–	–	ns	Guaranteed by design

Low-voltage OVD Specifications

SID590	VTR_R_LVOVD	LV OVD trimmed rising trip point for V_{CCD}	Typ – 3%	1300	Typ + 3%	mV	
SID591	VTR_F_LVOVD	LV OVD trimmed falling trip point for V_{CCD}	Typ – 3%	1275	Typ + 3%	mV	Same as $V_{TR_R_LVOVD} - 25\text{ mV}$
SID595	tdLY_ACT_LVOVD	Active mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through $V_{DD}/2$	–	–	1	µs	Guaranteed by design
SID595 A	tdLY_DS_LVOVD	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through $V_{DD}/2$	–	–	12	µs	Guaranteed by design
SID596	tRES_LVOVD	Response time of LV OVD. LV OVD guaranteed to generate pulse for V_{CCD} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR_R_LVOVD}$)	100	–	–	ns	Guaranteed by design

Over current detection (OCD) Specifications

SID598	IOCD	Over current detection range for internal Active regulator	312	–	630	mA	
SID599	IOCD_DPSLP	Over current detection range for internal DeepSleep regulator	18	–	72	mA	

26 电气规格

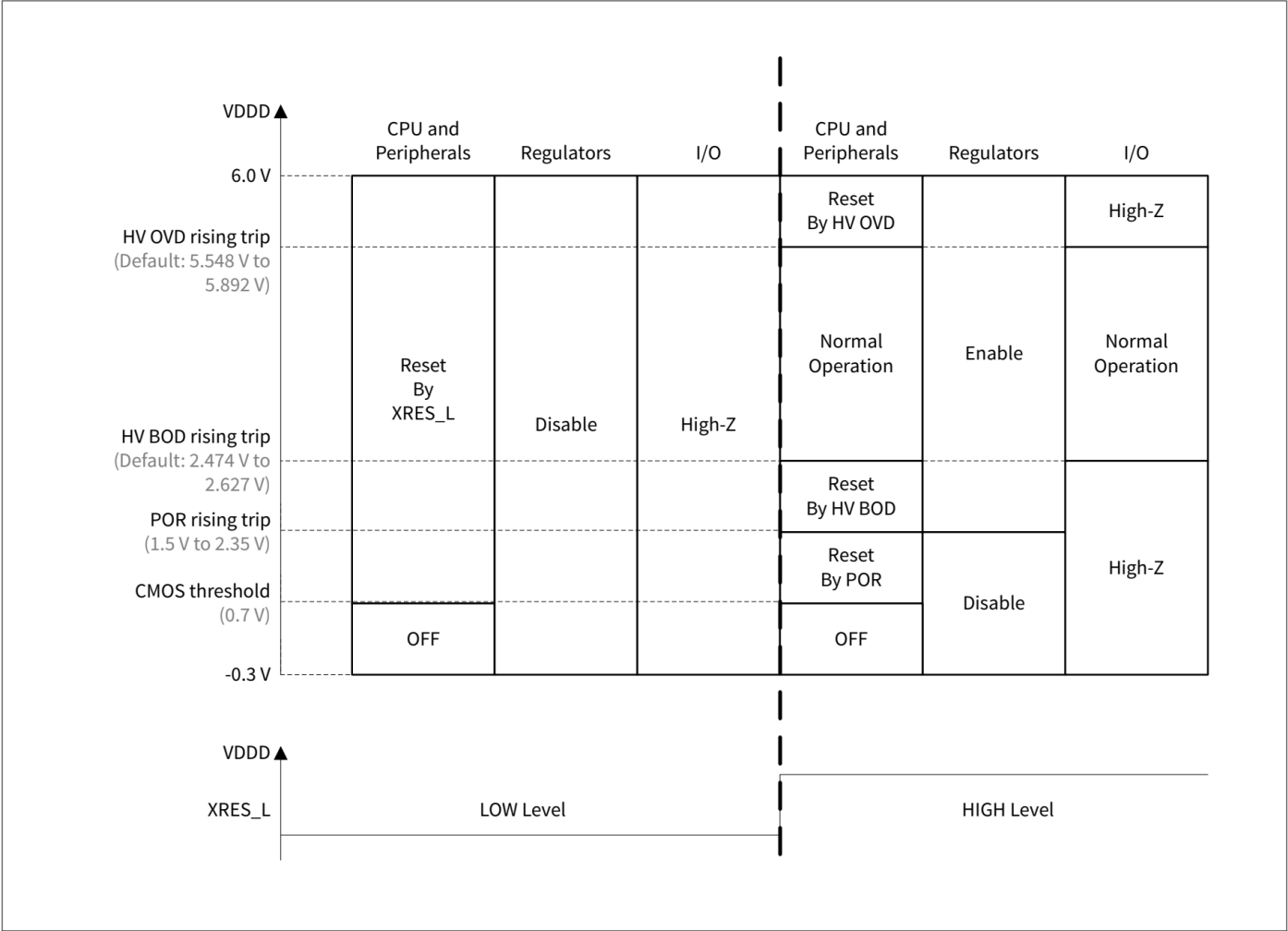


图 23 器件操作电源范围

26 电气规格

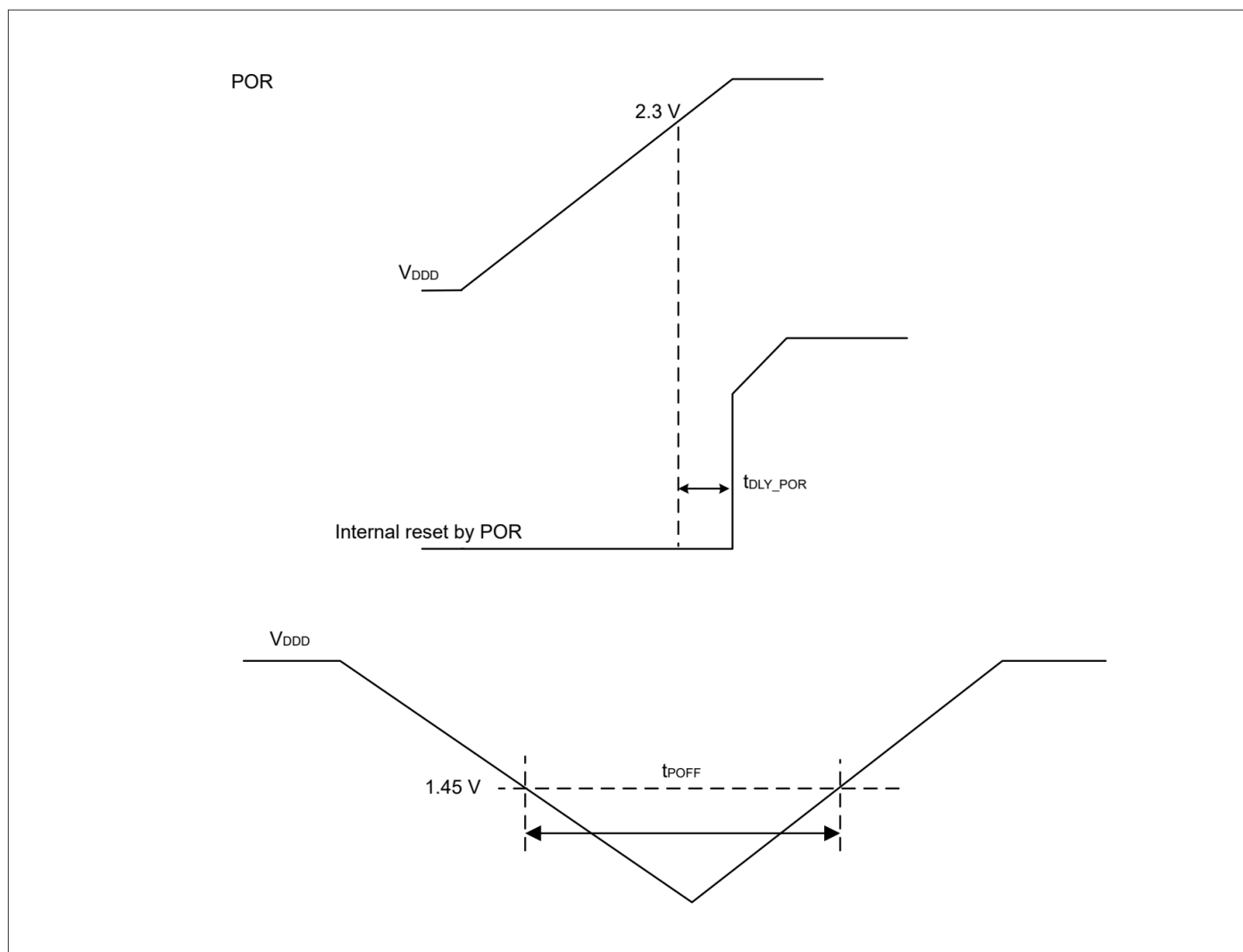


图 24

POR 规格

26 电气规格

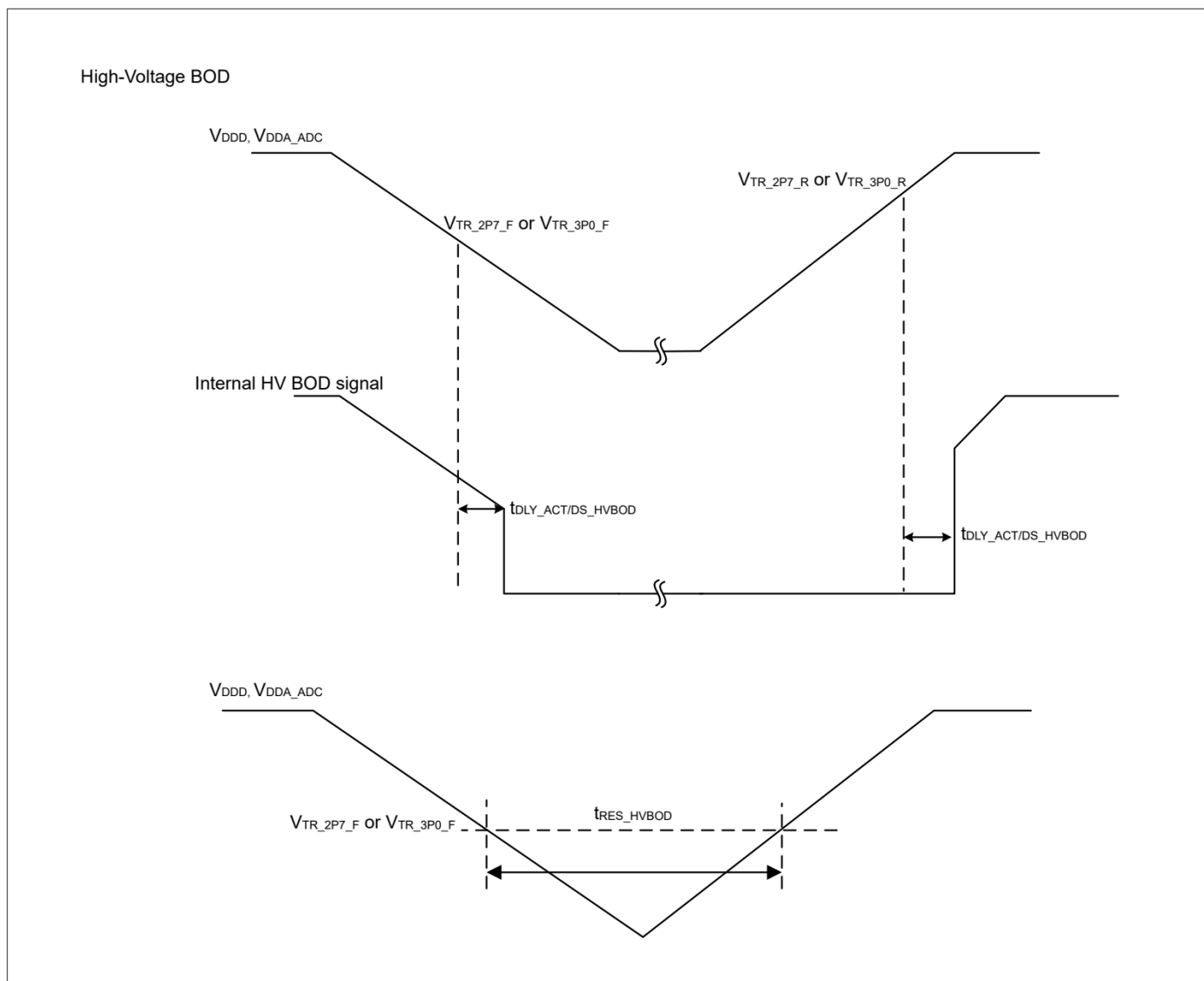


图 25

高压 BOD 规格

26 电气规格

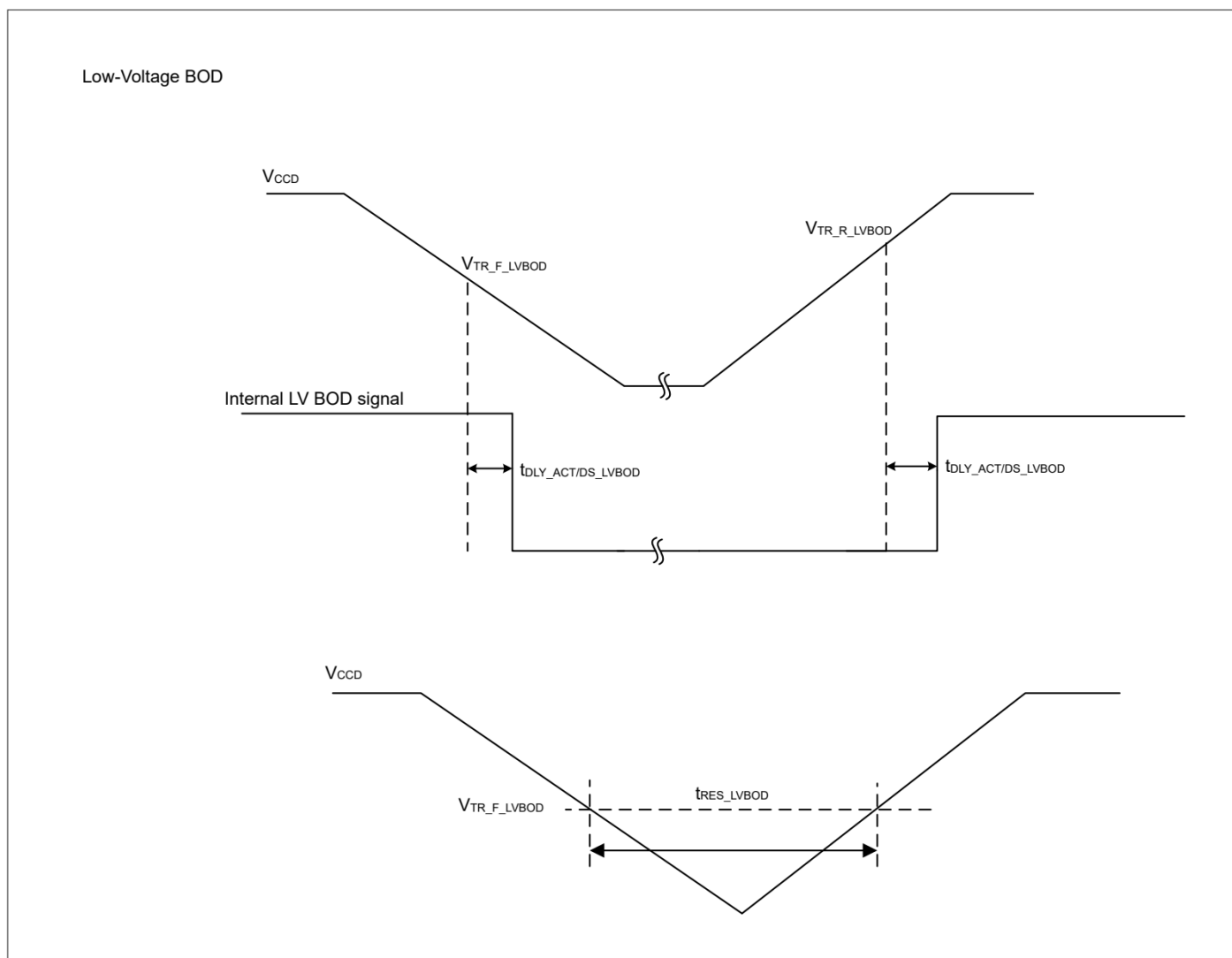


图 26 低压 BOD 规格

26 电气规格

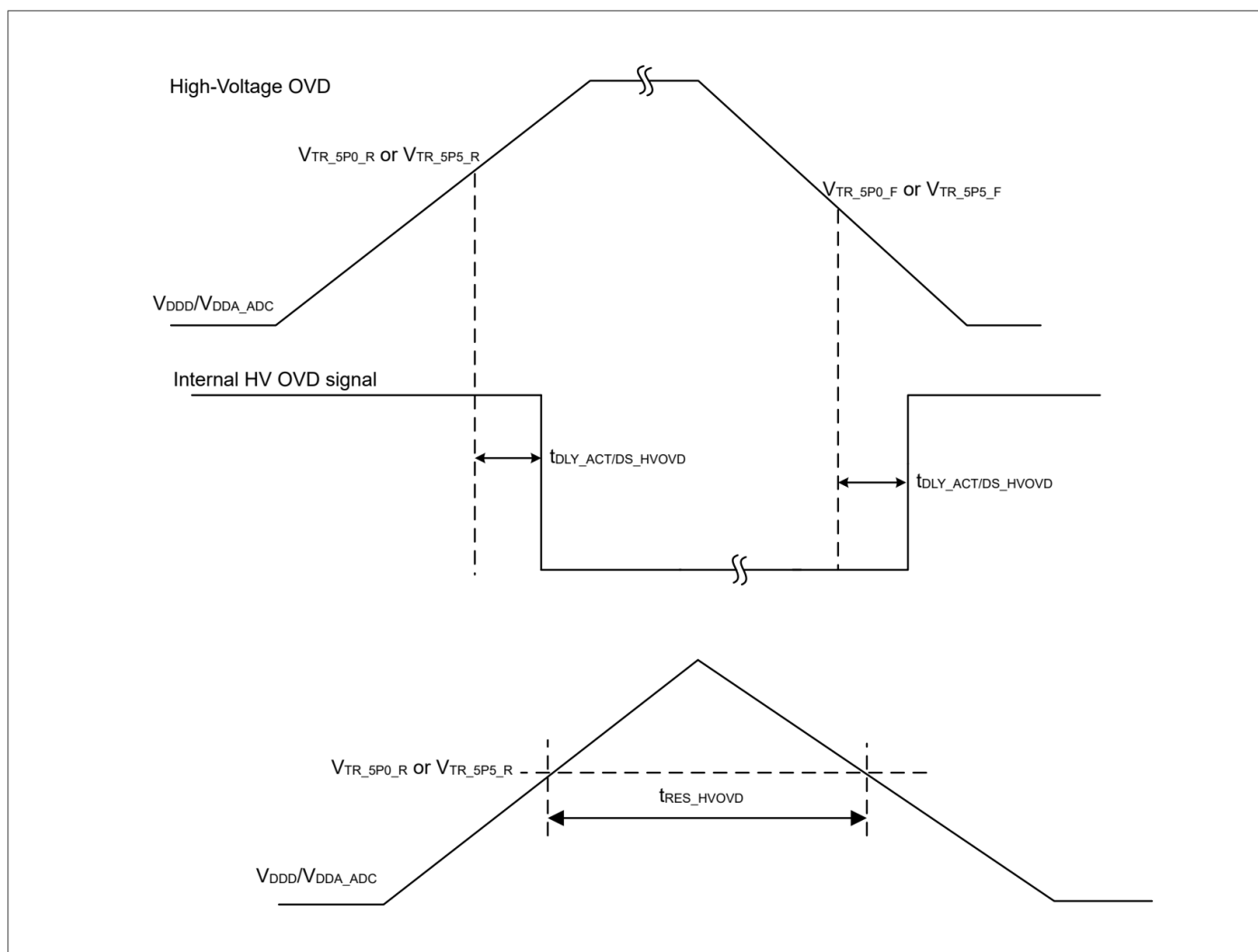


图 27

高压 OVD 规格

26 电气规格

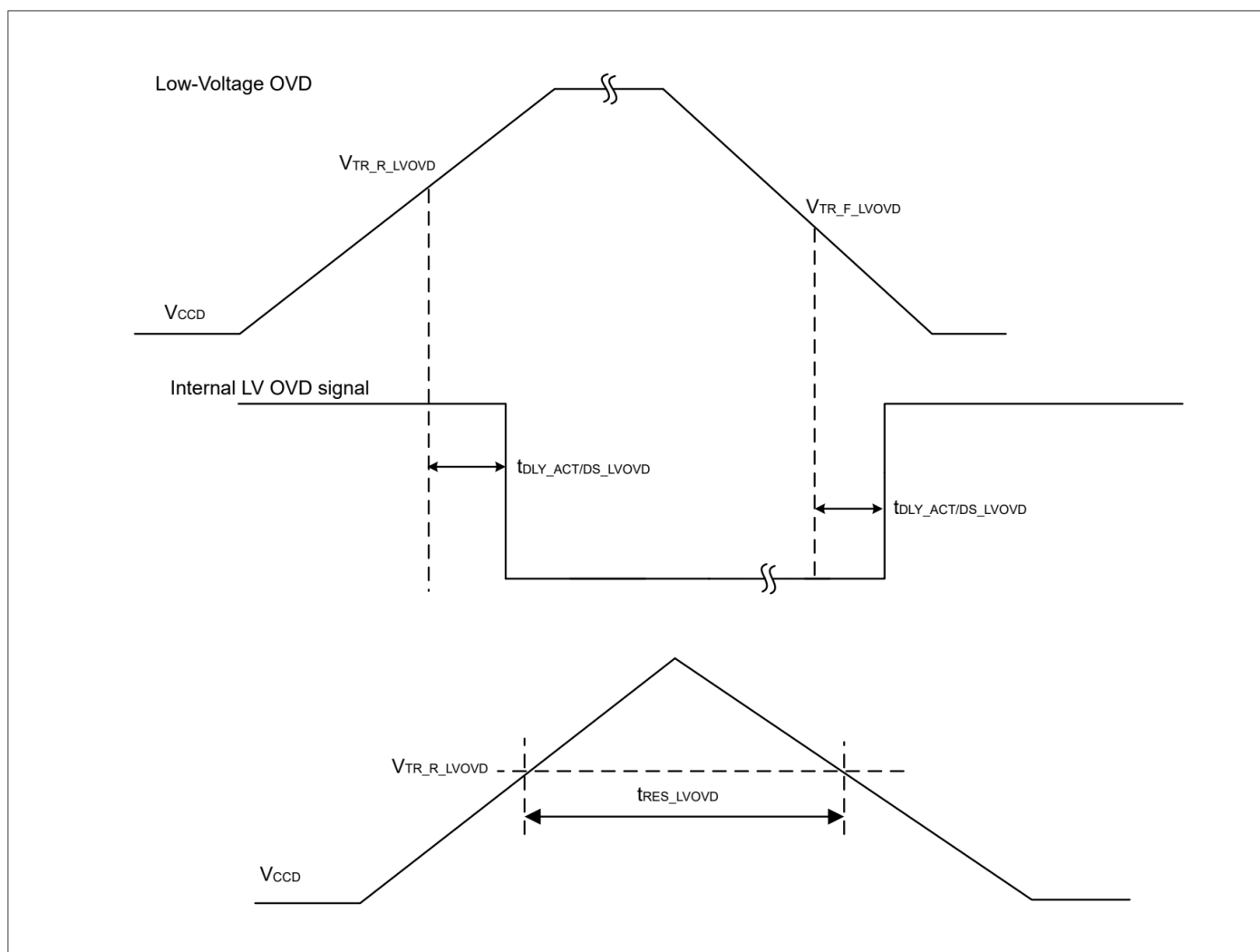


图 28

低压 OVD 规格

26 电气规格

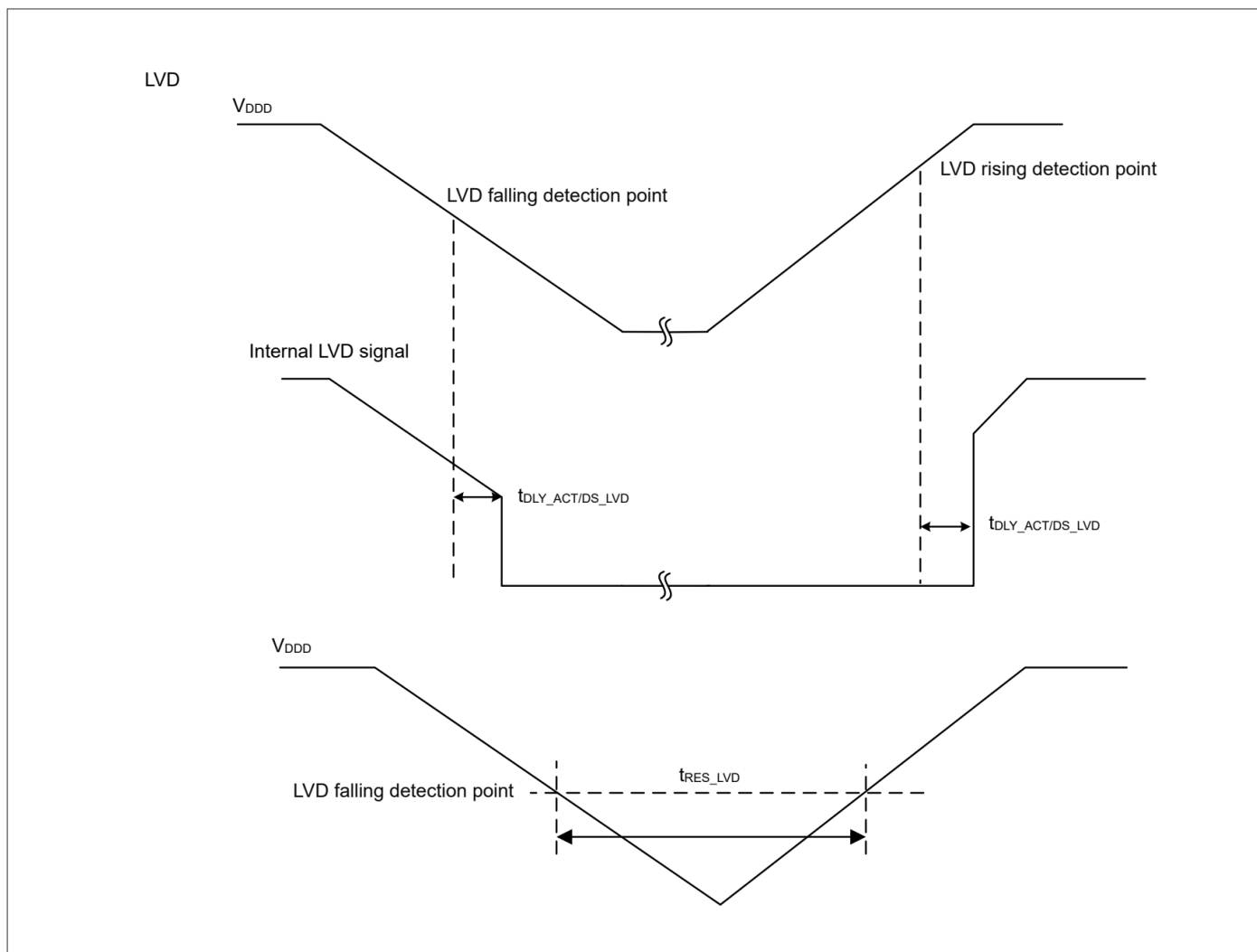


图 29 LVD规格

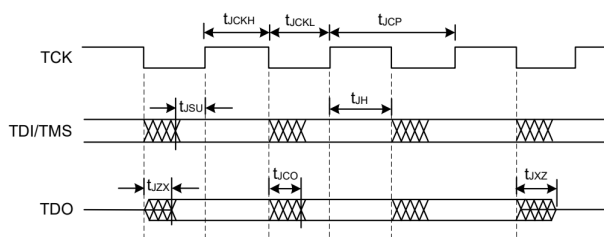
26.9.1 SWD、JTAG 和跟踪规格

表 45 SWD 接口规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置：							
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID300	fSWDCLK	SWD clock input frequency	–	–	10	MHz	$2.7\text{ V} \leq V_{\text{DDIO_GPIO}} \leq 5.5\text{ V}$
SID301	tSWDI_SETUP	SWDI setup time	$0.25 \times T$	–	–	ns	$T = 1 / f_{\text{SWDCLK}}$
SID302	tSWDI_HOLD	SWDI hold time	$0.25 \times T$	–	–	ns	$T = 1 / f_{\text{SWDCLK}}$
SID303	tSWDO_VALID	SWDO valid time	–	–	$0.5 \times T$	ns	$T = 1 / f_{\text{SWDCLK}}$
SID304	tSWDO_HOLD	SWDO hold time	1	–	–	ns	$T = 1 / f_{\text{SWDCLK}}$

26 电气规格
表46 JTAG AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置： GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID620	t _{JCKH}	TCK HIGH time	25	–	–	ns	30-pF load on TDO
SID621	t _{JCKL}	TCK LOW time	25	–	–	ns	30-pF load on TDO
SID622	t _{JCP}	TCK clock period	62.5	–	–	ns	30-pF load on TDO
SID623	t _{JSU}	TDI/TMS setup time	6.25	–	–	ns	30-pF load on TDO
SID624	t _{JH}	TDI/TMS hold time	6.25	–	–	ns	30-pF load on TDO
SID625	t _{JZX}	TDO High-Z to active	–	–	25	ns	30-pF load on TDO
SID626	t _{JXZ}	TDO active to High-Z	–	–	25	ns	30-pF load on TDO
SID627	t _{JCO}	TDO clock to output	–	–	25	ns	30-pF load on TDO


图 30 JTAG 规格
表 47 跟踪规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置： HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1412 A	CTRACE	Trace capacitive load	–	–	30	pF	
SID1412	t _{TRACE_CYC}	Trace clock period	20	–	–	ns	Trace clock cycle time for 50 MHz
SID1413	t _{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width
SID1414	t _{TRACE_CLKH}	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width
SID1415	t _{TRACE_SETUP}	Trace data setup time	2	–	–	ns	Trace data setup time, CLK_PERI ≥ 75 MHz
SID1416	t _{TRACE_HOLD}	Trace data hold time	1	–	–	ns	Trace data hold time, CLK_PERI ≥ 75 MHz

(表格续下页.....)

26 电气规格
表 47 (续) 跟踪规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1415 A	tTRACE_SETUP	Trace data setup time	3	–	–	ns	Trace data setup time, CLK_PERI < 75 MHz
SID1416 A	tTRACE_HOLD	Trace data hold time	2	–	–	ns	Trace data hold time, CLK_PERI < 75 MHz

26.10 时钟规格
表 48 根时钟和中间时钟⁴⁾, ²⁾

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ⁴⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁵⁾			PLL/FLL Clock source: IMO ⁶⁾ , ⁷⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF0	160	PLL200#0	160	NA	NA	153	NA	NA	Root clock for CPUSS, PERI (CLK_MEM)
		FLL	100	NA	NA	100	NA	NA	
	100	PLL200#0	100	NA	NA	95	NA	NA	PERI (CLK_SLOW, CLK_PERI)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF1	240	PLL400#0	240	235	237	229	225	227	CM7 CPU Core#0
		FLL	100	NA	NA	100	NA	NA	
CLK_HF2	100	PLL200#1	100	NA	NA	95	NA	NA	Peripheral clock root other than CLK_PERI (CAN FD, etc.)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF3	100	PLL200#0	100	NA	NA	95	NA	NA	Event generator (CLK_REF), clock output on EXT_CLK pins (when used as output)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF4	50	PLL200#1	50	NA	NA	47	NA	NA	ETH Channel#0. Internal clock 50 MHz for RMII, External PHY provides 25 MHz for MII
		FLL	50	NA	NA	48	NA	NA	
CLK_HF5	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #0 root clock, ETH0 TSU clock (CLK_IF_SRSS0)
		FLL	100	NA	NA	100	NA	NA	

(表格续下页.....)

26 电气规格
表 48 (续) 根时钟和中间时钟^{1), 2)}

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ⁴⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁵⁾			PLL/FLL Clock source: IMO ⁶⁾ , ⁷⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF6	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #1 root clock (CLK_IF_SRSS1)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF7	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #2 root clock (CLK_IF_SRSS2)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF8	266	PLL400#1	200	NA	NA	191	NA	NA	SMIF#0 root clock
		PLL400#2	266	NA	NA	254	NA	NA	
		FLL	NA	NA	NA	NA	NA	NA	
CLK_HF9	266	PLL400#1	200	NA	NA	191	NA	NA	SMIF#1 root clock
		PLL400#2	266	NA	NA	254	NA	NA	
		FLL	NA	NA	NA	NA	NA	NA	
CLK_HF10	203	PLL400#3	203	200	201	195	191	193	Video Subsystem root clock
		FLL	100	NA	NA	100	NA	NA	
CLK_HF11	224	PLL400#4	224	220	222	214	210	212	Display#0 root clock
		PLL200#2	200	NA	NA	191	NA	NA	
		FLL	100	NA	NA	100	NA	NA	
CLK_HF12	163	PLL400#4	163	160	161	156	153	154	Display#1 root clock
		PLL200#2	161	NA	NA	153	NA	NA	
		FLL	100	NA	NA	100	NA	NA	
CLK_HF13	ILO		NA						CSV Dedicated (< 1MHz)
CLK_FAST_0	240	CLK_HF1	240	235	237	229	226	228	CM7 CPU Core#0, intermediate clock
		FLL	100	NA	NA	100	NA	NA	

(表格续下页.....)

26 电气规格
表 48 (续) 根时钟和中间时钟^{1), 2)}

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ⁴⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁵⁾			PLL/FLL Clock source: IMO ⁶⁾ , ⁷⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_MEM	160	CLK_HF0	160	NA	NA	153	NA	NA	Intermediate clock for SMIF, Flash, Ethernet, VIDEOSS
		FLL	100	NA	NA	100	NA	NA	
CLK_SLOW	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, VIDEOSS
		FLL	100	NA	NA	97	NA	NA	
CLK_PERI	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_HF0, intermediate clock for IOSS, TCPWM0, CPU trace, SMIF, Sound Subsystem, Ethernet
		FLL	100	NA	NA	97	NA	NA	

1) 未列出的中间时钟具有与其父时钟相同的限制。

2) 表格显示了根时钟 (CLK_HF_x) 与 PLL 之间的保证映射关系。

3) 相应时钟源 (PLL/FLL + 分频器) 之后的最大时钟频率。所有内部公差和影响都包含在这些频率内。

4) 相应时钟源 (PLL/FLL + 分频器) 之后的最大时钟频率。所有内部公差和影响都包含在这些频率内。

5) 对于 ECO, LPECO: 设计可容忍外部时钟源高达 ±150 ppm 的不确定度。

6) IMO 操作频率公差包括在内。

7) 通过设计保证了使用 IMO/FLL 以 100 MHz 的频率执行 ROM 和闪存启动。

表 49 PLL400 操作模式

PLL400 operation mode	Spread spectrum clock generation (SSCG)	Fractional
Integer	OFF	OFF
SSCG	ON	OFF
Fractional	OFF	ON

表 50 IMO AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID310	f _{IMO}	IMO operating frequency	7.632	8	8.368	MHz	Accuracy after factory trimming
SID311	t _{STARTIMO}	IMO startup time	–	–	7.5	μs	Startup time to 90% of final frequency
SID312	I _{IMO_ACT}	IMO current	–	13.5	22	μA	Guaranteed by design

26 电气规格
表 51 ILO AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID320	f _{ILOTRIM}	ILO operating frequency	30.965	32.768	34.57	kHz	5.5% accuracy after factory trimming
SID321	t _{STARTILO}	ILO startup time	–	8	12	µs	Startup time to 90% of final frequency
SID323	I _{ILO}	ILO current	–	500	2800	nA	Guaranteed by design

表 52 LPECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID325	f _{LPECO}	LPECO operating frequency	3.99	–	8.01	MHz	Drive level protection DL ≥ 100 µW, ESR ≤ 200 Ω Crystal load capacitance (C _L) 5 pF to 25 pF
SID329	I _{LPECO_4M}	LPECO current at 4 MHz	–	93	110	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID354	I _{LPECO_4M}	LPECO current at 4 MHz	–	97	125	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID326	I _{LPECO_4M}	LPECO current at 4 MHz	–	106	145	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID355	I _{LPECO_4M}	LPECO current at 4 MHz	–	115	155	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID356	I _{LPECO_8M}	LPECO current at 8 MHz	–	140	165	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID357	I _{LPECO_8M}	LPECO current at 8 MHz	–	149	175	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID327	I _{LPECO_8M}	LPECO current at 8 MHz	–	165	190	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0

(表格续下页.....)

26 电气规格

表 52 (续) LPECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID358	ILPECO_8M	LPECO current at 8 MHz	–	183	220	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b 0
SID328	tSTART_LPECO	LPECO startup time ¹⁾	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (BACKUP_LPECO_CTL.LPECO_ EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_LPECO_STATUS.LPE CO_READY<0:0>=0b1 and BACKUP_LPECO_STATUS.LPE CO_AMPDET_OK<0:0>=0b1).

1) 振荡器启动时间是一个性能参数，主要取决于所选的外部晶振和负载电容。

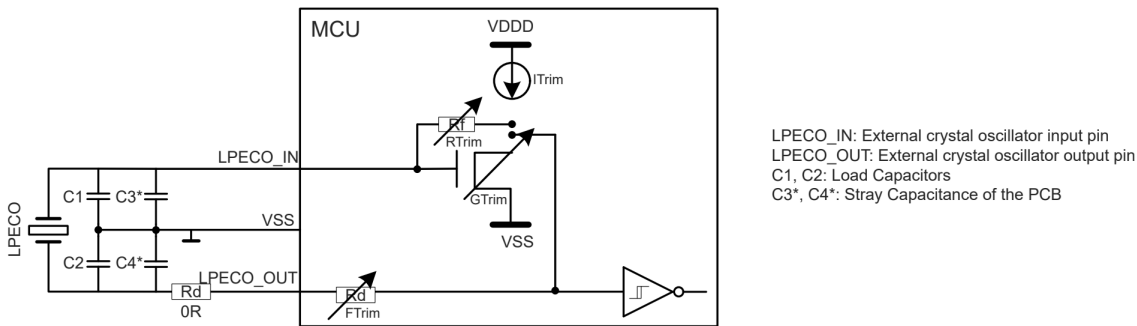


图 31 LPECO 连接方案²⁰⁾

表 53 ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID330	fECO	Crystal frequency range	7.2	–	33.34	MHz	
SID332	RFBK	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100 kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design

(表格续下页.....)

²⁰⁾ 有关晶振要求的更多信息，请参阅特定系列的架构 TRM (002-25800, TRAVEO™ T2G Automotive MCU cluster 2D 架构技术参考手册)。

26 电气规格

表 53 (续) ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID333	I _{ECO3}	ECO current at T _J = 150°C	–	1200	2000	μA	Maximum operation current with a 33-MHz crystal, max 18-pF load
SID334	t _{START_7.2M}	7.2-MHz ECO startup time ¹⁾	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.CO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.CO_OK<0:0>=0b1 and CLK_ECO_STATUS.CO_READY<0:0>=0b1).
SID335	t _{START_33M}	33-MHz ECO startup time ¹⁾	–	–	1	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.CO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.CO_OK<0:0>=0b1 and CLK_ECO_STATUS.CO_READY<0:0>=0b1).

1) 振荡器启动时间是一个性能参数, 主要取决于所选的外部晶振和负载电容。

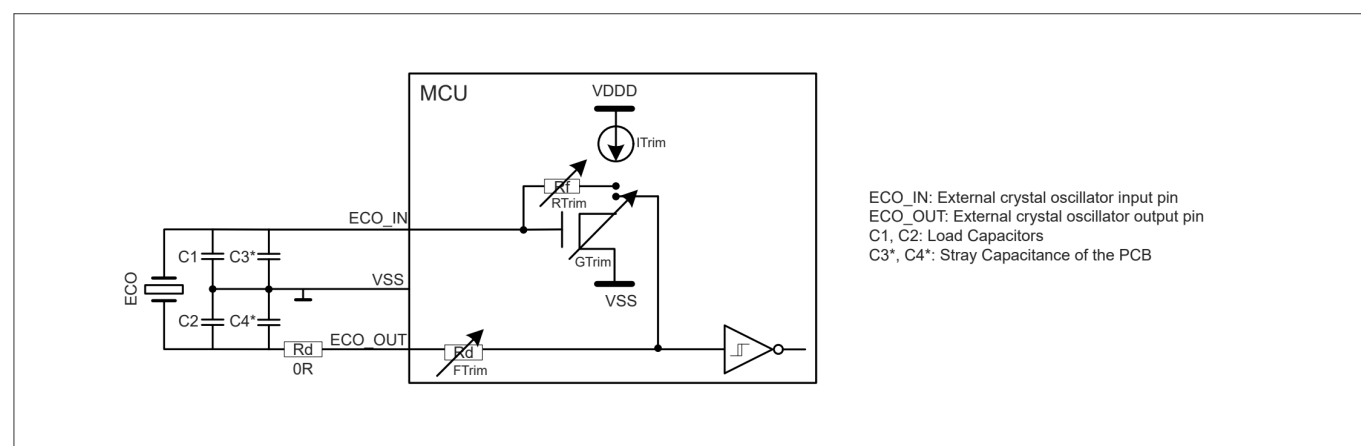


图 32 ECO 连接方案 ²⁰⁾

²⁰ 有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-25800，TRAVEO™ T2G Automotive MCU cluster 2D 架构技术参考手册）。

26 电气规格
表 54 PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
PLL Specifications for “PLL without SSCG and Fractional Operation” (PLL200)							
SID340	t _{PLL200_LOCK}	Time to achieve PLL lock	–	–	35	μs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SID341	f _{OUT}	Output frequency from PLL block (PLL_OUT)	10.99 8	–	200.0 3	MHz	
SID346	f _{IN}	PLL input frequency (Reference Clock f _{REF})	3.988	–	33.34	MHz	
SID347	I _{PLL_200M}	PLL operating current	–	0.87	1.85	mA	f _{OUT} = 200 MHz
SID348C	f _{PLL_VCO}	VCO frequency, clock output of 'Voltage Control Oscillator (VCO)'	169.9 745	–	400.0 6	MHz	
SID349C	f _{PLL_PFD}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	8.001 2	MHz	
SID342	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by design f _{PLL_VCO} : 320 MHz or 400 MHz f _{PLL_OUT} : 40 MHz to 200 MHz f _{PLL_PFD} : 8 MHz f _{PLL_IN} : ECO
SID343	PLL_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns Guaranteed by design f _{PLL_VCO} : 320 MHz or 400 MHz f _{PLL_OUT} : 40 MHz to 200 MHz f _{PLL_PFD} : 8 MHz f _{PLL_IN} : ECO

(表格续下页.....)

26 电气规格
表 54 (续) PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID344	PLL_LJIT3	Long term jitter	-0.5	-	0.5	ns	For 1000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SID345A1	PLL_LJIT5	Long term jitter	-0.75	-	0.75	ns	For 10000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO

PLL Specifications for “PLL with SSCG and Fractional Operation” (PLL400)

SID340A	$t_{\text{PLL400_LOCK}}$	Time to achieve PLL lock	-	-	50	μs	
SID341A	f_{OUT}	Output frequency from PLL block (PLL_OUT)	24.99 6	-	400.0 6	MHz	
SID343A	SPREAD_D	Spread spectrum modulation depth	0.5	-	3	%	Downspread only, triangle modulation
SID343B	$f_{\text{SPREAD_MR}}$	Spread spectrum modulation rate	-	-	32	kHz	Selected by modulation divider from f_{PFD}
SID346A	f_{IN}	PLL input frequency (Reference Clock f_{REF})	3.988	-	33.34	MHz	
SID347A	$I_{\text{PLL_400M}}$	PLL operating current	-	1.4	2.2	mA	$f_{\text{OUT}} = 400 \text{ MHz}$
SID348A	$f_{\text{PFD_S}}$	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	-	20.00 3	MHz	Fractional operation OFF
SID349A	$f_{\text{PFD_F}}$	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	7.998 8	-	20.00 3	MHz	Fractional operation ON
SID345A	f_{VCO}	VCO frequency, Clock output of 'Voltage Control Oscillator (VCO)'	399.9 4	-	800.1 2	MHz	

(表格续下页.....)

26 电气规格
表 54 (续) PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID342D1	PLL400_LJIT1	Long term jitter	-0.25	-	0.25	ns	For 125 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz
SID343D1	PLL400_LJIT2	Long term jitter	-0.5	-	0.5	ns	For 500 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz
SID344D1	PLL400_LJIT3	Long term jitter	-1	-	1	ns	For 1000 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz
SID345E1	PLL400_LJIT5	Long term jitter	-1.5	-	1.5	ns	For 10000 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz

表 55 FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	-	-	5	μs	Wakeup with < 10°C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value

(表格续下页.....)

26 电气规格

表 55 (续) FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID351	f _{FLL_OUT}	Output frequency from FLL block	24	–	100	MHz	Output range of FLL divided-by-2 output
SID352	FLL_CJIT	FLL frequency accuracy	–1	–	1	%	This is added to the error of the source
SID353	f _{FLL_IN}	Input frequency	0.25	–	100	MHz	

表 56 WCO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	fwco	Watch crystal frequency	–	32.768	–	kHz	Tuning Fork Crystal with following parameters: DL (drive level) ≥ 0.5 μW, ESR ≤ 130 kΩ
SID361	WCO_DC	WCO duty cycle	10	–	90	%	
SID362	t _{START_WCO}	WCO start up time ¹⁾	–	–	1000	ms	Time from oscillator enable (BACKUP_CTL.WCO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_STATUS.WCO_OK<0:0>=0b1)
SID363	I _{wco}	WCO current	–	1.4	–	μA	AGC=OFF

1) 振荡器启动时间是一个性能参数，主要取决于所选的外部晶振和负载电容。

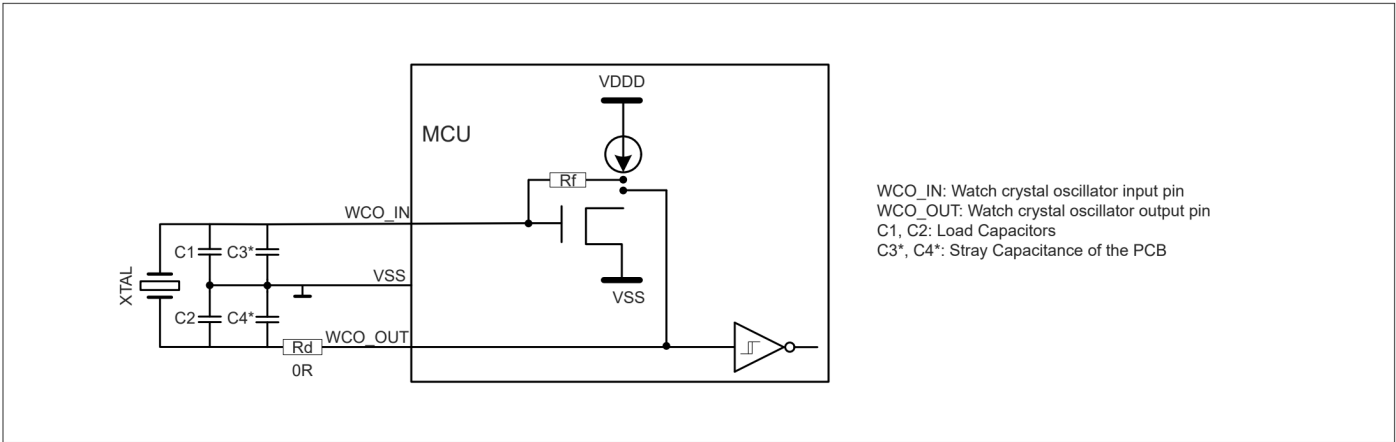


图 33 WCO 连接方案 ²¹⁾

²¹⁾ 有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-25800，TRAVEO™ T2G Automotive MCU cluster 2D 架构技术参考手册）。

26 电气规格
表 57 外部时钟输入规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f _{EXT}	External clock input frequency	0.25	–	100	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	Duty cycle	45	–	55	%	

表 58 MCWDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID410	t _{MCWDT1}	Minimum MCWDT timeout	57.85	–	–	μs	When using the ILO (32 kHz + 5.5%) and 16-bit MCWDT counter Guaranteed by design
SID411	t _{MCWDT2}	Maximum MCWDT timeout	–	–	2.12	s	When using the ILO (32 kHz – 5.5%) and 16-bit MCWDT counter Guaranteed by design

表 59 WDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID412	t _{WDT1}	Minimum WDT timeout	57.85	–	–	μs	When using the ILO (32 kHz + 5.5%) and 32-bit WDT counter Guaranteed by design
SID413	t _{WDT2}	Maximum WDT timeout	–	–	38.53	h	When using the ILO (32 kHz – 5.5%) and 32-bit WDT counter Guaranteed by design
SID414	t _{WDT3}	Default WDT timeout	–	1000	–	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design

26.11 以太网规格
表 60 以太网规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Ethernet General Specifications							

(表格续下页...)

26 电气规格
表 60 (续) 以太网规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID364	C _L	Load capacitance	–	–	20	pF	for all between MAC and PHY for MII-IF, RMII-IF, MDC/MDIO-IF
SID368	f _{sys}	System clock max frequency	–	–	100	MHz	Guaranteed by design
SID369	f _{AXI}	AXI clock max frequency	–	–	200	MHz	Guaranteed by design

Ethernet MII Specifications
建议 I/O 配置:

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b1, CFG_SLEW_EXT/SLEW<0:0>= 0b0

SID370	t _{TXCYC}	MII tx_clk cycle	39.5	40	40.5	ns	
SID371	t _{RXCYC}	MII rx_clk cycle	39.5	40	40.5	ns	
SID372	t _{SKEWT}	MII Transmit data (txd,tx_en,tx_er) valid after tx_clk	0.5	–	25	ns	
SID373	t _{SUR}	MII Receive data setup to rx_clk rising edge	10	–	–	ns	
SID374	t _{HOLDR}	MII Receive data hold to rx_clk rising edge	10	–	–	ns	
SID375	f _{TXRX_CLK}	MII TX/RX_CLK Clock frequency	–100 ppm	25	+100 ppm	MHz	
SID376A	DUTY_REF	Duty cycle of reference clock	40	–	60	%	
SID365A	t _{RF}	Input rise / fall time	–	–	2	ns	20% to 80%
SID365E	t _{RFO}	Output rise / fall time	–	–	6.5	ns	20% to 80%

Ethernet RMII Specifications
建议 I/O 配置:

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b1, CFG_SLEW_EXT/SLEW<0:0>= 0b0

SID375A	f _{REF_CLK}	RMII reference clock frequency (input)	–50 ppm	50	+50 ppm	MHz	
SID375B	f _{REF_CLK_OUT}	RMII reference clock frequency (output)	–50 ppm	50	+50 ppm	MHz	
SID376	DUTY_REF	Duty cycle of reference clock	40	–	60	%	

(表格续下页.....)

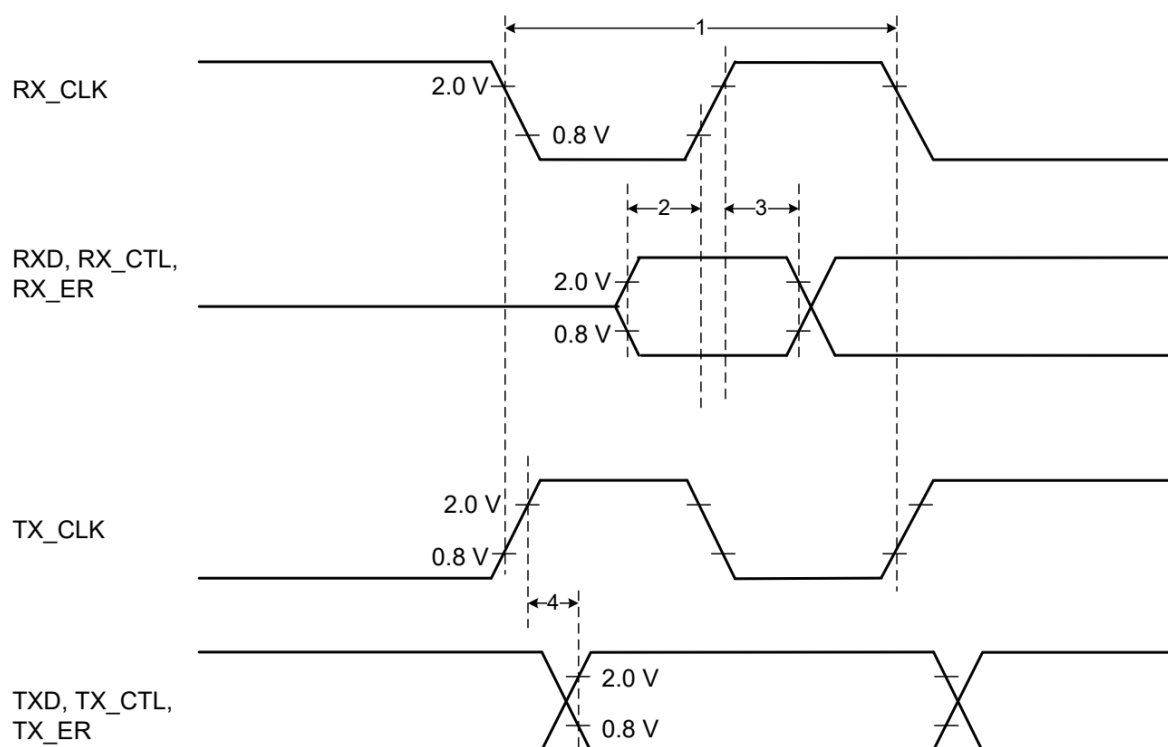
26 电气规格
表 60 (续) 以太网规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID377	tsu	RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge.	4	–	–	ns	
SID378	tHOLD	RXD[1:0], CRS_DV, RX_ER, Data hold from REF_CLK rising edge	2	–	–	ns	
SID379A	tTXOUTE	External clock mode. TXD[1:0], TX_EN Data output delay from REF_CLK rising edge	2	–	14	ns	
SID379B	tTXOUTI	Internal clock mode. TXD[1:0], TX_EN Data output delay from REF_CLK rising edge	2	–	16	ns	
SID365C	tRF	Input rise / fall time	–	–	2	ns	20% to 80%
SID365F	tRFO	Output rise / fall time	–	–	6.5	ns	20% to 80%

Ethernet MDIO Specifications

SID395	tMDCYC	MDC clock cycle	400	–	–	ns	
SID395A	tHL_MDC	MDIO Minimum high and low times for MDC	160	–	–	ns	
SID396	tMDIS	MDIO input setup time to MDC rising edge	100	–	–	ns	
SID397	tMDIH	MDIO input hold time to MDC rising edge	0	–	–	ns	
SID398	tMDIO	MDIO output skew from MDC rising edge	10	–	390	ns	
SID365D	tRF	Input rise / fall time	–	–	2	ns	20% to 80%
SID365G	tRFO	Output MDIO rise / fall time	–	–	6.5	ns	20% to 80%

26 电气规格



- 1: RX_CLK or TX_CLK cycle = $1/f_{\text{TXRX_CLK}}$
- 2: MII receive data setup time to RX_CLK rising edge = t_{SUR}
- 3: MII receive data hold time to RX_CLK rising edge = t_{HOLDR}
- 4: MII transmit data valid after TX_CLK rising edge = t_{SKEWT}

图 34

MII 时序图

26 电气规格

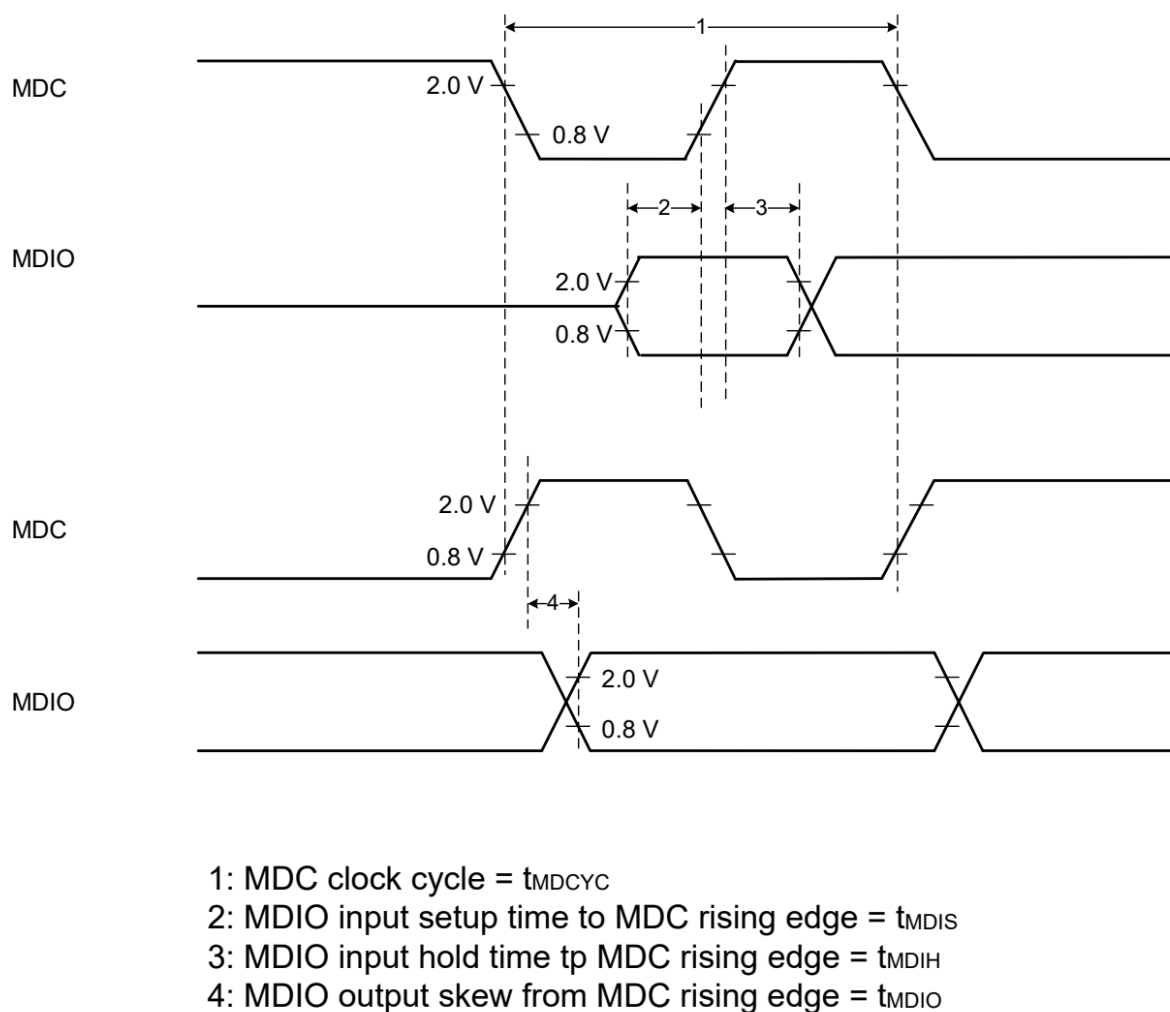


图 35

MDIO 时序图

26 电气规格

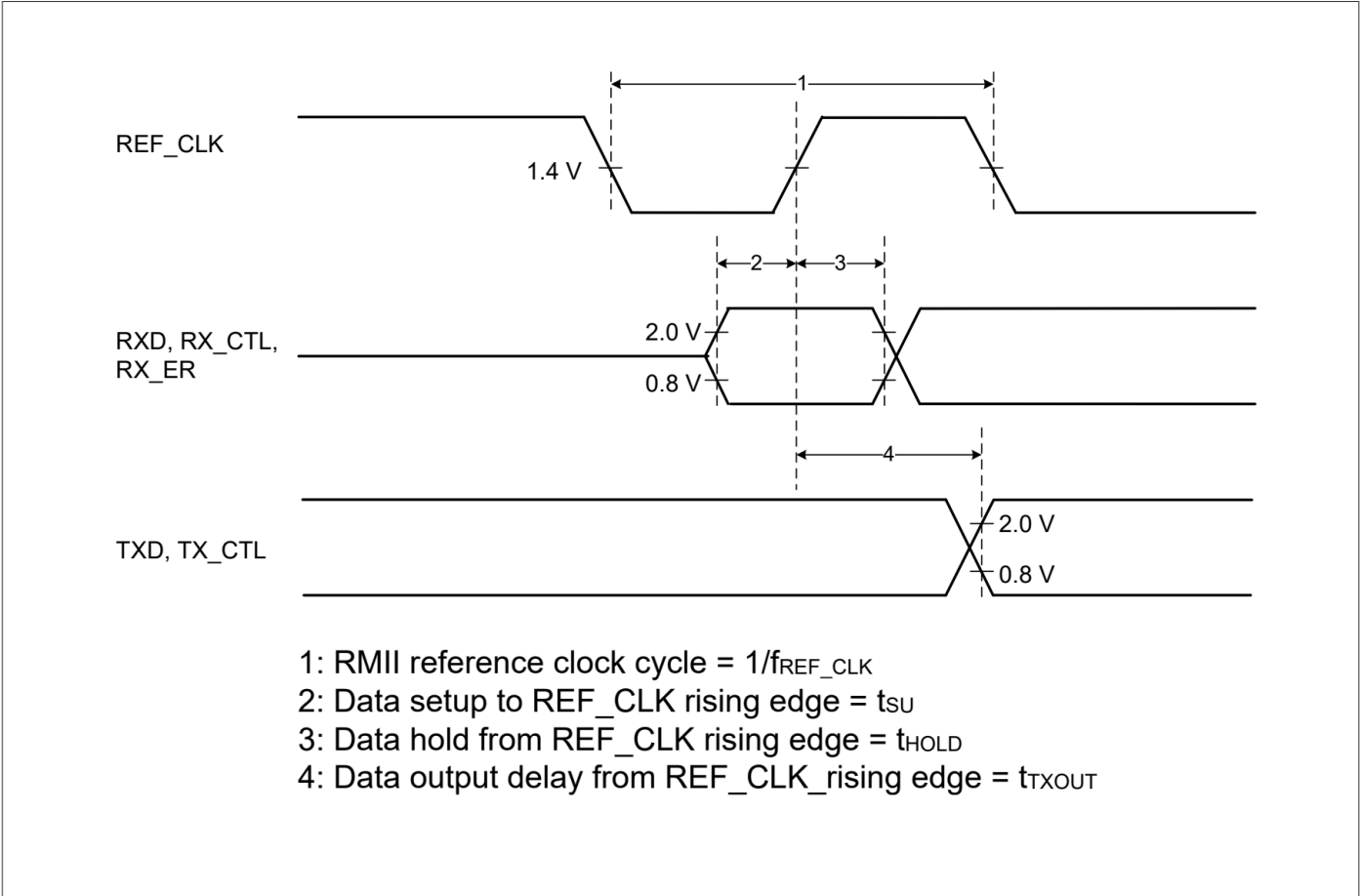


图 36 RMII 时序图

26.11.1 最低总线频率要求

下表详细说明了所有可能的以太网配置和 MAC 速度所需的最低工作频率。以太网模块使用 AXI 接口进行 DMA 访问。

表 61 MAC 速度的最小 AXI 频率

DMA bus width	MAC rate	Minimum AXI frequency
64	100 Mbps	10 MHz
64	10 Mbps	10 MHz

26.12 声音子系统规格

表 62 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
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I2S I/O settings

建议 I/O 配置

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<2:0> = 0b000

I2S Serial Clock Frequency

(表格续下页...)

26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID796	tsCLK	Serial clock period	162	–	–	ns	Guaranteed by design No feature is used for low frequency I2S operation: DUT RX Master: * RX_IF_CTL.LATE_SAMPLE = 0 * RX_IF_CTL.LATE_CAPTURE = 0b00 DUT TX Slave: No special configuration DUT RX Slave: * RX_IF_CTL.LATE_SAMPLE = 0
SID797	tHC	Serial clock high time	$0.35 \times \text{tsCLK}$	–	–	ns	Guaranteed by design
SID798	tLC	Serial clock low time	$0.35 \times \text{tsCLK}$	–	–	ns	Guaranteed by design
SID799	tMCLK	Master clock period	20	–	–	ns	Guaranteed by design

I²S Transmitter Timing

SID740	tDTR	Delay from rising edge of TX_CLK to transition on TX_SD/ TX_FSYNC (WS)	–	–	$0.8 \times \text{tsCLK}$	ns	Guaranteed by design
SID741	tHTR	Hold from rising edge of TX_CLK to transition on TX_SD/ TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID743	tHR_WS_POL_0	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	

I²S Receiver Timing

SID751	tsR	Setup on RX_SD/ RX_FSYNC (WS) before the rising edge to RX_CLK	$0.2 \times \text{tsCLK}$	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE or SCK_POLARITY setting
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(表格续下页.....)

26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID752	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the rising edge to RX_CLK	0	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0
SID753	t _{SCLK_TRANS}	SCLK transition timing	1	–	8	ns	20% to 80%
SID754	t _{MCLK_TRANS}	MCLK transition timing	1	–	8	ns	20% to 80%
SID755	t _{DATA_TRANS}	DATA transition timing	1	–	8	ns	20% to 80%

TDM I/O Settings
建议 I/O 配置
对于高于 25 MHz 的串行时钟

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<0:0> = 0b0

对于高达 25 MHz 的串行时钟

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0,
CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<0:0> = 0b0

TDM Serial Clock

SID1000A	t _{SCLK}	Serial clock period, TDM[x] (x=0 through 3)	20	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: not supported at 50 MHz TX Slave: not supported at 50 MHz RX Slave: not supported at 50 MHz
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26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1000B	tsCLK	Serial clock period, TDM[x] (x=0 through 3)	40	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX Slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX Slave: RX_IF_CTL.SCK_POLARITY= 0
SID1001	thC	Serial clock high time	$0.35 \times tsCLK$	–	–	ns	Guaranteed by design
SID1002	tlC	Serial clock low time	$0.35 \times tsCLK$	–	–	ns	Guaranteed by design
SID1010	tMCLK	Master clock input period	10	–	–	ns	MCLK must be SCLK*2; The maximum output frequency of the TDM depends on the used I/O type.
SID1002A	tMCLK	Master clock output period	20	–	–	ns	
SID1002D	tMCLK_IH	Master clock input high time	$0.45 \times tMCLK$	–	–	ns	
SID1002E	tMCLK_IL	Master clock input low time	$0.45 \times tMCLK$	–	–	ns	
SID1002F	tMCLK_OH	Master clock output high time	$0.35 \times tMCLK$	–	–	ns	
SID1002G	tMCLK_OL	Master clock output low time	$0.35 \times tMCLK$	–	–	ns	
TDM Transmit Timing							
SID1003	tDTR	Delay from rising edge of TX_CLK to transition on TX_SD/ TX_FSYNC (WS)	–	–	$0.8 \times tsCLK$	ns	Guaranteed by design

(表格续下页.....)

26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1004	t _{HTR}	Hold from rising edge of TX_CLK to transition on TX_SD/ TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID1011	t _{HR_WS_POL_0}	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	
SID1012	t _{HR_WS_POL_1}	TX Slave: Hold on TX_FSYNC (WS) after the 2nd edge following the driving edge of TX_CLK (SCK_POLARITY = 1, zero-cycle hold)	1.8	–	–	ns	

TDM Receive Timing

SID1005	t _{SR}	Setup on RX_SD/ RX_FSYNC (WS) before the 1st edge following the driving edge of RX_CLK	0.2 × t _{SCLK}	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE and SCK_POLARITY setting
SID1006	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 1st edge following the driving edge of RX_CLK	0	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 × t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0
SID1006A	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 2nd edge following the driving edge of RX_CLK	0	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 2nd edge (1 × t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 1, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 1

(表格续下页.....)

26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1006B	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 3rd edge following the driving edge of RX_CLK	0	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 3rd edge (1.5 x t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b01 RX Slave: Not Applicable

TDM Transition Timing

SID1007	t _{SCLK_TRANS}	SCLK input/output transition timing	–	–	0.15 × t _{SCLK}	ns	Guaranteed by design
SID1008	t _{MCLK_TRANS}	MCLK input/output transition timing	–	–	0.15 × t _{SCLK}	ns	Guaranteed by design
SID1009	t _{DATA_TRANS}	DATA input/output transition timing	–	–	0.15 × t _{SCLK}	ns	Guaranteed by design

(PCM) PWM
建议 I/O 配置
HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_SLEW_EXT/SLEW<0:0> = 0b0

SID1100_1	tpw_1	Pulse width on CH1_P, CH1_N, CH2_P, CH2_N for HSIO_STDLN	8	–	–	ns	PWM clock ≤ 100MHz, min pulse width nom. 10 ns – 20% max distortion Guaranteed by design
SID1101	f _{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1110	t _{MCLK}	Master clock input period	10	–	–	ns	Guaranteed by design
SID1111	t _{MCLKI_DUTY}	Master clock input duty cycle	40	–	50	%	Guaranteed by design

Sound Generator
建议 I/O 配置
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_SLEW_EXT/SLEW<0:0> = 0b0

SID1102	f _{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
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26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1103	tMCLK	Master clock input period	10	–	–	ns	Guaranteed by design
SID1104	tMCLKI_DUTY	Master clock input duty cycle	40	–	50	%	Guaranteed by design

AudioDAC

SID1300	fCLKDA0	System clock frequency	2.048	–	18.432	MHz	All parameters specified f _s = 44.1 kHz, system clock 256 × f _s and 16-bit data, R _L = 20 kΩ, C _L = 100 pF, unless otherwise noted
SID1301	f _s	Sampling clock	8	–	48	kHz	
SID1302	R _L	Analog output load resistance	20	–	–	kΩ	DAC_L, DAC_R
SID1303	C _L	Analog output load capacitance	–	–	100	pF	DAC_L, DAC_R
SID1304	C _{COM}	Com Capacitance	2.2	–	10	μF	C_L, C_R
SID1305	VOUT_MAX	Analog output single-end output range (±full scale)	0.655 × V _{DDA_D AC}	0.673 × V _{DDA_D AC}	0.690 × V _{DDA_DAC}	V _{P-P}	DAC_L, DAC_R, R _L = 20 kΩ, C _L = 100 pF
SID1306	VOUT_ZERO	Analog output voltage (zero)	0.49 × V _{DDA_D AC}	0.5 × V _{DDA_D AC}	0.51 × V _{DDA_DAC}	V	DAC_L, DAC_R
SID1307	THD + N	THD + N (Signal to Noise + Distortion ratio)	–	–82	–72	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f _c : 20 kHz)
SID1308	SNR	Signal to Noise ratio	85	89	–	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f _c : 20 kHz) A-weighting filter

(表格续下页.....)

26 电气规格
表 62 (续) 声音子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1309	DR	Dynamic range	83	86	–	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f_c : 20 kHz) A-weighting filter
SID1310	GAIN_MM	Gain mismatch between channels	–	–	0.4	dB	Signal frequency: 1 kHz
SID1312	CH_SEP	Channel Separation	–	80	–	dB	
SID1313	Z _{OUT}	Output impedance	150	200	250	Ω	
SID1314	PSRR_50	PSRR @ 50 Hz, digital input = 0	–	–35	–	dB	Digital input: zero noise 50 Hz
SID1315	PSRR_1K	PSRR @ 1 kHz, digital input = 0	–	–50	–	dB	Digital input: zero noise 1kHz
SID1316	PSRR_20K	PSRR @ 20 kHz, digital input = 0	–	–40	–	dB	Digital input: zero noise 20 kHz
SID1318	I _{DD}	Supply current normal operation	–	2.2	3.2	mA	
SID1319	I _{DD_OFF}	Supply current power-down	–	1	100	μA	Typ: T _A = 25°C, V _{DDA_DAC} = 5.0 V, process typ (TT) Max: T _A = 105°C, V _{DDA_DAC} = 5.5 V, process worst (FF) For S-grade devices
SID1319_125	I _{DD_OFF}	Supply current power-down	–	1	100	μA	Typ: T _A = 25°C, V _{DDA_DAC} = 5.0 V, process typ (TT) Max: T _A = 125°C, V _{DDA_DAC} = 5.5 V, process worst (FF) For E-grade devices
SID1320	t _{START}	Startup Time	–	–	70	ms	C _L and C _R should be 2.2 μF

26 电气规格
26.13 CXPI 规格
表 63 CXPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1400	fCLK_AHB	CLK_PERI clock frequency	–	–	100	MHz	Guaranteed by design, AHB Interface clock
SID1402	tBIT_CONT	Width of clock disparity against the bit width t _{BIT_REF} of nominal signaling rate	–0.5	–	+0.5	%	Guaranteed by design
SID1403	trx_0_HI_CONT	The time that should be detected the receiving node is HIGH level.	0.02	–	–	tBIT	tBIT = 1 / fBRC, Guaranteed by design
SID1404	ttX_DIF_CONT	Difference of width of LOW-level at the constant threshold that receiving node should discriminate logic '1' and logic '0'	0.05	–	–	tBIT	tBIT = 1 / fBRC, Guaranteed by design ttX_DIF_CONT = ttX_0_LO – ttX_1_LO
SID1405	ttX_0_PD_C _{ONT} ¹⁾	At the time of logical value '0' outputs, time from the LOW level detection of the communication bus unit falling the voltage "TH_dom".	–	–	0.01	tBIT	tBIT = 1 / fBRC, CTL0.FILTER_EN bit = '0', Guaranteed by design
SID1406	ttX_0_PD_C _{ONT} ¹⁾	At the time of logical value '0' outputs, time from the LOW-level detection of the communication bus unit falling the voltage "TH_dom".	–	–	0.0125	tBIT	tBIT = 1 / fBRC, CTL0.FILTER_EN bit = '1', Guaranteed by design
SID1407	trx_0_FF_CONST	Delay from external serial data input pin to a flop. This is a standard to satisfy AC.11.	–	–	20	ns	Guaranteed by design
SID1408	ttX_0_FF_CONST	Delay from a flop to external serial data output pin. This is a standard to satisfy AC.11.	–	–	80	ns	Guaranteed by design
SID1409	BR	Bit rate	–	–	20	kbps	
SID1411	OS	Oversampling factor	–	–	400		

1) 根据 CXPI 控制器规格, AC 规格最大为 0.01 t_{BIT0}。根据 CXPI 系统规格, AC 规格 (包括收发器或驱动器/接收器) 最大为 0.1 t_{BIT0}。

26 电气规格

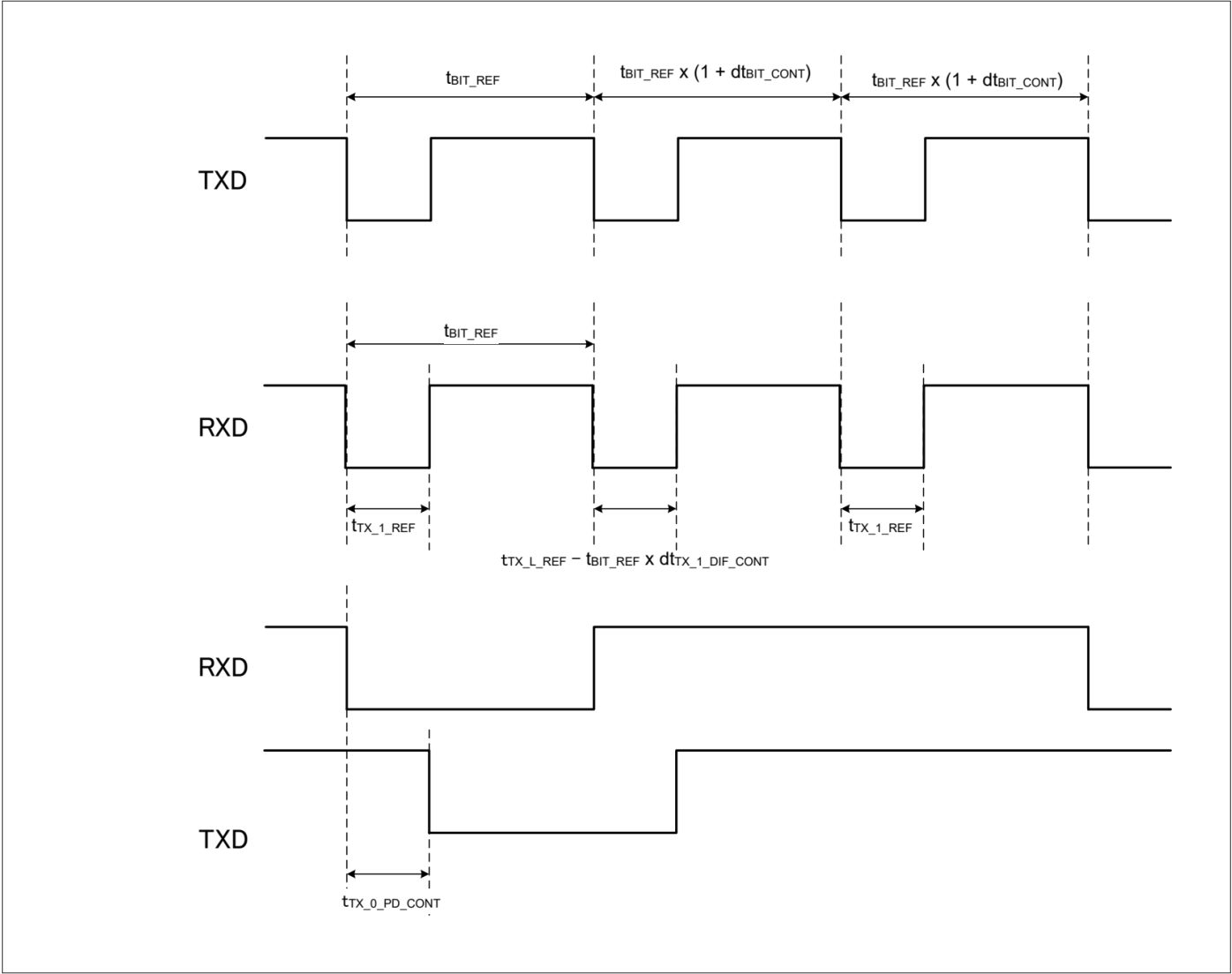


图 37 CXPI 规格

26.14 串行存储器接口规格

表 64 xSPI 规格

Spec ID	Parameter	Description	Min	Max	Min	Max	Units
xSPI (JEDEC JESD251)			xSPI266		xSPI200		
建议 I/O 配置							
xSPI266: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single and dual slave [load ≤ 15 pF])							
xSPI200: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single and dual slave [load ≤ 15 pF])							
SID1500_2	t _{CK}	Interface clock period (JEDEC)	7.5	–	10	–	ns
SID1500_2CM	t _{CK}	Interface clock period (CMOS)	7.5	–	10	–	ns

(表格续下页.....)

26 电气规格
表 64 (续) xSPI 规格

Spec ID	Parameter	Description	Min	Max	Min	Max	Units
SID1501_2	tCKDCD	Allowable clock distortion ¹⁾	–	0.05 × tCK	–	0.05 × tCK	ns
SID1502_2	tCKMPW	Minimum clock pulse width (JEDEC)	3.375	–	4.5	–	ns
SID1502_2CM	tCKMPW	Minimum clock pulse width (CMOS)	3.375	–	4.5	–	ns
SID1503_2HV	OUT_SR	Output slew rate with respect to V _{OH} /V _{OL}	1.37	–	1.03	–	V/ns
SID1504_2	tosu	Output setup time of DS and I/O[7:0] to CK	0.9	–	1.1	–	ns
SID1505_2	toH	Output hold time of DS and I/O[7:0] to CK	0.9	–	1.1	–	ns
SID1506_2HV	IN_SR	Input slew rate with respect to V _{IH} /V _{IL}	1.37	–	1.03	–	V/ns
SID1507_2	tDSMPW	Input min pulse width of DS (JEDEC)	3.075	–	4.1	–	ns
SID1507_2CM	tDSMPW	Input min pulse width of DS (CMOS)	3.075	–	4.1	–	ns
SID1508_2	trQ	Input DS to I/O[7:0] valid time (JEDEC)	–	0.675	–	0.9	ns
SID1508_2CM	trQ	Input DS to I/O[7:0] valid time (CMOS)	–	0.675	–	0.9	ns
SID1509_2	trQH	Input I/O[7:0] invalid to DS time (JEDEC)	–	0.675	–	0.9	ns
SID1509_2CM	trQH	Input I/O[7:0] invalid to DS time (CMOS)	–	0.675	–	0.9	ns
SID1511_2	tCKLCSL	CK LOW to CS LOW	6	–	8	–	ns
SID1512_2	tCSLCKH	CS LOW to CK HIGH	6	–	8	–	ns
SID1513_2	tCKLCSH	CK LOW to CS HIGH	6	–	8	–	ns
SID1514_2	tCSHCKH	CS HIGH to CK HIGH	6	–	8	–	ns
SID1515_2	tDSLCSH	DS LOW to CS HIGH	6	–	8	–	ns
SID1516_2	tCSHDST	CS HIGH to DS High-Z	–	7.5	–	10	ns
SID1517_2	tCSLDSL	CS LOW to DS LOW	0	–	0	–	ns
SID1518_2	tDSTCSL	DS High-Z to CS LOW	0	–	0	–	ns

1) PLL#400, SSCG = 0, 小数分频器关闭

表 65 xSPI (JEDEC JESD251) 延迟抽头推荐配置

Feature	xSPI266	xSPI200
	Rx	Rx
Delay Tap Selection (SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0>) for SMIF0	1	6
Delay Line Selection (SMIF_CTL/DELAY_LINE_SEL<2:0>) for SMIF0	0	0
Delay Tap Selection (SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0>) for SMIF1	1	6
Delay Line Selection (SMIF_CTL/DELAY_LINE_SEL<2:0>) for SMIF1	0	0

26 电气规格

表 66 支持的输入、输出基准电压参考电平

Signal	Supported modes for voltage reference levels	
	CMOS	JEDEC
Clock	$V_T = (50\% \times V_{DDIO_HSIO})$	
RWDS (output)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO_HSIO}$
DQ[7:0] (output)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO_HSIO}$
RWDS (input)	$V_T = (50\% \times V_{DDIO_HSIO})$	
DQ[7:0] (input)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{IH}/V_{IL} = 70\% / 30\% \times V_{DDIO_HSIO}$

- 注： 根据实际存储器的要求， 需要选择其中一种模式（"CMOS"、"JEDEC"）。
- 某些参数可能是可用的， 并单独列出了各个模式的参数。 参数描述中会提到相应的模式。
 - 没有明确模式描述的参数（例如 t_{OSU} ）适用于所有模式， 但基准电压参考电平按照表格仍然适用。

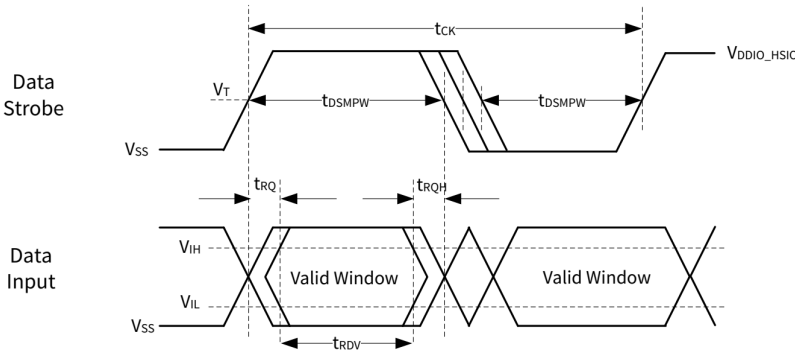


图 38 xSPI 主机数据输入时序基准电平（JEDEC）

26 电气规格

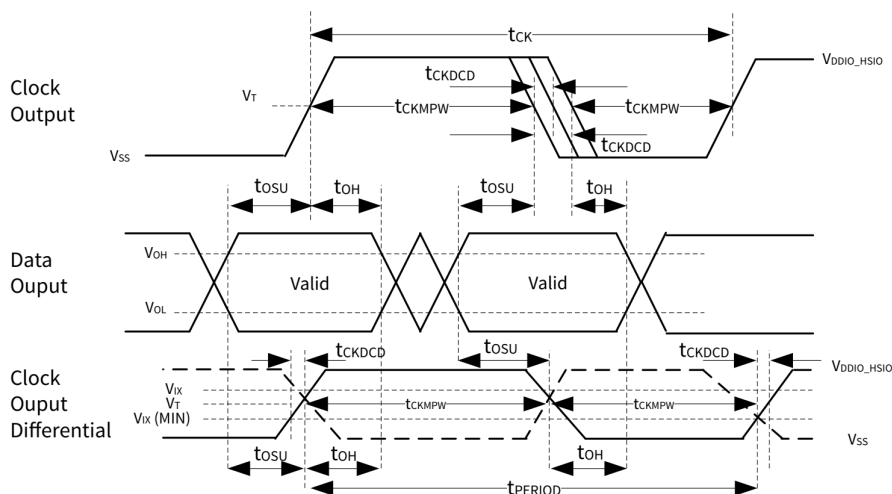


图 39 xSPI 主机数据输出时序基准电平 (JEDEC)

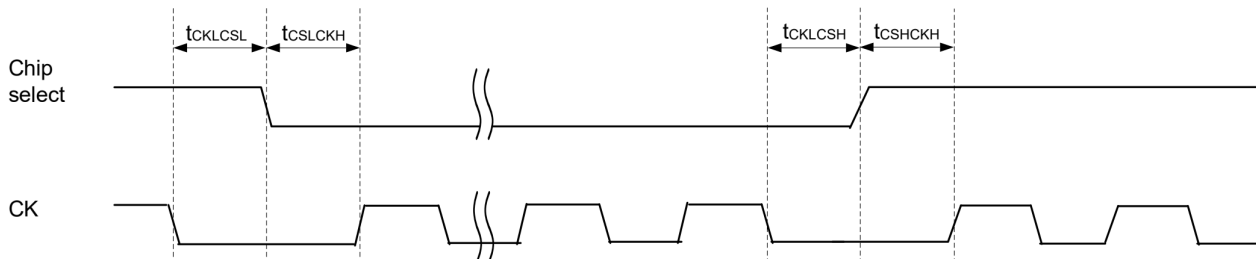


图 40 xSPI 时钟到片选时序图

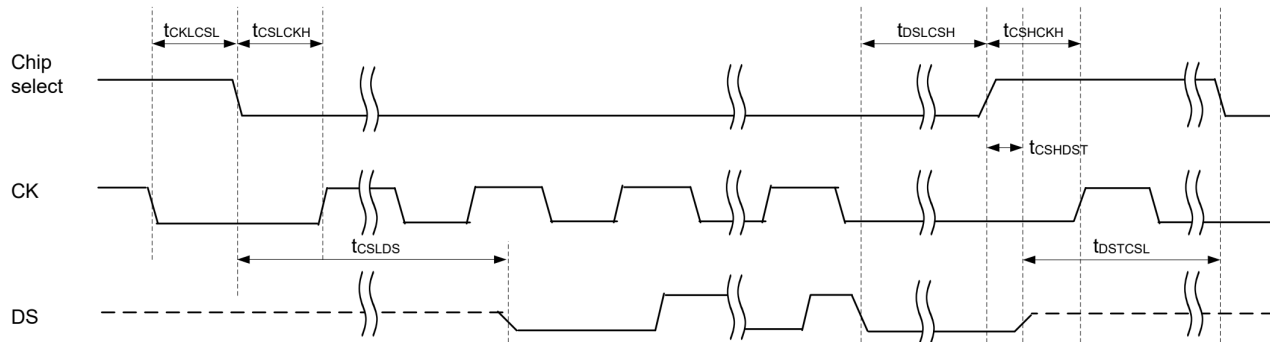


图 41 xSPI 数据选通到片选时序图

26 电气规格
表 67 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Standard SPI SDR							
建议 I/O 配置							
HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b0, CFG_SLEW_EXT/SLEW<0:0>= 0b0							
接收器的 DLL Tap 设置:							
SMIF_CTL/DELAY_LINE_SEL<2:0>= 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0>= 2							
所有时序均与 $V_T = (50\% \times V_{DDIO_HSIO})$ 对齐。							
SID1600_21)	t _{CK}	Interface clock period	10	–	–	ns	15-pF output loads
SID1601	t _{CKPW}	Clock pulse width	$0.45 \times t_{CK}$	–	$0.55 \times t_{CK}$	ns	15-pF output loads
SID1602_HS	t _{css}	CS# active setup to CK ($f_{CK} > 50$ MHz)	4	–	–	ns	15-pF output loads, $f_{CK} > 50$ MHz Guaranteed by design
SID1602_LS	t _{css}	CS# active setup to CK ($f_{CK} \leq 50$ MHz)	5	–	–	ns	15-pF output loads, $f_{CK} \leq 50$ MHz Guaranteed by design
SID1603	t _{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1604	t _{CSH3}	CS# active hold to CK (mode 3)	6	–	–	ns	15-pF output loads Guaranteed by design
SID1605_2	t _{osu}	Output setup time of DQ[7:0] to CK high ($f_{CK} = 100$ MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{osu} = t_{osu_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t_{osu_min} = value at MIN of SID1605_2 t_{CK_min} = value at MIN of SID1600_2 t_{CK} = actual clock period

(表格续下页.....)

26 电气规格
表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1606_2	t _{OH}	Output hold time of DQ[7:0] to CK high (f _{CK} = 100 MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t _{OH_min} = value at MIN of SID1606_2 t _{CK_min} = value at MIN of SID1600_2 t _{CK} = actual clock period
SID1607	t _{IN_V}	CK edge low to DQ[7:0] input valid time	1	–	6.7	ns	CTL/ DELAY_TAP_ENABL E=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLE<0:0> = 0b0 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0> = 0b0 1 3) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLE<0:0> = 0b1 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING

(表格续下页.....)

26 电气规格

表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1607A	t _{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/ DELAY_TAP_ENABL E=0 (Delay line is disabled/bypassed) CTL/ CLOCK_IF_RX_SEL< 2:0> = 0b011
SID1608	t _{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/ DELAY_TAP_ENABL E=0 (Delay line is disabled/bypassed) CTL/ CLOCK_IF_RX_SEL< 2:0> = 0b011

(表格续下页.....)

26 电气规格
表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1609	trDV	Input data valid time of DQ[7:0]	3.8	–	–	ns	CTL/ DELAY_TAP_ENABL E=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> =0b0 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0>=0b0 1 3) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> =0b1 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING
SID1610	tcs	CS# HIGH time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1610A	tcs	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1610B	tcs	CS# High time (Program / Erase)	50	–	–	ns	15-pF output loads Guaranteed by design

(表格续下页.....)

26 电气规格
表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1611	t _{DIS}	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1613	IN_SR	Input slew rate with respect to VIH/VIL	0.7	–	–	V/ns	–

Standard SPI DDR
建议 I/O 配置:

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> = 0b000

接收器的 DLL Tap 设置:

SMIF_CTL/DELAY_LINE_SEL<2:0> = 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0> = 2

所有时序均与 $V_T = (50\% \times V_{DDIO_HSIO})$ 对齐。

SID1700_2 ¹⁾	t _{CK}	Interface clock period	12.5	–	–	ns	15-pF output loads
SID1701	t _{CKPW}	Clock pulse width	$0.45 \times t_{CK}$	–	$0.55 \times t_{CK}$	ns	15-pF output loads
SID1702_HS	t _{CSS}	CS# active setup to CK ($f_{CK} > 50$ MHz)	4	–	–	ns	15-pF output loads, $f_{CK} > 50$ MHz Guaranteed by design
SID1702_LS	t _{CSS}	CS# active setup to CK ($f_{CK} \leq 50$ MHz)	5	–	–	ns	15-pF output loads, $f_{CK} \leq 50$ MHz Guaranteed by design
SID1703	t _{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1705_2	t _{OSU}	Output setup time of DQ[7:0] to CK edge ($f_{CK} = 80$ MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OSU} = t_{OSU_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t_{OSU_min} = value at MIN of SID1705_2 t_{CK_min} = value at MIN of SID1700_2 t_{CK} = actual clock period

(表格续下页.....)

26 电气规格
表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1706_2	t _{OH}	Output hold time of DQ[7:0] to CK edge (f _{CK} = 80 MHz)	1.6	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t _{OH_min} = value at MIN of SID1706_2 t _{CK_min} = value at MIN of SID1700_2 t _{CK} = actual clock period
SID1707	t _{IN_V}	CK edge low to DQ[7:0] input valid time	1	–	6.7	ns	CTL/ DELAY_TAP_ENABL E=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> = 0b0 CTL/ INT_CLOCK_CAPTURE_CYCLE<1:0> = 0b01 3) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> = 0b1 CTL/ INT_CLOCK_CAPTURE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING

(表格续下页.....)

26 电气规格

表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1707A	t _{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/ DELAY_TAP_ENABL E=0 (Delay line is disabled/bypassed) CTL/ CLOCK_IF_RX_SEL< 2:0> = 0b011
SID1708	t _{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/ DELAY_TAP_ENABL E=0 (Delay line is disabled/bypassed) CTL/ CLOCK_IF_RX_SEL< 2:0> = 0b011

(表格续下页.....)

26 电气规格
表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1709_2	trDV	Input data valid time of DQ[7:0] ($f_{CK} \leq 80$ MHz)	3.5	–	–	ns	CTL/ DELAY_TAP_ENABL E=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> = 0b0 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0> = 0b0 1 3) CTL/ CLOCK_IF_RX_SEL < 2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_EN ABLED<0:0> = 0b1 CTL/ INT_CLOCK_CAPTU RE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING
SID1710	tcs	CS# High time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1710A	tcs	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1710B	tcs	CS# High time (Program / Erase)	50	–	–	ns	15-pF output loads Guaranteed by design

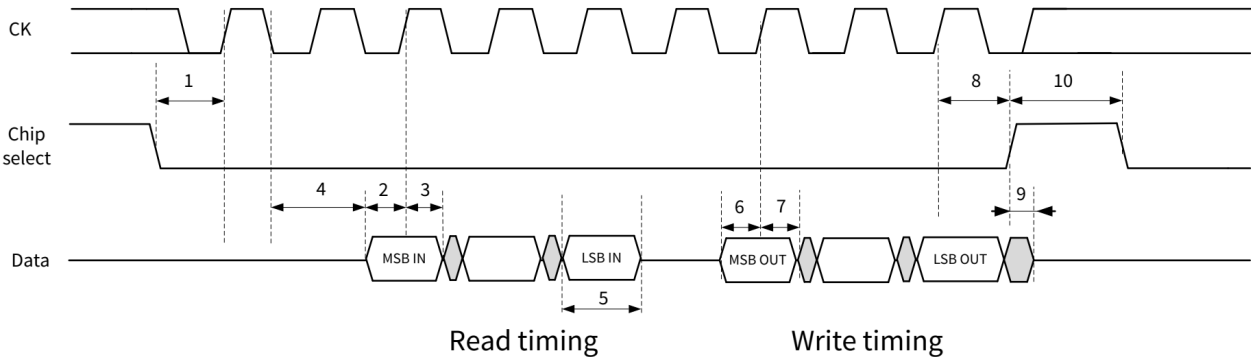
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26 电气规格

表 67 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1711	t _{DIS}	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1713	IN_SR	Input slew rate with respect to VIH/VIL	0.7	–	–	V/ns	–

1) 确保将 PLL#400 明确配置为整数模式，设置 "SSCG = OFF"，"Fractional = OFF"。



- 1: CS# active setup time to CK = t_{CSS}
- 2: Input data setup time = t_{ISU}
- 3: Input data hold time = t_{IH}
- 4: CK edge low to DQ[7:0] input valid time = t_{IN_V}
- 5: Read data valid time of DQ[7:0] = t_{RDV}
- 6: Output setup time of DQ[7:0] to CK rise = t_{OSU}
- 7: Output hold time of DQ[7:0] from CK rise = t_{OH}
- 8: CS# active hold time to CK = t_{CSH}
- 9: CS# inactive to output disable time = t_{DIS}
- 10: CS# HIGH time = t_{CS}

图 42 SDR 写入和读取时序图

26 电气规格

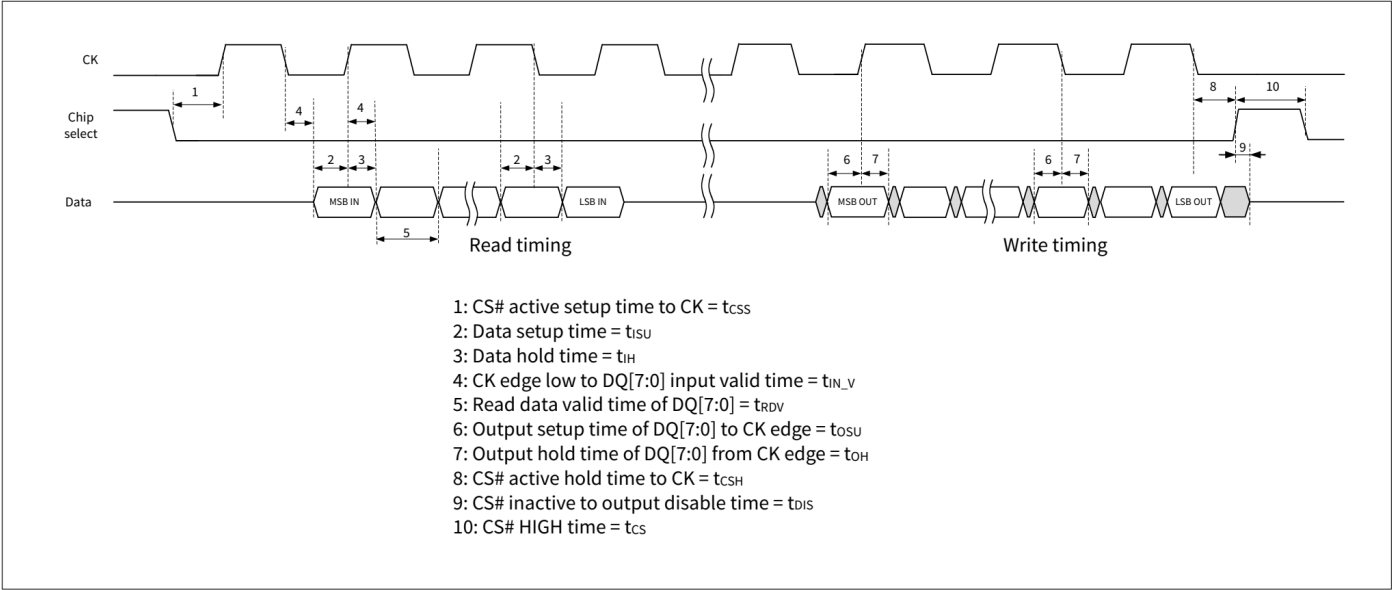


图 43 DDR 写入和读取时序图

26.15 图形子系统规格

表 68 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Display Output - TTL Mode							
建议 I/O 配置：							
HSIO_STDLN (BGA package): CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
HSIO_STDLN (TEQFP package): CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
注：数值适用于整数、SSCG 和小数工作模式下的 FLL、PLL200 和 PLL400。							
SID866	t_{DC1CYC}	Clock cycle	25	–	–	ns	TTL_DSP1_CLOCK, $C_L = 15 \text{ pF}$
SID873	$t_{DC1CKPW}$	Clock pulse width	$0.40 \times t_{DC1CYC}$	–	$0.60 \times t_{DC1CYC}$	ns	TTL_DSP1_CLOCK pulse width $C_L = 15 \text{ pF}$
SID868	t_{DC1S}	Data/control output to TTL_DSP1_CLOCK time	4	–	–	ns	TTL_DSP1_DATA_A0[11:0] TTL_DSP1_DATA_A1[11:0] TTL_DSP1_CONTROL[11:0] (TCON for FPDLink) $C_L = 15 \text{ pF}$

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID869	tDC1H	TTL_DSP1_CLOCK to Data/ Control valid time	5	–	–	ns	TTL_DSP1_DATA_A0[1 1-0] TTL_DSP1_DATA_A1[1 1-0] TTL_DSP1_CONTROL[11-0] (TCON for FPDLink) C _L = 15 pF
SID890	tDSP0_CONTRO L_SKEW	TTL_DSP0_CONTROL skew	–	–	4	ns	Skew between signals TTL_DSP0_CONTROL[11-0] C _L = 15 pF

Display Capture
建议 I/O 配置

CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b0

SID875	tCAP0CYC	Display capture Clock Cycle	12.5	–	–	ns	TTL_CAP0_CLK (HSIO)
SID876	tCAP0SU	Display capture data setup time	1.9	–	–	ns	TTL_CAP0_DATA[35-0] (HSIO)
SID877	tCAP0HD	Display capture data hold time	2.7	–	–	ns	TTL_CAP0_DATA[35-0] (HSIO)

FPD Link

FPD-Link 应在整数模式下与 PLL200 或 PLL400 配合使用。

所有数值均为 PLL200 或 PLL400 在 SSCG = OFF、Fractional divider = OFF 条件下的值。

SID880	IVDDA	Total analog supply current in TX mode	–	–	30	mA	
SID881	IVDDPLL	Total PLL supply current in TX mode	–	–	4	mA	
SID881B	IVDDHA	Total I/O (LVDS driver) supply current in TX mode	–	–	91	mA	
SID884	IVDDA_PD	Total analog supply current in Power-Down mode	–	4	300	μA	Typ: T _A = 25°C, V _{DDA_FPD} = 1.15 V, process typ (TT) Max: T _A = 105°C, V _{DDA_FPD} = 1.21 V, process worst (FF) For S-grade devices

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID884_125	IVDDA_PD	Total analog supply current in Power-Down mode	–	4	300	μA	Typ: T _A = 25°C, V _{DDA_FPD} = 1.15 V, process typ (TT) Max: T _A = 125°C, V _{DDA_FPD} = 1.21 V, process worst (FF) For E-grade devices
SID884_1	IVDDA_PD_1	Total analog supply current in Power-Down mode (room temp)	–	–	5	μA	Max: T _A = 25°C, V _{DDA_FPD} = 1.15 V (max VREG), process worst (FF)
SID884_2	IVDDA_PD_2	Total analog supply current in Power-Down mode	–	–	40	μA	Max: T _A = 85°C, V _{DDA_FPD} = 1.15 V (max VREG), process worst (FF)
SID885	IVDDPLL_PD	Total PLL supply current in Power-Down mode	–	3	200	μA	Typ: T _A = 25°C, V _{DDPLL_FPD} = 1.15 V, process typ (TT) Max: T _A = 105°C, V _{DDPLL_FPD} = 1.21 V, process worst (FF); For S-grade devices
SID885_125	IVDDPLL_PD	Total PLL supply current in Power-Down mode	–	3	200	μA	Typ: T _A = 25°C, V _{DDPLL_FPD} = 1.15 V, process typ (TT) Max: T _A = 125°C, V _{DDPLL_FPD} = 1.21 V, process worst (FF); For E-grade devices
SID885_1	IVDDPLL_PD_1	Total PLL supply current in Power-Down mode (room temp)	–	–	4	μA	Max: T _A = 25°C, V _{DDPLL_FPD} = 1.15 V (max VREG), process worst (FF)
SID885_2	IVDDPLL_PD_2	Total PLL supply current in Power-Down mode	–	–	25	μA	Max: T _A = 85°C, V _{DDPLL_FPD} = 1.15 V (max VREG), process worst (FF)

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID885B	IVDDHA_PD	Total I/O (LVDS driver) supply current in Power-Down mode	–	0.5	50	μA	Typ: T _A = 25°C, VDDHA_FPD = 3.3 V, process typ (TT) Max: T _A = 105°C, VDDHA_FPD = 3.6 V, process worst (FF); For S-grade devices
SID885B_125	IVDDHA_PD	Total I/O (LVDS driver) supply current in Power-Down mode	–	0.5	50	μA	Typ: T _A = 25°C, VDDHA_FPD = 3.3 V, process typ (TT) Max: T _A = 125°C, VDDHA_FPD = 3.6 V, process worst (FF); For E-grade devices
SID885B_1	IVDDHA_PD_1	Total I/O (LVDS driver) supply current in Power-Down mode (room temp)	–	–	1	μA	Max: T _A = 25°C, VDDHA_FPD = 3.6 V (max VREG), process worst (FF)
SID885B_2	IVDDHA_PD_2	Total I/O (LVDS driver) supply current in Power-Down mode	–	–	12	μA	Max: T _A = 85°C, VDDHA_FPD = 3.6 V (max VREG), process worst (FF)
SID895	VOD	Steady-state magnitude of the differential output voltage	247	350	454	mV	
SID896	VΔVOD_M	Variation of signal swing voltage between drivers	–	–	25	mV	
SID897	VCM	Output Common-mode voltage	1.125	1.25	1.375	V	
SID898	VΔVCM_M	Delta in Common-mode voltage between drivers	–	–	25	mV	
SID899A	I _{SA}	Magnitude of current flowing through output terminal P when the output terminals are short-circuited to ground.	–	–	24	mA	See Figure 6 of “TIA/EIA-644-A” specifications.
SID899B	I _{SB}	Magnitude of current flowing through output terminal M when the output terminals are short-circuited to ground.	–	–	24	mA	See Figure 6 of “TIA/EIA-644-A” specifications.

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID899C	I _{OS}	Magnitude of current flowing through the output terminals when they are short-circuited to each other.	–	–	12	mA	See Figure 7 of “TIA/EIA-644-A” specifications.
SID900	t _{WAKE}	Wakeup time	–	–	1.2	ms	
SID901	t _{PDD}	Power down delay time	–	–	100	μs	Guaranteed by design
SID902	f _{PX}	Configured pixel clock frequency	7	–	110	MHz	BGA package Guaranteed by design
SID902_3	f _{PX}	Configured pixel clock frequency	7	–	80	MHz	TEQFP package Characterization only
SID903	f _{PX110}	Output clock frequency (110 MHz)	103.7	110	116.3	MHz	BGA only; When transmitting an alternating 0/1 bit pattern
SID904	f _{PX55}	Output clock frequency (55 MHz)	52.35	55	57.65	MHz	When transmitting an alternating 0/1 bit pattern
SID905	f _{PX28}	Output clock frequency (28 MHz)	26.66	28	29.34	MHz	When transmitting an alternating 0/1 bit pattern
SID906	f _{PX14}	Output clock frequency (14 MHz)	13.28	14	14.72	MHz	When transmitting an alternating 0/1 bit pattern
SID907	f _{PX7}	Output clock frequency (7 MHz)	6.59	7	7.41	MHz	When transmitting an alternating 0/1 bit pattern
SID908	GAIN_JIT_LVDS	Gain region max long-term total jitter	–	–	0.32	UI2 p-p	
SID909	ATTEN_JIT_LVDS	Attenuation region long-term total jitter	–	–	0.34	UI2 p-p	
SID910	C2C_JIT	Cycle-to-cycle jitter	–	–	0.11	UI	
SID911	t _{CSK}	Channel-to-channel skew of driver outputs	–	–	100	ps	BGA package
SID911_2	t _{CSK}	Channel-to-channel skew of driver outputs	–	–	200	ps	TEQFP package
SID913	TPPos0	Transmit Pulse Position Offset 0	–0.168	0	0.168	ns	

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID914	TPPos1	Transmit Pulse Position Offset 1	$T/7 - \text{TPPos}_0$	$T/7$	$T/7 + \text{TPPos}_0$	ns	
SID915	TPPos2	Transmit Pulse Position Offset 2	$2T/7 - \text{TPPos}_0$	$2T/7$	$T/7 + \text{TPPos}_0$	ns	
SID916	TPPos3	Transmit Pulse Position Offset 3	$3T/7 - \text{TPPos}_0$	$3T/7$	$3T/7 + \text{TPPos}_0$	ns	
SID917	TPPos4	Transmit Pulse Position Offset 4	$4T/7 - \text{TPPos}_0$	$4T/7$	$4T/7 + \text{TPPos}_0$	ns	
SID918	TPPos5	Transmit Pulse Position Offset 5	$5T/7 - \text{TPPos}_0$	$5T/7$	$5T/7 + \text{TPPos}_0$	ns	
SID919	TPPos6	Transmit Pulse Position Offset 6	$6T/7 - \text{TPPos}_0$	$6T/7$	$6T/7 + \text{TPPos}_0$	ns	
SID920	t _{LLHT}	Differential driver rise time	–	–	390	ps	BGA package
SID920_2	t _{LLHT}	Differential driver rise time	–	–	500	ps	TEQFP package
SID921	t _{LHLT}	Differential driver fall time	–	–	390	ps	BGA package
SID921_2	t _{LHLT}	Differential driver fall time	–	–	500	ps	TEQFP package
SID922	t _{RF_MATCH}	Lane-to-lane rise/fall delta	–	–	40	ps	
SID923	f _{PLL}	Input clock frequency of FPD-Link PLL	110	–	220	MHz	–

MIPI/DPHY

SID1447	f _{PX_QFP}	Pixel clock frequency	–	–	80	MHz	TEQFP package
SID1448	f _{PX_BGA}	Pixel clock frequency	–	–	110	MHz	BGA package
SID1417	V _{CMRX}	Common-mode voltage HS receive mode	70	–	330	mV	
SID1418	V _{IDTH}	Differential input HIGH threshold	70	–	–	mV	
SID1419	V _{IDTL}	Differential Input LOW threshold	–	–	–70	mV	
SID1420	V _{IHHS}	Single-ended input HIGH voltage	–	–	460	mV	

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1421	VILHS	Single-ended Input LOW voltage	-40	-	-	mV	
SID1422	ZID	Differential Input Impedance	80	-	125	Ω	
SID1423	VIH_LS	Logic 1 input voltage LS	-	-	880	mV	
SID1424	VIL_LS	Logic 0 Input voltage LS	550	-	-	mV	
SID1425	VHYST	Input hysteresis	25	-	-	mV	
SID1426	I _{LEAK}	Pin leakage current DPx, DNx, CLKP/N in LP mode	-100	-	100	μA	T _A = 85°C
SID1427	I _{VDDA_LP}	Current in LP	-	-	3	mA	
SID1428	I _{VDDA_PD}	Current when D-PHY powered down	-	8	800	μA	Typ: T _A = 25°C, V _{DDA_MIP1} = 1.15 V, process typ (TT) Max: T _A = 105 °C, V _{DDA_MIP1} = 1.21 V, process worst (FF)
SID1428_1	I _{VDDA_PD_1}	Current when D-PHY powered down (room temp)	-	-	20	μA	Max: T _A = 25°C, V _{DDA_MIP1} = 1.15 V (max VREG), process worst (FF)
SID1428_2	I _{VDDA_PD_2}	Current when D-PHY powered down	-	-	150	μA	Max: T _A = 85°C, V _{DDA_MIP1} = 1.15 V (max VREG), process worst (FF)
SID1429	I _{VDDA_ULP}	Current in ULP	-	-	2	mA	
SID1430	I _{VDDA_HS}	current in HS	-	-	35	mA	
SID1431	t _{CLK_TERM_EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	38	ns	
SID1432	t _{D_TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses, VIL,MAX	-	-	38	ns	

(表格续下页.....)

26 电气规格
表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1433	tCLK_SETTLE	Time interval during which HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	–	300	ns	
SID1434	tHS_SETTLE	Time interval during which the HS receiver shall ignore any DATA Lane HS transitions, starting from the beginning of THSPREPARE. The HS receiver shall ignore any Data Lane transitions before minimum value, and the HS receiver shall respond to any Data Lane transitions after maximum value	85 + 6 × UI	–	145 + 10 × UI	ns	
SID1435	tHS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	–	55 + 4 × UI	ns	
SID1436	VΔVCMRX_HF	Common-mode interference	–	–	100	mV	Beyond 450 MHz
SID1437	VΔVCMRX_LF	Common-mode interference	–	–	50	mV	50 to 450 MHz
SID1438	CCM	Common-mode termination	–	–	60	pF	
SID1439	tE_SPIKE	Input pulse rejection	–	–	300	ps	
SID1440	tMIN_RX	Minimum pulse width response	–	–	20	ns	
SID1441	tSETUP_QFP	Data to clock setup time	0.15	–	–	UI	Valid for TEQFP package
SID1442	tHOLD_QFP	Clock to data hold time	0.15	–	–	UI	Valid for TEQFP package
SID1443	tSETUP_BGA	Data to clock setup time	0.2	–	–	UI	Valid for BGA package
SID1444	tHOLD_BGA	Clock to data hold time	0.2	–	–	UI	Valid for BGA package

(表格续下页.....)

26 电气规格

表 68 (续) 图形规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1445	I _{VDDA_1P4GBPS_HS}	Current in high speed max frequency	–	–	35	mA	
SID1446	I _{VDDA_10M_LP}	Current in LP mode max frequency	–	–	2	mA	

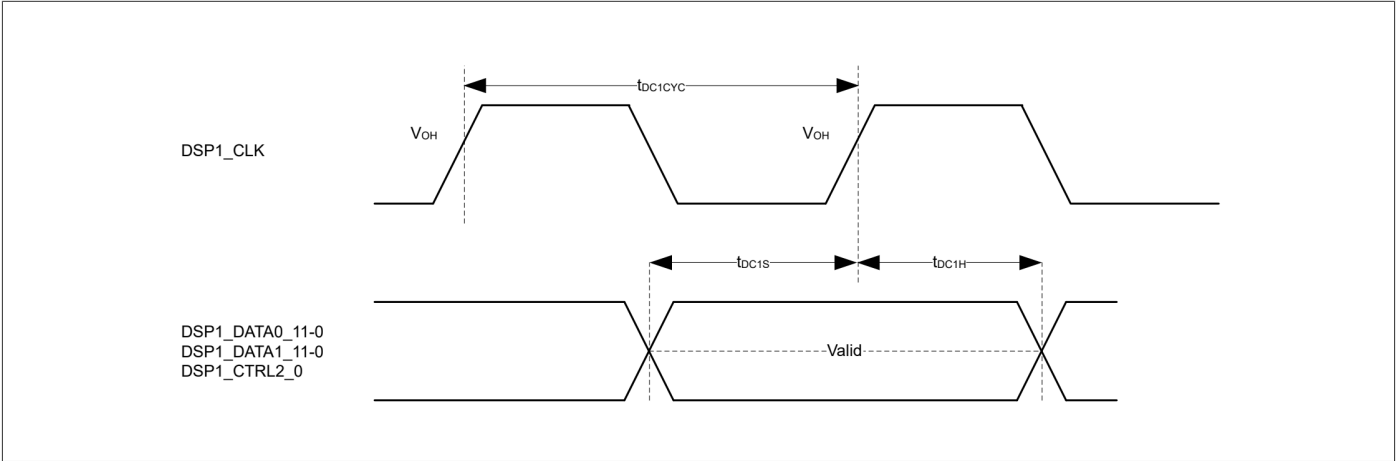


图 44 TTL 显示输出时序

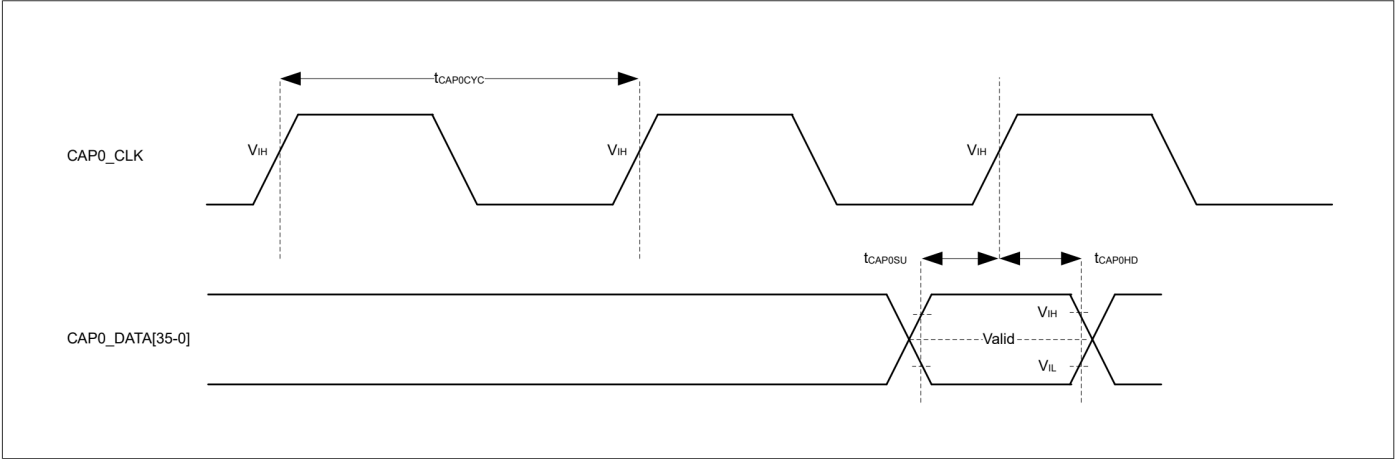


图 45 视频捕获时序

26 电气规格

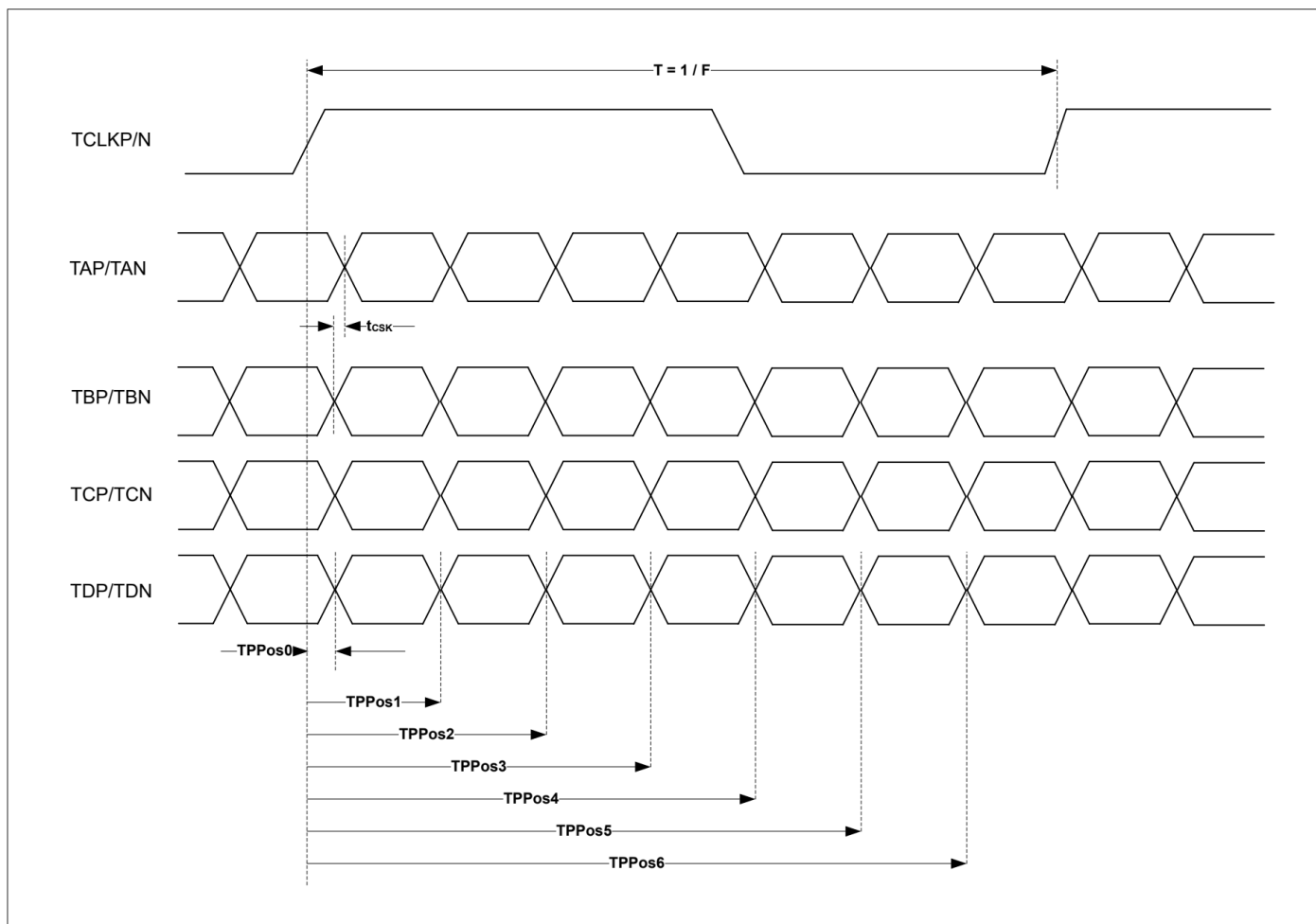


图 46 FPD-link 输出脉冲位置误差和通道间偏差

26 电气规格

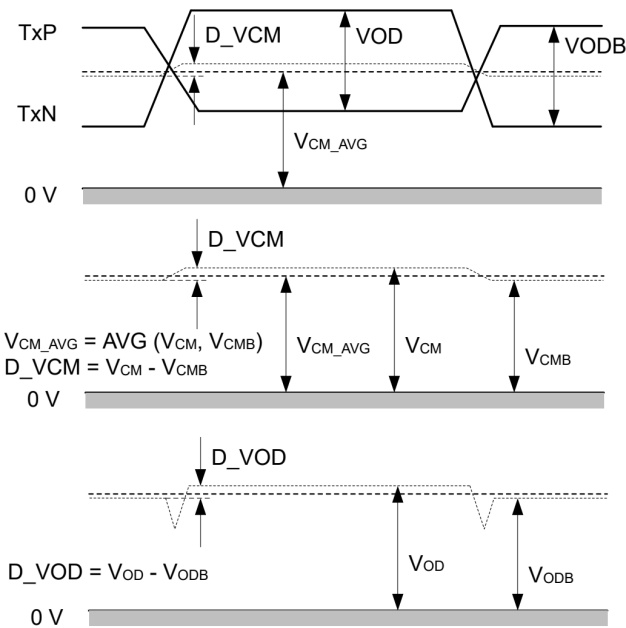


图 47 TxP 和 TxN 之间的偏差以及稳态差分振幅和共模电压

26.15.1 VIDEOSS 捕获时序组

表 69 列出了捕获信号和时钟。所有时钟和捕获信号之间均保证交流时序。所有时钟和信号都在同一组中。

表 69 捕获时序组

Pin	ACT#6	ACT#11	Group (ACT#6/ ACT#11)
P13.2	TTL_CAP0_DATA[23]		Group 0
P13.3	TTL_CAP0_DATA[22]	TTL_CAP0_DATA[26]	
P13.4	TTL_CAP0_DATA[21]	TTL_CAP0_DATA[25]	
P13.5	TTL_CAP0_DATA[20]	TTL_CAP0_DATA[24]	
P13.6	TTL_CAP0_DATA[19]	TTL_CAP0_DATA[0]	
P13.7	TTL_CAP0_DATA[18]	TTL_CAP0_DATA[1]	
P14.0	TTL_CAP0_DATA[17]	TTL_CAP0_DATA[2]	
P14.1	TTL_CAP0_DATA[16]	TTL_CAP0_DATA[3]	
P14.2	TTL_CAP0_DATA[15]	TTL_CAP0_DATA[4]	
P14.3	TTL_CAP0_DATA[14]	TTL_CAP0_DATA[5]	
P14.4	TTL_CAP0_DATA[13]	TTL_CAP0_DATA[6]	
P14.5	TTL_CAP0_DATA[12]	TTL_CAP0_DATA[7]	

(表格续下页.....)

26 电气规格

表 69 (续) 捕获时序组

Pin	ACT#6	ACT#11	Group (ACT#6/ ACT#11)
P14.6	TTL_CAP0_DATA[11]	TTL_CAP0_DATA[8]	
P14.7	TTL_CAP0_DATA[10]	TTL_CAP0_DATA[9]	
P15.0	TTL_CAP0_CLK		
P15.1	TTL_CAP0_DATA[10]	TTL_CAP0_DATA[9]	
P15.2	TTL_CAP0_DATA[11]	TTL_CAP0_DATA[8]	
P15.3	TTL_CAP0_DATA[12]	TTL_CAP0_DATA[7]	
P15.4	TTL_CAP0_DATA[13]	TTL_CAP0_DATA[6]	
P15.5	TTL_CAP0_DATA[14]	TTL_CAP0_DATA[5]	
P15.6	TTL_CAP0_DATA[15]	TTL_CAP0_DATA[4]	
P15.7	TTL_CAP0_DATA[16]	TTL_CAP0_DATA[3]	
P16.0	TTL_CAP0_DATA[17]	TTL_CAP0_DATA[2]	
P16.1	TTL_CAP0_DATA[18]	TTL_CAP0_DATA[1]	
P16.2	TTL_CAP0_DATA[19]	TTL_CAP0_DATA[0]	
P16.3	TTL_CAP0_DATA[20]	TTL_CAP0_DATA[24]	
P16.4	TTL_CAP0_DATA[21]	TTL_CAP0_DATA[25]	
P16.5	TTL_CAP0_DATA[22]	TTL_CAP0_DATA[26]	
P16.6	TTL_CAP0_DATA[23]		

表 70 捕获时序组时钟

Group	Clock	EROS Parameter
Group 0	P15.0	SID875

27 订购信息

27 订购信息

CYT3DL 微控制器部件编号和特性列于表 71 中。

27 订购信息

表 71 CYT3DL 订购信息 ¹⁾

Base device code	Product	Package	CM7 Cores	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC channels	SCB	CAN FD	LIN	CXPI	Ethernet channels	SMIF	Audio DAC	MIP1	Free graphics software ²⁾	Qt bundle ³⁾	Autosar package	Temperature grade ⁴⁾	JTAG ID code
CYT3DLBB AS	CYT3DLBBABQ1B ZSGS	272- BGA	1	4160 ⁵⁾)	128 ⁶⁾	384	48	12 4	4	2 2	2 2	1 1	2 2	0 0	0	No	No	No	S	0x1E84106 97)
CYT3DLBB AE	CYT3DLBBABQ1B ZEGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	0 0	0	No	No	No	E	0x1E84106 9
CYT3DLBB BS	CYT3DLBBBQB1 BZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	0 0	0	No	No	No	S	0x1E84206 9
CYT3DLBB CS	CYT3DLBBBQB1 BZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	0 0	1	No	No	No	S	0x1E84306 9
CYT3DLBB DS	CYT3DLBBBQB1 BZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	0 0	1	No	No	No	S	0x1E84406 9
CYT3DLBBE S	CYT3DLBBBQB1 ZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	1 1	0	No	No	No	S	0x1E84506 9
CYT3DLBBFS	CYT3DLBBFBQB1 ZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	1 1	0	No	No	No	S	0x1E84606 9
CYT3DLBB GS	CYT3DLBBGBQB1 BZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	1 1	1	No	No	No	S	0x1E84706 9
CYT3DLBBH S ⁸⁾	CYT3DLBBHBQB1 BZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	1 1	1	No	No	No	S	0x1E84806 9
CYT3DLBB SS	CYT3DLBBBQB1 ZSGS	272- BGA	1	4160	128	384	48	12 4	4	2 2	2 2	1 1	2 2	1 1	1	Yes	Yes	No	S	0x1E87006 9

(表格续下页.....)

27 订购信息

表 71 (续) CYT3DL 订购信息¹⁾

Base device code	Product	Package	CM7 Cores	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC channels	SCB	CAN FD	LIN	CXPI	Ethernet channels	SMIF	Audio DAC	MIP1	Free graphics software ²⁾	Qt bundle ³⁾	Autosar package	Temperature grade ⁴⁾	JTAG ID code
CYT3DLBB Z S	CYT3DLBBZBQ1B ZSGS	272- BGA	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	No	No	S	0x1E87E06 9
CYT3DLBBV S	CYT3DLBBVBQ1B ZSGS	272- BGA	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	Yes	Yes	S	0x1E87206 9
CYT3DLBBY S	CYT3DLBBYBQ1B ZSGS	272- BGA	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	No	Yes	S	0x1E87306 9
CYT3DLABA S	CYT3DLABABQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	0	0	No	No	No	S	0x1E84906 9
CYT3DLABA E	CYT3DLABABQ1A EEGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	0	0	No	No	No	E	0x1E84906 9
CYT3DLAB B S	CYT3DLABBBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	0	0	No	No	No	S	0x1E84A06 9
CYT3DLABC S	CYT3DLABCBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	0	1	No	No	No	S	0x1E84B06 9
CYT3DLABD S	CYT3DLABDBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	0	1	No	No	No	S	0x1E84C06 9
CYT3DLABE S	CYT3DLABEBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	0	No	No	No	S	0x1E84D06 9
CYT3DLABF S	CYT3DLABFBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	0	No	No	No	S	0x1E84E06 9

(表格续下页.....)

27 订购信息

表 71 (续) CYT3DL 订购信息¹⁾

Base device code	Product	Package	CM7 Cores	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC channels	SCB	CAN FD	LIN	CXPI	Ethernet channels	SMIF	Audio DAC	MIP1	Free graphics software ²⁾	Qt bundle ³⁾	Autosar package	Temperature grade ⁴⁾	JTAG ID code
CYT3DLABG S	CYT3DLABGBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	No	No	No	S	0x1E84F06 9
CYT3DLABH S ⁸⁾	CYT3DLABHBQ1 AESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	No	No	No	S	0x1E85006 9
CYT3DLABS S	CYT3DLABSBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	Yes	No	S	0x1E87106 9
CYT3DLABV S	CYT3DLABVBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	Yes	Yes	S	0x1E87406 9
CYT3DLABY S	CYT3DLABYBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	No	Yes	S	0x1E87506 9
CYT3DLABZ S	CYT3DLABZBQ1A ESGS	216- TEQFP	1	4160	128	384	48	12	4	2	2	1	2	1	1	Yes	No	No	S	0x1E87F06 9

1) 支持的装运类型为“托盘”（默认）和“卷带包装”。在末尾添加字符‘T’，获取“卷带包装”装运类型的订购代码。

2) 图形软件

3) 发行许可模式由 Qt Company Oy 提供。关于 Qt Group。

4) S 级温度 (-40°C 至 105°C) 和 E 级温度 (-40°C 至 125°C)。

5) 代码闪存大小 4160 KB = 32 KB × 126 (大扇区) + 8 KB × 16 (小扇区)。

6) 工作闪存大小 128 KB = 2 KB × 48 (大扇区) + 128 B × 256 (小扇区)。

7) JTAG ID CODE 位 12 至 27 代表器件的 Silicon ID。

8) 该零件为工程样品。

27 订购信息

27.1 料号命名规则

表 72 器件代码命名规则

Field	Description	Value	Meaning					
CY	Cypress (an Infineon company) prefix	CY						
T	Category	T	TRAVEO™					
F	Family name	3	TRAVEO™ T2G (Core M7 Single)					
A	Application	D	Cluster with 2D Graphics					
D	Code-flash/Work-flash/SRAM quantity	L	4160 KB / 128 KB / 384 KB					
P	Packages	B	272-BGA					
		A	216-TEQFP					
H	Hardware option	B	Security on (HSM), RSA - 3K					
I	Marketing option		Audio DAC	MIPI	2 x Video Out ¹⁾	Free graphics software	Qt bundle	Autosar package
		A	No	No	No	No	No	No
		B	No	No	Yes	No	No	No
		C	No	Yes	No	No	No	No
		D	No	Yes	Yes	No	No	No
		E	Yes	No	No	No	No	No
		F	Yes	No	Yes	No	No	No
		G	Yes	Yes	No	No	No	No
		H	Yes	Yes	Yes	No	No	No
		S	Yes	Yes	Yes	Yes ²⁾	Yes	No
		V	Yes	Yes	Yes	Yes	Yes	Yes
		Y	Yes	Yes	Yes	Yes	No	Yes
		Z	Yes	Yes	Yes	Yes ³⁾	No	No
C	Temperature grade	S	S-grade (–40°C to 105°C)					
		E	E-grade (–40°C to 125°C)					

1) "No"表示存在 FPD-link 或 RGB 视频输出之一，"Yes"表示 FPD-link 和 RGB 视频输出均可用。

2) Qt 运行时、英飞凌图形软件包（2D Graphics Driver, Safety Signature Driver, Dynamic Warping Library）。

3) 英飞凌图形软件包（2D Graphics Driver, Safety Signature Driver, Dynamic Warping Library）。

27 订购信息
表 73 订购代码命名规则

Field	Description	Value	Meaning					
CY	Cypress (an Infineon company) prefix	CY						
T	Category	T	TRAVEO™					
F	Family name	3	TRAVEO™ T2G (Core M7 Single)					
A	Application	D	Cluster with 2D Graphics					
D	Code-flash/Work-flash/SRAM quantity	L	4160 KB / 128 KB / 384 KB					
P	Packages	B	272-BGA					
		A	216-TEQFP					
H	Hardware option	B	Security on (HSM), RSA - 3K					
I	Marketing option		Audio DAC	MIPI	2 x Video Out ¹⁾	Free graphics software	Qt bundle	Autosar package
		A	No	No	No	No	No	No
		B	No	No	Yes	No	No	No
		C	No	Yes	No	No	No	No
		D	No	Yes	Yes	No	No	No
		E	Yes	No	No	No	No	No
		F	Yes	No	Yes	No	No	No
		G	Yes	Yes	No	No	No	No
		H	Yes	Yes	Yes	No	No	No
		S	Yes	Yes	Yes	Yes ²⁾	Yes	No
		V	Yes	Yes	Yes	Yes	Yes	Yes
		Y	Yes	Yes	Yes	Yes	No	Yes
		Z	Yes	Yes	Yes	Yes ²⁾	No	No
R	Revision	B	First revision (0x13)					
F	Fab location	Q	UMC (Fab 12i) Singapore					
X	Reserved	1	Reserved					
K	Package code	AE	TEQFP					
		BZ	BGA					
C	Temperature grade	S	S-grade (–40°C to 105°C)					
		E	E-grade (–40°C to 125°C)					
Q	Quality grade	ES	Engineering samples					
		GS	Standard grade of automotive					

(表格续下页.....)

27 订购信息

表 73 (续) 订购代码命名规则

Field	Description	Value	Meaning
S	Shipment type	Blank	Tray shipment
		T	Tape and Reel shipment

- 1) "No" 表示保证 1x 视频输出，即 RGB 视频输出或 FPD-link；"Yes" 表示保证 2x 视频输出，即 RGB 视频输出和 FPD-link。
- 2) 英飞凌图形软件包（2D Graphics Driver, Safety Signature Driver, Dynamic Warping Library）。

28 封装

28 封装

CYT3DL 微控制器提供表 74 中列出的封装形式。

表 74 封装信息

Package	Dimensions ¹⁾	Contact/Lead Pitch	Coefficient of Thermal Expansion	I/O Pins
216-TEQFP	24 × 24 × 1.6 mm (max)	0.4-mm	a1 ²⁾ = 8.4 ppm/°C, a2 ³⁾ = 29.4 ppm/°C	108
272-BGA	16 × 16 × 1.7 mm (max)	0.8-mm	a1 ²⁾ = 11.9 ppm/°C, a2 ³⁾ = 34.3 ppm/°C	135

1) 尺寸 (第 2 列) 适用于室温。

2) a1 = 低于 T_g 的 CTE (热膨胀系数) 值 (ppm/°C) (T_g 是玻璃化转变温度, 为 131°C)。

3) a2 = 高于 T_g 的 CTE 值 (ppm/°C)。

表 75 封装特性¹⁾

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	S-grade	-40	-	105	°C
		E-grade			125	
T_J	Operating junction temperature	150	-	-	150	°C
$R_{\theta JA}$	Package thermal resistance, junction to ambient θ_{JA}	216-TEQFP	-	-	16.2	°C/Watt
		272-BGA	-	-	17.7	°C/Watt
$R_{\theta JB}$	Package thermal resistance, junction to board θ_{JB}	216-TEQFP	-	-	11.9	°C/Watt
		272-BGA	-	-	12.6	°C/Watt
$R_{\theta JC}$	Package thermal resistance, junction to case θ_{JC}	216-TEQFP	-	-	2.4	°C/Watt
		272-BGA	-	-	3.0	°C/Watt

1) 电路板条件符合 JESD51-7 (4层)。

表 76 回流焊峰值温度、封装湿度敏感度等级 (MSL)、IPC/JEDEC J-STD-2

Package	Maximum Peak Temperature (°C)	Maximum Time at Peak Temperature (seconds)	MSL
216-TEQFP	260	30	3
272-BGA	260	30	3

28 封装

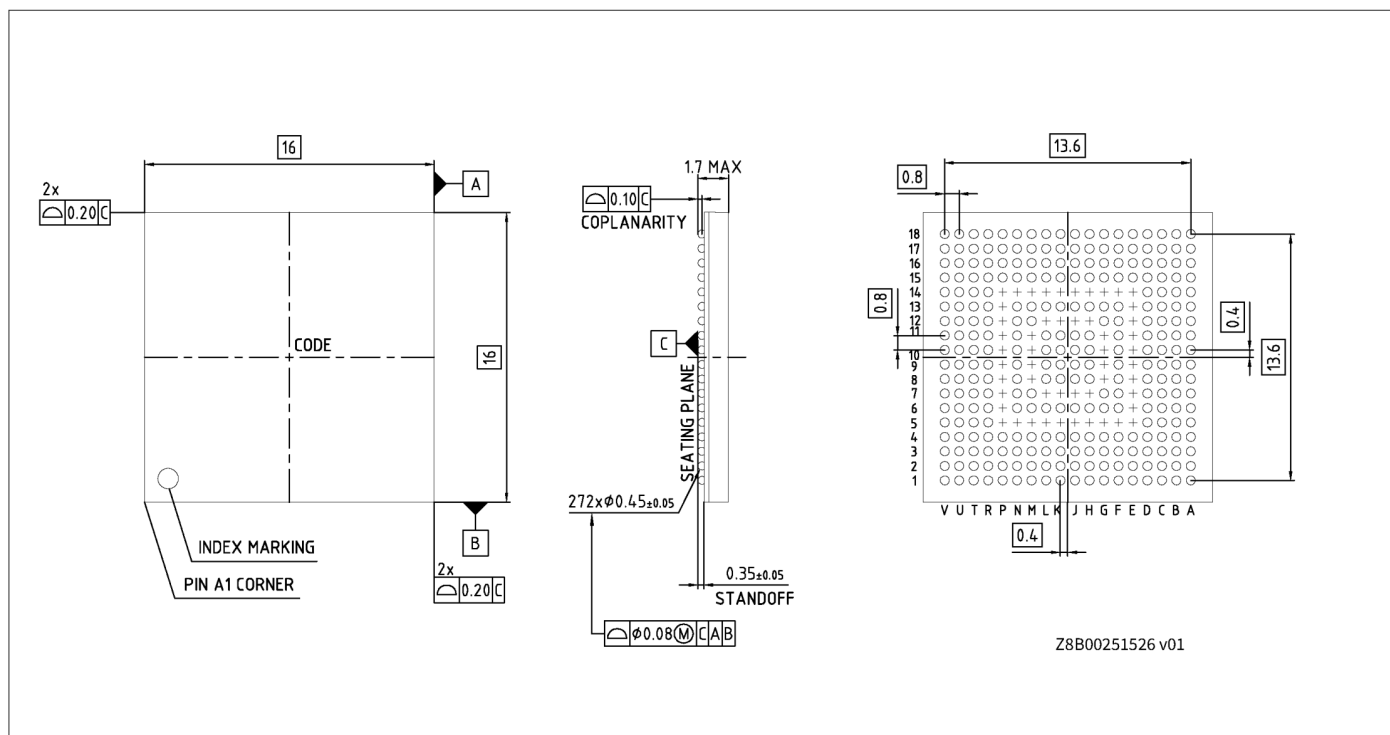
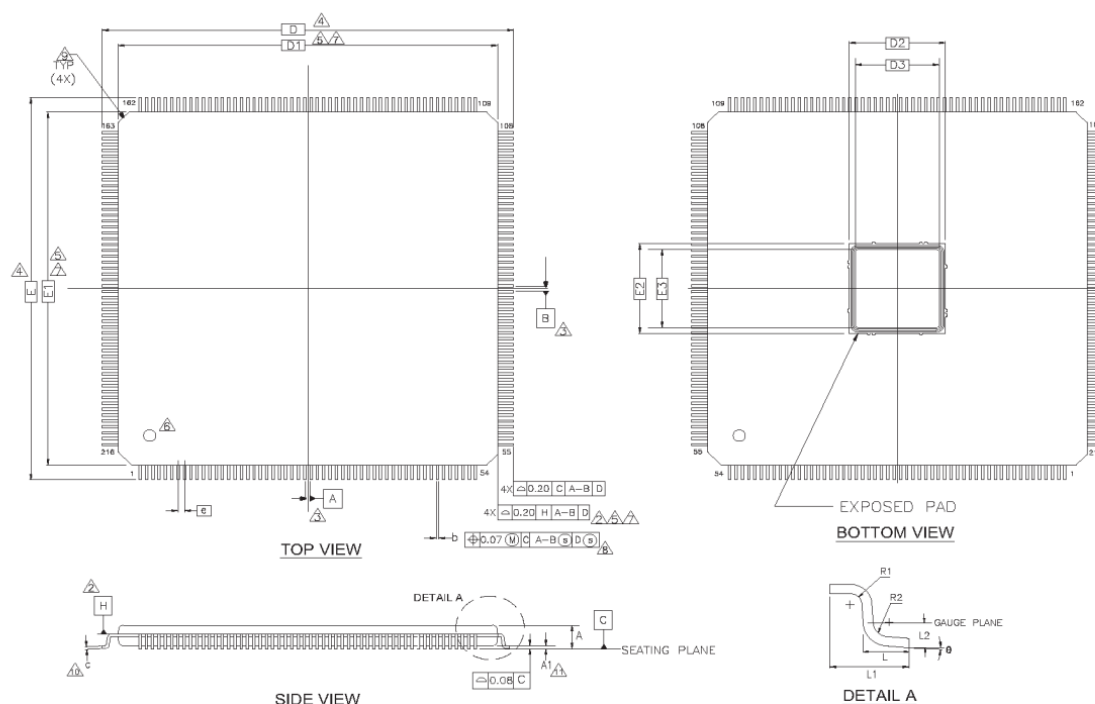


图 48 272 球 FBGA 封装外形图 (PG-LFBGA-272)

28 封装



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
D	26.00 BSC		
D1	24.00 BSC		
D2	7.40 REF		
D3	6.60 REF		
E	26.00 BSC		
E1	24.00 BSC		
E2	7.40 REF		
E3	6.60 REF		
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
c	0.09	0.127	0.20
b	0.13	0.16	0.23
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.40 BSC		

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-30407 **

图 49 216-TEQFP 封装外形图 (PG-TQFP-216)

A 附录
A 附录
A.1 外部 IP 修订
表 77 IP 修订

Module	IP	Revision	Vendor
CAN FD	mxttCAN FD	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex-M0+-r0p1	Arm®
Arm® Cortex®-M7	armcm7	Cortex-M7-r1p2	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100-r3p2	Arm®
Ethernet	mxeth	GEM_GXL r1p09	Cadence

A.2 内部 IP 修订
表 78 内部 IP 修订

Module	Revision
SMIF	SMIF version 3.0 (Variant v3.1)

A.3 支持的 MIPI 格式
表 79 支持的 MIPI 格式 ¹⁾

MIPI Format	ID	Remarks
YUV422 8-bit	0x1E	Full processing supported
YUV422 10-bit	0x1F	
RGB888	0x24	
RGB666	0x23	
RGB565	0x22	
RGB555	0x21	
RGB444	0x20	
RAW8	0x2A	Data can be written to VRAM as is, no color processing or format conversion supported.
RAW10	0x2B	
RAW12	0x2C	
RAW14	0x2D	
RAW16	0x2E	
RAW20	0x2F	
Generic 8-bit Long Packet Data Types	0x10	Supported
	0x11	Data can be written to VRAM as is, no color processing or format conversion supported.

(表格续下页.....)

A 附录

表 79 (续) 支持的 MIPI 格式 ¹⁾

MIPI Format	ID	Remarks
User Defined Byte-based Data	0x30 - 0x37	Data can be written to VRAM as is, no color processing or format conversion supported.

1) CYT3DL 器件不支持 MIPI 数据 ID 类型 0x12。

缩略语
缩略语
表 80 **本文档中使用的缩略语**

Acronym	Description
A/D	Analog to Digital
ABS	Absolute
ADC	Analog to Digital converter
AES	Advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus
Arm®	Advanced RISC machine, a CPU architecture
ASIL	Automotive safety integrity level
BOD	Brown-out detection
CAN FD	Controller Area Network with Flexible Data rate
CMOS	Complementary metal-oxide-semiconductor
CPU	Central Processing Unit
CRC	Cyclic redundancy check, an error-checking protocol
CSV	Clock supervisor
DES	Data encryption standard
DW	Datawire same as P-DMA
ECC	Error correcting code
ECO	External crystal oscillator
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating point unit
GHS	Green hills tool chain with IDE
GPIO	General purpose input/output
HSM	Hardware security module
I/O	Input/output
I2C	Inter-Integrated Circuit, a communications protocol
ILO	Internal low-speed oscillator
IMO	Internal main oscillator
IPC	Inter-processor communication
IrDA	Infrared interface
IRQ	Interrupt request
JTAG	Joint test action group
LIN	Local Interconnect Network, a communications protocol

(表格续下页.....)

缩略语
表 80 (续) 本文档中使用的缩略语

Acronym	Description
LVD	Low voltage detection
OTA	Over-the-air programming
OTP	One-time programmable
OVD	Over voltage detection
P-DMA	Peripheral-Direct Memory Access
PASS	Programmable Analog Subsystem
PLL	Phase Locked Loop
POR	Power-on reset
PPU	Peripheral protection unit
PRNG	Pseudorandom number generator
PSOC™	Programmable system on chip
PWM	Pulse-width modulation
MCU	Microcontroller Unit
MCWDT	Multi-counter watchdog timer
M-DMA	Memory-Direct Memory Access
MISO	Master-in slave-out
MMIO	Memory mapped I/O
MOSI	Master-out slave-in
MPU	Memory protection unit
NVIC	Nested vectored interrupt controller
RAM	Random access memory
RISC	Reduced-instruction-set computing
ROM	Read only memory
RTC	Real-time clock
SAR	Successive approximation register
SCB	Serial communication block
SCL	I2C serial clock
SDA	I2C serial data
SHA	Secure hash algorithm
SHE	Secure hardware extension
SMPU	Shared memory protection unit
SPI	Serial peripheral interface, a communications protocol
SRAM	Static random access memory

(表格续下页.....)

缩略语

表 80 (续) 本文档中使用的缩略语

Acronym	Description
SWD	Single wire debug
TCM	Tightly Coupled Memory
TCPWM	Timer/Counter Pulse-width modulator
TTL	Transistor-transistor logic
TRNG	True random number generator
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
WCO	Watch crystal oscillator
WDT	Watchdog timer reset
XIP	eXecute In Place
XTAL	Crystal

修订记录

修订记录

Document version	Date of release	Description of changes
*I	2024-03-05	Updated Ethernet MAC. Changed description of SID902 and SID902_3 to "Configured Pixel Clock Frequency" Removed text "BGA only;" from the comments of SID904. Changed SID1613 min value from 1.37 to 0.7 V/ns. Added SID1613 and SID1713 in Table 67. Added content under FDP-LINK in Table 68. Updated IMO connections in Figure 3. Updated content for HSIO_STDLN under I2C Interface-Standard-mode, I2C Interface-Fast-mode, and I2C Interface-Fast-Plus mode in Table 39. Removed SID68 in Figure 12. Updated Errata.
*J	2025-06-24	Updated the code-flash, maximum ambient temperature, and GPIO_STD in Table 1. Updated Ethernet MAC. Added +B input in Table 16. Updated the following in Table 30: - Updated details/conditions for: SID33B, SID26B, SID34, SID34_2 - Added Spec ID: SID33I, SID26B_125, SID33B_125, SID34_125, SID34_2_125, SID36_125 Updated the following in Table 31: - Included support for E-grade devices - Updated min and max values for SID606 and SID606A - Updated details/conditions for: SID51C, SID52C, SID50B - Added Spec ID: SID51C_125, SID52C_125, SID50B_125 Updated the following in Table 33: - Updated details/conditions for: SID73, SID82, SID83, SID84, SID85 - Added Spec ID: SID73_125, SID82_125, SID83_125, SID84_125, SID85_125 Updated the legends in Figure 15. Updated the following in Table 34: - Updated details/conditions for: SID670, SID670A, SID670C, SID653B, SID657B, SID676H - Added Spec ID: SID670_125, SID670A_125, SID670C_125, SID653B_125, SID657B_125, SID676H_125 Updated the following in Table 36: - Updated details/conditions for: SID104, SID105, SID109, SID109A, SID110, SID111, SID112, SID115, SID115B, SID115D, SID115A, SID115C, SID115E - Added Spec ID: SID104_125, SID105_125, SID109_125, SID109A_125, SID110_125, SID111_125, SID112_125, SID115_125, SID115B_125, SID115D_125, SID115A_125, SID115C_125, SID115E_125

修订记录

Document version	Date of release	Description of changes
*J	2025-06-24	Updated the following in Table 39: - Added SID129_3 and SID129_4 - Updated the description for SID129_2 Updated the following in Table 62: - Updated details/conditions for: SID1319, SID1004, SID1007, SID1008, SID1009 - Added Spec ID: SID1319_125, SID52C_125, SID50B_125, SID Added note and updated the following in Table 68: - Updated details/conditions for: SID884, SID885, SID885B - Added Spec ID: SID923, SID884_125, SID885_125, SID885B_125 Updated Table 69. Updated the following in Table 71: - Added products CYT3DLBBSS, CYT3DLBBVS, CYT3DLBBYS, CYT3DLBBZS, CYT3DLABSS, CYT3DLABVS, CYT3DLABYS, and CYT3DLABZS - Added note [84] to support E-grade devices Added Free graphics software, Qt bundle, and Autosar package columns and marketing option for S, V, Y, and Z values in Table 72, and Table 73. Update note [93] in Table 73. Updated Figure 48. Updated the following in Table 75: - Updated conditions and max value for T_A, T_J - Updated max values for $R_{\theta JA}$, $R_{\theta JB}$, and $R_{\theta JC}$ Added Revision history change log. Removed Errata.
*K	2025-12-04	Updated Table 39. Updated Table 16. Updated Table 72. Updated Table 73. Updated Figure 16. Updated Figure 3, Figure 4, Figure 7, Figure 8, Figure 9 as per the Infineon branding. Added two Base device codes in Table 71.
*L	2026-07-03	Updated tables: Table 1, Table 2, Table 3, Table 4, Table 14, Table 25, Table 26, Table 27, Table 44, Table 48, Table 68, Table 77, Table 78, and Table 79. Updated document template.

修订记录变更日志

修订 *L 部分更新

Section	Change description	Current spec	New spec	Reason for change
Description	Added automotive compliance statement	No compliance statement	Added ISO 26262 functional safety and ISO 21434 cybersecurity compliance statement	Updated
Features	Updated Security feature description	Previous security description	ISO 21434 compliant/EVITA Full	Updated
Features	Under Table 1 , updated Functional Safety feature description	Functional safety description	ISO 26262 ASIL-B compliant	Updated
Features list	Under Table 1 , updated Security entry	Previous security specification	ISO 21434 compliant	Correction
Features list	Under Table 1 , updated Functional Safety entry	Previous functional safety specification	ISO 26262 ASIL-B compliant	Correction
Features list	Updated Video Capture feature description	Previous Video Capture description	One Capture (1× RGB or 1× MIPI CSI-2, up to 4 lanes)	Correction
Features	Updated feature formatting	Existing formatting	Bold formatting applied to feature and sub-feature headings	Editorial
Alternate function pin assignments	Corrected table heading orientation for Table 18	Incorrect table heading orientation	Corrected orientation	Correction
Electrical specifications	Under Table 60 , updated RMI reference clock frequency tolerance	±50 ppm	±100 ppm	Updated
Electrical specifications	Under Table 60 , added SID375B specification	N/A	RMI reference Clock frequency (output) added	Addition
Electrical specifications	Updated RMI reference clock description	Existing description	RMI reference Clock frequency (input)	Correction
Packaging	In Table 75 , updated package characteristic value	–	Updated value as per review comment	Updated
Packaging	In Table 75 , updated package maximum temperature value	145/145.5	150/150	Updated

修订记录变更日志

表 81 Rev. *L 电气规格更新

Spec ID	Description	Changed item	Current spec	New spec	Reason for change
SID375B	RMII reference Clock frequency (output)	New parameter	N/A	Newly added	Added specification
SID375 A	RMII reference Clock frequency (input)	Description	RMII reference Clock frequency	RMII reference Clock frequency (input)	Updated description
SID375	Clock frequency tolerance	MII TX/RX_CLK Clock frequency value	±50 ppm	±100 ppm	Updated

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