

英飞凌 TRAVEO™ T2G 32 位汽车类 MCU

基于 Arm® Cortex® -M7 单核/双核

概述

CYT3BB/4BB 是 TRAVEO™ T2G 微控制器系列，针对汽车系统，例如高端车身控制单元。CYT3BB/4BB 有一个或两个 Arm® Cortex® -M7 CPU 用于主处理，还有一个 Arm® Cortex® -M0+ CPU 用于外设和安全处理。这些器件包含嵌入式外设，支持具有灵活数据速率的控制器区域网络 (CAN FD)、本地互连网络 (LIN) 和以太网。TRAVEO™ T2G 器件采用先进的 40 纳米工艺制造。CYT3BB/4BB 集成低功耗闪存、多个高性能模拟和数字外设，并支持创建安全的计算平台。

特性

• CPU 子系统

- 一至两个^[1] 250 MHz 32 位 Arm® Cortex® -M7 CPU，每个都具有
 - 单周期乘法
 - 单/双精度浮点单元 (FPU)
 - 16 KB 数据缓存、16 KB 指令缓存
 - 存储器保护单元 (MPU)
 - 16 KB 指令和 16 KB 数据紧耦合存储器 (TCM)
- 100 MHz 32 位 Arm® Cortex® M0+ CPU，带有
 - 单周期乘法
 - MPU
- 硬件支持处理器之间通信
- 三个 DMA 控制器
 - 外设 DMA 控制器 #0 (P-DMA0) 带 100 个通道
 - 外设 DMA 控制器 #1 (P-DMA1) 带 58 个通道
 - 内存 DMA 控制器 (M-DMA0) 带 8 个通道

• 集成存储器

- 4160 KB 代码闪存，另加 256 KB 工作闪存
 - 边读边写 (RWW) 允许在执行代码闪存/工作闪存时对其进行更新
 - 单组和双组模式（专门用于无线固件更新 [FOTA]）
 - 通过 SWD / JTAG 接口进行 Flash 烧写
- 768 KB SRAM，具有可选保留粒度

• 加密引擎

- 支持增强型安全硬件扩展 (eSHE) 和硬件安全模块 (HSM)
- 安全启动和身份验证
 - 使用数字签名验证
 - 使用快速安全启动
- AES: 128 位块，128/192/256 位密钥
- 3DES: 64 位块，64 位密钥
- 向量单元支持非对称密钥加密算法（如 Rivest-Shamir-Adleman (RSA) 和 Elliptic Curve (ECC)）
- SHA-1/2/3: SHA-512、SHA-256、SHA-160，输入数据长度可变
- CRC: 支持 CCITT CRC16 和 IEEE-802.3 CRC32
- 真随机数生成器 (TRNG) 和伪随机数生成器 (PRNG)
- 伽罗瓦/计数器模式 (GCM)

• 功能安全可达 ASIL-B 标准

注:

1. 选定的 MPN 支持双核 Cortex-M7 CPU。有关更多信息，请参阅[订购信息](#)。

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

特性

- 存储器保护单元 (MPU)
- 共享存储器保护单元 (SMPU)
- 外设保护单元 (PPU)
- 看门狗计时器 (WDT)
- 多计数器看门狗定时器 (MCWDT)
- 低电压检测器 (LVD)
- 电压欠压检测 (BOD)
- 过压检测 (OVD)
- 时钟监视器 (CSV)
- 所有安全关键型存储器 (SRAM, Flash, TCM) 均采用硬件纠错 (SECDED ECC)
- **低功耗 2.7 V 至 5.5 V 操作**
 - 低功耗运行、睡眠、低功耗睡眠、深度睡眠和休眠模式，可实现精细的电源管理
 - 可配置选项以实现稳健的电压欠压检测 (BOD)
 - V_{DD} 和 V_{DDA} 上 BOD 的两个阈值电平 (2.7 V 和 3.0 V)
 - V_{CCD} 上 BOD 的一个阈值电平 (1.1 V)
- **唤醒**
 - 最多两个引脚可从休眠模式唤醒
 - 最多 220 个 GPIO 引脚可从睡眠模式唤醒
 - 事件发生器、SCB、看门狗计时器、RTC 警报可从深度睡眠模式中唤醒
- **时钟**
 - 内部主振荡器 (IMO)
 - 内部低速振荡器 (ILO)
 - 外部晶体振荡器 (ECO)
 - 时钟晶体振荡器 (WCO)
 - 锁相环 (PLL)
 - 锁频环 (FLL)
- **通信接口**
 - 最多八个 CAN FD 通道
 - 与传统 CAN 相比，数据速率提高 (高达 8 Mbps)，但受物理层拓扑和收发器的限制
 - 符合 ISO 11898-1:2015 标准
 - 支持 Bosch CAN FD 规范 V1.0 对非 ISO CAN FD 的所有要求
 - ISO 16845:2015 证书可用
 - 多达 11 个运行时可配置的串行通讯功能块 (SCB) 通道，每个功能块可配置为 I²C, SPI, 或 UART
 - 最多 16 个独立 LIN 通道
 - LIN 协议符合 ISO 17987 标准
 - 一个符合 IEEE-802.3bw 的 10/100 Mbps 以太网 MAC 接口
 - 支持以下 PHY 接口：媒体独立接口 (MII)
 - 精简媒体独立接口 (RMII)
 - 符合 IEEE-802.1BA 音频视频桥接 (AVB) 标准
 - 符合 IEEE-1588 精确时间协议 (PTP)

特性

• 外部存储器接口

- 一个SPI (单、双、四或八) 或HYPERBUS™ 接口
- 即时加密和解密
- 从外部存储器就地执行 (XIP)

• SDHC 接口

- 一个安全数字大容量 (SDHC) 接口, 支持嵌入式多媒体卡 (eMMC)、安全数字 (SD) 或安全数字输入输出 (SDIO)
 - 符合 eMMC 5.1、SD 6.0 和 SDIO 4.10 规范
- 数据速率高达 SD 高速 50 MHz 或 eMMC 52 MHz DDR

• 音频接口

- 三个 IC 间音频 (I²S) 接口, 用于连接数字音频设备
- I²S、左对齐或时分复用 (TDM) 音频格式
- 独立的发送或接收操作, 各自处于主模式或从模式

• 定时器

- 最多 75 个 16 位和 8 个 32 位定时器/计数器脉宽调制器 (TCPWM) 模块
 - 最多 12 个 16 位计数器用于电机控制
 - 最多 63 个 16 位计数器和 8 个 32 位计数器用于常规操作
 - 支持定时器、捕获、正交解码、脉冲宽度调制 (PWM)、带死区时间的 PWM (PWM_DT)、伪随机 PWM (PWM_PR) 和移位寄存器 (SR) 模式
- 最多 16 个事件生成 (EVTGEN) 定时器, 支持从深度睡眠模式循环唤醒
 - 事件触发特定的器件操作 (例如中断处理程序的执行、SAR ADC 转换等)

• 实时时钟(RTC)

- 年/月/日、星期几、时:分:秒字段
- 12 小时和 24 小时格式
- 自动闰年校正

• I/O

- 最多 220 个可编程 I/O
- 三种 I/O 类型
 - GPIO 标准 (GPIO_STD)
 - GPIO 增强 (GPIO_ENH)
 - 高速 I/O 标准 (HSIO_STD)

• 稳压器

- 支持 2.7 V 至 5.5 V 输入电压生成 1.1 V 内核电压
- 三个稳压器:
 - 深度睡眠
 - 核芯内部
 - 核芯外部

• 可编程的模拟资源

- 三个 SAR A/D 转换器, 最多有 75 个外部通道 (72 个 I/O + 3 个用于电机控制的 I/O)
 - ADC0 支持 32 个逻辑通道, 具有 32 + 1 个物理连接
 - ADC1 支持 32 个逻辑通道, 具有 32 + 1 个物理连接
 - ADC2 支持 8 个逻辑通道, 具有 8 + 1 个物理连接
 - 任何外部通道均可连接到相应 SAR 中的任何逻辑通道
- 每个 ADC 支持 12 位分辨率和高达 1 Msps 的采样率
- 每个 ADC 还支持六个内部模拟输入, 如
 - 带隙基准建立绝对电压水平

特性

- 用于结温计算的校准二极管
- 两个 AMUXBUS 输入和两个直接连接至电源监测器
- 每个 ADC 支持外部多路复用器的寻址
- 每个 ADC 都有一个序列器，支持对配置的通道进行自主扫描
- 针对电机感应应用对所有 ADC 进行同步采样
- **智能I/O**
 - 最多 5 个智能 I/O 块，可对往返于 I/O 的信号执行布尔运算
 - 支持最多 36 个 I/O (GPIO_STD)
- **调试接口**
 - 符合 IEEE-1149.1-2001 的 JTAG 控制器和接口
 - Arm®串行线调试 (SWD) 端口
 - 支持Arm®嵌入式跟踪宏单元 (ETM)
 - 使用 SWD 进行数据跟踪
 - 使用JTAG进行指令和数据跟踪
- **与行业标准工具兼容**
 - GHS MULTI 或 IAR EWARM 用于代码开发和调试
- **封装**
 - - 100-TEQFP, 14 × 14 × 1.6 毫米 (最大), 0.5 毫米引脚间距
 - - 144-TEQFP, 20 × 20 × 1.6 毫米 (最大), 0.5 毫米引脚间距
 - - 176-TEQFP, 24 × 24 × 1.6 毫米 (最大), 0.5 毫米引脚间距
 - 272-BGA, 16 × 16 × 1.7 毫米 (最大), 0.8 毫米球距
- **认证**
 - 符合 AEC-Q100 的汽车应用要求

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功能列表

1 特性列表

表 1-1 CYT3BB/4BB 所有封装特性列表

Features	Packages			
	100-TEQFP	144-TEQFP	176-TEQFP	272-BGA
CPU				
Core	One or two 32-bit Arm® Cortex®-M7 CPUs and a 32-bit Arm® Cortex® M0+ CPU			
Functional safety	ASIL-B			
Operating voltage	2.7 V to 5.5 V			
Operating voltage for HSIO_STD	Not supported			2.7 V to 3.6 V
Core voltage	1.05 V to 1.15 V			
Operating frequency	Arm® Cortex®-M7 250 MHz (max for each) and Arm® Cortex®-M0+ 100 MHz (max)			
MPU, PPU	Supported			
FPU	Supports both single (32-bit) and double (64-bit) precision			
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M7 CPUs			
TCM	16-KB instruction and 16-KB data for each Cortex-M7 CPU			
存储器				
Code-flash	4160 KB (4032 KB + 128 KB)			
Work-flash	256 KB (192 KB + 64 KB)			
SRAM (configurable for retention)	768 KB			
ROM	64 KB			
通信接口				
CAN0 (CAN-FD: Up to 8 Mbps)	4 ch			
CAN1 (CAN-FD: Up to 8 Mbps)	4 ^[3] /3 ^[4] ch	4 ch		
CAN RAM	32 KB per instance (CAN0/1), 64 KB in total			
Serial communication block (SCB/UART)	9 ch	10 ch		11 ch
Serial communication block (SCB/I²C)	9 ^[5] /8 ^[6] ch	10 ch		11 ch
Serial communication block (SCB/SPI)	8 ch	10 ch		11 ch
LIN	9 ch	12 ch	16 ch	
Ethernet MAC	1 ch × 10/100 (ETH0, MII/RMII on GPIO_STD)			
存储器接口				
eMMC/SD	1 ch (GPIO_STD at 32 MHz)			1 ch (HSIO_STD at 50 MHz, GPIO_STD at 32 MHz)
Single SPI / Dual SPI / Quad SPI / Octal SPI / HYPERBUS™	1 ch (GPIO_STD at 32 MHz)			1 ch (HSIO_STD at 100 MHz, GPIO_STD at 32 MHz)



功能列表

表 1-1 CYT3BB/4BB所有封装特点列表 (续)

Features	Packages			
	100-TEQFP	144-TEQFP	176-TEQFP	272-BGA
定时器				
RTC	1 ch			
TCPWM (16-bit) (Motor Control)	12 ch			
TCPWM (16-bit)	63 ch			
TCPWM (32-bit)	8 ch			
External interrupts	72	116	148	220
模拟模块				
12-bit, 1 Msps SAR ADC	3 Units (SAR0/32, SAR1/32, SAR2/8 logical channels)			
	37 external channels (SAR0/14 ch, SAR1/15 ch, SAR2/8 ch)	52 external channels (SAR0/21 ch, SAR1/23 ch, SAR2/8 ch)	64 external channels (SAR0/24 ch, SAR1/32 ch, SAR2/8 ch)	72 external channels (SAR0/32 ch, SAR1/32 ch, SAR2/8 ch)
	18 ch (6 per ADC) Internal sampling			
Motor control input	3 ch (synchronous sampling of one channel on each of the 3 ADCs)			
安全				
Flash security (program/work read protection)	Supported			
Flash chip erase enable	Configurable			
eSHE / HSM	By separate firmware ^[2]			
音响				
I ² S / TDM	Tx 2 ch, Rx 2 ch	Tx 3 ch, Rx 3 ch		
系统				
DMA controller	P-DMA0 with 100 channels (16 general-purpose), P-DMA1 with 58 channels (8 general-purpose), and M-DMA0 with 8 channels			
Internal main oscillator	8 MHz			
Internal low speed oscillator	32.768 kHz (nominal)			
PLL	Input: 3.988 to 33.34 MHz, PLL output: up to 250 MHz			
FLL	Input: 0.25 to 80 MHz, FLL output: up to 100 MHz			
Watchdog timer and Multi-counter Watchdog timer	Supported (WDT + 3× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM7_0, MCWDT#2 to CM7_1			
Clock supervisor	Supported			
Cyclic wakeup from DeepSleep	Supported			
GPIO_STD	68	112	144	203
GPIO_ENH	4			
HSIO_STD	Not supported			13
Smart I/O (Blocks)	3 blocks, mapped through 15 I/Os	5 blocks, mapped through 27 I/Os	5 blocks, mapped through 36 I/Os	
Low-voltage detect	Two, 26 selectable levels			

注：
2. 增强型安全硬件扩展 (eSHE) 和硬件安全模块 (HSM) 支持由第三方固件启用。



功能列表

表 1-1 CYT3BB/4BB所有封装特点列表 (续)

Features	Packages			
	100-TEQFP	144-TEQFP	176-TEQFP	272-BGA
Maximum ambient temperature	105 °C for S-grade, 125 °C for E-grade			
Debug interface	SWD/JTAG			
Debug trace	Arm® Cortex®-M7 ETB size of 8 KB, Arm® Cortex® M0+ MTB size of 4 KB			

1.1 通讯外设实例列表

下表列出了通讯外设在每个封装下支持的实例，根据实现功能所需的最少引脚数。

表1-2 通讯外设实例列表

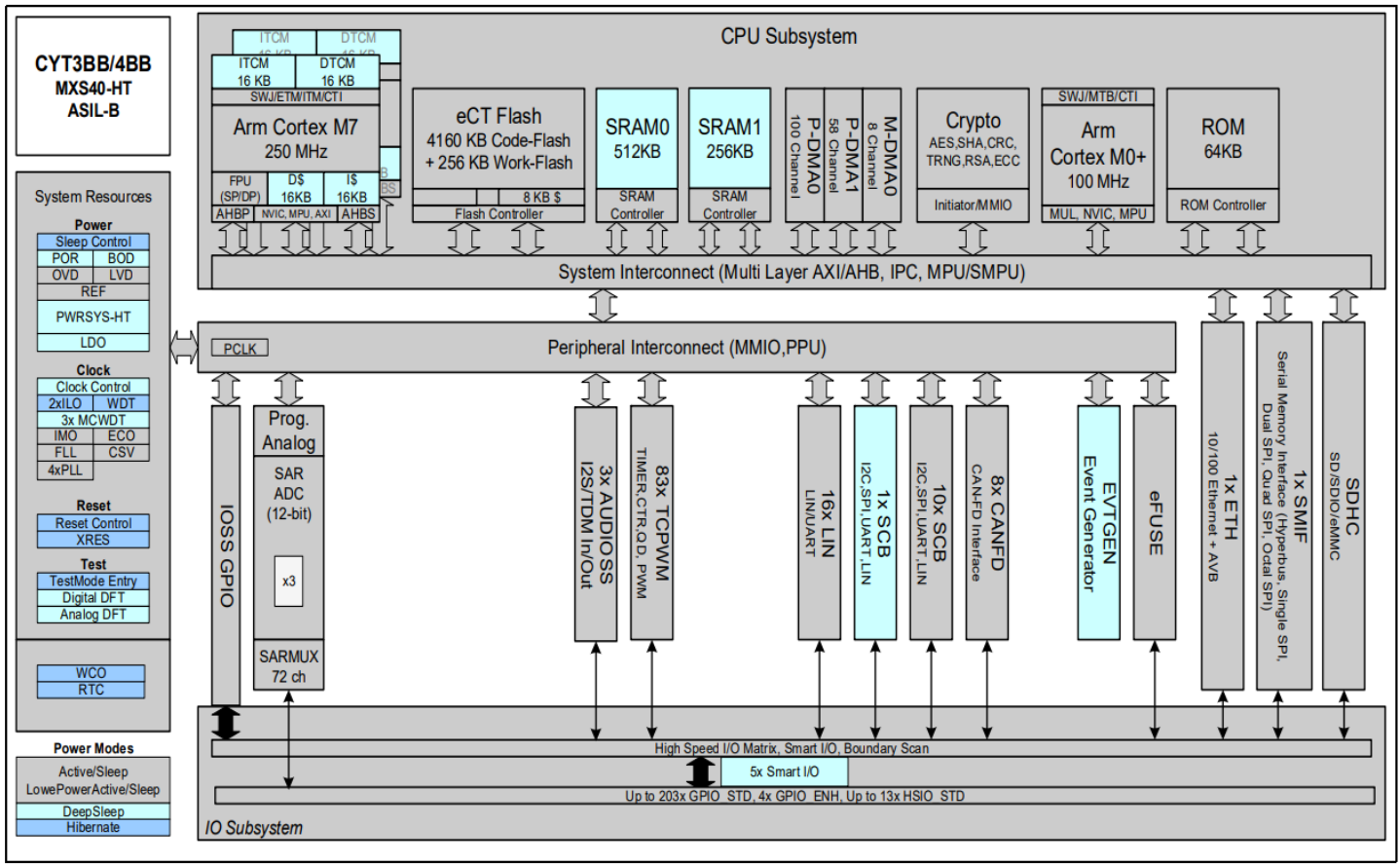
Module	100-TEQFP	144-TEQFP	176-TEQFP	272-BGA	Minimum pin functions
CAN0	0/1/2/3	0/1/2/3	0/1/2/3	0/1/2/3	TX, RX
CAN1	0/1/2/3 ^[3] or 0/2/3 ^[4]	0/1/2/3	0/1/2/3	0/1/2/3	TX, RX
LIN0	0/1/2/3/4/6/7/8/9	0 to 11	0 to 15	0 to 15	TX, RX
SCB/UART	0 to 8	0 to 9	0 to 9	0 to 10	TX, RX
SCB/I2C	0 to 8 ^[5] or 0/1/2/3/4/5/7/8 ^[6]	0 to 9	0 to 9	0 to 10	SCL, SDA
SCB/SPI	0/1/2/3/4/5/7/8	0 to 9	0 to 9	0 to 10	MISO, MOSI, SCK, SELECT0

注:

- 3. 在 P22.1 上的 EXT_PS_CTL0 功能未使用。
- 4. 在 P22.1 上的 EXT_PS_CTL0 功能使用。
- 5. 在 P21.1 上的 EXT_PS_CTL0 功能和在 P21.2 上的 EXT_PS_CTL1 功能未使用。
- 6. 在 P21.1 上的 EXT_PS_CTL0 功能或在 P21.2 上的 EXT_PS_CTL1功能使用。

2 模块和功能

2.1 框图



框图显示了CYT3BB/4BB架构框图，其中给出了子系统和模块之间互连的简化视图。CYT3BB/4BB有四个主要子系统：CPU、系统资源、外设和 I/O^[7,8,9]。颜色编码显示最低功率模式，其中特定功能块仍然起作用。

CYT3BB/4BB器件能够为硬件和固件的编程、测试、调试和跟踪提供广泛的支持。

调试片上功能支持使用生产器件进行系统调试。它不需要特殊的接口、调试转接板、模拟器或仿真器。

JTAG接口与I-jet、J-Link和GHS等行业标准的第三方探测器完全兼容。调试电路默认启用。

CYT3BB/4BB 提供高水平的安全性，具有强大的闪存保护以及禁用调试等功能。

此外，如果某些应用担心网络钓鱼攻击会通过器件恶意重新编程或试图启动和中断闪存编程序列来击败安全设定，所有器件接口都可以被永久禁用。当器件的最大安全级别被使能时，将禁用所有编程、调试和测试接口。

注：

- GPIO_STD 支持 2.7 V 至 5.5 V V_{DDIO} 范围。
- GPIO_ENH 支持 2.7 V 至 5.5 V V_{DDIO} 范围，在较低电压下可产生较高的电流。
- HSIO_STD 支持 2.7 V 至 3.6 V V_{DDIO} 范围，具有高速信号和可编程驱动强度。

3 功能说明

3.1 CPU 子系统

3.1.1 CPU

CYT3BB/4BB CPU子系统包含一个32位Arm® Cortex®-M0+ CPU带有MPU，以及一个或两个32位Arm® Cortex®-M7 CPU，每个都带有MPU、单/双精度FPU以及16 KB数据和指令缓存。该子系统还包括 P-/M-DMA 控制器、加密加速器、4160 KB 代码闪存、256 KB 工作闪存、768 KB SRAM 和 64 KB ROM。

Cortex® -M0+ CPU 提供了安全、不可中断的启动函数。这保证了启动函数完成后，系统完整性有效且权限得到强制执行。共享资源（闪存、SRAM、外设等）可以通过总线仲裁进行访问，并且使用硬件信号量的处理器间通讯（IPC）机制来支持独占访问。

每个Cortex® -M7 CPU 具有 16 KB 指令和 16 KB 数据 TCM，并带有可编程读取等待状态。每个TCM时钟均由相关的Cortex® -M7 CPU 时钟提供。

3.1.2 DMA控制器

CYT3BB/4BB 有三个DMA控制器：具有16个通用通道和84个专用通道的P-DMA0、具有8个通用通道和50个专用通道的P-DMA1以及具有8个通道的M-DMA0。P-DMA用于外设到存储器和存储器到外设的数据传输，并为大量通道提供低延迟。每个P-DMA控制器使用单个数据传输引擎并由相关通道共享。通用通道具有丰富的互连矩阵，包括 P-DMA交叉触发，可满足苛刻的数据传输场景的要求。专用通道具有单个触发输入（例如ADC 通道）来处理常见的传输需求。M-DMA用于存储器到存储器的数据传输，并为少量通道提供高内存带宽。M-DMA为每个通道使用专用的数据传输引擎。它们支持使用AHB多层总线去独立访问外设。

3.1.3 Flash

CYT3BB/4BB 具有 4160 KB（4032 KB 扇区大小为 32 KB，128 KB 扇区大小为 8 KB）的代码闪存，以及额外的工作闪存 256 KB（192 KB 扇区大小为 2 KB，64 KB 扇区大小为 128 B）。工作闪存经过了优化，可以比代码闪存进行更多次重新编程。代码闪存支持边写边读（RWW）操作，允许在CPU运行模式时更新闪存。代码闪存和工作闪存区域均支持远程升级（OTA）编程的双库操作。

3.1.4 SRAM

CYT3BB/4BB 具有 768 KB 的 SRAM 和两个独立的控制器。SRAM0 以 32 KB 的增量提供在深度睡眠模式保留，而 SRAM1 可在完全保留或不保留之间选择。

3.1.5 ROM

CYT3BB/4BB 具有 64 KB 的 ROM，其中包含启动和配置例程。该ROM可实现安全启动和用户的闪存验证，以保证系统的安全。

3.1.6 安全加密加速器

密码加速器实现(3)DES功能块密码、AES功能块密码、SHA散列、循环冗余校验、伪随机数生成、真随机数生成、伽罗瓦/计数器模式和矢量装置以支持RSA和ECC等非对称密钥密码。

3.2 系统资源

3.2.1 电源系统

电源系统确保供电电压水平满足每种电源模式的要求，并在这些水平无效时提供全系统复位。内部上电复位 (POR) 确保在初始上电斜坡期间全芯片复位。

三个BOD 电路监测外部电源电压 (V_{DD0} 、 V_{DDA} 、 V_{CCD})。在 V_{DD0} 和 V_{CCD} 上的BOD 最初是启用的，不能禁用。 V_{DDA} 上的BOD 最初是禁用的，用户可以启用。对于外部电源 V_{DD0} 和 V_{DDA} ，BOD 电路可通过软件配置两种设置：2.7 V 最小电压，适用于所有内部信号，3.0 V 最小电压，也适用于所有 I/O 规格（保证在 2.7 V）。 V_{CCD} 的BOD 作为安全措施提供，而不是一个强大的屏障。

提供三个过压检测 (OVD) 电路用于监控外部电源 (V_{DD0} 、 V_{DDA} 、 V_{CCD})，以及过流检测电路 (OCD) 用于监控内部和外部稳压器。 V_{DD0} 和 V_{DDA} 上的 OVD 阈值可配置为两种设置：5.0 V 和 5.5 V 最大电压。

监测器提供了两个电压检测电路，用于检测下降和上升电平的外部供电电压 (V_{DD0})，每个电路可配置 26 个可选电平之一。

V_{DD0} 和 V_{CCD} 上的所有 BOD、OVD 和 OCD 电路 都会产生复位，因为它们可保护 CPU 和故障逻辑。 V_{DDA} 上的 BOD 和 OVD 电路可配置为产生复位或故障。

3.2.2 稳压器

CYT3BB/4BB 包含三个稳压器，为低压核晶体管提供电源：深度睡眠、核内和核外。这些稳压器接受 2.7 V 至 5.5 V V_{DD0} 供电，并为器件的各个部分提供低噪声的 1.1 V 供电。

在电源模式之间切换时，硬件和固件会自动启用和禁用这些调压器。核内和核外稳压器在工作模式下运行，并为 CPU 子系统和相关外设提供电源。

3.2.2.1 深度睡眠

深度睡眠稳压器用于在深度睡眠模式下维持供电给少数模块。这些模块包括 ILO 和 WDT 定时器、BOD 检测器、SCB0、SRAM 存储器、智能 I/O 和其他配置存储器。深度睡眠稳压器在深度睡眠模式下启用，此时核内稳压器被禁用。当 XRES_L 有效（低电平）并且核内稳压器被禁用时，它被禁用。

3.2.2.2 核芯内部

核内稳压器支持高达 300 mA 的负载电流，并且在器件启动（启动过程）期间以及在工作/睡眠模式下运行。

3.2.2.3 核芯外部^[10]

为了支持最坏情况的负载，当 M7 CPU 和 M0+ CPU 都处于最大时钟频率并且所有集成外设都运行时，需要一个核外部稳压器，其负载电流可达 600 mA。虽然核外部稳压器的控制和监测器电路位于 CYT3BB/4BB 内部，但供电调节元件（NPN 传输晶体管、PMIC或LDO）位于外部。这降低了 CYT3BB/4BB 封装内的整体功率耗散，同时保持了良好调节的核供电。

核芯外部调压器可以通过外部 NPN 通道晶体管、PMIC或线性电压调压器 (LDO) 来实现。每个实施都需要在PCB上的不同外部器件，以及与 CYT3BB/4BB 的不同连接以进行调节和控制。

注：

10. 当 CYT3BB/4BB 处于休眠模式时，用于控制核芯外部调压器的 GPIO 为高阻态。这可能需要一个外部上拉或下拉电阻来禁用外部调压器，并将其配置为最小工作电流。

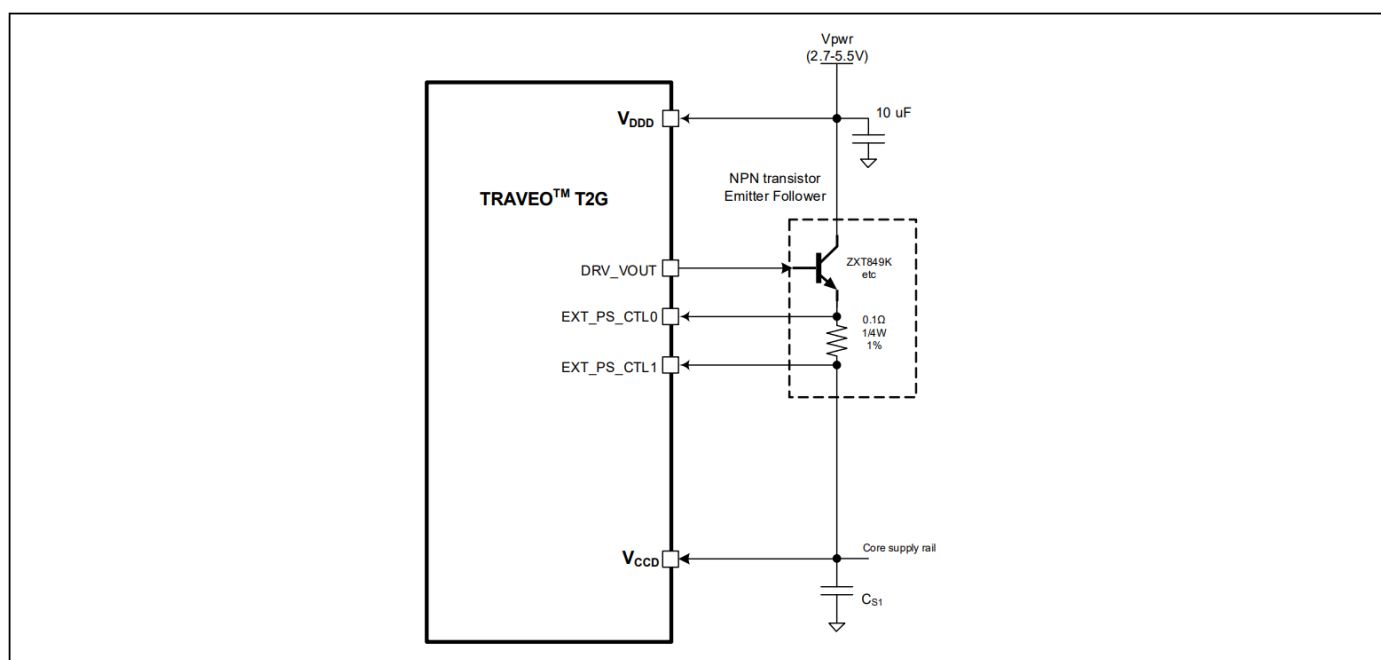


图 3-1 带 NPN 晶体管的核芯外部调压器示例

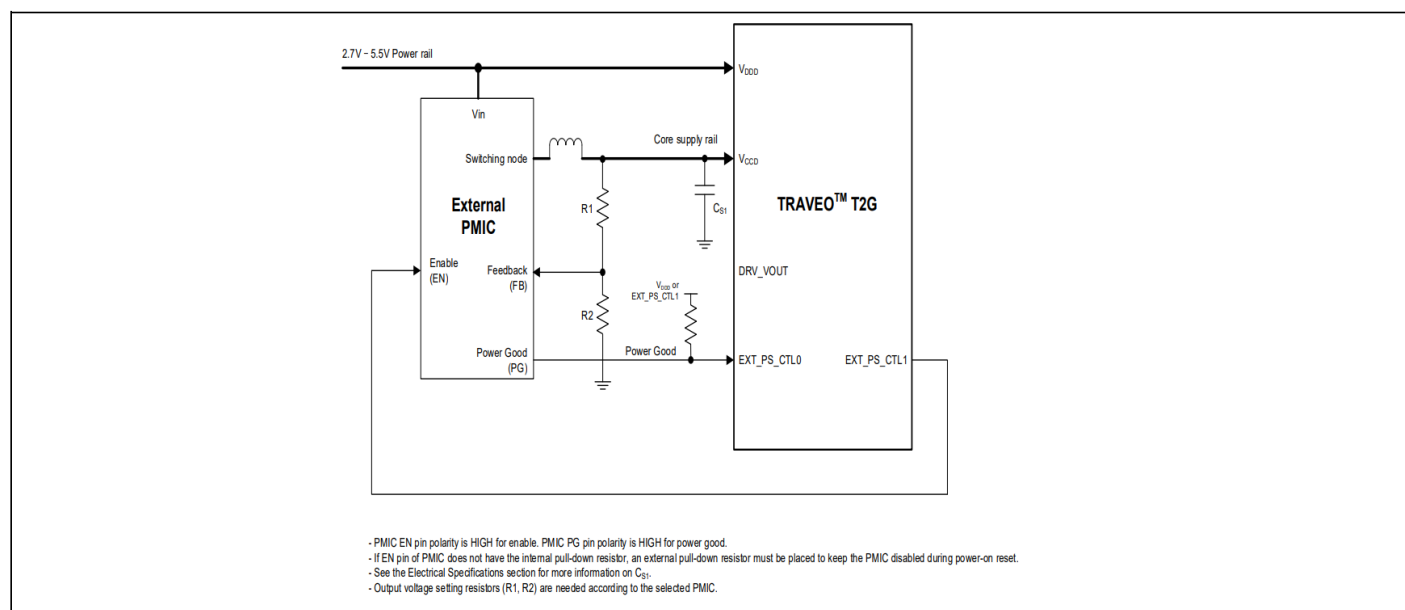


图 3-2 带PMIC / LDO的核芯外部调压器示例

核芯内部和核芯外部调压器都需要连接到VCCD引脚的外部大容量存储电容器。该电容器在低压核芯晶体管的动态负载下提供充电。

3.2.3 时钟系统

CYT3BB/4BB 时钟系统为所有需要它们的子系统提供时钟，并在不同时钟源之间实现无缝切换。此外，它还确保不发生亚稳态。

CYT3BB/4BB 的时钟系统由 8 MHz IMO、两个 ILO、四个看门狗定时器、四个 PLL、一个 FLL、五个时钟监视器 (CSV)、一个 8 至 33.34 MHz ECO 和一个 32.768 kHz WCO 组成。

时钟系统支持三个主时钟域：CLK_HF，CLK_SLOW和CLK_LF。

- CLK_HF_x 是运行模式时钟。每个都可以使用任何高频时钟源，包括 IMO、EXT_CLK、ECO、FLL 或 PLL
- CLK_SLOW 为 Cortex-CM0+ CPU、Crypto、P-/M-DMA 和 CPU 子系统的其他慢速基础模块提供基准时钟
- CLK_LF是深度睡眠域时钟，为MCWDT或RTC模块提供基准时钟。CLK_LF 域的基准时钟可以禁用，也可以从 ILO0、ILO1 或WCO中选择。

表 3-1 CLK_HF 目标

Name	Description
CLK_HF0	CPUSS (Memories, CLK_SLOW, Peripherals)
CLK_HF1	CPUSS (Cortex-M7 CPU 0, 1)
CLK_HF2	CAN FD, LIN, TCPWM, SCB, SAR
CLK_HF3	Event Generator
CLK_HF4	Ethernet Internal Clock
CLK_HF5	Audio Subsystem (I ² S), Ethernet TSU
CLK_HF6	SDHC Interface, SMIF

3.2.3.1 IMO时钟源

IMO是 CYT3BB/4BB 中的频率基准，当没有外部基准可用或使能时。IMO 的运行频率约为 8 MHz。

3.2.3.2 IMO时钟源

ILO 是一种低功耗振荡器，标称频率为 32.768 kHz，在深度睡眠模式下为看门狗定时器产生时钟。有两个 ILO 可确保深度睡眠模式下的时钟监控器 (CSV) 功能。可以根据 IMO、WCO 或 ECO 来校准 ILO 驱动的计数器，以提高其准确性。ILO1 也用于时钟监控。

3.2.3.3 PLL 和 FLL

可以使用 PLL（两个 200 MHz 和两个 400 MHz 中的一个）或FLL从IMO、ECO或EXT_CLK生成高速时钟。FLL 提供比PLL更快的锁定速度（5 μs 而不是 45 μs），但频率误差较小（±2%）^[11]。400 MHz PLL 支持向下扩频时钟产生器（SSCG）。

3.2.3.4 时钟监控器

每个时钟监控器 (CSV) 允许一个时钟 (基准) 监控另一个时钟(被监控)的行为。每个 CSV 都有用于监控和参考时钟的计数器。每个计数器的参数决定基准时钟的频率以及受监控时钟的频率上限和下限。如果频率范围比较器检测到停止的时钟或指定频率范围之外的时钟，则会发出异常状态信号并产生复位或中断。

注：

11. 由于允许的频率误差，不建议使用基于FLL的基准来操作基准定时外设（例如通用非同步收发传输器）。

3.2.3.5 EXT_CLK

三个 GPIO_STD I/O 中的一个可用于提供高达 80 MHz 的外部时钟输入。该时钟可以用作 PLL 或 FLL 的源时钟，也可以直接由 CLK_HF 域使用。

3.2.3.6 ECO

ECO使用连接到 ECO_IN 和 ECO_OUT 引脚的外部晶振提供高频时钟。它支持基模（非泛音）石英晶振，范围为 8 至 33.34 MHz。当与 PLL 结合使用时，它会生成 CPU 和外部设置时钟，最高频率可达器件的最大频率。ECO精度取决于所选的晶振。如果 ECO 被禁用，则相关引脚可用于任何可用的 I/O 功能。

3.2.3.7 WCO

WCO是一款低功耗时钟晶振振荡器，适用于实时时钟应用。它需要一个外部 32.768-kHz 晶振连接到 WCO_IN 和 WCO_OUT 引脚。WCO还可以配置为 CLK_LF 的时钟基准，CLK_LF 是MCWDT和RTC的时钟源。

3.2.4 复位

CYT3BB/4BB 可以从多种来源复位，包括软件。复位事件是异步的，并能够确保器件恢复到一个已知状态。复位原因（POR、BOD、OVD、过流、XRES_L、WDT、MCWDT、软件复位、故障、CSV、休眠唤醒、调试）记录在一个寄存器中，该寄存器在复位后保留，并允许软件确定复位的原因。XRES_L引脚可用于外部复位。

3.2.5 看门狗定时器

CYT3BB/4BB 具有 1 个看门狗定时器（WDT）和 3 个多计数器看门狗定时器（MCWDT）。

WDT 是一个自由运行的计数器，仅由 ILO0 提供时钟，因此可以将其用作休眠模式的唤醒源。在所有运行模式下都可以进行看门狗操作。为了防止因WDT超时而导致器件复位，必须在配置的窗口期间对WDT进行服务。看门狗复位被记录在复位原因寄存器中。

每个 CPU 核心都有一个 MCWDT。这些定时器提供比WDT更多的功能，并且仅在运行、睡眠和深度睡眠模式下可用。这些计时器有多个计数器，可以单独使用或级联使用来触发中断和/或复位。它们由 ILO0 或 WCO 提供时钟。

3.2.6 功耗模式

CYT3BB/4BB 有六种运行模式。

- 运行 – 所有外围设备均可用
- 低功耗运行 (LPACTIVE) – 运行模式的低功耗配置，其中所有外设和 CPU 均可用，但功能有限
- 睡眠 – 除 CPU 外的所有外设均可用
- 低功耗睡眠 (LPSLEEP) – 睡眠模式的低功耗配置，其中除 CPU 之外的所有外设均可用，但功能有限
- 深度睡眠 – 仅可使用与 CLK_LF 配合使用的外设
- 休眠 – 器件和 I/O 状态被冻结，器件在唤醒时会复位

3.3 外设

3.3.1 外设时钟分频器

提供整数和小数时钟分频器用于外设和定时目的。

表 3-2 时钟分频器 - CPUSS 组 (Nr.0)

Divider type	Instances	Description
div_8	3	Integer divider, 8 bits
div_16	1	Integer divider, 16 bits

表 3-3 时钟分频器 - COMM 组 (Nr.1)

Divider type	Instances	Description
div_8	16	Integer divider, 8 bits
div_16	17	Integer divider, 16 bits
div_24_5	16	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 外设保护单元

外设保护单元(PPU)控制和监视从所有主设备(CPU、P-/M-DMA、加密和任何启用的调试接口)到外设的未经授权的访问。它允许或限制总线基础设施上的数据传输。访问规则是根据传输的特定属性来强制执行的，例如传输的地址范围和访问属性（例如读/写、用户/权限和安全/非安全）。

3.3.3 12位SAR ADC

CYT3BB/4BB 包含三个 1 Msps SAR ADC。这些 ADC 的时钟频率最高可达 26.67 MHz，可在 26 个时钟周期内提供12位结果。所有三个 SAR ADC 的参考均来自一对专用输入：VREFH 和 VREFL^[12]。

CYT3BB/4BB 支持最多 93 个逻辑 ADC 通道，以及来自最多 75 个 I/O 的外部输入。每个 ADC 还支持六个内部连接，用于诊断和监控目的。[表 1-1](#) 列出了 ADC 通道数量（每个 ADC 和封装类型）。

每个 ADC 都有一个序列器，它以零切换开销自主循环通过已配置的通道（序列器扫描）（也就是说，当时钟频率为 26.67 MHz 时，无论是用于单个通道还是分布在多个通道上，总采样带宽都等于 1 Msps）。序列器切换通过状态机或固件控制。序列器对触发请求进行优先级排序，启用适当的模拟通道，控制 ADC 采样，启动 ADC 数据转换，管理结果，并启动后续的重复转换或组转换，而无需 CPU 干预。

每个 SAR ADC 都有一个模拟多路复用器，用于将要测量的信号连接到 ADC。它有 32 个 GPIO_STD 输入、一个用于电机感应的特殊 GPIO_STD 输入，以及六个附加输入，用于测量内部信号，如带隙基准、温度传感器和电源。该器件支持三个 ADC 上一个电机检测通道的同步采样。

CYT3BB/4BB 有一个温度传感器，由三个 ADC 共享。温度传感器每次只能由一个 ADC 采样。需要软件后处理将温度传感器读数转换为开尔文或摄氏度值。

为了适应具有不同源阻抗和频率的信号，可以为每个通道编程不同的采样时间。每个 ADC 还支持范围比较，这样可以快速检测超范围值，而无需等待序列器扫描完成，也无需等待 CPU 固件评估超范围值的测量值。由于 ADC 需要高速时钟，因此它们在深度睡眠和休眠模式下不可用。ADC 输入基准电压 VREFH 范围为 2.7 V 至 V_{DDA} ，VREFL 为 V_{SSA} 。

注：

12.VREF_L 可防止 VSSIO 和 VSSA 路径中的 IR 压降影响测量。当 VREF_L 正确连接时，可以降低或消除 VSSIO 和 VSSA 路径中的 IR 压降对测量的影响。

3.3.4 定时器/计数器/脉宽调制器模块 (TCPWM)

TCPWM功能块由16位（75个通道）和32位（8个通道）计数器组成，具有用户可编程周期。其中 12 个 16 位计数器针对电机控制操作进行了优化。每个 TCPWM 计数器包含一个捕获寄存器，用于记录发生事件时的计数值，一个周期寄存器（用于停止或自动重新加载计数器当如果它的计数值等于周期寄存器的值）和多个比较寄存器，可用于产生作为PWM占空比的输出。

TCPWM功能块中的每个计数器都支持多种功能模式，例如定时器、捕获、正交、PWM、带死区插入的PWM（PWM_DT，8位）、伪随机PWM（PWM_PR）和移位寄存器。

在电机控制应用中，TCPWM功能块内的计数器支持增强型正交模式，具有非对称PWM产生、死区插入（16位）以及PWM输出信号的不同死区关联等功能。

TCPWM 模块还提供了正向输出和反向输出间，它们之间具有可编程偏移，以允许它们用作死区反向 PWM 输出。TCPWM 模块还有一个 (Kill) 输入（仅适用于PWM模式）用于强制输出进入预定状态；例如，在马达驱动系统中，当出现过电流状态时，需要立即使用它来关闭驱动FET的PWM（没有时间软件干预）。

3.3.5 串行通信模块 (SCB)

CYT3BB/4BB 包含多达 11 个串行通讯模块，每个模块都可配置为支持 I²C、UART或SPI。

3.3.5.1 I2C接口

SCB可配置为实现完整的 I2C^主设备（能够进行多主设备仲裁）或从设备接口。每个由 SCB 配置的 I2C^主都可以以高达 1 Mbps 的速度运行（增强型快速模式），并具有灵活的缓冲选项，以减少中断开销和 CPU 的延迟。此外，每个SCB都支持接收和发送数据的 FIFO 缓冲，这通过增加 CPU 读取数据的时间，减少了时钟延长的需要。I2C^{接口}与标准、快速模式和增强型快速模式设备兼容，并按 NXP I2C 总线规范和用户手册 (UM10204) 中指定。I2C 总线I/O通过开漏模式的 GPIO 实现^[13、14]。

3.3.5.2 UART接口

当配置为UART，每个SCB提供全功能UART，其最大信号速率由配置的外设时钟频率和过采样率确定。它支持红外接口 (IrDA) 和智能卡 (ISO 7816) 协议，这些协议是UART协议的小变种。此外，它还支持9位多处理器模式，此模式允许寻址连接到通用RX和TX线的外设。支持通用UART功能，如奇偶校验、停止位的数量、中断检测和帧错误。发送和接收数据的 FIFO 缓冲允许容忍更大的 CPU 服务延迟。

LIN 协议由 UART 支持。LIN 基于单主多从拓扑结构。LIN总线上有一个主节点和多个从机节点。SCB UART 仅支持LIN从机功能。

与专用 LIN 模块相比，以SCB/UART 用作 LIN 需要更高水平的软件交互和增加 CPU 负载。

注：

13. 这并非 100% 符合 I²C总线规范；I/O 不耐过压，不支持增强型快速模式的 20 mA 灌电流要求，并且在不供电的情况下违反泄漏规范。

14. 只有 Port 0 启用斜率控制下满足最小下降时间要求。

3.3.5.3 SPI接口

SPI 配置支持完整的 Motorola SPI、TI 同步串行协议 (SSP，本质上是添加启动脉冲用于同步基于 SPI 的编解码) 和 National Microwire (SPI 的半双工形式)。SPI 接口可以使用 FIFO。SPI 接口以高达 12.5 MHz 的 SPI 时钟运行。SCB 还支持 EZSPI^[15] 模式。

SCB0 支持以下附加功能：

- 在深度睡眠模式下可作为从机操作
- I²C 从机 EZ (EZI²C^[16]) 模式，最多可容纳 256-B 数据缓冲 无需 CPU 干预即可实现多字节通讯
- I²C 从机外部供时钟操作
- 具有 512-B 数据缓冲器的指令/响应模式，用于多字节通讯，无需 CPU 干预

3.3.6 CAN FD

CYT3BB/4BB 包含两个 CAN FD 控制器模块，每个模块支持四个 CAN FD 通道。所有 CAN FD 控制器均符合 ISO 11898-1:2015 标准；可提供 ISO 16845:2015 证书。它还在硬件中完全实现了 ISO 11898-4 (TTCAN 协议级别 1 和 2) 中指定的时间触发 CAN (TTCAN) 协议。所有与信息处理有关的功能均由 Rx 和 Tx 处理程序实现。Rx 处理器管理信息接受过滤、将接收到的消息从 CAN 核心传输到消息 RAM，并提供接收消息状态。Tx 处理器负责将发送信息从信息 RAM 传输到 CAN 核心，并提供发送消息状态。

3.3.7 局域互连网络 (LIN)

CYT3BB/4BB 包含最多 16 个 LIN 块。每个功能块都支持按照 LIN ISO 标准 17987 的协议传输/接收数据。每个 LIN 功能块通过 3 针接口 (包括使能函数) 连接到外部收发器，并支持主机和从机功能。每个功能块还支持经典和增强的检验和，以及消息接收和唤醒信令期间的中断检测。断点检测、同步场、校验和计算以及错误中断均由硬件处理。

3.3.8 Ethernet MAC

CYT3BB/4BB 支持一个以太网通道，传输速率为 10 或 100 Mbps。输入/输出帧和流量控制符合以太网/IEEE 802.3bw 标准以及 IEEE 1588 精确时间协议 (PTP)。CYT3BB/4BB 支持使用外部 PHY 设备的全双工数据传输。MAC 支持通过 IEEE 标准 MII 和 RMII 接口与 PHY 进行无缝连接。该器件还支持音频-视频桥接 (AVB)。MAC 支持标准的 6 字节可编程地址。使用 **AHB-Lite** 接口进行 DMA 访问。

3.3.9 外部存储器接口

除了内部闪存外，CYT3BB/4BB 还支持直接连接多达 128 MB 的外部快闪式存储器或 RAM 存储器。此连接是通过 HYPERBUS™ 或串行接口 (SPI) 建立的。HYPERBUS™ 允许连接 HYPERFLASH™ 和 HYPERRAM™ 设备，而 SPI (单、双、四或八进制 SPI) 可以连接串行闪存。通过该接口连接的闪存中存储的代码允许就地执行 (XIP) 操作，这不需要先将指令复制到内部内存，并且对于需要安全的外部数据和代码的环境可以进行即时加密和解密。

注：

15. Easy SPI (EZSPI) 协议基于摩托罗拉 SPI 协议在任何模式 (0、1、2 或 3) 下运行的。它允许主机和从机之间进行通信，同时减少 CPU 干预的需要。
16. Easy I²C (EZI²C) 协议是 赛普拉斯 在 I²C 协议基础上构建的独特通信方案。它使用标准 I²C 协议周围的元协议，使用索引内存传输与 I²C 从机进行通信。这减少了对 CPU 干预的需要。

3.3.10 SDHC 接口

CYT3BB/4BB 支持一个安全数字大容量 (SDHC) 接口，符合安全数字 (SD) 6.0、安全数字输入输出 (SDIO) 4.10 和嵌入式多媒体卡 (eMMC) 5.1 规范以及主控接口 (HCI) 4.2 规范。该接口支持系统 DMA (SDMA)、高级 DMA (ADMA2、ADMA3) 和指令队列 (CQ) 功能。该接口支持 SD DS (默认速度，25 MHz 时为4位)、SD HS (高速，50 MHz时为4位) 和 eMMC 52 MHz DDR (52 MHz 卡时钟时为 8 位) 的数据速率。

3.3.11 音频接口

CYT3BB/4BB 支持三种IC音频总线(I²S)实例，用于连接数字音频设备：支持主从模式下的I²S左对齐 (LJ) 和八通道时分复用 (TDM) 数字音频格式，接收和发送方向均可独立操作。

3.3.12 一次性可编程 (OTP) eFuse

CYT3BB/4BB 包含一个 1024 位OTP eFuse 存储器，可用于存储和访问每个器件的唯一且不可更改的标识符或序列号。eFuse 还用于控制器件的生命周期 (制造、编程、正常运行、寿命终止等) 和安全状态。在 1024 位中，192 位可供用户使用。

3.3.13 事件发生器

事件发生器支持在运行模式下产生中断和触发，以及在深度睡眠模式下产生中断。事件发生器用于触发特定的器件操作 (执行中断处理程序、SAR ADC 转换等) 并提供从深度睡眠模式的循环唤醒机制。它们为器件功能提供无需 CPU 的触发器，减少 CPU 在触发器件功能时的参与，从而降低总体功率消耗和处理开销。

3.3.14 触发多路复用器

CYT3BB/4BB 支持使用触发信号连接各种外设。触发器用于通知外部设备事件的发生或状态的改变。这些触发器用于影响或启动其他外围设备的某些操作。触发器多路复用器用于将触发器从来源设备路由到目的地。触发器提供主动的逻辑功能，并且通常在运行模式下支持。

3.4 I/Os

CYT3BB/4BB 具有多达 220 个可编程 I/O。

I/O 被组织为称为端口的逻辑实体，其最大宽度为 8 位。在上电和复位期间，I/O 被强制进入 High-Z 状态。在休眠模式期间，I/O 被冻结。

每个I/O引脚都能生成一个中断(如果中断被使能)，并且每个I/O端口都有一个与其相关的中断请求 (IRQ) 和中断服务子程序 (ISR) 向量。

I/O 端口功率源映射列于 [表 3-4](#) 中。相关电源决定了 配置为 CMOS 和汽车阈值时的 V_{OH} 、 V_{OL} 、 V_{IH} 和 V_{IL} 电平。

表 3-4 I/O 端口 电源

Supply pins	Ports
VDDD	P0, P1, P2, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23, P28, P29, P30, P31
VDDIO_1	P6, P7, P8, P9, P32
VDDIO_2	P10, P11, P12, P13, P14, P15, P26, P27
VDDIO_3	P24, P25

3.4.1 端口命名法

Px.y 描述 I/O 端口“x”内可用的特定位“y”。例如，P4.2 读取“端口 4，位 2”。

每个 I/O 实现以下内容：

- 可编程驱动模式
 - 高阻抗
 - 电阻上拉
 - 电阻下拉
 - 开漏和强下拉模式
 - 开漏和强上拉模式
 - 强力上拉或下拉
 - 弱上拉或下拉

CYT3BB/4BB 有三种类型的可编程 I/O：GPIO 标准、GPIO 增强型和 HSIO 标准。

3.4.2 GPIO 标准 (GPIO_STD)

支持 2.7 V 至 5.5 V_{DDIO} 范围内的标准汽车信号。GPIO 标准 I/O 具有多个可配置的驱动级别、驱动模式和可选的输入级别。

3.4.3 GPIO 增强 (GPIO_ENH)

支持 2.7 V 至 5.5 V_{DDIO} 范围内的扩展功能汽车信号，可在较低电压下提供更高的电流（完全 I²C 时序支持、斜率控制）。

GPIO_STD 和 GPIO_ENH 都实现了以下内容：

- 可配置输入阈值（CMOS、TTL 或汽车）
- 保持模式，用于锁存先前状态（即保持 I/O 状态处于深度睡眠模式）
- 模拟输入模式（输入和输出缓冲区禁用）

3.4.4 HSIO 标准 (HSIO_STD)

这些 I/O 专门针对高速信号传输进行了优化，不支持斜率控制、深度睡眠模式操作、POR 模式控制、模拟连接或非 CMOS 信号传输级别。HSIO_STD 支持高速外设，例如 QSPI、HYPERBUS™、以太网和 SDHC 控制器。HSIO_STD 还支持可编程驱动强度。这些 I/O 仅在运行模式下可用，并在深度睡眠模式下保留状态。

3.4.5 智能 I/O

智能 I/O 允许对从芯片子系统发送到 I/O 的信号或进入芯片的信号进行布尔运算。CYT3BB/4BB 有五个智能 I/O 块。操作可以是同步或异步，并且块可以在除休眠之外的所有器件功率模式下操作。

4 CYT3BB/4BB 地址映射

CYT3BB/4BB 微处理器支持所示的存储空间如 [图4-1](#)。

- 4160 KB (4032 KB + 128 KB) 代码闪存，用于单组或双组模式基于相关的位元在闪存控制寄存器
 - 单库模式：4160 KB
 - 双组模式：每组 2080 KB
- 256 KB (192 KB + 64 KB) 工作闪存，用于单组或双组模式基于相关的位元在闪存控制寄存器
 - 单组模式：256 KB
 - 双组模式：每组128KB
- 64 KB 安全 ROM
- 768 KB SRAM （前 2 KB 保留供内部使用）
- 每个 Cortex-M7 CPU 有 16 KB 指令 TCM
- 每个 Cortex-M7 CPU 有 16 KB 数据 TCM
- 128 MB SMIF XIP

CYT3BB/4BB 地址映射

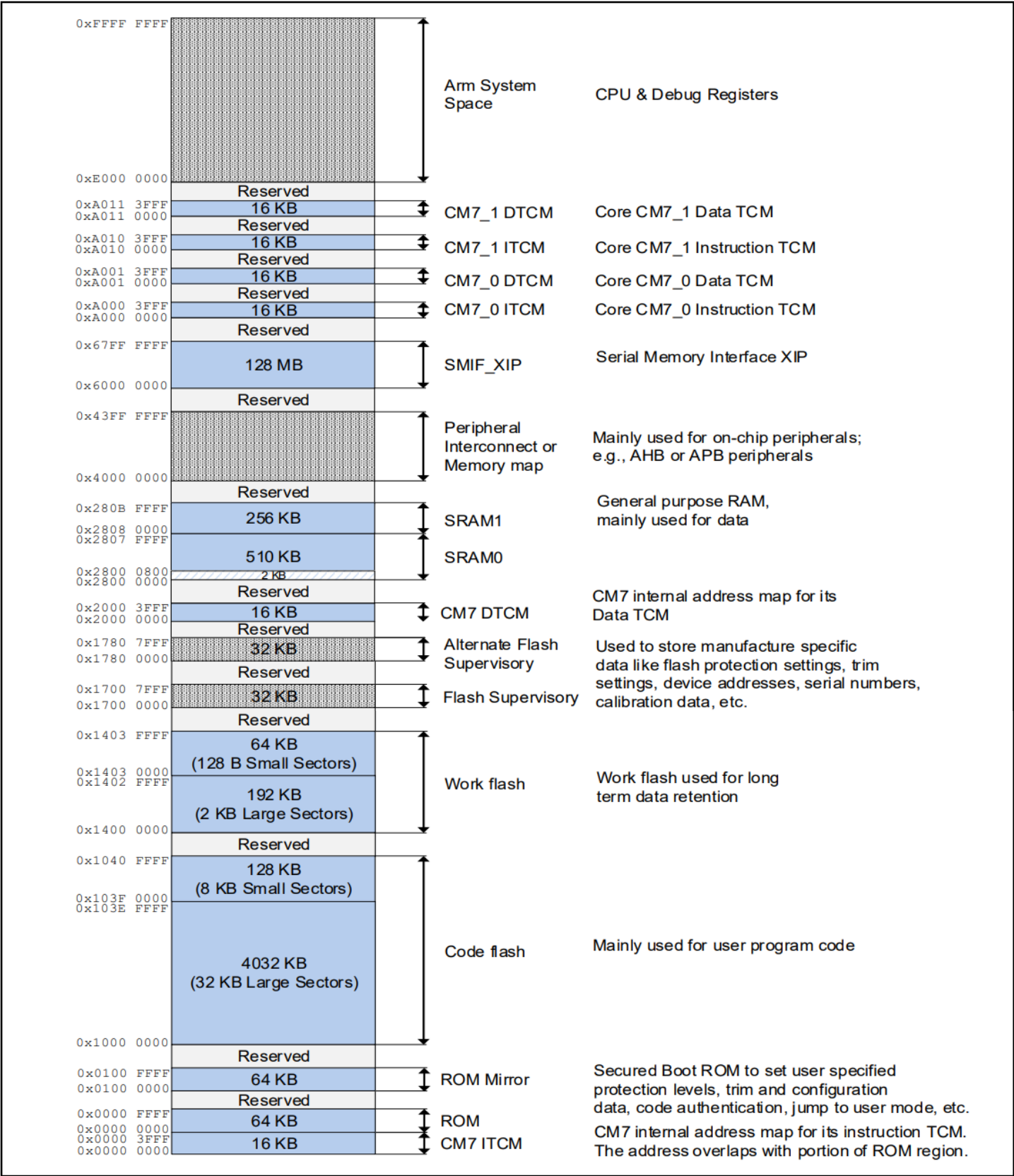


图 4-1 CYT3BB/4BB 地址映射^[17, 18]
注:

17. 尺寸表示不符合比例。
18. 前 2KB SRAM 被保留，不供用户使用。用户必须将 SRAM0 的前 32KB 功能块的保持供电，在所有的工作、低功耗工作、睡眠、低功耗睡眠、深度睡眠模式下无论使能还是保持。

闪存基地址映射

5 闪存基地址映射

表 5-1 通过表 5-6 提供有关代码和工作闪存区域的扇区映射及其各自基地址的信息。

表 5-1 单组模式下代码闪存地址映射

Code-flash Size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large Sector Base Address	Small Sector Base Address
4160	32 KB × 126	8 KB × 16	0x1000 0000	0x103F 0000

表 5-2 单组模式下工作闪存地址映射

Work-flash Size (KB)	Large Sectors	Small Sectors	Large Sector Base Address	Small Sector Base Address
256	2 KB × 96	128 B × 512	0x1400 0000	0x1403 0000

表 5-3 双组模式下的代码闪存地址映射（映射 A）

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1000 0000	0x101F 8000	0x1200 0000	0x121F 8000

表 5-4 双组模式下的代码闪存地址映射（映射 B）

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1200 0000	0x121F 8000	0x1000 0000	0x101F 8000

表 5-5 双组模式下工作闪存地址映射（映射 A）

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
256	2 KB × 48	128 B × 256	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000	0x1500 0000	0x1501 8000

表 5-6 双组模式下的工作闪存地址映射（映射 B）

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
256	2 KB × 48	128 B × 256	2 KB × 48	128 B × 256	0x1500 0000	0x1501 8000	0x1400 0000	0x1401 8000

6 外设 I/O 映射

表 6-1 CYT3BB/4BB 外设 I/O 映射

Section	Description	Base Address	Instances	Instance Size	Group	Slave
PERI	Peripheral interconnect	0x4000 0000			0	0
	Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9)	0x4000 4000	9	0x40		
	Peripheral trigger group	0x4000 8000	11	0x400		
	Peripheral 1:1 trigger group	0x4000 C000	11	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4002 0000			0	1
	PERI Programmable PPU	0x4002 0000	10 ^[19]	0x40		
	PERI Fixed PPU	0x4002 0800	700	0x40		
PERI_PCLK	Peripheral Clock Groups	0x4004 0000	2	0x2000	0	2
CRYPTO	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000			2	2
	IPC structures	0x4022 0000	8	0x20		
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000			2	3
	Shared memory protection unit structures	0x4023 2000	16	0x40		
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	Flash controller	0x4024 0000			2	4
SRSS	System Resources Sub-System Core Registers	0x4026 0000			2	5
	Clock Supervision High Frequency	0x4026 1400	8	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Clock PLL 400 MHz	0x4026 1900	2	0x10		
	Multi Counter WDT	0x4026 8000	3	0x100		
	Free Running WDT	0x4026 C000	1			
BACKUP	SRSS Backup Domain/RTC	0x4027 0000			2	6
	Backup Register	0x4027 1000	4	0x04		
P-DMA	P-DMA0 Controller	0x4028 0000			2	7
	P-DMA0 channel structures	0x4028 8000	100	0x40		
	P-DMA1 Controller	0x4029 0000			2	8
	P-DMA1 channel structures	0x4029 8000	58	0x40		
M-DMA	M-DMA0 Controller	0x402A 0000			2	9
	M-DMA0 channels	0x402A 1000	8	0x100		

注：

19. 这些可编程 PPU 由 Boot ROM 配置，并根据访问权限供用户使用。请参阅特定于设备的 TRM 以了解有关这些可编程 PPU 的配置的更多信息。

外设 I/O 映射

表 6-1 CYT3BB/4BB 外设 I/O 映射 (续)

Section	Description	Base Address	Instances	Instance Size	Group	Slave
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	10
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	33	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	33	0x80	3	1
SMARTIO	Programmable I/O configuration	0x4032 0000			3	2
	SMARTIO port configuration	0x4032 0C00	5	0x100		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	3
	Event generator 0 comparator structures	0x403F 0800	16	0x20		
SMIF	Serial Memory Interface 0 (SMIF0)	0x4042 0000			4	0
	SMIF0 Devices	0x4042 0800	1	0x80		
SDHC	Secure Digital High Capacity 0 (SDHC0)	0x4046 0000			4	1
	SDHC0 Wrap	0x4046 0000				
	SDHC0 Core	0x4046 1000				
ETH	Ethernet 0 (ETH0)	0x4048 0000	1	0x10000	4	2
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	16	0x100		
TTCANFD	CAN0 controller	0x4052 0000	4	0x200	5	1
	Message RAM CAN0	0x4053 0000		0x8000		
	CAN1 controller	0x4054 0000	4	0x200	5	2
	Message RAM CAN1	0x4055 0000		0x8000		
TCPWM	Timer/Counter/PWM 0 (TCPWM0)	0x4058 0000			5	3
	TCPWM0 Group #0 (16-bit)	0x4058 0000	63	0x80		
	TCPWM0 Group #1 (16-bit, Motor control)	0x4058 8000	12	0x80		
	TCPWM0 Group #2 (32-bit)	0x4059 0000	8	0x80		
SCB	Serial Communications Block (SPI/UART/I ² C)	0x4060 0000	11	0x10000	6	0-10
I ² S	I ² S Audio Subsystem	0x4080 0000	3	0x1000	8	0-2
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR1 channel controller	0x4090 1000				
	SAR2 channel controller	0x4090 2000				
	SAR0 channel structures	0x4090 0800	32	0x40		
	SAR1 channel structures	0x4090 1800	32	0x40		
	SAR2 channel structures	0x4090 2800	8	0x40		

7 CYT3BB/4BB 时钟图

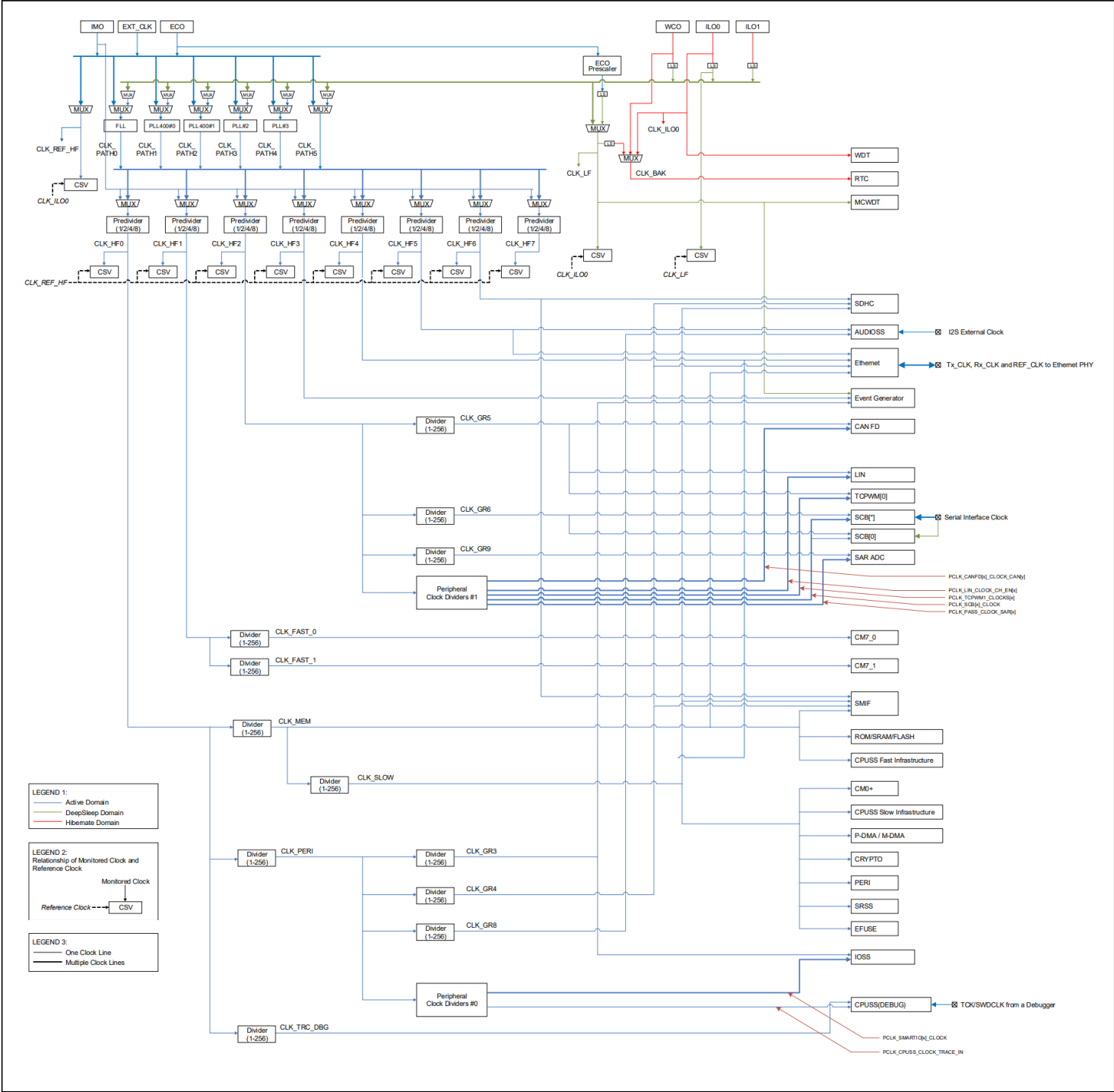


图 7-1 CYT3BB/4BB 时钟图

8 CYT3BB/4BB CPU 启动序列

启动顺序描述如下步骤：

1. 系统复位 (@0x0000 0000)
2. CM0+ 执行 ROM 启动 (@0x0000 0004)
 - i. 应用调整值
 - ii. 应用调试访问端口 (DAP) 访问限制以及的系统保护来自 eFuse 和监管闪存
 - iii. 验证闪存启动（仅在安全生命周期阶段）并将控制权转移给它
3. CM0+ 执行闪存启动（来自监管闪存 @0x1700 2000）
 - i. 调试引脚根据 SWD/JTAG 规范配置^[20]
 - ii. 将 CM0+ 矢量偏移寄存器（Arm®系统空间的 CM0_VTOR 部分）设置为闪存的开头 (@0x1000 0000)
 - iii. CM0+ 分支到其复位处理程序
4. CM0+ 开始执行应用程序
 - i. 将 CM0+ 向量表移至 SRAM（更新 CM0+ 向量表基址）
 - ii. 为 CM7_0 (CLK_HF1) 和 CM7_1 (CLK_HF1) 设置时钟
 - iii. 设置 CM7_0 (CM7_0_VECTOR_TABLE_BASE @0x4020 0200) 和 CM7_1 (CM7_1_VECTOR_TABLE_BASE @0x4020 0600) 向量表到各自的位置，也在中闪存提到（在链接器定义文件中指定）
 - iv. 为 CPU 核心 CM7_0 和 CM7_1 启用电源
 - v. 禁用 CPU_WAIT 以允许从调试器 vi 访问。从复位释放 CM7_0 和/或 CM7_1
 - vii. 继续执行 CM0+ 用户应用程序
5. CM7_0 和/或 CM7_1 直接从代码闪存或 SRAM 执行
 - i. CM7_0/CM7_1 分支到其复位处理程序
 - ii. 继续执行用户应用程序

注：

20. SWD/JTAG 引脚的端口配置将从默认的 GPIO 模式更改，以支持启动过程后的调试，参考表 11-1 用于引脚分配。

9 引脚分配

注释：对于所有 TEQFP 封装，热焊垫需要连接到 VSSD。

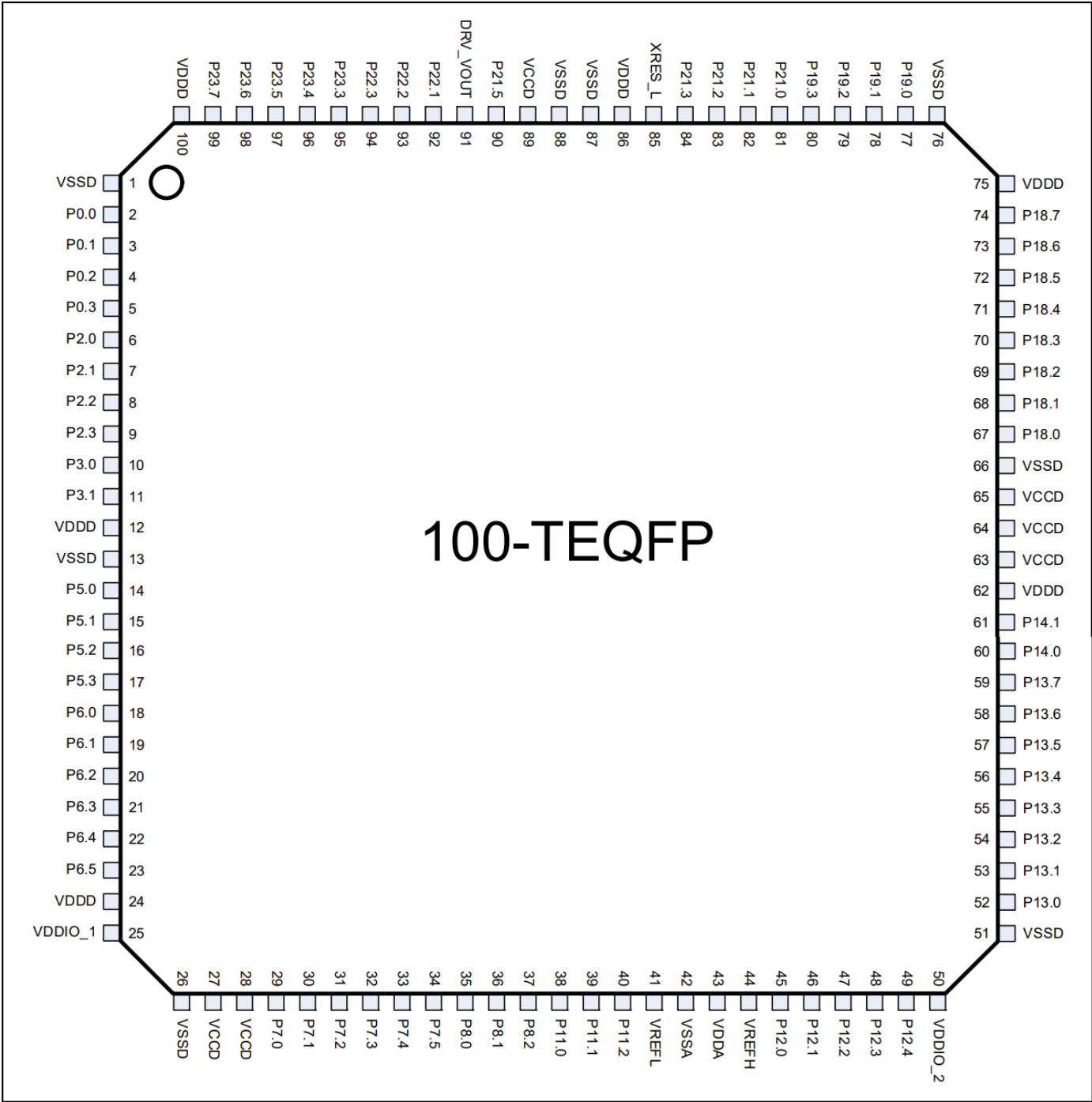


图9-1 100-TEQFP 引脚分配

引脚分配

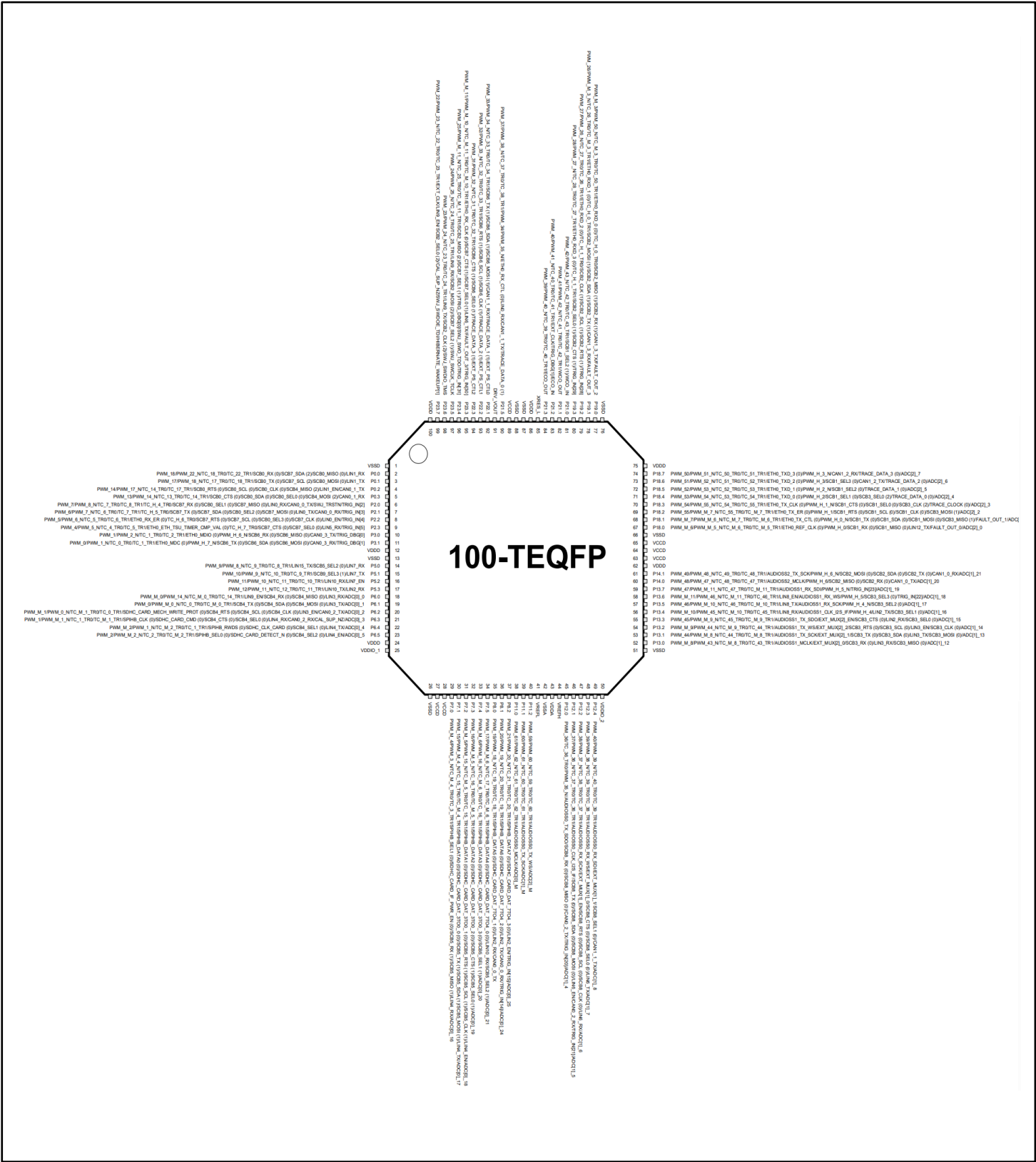


图 9-2 100-TEQFP 引脚分配及备用功能

引脚分配

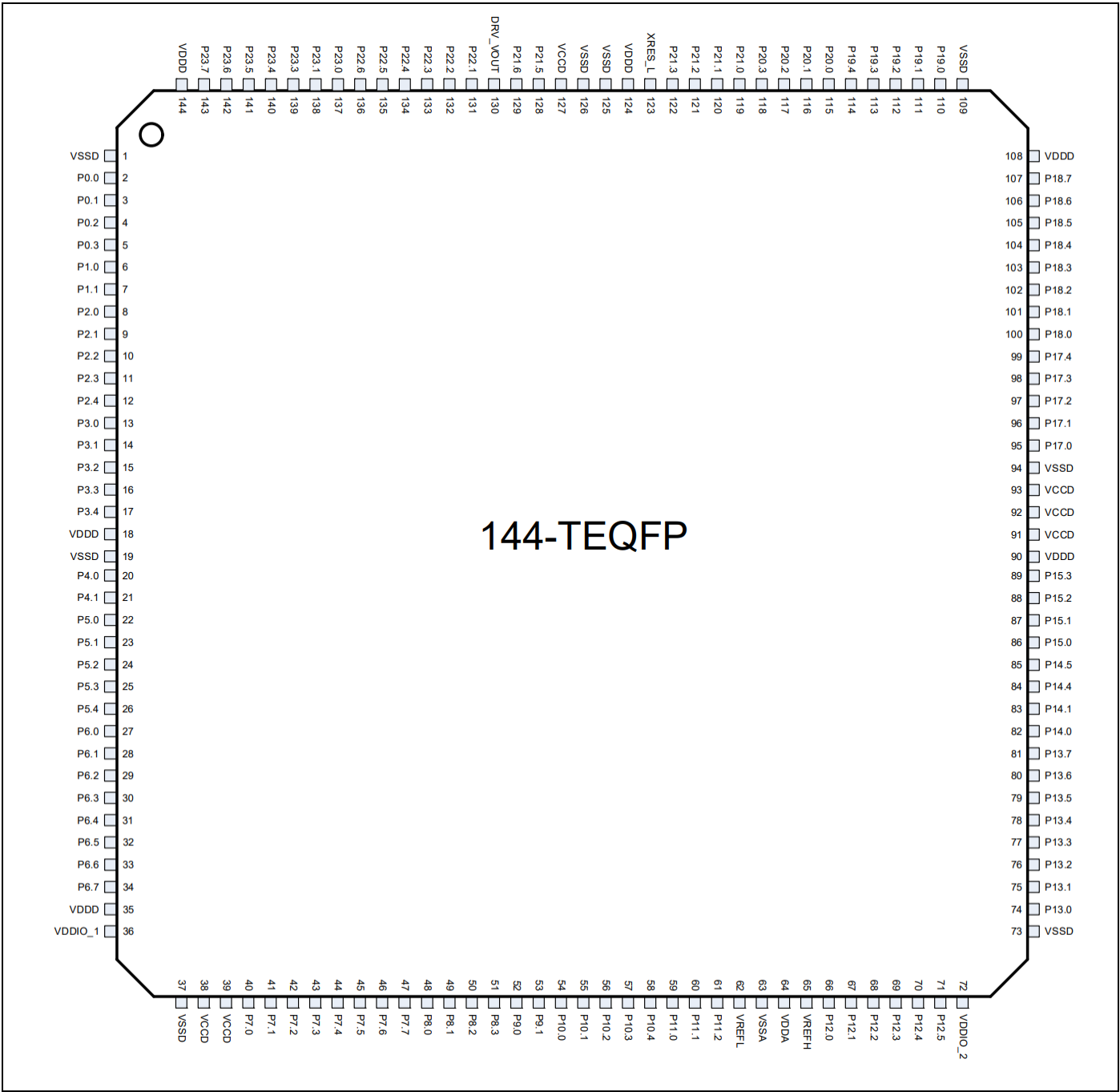


图9-3 144-TEQFP 引脚分配

引脚分配

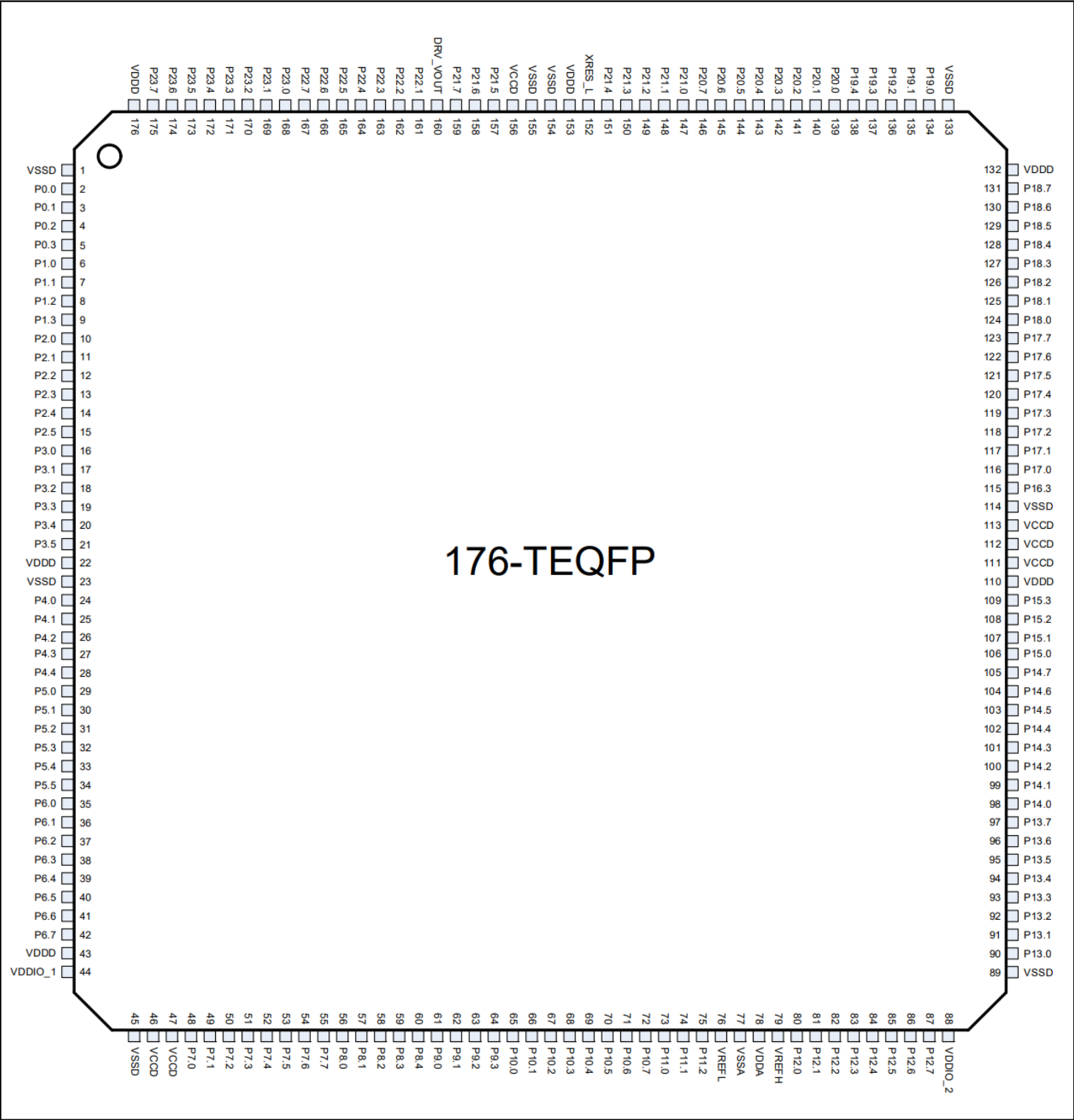


图 9-5 176-TEQFP 引脚分配

引脚分配

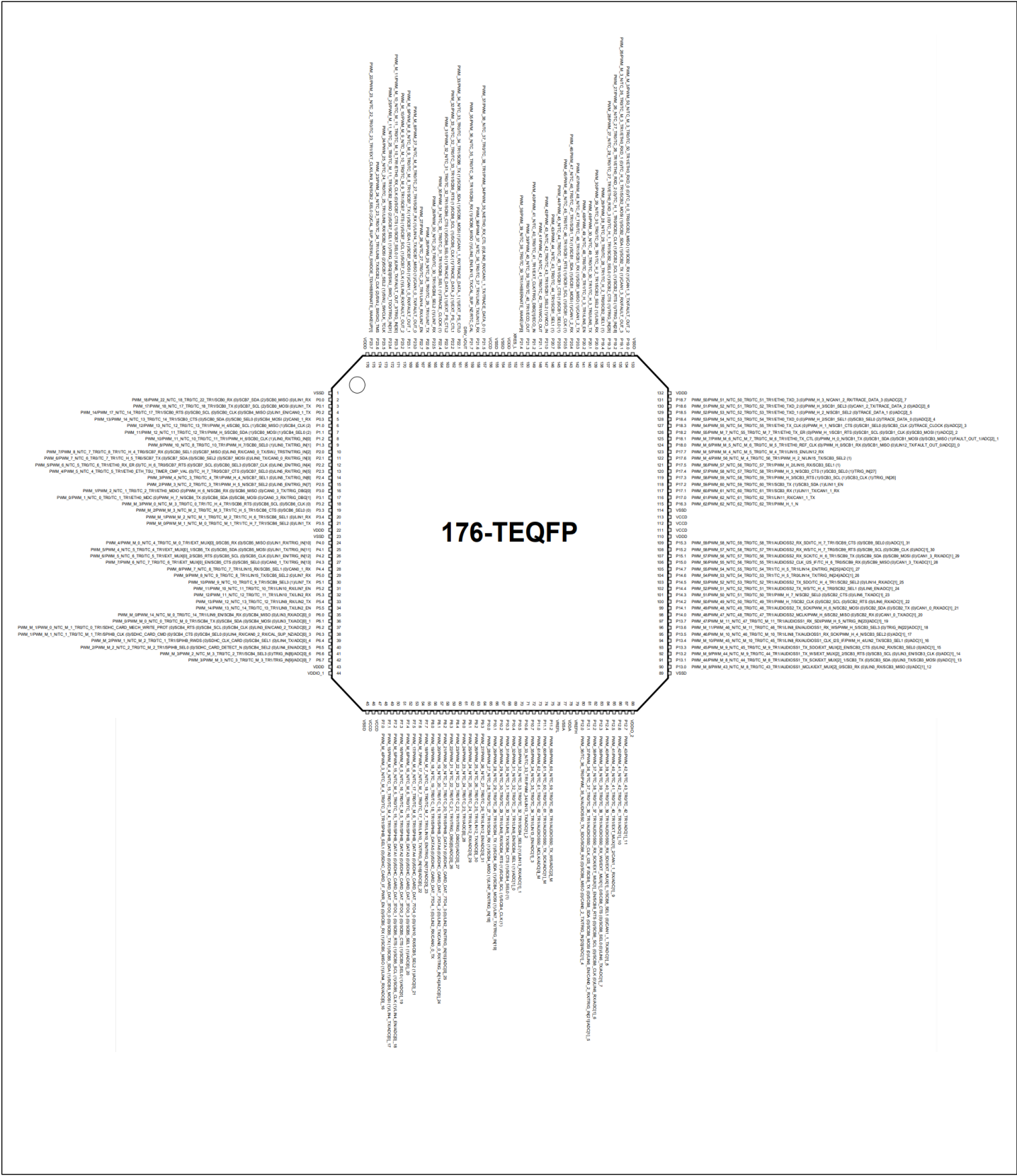


图 9-6 176-TEQFP 引脚分配及备用功能

引脚分配

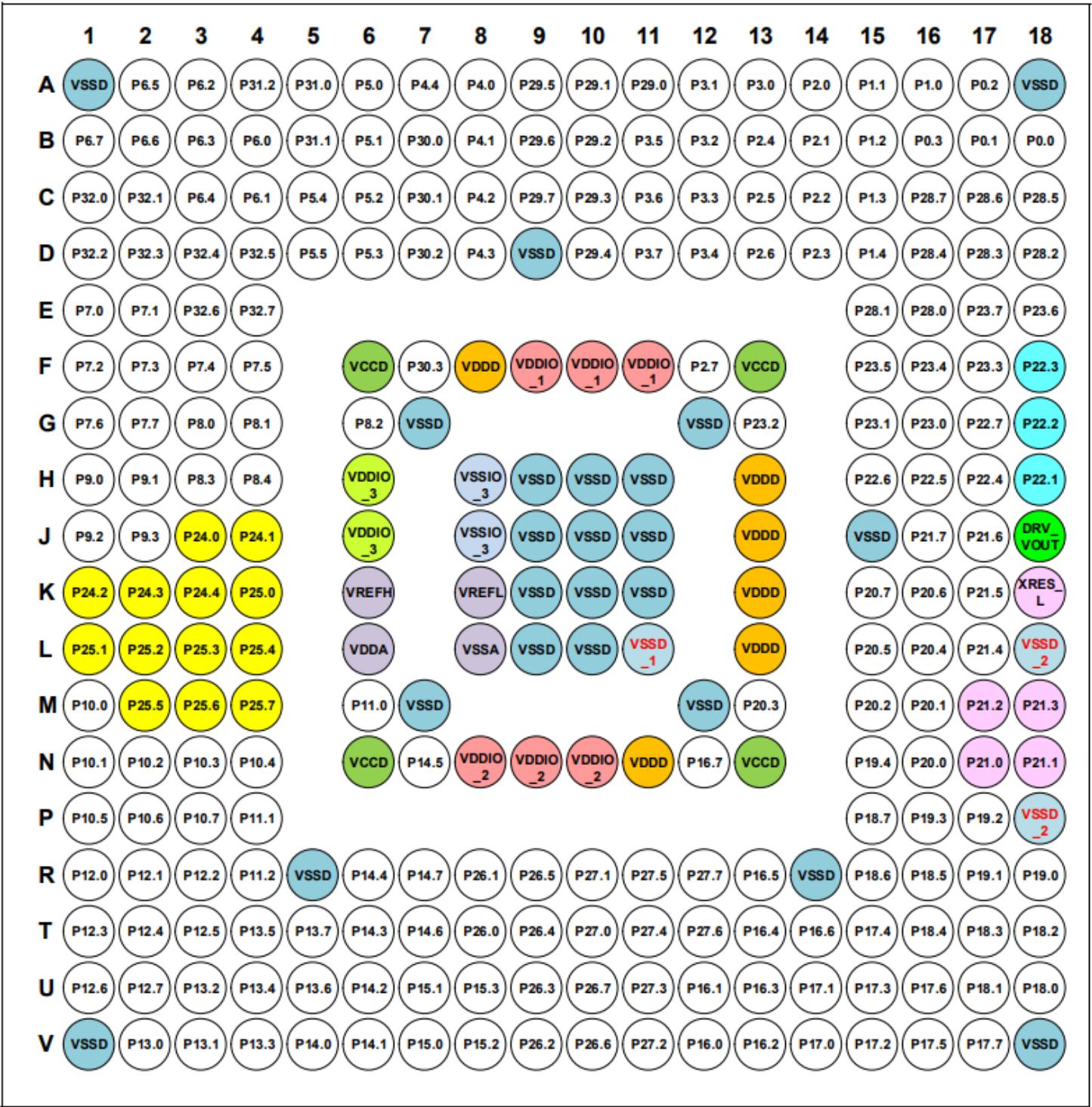


图 9-7 272-BGA 球图



高速 I/O 矩阵连接

10 高速 I/O 矩阵连接

表 10-1 HSIOM 连接基准

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7



11 封装引脚列表和备用功能

大多数引脚具有复用功能，如 表 11-1 所示。

Port 11 具有以下附加功能，

- 当 $V_{DDIO} < V_{DDA}$ 时，能够将全电平模拟信号传送至 SAR，而不会削波至 V_{DDIO}
- 能够同时捕获所有三个具有最高优先级的 ADC 信号 (ADC[0:2]_M)
- 噪音更低，适用于最灵敏的传感器

表 11-1 深度睡眠(DS) 模式、模拟、智能 I/O 下的引脚选择器和备用引脚功能^[24, 25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P0.0	B18	2	2	2	GPIO_ENH			SCB0_MISO (0)		
P0.1	B17	3	3	3	GPIO_ENH			SCB0_MOSI (0)		
P0.2	A17	4	4	4	GPIO_ENH	SCB0_SCL (0)		SCB0_CLK (0)		
P0.3	B16	5	5	5	GPIO_ENH	SCB0_SDA (0)		SCB0_SEL0 (0)		
P1.0	A16	6	6	NA	GPIO_STD	SCB0_SCL (1)		SCB0_MISO (1)		
P1.1	A15	7	7	NA	GPIO_STD	SCB0_SDA (1)		SCB0_MOSI (1)		
P1.2	B15	8	NA	NA	GPIO_STD			SCB0_CLK (1)		
P1.3	C15	9	NA	NA	GPIO_STD			SCB0_SEL0 (1)		
P1.4	D15	NA	NA	NA	GPIO_STD					
P2.0	A14	10	8	6	GPIO_STD		SWJ_TRSTN	SCB0_SEL1 (0)		
P2.1	B14	11	9	7	GPIO_STD			SCB0_SEL2 (0)		
P2.2	C14	12	10	8	GPIO_STD			SCB0_SEL3 (0)		
P2.3	D14	13	11	9	GPIO_STD					
P2.4	B13	14	12	NA	GPIO_STD					
P2.5	C13	15	NA	NA	GPIO_STD					
P2.6	D13	NA	NA	NA	GPIO_STD					
P2.7	F12	NA	NA	NA	GPIO_STD					

注：

- 21.HCon 指的是高速 I/O 矩阵连接基准，如 表 10-1 。
- 22.深度睡眠排序（ DS #0、 DS #1、 DS #2）对选择任何备用功能没有任何影响； HSIOM 模块处理单独的替换功能属性。
- 23.所有在深度睡眠模式下可用的端口引脚功能在运行模式下也可用。
- 24.参考 表格 13-2 有关使用的引脚多路复用器缩写的更多信息。
- 25.对于任何标有标识符 (n) 的函数，交流时序仅在相应的组“n”内得到保证。



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P3.0	A13	16	13	10	GPIO_STD					
P3.1	A12	17	14	11	GPIO_STD					
P3.2	B12	18	15	NA	GPIO_STD					
P3.3	C12	19	16	NA	GPIO_STD					
P3.4	D12	20	17	NA	GPIO_STD					
P3.5	B11	21	NA	NA	GPIO_STD					
P3.6	C11	NA	NA	NA	GPIO_STD					
P3.7	D11	NA	NA	NA	GPIO_STD					
P4.0	A8	24	20	NA	GPIO_STD					
P4.1	B8	25	21	NA	GPIO_STD					
P4.2	C8	26	NA	NA	GPIO_STD					
P4.3	D8	27	NA	NA	GPIO_STD					
P4.4	A7	28	NA	NA	GPIO_STD					
P5.0	A6	29	22	14	GPIO_STD					
P5.1	B6	30	23	15	GPIO_STD					
P5.2	C6	31	24	16	GPIO_STD					
P5.3	D6	32	25	17	GPIO_STD					
P5.4	C5	33	26	NA	GPIO_STD					
P5.5	D5	34	NA	NA	GPIO_STD					
P6.0	B4	35	27	18	GPIO_STD				ADC[0]_0	
P6.1	C4	36	28	19	GPIO_STD				ADC[0]_1	
P6.2	A3	37	29	20	GPIO_STD				ADC[0]_2	
P6.3	B3	38	30	21	GPIO_STD				ADC[0]_3	
P6.4	C3	39	31	22	GPIO_STD				ADC[0]_4	
P6.5	A2	40	32	23	GPIO_STD				ADC[0]_5	
P6.6	B2	41	33	NA	GPIO_STD				ADC[0]_6	
P6.7	B1	42	34	NA	GPIO_STD				ADC[0]_7	
P7.0	E1	48	40	29	GPIO_STD				ADC[0]_16	
P7.1	E2	49	41	30	GPIO_STD				ADC[0]_17	
P7.2	F1	50	42	31	GPIO_STD				ADC[0]_18	
P7.3	F2	51	43	32	GPIO_STD				ADC[0]_19	



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P7.4	F3	52	44	33	GPIO_STD				ADC[0]_20	
P7.5	F4	53	45	34	GPIO_STD				ADC[0]_21	
P7.6	G1	54	46	NA	GPIO_STD				ADC[0]_22	
P7.7	G2	55	47	NA	GPIO_STD				ADC[0]_23	
P8.0	G3	56	48	35	GPIO_STD					
P8.1	G4	57	49	36	GPIO_STD				ADC[0]_24	
P8.2	G6	58	50	37	GPIO_STD				ADC[0]_25	
P8.3	H3	59	51	NA	GPIO_STD				ADC[0]_26	
P8.4	H4	60	NA	NA	GPIO_STD				ADC[0]_27	
P9.0	H1	61	52	NA	GPIO_STD				ADC[0]_28	
P9.1	H2	62	53	NA	GPIO_STD				ADC[0]_29	
P9.2	J1	63	NA	NA	GPIO_STD				ADC[0]_30	
P9.3	J2	64	NA	NA	GPIO_STD				ADC[0]_31	
P10.0	M1	65	54	NA	GPIO_STD					
P10.1	N1	66	55	NA	GPIO_STD					
P10.2	N2	67	56	NA	GPIO_STD					
P10.3	N3	68	57	NA	GPIO_STD					
P10.4	N4	69	58	NA	GPIO_STD				ADC[1]_0	
P10.5	P1	70	NA	NA	GPIO_STD				ADC[1]_1	
P10.6	P2	71	NA	NA	GPIO_STD				ADC[1]_2	
P10.7	P3	72	NA	NA	GPIO_STD				ADC[1]_3	
P11.0	M6	73	59	38	GPIO_STD				ADC[0]_M	
P11.1	P4	74	60	39	GPIO_STD				ADC[1]_M	
P11.2	R4	75	61	40	GPIO_STD				ADC[2]_M	
P12.0	R1	80	66	45	GPIO_STD				ADC[1]_4	SMARTIO12_0
P12.1	R2	81	67	46	GPIO_STD				ADC[1]_5	SMARTIO12_1
P12.2	R3	82	68	47	GPIO_STD				ADC[1]_6	SMARTIO12_2
P12.3	T1	83	69	48	GPIO_STD				ADC[1]_7	SMARTIO12_3
P12.4	T2	84	70	49	GPIO_STD				ADC[1]_8	SMARTIO12_4
P12.5	T3	85	71	NA	GPIO_STD				ADC[1]_9	SMARTIO12_5
P12.6	U1	86	NA	NA	GPIO_STD				ADC[1]_10	SMARTIO12_6



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P12.7	U2	87	NA	NA	GPIO_STD				ADC[1]_11	SMARTIO12_7
P13.0	V2	90	74	52	GPIO_STD				ADC[1]_12	SMARTIO13_0
P13.1	V3	91	75	53	GPIO_STD				ADC[1]_13	SMARTIO13_1
P13.2	U3	92	76	54	GPIO_STD				ADC[1]_14	SMARTIO13_2
P13.3	V4	93	77	55	GPIO_STD				ADC[1]_15	SMARTIO13_3
P13.4	U4	94	78	56	GPIO_STD				ADC[1]_16	SMARTIO13_4
P13.5	T4	95	79	57	GPIO_STD				ADC[1]_17	SMARTIO13_5
P13.6	U5	96	80	58	GPIO_STD				ADC[1]_18	SMARTIO13_6
P13.7	T5	97	81	59	GPIO_STD				ADC[1]_19	SMARTIO13_7
P14.0	V5	98	82	60	GPIO_STD				ADC[1]_20	SMARTIO14_0
P14.1	V6	99	83	61	GPIO_STD				ADC[1]_21	SMARTIO14_1
P14.2	U6	100	NA	NA	GPIO_STD				ADC[1]_22	SMARTIO14_2
P14.3	T6	101	NA	NA	GPIO_STD				ADC[1]_23	SMARTIO14_3
P14.4	R6	102	84	NA	GPIO_STD				ADC[1]_24	SMARTIO14_4
P14.5	N7	103	85	NA	GPIO_STD				ADC[1]_25	SMARTIO14_5
P14.6	T7	104	NA	NA	GPIO_STD				ADC[1]_26	SMARTIO14_6
P14.7	R7	105	NA	NA	GPIO_STD				ADC[1]_27	SMARTIO14_7
P15.0	V7	106	86	NA	GPIO_STD				ADC[1]_28	SMARTIO15_0
P15.1	U7	107	87	NA	GPIO_STD				ADC[1]_29	SMARTIO15_1
P15.2	V8	108	88	NA	GPIO_STD				ADC[1]_30	SMARTIO15_2
P15.3	U8	109	89	NA	GPIO_STD				ADC[1]_31	SMARTIO15_3
P16.0	V12	NA	NA	NA	GPIO_STD					
P16.1	U12	NA	NA	NA	GPIO_STD					
P16.2	V13	NA	NA	NA	GPIO_STD					
P16.3	U13	115	NA	NA	GPIO_STD					
P16.4	T13	NA	NA	NA	GPIO_STD					
P16.5	R13	NA	NA	NA	GPIO_STD					
P16.6	T14	NA	NA	NA	GPIO_STD					
P16.7	N12	NA	NA	NA	GPIO_STD					
P17.0	V14	116	95	NA	GPIO_STD					SMARTIO17_0
P17.1	U14	117	96	NA	GPIO_STD					SMARTIO17_1



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P17.2	V15	118	97	NA	GPIO_STD					SMARTIO17_2
P17.3	U15	119	98	NA	GPIO_STD					SMARTIO17_3
P17.4	T15	120	99	NA	GPIO_STD					SMARTIO17_4
P17.5	V16	121	NA	NA	GPIO_STD					SMARTIO17_5
P17.6	U16	122	NA	NA	GPIO_STD					SMARTIO17_6
P17.7	V17	123	NA	NA	GPIO_STD					SMARTIO17_7
P18.0	U18	124	100	67	GPIO_STD				ADC[2]_0	
P18.1	U17	125	101	68	GPIO_STD				ADC[2]_1	
P18.2	T18	126	102	69	GPIO_STD				ADC[2]_2	
P18.3	T17	127	103	70	GPIO_STD				ADC[2]_3	
P18.4	T16	128	104	71	GPIO_STD				ADC[2]_4	
P18.5	R16	129	105	72	GPIO_STD				ADC[2]_5	
P18.6	R15	130	106	73	GPIO_STD				ADC[2]_6	
P18.7	P15	131	107	74	GPIO_STD				ADC[2]_7	
P19.0	R18	134	110	77	GPIO_STD					
P19.1	R17	135	111	78	GPIO_STD					
P19.2	P17	136	112	79	GPIO_STD					
P19.3	P16	137	113	80	GPIO_STD					
P19.4	N15	138	114	NA	GPIO_STD					
P20.0	N16	139	115	NA	GPIO_STD					
P20.1	M16	140	116	NA	GPIO_STD					
P20.2	M15	141	117	NA	GPIO_STD					
P20.3	M13	142	118	NA	GPIO_STD					
P20.4	L16	143	NA	NA	GPIO_STD					
P20.5	L15	144	NA	NA	GPIO_STD					
P20.6	K16	145	NA	NA	GPIO_STD					
P20.7	K15	146	NA	NA	GPIO_STD					
P21.0	N17	147	119	81	GPIO_STD				WCO_IN ^[26]	
P21.1	N18	148	120	82	GPIO_STD				WCO_OUT ^[26]	
P21.2	M17	149	121	83	GPIO_STD				ECO_IN ^[26]	
P21.3	M18	150	122	84	GPIO_STD				ECO_OUT ^[26]	



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P21.4 ^[27]	L17	151	NA	NA	GPIO_STD				HIBERNATE_WAKEUP[0]	
P21.5	K17	157	128	90	GPIO_STD					
P21.6	J17	158	129	NA	GPIO_STD					
P21.7	J16	159	NA	NA	GPIO_STD		RTC_CAL			
P22.1	H18	161	131	92	GPIO_STD				EXT_PS_CTL0	
P22.2	G18	162	132	93	GPIO_STD				EXT_PS_CTL1	
P22.3	F18	163	133	94	GPIO_STD				EXT_PS_CTL2	
P22.4	H17	164	134	NA	GPIO_STD					
P22.5	H16	165	135	NA	GPIO_STD					
P22.6	H15	166	136	NA	GPIO_STD					
P22.7	G17	167	NA	NA	GPIO_STD					
P23.0	G16	168	137	NA	GPIO_STD					
P23.1	G15	169	138	NA	GPIO_STD					
P23.2	G13	170	NA	NA	GPIO_STD					
P23.3	F17	171	139	95	GPIO_STD					
P23.4	F16	172	140	96	GPIO_STD		SWJ_SWO_TDO			
P23.5	F15	173	141	97	GPIO_STD		SWJ_SWCLK_TCLK			
P23.6	E18	174	142	98	GPIO_STD		SWJ_SWDIO_TMS			
P23.7	E17	175	143	99	GPIO_STD		SWJ_SWDOE_TDI		HIBERNATE_WAKEUP[1]	
P24.0	J3	NA	NA	NA	HSIO_STD					
P24.1	J4	NA	NA	NA	HSIO_STD					
P24.2	K1	NA	NA	NA	HSIO_STD					
P24.3	K2	NA	NA	NA	HSIO_STD					
P24.4	K3	NA	NA	NA	HSIO_STD					
P25.0	K4	NA	NA	NA	HSIO_STD					
P25.1	L1	NA	NA	NA	HSIO_STD					
P25.2	L2	NA	NA	NA	HSIO_STD					
P25.3	L3	NA	NA	NA	HSIO_STD					

注:

26. 如果振荡器是启用的, 则支持振荡器函数 (WCO或ECO) 的 I/O 引脚必须配置为高阻。

27. 的当V_{DD} 电源低于 POR 阈值时, 此 I/O 的接地泄漏会增加。



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P25.4	L4	NA	NA	NA	HSIO_STD					
P25.5	M2	NA	NA	NA	HSIO_STD					
P25.6	M3	NA	NA	NA	HSIO_STD					
P25.7	M4	NA	NA	NA	HSIO_STD					
P26.0	T8	NA	NA	NA	GPIO_STD					
P26.1	R8	NA	NA	NA	GPIO_STD					
P26.2	V9	NA	NA	NA	GPIO_STD					
P26.3	U9	NA	NA	NA	GPIO_STD					
P26.4	T9	NA	NA	NA	GPIO_STD					
P26.5	R9	NA	NA	NA	GPIO_STD					
P26.6	V10	NA	NA	NA	GPIO_STD					
P26.7	U10	NA	NA	NA	GPIO_STD					
P27.0	T10	NA	NA	NA	GPIO_STD					
P27.1	R10	NA	NA	NA	GPIO_STD					
P27.2	V11	NA	NA	NA	GPIO_STD					
P27.3	U11	NA	NA	NA	GPIO_STD					
P27.4	T11	NA	NA	NA	GPIO_STD					
P27.5	R11	NA	NA	NA	GPIO_STD					
P27.6	T12	NA	NA	NA	GPIO_STD					
P27.7	R12	NA	NA	NA	GPIO_STD					
P28.0	E16	NA	NA	NA	GPIO_STD					
P28.1	E15	NA	NA	NA	GPIO_STD					
P28.2	D18	NA	NA	NA	GPIO_STD					
P28.3	D17	NA	NA	NA	GPIO_STD					
P28.4	D16	NA	NA	NA	GPIO_STD					
P28.5	C18	NA	NA	NA	GPIO_STD					
P28.6	C17	NA	NA	NA	GPIO_STD					
P28.7	C16	NA	NA	NA	GPIO_STD					
P29.0	A11	NA	NA	NA	GPIO_STD					
P29.1	A10	NA	NA	NA	GPIO_STD					
P29.2	B10	NA	NA	NA	GPIO_STD					



表 11-1 深度睡眠 (DS) 模式下的引脚选择器和备用引脚功能、模拟、智能 I/O (续) [24、25]

Name	Package				I/O type	DeepSleep mapping			Analog	SMART I/O
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	HCon#0 ^[21]	HCon#14	HCon#29	HCon#30		
	Pin	Pin	Pin	Pin		DS #0 ^[22, 23]	DS #1	DS #2		
P29.3	C10	NA	NA	NA	GPIO_STD					
P29.4	D10	NA	NA	NA	GPIO_STD					
P29.5	A9	NA	NA	NA	GPIO_STD					
P29.6	B9	NA	NA	NA	GPIO_STD					
P29.7	C9	NA	NA	NA	GPIO_STD					
P30.0	B7	NA	NA	NA	GPIO_STD					
P30.1	C7	NA	NA	NA	GPIO_STD					
P30.2	D7	NA	NA	NA	GPIO_STD					
P30.3	F7	NA	NA	NA	GPIO_STD					
P31.0	A5	NA	NA	NA	GPIO_STD					
P31.1	B5	NA	NA	NA	GPIO_STD					
P31.2	A4	NA	NA	NA	GPIO_STD					
P32.0	C1	NA	NA	NA	GPIO_STD				ADC[0]_8	
P32.1	C2	NA	NA	NA	GPIO_STD				ADC[0]_9	
P32.2	D1	NA	NA	NA	GPIO_STD				ADC[0]_10	
P32.3	D2	NA	NA	NA	GPIO_STD				ADC[0]_11	
P32.4	D3	NA	NA	NA	GPIO_STD				ADC[0]_12	
P32.5	D4	NA	NA	NA	GPIO_STD				ADC[0]_13	
P32.6	E3	NA	NA	NA	GPIO_STD				ADC[0]_14	
P32.7	E4	NA	NA	NA	GPIO_STD				ADC[0]_15	
XRES_L	K18	152	123	85						
DRV_VOUT	J18	160	130	91						



电源引脚分配

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表 12-1 电源引脚分配

Power pin name	Package				Remarks
	272-BGA	176-TEQFP	144-TEQFP	100-TEQFP	
VDDD	F8, H13, J13, K13, L13, N11	22, 43, 110, 132, 153, 176	18, 35, 90, 108, 124, 144	12, 24, 62, 75, 86, 100	Main digital supply
VSSD	A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, M7, M12, R5, R14, V1, V18, L9, L10	1, 23, 45, 89, 114, 133, 154, 155	1, 19, 37, 73, 94, 109, 125, 126	1, 13, 26, 51, 66, 76, 87, 88	Main digital ground
VSSD_1	L11	NA	NA	NA	Digital ground
VSSD_2	L18, P18	NA	NA	NA	Noise guard for ECO inputs
VDDIO_1	F9, F10, F11	44	36	25	I/O supply (except analog I/Os on VDDA)
VDDIO_2	N8, N9, N10	88	72	50	I/O supply (except analog I/Os on VDDA)
VDDIO_3	H6, J6	NA	NA	NA	I/O supply for high speed domain#0 (HSIO_STD), P24, P25
VSSIO_3	H8, J8	NA	NA	NA	HSIO ground
VCCD ^[28]	F6, F13, N6, N13	46, 47, 111, 112, 113, 156	38, 39, 91, 92, 93, 127	27, 28, 63, 64, 65, 89	Main regulated supply. Driven by LDO regulator (either internal LDO or external LDO/PMIC)
VREFH	K6	79	65	44	High-reference voltage for SAR ADCs
VREFL	K8	76	62	41	Low-reference voltage for SAR ADCs
VDDA	L6	78	64	43	Main analog supply for SAR ADCs
VSSA	L8	77	63	42	Main analog ground

注：
28. V_{CCD} 引脚必须连接在一起，以确保低阻抗连接。（参见图 26-2）



备用功能引脚分配

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表 13-1 运行模式下的备用引脚功能^[23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P0.0	PWM0_18	PWM0_22_N	TC0_18_TR0	TC0_22_TR1		SCB0_RX (0)	SCB7_SDA (2)		LIN1_RX							
P0.1	PWM0_17	PWM0_18_N	TC0_17_TR0	TC0_18_TR1		SCB0_TX (0)	SCB7_SCL (2)		LIN1_TX							
P0.2	PWM0_14	PWM0_17_N	TC0_14_TR0	TC0_17_TR1		SCB0_RTS (0)		SCB4_MISO (2)	LIN1_EN	CAN0_1_TX						
P0.3	PWM0_13	PWM0_14_N	TC0_13_TR0	TC0_14_TR1		SCB0_CTS (0)		SCB4_MOSI (2)		CAN0_1_RX						
P1.0	PWM0_12	PWM0_13_N	TC0_12_TR0	TC0_13_TR1	PWM0_H_4			SCB4_CLK (2)								
P1.1	PWM0_11	PWM0_12_N	TC0_11_TR0	TC0_12_TR1	PWM0_H_5			SCB4_SEL0 (2)								
P1.2	PWM0_10	PWM0_11_N	TC0_10_TR0	TC0_11_TR1	PWM0_H_6				LIN0_RX						TRIG_IN[0]	
P1.3	PWM0_8	PWM0_10_N	TC0_8_TR0	TC0_10_TR1	PWM0_H_7				LIN0_TX						TRIG_IN[1]	
P1.4											LIN8_RX					
P2.0	PWM0_7	PWM0_8_N	TC0_7_TR0	TC0_8_TR1	TC0_H_4_TR0	SCB7_RX (0)		SCB7_MISO (0)	LIN0_RX	CAN0_0_TX					TRIG_IN[2]	
P2.1	PWM0_6	PWM0_7_N	TC0_6_TR0	TC0_7_TR1	TC0_H_5_TR0	SCB7_TX (0)	SCB7_SDA (0)	SCB7_MOSI (0)	LIN0_TX	CAN0_0_RX					TRIG_IN[3]	
P2.2	PWM0_5	PWM0_6_N	TC0_5_TR0	TC0_6_TR1	TC0_H_6_TR0	SCB7_RTS (0)	SCB7_SCL (0)	SCB7_CLK (0)	LIN0_EN				ETH0_RX_ER (0)		TRIG_IN[4]	
P2.3	PWM0_4	PWM0_5_N	TC0_4_TR0	TC0_5_TR1	TC0_H_7_TR0	SCB7_CTS (0)		SCB7_SEL0 (0)	LIN5_RX				ETH0_ETH_TSU - TIMER_CMP_VAL (0)		TRIG_IN[5]	
P2.4	PWM0_3	PWM0_4_N	TC0_3_TR0	TC0_4_TR1	PWM0_H_4_N			SCB7_SEL1 (0)	LIN5_TX						TRIG_IN[6]	
P2.5	PWM0_2	PWM0_3_N	TC0_2_TR0	TC0_3_TR1	PWM0_H_5_N			SCB7_SEL2 (0)	LIN5_EN						TRIG_IN[7]	
P2.6																
P2.7									LIN11_RX							
P3.0	PWM0_1	PWM0_2_N	TC0_1_TR0	TC0_2_TR1	PWM0_H_6_N	SCB6_RX (0)		SCB6_MISO (0)		CAN0_3_TX			ETH0_MDIO (0)			TRIG_DBG[0]
P3.1	PWM0_0	PWM0_1_N	TC0_0_TR0	TC0_1_TR1	PWM0_H_7_N	SCB6_TX (0)	SCB6_SDA (0)	SCB6_MOSI (0)		CAN0_3_RX			ETH0_MDC (0)			TRIG_DBG[1]
P3.2	PWM0_M_3	PWM0_0_N	TC0_M_3_TR0	TC0_0_TR1	TC0_H_4_TR1	SCB6_RTS (0)	SCB6_SCL (0)	SCB6_CLK (0)								
P3.3	PWM0_M_2	PWM0_M_3_N	TC0_M_2_TR0	TC0_M_3_TR1	TC0_H_5_TR1	SCB6_CTS (0)		SCB6_SEL0 (0)								
P3.4	PWM0_M_1	PWM0_M_2_N	TC0_M_1_TR0	TC0_M_2_TR1	TC0_H_6_TR1			SCB6_SEL1 (0)	LIN1_RX							
P3.5	PWM0_M_0	PWM0_M_1_N	TC0_M_0_TR0	TC0_M_1_TR1	TC0_H_7_TR1			SCB6_SEL2 (0)	LIN1_TX							

注：
29. 高速 I/O 矩阵连接 (HCon) 基准见[表 10-1](#)。
30. 运行模式顺序 (ACT #0、ACT #1 等) 对配置备用功能没有任何影响；HSIOM 模块处理替换功能分配。
31. 参考[表格 13-2](#) 有关使用的引脚多路复用器缩写的更多信息。
32. 对于任何标有标识符 (n) 的函数，交流时序仅在相应的组“n”内得到保证。



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P3.6								SCB8_SEL2 (0)	LIN11_TX	CAN1_2_TX						
P3.7									LIN11_EN	CAN1_2_RX						
P4.0	PWM0_4	PWM0_M_0_N	TC0_4_TR0	TC0_M_0_TR1	EXT_MUX[0]_0	SCB5_RX (0)		SCB5_MISO (0)	LIN1_RX						TRIG_IN[10]	
P4.1	PWM0_5	PWM0_4_N	TC0_5_TR0	TC0_4_TR1	EXT_MUX[0]_1	SCB5_TX (0)	SCB5_SDA (0)	SCB5_MOSI (0)	LIN1_TX						TRIG_IN[11]	
P4.2	PWM0_6	PWM0_5_N	TC0_6_TR0	TC0_5_TR1	EXT_MUX[0]_2	SCB5_RTS (0)	SCB5_SCL (0)	SCB5_CLK (0)	LIN1_EN						TRIG_IN[12]	
P4.3	PWM0_7	PWM0_6_N	TC0_7_TR0	TC0_6_TR1	EXT_MUX[0]_EN	SCB5_CTS (0)		SCB5_SEL0 (0)		CAN0_1_TX					TRIG_IN[13]	
P4.4	PWM0_8	PWM0_7_N	TC0_8_TR0	TC0_7_TR1			LIN15_RX	SCB5_SEL1 (0)		CAN0_1_RX						
P5.0	PWM0_9	PWM0_8_N	TC0_9_TR0	TC0_8_TR1			LIN15_TX	SCB5_SEL2 (0)	LIN7_RX							
P5.1	PWM0_10	PWM0_9_N	TC0_10_TR0	TC0_9_TR1				SCB9_SEL3 (1)	LIN7_TX							
P5.2	PWM0_11	PWM0_10_N	TC0_11_TR0	TC0_10_TR1			LIN10_RX		LIN7_EN							
P5.3	PWM0_12	PWM0_11_N	TC0_12_TR0	TC0_11_TR1			LIN10_TX		LIN2_RX							
P5.4	PWM0_13	PWM0_12_N	TC0_13_TR0	TC0_12_TR1					LIN2_TX			LIN9_RX				
P5.5	PWM0_14	PWM0_13_N	TC0_14_TR0	TC0_13_TR1					LIN2_EN			LIN9_TX				
P6.0	PWM0_M_0	PWM0_14_N	TC0_M_0_TR0	TC0_14_TR1		SCB4_RX (0)		SCB4_MISO (0)	LIN3_RX			LIN9_EN				
P6.1	PWM0_0	PWM0_M_0_N	TC0_0_TR0	TC0_M_0_TR1		SCB4_TX (0)	SCB4_SDA (0)	SCB4_MOSI (0)	LIN3_TX							
P6.2	PWM0_M_1	PWM0_0_N	TC0_M_1_TR0	TC0_0_TR1		SCB4_RTS (0)	SCB4_SCL (0)	SCB4_CLK (0)	LIN3_EN	CAN0_2_TX				SDHC_CARD_- MECH_WRITE_P ROT (0)		
P6.3	PWM0_1	PWM0_M_1_N	TC0_1_TR0	TC0_M_1_TR1		SCB4_CTS (0)		SCB4_SEL0 (0)	LIN4_RX	CAN0_2_RX		SPIHB_CLK (0)		SDHC_- CARD_CMD (0)		CAL_SUP_NZ
P6.4	PWM0_M_2	PWM0_1_N	TC0_M_2_TR0	TC0_1_TR1				SCB4_SEL1 (0)	LIN4_TX			SPIHB_RWD S (0)		SDHC_- CLK_CARD (0)		
P6.5	PWM0_2	PWM0_M_2_N	TC0_2_TR0	TC0_M_2_TR1				SCB4_SEL2 (0)	LIN4_EN			SPIHB_SELO (0)		SDHC_CARD_- DETECT_N (0)		
P6.6	PWM0_M_3	PWM0_2_N	TC0_M_3_TR0	TC0_2_TR1				SCB4_SEL3 (0)							TRIG_IN[8]	
P6.7	PWM0_3	PWM0_M_3_N	TC0_3_TR0	TC0_M_3_TR1											TRIG_IN[9]	
P7.0	PWM0_M_4	PWM0_3_N	TC0_M_4_TR0	TC0_3_TR1		SCB5_RX (1)		SCB5_MISO (1)	LIN4_RX			SPIHB_SEL1 (0)		SDHC_- CARD_IF_P- WR_EN (0)		
P7.1	PWM0_15	PWM0_M_4_N	TC0_15_TR0	TC0_M_4_TR1		SCB5_TX (1)	SCB5_SDA (1)	SCB5_MOSI (1)	LIN4_TX			SPIHB_- DATA0 (0)		SDHC_CARD_- DAT_3TO0_0 (0)		
P7.2	PWM0_M_5	PWM0_15_N	TC0_M_5_TR0	TC0_15_TR1		SCB5_RTS (1)	SCB5_SCL (1)	SCB5_CLK (1)	LIN4_EN			SPIHB_- DATA1 (0)		SDHC_CARD_- DAT_3TO0_1 (0)		
P7.3	PWM0_16	PWM0_M_5_N	TC0_16_TR0	TC0_M_5_TR1		SCB5_CTS (1)		SCB5_SEL0 (1)				SPIHB_- DATA2 (0)		SDHC_CARD_- DAT_3TO0_2 (0)		
P7.4	PWM0_M_6	PWM0_16_N	TC0_M_6_TR0	TC0_16_TR1				SCB5_SEL1 (1)				SPIHB_- DATA3 (0)		SDHC_CARD_- DAT_3TO0_3 (0)		
P7.5	PWM0_17	PWM0_M_6_N	TC0_17_TR0	TC0_M_6_TR1			LIN10_RX	SCB5_SEL2 (1)				SPIHB_- DATA4 (0)		SDHC_CARD_- DAT_7TO4_0 (0)		
P7.6	PWM0_M_7	PWM0_17_N	TC0_M_7_TR0	TC0_17_TR1			LIN10_TX								TRIG_IN[16]	



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P7.7	PWM0_18	PWM0_M_7_N	TC0_18_TR0	TC0_M_7_TR1			LIN10_EN								TRIG_IN[17]	
P8.0	PWM0_19	PWM0_18_N	TC0_19_TR0	TC0_18_TR1					LIN2_RX	CAN0_0_TX		SPIHB - DATA5 (0)		SDHC_CARD - DAT_7TO4_1 (0)		
P8.1	PWM0_20	PWM0_19_N	TC0_20_TR0	TC0_19_TR1					LIN2_TX	CAN0_0_RX		SPIHB - DATA6 (0)		SDHC_CARD - DAT_7TO4_2 (0)	TRIG_IN[14]	
P8.2	PWM0_21	PWM0_20_N	TC0_21_TR0	TC0_20_TR1					LIN2_EN			SPIHB - DATA7 (0)		SDHC_CARD - DAT_7TO4_3 (0)	TRIG_IN[15]	
P8.3	PWM0_22	PWM0_21_N	TC0_22_TR0	TC0_21_TR1												TRIG_DBG[0]
P8.4	PWM0_23	PWM0_22_N	TC0_23_TR0	TC0_22_TR1												TRIG_DBG[1]
P9.0	PWM0_24	PWM0_23_N	TC0_24_TR0	TC0_23_TR1												
P9.1	PWM0_25	PWM0_24_N	TC0_25_TR0	TC0_24_TR1						LIN12_RX						
P9.2	PWM0_26	PWM0_25_N	TC0_26_TR0	TC0_25_TR1						LIN12_TX						
P9.3	PWM0_27	PWM0_26_N	TC0_27_TR0	TC0_26_TR1						LIN12_EN						
P10.0	PWM0_28	PWM0_27_N	TC0_28_TR0	TC0_27_TR1		SCB4_RX (1)		SCB4_MISO (1)	LIN7_RX						TRIG_IN[18]	
P10.1	PWM0_29	PWM0_28_N	TC0_29_TR0	TC0_28_TR1		SCB4_TX (1)	SCB4_SDA (1)	SCB4_MOSI (1)	LIN7_TX						TRIG_IN[19]	
P10.2	PWM0_30	PWM0_29_N	TC0_30_TR0	TC0_29_TR1		SCB4_RTS (1)	SCB4_SCL (1)	SCB4_CLK (1)			LIN8_RX					
P10.3	PWM0_31	PWM0_30_N	TC0_31_TR0	TC0_30_TR1		SCB4_CTS (1)		SCB4_SEL0 (1)			LIN8_TX					
P10.4	PWM0_32	PWM0_31_N	TC0_32_TR0	TC0_31_TR1				SCB4_SEL1 (1)			LIN8_EN					
P10.5	PWM0_33	PWM0_32_N	TC0_33_TR0	TC0_32_TR1				SCB4_SEL2 (1)		LIN13_RX						
P10.6		PWM0_33_N		TC0_33_TR1						LIN13_TX	PWM0_34					
P10.7	PWM0_35	PWM0_34_N	TC0_35_TR0	TC0_34_TR1						LIN13_EN						
P11.0	PWM0_61	PWM0_62_N	TC0_61_TR0	TC0_62_TR1										AUDIOSS0_MCLK		
P11.1	PWM0_60	PWM0_61_N	TC0_60_TR0	TC0_61_TR1										AUDIOSS0_TX_SCK		
P11.2	PWM0_59	PWM0_60_N	TC0_59_TR0	TC0_60_TR1										AUDIOSS0_TX_WS		
P12.0	PWM0_36		TC0_36_TR0			SCB8_RX (0)		SCB8_MISO (0)		CAN0_2_TX		PWM0_35_N		AUDIOSS0_TX_SDO	TRIG_IN[20]	
P12.1	PWM0_37	PWM0_36_N	TC0_37_TR0	TC0_36_TR1		SCB8_TX (0)	SCB8_SDA (0)	SCB8_MOSI (0)	LIN6_EN	CAN0_2_RX				AUDIOSS0_CLK_I2S_IF	TRIG_IN[21]	
P12.2	PWM0_38	PWM0_37_N	TC0_38_TR0	TC0_37_TR1	EXT_MUX[1]_EN	SCB8_RTS (0)	SCB8_SCL (0)	SCB8_CLK (0)	LIN6_RX					AUDIOSS0_RX_SCK		
P12.3	PWM0_39	PWM0_38_N	TC0_39_TR0	TC0_38_TR1	EXT_MUX[1]_0	SCB8_CTS (0)		SCB8_SEL0 (0)	LIN6_TX					AUDIOSS0_RX_WS		
P12.4	PWM0_40	PWM0_39_N	TC0_40_TR0	TC0_39_TR1	EXT_MUX[1]_1			SCB8_SEL1 (0)		CAN1_1_TX				AUDIOSS0_RX_SDI		
P12.5	PWM0_41	PWM0_40_N	TC0_41_TR0	TC0_40_TR1	EXT_MUX[1]_2					CAN1_1_RX						
P12.6	PWM0_42	PWM0_41_N	TC0_42_TR0	TC0_41_TR1												
P12.7	PWM0_43	PWM0_42_N	TC0_43_TR0	TC0_42_TR1												

表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P13.0	PWM0_M_8	PWM0_43_N	TC0_M_8_TR0	TC0_43_TR1	EXT_MUX[2]_0	SCB3_RX (0)			LIN3_RX	SCB3_MISO (0)				AUDIOSS1_MCLK		
P13.1	PWM0_44	PWM0_M_8_N	TC0_44_TR0	TC0_M_8_TR1	EXT_MUX[2]_1	SCB3_TX (0)	SCB3_SDA (0)		LIN3_TX	SCB3_MOSI (0)				AUDIOSS1_TX_SCK		
P13.2	PWM0_M_9	PWM0_44_N	TC0_M_9_TR0	TC0_44_TR1	EXT_MUX[2]_2	SCB3_RTS (0)	SCB3_SCL (0)		LIN3_EN	SCB3_CLK (0)				AUDIOSS1_TX_WS		
P13.3	PWM0_45	PWM0_M_9_N	TC0_45_TR0	TC0_M_9_TR1	EXT_MUX[2]_EN	SCB3_CTS (0)			LIN2_RX	SCB3_SEL0 (0)				AUDIOSS1_TX_SDO		
P13.4	PWM0_M_10	PWM0_45_N	TC0_M_10_TR0	TC0_45_TR1	PWM0_H_4				LIN2_TX	SCB3_SEL1 (0)	LIN8_RX			AUDIOSS1_CLK_I2S_IF		
P13.5	PWM0_46	PWM0_M_10_N	TC0_46_TR0	TC0_M_10_TR1	PWM0_H_4_N					SCB3_SEL2 (0)	LIN8_TX			AUDIOSS1_RX_SCK		
P13.6	PWM0_M_11	PWM0_46_N	TC0_M_11_TR0	TC0_46_TR1	PWM0_H_5					SCB3_SEL3 (0)	LIN8_EN			AUDIOSS1_RX_WS	TRIG_IN[22]	
P13.7	PWM0_47	PWM0_M_11_N	TC0_47_TR0	TC0_M_11_TR1	PWM0_H_5_N									AUDIOSS1_RX_SDI	TRIG_IN[23]	
P14.0	PWM0_48	PWM0_47_N	TC0_48_TR0	TC0_47_TR1	PWM0_H_6	SCB2_MISO (0)		SCB2_RX (0)		CAN1_0_TX				AUDIOSS2_MCLK		
P14.1	PWM0_49	PWM0_48_N	TC0_49_TR0	TC0_48_TR1	PWM0_H_6_N	SCB2_MOSI (0)	SCB2_SDA (0)	SCB2_TX (0)		CAN1_0_RX				AUDIOSS2_TX_SCK		
P14.2	PWM0_50	PWM0_49_N	TC0_50_TR0	TC0_49_TR1	PWM0_H_7	SCB2_CLK (0)	SCB2_SCL (0)	SCB2_RTS (0)	LIN6_RX							
P14.3	PWM0_51	PWM0_50_N	TC0_51_TR0	TC0_50_TR1	PWM0_H_7_N	SCB2_SEL0 (0)		SCB2_CTS (0)	LIN6_TX							
P14.4	PWM0_52	PWM0_51_N	TC0_52_TR0	TC0_51_TR1	TC0_H_4_TR0	SCB2_SEL1 (0)			LIN6_EN					AUDIOSS2_TX_WS		
P14.5	PWM0_53	PWM0_52_N	TC0_53_TR0	TC0_52_TR1	TC0_H_4_TR1	SCB2_SEL2 (0)	LIN14_RX							AUDIOSS2_TX_SDO		
P14.6	PWM0_54	PWM0_53_N	TC0_54_TR0	TC0_53_TR1	TC0_H_5_TR0		LIN14_TX								TRIG_IN[24]	
P14.7	PWM0_55	PWM0_54_N	TC0_55_TR0	TC0_54_TR1	TC0_H_5_TR1		LIN14_EN								TRIG_IN[25]	
P15.0	PWM0_56	PWM0_55_N	TC0_56_TR0	TC0_55_TR1	TC0_H_6_TR0	SCB9_RX (0)		SCB9_MISO (0)		CAN1_3_TX				AUDIOSS2_CLK_I2S_IF		
P15.1	PWM0_57	PWM0_56_N	TC0_57_TR0	TC0_56_TR1	TC0_H_6_TR1	SCB9_TX (0)	SCB9_SDA (0)	SCB9_MOSI (0)		CAN1_3_RX				AUDIOSS2_RX_SCK		
P15.2	PWM0_58	PWM0_57_N	TC0_58_TR0	TC0_57_TR1	TC0_H_7_TR0	SCB9_RTS (0)	SCB9_SCL (0)	SCB9_CLK (0)						AUDIOSS2_RX_WS		
P15.3	PWM0_59	PWM0_58_N	TC0_59_TR0	TC0_58_TR1	TC0_H_7_TR1	SCB9_CTS (0)		SCB9_SEL0 (0)						AUDIOSS2_RX_SDI		
P16.0	PWM0_60	PWM0_59_N	TC0_60_TR0	TC0_59_TR1	PWM0_H_0			SCB9_SEL1 (0)	LIN11_RX							
P16.1	PWM0_61	PWM0_60_N	TC0_61_TR0	TC0_60_TR1	PWM0_H_0_N			SCB9_SEL2 (0)	LIN11_TX							
P16.2	PWM0_62	PWM0_61_N	TC0_62_TR0	TC0_61_TR1	PWM0_H_1			SCB9_SEL3 (0)	LIN11_EN							
P16.3	PWM0_62	PWM0_62_N	TC0_62_TR0	TC0_62_TR1	PWM0_H_1_N											
P16.4																
P16.5																
P16.6																
P16.7																



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P17.0	PWM0_61	PWM0_62_N	TC0_61_TR0	TC0_62_TR1					LIN11_RX	CAN1_1_TX						
P17.1	PWM0_60	PWM0_61_N	TC0_60_TR0	TC0_61_TR1		SCB3_RX (1)			LIN11_TX	CAN1_1_RX						
P17.2	PWM0_59	PWM0_60_N	TC0_59_TR0	TC0_60_TR1		SCB3_TX (1)	SCB3_SDA (1)		LIN11_EN							
P17.3	PWM0_58	PWM0_59_N	TC0_58_TR0	TC0_59_TR1	PWM0_H_3	SCB3_RTS (1)	SCB3_SCL (1)			SCB3_CLK (1)					TRIG_IN[26]	
P17.4	PWM0_57	PWM0_58_N	TC0_57_TR0	TC0_58_TR1	PWM0_H_3_N	SCB3_CTS (1)				SCB3_SEL0 (1)					TRIG_IN[27]	
P17.5	PWM0_56	PWM0_57_N	TC0_56_TR0	TC0_57_TR1	PWM0_H_2		LIN15_RX			SCB3_SEL1 (1)						
P17.6	PWM0_M_4	PWM0_56_N	TC0_M_4_TR0	TC0_56_TR1	PWM0_H_2_N		LIN15_TX			SCB3_SEL2 (1)						
P17.7	PWM0_M_5	PWM0_M_4_N	TC0_M_5_TR0	TC0_M_4_TR1			LIN15_EN			LIN12_RX						
P18.0	PWM0_M_6	PWM0_M_5_N	TC0_M_6_TR0	TC0_M_5_TR1	PWM0_H_0	SCB1_RX (0)		SCB1_MISO (0)		LIN12_TX			ETH0_REF_CLK (0)			FAULT_OUT_0
P18.1	PWM0_M_7	PWM0_M_6_N	TC0_M_7_TR0	TC0_M_6_TR1	PWM0_H_0_N	SCB1_TX (0)	SCB1_SDA (0)	SCB1_MOSI (0)		SCB3_MISO (1)			ETH0_TX_CTL (0)			FAULT_OUT_1
P18.2	PWM0_55	PWM0_M_7_N	TC0_55_TR0	TC0_M_7_TR1	PWM0_H_1	SCB1_RTS (0)	SCB1_SCL (0)	SCB1_CLK (0)		SCB3_MOSI (1)			ETH0_TX_ER (0)			
P18.3	PWM0_54	PWM0_55_N	TC0_54_TR0	TC0_55_TR1	PWM0_H_1_N	SCB1_CTS (0)		SCB1_SEL0 (0)		SCB3_CLK (2)			ETH0_TX_CLK (0)			TRACE_CLOCK (0)
P18.4	PWM0_53	PWM0_54_N	TC0_53_TR0	TC0_54_TR1	PWM0_H_2			SCB1_SEL1 (0)		SCB3_SEL0 (2)			ETH0_TXD_0 (0)			TRACE_-DATA_0 (0)
P18.5	PWM0_52	PWM0_53_N	TC0_52_TR0	TC0_53_TR1	PWM0_H_2_N			SCB1_SEL2 (0)					ETH0_TXD_1 (0)			TRACE_-DATA_1 (0)
P18.6	PWM0_51	PWM0_52_N	TC0_51_TR0	TC0_52_TR1	PWM0_H_3			SCB1_SEL3 (0)		CAN1_2_TX			ETH0_TXD_2 (0)			TRACE_-DATA_2 (0)
P18.7	PWM0_50	PWM0_51_N	TC0_50_TR0	TC0_51_TR1	PWM0_H_3_N					CAN1_2_RX			ETH0_TXD_3 (0)			TRACE_-DATA_3 (0)
P19.0	PWM0_M_3	PWM0_50_N	TC0_M_3_TR0	TC0_50_TR1	TC0_H_0_TR0	SCB2_MISO (1)		SCB2_RX (1)		CAN1_3_TX			ETH0_RXD_0 (0)			FAULT_OUT_2
P19.1	PWM0_26	PWM0_M_3_N	TC0_26_TR0	TC0_M_3_TR1	TC0_H_0_TR1	SCB2_MOSI (1)	SCB2_SDA (1)	SCB2_TX (1)		CAN1_3_RX			ETH0_RXD_1 (0)			FAULT_OUT_3
P19.2	PWM0_27	PWM0_26_N	TC0_27_TR0	TC0_26_TR1	TC0_H_1_TR0	SCB2_CLK (1)	SCB2_SCL (1)	SCB2_RTS (1)					ETH0_RXD_2 (0)		TRIG_IN[28]	
P19.3	PWM0_28	PWM0_27_N	TC0_28_TR0	TC0_27_TR1	TC0_H_1_TR1	SCB2_SEL0 (1)		SCB2_CTS (1)					ETH0_RXD_3 (0)		TRIG_IN[29]	
P19.4	PWM0_29	PWM0_28_N	TC0_29_TR0	TC0_28_TR1	TC0_H_2_TR0	SCB2_SEL1 (1)										
P20.0	PWM0_30	PWM0_29_N	TC0_30_TR0	TC0_29_TR1	TC0_H_2_TR1	SCB2_SEL2 (1)			LIN5_RX							
P20.1	PWM0_49	PWM0_30_N	TC0_49_TR0	TC0_30_TR1	TC0_H_3_TR0				LIN5_TX							
P20.2	PWM0_48	PWM0_49_N	TC0_48_TR0	TC0_49_TR1	TC0_H_3_TR1				LIN5_EN							
P20.3	PWM0_47	PWM0_48_N	TC0_47_TR0	TC0_48_TR1		SCB1_RX (1)		SCB1_MISO (1)		CAN1_2_TX						
P20.4	PWM0_46	PWM0_47_N	TC0_46_TR0	TC0_47_TR1		SCB1_TX (1)	SCB1_SDA (1)	SCB1_MOSI (1)		CAN1_2_RX						
P20.5	PWM0_45	PWM0_46_N	TC0_45_TR0	TC0_46_TR1		SCB1_RTS (1)	SCB1_SCL (1)	SCB1_CLK (1)								
P20.6	PWM0_44	PWM0_45_N	TC0_44_TR0	TC0_45_TR1		SCB1_CTS (1)		SCB1_SEL0 (1)								
P20.7	PWM0_43	PWM0_44_N	TC0_43_TR0	TC0_44_TR1				SCB1_SEL1 (1)								



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P21.0	PWM0_42	PWM0_43_N	TC0_42_TR0	TC0_43_TR1				SCB1_SEL2 (1)								
P21.1	PWM0_41	PWM0_42_N	TC0_41_TR0	TC0_42_TR1												
P21.2	PWM0_40	PWM0_41_N	TC0_40_TR0	TC0_41_TR1							EXT_CLK					TRIG_DBG[1]
P21.3	PWM0_39	PWM0_40_N	TC0_39_TR0	TC0_40_TR1												
P21.4	PWM0_38	PWM0_39_N	TC0_38_TR0	TC0_39_TR1												
P21.5	PWM0_37	PWM0_38_N	TC0_37_TR0	TC0_38_TR1					LIN0_RX	CAN1_1_TX	PWM0_34	PWM0_35_N	ETH0_RX_CTL (0)			TRACE_- DATA_0 (1)
P21.6	PWM0_36	PWM0_37_N	TC0_36_TR0	TC0_37_TR1					LIN0_TX	LIN13_RX						
P21.7	PWM0_35	PWM0_36_N	TC0_35_TR0	TC0_36_TR1		SCB6_RX (1)		SCB6_MISO (1)	LIN0_EN	LIN13_TX						CAL_SUP_NZ
P22.1	PWM0_33	PWM0_34_N	TC0_33_TR0	TC0_34_TR1		SCB6_TX (1)	SCB6_SDA (1)	SCB6_MOSI (1)		CAN1_1_RX						TRACE_- DATA_1 (1)
P22.2	PWM0_32	PWM0_33_N	TC0_32_TR0	TC0_33_TR1		SCB6_RTS (1)	SCB6_SCL (1)	SCB6_CLK (1)								TRACE_- DATA_2 (1)
P22.3	PWM0_31	PWM0_32_N	TC0_31_TR0	TC0_32_TR1		SCB6_CTS (1)		SCB6_SEL0 (1)								TRACE_- DATA_3 (1)
P22.4	PWM0_30	PWM0_31_N	TC0_30_TR0	TC0_31_TR1				SCB6_SEL1 (1)								TRACE_CLOCK (1)
P22.5	PWM0_29	PWM0_30_N	TC0_29_TR0	TC0_30_TR1				SCB6_SEL2 (1)	LIN7_RX							
P22.6	PWM0_28	PWM0_29_N	TC0_28_TR0	TC0_29_TR1					LIN7_TX							
P22.7	PWM0_27	PWM0_28_N	TC0_27_TR0	TC0_28_TR1			LIN14_RX		LIN7_EN							
P23.0	PWM0_M_8	PWM0_27_N	TC0_M_8_TR0	TC0_27_TR1		SCB7_RX (1)	LIN14_TX	SCB7_MISO (1)		CAN1_0_TX						FAULT_OUT_0
P23.1	PWM0_M_9	PWM0_M_8_N	TC0_M_9_TR0	TC0_M_8_TR1		SCB7_TX (1)	SCB7_SDA (1)	SCB7_MOSI (1)		CAN1_0_RX						FAULT_OUT_1
P23.2	PWM0_M_10	PWM0_M_9_N	TC0_M_10_TR0	TC0_M_9_TR1		SCB7_RTS (1)	SCB7_SCL (1)	SCB7_CLK (1)	LIN6_RX							FAULT_OUT_2
P23.3	PWM0_M_11	PWM0_M_10_N	TC0_M_11_TR0	TC0_M_10_TR1		SCB7_CTS (1)		SCB7_SEL0 (1)	LIN6_TX				ETH0_RX_CLK (0)		TRIG_IN[30]	FAULT_OUT_3
P23.4	PWM0_25	PWM0_M_11_N	TC0_25_TR0	TC0_M_11_TR1		SCB2_MISO (2)		SCB7_SEL1 (1)							TRIG_IN[31]	TRIG_DBG[0]
P23.5	PWM0_24	PWM0_25_N	TC0_24_TR0	TC0_25_TR1		SCB2_MOSI (2)		SCB7_SEL2 (1)				LIN9_RX				
P23.6	PWM0_23	PWM0_24_N	TC0_23_TR0	TC0_24_TR1		SCB2_CLK (2)						LIN9_TX				
P23.7	PWM0_22	PWM0_23_N	TC0_22_TR0	TC0_23_TR1		SCB2_SEL0 (2)					EXT_CLK	LIN9_EN				CAL_SUP_NZ
P24.0											EXT_CLK				SDHC_CARD_- DETECT_N (1)	
P24.1												SPIHB_CLK (1)			SDHC_CARD_- MECH_WRITE_P ROT (1)	
P24.2												SPIHB_RWD S (1)			SDHC_- CLK_CARD (1)	
P24.3												SPIHB_SEL0 (1)			SDHC_- CARD_CMD (1)	
P24.4												SPIHB_SEL1 (1)			SDHC_- CARD_IF_P- WR_EN (1)	



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P25.0												SPIHB - DATA0 (1)		SDHC_CARD - DAT_3TO0_0 (1)		
P25.1												SPIHB - DATA1 (1)		SDHC_CARD - DAT_3TO0_1 (1)		
P25.2												SPIHB - DATA2 (1)		SDHC_CARD - DAT_3TO0_2 (1)		
P25.3												SPIHB - DATA3 (1)		SDHC_CARD - DAT_3TO0_3 (1)		
P25.4												SPIHB - DATA4 (1)		SDHC_CARD - DAT_7TO4_0 (1)		
P25.5												SPIHB - DATA5 (1)		SDHC_CARD - DAT_7TO4_1 (1)		
P25.6												SPIHB - DATA6 (1)		SDHC_CARD - DAT_7TO4_2 (1)		
P25.7												SPIHB - DATA7 (1)		SDHC_CARD - DAT_7TO4_3 (1)		
P26.0																
P26.1																
P26.2																
P26.3																
P26.4																
P26.5																
P26.6																
P26.7																
P27.0																
P27.1																
P27.2																
P27.3																
P27.4																
P27.5																
P27.6																
P27.7																
P28.0						SCB10_RX (0)		SCB10_MISO (0)								
P28.1						SCB10_TX (0)	SCB10_SDA (0)	SCB10_MOSI (0)								
P28.2						SCB10_RTS (0)	SCB10_SCL (0)	SCB10_CLK (0)								
P28.3						SCB10_CTS (0)		SCB10_SELO (0)								
P28.4								SCB10_SEL1 (0)								



表 13-1 运行模式下的备用引脚功能 (续) [23, 31, 32]

Port pin	Active mapping															
	HCon#8 ^[29]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT #0 ^[30]	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15
P28.5								SCB10_SEL2 (0)								
P28.6								SCB10_SEL3 (0)								
P28.7																
P29.0																
P29.1																
P29.2																
P29.3																
P29.4																
P29.5																
P29.6																
P29.7																
P30.0						SCB9_RTS (1)		SCB9_CLK (1)								
P30.1						SCB9_CTS (1)		SCB9_SEL0 (1)								
P30.2								SCB9_SEL1 (1)		CAN1_3_TX						
P30.3								SCB9_SEL2 (1)		CAN1_3_RX						
P31.0																
P31.1																
P31.2																
P32.0						SCB10_RX (1)		SCB10_MISO (1)								
P32.1						SCB10_TX (1)	SCB10_SDA (1)	SCB10_MOSI (1)								
P32.2						SCB10_RTS (1)	SCB10_SCL (1)	SCB10_CLK (1)								
P32.3						SCB10_CTS (1)		SCB10_SEL0 (1)								
P32.4							LIN10_RX	SCB10_SEL1 (1)								
P32.5							LIN10_TX	SCB10_SEL2 (1)								
P32.6							LIN10_EN	SCB10_SEL3 (1)								
P32.7																

备用功能引脚分配

13.1 引脚功能描述

表 13-2 引脚功能描述

Sl. No.	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_M_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number
9	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
10	SCBx_RX	SCB	UART Receive, x-SCB block
11	SCBx_TX	SCB	UART Transmit, x-SCB block
12	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
13	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
14	SCBx_SDA	SCB	I ² C Data line, x-SCB block
15	SCBx_SCL	SCB	I ² C Clock line, x-SCB block
16	SCBx_MISO	SCB	SPI Master Input Slave Output, x-SCB block
17	SCBx_MOSI	SCB	SPI Master Output Slave Input, x-SCB block
18	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
19	SCBx_SELy	SCB	SPI Slave Select, x-SCB block, y-select line
20	LINx_RX	LIN	LIN Receive line, x-LIN block
21	LINx_TX	LIN	LIN Transmit line, x-LIN block
22	LINx_EN	LIN	LIN Enable line, x-LIN block
23	CANx_y_TX	CANFD	CAN Transmit line, x-CAN block, y-channel number
24	CANx_y_RX	CANFD	CAN Receive line, x-CAN block, y-channel number
25	SPIHB_CLK	SMIF	SMIF interface clock
26	SPIHB_RWDS	SMIF	SMIF (SPI/HYPERBUS™) read-write-data-strobe line
27	SPIHB_SELx	SMIF	SMIF (SPI/HYPERBUS™) memory select line, x-select line number
28	SPIHB_DATAx	SMIF	SMIF (SPI/HYPERBUS™) memory data read and write line, x-0 to 7 data lines
29	ETHx_RX_ER	Ethernet	Ethernet receive error indication line, x-ETH module number
30	ETHx_ETH_TSU_TIMER_C-MP_VAL	Ethernet	Ethernet time stamp unit timer compare indication line, x-ETH module number
31	ETHx_MDIO	Ethernet	Ethernet management data input/output (MDIO) interface to PHY, x-ETH module number
32	ETHx_MDC	Ethernet	Ethernet management data clock (MDC) line, x-ETH module number
33	ETHx_REF_CLK	Ethernet	Ethernet reference clock line, x-ETH module number
34	ETHx_TX_CTL	Ethernet	Ethernet transmit control line, x-ETH module number
35	ETHx_TX_ER	Ethernet	Ethernet transmit error indication line, x-ETH module number
36	ETHx_TX_CLK	Ethernet	Ethernet transmit clock line, x-ETH module number
37	ETHx_TXD_y	Ethernet	Ethernet transmit data line, , x-ETH module number, y-transmit channel number
38	ETHx_RXD_y	Ethernet	Ethernet receive data line, , x-ETH module number, y-receive channel number
39	ETHx_RX_CTL	Ethernet	Ethernet receive control line, x-ETH module number
40	ETHx_RX_CLK	Ethernet	Ethernet receive clock line, x-ETH module number

备用功能引脚分配

表 13-2 引脚函数的描述 (续)

Sl. No.	Pin	Module	Description
41	SDHC_CARD_-MECH_WRITE_PROT	SDHC	SDHC mechanical write protect
42	SDHC_CARD_CMD	SDHC	SDHC command line
43	SDHC_CLK_CARD	SDHC	SDHC clock line
44	SDHC_CARD_DETECT_N	SDHC	SDHC interface insertion or removal detection line
45	SDHC_CARD_IF_PWR_EN	SDHC	SDHC interface power cycle line
46	SDHC_CARD_DAT_3TO0_x	SDHC	SDHC lower 4-bits of the data
47	SDHC_CARD_DAT_7TO4_x	SDHC	SDHC upper 4-bits of the data in 8-bit mode
48	AUDIOSSx_MCLK	AUDIOSS	AudioSS master clock out, x-AudioSS block
49	AUDIOSSx_TX_SCK	AUDIOSS	I ² S serial clock for transmitter, x-AudioSS block
50	AUDIOSSx_TX_WS	AUDIOSS	I ² S word select for transmitter, x-AudioSS block
51	AUDIOSSx_TX_SDO	AUDIOSS	I ² S serial data output for transmitter, x-AudioSS block
52	AUDIOSSx_CLK_I2S_IF	AUDIOSS	I ² S clock supplied from external I2S bus host, x-AudioSS block
53	AUDIOSSx_RX_SCK	AUDIOSS	I ² S serial clock for receiver, x-AudioSS block
54	AUDIOSSx_RX_WS	AUDIOSS	I ² S word select for receiver, x-AudioSS block
55	AUDIOSSx_RX_SDI	AUDIOSS	I ² S serial data input for receiver, x-AudioSS block
56	CAL_SUP_NZ	System	ETAS Calibration support line
57	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
58	TRACE_DATA_x	SRSS	Trace data out line x-0 to 3
59	TRACE_CLOCK	SRSS	Trace clock line
60	RTC_CAL	SRSS RTC	RTC calibration clock input
61	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
62	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
63	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
64	SWJ_SWDIO_TMS	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/Output)
65	SWJ_SWDIOE_TDI	SRSS	JTAG Test data input
66	HIBERNATE_WAKEUP[x]	SRSS	Hibernate wakeup line x-0 to 1
67	EXT_CLK	SRSS	External clock input or output
68	EXT_PS_CTL0	SRSS REGHC	REGHC control line, Transistor mode/Positive terminal of the current sense resistor, PMIC mode/Power good input from PMIC
69	EXT_PS_CTL1	SRSS REGHC	REGHC control line, Transistor mode/Negative terminal of the current sense resistor, PMIC mode/Enable output for PMIC
70	EXT_PS_CTL2	SRSS REGHC	REGHC control line, Transistor mode/unused, PMIC mode/Reset threshold adjustment for some PMICs
71	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
72	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
73	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
74	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
75	TRIG_IN[x]	HSIOM	HSIOM_IO_INPUT[x] of trigger inputs, x-0 to 47
76	TRIG_DBG[x]	HSIOM	HSIOM_IO_OUTPUT[x] of trigger outputs, x-0 to 1
77	WCO_IN	SRSS	Watch crystal oscillator input
78	WCO_OUT	SRSS	Watch crystal oscillator output
79	ECO_IN	SRSS	External crystal oscillator input
80	ECO_OUT	SRSS	External crystal oscillator output



中断和唤醒分配

14 中断和唤醒分配

表 14-1 外设中断分配和唤醒源

Interrupt	Source	Power Mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS Fault Structure #0 Interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS Fault Structure #1 Interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS Fault Structure #2 Interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS Fault Structure #3 Interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain Interrupt
13	srss_interrupt_mcwdt_0_IRQn	DeepSleep	Multi Counter Watchdog Timer #0 interrupt
14	srss_interrupt_mcwdt_1_IRQn	DeepSleep	Multi Counter Watchdog Timer #1 interrupt
15	srss_interrupt_mcwdt_2_IRQn	DeepSleep	Multi Counter Watchdog Timer #2 interrupt
16	srss_interrupt_wdt_IRQn	DeepSleep	Hardware Watchdog Timer interrupt
17	srss_interrupt_IRQn	DeepSleep	Other combined Interrupts for SRSS (LVD, CLKCAL)
18	scb_0_interrupt_IRQn	DeepSleep	SCB0 interrupt (DeepSleep capable)
19	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event gen DeepSleep domain interrupt
20	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Supply (V _{DDIO} , V _{DDA} , V _{DDD}) state change Interrupt
21	ioss_interrupt_gpio_dpslp_IRQn	DeepSleep	Consolidated Interrupt for GPIO_STD and GPIO_ENH, All Ports
22	ioss_interrupts_gpio_dpslp_0_IRQn	DeepSleep	GPIO_ENH Port #0 Interrupt
23	ioss_interrupts_gpio_dpslp_1_IRQn	DeepSleep	GPIO_STD Port #1 Interrupt
24	ioss_interrupts_gpio_dpslp_2_IRQn	DeepSleep	GPIO_STD Port #2 Interrupt
25	ioss_interrupts_gpio_dpslp_3_IRQn	DeepSleep	GPIO_STD Port #3 Interrupt
26	ioss_interrupts_gpio_dpslp_4_IRQn	DeepSleep	GPIO_STD Port #4 Interrupt
27	ioss_interrupts_gpio_dpslp_5_IRQn	DeepSleep	GPIO_STD Port #5 Interrupt
28	ioss_interrupts_gpio_dpslp_6_IRQn	DeepSleep	GPIO_STD Port #6 Interrupt
29	ioss_interrupts_gpio_dpslp_7_IRQn	DeepSleep	GPIO_STD Port #7 Interrupt
30	ioss_interrupts_gpio_dpslp_8_IRQn	DeepSleep	GPIO_STD Port #8 Interrupt
31	ioss_interrupts_gpio_dpslp_9_IRQn	DeepSleep	GPIO_STD Port #9 Interrupt
32	ioss_interrupts_gpio_dpslp_10_IRQn	DeepSleep	GPIO_STD Port #10 Interrupt
33	ioss_interrupts_gpio_dpslp_11_IRQn	DeepSleep	GPIO_STD Port #11 Interrupt
34	ioss_interrupts_gpio_dpslp_12_IRQn	DeepSleep	GPIO_STD Port #12 Interrupt
35	ioss_interrupts_gpio_dpslp_13_IRQn	DeepSleep	GPIO_STD Port #13 Interrupt
36	ioss_interrupts_gpio_dpslp_14_IRQn	DeepSleep	GPIO_STD Port #14 Interrupt
37	ioss_interrupts_gpio_dpslp_15_IRQn	DeepSleep	GPIO_STD Port #15 Interrupt
38	ioss_interrupts_gpio_dpslp_16_IRQn	DeepSleep	GPIO_STD Port #16 Interrupt
39	ioss_interrupts_gpio_dpslp_17_IRQn	DeepSleep	GPIO_STD Port #17 Interrupt
40	ioss_interrupts_gpio_dpslp_18_IRQn	DeepSleep	GPIO_STD Port #18 Interrupt
41	ioss_interrupts_gpio_dpslp_19_IRQn	DeepSleep	GPIO_STD Port #19 Interrupt
42	ioss_interrupts_gpio_dpslp_20_IRQn	DeepSleep	GPIO_STD Port #20 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
43	ioss_interrupts_gpio_dpslp_21_IRQn	DeepSleep	GPIO_STD Port #21 Interrupt
44	ioss_interrupts_gpio_dpslp_22_IRQn	DeepSleep	GPIO_STD Port #22 Interrupt
45	ioss_interrupts_gpio_dpslp_23_IRQn	DeepSleep	GPIO_STD Port #23 Interrupt
46	ioss_interrupts_gpio_dpslp_28_IRQn	DeepSleep	GPIO_STD Port #28 Interrupt
47	ioss_interrupts_gpio_dpslp_29_IRQn	DeepSleep	GPIO_STD Port #29 Interrupt
48	ioss_interrupts_gpio_dpslp_30_IRQn	DeepSleep	GPIO_STD Port #30 Interrupt
49	ioss_interrupts_gpio_dpslp_31_IRQn	DeepSleep	GPIO_STD Port #31 Interrupt
50	ioss_interrupts_gpio_dpslp_32_IRQn	DeepSleep	GPIO_STD Port #32 Interrupt
51	ioss_interrupts_gpio_act_IRQn	Active	Consolidated Interrupt for HSIO_STD, All Ports
52	ioss_interrupts_gpio_act_24_IRQn	Active	HSIO_STD Port #24 Interrupt
53	ioss_interrupts_gpio_act_25_IRQn	Active	HSIO_STD Port #25 Interrupt
54	ioss_interrupts_gpio_act_26_IRQn	Active	GPIO_STD Port #26 Interrupt
55	ioss_interrupts_gpio_act_27_IRQn	Active	GPIO_STD Port #27 Interrupt
56	cpuss_interrupt_crypto_IRQn	Active	CRYPTO Accelerator Interrupt
57	cpuss_interrupt_fm_IRQn	Active	Flash Macro Interrupt
58	cpuss_interrupts_cm7_0_fp_IRQn	Active	CM7_0 Floating Point operation fault
59	cpuss_interrupts_cm7_1_fp_IRQn	Active	CM7_1 Floating Point operation fault
60	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross Trigger Interface) #0
61	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI #1
62	cpuss_interrupts_cm7_0_cti_0_IRQn	Active	CM7_0 CTI #0
63	cpuss_interrupts_cm7_0_cti_1_IRQn	Active	CM7_0 CTI #1
64	cpuss_interrupts_cm7_1_cti_0_IRQn	Active	CM7_1 CTI #0
65	cpuss_interrupts_cm7_1_cti_1_IRQn	Active	CM7_1 CTI #1
66	evtgen_0_interrupt_IRQn	Active	Event gen Active domain Interrupt
67	canfd_0_interrupt0_IRQn	Active	CAN0, Consolidated Interrupt #0 for all four channels
68	canfd_0_interrupt1_IRQn	Active	CAN0, Consolidated Interrupt #1 for all four channels
69	canfd_1_interrupt0_IRQn	Active	CAN1, Consolidated Interrupt #0 for all four channels
70	canfd_1_interrupt1_IRQn	Active	CAN1, Consolidated Interrupt #1 for all four channels
71	canfd_0_interrupts0_0_IRQn	Active	CAN0, Interrupt #0, Channel #0
72	canfd_0_interrupts0_1_IRQn	Active	CAN0, Interrupt #0, Channel #1
73	canfd_0_interrupts0_2_IRQn	Active	CAN0, Interrupt #0, Channel #2
74	canfd_0_interrupts0_3_IRQn	Active	CAN0, Interrupt #0, Channel #3
75	canfd_0_interrupts1_0_IRQn	Active	CAN0, Interrupt #1, Channel #0
76	canfd_0_interrupts1_1_IRQn	Active	CAN0, Interrupt #1, Channel #1
77	canfd_0_interrupts1_2_IRQn	Active	CAN0, Interrupt #1, Channel #2
78	canfd_0_interrupts1_3_IRQn	Active	CAN0, Interrupt #1, Channel #3
79	canfd_1_interrupts0_0_IRQn	Active	CAN1, Interrupt #0, Channel #0
80	canfd_1_interrupts0_1_IRQn	Active	CAN1, Interrupt #0, Channel #1
81	canfd_1_interrupts0_2_IRQn	Active	CAN1, Interrupt #0, Channel #2
82	canfd_1_interrupts0_3_IRQn	Active	CAN1, Interrupt #0, Channel #3
83	canfd_1_interrupts1_0_IRQn	Active	CAN1, Interrupt #1, Channel #0
84	canfd_1_interrupts1_1_IRQn	Active	CAN1, Interrupt #1, Channel #1
85	canfd_1_interrupts1_2_IRQn	Active	CAN1, Interrupt #1, Channel #2
86	canfd_1_interrupts1_3_IRQn	Active	CAN1, Interrupt #1, Channel #3
87	lin_0_interrupts_0_IRQn	Active	LIN0, Channel #0 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
88	lin_0_interrupts_1_IRQn	Active	LIN0, Channel #1 Interrupt
89	lin_0_interrupts_2_IRQn	Active	LIN0, Channel #2 Interrupt
90	lin_0_interrupts_3_IRQn	Active	LIN0, Channel #3 Interrupt
91	lin_0_interrupts_4_IRQn	Active	LIN0, Channel #4 Interrupt
92	lin_0_interrupts_5_IRQn	Active	LIN0, Channel #5 Interrupt
93	lin_0_interrupts_6_IRQn	Active	LIN0, Channel #6 Interrupt
94	lin_0_interrupts_7_IRQn	Active	LIN0, Channel #7 Interrupt
95	lin_0_interrupts_8_IRQn	Active	LIN0, Channel #8 Interrupt
96	lin_0_interrupts_9_IRQn	Active	LIN0, Channel #9 Interrupt
97	lin_0_interrupts_10_IRQn	Active	LIN0, Channel #10 Interrupt
98	lin_0_interrupts_11_IRQn	Active	LIN0, Channel #11 Interrupt
99	lin_0_interrupts_12_IRQn	Active	LIN0, Channel #12 Interrupt
100	lin_0_interrupts_13_IRQn	Active	LIN0, Channel #13 Interrupt
101	lin_0_interrupts_14_IRQn	Active	LIN0, Channel #14 Interrupt
102	lin_0_interrupts_15_IRQn	Active	LIN0, Channel #15 Interrupt
103	scb_1_interrupt_IRQn	Active	SCB1 Interrupt
104	scb_2_interrupt_IRQn	Active	SCB2 Interrupt
105	scb_3_interrupt_IRQn	Active	SCB3 Interrupt
106	scb_4_interrupt_IRQn	Active	SCB4 Interrupt
107	scb_5_interrupt_IRQn	Active	SCB5 Interrupt
108	scb_6_interrupt_IRQn	Active	SCB6 Interrupt
109	scb_7_interrupt_IRQn	Active	SCB7 Interrupt
110	scb_8_interrupt_IRQn	Active	SCB8 Interrupt
111	scb_9_interrupt_IRQn	Active	SCB9 Interrupt
112	scb_10_interrupt_IRQn	Active	SCB10 Interrupt
113	pass_0_interrupts_sar_0_IRQn	Active	SAR0, Logical Channel #0 Interrupt
114	pass_0_interrupts_sar_1_IRQn	Active	SAR0, Logical Channel #1 Interrupt
115	pass_0_interrupts_sar_2_IRQn	Active	SAR0, Logical Channel #2 Interrupt
116	pass_0_interrupts_sar_3_IRQn	Active	SAR0, Logical Channel #3 Interrupt
117	pass_0_interrupts_sar_4_IRQn	Active	SAR0, Logical Channel #4 Interrupt
118	pass_0_interrupts_sar_5_IRQn	Active	SAR0, Logical Channel #5 Interrupt
119	pass_0_interrupts_sar_6_IRQn	Active	SAR0, Logical Channel #6 Interrupt
120	pass_0_interrupts_sar_7_IRQn	Active	SAR0, Logical Channel #7 Interrupt
121	pass_0_interrupts_sar_8_IRQn	Active	SAR0, Logical Channel #8 Interrupt
122	pass_0_interrupts_sar_9_IRQn	Active	SAR0, Logical Channel #9 Interrupt
123	pass_0_interrupts_sar_10_IRQn	Active	SAR0, Logical Channel #10 Interrupt
124	pass_0_interrupts_sar_11_IRQn	Active	SAR0, Logical Channel #11 Interrupt
125	pass_0_interrupts_sar_12_IRQn	Active	SAR0, Logical Channel #12 Interrupt
126	pass_0_interrupts_sar_13_IRQn	Active	SAR0, Logical Channel #13 Interrupt
127	pass_0_interrupts_sar_14_IRQn	Active	SAR0, Logical Channel #14 Interrupt
128	pass_0_interrupts_sar_15_IRQn	Active	SAR0, Logical Channel #15 Interrupt
129	pass_0_interrupts_sar_16_IRQn	Active	SAR0, Logical Channel #16 Interrupt
130	pass_0_interrupts_sar_17_IRQn	Active	SAR0, Logical Channel #17 Interrupt
131	pass_0_interrupts_sar_18_IRQn	Active	SAR0, Logical Channel #18 Interrupt
132	pass_0_interrupts_sar_19_IRQn	Active	SAR0, Logical Channel #19 Interrupt



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表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
133	pass_0_interrupts_sar_20_IRQn	Active	SAR0, Logical Channel #20 Interrupt
134	pass_0_interrupts_sar_21_IRQn	Active	SAR0, Logical Channel #21 Interrupt
135	pass_0_interrupts_sar_22_IRQn	Active	SAR0, Logical Channel #22 Interrupt
136	pass_0_interrupts_sar_23_IRQn	Active	SAR0, Logical Channel #23 Interrupt
137	pass_0_interrupts_sar_24_IRQn	Active	SAR0, Logical Channel #24 Interrupt
138	pass_0_interrupts_sar_25_IRQn	Active	SAR0, Logical Channel #25 Interrupt
139	pass_0_interrupts_sar_26_IRQn	Active	SAR0, Logical Channel #26 Interrupt
140	pass_0_interrupts_sar_27_IRQn	Active	SAR0, Logical Channel #27 Interrupt
141	pass_0_interrupts_sar_28_IRQn	Active	SAR0, Logical Channel #28 Interrupt
142	pass_0_interrupts_sar_29_IRQn	Active	SAR0, Logical Channel #29 Interrupt
143	pass_0_interrupts_sar_30_IRQn	Active	SAR0, Logical Channel #30 Interrupt
144	pass_0_interrupts_sar_31_IRQn	Active	SAR0, Logical Channel #31 Interrupt
145	pass_0_interrupts_sar_32_IRQn	Active	SAR1, Logical Channel #0 Interrupt
146	pass_0_interrupts_sar_33_IRQn	Active	SAR1, Logical Channel #1 Interrupt
147	pass_0_interrupts_sar_34_IRQn	Active	SAR1, Logical Channel #2 Interrupt
148	pass_0_interrupts_sar_35_IRQn	Active	SAR1, Logical Channel #3 Interrupt
149	pass_0_interrupts_sar_36_IRQn	Active	SAR1, Logical Channel #4 Interrupt
150	pass_0_interrupts_sar_37_IRQn	Active	SAR1, Logical Channel #5 Interrupt
151	pass_0_interrupts_sar_38_IRQn	Active	SAR1, Logical Channel #6 Interrupt
152	pass_0_interrupts_sar_39_IRQn	Active	SAR1, Logical Channel #7 Interrupt
153	pass_0_interrupts_sar_40_IRQn	Active	SAR1, Logical Channel #8 Interrupt
154	pass_0_interrupts_sar_41_IRQn	Active	SAR1, Logical Channel #9 Interrupt
155	pass_0_interrupts_sar_42_IRQn	Active	SAR1, Logical Channel #10 Interrupt
156	pass_0_interrupts_sar_43_IRQn	Active	SAR1, Logical Channel #11 Interrupt
157	pass_0_interrupts_sar_44_IRQn	Active	SAR1, Logical Channel #12 Interrupt
158	pass_0_interrupts_sar_45_IRQn	Active	SAR1, Logical Channel #13 Interrupt
159	pass_0_interrupts_sar_46_IRQn	Active	SAR1, Logical Channel #14 Interrupt
160	pass_0_interrupts_sar_47_IRQn	Active	SAR1, Logical Channel #15 Interrupt
161	pass_0_interrupts_sar_48_IRQn	Active	SAR1, Logical Channel #16 Interrupt
162	pass_0_interrupts_sar_49_IRQn	Active	SAR1, Logical Channel #17 Interrupt
163	pass_0_interrupts_sar_50_IRQn	Active	SAR1, Logical Channel #18 Interrupt
164	pass_0_interrupts_sar_51_IRQn	Active	SAR1, Logical Channel #19 Interrupt
165	pass_0_interrupts_sar_52_IRQn	Active	SAR1, Logical Channel #20 Interrupt
166	pass_0_interrupts_sar_53_IRQn	Active	SAR1, Logical Channel #21 Interrupt
167	pass_0_interrupts_sar_54_IRQn	Active	SAR1, Logical Channel #22 Interrupt
168	pass_0_interrupts_sar_55_IRQn	Active	SAR1, Logical Channel #23 Interrupt
169	pass_0_interrupts_sar_56_IRQn	Active	SAR1, Logical Channel #24 Interrupt
170	pass_0_interrupts_sar_57_IRQn	Active	SAR1, Logical Channel #25 Interrupt
171	pass_0_interrupts_sar_58_IRQn	Active	SAR1, Logical Channel #26 Interrupt
172	pass_0_interrupts_sar_59_IRQn	Active	SAR1, Logical Channel #27 Interrupt
173	pass_0_interrupts_sar_60_IRQn	Active	SAR1, Logical Channel #28 Interrupt
174	pass_0_interrupts_sar_61_IRQn	Active	SAR1, Logical Channel #29 Interrupt
175	pass_0_interrupts_sar_62_IRQn	Active	SAR1, Logical Channel #30 Interrupt
176	pass_0_interrupts_sar_63_IRQn	Active	SAR1, Logical Channel #31 Interrupt
177	pass_0_interrupts_sar_64_IRQn	Active	SAR2, Logical Channel #0 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
178	pass_0_interrupts_sar_65_IRQn	Active	SAR2, Logical Channel #1 Interrupt
179	pass_0_interrupts_sar_66_IRQn	Active	SAR2, Logical Channel #2 Interrupt
180	pass_0_interrupts_sar_67_IRQn	Active	SAR2, Logical Channel #3 Interrupt
181	pass_0_interrupts_sar_68_IRQn	Active	SAR2, Logical Channel #4 Interrupt
182	pass_0_interrupts_sar_69_IRQn	Active	SAR2, Logical Channel #5 Interrupt
183	pass_0_interrupts_sar_70_IRQn	Active	SAR2, Logical Channel #6 Interrupt
184	pass_0_interrupts_sar_71_IRQn	Active	SAR2, Logical Channel #7 Interrupt
185	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA0, Channel #0 Interrupt
186	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA0, Channel #1 Interrupt
187	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA0, Channel #2 Interrupt
188	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA0, Channel #3 Interrupt
189	cpuss_interrupts_dmac_4_IRQn	Active	CPUSS M-DMA0, Channel #4 Interrupt
190	cpuss_interrupts_dmac_5_IRQn	Active	CPUSS M-DMA0, Channel #5 Interrupt
191	cpuss_interrupts_dmac_6_IRQn	Active	CPUSS M-DMA0, Channel #6 Interrupt
192	cpuss_interrupts_dmac_7_IRQn	Active	CPUSS M-DMA0, Channel #7 Interrupt
193	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA0, Channel #0 Interrupt
194	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA0, Channel #1 Interrupt
195	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA0, Channel #2 Interrupt
196	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA0, Channel #3 Interrupt
197	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA0, Channel #4 Interrupt
198	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA0, Channel #5 Interrupt
199	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA0, Channel #6 Interrupt
200	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA0, Channel #7 Interrupt
201	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA0, Channel #8 Interrupt
202	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA0, Channel #9 Interrupt
203	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA0, Channel #10 Interrupt
204	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA0, Channel #11 Interrupt
205	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA0, Channel #12 Interrupt
206	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA0, Channel #13 Interrupt
207	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA0, Channel #14 Interrupt
208	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA0, Channel #15 Interrupt
209	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA0, Channel #16 Interrupt
210	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA0, Channel #17 Interrupt
211	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA0, Channel #18 Interrupt
212	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA0, Channel #19 Interrupt
213	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA0, Channel #20 Interrupt
214	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA0, Channel #21 Interrupt
215	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA0, Channel #22 Interrupt
216	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA0, Channel #23 Interrupt
217	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA0, Channel #24 Interrupt
218	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA0, Channel #25 Interrupt
219	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA0, Channel #26 Interrupt
220	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA0, Channel #27 Interrupt
221	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA0, Channel #28 Interrupt
222	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA0, Channel #29 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
223	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA0, Channel #30 Interrupt
224	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA0, Channel #31 Interrupt
225	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA0, Channel #32 Interrupt
226	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA0, Channel #33 Interrupt
227	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA0, Channel #34 Interrupt
228	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA0, Channel #35 Interrupt
229	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA0, Channel #36 Interrupt
230	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA0, Channel #37 Interrupt
231	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA0, Channel #38 Interrupt
232	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA0, Channel #39 Interrupt
233	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA0, Channel #40 Interrupt
234	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA0, Channel #41 Interrupt
235	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA0, Channel #42 Interrupt
236	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA0, Channel #43 Interrupt
237	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA0, Channel #44 Interrupt
238	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA0, Channel #45 Interrupt
239	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA0, Channel #46 Interrupt
240	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA0, Channel #47 Interrupt
241	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA0, Channel #48 Interrupt
242	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA0, Channel #49 Interrupt
243	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA0, Channel #50 Interrupt
244	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA0, Channel #51 Interrupt
245	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA0, Channel #52 Interrupt
246	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA0, Channel #53 Interrupt
247	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA0, Channel #54 Interrupt
248	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA0, Channel #55 Interrupt
249	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA0, Channel #56 Interrupt
250	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA0, Channel #57 Interrupt
251	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA0, Channel #58 Interrupt
252	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA0, Channel #59 Interrupt
253	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA0, Channel #60 Interrupt
254	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA0, Channel #61 Interrupt
255	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA0, Channel #62 Interrupt
256	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA0, Channel #63 Interrupt
257	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA0, Channel #64 Interrupt
258	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA0, Channel #65 Interrupt
259	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA0, Channel #66 Interrupt
260	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA0, Channel #67 Interrupt
261	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA0, Channel #68 Interrupt
262	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA0, Channel #69 Interrupt
263	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA0, Channel #70 Interrupt
264	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA0, Channel #71 Interrupt
265	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA0, Channel #72 Interrupt
266	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA0, Channel #73 Interrupt
267	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA0, Channel #74 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
268	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA0, Channel #75 Interrupt
269	cpuss_interrupts_dw0_76_IRQn	Active	CPUSS P-DMA0, Channel #76 Interrupt
270	cpuss_interrupts_dw0_77_IRQn	Active	CPUSS P-DMA0, Channel #77 Interrupt
271	cpuss_interrupts_dw0_78_IRQn	Active	CPUSS P-DMA0, Channel #78 Interrupt
272	cpuss_interrupts_dw0_79_IRQn	Active	CPUSS P-DMA0, Channel #79 Interrupt
273	cpuss_interrupts_dw0_80_IRQn	Active	CPUSS P-DMA0, Channel #80 Interrupt
274	cpuss_interrupts_dw0_81_IRQn	Active	CPUSS P-DMA0, Channel #81 Interrupt
275	cpuss_interrupts_dw0_82_IRQn	Active	CPUSS P-DMA0, Channel #82 Interrupt
276	cpuss_interrupts_dw0_83_IRQn	Active	CPUSS P-DMA0, Channel #83 Interrupt
277	cpuss_interrupts_dw0_84_IRQn	Active	CPUSS P-DMA0, Channel #84 Interrupt
278	cpuss_interrupts_dw0_85_IRQn	Active	CPUSS P-DMA0, Channel #85 Interrupt
279	cpuss_interrupts_dw0_86_IRQn	Active	CPUSS P-DMA0, Channel #86 Interrupt
280	cpuss_interrupts_dw0_87_IRQn	Active	CPUSS P-DMA0, Channel #87 Interrupt
281	cpuss_interrupts_dw0_88_IRQn	Active	CPUSS P-DMA0, Channel #88 Interrupt
282	cpuss_interrupts_dw0_89_IRQn	Active	CPUSS P-DMA0, Channel #89 Interrupt
283	cpuss_interrupts_dw0_90_IRQn	Active	CPUSS P-DMA0, Channel #90 Interrupt
284	cpuss_interrupts_dw0_91_IRQn	Active	CPUSS P-DMA0, Channel #91 Interrupt
285	cpuss_interrupts_dw0_92_IRQn	Active	CPUSS P-DMA0, Channel #92 Interrupt
286	cpuss_interrupts_dw0_93_IRQn	Active	CPUSS P-DMA0, Channel #93 Interrupt
287	cpuss_interrupts_dw0_94_IRQn	Active	CPUSS P-DMA0, Channel #94 Interrupt
288	cpuss_interrupts_dw0_95_IRQn	Active	CPUSS P-DMA0, Channel #95 Interrupt
289	cpuss_interrupts_dw0_96_IRQn	Active	CPUSS P-DMA0, Channel #96 Interrupt
290	cpuss_interrupts_dw0_97_IRQn	Active	CPUSS P-DMA0, Channel #97 Interrupt
291	cpuss_interrupts_dw0_98_IRQn	Active	CPUSS P-DMA0, Channel #98 Interrupt
292	cpuss_interrupts_dw0_99_IRQn	Active	CPUSS P-DMA0, Channel #99 Interrupt
293	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA1, Channel #0 Interrupt
294	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA1, Channel #1 Interrupt
295	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA1, Channel #2 Interrupt
296	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA1, Channel #3 Interrupt
297	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA1, Channel #4 Interrupt
298	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA1, Channel #5 Interrupt
299	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA1, Channel #6 Interrupt
300	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA1, Channel #7 Interrupt
301	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA1, Channel #8 Interrupt
302	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA1, Channel #9 Interrupt
303	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA1, Channel #10 Interrupt
304	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA1, Channel #11 Interrupt
305	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA1, Channel #12 Interrupt
306	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA1, Channel #13 Interrupt
307	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA1, Channel #14 Interrupt
308	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA1, Channel #15 Interrupt
309	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA1, Channel #16 Interrupt
310	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA1, Channel #17 Interrupt
311	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA1, Channel #18 Interrupt
312	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA1, Channel #19 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
313	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA1, Channel #20 Interrupt
314	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA1, Channel #21 Interrupt
315	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA1, Channel #22 Interrupt
316	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA1, Channel #23 Interrupt
317	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA1, Channel #24 Interrupt
318	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA1, Channel #25 Interrupt
319	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA1, Channel #26 Interrupt
320	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA1, Channel #27 Interrupt
321	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA1, Channel #28 Interrupt
322	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA1, Channel #29 Interrupt
323	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA1, Channel #30 Interrupt
324	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA1, Channel #31 Interrupt
325	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA1, Channel #32 Interrupt
326	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA1, Channel #33 Interrupt
327	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA1, Channel #34 Interrupt
328	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA1, Channel #35 Interrupt
329	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA1, Channel #36 Interrupt
330	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA1, Channel #37 Interrupt
331	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA1, Channel #38 Interrupt
332	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA1, Channel #39 Interrupt
333	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA1, Channel #40 Interrupt
334	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA1, Channel #41 Interrupt
335	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA1, Channel #42 Interrupt
336	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA1, Channel #43 Interrupt
337	cpuss_interrupts_dw1_44_IRQn	Active	CPUSS P-DMA1, Channel #44 Interrupt
338	cpuss_interrupts_dw1_45_IRQn	Active	CPUSS P-DMA1, Channel #45 Interrupt
339	cpuss_interrupts_dw1_46_IRQn	Active	CPUSS P-DMA1, Channel #46 Interrupt
340	cpuss_interrupts_dw1_47_IRQn	Active	CPUSS P-DMA1, Channel #47 Interrupt
341	cpuss_interrupts_dw1_48_IRQn	Active	CPUSS P-DMA1, Channel #48 Interrupt
342	cpuss_interrupts_dw1_49_IRQn	Active	CPUSS P-DMA1, Channel #49 Interrupt
343	cpuss_interrupts_dw1_50_IRQn	Active	CPUSS P-DMA1, Channel #50 Interrupt
344	cpuss_interrupts_dw1_51_IRQn	Active	CPUSS P-DMA1, Channel #51 Interrupt
345	cpuss_interrupts_dw1_52_IRQn	Active	CPUSS P-DMA1, Channel #52 Interrupt
346	cpuss_interrupts_dw1_53_IRQn	Active	CPUSS P-DMA1, Channel #53 Interrupt
347	cpuss_interrupts_dw1_54_IRQn	Active	CPUSS P-DMA1, Channel #54 Interrupt
348	cpuss_interrupts_dw1_55_IRQn	Active	CPUSS P-DMA1, Channel #55 Interrupt
349	cpuss_interrupts_dw1_56_IRQn	Active	CPUSS P-DMA1, Channel #56 Interrupt
350	cpuss_interrupts_dw1_57_IRQn	Active	CPUSS P-DMA1, Channel #57 Interrupt
351	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 Group #0, Counter #0 Interrupt
352	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 Group #0, Counter #1 Interrupt
353	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 Group #0, Counter #2 Interrupt
354	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 Group #0, Counter #3 Interrupt
355	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 Group #0, Counter #4 Interrupt
356	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 Group #0, Counter #5 Interrupt
357	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 Group #0, Counter #6 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
358	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 Group #0, Counter #7 Interrupt
359	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 Group #0, Counter #8 Interrupt
360	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 Group #0, Counter #9 Interrupt
361	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 Group #0, Counter #10 Interrupt
362	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 Group #0, Counter #11 Interrupt
363	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 Group #0, Counter #12 Interrupt
364	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 Group #0, Counter #13 Interrupt
365	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 Group #0, Counter #14 Interrupt
366	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 Group #0, Counter #15 Interrupt
367	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 Group #0, Counter #16 Interrupt
368	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 Group #0, Counter #17 Interrupt
369	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 Group #0, Counter #18 Interrupt
370	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 Group #0, Counter #19 Interrupt
371	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 Group #0, Counter #20 Interrupt
372	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 Group #0, Counter #21 Interrupt
373	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 Group #0, Counter #22 Interrupt
374	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 Group #0, Counter #23 Interrupt
375	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 Group #0, Counter #24 Interrupt
376	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 Group #0, Counter #25 Interrupt
377	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 Group #0, Counter #26 Interrupt
378	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 Group #0, Counter #27 Interrupt
379	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 Group #0, Counter #28 Interrupt
380	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 Group #0, Counter #29 Interrupt
381	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 Group #0, Counter #30 Interrupt
382	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 Group #0, Counter #31 Interrupt
383	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 Group #0, Counter #32 Interrupt
384	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 Group #0, Counter #33 Interrupt
385	tcpwm_0_interrupts_34_IRQn	Active	TCPWM0 Group #0, Counter #34 Interrupt
386	tcpwm_0_interrupts_35_IRQn	Active	TCPWM0 Group #0, Counter #35 Interrupt
387	tcpwm_0_interrupts_36_IRQn	Active	TCPWM0 Group #0, Counter #36 Interrupt
388	tcpwm_0_interrupts_37_IRQn	Active	TCPWM0 Group #0, Counter #37 Interrupt
389	tcpwm_0_interrupts_38_IRQn	Active	TCPWM0 Group #0, Counter #38 Interrupt
390	tcpwm_0_interrupts_39_IRQn	Active	TCPWM0 Group #0, Counter #39 Interrupt
391	tcpwm_0_interrupts_40_IRQn	Active	TCPWM0 Group #0, Counter #40 Interrupt
392	tcpwm_0_interrupts_41_IRQn	Active	TCPWM0 Group #0, Counter #41 Interrupt
393	tcpwm_0_interrupts_42_IRQn	Active	TCPWM0 Group #0, Counter #42 Interrupt
394	tcpwm_0_interrupts_43_IRQn	Active	TCPWM0 Group #0, Counter #43 Interrupt
395	tcpwm_0_interrupts_44_IRQn	Active	TCPWM0 Group #0, Counter #44 Interrupt
396	tcpwm_0_interrupts_45_IRQn	Active	TCPWM0 Group #0, Counter #45 Interrupt
397	tcpwm_0_interrupts_46_IRQn	Active	TCPWM0 Group #0, Counter #46 Interrupt
398	tcpwm_0_interrupts_47_IRQn	Active	TCPWM0 Group #0, Counter #47 Interrupt
399	tcpwm_0_interrupts_48_IRQn	Active	TCPWM0 Group #0, Counter #48 Interrupt
400	tcpwm_0_interrupts_49_IRQn	Active	TCPWM0 Group #0, Counter #49 Interrupt
401	tcpwm_0_interrupts_50_IRQn	Active	TCPWM0 Group #0, Counter #50 Interrupt
402	tcpwm_0_interrupts_51_IRQn	Active	TCPWM0 Group #0, Counter #51 Interrupt



中断和唤醒分配

表 14-1 外设中断分配和唤醒源 (续)

Interrupt	Source	Power Mode	Description
403	tcpwm_0_interrupts_52_IRQn	Active	TCPWM0 Group #0, Counter #52 Interrupt
404	tcpwm_0_interrupts_53_IRQn	Active	TCPWM0 Group #0, Counter #53 Interrupt
405	tcpwm_0_interrupts_54_IRQn	Active	TCPWM0 Group #0, Counter #54 Interrupt
406	tcpwm_0_interrupts_55_IRQn	Active	TCPWM0 Group #0, Counter #55 Interrupt
407	tcpwm_0_interrupts_56_IRQn	Active	TCPWM0 Group #0, Counter #56 Interrupt
408	tcpwm_0_interrupts_57_IRQn	Active	TCPWM0 Group #0, Counter #57 Interrupt
409	tcpwm_0_interrupts_58_IRQn	Active	TCPWM0 Group #0, Counter #58 Interrupt
410	tcpwm_0_interrupts_59_IRQn	Active	TCPWM0 Group #0, Counter #59 Interrupt
411	tcpwm_0_interrupts_60_IRQn	Active	TCPWM0 Group #0, Counter #60 Interrupt
412	tcpwm_0_interrupts_61_IRQn	Active	TCPWM0 Group #0, Counter #61 Interrupt
413	tcpwm_0_interrupts_62_IRQn	Active	TCPWM0 Group #0, Counter #62 Interrupt
414	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 Group #1, Counter #0 Interrupt
415	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 Group #1, Counter #1 Interrupt
416	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 Group #1, Counter #2 Interrupt
417	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 Group #1, Counter #3 Interrupt
418	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 Group #1, Counter #4 Interrupt
419	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 Group #1, Counter #5 Interrupt
420	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 Group #1, Counter #6 Interrupt
421	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 Group #1, Counter #7 Interrupt
422	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 Group #1, Counter #8 Interrupt
423	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 Group #1, Counter #9 Interrupt
424	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 Group #1, Counter #10 Interrupt
425	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 Group #1, Counter #11 Interrupt
426	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 Group #2, Counter #0 Interrupt
427	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 Group #2, Counter #1 Interrupt
428	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 Group #2, Counter #2 Interrupt
429	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 Group #2, Counter #3 Interrupt
430	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 Group #2, Counter #4 Interrupt
431	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 Group #2, Counter #5 Interrupt
432	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 Group #2, Counter #6 Interrupt
433	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 Group #2, Counter #7 Interrupt
434	smif_0_interrupt_IRQn	Active	SMIF0 (QSPI) interrupt
435	eth_0_interrupt_eth_0_IRQn	Active	Ethernet0 interrupt for dma_priority_queue0
436	eth_0_interrupt_eth_2_IRQn	Active	Ethernet0 interrupt for dma_priority_queue2
437	eth_0_interrupt_eth_1_IRQn	Active	Ethernet0 interrupt for dma_priority_queue1
438	sdhc_0_interrupt_general_IRQn	Active	SDHC0 general interrupt
439	sdhc_0_interrupt_wakeup_IRQn	Active	SDHC0 wakeup interrupt
440	audioss_0_interrupt_i2s_IRQn	Active	AUDIOSS I ² S0 interrupt
441	audioss_1_interrupt_i2s_IRQn	Active	AUDIOSS I ² S1 interrupt
442	audioss_2_interrupt_i2s_IRQn	Active	AUDIOSS I ² S2 interrupt



核心中断类型

15 核心中断类型

表 15-1 核心中断类型

Interrupt	Source	Power mode	Description
0	CPUIntIdx0_IRQn ^[33]	DeepSleep	CPU User Interrupt #0
1	CPUIntIdx1_IRQn ^[33]	DeepSleep	CPU User Interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU User Interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU User Interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU User Interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU User Interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU User Interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU User Interrupt #7
8	Internal0_IRQn	Active	Internal Software Interrupt #0
9	Internal1_IRQn	Active	Internal Software Interrupt #1
10	Internal2_IRQn	Active	Internal Software Interrupt #2
11	Internal3_IRQn	Active	Internal Software Interrupt #3
12	Internal4_IRQn	Active	Internal Software Interrupt #4
13	Internal5_IRQn	Active	Internal Software Interrupt #5
14	Internal6_IRQn	Active	Internal Software Interrupt #6
15	Internal7_IRQn	Active	Internal Software Interrupt #7

注:

33. 用户中断不能用于 CM0+ 应用程序, 因为它由系统调用内部使用。注意, 这不会影响 CM7 应用程序。

16 触发用多路复用器

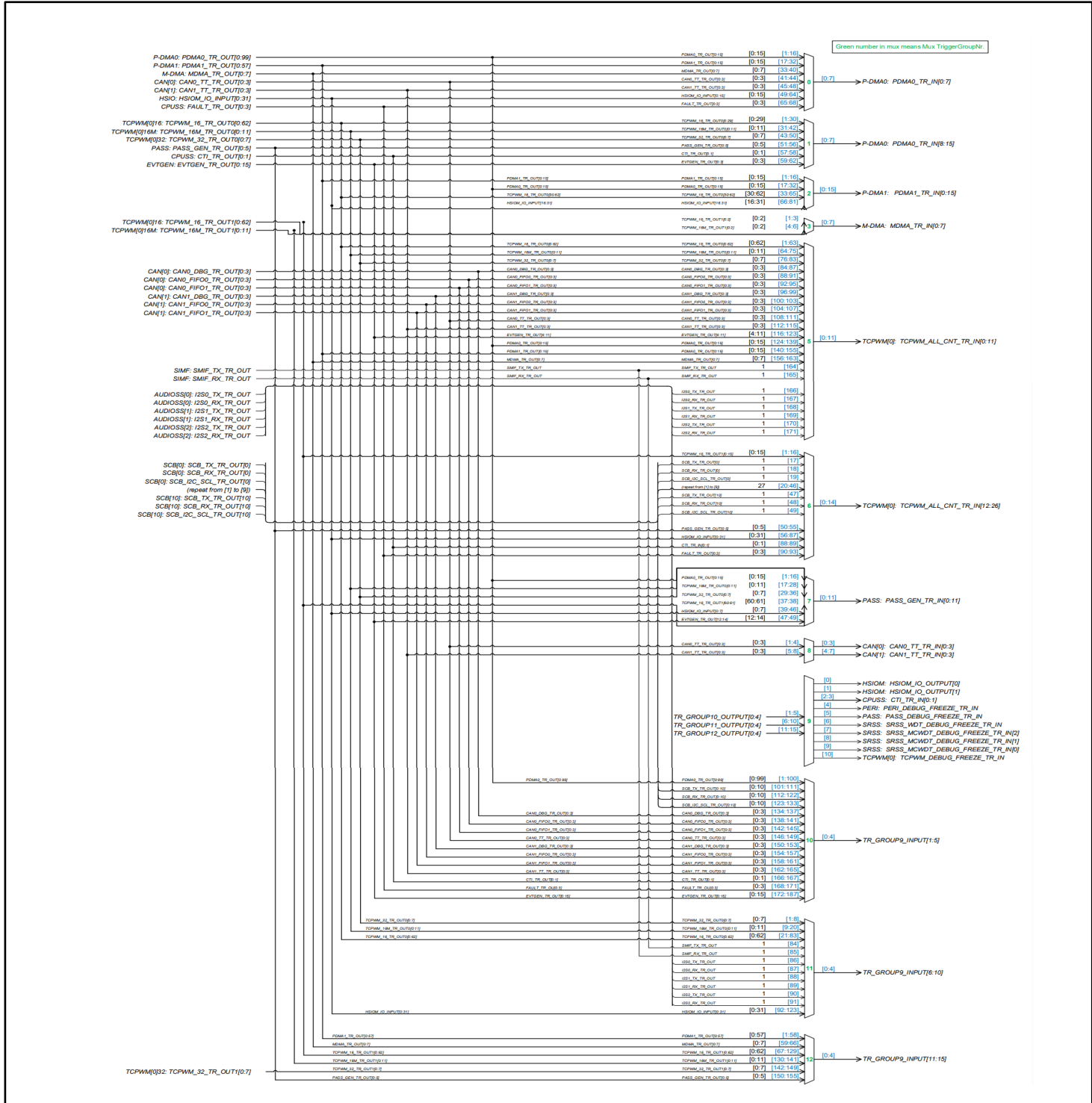


图 16-1 触发用多路复用器^[34]

注:

34. 该图仅显示TRIG_LABEL; 最终触发形成基于公式TRIG_{PREFIX(IN/OUT)}_{MUX_x}_{TRIG_LABEL}和表17-1和表 18-1 中提供的信息。

触发组输入

17 触发组输入

表 17-1 触发输入

Input	Trigger	Description
MUX Group 0: P-DMA0 trigger multiplexer		
1:16 ^[35]	PDMA0_TR_OUT[0:15]	Allow P-DMA0 to chain to itself. Channels 0 - 15 are dedicated for chaining
17:32	PDMA1_TR_OUT[0:15]	Cross connections from P-DMA1 to P-DMA0, Channels 0-15 are used
33:40	MDMA_TR_OUT[0:7]	Cross connections from M-DMA0 to P-DMA0
41:44	CAN0_TT_TR_OUT[0:3]	CAN0 TT Sync Outputs
45:48	CAN1_TT_TR_OUT[0:3]	CAN1 TT Sync Outputs
49:64	HSIOM_IO_INPUT[0:15]	I/O Inputs
65:68	FAULT_TR_OUT[0:3]	Fault events
MUX Group 1: TCPWM to P-DMA0 trigger multiplexer		
1:30	TCPWM_16_TR_OUT0[0:29]	16-bit TCPWM0 counters
31:42	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
43:50	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
51:56	PASS_GEN_TR_OUT[0:5]	PASS SAR events
57:58	CTI_TR_OUT[0:1]	Trace events
59:62	EVTGEN_TR_OUT[0:3]	Event generator triggers
MUX Group 2: P-DMA1 trigger multiplexer		
1:16	PDMA1_TR_OUT[0:15]	Allow P-DMA1 to chain to itself. Channels 0–15 are dedicated for chaining
17:32	PDMA0_TR_OUT[0:15]	Cross connections from P-DMA0 to P-DMA1, channels 0–15 are used
33:65	TCPWM_16_TR_OUT0[30:62]	16-bit TCPWM0 counters
66:81	HSIOM_IO_INPUT[16:31]	I/O Inputs
MUX Group 3: M-DMA0 trigger multiplexer		
1:3	TCPWM_16_TR_OUT1[0:2]	16-bit TCPWM0 counters
4:6	TCPWM_16M_TR_OUT1[0:2]	16-bit Motor enhanced TCPWM0 counters
MUX Group 5: TCPWM0 Loop back trigger multiplexer		
1:63	TCPWM_16_TR_OUT0[0:62]	16-bit TCPWM0 counters
64:75	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
76:83	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
84:87	CAN0_DBG_TR_OUT[0:3]	CAN0 M-DMA0 events
88:91	CAN0_FIFO0_TR_OUT[0:3]	CAN0 FIFO0 events
92:95	CAN0_FIFO1_TR_OUT[0:3]	CAN0 FIFO1 events
96:99	CAN1_DBG_TR_OUT[0:3]	CAN1 M-DMA0 events
100:103	CAN1_FIFO0_TR_OUT[0:3]	CAN1 FIFO0 events
104:107	CAN1_FIFO1_TR_OUT[0:3]	CAN1 FIFO1 events
108:111	CAN0_TT_TR_OUT[0:3]	CAN0 TT Sync Outputs
112:115	CAN1_TT_TR_OUT[0:3]	CAN1 TT Sync Outputs
116:123	EVTGEN_TR_OUT[4:11]	Event generator triggers
124:139	PDMA0_TR_OUT[0:15]	P-DMA0 general-purpose triggers
140:155	PDMA1_TR_OUT[0:15]	P-DMA1 general-purpose triggers
156:163	MDMA_TR_OUT[0:7]	M-DMA0 events
164	SMIF_TX_TR_OUT	SMIF0 TX trigger
165	SMIF_RX_TR_OUT	SMIF0 RX trigger
166	I2S0_TX_TR_OUT	I ² S0 TX trigger

注：
35. “x:y” 表示从“x”到“y”的范围。



触发组输入

表 17-1 触发输入 (续)

Input	Trigger	Description
167	I2S0_RX_TR_OUT	I ² S0 RX trigger
168	I2S1_TX_TR_OUT	I ² S1 TX trigger
169	I2S1_RX_TR_OUT	I ² S1 RX trigger
170	I2S2_TX_TR_OUT	I ² S2 TX trigger
171	I2S2_RX_TR_OUT	I ² S2 RX trigger
MUX Group 6: TCPWM0 trigger Multiplexer		
1:16	TCPWM_16_TR_OUT1[0:15]	16-bit TCPWM0 counters
17	SCB_TX_TR_OUT[0]	SCB0 TX trigger
18	SCB_RX_TR_OUT[0]	SCB0 RX trigger
19	SCB_I2C_SCL_TR_OUT[0]	SCB0 I ² C trigger
20	SCB_TX_TR_OUT[1]	SCB1 TX trigger
21	SCB_RX_TR_OUT[1]	SCB1 RX trigger
22	SCB_I2C_SCL_TR_OUT[1]	SCB1 I ² C trigger
23	SCB_TX_TR_OUT[2]	SCB2 TX trigger
24	SCB_RX_TR_OUT[2]	SCB2 RX trigger
25	SCB_I2C_SCL_TR_OUT[2]	SCB2 I ² C trigger
26	SCB_TX_TR_OUT[3]	SCB3 TX trigger
27	SCB_RX_TR_OUT[3]	SCB3 RX trigger
28	SCB_I2C_SCL_TR_OUT[3]	SCB3 I ² C trigger
29	SCB_TX_TR_OUT[4]	SCB4 TX trigger
30	SCB_RX_TR_OUT[4]	SCB4 RX trigger
31	SCB_I2C_SCL_TR_OUT[4]	SCB4 I ² C trigger
32	SCB_TX_TR_OUT[5]	SCB5 TX trigger
33	SCB_RX_TR_OUT[5]	SCB5 RX trigger
34	SCB_I2C_SCL_TR_OUT[5]	SCB5 I ² C trigger
35	SCB_TX_TR_OUT[6]	SCB6 TX trigger
36	SCB_RX_TR_OUT[6]	SCB6 RX trigger
37	SCB_I2C_SCL_TR_OUT[6]	SCB6 I ² C trigger
38	SCB_TX_TR_OUT[7]	SCB7 TX trigger
39	SCB_RX_TR_OUT[7]	SCB7 RX trigger
40	SCB_I2C_SCL_TR_OUT[7]	SCB7 I ² C trigger
41	SCB_TX_TR_OUT[8]	SCB8 TX trigger
42	SCB_RX_TR_OUT[8]	SCB8 RX trigger
43	SCB_I2C_SCL_TR_OUT[8]	SCB8 I ² C trigger
44	SCB_TX_TR_OUT[9]	SCB9 TX trigger
45	SCB_RX_TR_OUT[9]	SCB9 RX trigger
46	SCB_I2C_SCL_TR_OUT[9]	SCB9 I ² C trigger
47	SCB_TX_TR_OUT[10]	SCB10 TX trigger
48	SCB_RX_TR_OUT[10]	SCB10 RX trigger
49	SCB_I2C_SCL_TR_OUT[10]	SCB10 I ² C trigger
50:55	PASS_GEN_TR_OUT[0:5]	PASS SAR events
56:87	HSIOM_IO_INPUT[0:31]	I/O Inputs
88:89	CTI_TR_IN[0:1]	Trace events
90:93	FAULT_TR_OUT[0:3]	Fault events

触发组输入

表 17-1 触发输入 (续)

Input	Trigger	Description
MUX Group 7: PASS trigger multiplexer		
1:16	PDMA0_TR_OUT[0:15]	General-purpose P-DMA0 triggers
17:28	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
29:36	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
37:38	TCPWM_16_TR_OUT1[60:61]	16-bit TCPWM0 counters
39:46	HSIOM_IO_INPUT[0:7]	I/O Inputs
47:49	EVTGEN_TR_OUT[12:14]	Event generator triggers
MUX Group 8: CAN TT Sync		
1:4	CAN0_TT_TR_OUT[0:3]	CAN0 TT Sync Outputs
5:8	CAN1_TT_TR_OUT[0:3]	CAN1 TT Sync Outputs
MUX Group 9: Debug multiplexer		
1:5	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP11_OUTPUT[0:4]	Output from debug reduction multiplexer #2
11:15	TR_GROUP12_OUTPUT[0:4]	Output from debug reduction multiplexer #3
MUX Group 10: Debug Reduction #1		
1:100	PDMA0_TR_OUT[0:99]	General-purpose P-DMA0 triggers
101:111	SCB_TX_TR_OUT[0:10]	SCB TX triggers
112:122	SCB_RX_TR_OUT[0:10]	SCB RX triggers
123:133	SCB_I2C_SCL_TR_OUT[0:10]	SCB I ² C triggers
134:137	CAN0_DBG_TR_OUT[0:3]	CAN0 DMA
138:141	CAN0_FIFO0_TR_OUT[0:3]	CAN0 FIFO0
142:145	CAN0_FIFO1_TR_OUT[0:3]	CAN0 FIFO1
146:149	CAN0_TT_TR_OUT[0:3]	CAN0 TT Sync Outputs
150:153	CAN1_DBG_TR_OUT[0:3]	CAN1 DMA
154:157	CAN1_FIFO0_TR_OUT[0:3]	CAN1 FIFO0
158:161	CAN1_FIFO1_TR_OUT[0:3]	CAN1 FIFO1
162:165	CAN1_TT_TR_OUT[0:3]	CAN1 TT Sync Outputs
166:167	CTI_TR_OUT[0:1]	Trace events
168:171	FAULT_TR_OUT[0:3]	Fault events
172:187	EVTGEN_TR_OUT[0:15]	EVTGEN Triggers
MUX Group 11: Debug Reduction #2		
1:8	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
9:20	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
21:83	TCPWM_16_TR_OUT0[0:62]	16-bit TCPWM0 counters
84	SMIF_TX_TR_OUT	SMIF TX trigger
85	SMIF_RX_TR_OUT	SMIF RX trigger
86	I2S0_TX_TR_OUT	I ² S0 TX trigger
87	I2S0_RX_TR_OUT	I ² S0 RX trigger
88	I2S1_TX_TR_OUT	I ² S1 TX trigger
89	I2S1_RX_TR_OUT	I ² S1 RX trigger
90	I2S2_TX_TR_OUT	I ² S2 TX trigger
91	I2S2_RX_TR_OUT	I ² S2 RX trigger
92:123	HSIOM_IO_INPUT[0:31]	I/O inputs
MUX Group 12: Debug Reduction #3		
1:58	PDMA1_TR_OUT[0:57]	General-purpose P-DMA1 triggers



触发组输入

表 17-1 触发输入 (续)

Input	Trigger	Description
59:66	MDMA_TR_OUT[0:7]	M-DMA0 triggers
67:129	TCPWM_16_TR_OUT1[0:62]	16-bit TCPWM0 counters
130:141	TCPWM_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM0 counters
142:149	TCPWM_32_TR_OUT1[0:7]	32-bit TCPWM0 counters
150:155	PASS_GEN_TR_OUT[0:5]	PASS SAR events

触发组输出

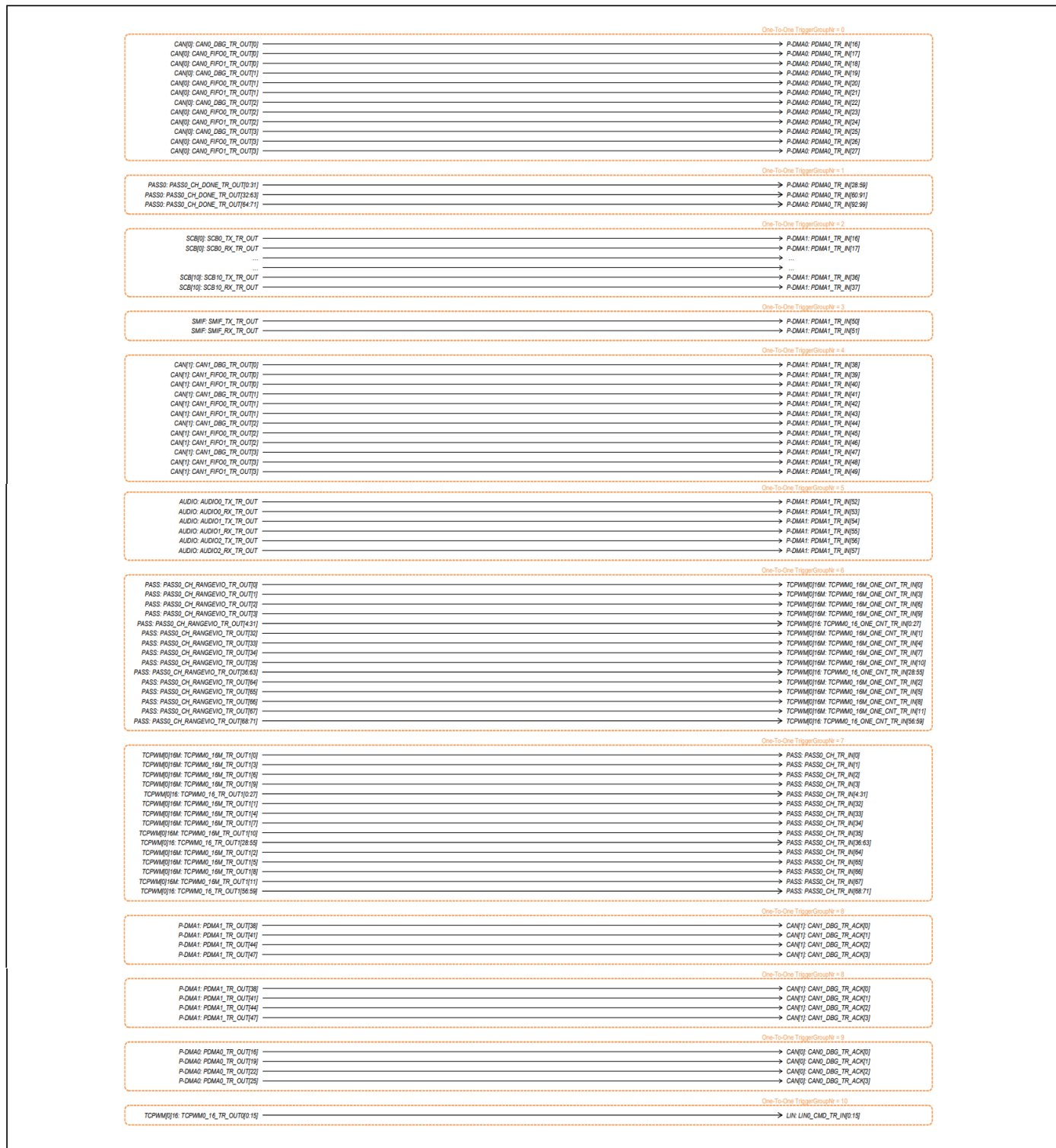
18 触发组输出

表 18-1 触发输出

Output	Trigger	Description
MUX Group 0: P-DMA0 trigger multiplexer		
0:7	PDMA0_TR_IN[0:7]	Triggers to P-DMA0[0:7]
MUX Group 1: TCPWM to P-DMA0 trigger multiplexer		
0:7	PDMA0_TR_IN[8:15]	Triggers to P-DMA0[8:15]
MUX Group 2: P-DMA1 trigger multiplexer		
0:15	PDMA1_TR_IN[0:15]	Triggers to P-DMA1
MUX Group 3: M-DMA0 trigger multiplexer		
0:7	MDMA_TR_IN[0:7]	Triggers to M-DMA0
MUX Group 5: TCPWM0 loop-back multiplexer		
0:11	TCPWM_ALL_CNT_TR_IN[0:11]	Triggers to TCPWM0
MUX Group 6: TCPWM0 Trigger Multiplexer		
0:14	TCPWM_ALL_CNT_TR_IN[12:26]	Triggers to TCPWM0
MUX Group 7: PASS trigger multiplexer		
0:11	PASS_GEN_TR_IN[0:11]	Triggers to SAR ADCs
MUX Group 8: CAN TT Sync		
0:3	CAN0_TT_TR_IN[0:3]	CAN0 TT Sync Inputs
4:7	CAN1_TT_TR_IN[0:3]	CAN1 TT Sync Inputs
MUX Group 9: Debug multiplexer		
0	HSIOM_IO_OUTPUT[0]	To HSIOM as an output
1	HSIOM_IO_OUTPUT[1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To the Cross Trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze PASS operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
7	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[2]	Signal to Freeze MCWDT2 operation
8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1]	Signal to Freeze MCWDT1 operation
9	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0]	Signal to Freeze MCWDT0 operation
10	TCPWM_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM0 operation
MUX Group 10: Debug Reduction #1		
0:4	TR_GROUP9_INPUT[1:5]	To main debug multiplexer
MUX Group 11: Debug Reduction #2		
0:4	TR_GROUP9_INPUT[6:10]	To main debug multiplexer
MUX Group 12: Debug Reduction #3		
0:4	TR_GROUP9_INPUT[11:15]	To main debug multiplexer

一对一触发器

19 一对一触发器


图 19-1 一对一触发器^[36]

注：

36. 该图仅显示TRIG_LABEL；最终触发形成基于公式 $\text{TRIG_}\{\text{PREFIX}(\text{IN_1TO1}/\text{OUT_1- TO1})\}_{\{x\}}_{\{\text{TRIG_LABEL}\}}$ 和表 19-1 中提供的信息。



一对一触发器

表 19-1 一对一触发器

Input	Trigger in	Trigger out	Description
MUX Group 0: CAN0 to P-DMA0 Triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[16]	CAN0, Channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[17]	CAN0, Channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[18]	CAN0, Channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[19]	CAN0, Channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[20]	CAN0, Channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[21]	CAN0, Channel #1 FIFO1 trigger
6	CAN0_DBG_TR_OUT[2]	PDMA0_TR_IN[22]	CAN0, Channel #2 P-DMA0 trigger
7	CAN0_FIFO0_TR_OUT[2]	PDMA0_TR_IN[23]	CAN0, Channel #2 FIFO0 trigger
8	CAN0_FIFO1_TR_OUT[2]	PDMA0_TR_IN[24]	CAN0, Channel #2 FIFO1 trigger
9	CAN0_DBG_TR_OUT[3]	PDMA0_TR_IN[25]	CAN0, Channel #3 P-DMA0 trigger
10	CAN0_FIFO0_TR_OUT[3]	PDMA0_TR_IN[26]	CAN0, Channel #3 FIFO0 trigger
11	CAN0_FIFO1_TR_OUT[3]	PDMA0_TR_IN[27]	CAN0, Channel #3 FIFO1 trigger
MUX Group 1: PASS SARx to P-DMA0 direct connect			
0:31	PASS0_CH_DONE_TR_OUT[0:31]	PDMA0_TR_IN[28:59]	PASS SAR0 [0:31] to P-DMA0 direct connect
32:63	PASS0_CH_DONE_TR_OUT[32:63]	PDMA0_TR_IN[60:91]	PASS SAR1 [0:31] to P-DMA0 direct connect
64:71	PASS0_CH_DONE_TR_OUT[64:71]	PDMA0_TR_IN[92:99]	PASS SAR2 [0:7] to P-DMA0 direct connect
MUX Group 2: SCBx to P-DMA1 Triggers			
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[16]	SCB0 to P-DMA1 Trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[17]	SCB0 to P-DMA1 Trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[18]	SCB1 to P-DMA1 Trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[19]	SCB1 to P-DMA1 Trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[20]	SCB2 to P-DMA1 Trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[21]	SCB2 to P-DMA1 Trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[22]	SCB3 to P-DMA1 Trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[23]	SCB3 to P-DMA1 Trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[24]	SCB4 to P-DMA1 Trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[25]	SCB4 to P-DMA1 Trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[26]	SCB5 to P-DMA1 Trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[27]	SCB5 to P-DMA1 Trigger
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[28]	SCB6 to P-DMA1 Trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[29]	SCB6 to P-DMA1 Trigger
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[30]	SCB7 to P-DMA1 Trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[31]	SCB7 to P-DMA1 Trigger
16	SCB8_TX_TR_OUT	PDMA1_TR_IN[32]	SCB8 to P-DMA1 Trigger
17	SCB8_RX_TR_OUT	PDMA1_TR_IN[33]	SCB8 to P-DMA1 Trigger
18	SCB9_TX_TR_OUT	PDMA1_TR_IN[34]	SCB9 to P-DMA1 Trigger
19	SCB9_RX_TR_OUT	PDMA1_TR_IN[35]	SCB9 to P-DMA1 Trigger
20	SCB10_TX_TR_OUT	PDMA1_TR_IN[36]	SCB10 to P-DMA1 Trigger
21	SCB10_RX_TR_OUT	PDMA1_TR_IN[37]	SCB10 to P-DMA1 Trigger
MUX Group 3: SMIF0 to P-DMA1 Triggers			
0	SMIF_TX_TR_OUT	PDMA1_TR_IN[50]	SMIF0 to P-DMA1 Trigger
1	SMIF_RX_TR_OUT	PDMA1_TR_IN[51]	SMIF0 to P-DMA1 Trigger
MUX Group 4: CAN1 to P-DMA1 triggers			
0	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[38]	CAN1 Channel #0 P-DMA1 trigger
1	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[39]	CAN1 Channel #0 FIFO0 trigger
2	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[40]	CAN1 Channel #0 FIFO1 trigger
3	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[41]	CAN1 Channel #1 P-DMA1 trigger
4	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[42]	CAN1 Channel #1 FIFO0 trigger

一对一触发器

表 19-1 一对一触发器 (续)

Input	Trigger in	Trigger out	Description
5	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[43]	CAN1 Channel #1 FIFO1 trigger
6	CAN1_DBG_TR_OUT[2]	PDMA1_TR_IN[44]	CAN1 Channel #2 P-DMA1 trigger
7	CAN1_FIFO0_TR_OUT[2]	PDMA1_TR_IN[45]	CAN1 Channel #2 FIFO0 trigger
8	CAN1_FIFO1_TR_OUT[2]	PDMA1_TR_IN[46]	CAN1 Channel #2 FIFO1 trigger
9	CAN1_DBG_TR_OUT[3]	PDMA1_TR_IN[47]	CAN1 Channel #3 P-DMA1 trigger
10	CAN1_FIFO0_TR_OUT[3]	PDMA1_TR_IN[48]	CAN1 Channel #3 FIFO0 trigger
11	CAN1_FIFO1_TR_OUT[3]	PDMA1_TR_IN[49]	CAN1 Channel #3 FIFO1 trigger
MUX Group 5: I²Sx to P-DMA1 Triggers			
0	AUDIO0_TX_TR_OUT	PDMA1_TR_IN[52]	I ² S0 TX to P-DMA1 trigger
1	AUDIO0_RX_TR_OUT	PDMA1_TR_IN[53]	I ² S0 RX to P-DMA1 trigger
2	AUDIO1_TX_TR_OUT	PDMA1_TR_IN[54]	I ² S1 TX to P-DMA1 trigger
3	AUDIO1_RX_TR_OUT	PDMA1_TR_IN[55]	I ² S1 RX to P-DMA1 trigger
4	AUDIO2_TX_TR_OUT	PDMA1_TR_IN[56]	I ² S2 TX to P-DMA1 trigger
5	AUDIO2_RX_TR_OUT	PDMA1_TR_IN[57]	I ² S2 RX to P-DMA1 trigger
MUX Group 6: PASS SARx to TCPWM0 direct connect			
0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#0 ^[37] , range violation to TCPWM0 Group #1 Counter #00 trig = 4
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#1, range violation to TCPWM0 Group #1 Counter #03 trig = 4
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#2, range violation to TCPWM0 Group #1 Counter #06 trig = 4
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#3, range violation to TCPWM0 Group #1 Counter #09 trig = 4
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#4, range violation to TCPWM0 Group #0 Counter #00 trig = 4
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR0 ch#5, range violation to TCPWM0 Group #0 Counter #01 trig = 4
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR0 ch#6, range violation to TCPWM0 Group #0 Counter #02 trig = 4
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#7, range violation to TCPWM0 Group #0 Counter #03 trig = 4
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR0 ch#8, range violation to TCPWM0 Group #0 Counter #04 trig = 4
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR0 ch#9, range violation to TCPWM0 Group #0 Counter #05 trig = 4
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#10, range violation to TCPWM0 Group #0 Counter #06 trig = 4
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR0 ch#11, range violation to TCPWM0 Group #0 Counter #07 trig = 4
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR0 ch#12, range violation to TCPWM0 Group #0 Counter #08 trig = 4
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#13, range violation to TCPWM0 Group #0 Counter #09 trig = 4
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR0 ch#14, range violation to TCPWM0 Group #0 Counter #10 trig = 4
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR0 ch#15, range violation to TCPWM0 Group #0 Counter #11 trig = 4
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16M_ONE_CNT_TR_IN[12]	SAR0 ch#16, range violation to TCPWM0 Group #0 Counter #12 trig = 4
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16M_ONE_CNT_TR_IN[13]	SAR0 ch#17, range violation to TCPWM0 Group #0 Counter #13 trig = 4
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16M_ONE_CNT_TR_IN[14]	SAR0 ch#18, range violation to TCPWM0 Group #0 Counter #14 trig = 4
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16M_ONE_CNT_TR_IN[15]	SAR0 ch#19, range violation to TCPWM0 Group #0 Counter #15 trig = 4
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16M_ONE_CNT_TR_IN[16]	SAR0 ch#20, range violation to TCPWM0 Group #0 Counter #16 trig = 4
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16M_ONE_CNT_TR_IN[17]	SAR0 ch#21, range violation to TCPWM0 Group #0 Counter #17 trig = 4

注:

37. SAR ADC[x] 的每个逻辑通道都可以连接到任意 SAR ADC[x]_y 外部引脚。(x=0, 或 1, 或 2 且 y=0 到 31)。



一对一触发器

表 19-1 一对一触发器 (续)

Input	Trigger in	Trigger out	Description
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#22, range violation to TCPWM0 Group #0 Counter #18 trig = 4
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#23, range violation to TCPWM0 Group #0 Counter #19 trig = 4
24	PASS0_CH_RANGEVIO_TR_OUT[24]	TCPWM0_16_ONE_CNT_TR_IN[20]	SAR0 ch#24, range violation to TCPWM0 Group #0 Counter #20 trig = 4
25	PASS0_CH_RANGEVIO_TR_OUT[25]	TCPWM0_16_ONE_CNT_TR_IN[21]	SAR0 ch#25, range violation to TCPWM0 Group #0 Counter #21 trig = 4
26	PASS0_CH_RANGEVIO_TR_OUT[26]	TCPWM0_16_ONE_CNT_TR_IN[22]	SAR0 ch#26, range violation to TCPWM0 Group #0 Counter #22 trig = 4
27	PASS0_CH_RANGEVIO_TR_OUT[27]	TCPWM0_16_ONE_CNT_TR_IN[23]	SAR0 ch#27, range violation to TCPWM0 Group #0 Counter #23 trig = 4
28	PASS0_CH_RANGEVIO_TR_OUT[28]	TCPWM0_16_ONE_CNT_TR_IN[24]	SAR0 ch#28, range violation to TCPWM0 Group #0 Counter #24 trig = 4
29	PASS0_CH_RANGEVIO_TR_OUT[29]	TCPWM0_16_ONE_CNT_TR_IN[25]	SAR0 ch#29, range violation to TCPWM0 Group #0 Counter #25 trig = 4
30	PASS0_CH_RANGEVIO_TR_OUT[30]	TCPWM0_16_ONE_CNT_TR_IN[26]	SAR0 ch#30, range violation to TCPWM0 Group #0 Counter #26 trig = 4
31	PASS0_CH_RANGEVIO_TR_OUT[31]	TCPWM0_16_ONE_CNT_TR_IN[27]	SAR0 ch#31, range violation to TCPWM0 Group #0 Counter #27 trig = 4
32	PASS0_CH_RANGEVIO_TR_OUT[32]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR1 ch#0, range violation to TCPWM0 Group #1 Counter #01 trig = 4
33	PASS0_CH_RANGEVIO_TR_OUT[33]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR1 ch#1, range violation to TCPWM0 Group #1 Counter #04 trig = 4
34	PASS0_CH_RANGEVIO_TR_OUT[34]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR1 ch#2, range violation to TCPWM0 Group #1 Counter #07 trig = 4
35	PASS0_CH_RANGEVIO_TR_OUT[35]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR1 ch#3, range violation to TCPWM0 Group #1 Counter #10 trig = 4
36	PASS0_CH_RANGEVIO_TR_OUT[36]	TCPWM0_16_ONE_CNT_TR_IN[28]	SAR1 ch#4, range violation to TCPWM0 Group #0 Counter #28 trig = 4
37	PASS0_CH_RANGEVIO_TR_OUT[37]	TCPWM0_16_ONE_CNT_TR_IN[29]	SAR1 ch#5, range violation to TCPWM0 Group #0 Counter #29 trig = 4
38	PASS0_CH_RANGEVIO_TR_OUT[38]	TCPWM0_16_ONE_CNT_TR_IN[30]	SAR1 ch#6, range violation to TCPWM0 Group #0 Counter #30 trig = 4
39	PASS0_CH_RANGEVIO_TR_OUT[39]	TCPWM0_16_ONE_CNT_TR_IN[31]	SAR1 ch#7, range violation to TCPWM0 Group #0 Counter #31 trig = 4
40	PASS0_CH_RANGEVIO_TR_OUT[40]	TCPWM0_16_ONE_CNT_TR_IN[32]	SAR1 ch#8, range violation to TCPWM0 Group #0 Counter #32 trig = 4
41	PASS0_CH_RANGEVIO_TR_OUT[41]	TCPWM0_16_ONE_CNT_TR_IN[33]	SAR1 ch#9, range violation to TCPWM0 Group #0 Counter #33 trig = 4
42	PASS0_CH_RANGEVIO_TR_OUT[42]	TCPWM0_16_ONE_CNT_TR_IN[34]	SAR1 ch#10, range violation to TCPWM0 Group #0 Counter #34 trig = 4
43	PASS0_CH_RANGEVIO_TR_OUT[43]	TCPWM0_16_ONE_CNT_TR_IN[35]	SAR1 ch#11, range violation to TCPWM0 Group #0 Counter #35 trig = 4
44	PASS0_CH_RANGEVIO_TR_OUT[44]	TCPWM0_16_ONE_CNT_TR_IN[36]	SAR1 ch#12, range violation to TCPWM0 Group #0 Counter #36 trig = 4
45	PASS0_CH_RANGEVIO_TR_OUT[45]	TCPWM0_16_ONE_CNT_TR_IN[37]	SAR1 ch#13, range violation to TCPWM0 Group #0 Counter #37 trig = 4
46	PASS0_CH_RANGEVIO_TR_OUT[46]	TCPWM0_16_ONE_CNT_TR_IN[38]	SAR1 ch#14, range violation to TCPWM0 Group #0 Counter #38 trig = 4
47	PASS0_CH_RANGEVIO_TR_OUT[47]	TCPWM0_16_ONE_CNT_TR_IN[39]	SAR1 ch#15, range violation to TCPWM0 Group #0 Counter #39 trig = 4
48	PASS0_CH_RANGEVIO_TR_OUT[48]	TCPWM0_16_ONE_CNT_TR_IN[40]	SAR1 ch#16, range violation to TCPWM0 Group #0 Counter #40 trig = 4
49	PASS0_CH_RANGEVIO_TR_OUT[49]	TCPWM0_16_ONE_CNT_TR_IN[41]	SAR1 ch#17, range violation to TCPWM0 Group #0 Counter #41 trig = 4
50	PASS0_CH_RANGEVIO_TR_OUT[50]	TCPWM0_16_ONE_CNT_TR_IN[42]	SAR1 ch#18, range violation to TCPWM0 Group #0 Counter #42 trig = 4
51	PASS0_CH_RANGEVIO_TR_OUT[51]	TCPWM0_16_ONE_CNT_TR_IN[43]	SAR1 ch#19, range violation to TCPWM0 Group #0 Counter #43 trig = 4
52	PASS0_CH_RANGEVIO_TR_OUT[52]	TCPWM0_16_ONE_CNT_TR_IN[44]	SAR1 ch#20, range violation to TCPWM0 Group #0 Counter #44 trig = 4
53	PASS0_CH_RANGEVIO_TR_OUT[53]	TCPWM0_16_ONE_CNT_TR_IN[45]	SAR1 ch#21, range violation to TCPWM0 Group #0 Counter #45 trig = 4
54	PASS0_CH_RANGEVIO_TR_OUT[54]	TCPWM0_16_ONE_CNT_TR_IN[46]	SAR1 ch#22, range violation to TCPWM0 Group #0 Counter #46 trig = 4
55	PASS0_CH_RANGEVIO_TR_OUT[55]	TCPWM0_16_ONE_CNT_TR_IN[47]	SAR1 ch#23, range violation to TCPWM0 Group #0 Counter #47 trig = 4



一对一触发器

表 19-1 一对一触发器 (续)

Input	Trigger in	Trigger out	Description
56	PASS0_CH_RANGEVIO_TR_OUT[56]	TCPWM0_16_ONE_CNT_TR_IN[48]	SAR1 ch#24, range violation to TCPWM0 Group #0 Counter #48 trig = 4
57	PASS0_CH_RANGEVIO_TR_OUT[57]	TCPWM0_16_ONE_CNT_TR_IN[49]	SAR1 ch#25, range violation to TCPWM0 Group #0 Counter #49 trig = 4
58	PASS0_CH_RANGEVIO_TR_OUT[58]	TCPWM0_16_ONE_CNT_TR_IN[50]	SAR1 ch#26, range violation to TCPWM0 Group #0 Counter #50 trig = 4
59	PASS0_CH_RANGEVIO_TR_OUT[59]	TCPWM0_16_ONE_CNT_TR_IN[51]	SAR1 ch#27, range violation to TCPWM0 Group #0 Counter #51 trig = 4
60	PASS0_CH_RANGEVIO_TR_OUT[60]	TCPWM0_16_ONE_CNT_TR_IN[52]	SAR1 ch#28, range violation to TCPWM0 Group #0 Counter #52 trig = 4
61	PASS0_CH_RANGEVIO_TR_OUT[61]	TCPWM0_16_ONE_CNT_TR_IN[53]	SAR1 ch#29, range violation to TCPWM0 Group #0 Counter #53 trig = 4
62	PASS0_CH_RANGEVIO_TR_OUT[62]	TCPWM0_16_ONE_CNT_TR_IN[54]	SAR1 ch#30, range violation to TCPWM0 Group #0 Counter #54 trig = 4
63	PASS0_CH_RANGEVIO_TR_OUT[63]	TCPWM0_16_ONE_CNT_TR_IN[55]	SAR1 ch#31, range violation to TCPWM0 Group #0 Counter #55 trig = 4
64	PASS0_CH_RANGEVIO_TR_OUT[64]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR2 ch#0, range violation to TCPWM0 Group #1 Counter #02 trig = 4
65	PASS0_CH_RANGEVIO_TR_OUT[65]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR2 ch#1, range violation to TCPWM0 Group #1 Counter #05 trig = 4
66	PASS0_CH_RANGEVIO_TR_OUT[66]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR2 ch#2, range violation to TCPWM0 Group #1 Counter #08 trig = 4
67	PASS0_CH_RANGEVIO_TR_OUT[67]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR2 ch#3, range violation to TCPWM0 Group #1 Counter #11 trig = 4
68	PASS0_CH_RANGEVIO_TR_OUT[68]	TCPWM0_16_ONE_CNT_TR_IN[56]	SAR2 ch#4, range violation to TCPWM0 Group #0 Counter #56 trig = 4
69	PASS0_CH_RANGEVIO_TR_OUT[69]	TCPWM0_16_ONE_CNT_TR_IN[57]	SAR2 ch#5, range violation to TCPWM0 Group #0 Counter #57 trig = 4
70	PASS0_CH_RANGEVIO_TR_OUT[70]	TCPWM0_16_ONE_CNT_TR_IN[58]	SAR2 ch#6, range violation to TCPWM0 Group #0 Counter #58 trig = 4
71	PASS0_CH_RANGEVIO_TR_OUT[71]	TCPWM0_16_ONE_CNT_TR_IN[59]	SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #59 trig = 4
MUX Group 7: TCPWM0 to PASS SARx			
0	TCPWM0_16M_TR_OUT1[0]	PASS0_CH_TR_IN[0]	TCPWM0 Group #1 Counter #00 (PWM0_M_0) to SAR0 ch#0
1	TCPWM0_16M_TR_OUT1[3]	PASS0_CH_TR_IN[1]	TCPWM0 Group #1 Counter #03 (PWM0_M_3) to SAR0 ch#1
2	TCPWM0_16M_TR_OUT1[6]	PASS0_CH_TR_IN[2]	TCPWM0 Group #1 Counter #06 (PWM0_M_6) to SAR0 ch#2
3	TCPWM0_16M_TR_OUT1[9]	PASS0_CH_TR_IN[3]	TCPWM0 Group #1 Counter #09 (PWM0_M_9) to SAR0 ch#3
4:31	TCPWM0_16_TR_OUT1[0:27]	PASS0_CH_TR_IN[4:31]	TCPWM0 Group #0 Counter #00 through 27 (PWM0_0 to PWM0_27) to SAR0 ch#4 through SAR0 ch#31
32	TCPWM0_16M_TR_OUT1[1]	PASS0_CH_TR_IN[32]	TCPWM0 Group #1 Counter #01 (PWM0_M_1) to SAR1 ch#0
33	TCPWM0_16M_TR_OUT1[4]	PASS0_CH_TR_IN[33]	TCPWM0 Group #1 Counter #04 (PWM0_M_4) to SAR1 ch#1
34	TCPWM0_16M_TR_OUT1[7]	PASS0_CH_TR_IN[34]	TCPWM0 Group #1 Counter #07 (PWM0_M_7) to SAR1 ch#2
35	TCPWM0_16M_TR_OUT1[10]	PASS0_CH_TR_IN[35]	TCPWM0 Group #1 Counter #10 (PWM0_M_10) to SAR1 ch#3
36:63	TCPWM0_16_TR_OUT1[28:55]	PASS0_CH_TR_IN[36:63]	TCPWM0 Group #0 Counter #28 through 55 (PWM0_28 to PWM0_55) to SAR1 ch#4 through SAR1 ch#31
64	TCPWM0_16M_TR_OUT1[2]	PASS0_CH_TR_IN[64]	TCPWM0 Group #1 Counter #02 (PWM0_M_2) to SAR2 ch#0
65	TCPWM0_16M_TR_OUT1[5]	PASS0_CH_TR_IN[65]	TCPWM0 Group #1 Counter #05 (PWM0_M_5) to SAR2 ch#1
66	TCPWM0_16M_TR_OUT1[8]	PASS0_CH_TR_IN[66]	TCPWM0 Group #1 Counter #08 (PWM0_M_8) to SAR2 ch#2
67	TCPWM0_16M_TR_OUT1[11]	PASS0_CH_TR_IN[67]	TCPWM0 Group #1 Counter #11 (PWM0_M_11) to SAR2 ch#3
68:71	TCPWM0_16_TR_OUT1[56:59]	PASS0_CH_TR_IN[68:71]	TCPWM0 Group #0 Counter #56 through 59 (PWM0_56 to PWM0_59) to SAR2 ch#4 through SAR2 ch#7
MUX Group 8: Acknowledge triggers from P-DMA1 to CAN1			
0	PDMA1_TR_OUT[38]	CAN1_DBG_TR_ACK[0]	CAN1 Channel#0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[41]	CAN1_DBG_TR_ACK[1]	CAN1 Channel#1 P-DMA1 acknowledge



一对一触发器

表 19-1 一对一触发器 (续)

Input	Trigger in	Trigger out	Description
2	PDMA1_TR_OUT[44]	CAN1_DBG_TR_ACK[2]	CAN1 Channel#2 P-DMA1 acknowledge
3	PDMA1_TR_OUT[47]	CAN1_DBG_TR_ACK[3]	CAN1 Channel#3 P-DMA1 acknowledge
MUX Group 9: Acknowledge triggers from P-DMA0 to CAN0			
0	PDMA0_TR_OUT[32]	CAN0_DBG_TR_ACK[0]	CAN0 Channel#0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[35]	CAN0_DBG_TR_ACK[1]	CAN0 Channel#1 P-DMA0 acknowledge
2	PDMA0_TR_OUT[38]	CAN0_DBG_TR_ACK[2]	CAN0 Channel#2 P-DMA0 acknowledge
3	PDMA0_TR_OUT[41]	CAN0_DBG_TR_ACK[3]	CAN0 Channel#3 P-DMA0 acknowledge
MUX Group 10: TCPWM0 to LIN0 triggers			
0:15	TCPWM0_16_TR_OUT0[0:15]	LIN0_CMD_TR_IN[0:15]	TCPWM0 (Group #0 Counter #00 to #15) to LIN0



外设时钟

20 外设时钟

表 20-1 外设时钟分配

Output	Destination	Description
CPUSS root clocks (Group 0)		
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO12_CLOCK	Smart I/O #12
2	PCLK_SMARTIO13_CLOCK	Smart I/O #13
3	PCLK_SMARTIO14_CLOCK	Smart I/O #14
4	PCLK_SMARTIO15_CLOCK	Smart I/O #15
5	PCLK_SMARTIO17_CLOCK	Smart I/O #17
COMM root clocks (Group 1)		
0	PCLK_CANFD0_CLOCK_CAN0	CAN0, Channel #0
1	PCLK_CANFD0_CLOCK_CAN1	CAN0, Channel #1
2	PCLK_CANFD0_CLOCK_CAN2	CAN0, Channel #2
3	PCLK_CANFD0_CLOCK_CAN3	CAN0, Channel #3
4	PCLK_CANFD1_CLOCK_CAN0	CAN1, Channel #0
5	PCLK_CANFD1_CLOCK_CAN1	CAN1, Channel #1
6	PCLK_CANFD1_CLOCK_CAN2	CAN1, Channel #2
7	PCLK_CANFD1_CLOCK_CAN3	CAN1, Channel #3
8	PCLK_LIN0_CLOCK_CH_EN0	LIN0, Channel #0
9	PCLK_LIN0_CLOCK_CH_EN1	LIN0, Channel #1
10	PCLK_LIN0_CLOCK_CH_EN2	LIN0, Channel #2
11	PCLK_LIN0_CLOCK_CH_EN3	LIN0, Channel #3
12	PCLK_LIN0_CLOCK_CH_EN4	LIN0, Channel #4
13	PCLK_LIN0_CLOCK_CH_EN5	LIN0, Channel #5
14	PCLK_LIN0_CLOCK_CH_EN6	LIN0, Channel #6
15	PCLK_LIN0_CLOCK_CH_EN7	LIN0, Channel #7
16	PCLK_LIN0_CLOCK_CH_EN8	LIN0, Channel #8
17	PCLK_LIN0_CLOCK_CH_EN9	LIN0, Channel #9
18	PCLK_LIN0_CLOCK_CH_EN10	LIN0, Channel #10
19	PCLK_LIN0_CLOCK_CH_EN11	LIN0, Channel #11
20	PCLK_LIN0_CLOCK_CH_EN12	LIN0, Channel #12
21	PCLK_LIN0_CLOCK_CH_EN13	LIN0, Channel #13
22	PCLK_LIN0_CLOCK_CH_EN14	LIN0, Channel #14
23	PCLK_LIN0_CLOCK_CH_EN15	LIN0, Channel #15
24	PCLK_SCB0_CLOCK	SCB0
25	PCLK_SCB1_CLOCK	SCB1
26	PCLK_SCB2_CLOCK	SCB2
27	PCLK_SCB3_CLOCK	SCB3
28	PCLK_SCB4_CLOCK	SCB4
29	PCLK_SCB5_CLOCK	SCB5
30	PCLK_SCB6_CLOCK	SCB6
31	PCLK_SCB7_CLOCK	SCB7
32	PCLK_SCB8_CLOCK	SCB8



外设时钟

表 20-1 外设时钟分配 (续)

Output	Destination	Description
33	PCLK_SCB9_CLOCK	SCB9
34	PCLK_SCB10_CLOCK	SCB10
35	PCLK_PASS0_CLOCK_SAR0	SAR0
36	PCLK_PASS0_CLOCK_SAR1	SAR1
37	PCLK_PASS0_CLOCK_SAR2	SAR2
38	PCLK_TCPWM0_CLOCKS0	TCPWM0 Group #0, Counter #0
39	PCLK_TCPWM0_CLOCKS1	TCPWM0 Group #0, Counter #1
40	PCLK_TCPWM0_CLOCKS2	TCPWM0 Group #0, Counter #2
41	PCLK_TCPWM0_CLOCKS3	TCPWM0 Group #0, Counter #3
42	PCLK_TCPWM0_CLOCKS4	TCPWM0 Group #0, Counter #4
43	PCLK_TCPWM0_CLOCKS5	TCPWM0 Group #0, Counter #5
44	PCLK_TCPWM0_CLOCKS6	TCPWM0 Group #0, Counter #6
45	PCLK_TCPWM0_CLOCKS7	TCPWM0 Group #0, Counter #7
46	PCLK_TCPWM0_CLOCKS8	TCPWM0 Group #0, Counter #8
47	PCLK_TCPWM0_CLOCKS9	TCPWM0 Group #0, Counter #9
48	PCLK_TCPWM0_CLOCKS10	TCPWM0 Group #0, Counter #10
49	PCLK_TCPWM0_CLOCKS11	TCPWM0 Group #0, Counter #11
50	PCLK_TCPWM0_CLOCKS12	TCPWM0 Group #0, Counter #12
51	PCLK_TCPWM0_CLOCKS13	TCPWM0 Group #0, Counter #13
52	PCLK_TCPWM0_CLOCKS14	TCPWM0 Group #0, Counter #14
53	PCLK_TCPWM0_CLOCKS15	TCPWM0 Group #0, Counter #15
54	PCLK_TCPWM0_CLOCKS16	TCPWM0 Group #0, Counter #16
55	PCLK_TCPWM0_CLOCKS17	TCPWM0 Group #0, Counter #17
56	PCLK_TCPWM0_CLOCKS18	TCPWM0 Group #0, Counter #18
57	PCLK_TCPWM0_CLOCKS19	TCPWM0 Group #0, Counter #19
58	PCLK_TCPWM0_CLOCKS20	TCPWM0 Group #0, Counter #20
59	PCLK_TCPWM0_CLOCKS21	TCPWM0 Group #0, Counter #21
60	PCLK_TCPWM0_CLOCKS22	TCPWM0 Group #0, Counter #22
61	PCLK_TCPWM0_CLOCKS23	TCPWM0 Group #0, Counter #23
62	PCLK_TCPWM0_CLOCKS24	TCPWM0 Group #0, Counter #24
63	PCLK_TCPWM0_CLOCKS25	TCPWM0 Group #0, Counter #25
64	PCLK_TCPWM0_CLOCKS26	TCPWM0 Group #0, Counter #26
65	PCLK_TCPWM0_CLOCKS27	TCPWM0 Group #0, Counter #27
66	PCLK_TCPWM0_CLOCKS28	TCPWM0 Group #0, Counter #28
67	PCLK_TCPWM0_CLOCKS29	TCPWM0 Group #0, Counter #29
68	PCLK_TCPWM0_CLOCKS30	TCPWM0 Group #0, Counter #30
69	PCLK_TCPWM0_CLOCKS31	TCPWM0 Group #0, Counter #31
70	PCLK_TCPWM0_CLOCKS32	TCPWM0 Group #0, Counter #32
71	PCLK_TCPWM0_CLOCKS33	TCPWM0 Group #0, Counter #33
72	PCLK_TCPWM0_CLOCKS34	TCPWM0 Group #0, Counter #34
73	PCLK_TCPWM0_CLOCKS35	TCPWM0 Group #0, Counter #35
74	PCLK_TCPWM0_CLOCKS36	TCPWM0 Group #0, Counter #36



外设时钟

表 20-1 外设时钟分配 (续)

Output	Destination	Description
75	PCLK_TCPWM0_CLOCKS37	TCPWM0 Group #0, Counter #37
76	PCLK_TCPWM0_CLOCKS38	TCPWM0 Group #0, Counter #38
77	PCLK_TCPWM0_CLOCKS39	TCPWM0 Group #0, Counter #39
78	PCLK_TCPWM0_CLOCKS40	TCPWM0 Group #0, Counter #40
79	PCLK_TCPWM0_CLOCKS41	TCPWM0 Group #0, Counter #41
80	PCLK_TCPWM0_CLOCKS42	TCPWM0 Group #0, Counter #42
81	PCLK_TCPWM0_CLOCKS43	TCPWM0 Group #0, Counter #43
82	PCLK_TCPWM0_CLOCKS44	TCPWM0 Group #0, Counter #44
83	PCLK_TCPWM0_CLOCKS45	TCPWM0 Group #0, Counter #45
84	PCLK_TCPWM0_CLOCKS46	TCPWM0 Group #0, Counter #46
85	PCLK_TCPWM0_CLOCKS47	TCPWM0 Group #0, Counter #47
86	PCLK_TCPWM0_CLOCKS48	TCPWM0 Group #0, Counter #48
87	PCLK_TCPWM0_CLOCKS49	TCPWM0 Group #0, Counter #49
88	PCLK_TCPWM0_CLOCKS50	TCPWM0 Group #0, Counter #50
89	PCLK_TCPWM0_CLOCKS51	TCPWM0 Group #0, Counter #51
90	PCLK_TCPWM0_CLOCKS52	TCPWM0 Group #0, Counter #52
91	PCLK_TCPWM0_CLOCKS53	TCPWM0 Group #0, Counter #53
92	PCLK_TCPWM0_CLOCKS54	TCPWM0 Group #0, Counter #54
93	PCLK_TCPWM0_CLOCKS55	TCPWM0 Group #0, Counter #55
94	PCLK_TCPWM0_CLOCKS56	TCPWM0 Group #0, Counter #56
95	PCLK_TCPWM0_CLOCKS57	TCPWM0 Group #0, Counter #57
96	PCLK_TCPWM0_CLOCKS58	TCPWM0 Group #0, Counter #58
97	PCLK_TCPWM0_CLOCKS59	TCPWM0 Group #0, Counter #59
98	PCLK_TCPWM0_CLOCKS60	TCPWM0 Group #0, Counter #60
99	PCLK_TCPWM0_CLOCKS61	TCPWM0 Group #0, Counter #61
100	PCLK_TCPWM0_CLOCKS62	TCPWM0 Group #0, Counter #62
101	PCLK_TCPWM0_CLOCKS256	TCPWM0 Group #1, Counter #0
102	PCLK_TCPWM0_CLOCKS257	TCPWM0 Group #1, Counter #1
103	PCLK_TCPWM0_CLOCKS258	TCPWM0 Group #1, Counter #2
104	PCLK_TCPWM0_CLOCKS259	TCPWM0 Group #1, Counter #3
105	PCLK_TCPWM0_CLOCKS260	TCPWM0 Group #1, Counter #4
106	PCLK_TCPWM0_CLOCKS261	TCPWM0 Group #1, Counter #5
107	PCLK_TCPWM0_CLOCKS262	TCPWM0 Group #1, Counter #6
108	PCLK_TCPWM0_CLOCKS263	TCPWM0 Group #1, Counter #7
109	PCLK_TCPWM0_CLOCKS264	TCPWM0 Group #1, Counter #8
110	PCLK_TCPWM0_CLOCKS265	TCPWM0 Group #1, Counter #9
111	PCLK_TCPWM0_CLOCKS266	TCPWM0 Group #1, Counter #10
112	PCLK_TCPWM0_CLOCKS267	TCPWM0 Group #1, Counter #11
113	PCLK_TCPWM0_CLOCKS512	TCPWM0 Group #2, Counter #0
114	PCLK_TCPWM0_CLOCKS513	TCPWM0 Group #2, Counter #1
115	PCLK_TCPWM0_CLOCKS514	TCPWM0 Group #2, Counter #2
116	PCLK_TCPWM0_CLOCKS515	TCPWM0 Group #2, Counter #3



外设时钟

表 20-1 外设时钟分配 (续)

Output	Destination	Description
117	PCLK_TCPWM0_CLOCKS516	TCPWM0 Group #2, Counter #4
118	PCLK_TCPWM0_CLOCKS517	TCPWM0 Group #2, Counter #5
119	PCLK_TCPWM0_CLOCKS518	TCPWM0 Group #2, Counter #6
120	PCLK_TCPWM0_CLOCKS519	TCPWM0 Group #2, Counter #7

故障

21 故障

表 21-1 故障分配

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ SMPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0': MPU violation; '1': SMPU violation.
1	CPUSS_MPU_VIO_1	CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
5	CPUSS_MPU_VIO_5	SDHC MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
9	CPUSS_MPU_VIO_6	Ethernet0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
13	CPUSS_MPU_VIO_13	CM7_1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
14	CPUSS_MPU_VIO_14	CM7_0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_CM7_1_TCM_C_ECC	Correctable ECC error in CM7_1 TCM memory DATA0[23:2]: Violating address. DATA1[7:0]: Syndrome of code word (at address offset 0x0). DATA1[31:30]: 0=ITCM, 2=D0TCM, 3=D1TCM
17	CPUSS_CM7_1_TCM_NC_ECC	Non Correctable ECC error in CM7_1 TCM memory. See CPUSS_CM7_1_TCM_C_ECC description.
18	CPUSS_CM7_0_CACHE_C_ECC	Correctable ECC error in CM7_0 Cache memories DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details. DATA0[31]: 0=Instruction cache, 1= Data cache
19	CPUSS_CM7_0_CACHE_NC_ECC	Non Correctable ECC error in CM7_0 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description.
20	CPUSS_CM7_1_CACHE_C_ECC	Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description.
21	CPUSS_CM7_1_CACHE_NC_ECC	Non Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description.
25	PERI_MS_VIO_4	P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
26	PERI_PERI_C_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
27	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation
28	PERI_MS_VIO_0	CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": master interface, PPU violation, "1": timeout detected, "2": bus error, other: undefined.
29	PERI_MS_VIO_1	CM7_0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_2	CM7_1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
31	PERI_MS_VIO_3	P-DMA0 Peripheral Master Interface PPU_3 violation. See PERI_MS_VIO_0 description.

故障

表 21-1 故障分配 (续)

Fault	Source	Description
32	PERI_GROUP_VIO_0	Peripheral Group #0 violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.
36	PERI_GROUP_VIO_4	Peripheral Group #4 violation. See PERI_GROUP_VIO_0 description.
37	PERI_GROUP_VIO_5	Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.
40	PERI_GROUP_VIO_8	Peripheral Group #8 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERR	Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERR	Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
56	CPUSS_CM7_0_TCM_C_ECC	CPU CM7_0 TCM memory correctable ECC violation. See CPUSS_CM7_1_TCM_C_ECC description.
57	CPUSS_CM7_0_TCM_NC_ECC	CPU CM7_0 TCM memory non-correctable ECC violation. See CPUSS_CM7_1_TCM_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
64	CPUSS_CRYPT0_C_ECC	Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.

故障

表 21-1 故障分配 (续)

Fault	Source	Description
65	CPUSS_CRYPTO_NC_ECC	CRYPTO memory non-correctable ECC violation. See CPUSS_CRYPTO_C_ECC description.
70	CPUSS_DW0_C_ECC	P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
71	CPUSS_DW0_NC_ECC	P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
72	CPUSS_DW1_C_ECC	P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
73	CPUSS_DW1_NC_ECC	P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
74	CPUSS_FM_SRAM_C_ECC	Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
75	CPUSS_FM_SRAM_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.
80	CANFD_0_CAN_C_ECC	CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcand cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.
81	CANFD_0_CAN_NC_ECC	CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcand cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
82	CANFD_1_CAN_C_ECC	CAN1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description.
83	CANFD_1_CAN_NC_ECC	CAN1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDPA DATA[1]: OVD on VDPA DATA[16]: LVD/HVD #1 DATA[17]: LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description.
94	SRSS_FAULT_MCWDT2	Fault output for MCWDT2 (all sub-counters). See SRSS_FAULT_MCWDT0 description.

22 外设保护单位固定结构配对

保护配对由一对PPU结构、一个主机、一个从机结构组成。主结构保护从机结构，从机结构保护外设寄存器等资源，或外设本身。

表 22-1 PPU 固定结构配对

Pair no.	PPU fixed structure pair	Address	Size	Description
0	PERI_MS_PPU_FX_PERI_MAIN	0x40000200	0x00000040	Peripheral Interconnect main
1	PERI_MS_PPU_FX_PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_MS_PPU_FX_PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral Group #0 main
3	PERI_MS_PPU_FX_PERI_GR1_GROUP	0x40004050	0x00000004	Peripheral Group #1 main
4	PERI_MS_PPU_FX_PERI_GR2_GROUP	0x40004090	0x00000004	Peripheral Group #2 main
5	PERI_MS_PPU_FX_PERI_GR3_GROUP	0x400040C0	0x00000020	Peripheral Group #3 main
6	PERI_MS_PPU_FX_PERI_GR4_GROUP	0x40004100	0x00000020	Peripheral Group #4 main
7	PERI_MS_PPU_FX_PERI_GR5_GROUP	0x40004140	0x00000020	Peripheral Group #5 main
8	PERI_MS_PPU_FX_PERI_GR6_GROUP	0x40004180	0x00000020	Peripheral Group #6 main
9	PERI_MS_PPU_FX_PERI_GR8_GROUP	0x40004200	0x00000020	Peripheral Group #8 main
10	PERI_MS_PPU_FX_PERI_GR9_GROUP	0x40004240	0x00000020	Peripheral Group #9 main
11	PERI_MS_PPU_FX_PERI_GR0_BOOT	0x40004020	0x00000004	Peripheral Group #0 boot
12	PERI_MS_PPU_FX_PERI_GR1_BOOT	0x40004060	0x00000004	Peripheral Group #1 boot
13	PERI_MS_PPU_FX_PERI_GR2_BOOT	0x400040A0	0x00000004	Peripheral Group #2 boot
14	PERI_MS_PPU_FX_PERI_GR3_BOOT	0x400040E0	0x00000004	Peripheral Group #3 boot
15	PERI_MS_PPU_FX_PERI_GR4_BOOT	0x40004120	0x00000004	Peripheral Group #4 boot
16	PERI_MS_PPU_FX_PERI_GR5_BOOT	0x40004160	0x00000004	Peripheral Group #5 boot
17	PERI_MS_PPU_FX_PERI_GR6_BOOT	0x400041A0	0x00000004	Peripheral Group #6 boot
18	PERI_MS_PPU_FX_PERI_GR8_BOOT	0x40004220	0x00000004	Peripheral Group #8 boot
19	PERI_MS_PPU_FX_PERI_GR9_BOOT	0x40004260	0x00000004	Peripheral Group #9 boot
20	PERI_MS_PPU_FX_PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
21	PERI_MS_PPU_FX_PERI_MS_BOOT	0x40030000	0x00001000	Peripheral master slave boot
22	PERI_MS_PPU_FX_PERI_PCLK_MAIN	0x40040000	0x00004000	Peripheral clock main
23	PERI_MS_PPU_FX_CRYPT0_MAIN	0x40100000	0x00000400	Crypto main
24	PERI_MS_PPU_FX_CRYPT0_CRYPT0	0x40101000	0x00000800	Crypto MMIO (Memory Mapped I/O)
25	PERI_MS_PPU_FX_CRYPT0_BOOT	0x40102000	0x00000100	Crypto boot
26	PERI_MS_PPU_FX_CRYPT0_KEY0	0x40102100	0x00000004	Crypto Key #0
27	PERI_MS_PPU_FX_CRYPT0_KEY1	0x40102120	0x00000004	Crypto Key #1
28	PERI_MS_PPU_FX_CRYPT0_BUF	0x40108000	0x00002000	Crypto buffer
29	PERI_MS_PPU_FX_CPUS0_CM7_0	0x40200000	0x00000400	CM7_0 CPU core
30	PERI_MS_PPU_FX_CPUS0_CM7_1	0x40200400	0x00000400	CM7_1 CPU core
31	PERI_MS_PPU_FX_CPUS0_CM0	0x40201000	0x00001000	CM0+ CPU core
32	PERI_MS_PPU_FX_CPUS0_BOOT ^[40]	0x40202000	0x00000200	CPUS0 boot
33	PERI_MS_PPU_FX_CPUS0_CM0_INT	0x40208000	0x00001000	CPUS0 CM0+ interrupts
34	PERI_MS_PPU_FX_CPUS0_CM7_0_INT	0x4020A000	0x00001000	CPUS0 CM7_0 interrupts
35	PERI_MS_PPU_FX_CPUS0_CM7_1_INT	0x4020C000	0x00001000	CPUS0 CM7_1 interrupts
36	PERI_MS_PPU_FX_FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUS0 Fault Structure #0 main
37	PERI_MS_PPU_FX_FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUS0 Fault Structure #1 main

注：

40. 固定PPU配置在Boot内部，用户不得更改此PPU的属性。

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
38	PERI_MS_PPU_FX_FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS Fault Structure #2 main
39	PERI_MS_PPU_FX_FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS Fault Structure #3 main
40	PERI_MS_PPU_FX_IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC Structure #0
41	PERI_MS_PPU_FX_IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC Structure #1
42	PERI_MS_PPU_FX_IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC Structure #2
43	PERI_MS_PPU_FX_IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC Structure #3
44	PERI_MS_PPU_FX_IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC Structure #4
45	PERI_MS_PPU_FX_IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC Structure #5
46	PERI_MS_PPU_FX_IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC Structure #6
47	PERI_MS_PPU_FX_IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC Structure #7
48	PERI_MS_PPU_FX_IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC Interrupt Structure #0
49	PERI_MS_PPU_FX_IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC Interrupt Structure #1
50	PERI_MS_PPU_FX_IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC Interrupt Structure #2
51	PERI_MS_PPU_FX_IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC Interrupt Structure #3
52	PERI_MS_PPU_FX_IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC Interrupt Structure #4
53	PERI_MS_PPU_FX_IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC Interrupt Structure #5
54	PERI_MS_PPU_FX_IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC Interrupt Structure #6
55	PERI_MS_PPU_FX_IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC Interrupt Structure #7
56	PERI_MS_PPU_FX_PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection SMPU main
57	PERI_MS_PPU_FX_PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
58	PERI_MS_PPU_FX_PROT_MPU5_MAIN	0x40235400	0x00000400	Peripheral protection MPU #5 main
59	PERI_MS_PPU_FX_PROT_MPU6_MAIN	0x40235800	0x00000400	Peripheral protection MPU #6 main
60	PERI_MS_PPU_FX_PROT_MPU13_MAIN	0x40237400	0x00000004	Peripheral protection MPU #13 main
61	PERI_MS_PPU_FX_PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
62	PERI_MS_PPU_FX_PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
63	PERI_MS_PPU_FX_FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
64	PERI_MS_PPU_FX_FLASHC_CMD	0x40240008	0x00000004	Flash controller command
65	PERI_MS_PPU_FX_FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
66	PERI_MS_PPU_FX_FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
67	PERI_MS_PPU_FX_FLASHC_CM7_0	0x402404E0	0x00000004	Flash controller CM7_0
68	PERI_MS_PPU_FX_FLASHC_CM7_1	0x40240560	0x00000004	Flash controller CM7_1
69	PERI_MS_PPU_FX_FLASHC_CRYPT0	0x40240580	0x00000004	Flash controller Crypto
70	PERI_MS_PPU_FX_FLASHC_DW0	0x40240600	0x00000004	Flash controller P-DMA0
71	PERI_MS_PPU_FX_FLASHC_DW1	0x40240680	0x00000004	Flash controller P-DMA1
72	PERI_MS_PPU_FX_FLASHC_DMAC	0x40240700	0x00000004	Flash controller M-DMA0
73	PERI_MS_PPU_FX_FLASHC_SLOW0	0x40240780	0x00000004	Flash External AHB-Lite Master 0
74	PERI_MS_PPU_FX_FLASHC_FlashMgmt ^[41]	0x4024F000	0x00000080	Flash management
75	PERI_MS_PPU_FX_FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller code-flash safety
76	PERI_MS_PPU_FX_FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work-flash safety
77	PERI_MS_PPU_FX_FLASHC_FM	0x4024F000	0x00001000	Flash management
78	PERI_MS_PPU_FX_SRSS_GENERAL	0x40260000	0x00000400	SRSS General

注：

41. 固定PPU配置在Boot内部，用户不得更改此PPU的属性。



外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
79	PERI_MS_PPU_FX_SRSS_MAIN	0x40261000	0x00001000	SRSS main
80	PERI_MS_PPU_FX_SRSS_SECURE	0x40262000	0x00002000	SRSS secure
81	PERI_MS_PPU_FX_MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
82	PERI_MS_PPU_FX_MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
83	PERI_MS_PPU_FX_MCWDT2_CONFIG	0x40268200	0x00000080	MCWDT #2 configuration
84	PERI_MS_PPU_FX_MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
85	PERI_MS_PPU_FX_MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
86	PERI_MS_PPU_FX_MCWDT2_MAIN	0x40268280	0x00000040	MCWDT #2 main
87	PERI_MS_PPU_FX_WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
88	PERI_MS_PPU_FX_WDT_MAIN	0x4026C040	0x00000020	System WDT main
89	PERI_MS_PPU_FX_BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
90	PERI_MS_PPU_FX_DW0_DW	0x40280000	0x00000100	P-DMA0 main
91	PERI_MS_PPU_FX_DW1_DW	0x40290000	0x00000100	P-DMA1 main
92	PERI_MS_PPU_FX_DW0_DW_CRC	0x40280100	0x00000080	P-DMA0 CRC
93	PERI_MS_PPU_FX_DW1_DW_CRC	0x40290100	0x00000080	P-DMA1 CRC
94	PERI_MS_PPU_FX_DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA0 Channel #0
95	PERI_MS_PPU_FX_DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA0 Channel #1
96	PERI_MS_PPU_FX_DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA0 Channel #2
97	PERI_MS_PPU_FX_DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA0 Channel #3
98	PERI_MS_PPU_FX_DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA0 Channel #4
99	PERI_MS_PPU_FX_DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA0 Channel #5
100	PERI_MS_PPU_FX_DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA0 Channel #6
101	PERI_MS_PPU_FX_DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA0 Channel #7
102	PERI_MS_PPU_FX_DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA0 Channel #8
103	PERI_MS_PPU_FX_DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA0 Channel #9
104	PERI_MS_PPU_FX_DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA0 Channel #10
105	PERI_MS_PPU_FX_DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA0 Channel #11
106	PERI_MS_PPU_FX_DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA0 Channel #12
107	PERI_MS_PPU_FX_DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA0 Channel #13
108	PERI_MS_PPU_FX_DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA0 Channel #14
109	PERI_MS_PPU_FX_DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA0 Channel #15
110	PERI_MS_PPU_FX_DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA0 Channel #16
111	PERI_MS_PPU_FX_DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA0 Channel #17
112	PERI_MS_PPU_FX_DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA0 Channel #18
113	PERI_MS_PPU_FX_DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA0 Channel #19
114	PERI_MS_PPU_FX_DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA0 Channel #20
115	PERI_MS_PPU_FX_DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA0 Channel #21
116	PERI_MS_PPU_FX_DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA0 Channel #22
117	PERI_MS_PPU_FX_DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA0 Channel #23
118	PERI_MS_PPU_FX_DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA0 Channel #24
119	PERI_MS_PPU_FX_DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA0 Channel #25
120	PERI_MS_PPU_FX_DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA0 Channel #26
121	PERI_MS_PPU_FX_DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA0 Channel #27
122	PERI_MS_PPU_FX_DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA0 Channel #28
123	PERI_MS_PPU_FX_DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA0 Channel #29

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
124	PERI_MS_PPU_FX_DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA0 Channel #30
125	PERI_MS_PPU_FX_DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA0 Channel #31
126	PERI_MS_PPU_FX_DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA0 Channel #32
127	PERI_MS_PPU_FX_DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA0 Channel #33
128	PERI_MS_PPU_FX_DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA0 Channel #34
129	PERI_MS_PPU_FX_DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA0 Channel #35
130	PERI_MS_PPU_FX_DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA0 Channel #36
131	PERI_MS_PPU_FX_DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA0 Channel #37
132	PERI_MS_PPU_FX_DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA0 Channel #38
133	PERI_MS_PPU_FX_DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA0 Channel #39
134	PERI_MS_PPU_FX_DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA0 Channel #40
135	PERI_MS_PPU_FX_DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA0 Channel #41
136	PERI_MS_PPU_FX_DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA0 Channel #42
137	PERI_MS_PPU_FX_DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA0 Channel #43
138	PERI_MS_PPU_FX_DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA0 Channel #44
139	PERI_MS_PPU_FX_DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA0 Channel #45
140	PERI_MS_PPU_FX_DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA0 Channel #46
141	PERI_MS_PPU_FX_DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA0 Channel #47
142	PERI_MS_PPU_FX_DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA0 Channel #48
143	PERI_MS_PPU_FX_DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA0 Channel #49
144	PERI_MS_PPU_FX_DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA0 Channel #50
145	PERI_MS_PPU_FX_DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA0 Channel #51
146	PERI_MS_PPU_FX_DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA0 Channel #52
147	PERI_MS_PPU_FX_DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA0 Channel #53
148	PERI_MS_PPU_FX_DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA0 Channel #54
149	PERI_MS_PPU_FX_DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA0 Channel #55
150	PERI_MS_PPU_FX_DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA0 Channel #56
151	PERI_MS_PPU_FX_DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA0 Channel #57
152	PERI_MS_PPU_FX_DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA0 Channel #58
153	PERI_MS_PPU_FX_DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA0 Channel #59
154	PERI_MS_PPU_FX_DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA0 Channel #60
155	PERI_MS_PPU_FX_DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA0 Channel #61
156	PERI_MS_PPU_FX_DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA0 Channel #62
157	PERI_MS_PPU_FX_DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA0 Channel #63
158	PERI_MS_PPU_FX_DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA0 Channel #64
159	PERI_MS_PPU_FX_DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA0 Channel #65
160	PERI_MS_PPU_FX_DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA0 Channel #66
161	PERI_MS_PPU_FX_DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA0 Channel #67
162	PERI_MS_PPU_FX_DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA0 Channel #68
163	PERI_MS_PPU_FX_DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA0 Channel #69
164	PERI_MS_PPU_FX_DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA0 Channel #70
165	PERI_MS_PPU_FX_DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA0 Channel #71
166	PERI_MS_PPU_FX_DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA0 Channel #72
167	PERI_MS_PPU_FX_DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA0 Channel #73
168	PERI_MS_PPU_FX_DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA0 Channel #74



外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
169	PERI_MS_PPU_FX_DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA0 Channel #75
170	PERI_MS_PPU_FX_DW0_CH_STRUCT76_CH	0x40289300	0x00000040	P-DMA0 Channel #76
171	PERI_MS_PPU_FX_DW0_CH_STRUCT77_CH	0x40289340	0x00000040	P-DMA0 Channel #77
172	PERI_MS_PPU_FX_DW0_CH_STRUCT78_CH	0x40289380	0x00000040	P-DMA0 Channel #78
173	PERI_MS_PPU_FX_DW0_CH_STRUCT79_CH	0x402893C0	0x00000040	P-DMA0 Channel #79
174	PERI_MS_PPU_FX_DW0_CH_STRUCT80_CH	0x40289400	0x00000040	P-DMA0 Channel #80
175	PERI_MS_PPU_FX_DW0_CH_STRUCT81_CH	0x40289440	0x00000040	P-DMA0 Channel #81
176	PERI_MS_PPU_FX_DW0_CH_STRUCT82_CH	0x40289480	0x00000040	P-DMA0 Channel #82
177	PERI_MS_PPU_FX_DW0_CH_STRUCT83_CH	0x402894C0	0x00000040	P-DMA0 Channel #83
178	PERI_MS_PPU_FX_DW0_CH_STRUCT84_CH	0x40289500	0x00000040	P-DMA0 Channel #84
179	PERI_MS_PPU_FX_DW0_CH_STRUCT85_CH	0x40289540	0x00000040	P-DMA0 Channel #85
180	PERI_MS_PPU_FX_DW0_CH_STRUCT86_CH	0x40289580	0x00000040	P-DMA0 Channel #86
181	PERI_MS_PPU_FX_DW0_CH_STRUCT87_CH	0x402895C0	0x00000040	P-DMA0 Channel #87
182	PERI_MS_PPU_FX_DW0_CH_STRUCT88_CH	0x40289600	0x00000040	P-DMA0 Channel #88
183	PERI_MS_PPU_FX_DW0_CH_STRUCT89_CH	0x40289640	0x00000040	P-DMA0 Channel #89
184	PERI_MS_PPU_FX_DW0_CH_STRUCT90_CH	0x40289680	0x00000040	P-DMA0 Channel #90
185	PERI_MS_PPU_FX_DW0_CH_STRUCT91_CH	0x402896C0	0x00000040	P-DMA0 Channel #91
186	PERI_MS_PPU_FX_DW0_CH_STRUCT92_CH	0x40289700	0x00000040	P-DMA0 Channel #92
187	PERI_MS_PPU_FX_DW0_CH_STRUCT93_CH	0x40289740	0x00000040	P-DMA0 Channel #93
188	PERI_MS_PPU_FX_DW0_CH_STRUCT94_CH	0x40289780	0x00000040	P-DMA0 Channel #94
189	PERI_MS_PPU_FX_DW0_CH_STRUCT95_CH	0x402897C0	0x00000040	P-DMA0 Channel #95
190	PERI_MS_PPU_FX_DW0_CH_STRUCT96_CH	0x40289800	0x00000040	P-DMA0 Channel #96
191	PERI_MS_PPU_FX_DW0_CH_STRUCT97_CH	0x40289840	0x00000040	P-DMA0 Channel #97
192	PERI_MS_PPU_FX_DW0_CH_STRUCT98_CH	0x40289880	0x00000040	P-DMA0 Channel #98
193	PERI_MS_PPU_FX_DW0_CH_STRUCT99_CH	0x402898C0	0x00000040	P-DMA0 Channel #99
194	PERI_MS_PPU_FX_DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA1 Channel #0
195	PERI_MS_PPU_FX_DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA1 Channel #1
196	PERI_MS_PPU_FX_DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA1 Channel #2
197	PERI_MS_PPU_FX_DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA1 Channel #3
198	PERI_MS_PPU_FX_DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA1 Channel #4
199	PERI_MS_PPU_FX_DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA1 Channel #5
200	PERI_MS_PPU_FX_DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA1 Channel #6
201	PERI_MS_PPU_FX_DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA1 Channel #7
202	PERI_MS_PPU_FX_DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA1 Channel #8
203	PERI_MS_PPU_FX_DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA1 Channel #9
204	PERI_MS_PPU_FX_DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA1 Channel #10
205	PERI_MS_PPU_FX_DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA1 Channel #11
206	PERI_MS_PPU_FX_DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA1 Channel #12
207	PERI_MS_PPU_FX_DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA1 Channel #13
208	PERI_MS_PPU_FX_DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA1 Channel #14
209	PERI_MS_PPU_FX_DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA1 Channel #15
210	PERI_MS_PPU_FX_DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA1 Channel #16
211	PERI_MS_PPU_FX_DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA1 Channel #17
212	PERI_MS_PPU_FX_DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA1 Channel #18
213	PERI_MS_PPU_FX_DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA1 Channel #19



外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
214	PERI_MS_PPU_FX_DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA1 Channel #20
215	PERI_MS_PPU_FX_DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA1 Channel #21
216	PERI_MS_PPU_FX_DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA1 Channel #22
217	PERI_MS_PPU_FX_DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA1 Channel #23
218	PERI_MS_PPU_FX_DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA1 Channel #24
219	PERI_MS_PPU_FX_DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA1 Channel #25
220	PERI_MS_PPU_FX_DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA1 Channel #26
221	PERI_MS_PPU_FX_DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA1 Channel #27
222	PERI_MS_PPU_FX_DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA1 Channel #28
223	PERI_MS_PPU_FX_DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA1 Channel #29
224	PERI_MS_PPU_FX_DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA1 Channel #30
225	PERI_MS_PPU_FX_DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA1 Channel #31
226	PERI_MS_PPU_FX_DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA1 Channel #32
227	PERI_MS_PPU_FX_DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA1 Channel #33
228	PERI_MS_PPU_FX_DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA1 Channel #34
229	PERI_MS_PPU_FX_DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA1 Channel #35
230	PERI_MS_PPU_FX_DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA1 Channel #36
231	PERI_MS_PPU_FX_DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA1 Channel #37
232	PERI_MS_PPU_FX_DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA1 Channel #38
233	PERI_MS_PPU_FX_DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA1 Channel #39
234	PERI_MS_PPU_FX_DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA1 Channel #40
235	PERI_MS_PPU_FX_DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA1 Channel #41
236	PERI_MS_PPU_FX_DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA1 Channel #42
237	PERI_MS_PPU_FX_DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA1 Channel #43
238	PERI_MS_PPU_FX_DW1_CH_STRUCT44_CH	0x40298B00	0x00000040	P-DMA1 Channel #44
239	PERI_MS_PPU_FX_DW1_CH_STRUCT45_CH	0x40298B40	0x00000040	P-DMA1 Channel #45
240	PERI_MS_PPU_FX_DW1_CH_STRUCT46_CH	0x40298B80	0x00000040	P-DMA1 Channel #46
241	PERI_MS_PPU_FX_DW1_CH_STRUCT47_CH	0x40298BC0	0x00000040	P-DMA1 Channel #47
242	PERI_MS_PPU_FX_DW1_CH_STRUCT48_CH	0x40298C00	0x00000040	P-DMA1 Channel #48
243	PERI_MS_PPU_FX_DW1_CH_STRUCT49_CH	0x40298C40	0x00000040	P-DMA1 Channel #49
244	PERI_MS_PPU_FX_DW1_CH_STRUCT50_CH	0x40298C80	0x00000040	P-DMA1 Channel #50
245	PERI_MS_PPU_FX_DW1_CH_STRUCT51_CH	0x40298CC0	0x00000040	P-DMA1 Channel #51
246	PERI_MS_PPU_FX_DW1_CH_STRUCT52_CH	0x40298D00	0x00000040	P-DMA1 Channel #52
247	PERI_MS_PPU_FX_DW1_CH_STRUCT53_CH	0x40298D40	0x00000040	P-DMA1 Channel #53
248	PERI_MS_PPU_FX_DW1_CH_STRUCT54_CH	0x40298D80	0x00000040	P-DMA1 Channel #54
249	PERI_MS_PPU_FX_DW1_CH_STRUCT55_CH	0x40298DC0	0x00000040	P-DMA1 Channel #55
250	PERI_MS_PPU_FX_DW1_CH_STRUCT56_CH	0x40298E00	0x00000040	P-DMA1 Channel #56
251	PERI_MS_PPU_FX_DW1_CH_STRUCT57_CH	0x40298E40	0x00000040	P-DMA1 Channel #57
252	PERI_MS_PPU_FX_DMACH0_TOP	0x402A0000	0x00000010	M-DMA0 main
253	PERI_MS_PPU_FX_DMACH0_CH	0x402A1000	0x00000100	M-DMA0 Channel #0
254	PERI_MS_PPU_FX_DMACH1_CH	0x402A1100	0x00000100	M-DMA0 Channel #1
255	PERI_MS_PPU_FX_DMACH2_CH	0x402A1200	0x00000100	M-DMA0 Channel #2
256	PERI_MS_PPU_FX_DMACH3_CH	0x402A1300	0x00000100	M-DMA0 Channel #3
257	PERI_MS_PPU_FX_DMACH4_CH	0x402A1400	0x00000100	M-DMA0 Channel #4
258	PERI_MS_PPU_FX_DMACH5_CH	0x402A1500	0x00000100	M-DMA0 Channel #5



外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
259	PERI_MS_PPU_FX_DMAC_CH6_CH	0x402A1600	0x00000100	M-DMA0 Channel #6
260	PERI_MS_PPU_FX_DMAC_CH7_CH	0x402A1700	0x00000100	M-DMA0 Channel #7
261	PERI_MS_PPU_FX_EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
262	PERI_MS_PPU_FX_EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
263	PERI_MS_PPU_FX_BIST	0x402F0000	0x00001000	Built-in self test
264	PERI_MS_PPU_FX_HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOM Port #0
265	PERI_MS_PPU_FX_HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOM Port #1
266	PERI_MS_PPU_FX_HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOM Port #2
267	PERI_MS_PPU_FX_HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOM Port #3
268	PERI_MS_PPU_FX_HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOM Port #4
269	PERI_MS_PPU_FX_HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOM Port #5
270	PERI_MS_PPU_FX_HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOM Port #6
271	PERI_MS_PPU_FX_HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOM Port #7
272	PERI_MS_PPU_FX_HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOM Port #8
273	PERI_MS_PPU_FX_HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOM Port #9
274	PERI_MS_PPU_FX_HSIOM_PRT10_PRT	0x403000A0	0x00000008	HSIOM Port #10
275	PERI_MS_PPU_FX_HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOM Port #11
276	PERI_MS_PPU_FX_HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOM Port #12
277	PERI_MS_PPU_FX_HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOM Port #13
278	PERI_MS_PPU_FX_HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOM Port #14
279	PERI_MS_PPU_FX_HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOM Port #15
280	PERI_MS_PPU_FX_HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOM Port #16
281	PERI_MS_PPU_FX_HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOM Port #17
282	PERI_MS_PPU_FX_HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOM Port #18
283	PERI_MS_PPU_FX_HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOM Port #19
284	PERI_MS_PPU_FX_HSIOM_PRT20_PRT	0x40300140	0x00000008	HSIOM Port #20
285	PERI_MS_PPU_FX_HSIOM_PRT21_PRT	0x40300150	0x00000008	HSIOM Port #21
286	PERI_MS_PPU_FX_HSIOM_PRT22_PRT	0x40300160	0x00000008	HSIOM Port #22
287	PERI_MS_PPU_FX_HSIOM_PRT23_PRT	0x40300170	0x00000008	HSIOM Port #23
288	PERI_MS_PPU_FX_HSIOM_PRT24_PRT	0x40300180	0x00000008	HSIOM Port #24
289	PERI_MS_PPU_FX_HSIOM_PRT25_PRT	0x40300190	0x00000008	HSIOM Port #25
290	PERI_MS_PPU_FX_HSIOM_PRT26_PRT	0x403001A0	0x00000008	HSIOM Port #26
291	PERI_MS_PPU_FX_HSIOM_PRT27_PRT	0x403001B0	0x00000008	HSIOM Port #27
292	PERI_MS_PPU_FX_HSIOM_PRT28_PRT	0x403001C0	0x00000008	HSIOM Port #28
293	PERI_MS_PPU_FX_HSIOM_PRT29_PRT	0x403001D0	0x00000008	HSIOM Port #29
294	PERI_MS_PPU_FX_HSIOM_PRT30_PRT	0x403001E0	0x00000008	HSIOM Port #30
295	PERI_MS_PPU_FX_HSIOM_PRT31_PRT	0x403001F0	0x00000008	HSIOM Port #31
296	PERI_MS_PPU_FX_HSIOM_PRT32_PRT	0x40300200	0x00000008	HSIOM Port #32
297	PERI_MS_PPU_FX_HSIOM_AMUX	0x40302000	0x00000010	HSIOM Analog multiplexer
298	PERI_MS_PPU_FX_HSIOM_MON	0x40302200	0x00000010	HSIOM monitor
299	PERI_MS_PPU_FX_HSIOM_ALTJTAG	0x40302240	0x00000004	HSIOM Alternate JTAG
300	PERI_MS_PPU_FX_GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_ENH Port #0
301	PERI_MS_PPU_FX_GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD Port #1
302	PERI_MS_PPU_FX_GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD Port #2
303	PERI_MS_PPU_FX_GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_STD Port #3

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
304	PERI_MS_PPU_FX_GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD Port #4
305	PERI_MS_PPU_FX_GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_STD Port #5
306	PERI_MS_PPU_FX_GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_STD Port #6
307	PERI_MS_PPU_FX_GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_STD Port #7
308	PERI_MS_PPU_FX_GPIO_PRT8_PRT	0x40310400	0x00000040	GPIO_STD Port #8
309	PERI_MS_PPU_FX_GPIO_PRT9_PRT	0x40310480	0x00000040	GPIO_STD Port #9
310	PERI_MS_PPU_FX_GPIO_PRT10_PRT	0x40310500	0x00000040	GPIO_STD Port #10
311	PERI_MS_PPU_FX_GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_STD Port #11
312	PERI_MS_PPU_FX_GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_STD Port #12
313	PERI_MS_PPU_FX_GPIO_PRT13_PRT	0x40310680	0x00000040	GPIO_STD Port #13
314	PERI_MS_PPU_FX_GPIO_PRT14_PRT	0x40310700	0x00000040	GPIO_STD Port #14
315	PERI_MS_PPU_FX_GPIO_PRT15_PRT	0x40310780	0x00000040	GPIO_STD Port #15
316	PERI_MS_PPU_FX_GPIO_PRT16_PRT	0x40310800	0x00000040	GPIO_STD Port #16
317	PERI_MS_PPU_FX_GPIO_PRT17_PRT	0x40310880	0x00000040	GPIO_STD Port #17
318	PERI_MS_PPU_FX_GPIO_PRT18_PRT	0x40310900	0x00000040	GPIO_STD Port #18
319	PERI_MS_PPU_FX_GPIO_PRT19_PRT	0x40310980	0x00000040	GPIO_STD Port #19
320	PERI_MS_PPU_FX_GPIO_PRT20_PRT	0x40310A00	0x00000040	GPIO_STD Port #20
321	PERI_MS_PPU_FX_GPIO_PRT21_PRT	0x40310A80	0x00000040	GPIO_STD Port #21
322	PERI_MS_PPU_FX_GPIO_PRT22_PRT	0x40310B00	0x00000040	GPIO_STD Port #22
323	PERI_MS_PPU_FX_GPIO_PRT23_PRT	0x40310B80	0x00000040	GPIO_STD Port #23
324	PERI_MS_PPU_FX_GPIO_PRT24_PRT	0x40310C00	0x00000040	HSIO_STD Port #24
325	PERI_MS_PPU_FX_GPIO_PRT25_PRT	0x40310C80	0x00000040	HSIO_STD Port #25
326	PERI_MS_PPU_FX_GPIO_PRT26_PRT	0x40310D00	0x00000040	HSIO_STD Port #26
327	PERI_MS_PPU_FX_GPIO_PRT27_PRT	0x40310D80	0x00000040	HSIO_STD Port #27
328	PERI_MS_PPU_FX_GPIO_PRT28_PRT	0x40310E00	0x00000040	GPIO_STD Port #28
329	PERI_MS_PPU_FX_GPIO_PRT29_PRT	0x40310E80	0x00000040	GPIO_STD Port #29
330	PERI_MS_PPU_FX_GPIO_PRT30_PRT	0x40310F00	0x00000040	GPIO_STD Port #30
331	PERI_MS_PPU_FX_GPIO_PRT31_PRT	0x40310F80	0x00000040	GPIO_STD Port #31
332	PERI_MS_PPU_FX_GPIO_PRT32_PRT	0x40311000	0x00000040	GPIO_STD Port #32
333	PERI_MS_PPU_FX_GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_ENH Port #0 configuration
334	PERI_MS_PPU_FX_GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD Port #1 configuration
335	PERI_MS_PPU_FX_GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD Port #2 configuration
336	PERI_MS_PPU_FX_GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_STD Port #3 configuration
337	PERI_MS_PPU_FX_GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD Port #4 configuration
338	PERI_MS_PPU_FX_GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_STD Port #5 configuration
339	PERI_MS_PPU_FX_GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_STD Port #6 configuration
340	PERI_MS_PPU_FX_GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_STD Port #7 configuration
341	PERI_MS_PPU_FX_GPIO_PRT8_CFG	0x40310440	0x00000020	GPIO_STD Port #8 configuration
342	PERI_MS_PPU_FX_GPIO_PRT9_CFG	0x403104C0	0x00000020	GPIO_STD Port #9 configuration
343	PERI_MS_PPU_FX_GPIO_PRT10_CFG	0x40310540	0x00000020	GPIO_STD Port #10 configuration
344	PERI_MS_PPU_FX_GPIO_PRT11_CFG	0x403105C0	0x00000020	GPIO_STD Port #11 configuration
345	PERI_MS_PPU_FX_GPIO_PRT12_CFG	0x40310640	0x00000020	GPIO_STD Port #12 configuration
346	PERI_MS_PPU_FX_GPIO_PRT13_CFG	0x403106C0	0x00000020	GPIO_STD Port #13 configuration
347	PERI_MS_PPU_FX_GPIO_PRT14_CFG	0x40310740	0x00000020	GPIO_STD Port #14 configuration
348	PERI_MS_PPU_FX_GPIO_PRT15_CFG	0x403107C0	0x00000020	GPIO_STD Port #15 configuration

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
349	PERI_MS_PPU_FX_GPIO_PRT16_CFG	0x40310840	0x00000020	GPIO_STD Port #16 configuration
350	PERI_MS_PPU_FX_GPIO_PRT17_CFG	0x403108C0	0x00000020	GPIO_STD Port #17 configuration
351	PERI_MS_PPU_FX_GPIO_PRT18_CFG	0x40310940	0x00000020	GPIO_STD Port #18 configuration
352	PERI_MS_PPU_FX_GPIO_PRT19_CFG	0x403109C0	0x00000020	GPIO_STD Port #19 configuration
353	PERI_MS_PPU_FX_GPIO_PRT20_CFG	0x40310A40	0x00000020	GPIO_STD Port #20 configuration
354	PERI_MS_PPU_FX_GPIO_PRT21_CFG	0x40310AC0	0x00000020	GPIO_STD Port #21 configuration
355	PERI_MS_PPU_FX_GPIO_PRT22_CFG	0x40310B40	0x00000020	GPIO_STD Port #22 configuration
356	PERI_MS_PPU_FX_GPIO_PRT23_CFG	0x40310BC0	0x00000020	GPIO_STD Port #23 configuration
357	PERI_MS_PPU_FX_GPIO_PRT24_CFG	0x40310C40	0x00000020	HSIO_STD Port #24 configuration
358	PERI_MS_PPU_FX_GPIO_PRT25_CFG	0x40310CC0	0x00000020	HSIO_STD Port #25 configuration
359	PERI_MS_PPU_FX_GPIO_PRT26_CFG	0x40310D40	0x00000020	HSIO_STD Port #26 configuration
360	PERI_MS_PPU_FX_GPIO_PRT27_CFG	0x40310DC0	0x00000020	HSIO_STD Port #27 configuration
361	PERI_MS_PPU_FX_GPIO_PRT28_CFG	0x40310E40	0x00000020	GPIO_STD Port #28 configuration
362	PERI_MS_PPU_FX_GPIO_PRT29_CFG	0x40310EC0	0x00000020	GPIO_STD Port #29 configuration
363	PERI_MS_PPU_FX_GPIO_PRT30_CFG	0x40310F40	0x00000020	GPIO_STD Port #30 configuration
364	PERI_MS_PPU_FX_GPIO_PRT31_CFG	0x40310FC0	0x00000020	GPIO_STD Port #31 configuration
365	PERI_MS_PPU_FX_GPIO_PRT32_CFG	0x40311040	0x00000020	GPIO_STD Port #32 configuration
366	PERI_MS_PPU_FX_GPIO_GPIO	0x40314000	0x00000040	GPIO main
367	PERI_MS_PPU_FX_GPIO_TEST	0x40315000	0x00000008	GPIO test
368	PERI_MS_PPU_FX_SMARTIO_PRT12_PRT	0x40320C00	0x00000100	SMART I/O #12
369	PERI_MS_PPU_FX_SMARTIO_PRT13_PRT	0x40320D00	0x00000100	SMART I/O #13
370	PERI_MS_PPU_FX_SMARTIO_PRT14_PRT	0x40320E00	0x00000100	SMART I/O #14
371	PERI_MS_PPU_FX_SMARTIO_PRT15_PRT	0x40320F00	0x00000100	SMART I/O #15
372	PERI_MS_PPU_FX_SMARTIO_PRT17_PRT	0x40321100	0x00000100	SMART I/O #17
373	PERI_MS_PPU_FX_EVTGEN0	0x403F0000	0x00001000	Event generator #0
374	PERI_MS_PPU_FX_SMIF0	0x40420000	0x00010000	Serial Memory Interface #0
375	PERI_MS_PPU_FX_SDHC0	0x40460000	0x00010000	Secure Digital High Capacity #0
376	PERI_MS_PPU_FX_ETH0	0x40480000	0x00010000	Ethernet0
377	PERI_MS_PPU_FX_LIN0_MAIN	0x40500000	0x00000008	LIN0, main
378	PERI_MS_PPU_FX_LIN0_CH0_CH	0x40508000	0x00000100	LIN0, Channel #0
379	PERI_MS_PPU_FX_LIN0_CH1_CH	0x40508100	0x00000100	LIN0, Channel #1
380	PERI_MS_PPU_FX_LIN0_CH2_CH	0x40508200	0x00000100	LIN0, Channel #2
381	PERI_MS_PPU_FX_LIN0_CH3_CH	0x40508300	0x00000100	LIN0, Channel #3
382	PERI_MS_PPU_FX_LIN0_CH4_CH	0x40508400	0x00000100	LIN0, Channel #4
383	PERI_MS_PPU_FX_LIN0_CH5_CH	0x40508500	0x00000100	LIN0, Channel #5
384	PERI_MS_PPU_FX_LIN0_CH6_CH	0x40508600	0x00000100	LIN0, Channel #6
385	PERI_MS_PPU_FX_LIN0_CH7_CH	0x40508700	0x00000100	LIN0, Channel #7
386	PERI_MS_PPU_FX_LIN0_CH8_CH	0x40508800	0x00000100	LIN0, Channel #8
387	PERI_MS_PPU_FX_LIN0_CH9_CH	0x40508900	0x00000100	LIN0, Channel #9
388	PERI_MS_PPU_FX_LIN0_CH10_CH	0x40508A00	0x00000100	LIN0, Channel #10
389	PERI_MS_PPU_FX_LIN0_CH11_CH	0x40508B00	0x00000100	LIN0, Channel #11
390	PERI_MS_PPU_FX_LIN0_CH12_CH	0x40508C00	0x00000100	LIN0, Channel #12
391	PERI_MS_PPU_FX_LIN0_CH13_CH	0x40508D00	0x00000100	LIN0, Channel #13
392	PERI_MS_PPU_FX_LIN0_CH14_CH	0x40508E00	0x00000100	LIN0, Channel #14
393	PERI_MS_PPU_FX_LIN0_CH15_CH	0x40508F00	0x00000100	LIN0, Channel #15

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
394	PERI_MS_PPU_FX_CANFD0_CH0_CH	0x40520000	0x00000200	CAN0, Channel #0
395	PERI_MS_PPU_FX_CANFD0_CH1_CH	0x40520200	0x00000200	CAN0, Channel #1
396	PERI_MS_PPU_FX_CANFD0_CH2_CH	0x40520400	0x00000200	CAN0, Channel #2
397	PERI_MS_PPU_FX_CANFD0_CH3_CH	0x40520600	0x00000200	CAN0, Channel #3
398	PERI_MS_PPU_FX_CANFD1_CH0_CH	0x40540000	0x00000200	CAN1, Channel #0
399	PERI_MS_PPU_FX_CANFD1_CH1_CH	0x40540200	0x00000200	CAN1, Channel #1
400	PERI_MS_PPU_FX_CANFD1_CH2_CH	0x40540400	0x00000200	CAN1, Channel #2
401	PERI_MS_PPU_FX_CANFD1_CH3_CH	0x40540600	0x00000200	CAN1, Channel #3
402	PERI_MS_PPU_FX_CANFD0_MAIN	0x40521000	0x00000100	CAN0 main
403	PERI_MS_PPU_FX_CANFD1_MAIN	0x40541000	0x00000100	CAN1 main
404	PERI_MS_PPU_FX_CANFD0_BUF	0x40530000	0x00010000	CAN0 buffer
405	PERI_MS_PPU_FX_CANFD1_BUF	0x40550000	0x00010000	CAN1 buffer
406	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT0_CNT	0x40580000	0x00000080	TCPWM0 Group #0, Counter #0
407	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT1_CNT	0x40580080	0x00000080	TCPWM0 Group #0, Counter #1
408	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT2_CNT	0x40580100	0x00000080	TCPWM0 Group #0, Counter #2
409	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT3_CNT	0x40580180	0x00000080	TCPWM0 Group #0, Counter #3
410	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT4_CNT	0x40580200	0x00000080	TCPWM0 Group #0, Counter #4
411	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT5_CNT	0x40580280	0x00000080	TCPWM0 Group #0, Counter #5
412	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT6_CNT	0x40580300	0x00000080	TCPWM0 Group #0, Counter #6
413	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT7_CNT	0x40580380	0x00000080	TCPWM0 Group #0, Counter #7
414	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT8_CNT	0x40580400	0x00000080	TCPWM0 Group #0, Counter #8
415	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT9_CNT	0x40580480	0x00000080	TCPWM0 Group #0, Counter #9
416	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT10_CNT	0x40580500	0x00000080	TCPWM0 Group #0, Counter #10
417	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT11_CNT	0x40580580	0x00000080	TCPWM0 Group #0, Counter #11
418	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT12_CNT	0x40580600	0x00000080	TCPWM0 Group #0, Counter #12
419	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT13_CNT	0x40580680	0x00000080	TCPWM0 Group #0, Counter #13
420	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT14_CNT	0x40580700	0x00000080	TCPWM0 Group #0, Counter #14
421	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT15_CNT	0x40580780	0x00000080	TCPWM0 Group #0, Counter #15
422	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT16_CNT	0x40580800	0x00000080	TCPWM0 Group #0, Counter #16
423	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT17_CNT	0x40580880	0x00000080	TCPWM0 Group #0, Counter #17
424	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT18_CNT	0x40580900	0x00000080	TCPWM0 Group #0, Counter #18
425	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT19_CNT	0x40580980	0x00000080	TCPWM0 Group #0, Counter #19
426	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT20_CNT	0x40580A00	0x00000080	TCPWM0 Group #0, Counter #20
427	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT21_CNT	0x40580A80	0x00000080	TCPWM0 Group #0, Counter #21
428	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT22_CNT	0x40580B00	0x00000080	TCPWM0 Group #0, Counter #22
429	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT23_CNT	0x40580B80	0x00000080	TCPWM0 Group #0, Counter #23
430	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT24_CNT	0x40580C00	0x00000080	TCPWM0 Group #0, Counter #24
431	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT25_CNT	0x40580C80	0x00000080	TCPWM0 Group #0, Counter #25
432	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT26_CNT	0x40580D00	0x00000080	TCPWM0 Group #0, Counter #26
433	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT27_CNT	0x40580D80	0x00000080	TCPWM0 Group #0, Counter #27
434	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT28_CNT	0x40580E00	0x00000080	TCPWM0 Group #0, Counter #28
435	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT29_CNT	0x40580E80	0x00000080	TCPWM0 Group #0, Counter #29
436	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT30_CNT	0x40580F00	0x00000080	TCPWM0 Group #0, Counter #30
437	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT31_CNT	0x40580F80	0x00000080	TCPWM0 Group #0, Counter #31
438	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT32_CNT	0x40581000	0x00000080	TCPWM0 Group #0, Counter #32

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
439	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT33_CNT	0x40581080	0x00000080	TCPWM0 Group #0, Counter #33
440	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT34_CNT	0x40581100	0x00000080	TCPWM0 Group #0, Counter #34
441	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT35_CNT	0x40581180	0x00000080	TCPWM0 Group #0, Counter #35
442	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT36_CNT	0x40581200	0x00000080	TCPWM0 Group #0, Counter #36
443	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT37_CNT	0x40581280	0x00000080	TCPWM0 Group #0, Counter #37
444	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT38_CNT	0x40581300	0x00000080	TCPWM0 Group #0, Counter #38
445	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT39_CNT	0x40581380	0x00000080	TCPWM0 Group #0, Counter #39
446	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT40_CNT	0x40581400	0x00000080	TCPWM0 Group #0, Counter #40
447	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT41_CNT	0x40581480	0x00000080	TCPWM0 Group #0, Counter #41
448	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT42_CNT	0x40581500	0x00000080	TCPWM0 Group #0, Counter #42
449	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT43_CNT	0x40581580	0x00000080	TCPWM0 Group #0, Counter #43
450	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT44_CNT	0x40581600	0x00000080	TCPWM0 Group #0, Counter #44
451	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT45_CNT	0x40581680	0x00000080	TCPWM0 Group #0, Counter #45
452	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT46_CNT	0x40581700	0x00000080	TCPWM0 Group #0, Counter #46
453	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT47_CNT	0x40581780	0x00000080	TCPWM0 Group #0, Counter #47
454	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT48_CNT	0x40581800	0x00000080	TCPWM0 Group #0, Counter #48
455	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT49_CNT	0x40581880	0x00000080	TCPWM0 Group #0, Counter #49
456	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT50_CNT	0x40581900	0x00000080	TCPWM0 Group #0, Counter #50
457	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT51_CNT	0x40581980	0x00000080	TCPWM0 Group #0, Counter #51
458	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT52_CNT	0x40581A00	0x00000080	TCPWM0 Group #0, Counter #52
459	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT53_CNT	0x40581A80	0x00000080	TCPWM0 Group #0, Counter #53
460	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT54_CNT	0x40581B00	0x00000080	TCPWM0 Group #0, Counter #54
461	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT55_CNT	0x40581B80	0x00000080	TCPWM0 Group #0, Counter #55
462	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT56_CNT	0x40581C00	0x00000080	TCPWM0 Group #0, Counter #56
463	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT57_CNT	0x40581C80	0x00000080	TCPWM0 Group #0, Counter #57
464	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT58_CNT	0x40581D00	0x00000080	TCPWM0 Group #0, Counter #58
465	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT59_CNT	0x40581D80	0x00000080	TCPWM0 Group #0, Counter #59
466	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT60_CNT	0x40581E00	0x00000080	TCPWM0 Group #0, Counter #60
467	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT61_CNT	0x40581E80	0x00000080	TCPWM0 Group #0, Counter #61
468	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT62_CNT	0x40581F00	0x00000080	TCPWM0 Group #0, Counter #62
469	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT0_CNT	0x40588000	0x00000080	TCPWM0 Group #1, Counter #0
470	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT1_CNT	0x40588080	0x00000080	TCPWM0 Group #1, Counter #1
471	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT2_CNT	0x40588100	0x00000080	TCPWM0 Group #1, Counter #2
472	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT3_CNT	0x40588180	0x00000080	TCPWM0 Group #1, Counter #3
473	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT4_CNT	0x40588200	0x00000080	TCPWM0 Group #1, Counter #4
474	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT5_CNT	0x40588280	0x00000080	TCPWM0 Group #1, Counter #5
475	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT6_CNT	0x40588300	0x00000080	TCPWM0 Group #1, Counter #6
476	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT7_CNT	0x40588380	0x00000080	TCPWM0 Group #1, Counter #7
477	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT8_CNT	0x40588400	0x00000080	TCPWM0 Group #1, Counter #8
478	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT9_CNT	0x40588480	0x00000080	TCPWM0 Group #1, Counter #9
479	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT10_CNT	0x40588500	0x00000080	TCPWM0 Group #1, Counter #10
480	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT11_CNT	0x40588580	0x00000080	TCPWM0 Group #1, Counter #11
481	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT0_CNT	0x40590000	0x00000080	TCPWM0 Group #2, Counter #0
482	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT1_CNT	0x40590080	0x00000080	TCPWM0 Group #2, Counter #1
483	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT2_CNT	0x40590100	0x00000080	TCPWM0 Group #2, Counter #2

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
484	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT3_CNT	0x40590180	0x00000080	TCPWM0 Group #2, Counter #3
485	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT4_CNT	0x40590200	0x00000080	TCPWM0 Group #2, Counter #4
486	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT5_CNT	0x40590280	0x00000080	TCPWM0 Group #2, Counter #5
487	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT6_CNT	0x40590300	0x00000080	TCPWM0 Group #2, Counter #6
488	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT7_CNT	0x40590380	0x00000080	TCPWM0 Group #2, Counter #7
489	PERI_MS_PPU_FX_SCB0	0x40600000	0x00010000	SCB0
490	PERI_MS_PPU_FX_SCB1	0x40610000	0x00010000	SCB1
491	PERI_MS_PPU_FX_SCB2	0x40620000	0x00010000	SCB2
492	PERI_MS_PPU_FX_SCB3	0x40630000	0x00010000	SCB3
493	PERI_MS_PPU_FX_SCB4	0x40640000	0x00010000	SCB4
494	PERI_MS_PPU_FX_SCB5	0x40650000	0x00010000	SCB5
495	PERI_MS_PPU_FX_SCB6	0x40660000	0x00010000	SCB6
496	PERI_MS_PPU_FX_SCB7	0x40670000	0x00010000	SCB7
497	PERI_MS_PPU_FX_SCB8	0x40680000	0x00010000	SCB8
498	PERI_MS_PPU_FX_SCB9	0x40690000	0x00010000	SCB9
499	PERI_MS_PPU_FX_SCB10	0x406A0000	0x00010000	SCB10
500	PERI_MS_PPU_FX_I2S0	0x40800000	0x00001000	AUDIOSS I2S0
501	PERI_MS_PPU_FX_I2S1	0x40801000	0x00001000	AUDIOSS I2S1
502	PERI_MS_PPU_FX_I2S2	0x40802000	0x00001000	AUDIOSS I2S2
503	PERI_MS_PPU_FX_PASS0_SAR0_SAR	0x40900000	0x00000400	PASS SAR0
504	PERI_MS_PPU_FX_PASS0_SAR1_SAR	0x40901000	0x00000400	PASS SAR1
505	PERI_MS_PPU_FX_PASS0_SAR2_SAR	0x40902000	0x00000400	PASS SAR2
506	PERI_MS_PPU_FX_PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR0, Channel #0
507	PERI_MS_PPU_FX_PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR0, Channel #1
508	PERI_MS_PPU_FX_PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR0, Channel #2
509	PERI_MS_PPU_FX_PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR0, Channel #3
510	PERI_MS_PPU_FX_PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR0, Channel #4
511	PERI_MS_PPU_FX_PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR0, Channel #5
512	PERI_MS_PPU_FX_PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR0, Channel #6
513	PERI_MS_PPU_FX_PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR0, Channel #7
514	PERI_MS_PPU_FX_PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR0, Channel #8
515	PERI_MS_PPU_FX_PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR0, Channel #9
516	PERI_MS_PPU_FX_PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR0, Channel #10
517	PERI_MS_PPU_FX_PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR0, Channel #11
518	PERI_MS_PPU_FX_PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR0, Channel #12
519	PERI_MS_PPU_FX_PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR0, Channel #13
520	PERI_MS_PPU_FX_PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR0, Channel #14
521	PERI_MS_PPU_FX_PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR0, Channel #15
522	PERI_MS_PPU_FX_PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR0, Channel #16
523	PERI_MS_PPU_FX_PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR0, Channel #17
524	PERI_MS_PPU_FX_PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR0, Channel #18
525	PERI_MS_PPU_FX_PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR0, Channel #19
526	PERI_MS_PPU_FX_PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR0, Channel #20
527	PERI_MS_PPU_FX_PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR0, Channel #21
528	PERI_MS_PPU_FX_PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR0, Channel #22

外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
529	PERI_MS_PPU_FX_PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR0, Channel #23
530	PERI_MS_PPU_FX_PASS0_SAR0_CH24_CH	0x40900E00	0x00000040	SAR0, Channel #24
531	PERI_MS_PPU_FX_PASS0_SAR0_CH25_CH	0x40900E40	0x00000040	SAR0, Channel #25
532	PERI_MS_PPU_FX_PASS0_SAR0_CH26_CH	0x40900E80	0x00000040	SAR0, Channel #26
533	PERI_MS_PPU_FX_PASS0_SAR0_CH27_CH	0x40900EC0	0x00000040	SAR0, Channel #27
534	PERI_MS_PPU_FX_PASS0_SAR0_CH28_CH	0x40900F00	0x00000040	SAR0, Channel #28
535	PERI_MS_PPU_FX_PASS0_SAR0_CH29_CH	0x40900F40	0x00000040	SAR0, Channel #29
536	PERI_MS_PPU_FX_PASS0_SAR0_CH30_CH	0x40900F80	0x00000040	SAR0, Channel #30
537	PERI_MS_PPU_FX_PASS0_SAR0_CH31_CH	0x40900FC0	0x00000040	SAR0, Channel #31
538	PERI_MS_PPU_FX_PASS0_SAR1_CH0_CH	0x40901800	0x00000040	SAR1, Channel #0
539	PERI_MS_PPU_FX_PASS0_SAR1_CH1_CH	0x40901840	0x00000040	SAR1, Channel #1
540	PERI_MS_PPU_FX_PASS0_SAR1_CH2_CH	0x40901880	0x00000040	SAR1, Channel #2
541	PERI_MS_PPU_FX_PASS0_SAR1_CH3_CH	0x409018C0	0x00000040	SAR1, Channel #3
542	PERI_MS_PPU_FX_PASS0_SAR1_CH4_CH	0x40901900	0x00000040	SAR1, Channel #4
543	PERI_MS_PPU_FX_PASS0_SAR1_CH5_CH	0x40901940	0x00000040	SAR1, Channel #5
544	PERI_MS_PPU_FX_PASS0_SAR1_CH6_CH	0x40901980	0x00000040	SAR1, Channel #6
545	PERI_MS_PPU_FX_PASS0_SAR1_CH7_CH	0x409019C0	0x00000040	SAR1, Channel #7
546	PERI_MS_PPU_FX_PASS0_SAR1_CH8_CH	0x40901A00	0x00000040	SAR1, Channel #8
547	PERI_MS_PPU_FX_PASS0_SAR1_CH9_CH	0x40901A40	0x00000040	SAR1, Channel #9
548	PERI_MS_PPU_FX_PASS0_SAR1_CH10_CH	0x40901A80	0x00000040	SAR1, Channel #10
549	PERI_MS_PPU_FX_PASS0_SAR1_CH11_CH	0x40901AC0	0x00000040	SAR1, Channel #11
550	PERI_MS_PPU_FX_PASS0_SAR1_CH12_CH	0x40901B00	0x00000040	SAR1, Channel #12
551	PERI_MS_PPU_FX_PASS0_SAR1_CH13_CH	0x40901B40	0x00000040	SAR1, Channel #13
552	PERI_MS_PPU_FX_PASS0_SAR1_CH14_CH	0x40901B80	0x00000040	SAR1, Channel #14
553	PERI_MS_PPU_FX_PASS0_SAR1_CH15_CH	0x40901BC0	0x00000040	SAR1, Channel #15
554	PERI_MS_PPU_FX_PASS0_SAR1_CH16_CH	0x40901C00	0x00000040	SAR1, Channel #16
555	PERI_MS_PPU_FX_PASS0_SAR1_CH17_CH	0x40901C40	0x00000040	SAR1, Channel #17
556	PERI_MS_PPU_FX_PASS0_SAR1_CH18_CH	0x40901C80	0x00000040	SAR1, Channel #18
557	PERI_MS_PPU_FX_PASS0_SAR1_CH19_CH	0x40901CC0	0x00000040	SAR1, Channel #19
558	PERI_MS_PPU_FX_PASS0_SAR1_CH20_CH	0x40901D00	0x00000040	SAR1, Channel #20
559	PERI_MS_PPU_FX_PASS0_SAR1_CH21_CH	0x40901D40	0x00000040	SAR1, Channel #21
560	PERI_MS_PPU_FX_PASS0_SAR1_CH22_CH	0x40901D80	0x00000040	SAR1, Channel #22
561	PERI_MS_PPU_FX_PASS0_SAR1_CH23_CH	0x40901DC0	0x00000040	SAR1, Channel #23
562	PERI_MS_PPU_FX_PASS0_SAR1_CH24_CH	0x40901E00	0x00000040	SAR1, Channel #24
563	PERI_MS_PPU_FX_PASS0_SAR1_CH25_CH	0x40901E40	0x00000040	SAR1, Channel #25
564	PERI_MS_PPU_FX_PASS0_SAR1_CH26_CH	0x40901E80	0x00000040	SAR1, Channel #26
565	PERI_MS_PPU_FX_PASS0_SAR1_CH27_CH	0x40901EC0	0x00000040	SAR1, Channel #27
566	PERI_MS_PPU_FX_PASS0_SAR1_CH28_CH	0x40901F00	0x00000040	SAR1, Channel #28
567	PERI_MS_PPU_FX_PASS0_SAR1_CH29_CH	0x40901F40	0x00000040	SAR1, Channel #29
568	PERI_MS_PPU_FX_PASS0_SAR1_CH30_CH	0x40901F80	0x00000040	SAR1, Channel #30
569	PERI_MS_PPU_FX_PASS0_SAR1_CH31_CH	0x40901FC0	0x00000040	SAR1, Channel #31
570	PERI_MS_PPU_FX_PASS0_SAR2_CH0_CH	0x40902800	0x00000040	SAR2, Channel #0
571	PERI_MS_PPU_FX_PASS0_SAR2_CH1_CH	0x40902840	0x00000040	SAR2, Channel #1
572	PERI_MS_PPU_FX_PASS0_SAR2_CH2_CH	0x40902880	0x00000040	SAR2, Channel #2
573	PERI_MS_PPU_FX_PASS0_SAR2_CH3_CH	0x409028C0	0x00000040	SAR2, Channel #3



外设保护单位固定结构配对

表 22-1 PPU 固定结构配对 (续)

Pair no.	PPU fixed structure pair	Address	Size	Description
574	PERI_MS_PPU_FX_PASS0_SAR2_CH4_CH	0x40902900	0x00000040	SAR2, Channel #4
575	PERI_MS_PPU_FX_PASS0_SAR2_CH5_CH	0x40902940	0x00000040	SAR2, Channel #5
576	PERI_MS_PPU_FX_PASS0_SAR2_CH6_CH	0x40902980	0x00000040	SAR2, Channel #6
577	PERI_MS_PPU_FX_PASS0_SAR2_CH7_CH	0x409029C0	0x00000040	SAR2, Channel #7
578	PERI_MS_PPU_FX_PASS0_TOP	0x409F0000	0x00001000	PASS0 SAR main



23 总线主控器

仲裁器（闪存控制器的一部分）根据主控标识符执行基于优先级的仲裁。每个总线主控都有一个专用的4位主控标识符。该主控标识符用于总线仲裁和IPC功能。

表 23-1 用于访问和保护控制的总线主控器

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for CM0+
1	CPUSS_MS_ID_CRYPT0	Master ID for Crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA0
5	CPUSS_MS_ID_SLOW0	Master ID for External AHB-Lite Master 0 (SDHC)
6	CPUSS_MS_ID_SLOW1	Master ID for External AHB-Lite Master 1 (ETH0)
13	CPUSS_MS_ID_CM7_1	Master ID for CM7_1
14	CPUSS_MS_ID_CM7_0	Master ID for CM7_0
15	CPUSS_MS_ID_TC	Master ID for DAP Tap Controller

杂项配置

24 杂项配置

表 24-1 CYT3BB/4BB 设备的杂项配置

Sl. No.	Configuration	Number/instances	Description
0	SRSS_NUM_CLKPATH	7	Number of clock paths. One for each of FLL, PLL, Direct and CSV
1	SRSS_NUM_HFROOT	8	Number of CLK_HFs present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_PERI_PCLK_PCLK_GROUP_NR	2	Number of asynchronous PCLK groups
4	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_8_VECT	3	Group 0, Number of divide-by-8 clock dividers
5	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_16_VECT	1	Group 0, Number of divide-by-16 clock dividers
7	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_CLOCK_VECT	6	Group 0, Number of programmable clocks [1, 256]
8	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_8_VECT	16	Group 1, Number of divide-by-8 clock dividers
9	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_16_VECT	17	Group 1, Number of divide-by-16 clock dividers
10	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_24_5_VECT	16	Group 1, Number of divide-by-24.5 clock dividers
11	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_CLOCK_VECT	121	Group 1, Number of programmable clocks [1, 256]
12	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
13	CPUSS_CM7_0_FPU_LVL	2	CM7_0 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU
14	CPUSS_CM7_0_MPU_NR	16	Number of MPU regions in CM7_0
15	CPUSS_CM7_0_ICACHE_SIZE	16	CM7_0 Instruction cache (ICACHE) size in KB
16	CPUSS_CM7_0_DCACHE_SIZE	16	CM7_0 Data cache size (DCACHE) in KB
17	CPUSS_CM7_0_ITCM_SIZE	16	CM7_0 Instruction TCM (ITCM) size in KB
18	CPUSS_CM7_0_DTCM_SIZE	16	CM7_0 Data TCM (DTCM) size in KB
19	CPUSS_CM7_1_FPU_LVL	2	CM7_1 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU
20	CPUSS_CM7_1_MPU_NR	16	Number of MPU regions in CM7_1
21	CPUSS_CM7_1_ICACHE_SIZE	16	CM7_1 Instruction cache (ICACHE) size in KB
22	CPUSS_CM7_1_DCACHE_SIZE	16	CM7_1 Data cache size (DCACHE) in KB
23	CPUSS_CM7_1_ITCM_SIZE	16	CM7_1 Instruction TCM (ITCM) size in KB
24	CPUSS_CM7_1_DTCM_SIZE	16	CM7_1 Data TCM (DTCM) size in KB
25	CPUSS_DW0_CH_NR	100	Number of P-DMA0 channels
26	CPUSS_DW1_CH_NR	58	Number of P-DMA1 channels
27	CPUSS_DMACH_CH_NR	8	Number of M-DMA0 controller channels
28	CPUSS_CRYPTO_BUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
29	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
30	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM7_0 access 2 - Reserved for CM7_1 access 3 - Reserved for DAP access Remaining for user purposes
31	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of S MPU protection structures
32	SCBx_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports CMD_RESP mode
33	TCPWM0_TR_ONE_CNT_NR	3	Number of input triggers per counter, routed to one counter
34	TCPWM0_TR_ALL_CNT_NR	27	Number of input triggers routed to all counters, based on the pin package
35	TCPWM0_GRP_NR	3	Number of TCPWM0 counter groups
36	TCPWM0_GRP_NR0_GRP_GRP_CNT_NR	63	Number of counters per TCPWM0 Group #0



杂项配置

表 24-1 CYT3BB/4BB 器件的杂项配置 (续)

Sl. No.	Configuration	Number/instances	Description
37	TCPWM0_GRP_NR0_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #0
38	TCPWM0_GRP_NR1_GRP_GRP_CNT_NR	12	Number of counters per TCPWM0 Group #1
39	TCPWM0_GRP_NR1_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #1
40	TCPWM0_GRP_NR2_GRP_GRP_CNT_NR	8	Number of counters per TCPWM0 Group #2
41	TCPWM0_GRP_NR2_CNT_GRP_CNT_WIDTH	32	Counter width in number of bits per TCPWM0 Group #2
42	CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE	32	Message RAM size in KB shared by all the channels
43	EVTGEN_COMP_STRUCT_NR	16	Number of Event Generator comparator structures

25 开发支持

CYT3BB/4BB 拥有丰富的文档、编程工具和在线资源，协助开发过程。请访问www.infineon.com 了解更多信息。

25.1 文档

一系列文档支持 CYT3BB/4BB，确保您能够快速找到问题的答案。本节列出了一些关键文档。

25.1.1 软件用户指南

使用示例驱动程序库以及第三方 IDE（例如 IAR EWARM 和 GHS Multi）的分步指南。

25.1.2 技术参考手册

技术参考手册 (TRM) 包含使用 CYT3BB/4BB 器件所需的所有技术细节，包括所有寄存器的完整描述。TRM 可在www.infineon.com的文档部分找到。

25.2 工具

CYT3BB/4BB 受第三方开发工具生态系统（如 IAR 和 GHS）支持。英飞凌的编程工具也支持 CYT3BB/4BB，可使用英飞凌的 MiniProg4 或 Segger J-link 进行编程、擦除或读取。更多详细信息请参阅www.infineon.com上的文档部分。

26 电气规格

26.1 绝对最大额定值

在表 26-1 列出的最小和最大限值之外的条件下使用该器件可能会对器件造成永久性损坏。暴露于表 26-1 限制的条件下但超出正常操作时间可能会影响器件的可靠性。最大存储温度为 150 °C，符合 JEDEC 标准 JESD22-A103，高温存储寿命。在表 26-1 的限制条件下运行时但超出正常操作范围后，器件可能无法按规范操作。

功率考虑

平均芯片结温 T_J （以 °C 为单位）可使用方程式 1 计算：

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{方程式. 1}$$

其中

T_A 是环境温度，单位为摄氏度（°C）。

θ_{JA} 是封装结点至环境的热阻抗，单位为 °C/W。

P_D 是 P_{INT} 与 P_{IO} 之和（ $P_D = P_{INT} + P_{IO}$ ）。

P_{INT} 为芯片内部功率。（ $P_{INT} = V_{DD} \times I_{DD} + V_{DDA} \times I_A$ ）

P_{IO} 表示输入和输出引脚上的功耗；由用户确定。

对于大多数应用， $P_{IO} < P_{INT}$ 可以忽略。

另一方面，如果器件配置为连续驱动外部模块和/或存储器，则 P_{IO} 可能很重要。

警告

- 需要遵循推荐的运行条件来确保半导体器件的正常运行。当器件在这些条件下运行时，器件的所有电气特性均得到保证。
- 在除各自“详细信息/条件”中所述以外的任何条件下运行都可能对器件的可靠性产生不利影响，并可能导致器件故障。
- 对于本数据表中未提及的任何使用、运行条件或组合，不提供任何保证。如果您想在此处列出的条件以外的任何条件下运行器件，请联系销售代表。

电气规格

表 26-1 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID10	V_{DD_ABS}	V_{DD} power supply voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{SSD} + 6.0$	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31
SID10B	$V_{DDIO_1_ABS}$	V_{DDIO_1} power supply voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{SSD} + 6.0$	V	For ports 6, 7, 8, 9, 32
SID10C	$V_{DDIO_2_ABS}$	V_{DDIO_2} power supply voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{SSD} + 6.0$	V	For ports 10, 11, 12, 13, 14, 15, 26, 27
SID10D	$V_{DDIO_3_ABS}$	V_{DDIO_3} power supply voltage ^[42]	$V_{SSIO_3} - 0.3$	–	$V_{SSIO_3} + 4.0$	V	For ports 24, 25
SID11	V_{DDA_ABS}	V_{DDA} analog power supply voltage ^[42]	$V_{SSA} - 0.3$	–	$V_{SSA} + 6.0$	V	$V_{DDIO_2} = V_{DDA}$
SID12	V_{REFH_ABS}	Analog reference voltage, HIGH ^[42]	$V_{SSA} - 0.3$	–	$V_{SSA} + 6.0$	V	$V_{REFH} \leq (V_{DDA} + 0.3 \text{ V})$
SID12A	V_{REFL_ABS}	Analog reference voltage, LOW ^[42]	$V_{SSA} - 0.3$	–	$V_{SSA} + 0.3$	V	
SID13	V_{CCD_ABS}	V_{CCD} Power supply voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{SSD} + 1.21$	V	
SID15A	V_{I0_ABS}	Input voltage ^[42]	$V_{SSD} - 0.5$	–	$V_{DD} + 0.5$	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31
SID15B	V_{I1_ABS}	Input voltage ^[42]	$V_{SSD} - 0.5$	–	$V_{DDIO_1} + 0.5$	V	For ports 6, 7, 8, 9, 32
SID15C1	V_{I2_ABS}	Input voltage ^[42]	$V_{SSD} - 0.5$	–	$V_{DDIO_2} + 0.5$	V	For ports 10, 11, 12, 13, 14, 15, 26, 27
SID15D	V_{I3_ABS}	Input voltage ^[42]	$V_{SSIO_3} - 0.5$	–	$V_{DDIO_3} + 0.5$	V	For ports 24, 25
SID15F	V_{I5_ABS}	Input voltage ^[42]	$V_{SSD} - 0.5$	–	$V_{DD} + 0.5$	V	For EXT_PS_CTL0 in external PMIC/transistor mode, EXT_PS_CTL1 in external transistor mode.
SID16	V_{IA_ABS}	Analog input voltage ^[42]	$V_{SSA} - 0.3$	–	$V_{DDA} + 0.3$	V	
SID17A	V_{O0_ABS}	Output voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{DD} + 0.3$	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31
SID17B	V_{O1_ABS}	Output voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{DDIO_1} + 0.3$	V	For ports 6, 7, 8, 9, 32
SID17C1	V_{O2_ABS}	Output voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{DDIO_2} + 0.3$	V	For ports 10, 11, 12, 13, 14, 15, 26, 27
SID17D	V_{O3_ABS}	Output voltage ^[42]	$V_{SSIO_3} - 0.3$	–	$V_{DDIO_3} + 0.3$	V	For ports 24, 25

注:

42. 这些参数基于 $V_{SSD} = V_{SSA} = V_{SSIO_3} = 0.0 \text{ V}$ 的条件。

电气规格

表 26-1 绝对最大额定值 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID17F	V_{O4_ABS}	Output voltage ^[42]	$V_{SSD} - 0.3$	–	$V_{DD} + 0.3$	V	For EXT_PS_CTL1/2 in external PMIC mode, DRV_VOUT in external transistor mode
SID18	$ I_{CLAMP_ABS} $	Maximum clamp current ^[43, 44, 45]	–5	–	5	mA	
SID18A	$I_{CLAMP_SUPPLY_POS_ABS}$	Maximum positive clamp current per I/O supply pin. Limit applies to I/O supply pin closest to the B+ injected current ^[46]	–	–	10	mA	+B injected DC current is not allowed for Ports 11 and 21.
SID18B	$I_{CLAMP_SUPPLY_NEG_ABS}$	Maximum negative clamp current per I/O ground pin. Limit applies to I/O supply pin closest to the B+ injected current ^[46]	–	–	10	mA	+B injected DC current is not allowed for Ports 11 and 21.
SID18C	$I_{CLAMP_TOTAL_POS_ABS}$	Maximum positive clamp current per I/O supply, if not limited by the per supply pin (based on SID18A).	–	–	50	mA	
SID18D	$I_{CLAMP_TOTAL_NEG_ABS}$	Maximum negative clamp current per I/O ground, if not limited by the per supply pin (based on SID18B).	–	–	50	mA	
SID20A	I_{OL1A_ABS}	LOW-level maximum output current ^[47]	–	–	6	mA	GPIO_STD, configured for drive_sel<1:0>=0b0X
SID20B	I_{OL1B_ABS}	LOW-level maximum output current ^[47]	–	–	2	mA	GPIO_STD, configured for drive_sel<1:0>=0b10
SID20C	I_{OL1C_ABS}	LOW-level maximum output current ^[47]	–	–	1	mA	GPIO_STD, configured for drive_sel<1:0>=0b11
SID21A	I_{OL2A_ABS}	LOW-level maximum output current ^[47]	–	–	6	mA	GPIO_ENH, configured for drive_sel<1:0>=0b0X

注:

43. 必须配备限流电阻, 使得I/O引脚的电流在任何时候都不超过额定值, 包括功率瞬变期间。请参阅图 26-1 了解有关推荐电路的更多信息。

44. V_{DD} 和 V_{DDIO} 必须有足够的负载或受到保护, 以防止它们被钳位电流拉出建议的工作范围。

45. 当[43], [44]的条件满足且满足 SID18A/B/C/D时, $|I_{CLAMP_ABS}|$ 取代了 V_{IA_ABS} 和 V_{L_ABS} 。

46. “更近”的定义取决于封装。在 TEQFP 封装中, “最接近”是通过计算引脚数来确定的。例如, 在 176-TEQFP 封装中, P17.4 (引脚 120) 距离引脚 110 上的 V_{DD} 比距离引脚 132 上的 V_{DD} 更近。端口 11 和 21 不应用于注入电流。注入电流的影响仅针对 GPIO_STD/GPIO_ENH 类型 I/O 进行定义。在 BGA 封装中, 以下 IO 端口组被视为具有单独的电源引脚: 端口 0、1、2、22、23 和 28; 端口 3、4、5、29、30 和 31; 端口 6、7、8、9 和 32; 端口 10、12、13、14、15、26 和 27; 端口 16 和 17; 端口 18、19 和 20。

47. 最大输出电流是流过任何一个 I/O 的峰值电流。

电气规格
表 26-1 绝对最大额定值 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID21B	I_{OL2B_ABS}	LOW-level maximum output current ^[47]	–	–	2	mA	GPIO_ENH, configured for drive_sel<1:0>= 0b10
SID21C	I_{OL2C_ABS}	LOW-level maximum output current ^[47]	–	–	1	mA	GPIO_ENH, configured for drive_sel<1:0>= 0b11
SID22A	I_{OL3A_ABS}	LOW-level maximum output current ^[47]	–	–	10	mA	HSIO, configured for drive_sel<1:0>= 0b00
SID22B	I_{OL3B_ABS}	LOW-level maximum output current ^[47]	–	–	2	mA	HSIO, configured for drive_sel<1:0>= 0b01
SID22C	I_{OL3C_ABS}	LOW-level maximum output current ^[47]	–	–	1	mA	HSIO, configured for drive_sel<1:0>= 0b10
SID22D	I_{OL3D_ABS}	LOW-level maximum output current ^[48]	–	–	0.5	mA	HSIO, configured for drive_sel<1:0>= 0b11
SID23A	I_{OL4A_ABS}	Sink maximum current ^[48]	–	–	4	mA	For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode
SID23B	I_{OL4B_ABS}	Sink average current ^[50]	–	–	1	mA	For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode
SID23C	I_{OL4C_ABS}	Sink maximum current ^[47]	–	–	25	mA	For pin DRV_VOUT in external transistor mode
SID26A	$\Sigma I_{OL_ABS_GP_IO}$	LOW-level total output current ^[49]	–	–	50	mA	
SID26B	$\Sigma I_{OL_ABS_HS_IO}$	LOW-level total output current ^[52]	–	–	85	mA	
SID27A	I_{OH1A_ABS}	HIGH-level maximum output current ^[48]	–	–	–5	mA	GPIO_STD, configured for drive_sel<1:0>= 0b0X

表 26-1 绝对最大额定值 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID27B	I_{OH1B_ABS}	HIGH-level maximum output current ^[48]	–	–	–2	mA	GPIO_STD, configured for drive_sel<1:0>= 0b10
SID27C	I_{OH1C_ABS}	HIGH-level maximum output current ^[48]	–	–	–1	mA	GPIO_STD, configured for drive_sel<1:0>= 0b11
SID28A	I_{OH2A_ABS}	HIGH-level maximum output current ^[48]	–	–	–5	mA	GPIO_ENH, configured for drive_sel<1:0>= 0b0X
SID28B	I_{OH2B_ABS}	HIGH-level maximum output current ^[48]	–	–	–2	mA	GPIO_ENH, configured for drive_sel<1:0>= 0b10
SID28C	I_{OH2C_ABS}	HIGH-level maximum output current ^[48]	–	–	–1	mA	GPIO_ENH, configured for drive_sel<1:0>= 0b11
SID29A	I_{OH3A_ABS}	HIGH-level maximum output current ^[48]	–	–	–10	mA	HSIO, configured for drive_sel<1:0>= 0b00
SID29B	I_{OH3B_ABS}	HIGH-level maximum output current ^[48]	–	–	–2	mA	HSIO, configured for drive_sel<1:0>= 0b01
SID29C	I_{OH3C_ABS}	HIGH-level maximum output current ^[48]	–	–	–1	mA	HSIO, configured for drive_sel<1:0>= 0b10
SID29D	I_{OH3D_ABS}	HIGH-level maximum output current ^[48]	–	–	–0.5	mA	HSIO, configured for drive_sel<1:0>= 0b11
SID30A	I_{OH4A_ABS}	Source maximum current ^[48]	–	–	–4	mA	For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode.
SID30B	I_{OH4B_ABS}	Source maximum current ^[48]	–	–	–25	mA	For pin DRV_VOUT in external transistor mode.

注:

48. 最大输出电流是流过任何一个 I/O 的峰值电流。

49. 总输出电流是流过所有 GPIO_STD 和 GPIO_ENH I/O 的最大电流。

电气规格

表 26-1 绝对最大额定值 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID30C	I_{OH4C_ABS}	Source average current ^[50]	–	–	–1	mA	For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode.
SID30D	I_{OH4D_ABS}	Source average current ^[50]	–	–	–12	mA	For pin DRV_VOUT in external transistor mode.
SID33A	$\Sigma I_{OH_ABS_GPIO}$	HIGH-level total output current ^[51]	–	–	–50	mA	
SID33B	$\Sigma I_{OH_ABS_HSIO}$	HIGH-level total output current ^[52]	–	–	–85	mA	
SID33D	PIO	Total output power dissipation ^[53]	–	–	307	mW	
SID34	P_D	Power dissipation for external PMIC/transistor mode	–	–	1000	mW	T_J should not exceed 150 °C
SID34A	P_D	Power dissipation for internal regulator mode	–	–	2000	mW	T_J should not exceed 150 °C
SID35	T_A	Ambient temperature	–40	–	105	°C	For S-grade devices
SID36	T_A	Ambient temperature	–40	–	125	°C	For E-grade devices
SID37	T_{STG}	Storage temperature	–55	–	150	°C	
SID38	T_J	Operating junction temperature	–40	–	150	°C	
SID39A	V_{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	
SID39B1	V_{ESD_CDM1}	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B2	V_{ESD_CDM2}	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	I_{LU}	The maximum pin current the device can tolerate before triggering a latch-up	–100	–	100	mA	

注：

50. 平均输出电流定义为10ms周期内流过任一引脚的平均电流值。平均值为工作电流×工作比率。工作电流周期超过平均电流的规格应小于 100 ns。
51. 总输出电流是流过所有 GPIO_STD 和 GPIO_ENH I/O 的最大电流。
52. 总输出电流是流过所有 HSIO_STD I/O 的最大电流。
53. 总产出功耗是流经所有I/O的最大功耗。PIO = ($V_{DD} + V_{DDIO_1} + V_{DDIO_2}$) × ($|I_{OH_ABS_GPIO}| + |I_{OL_ABS_GPIO}|$) + V_{DDIO_3} × ($|I_{OH_ABS_HSIO}| + |I_{OL_ABS_HSIO}|$)

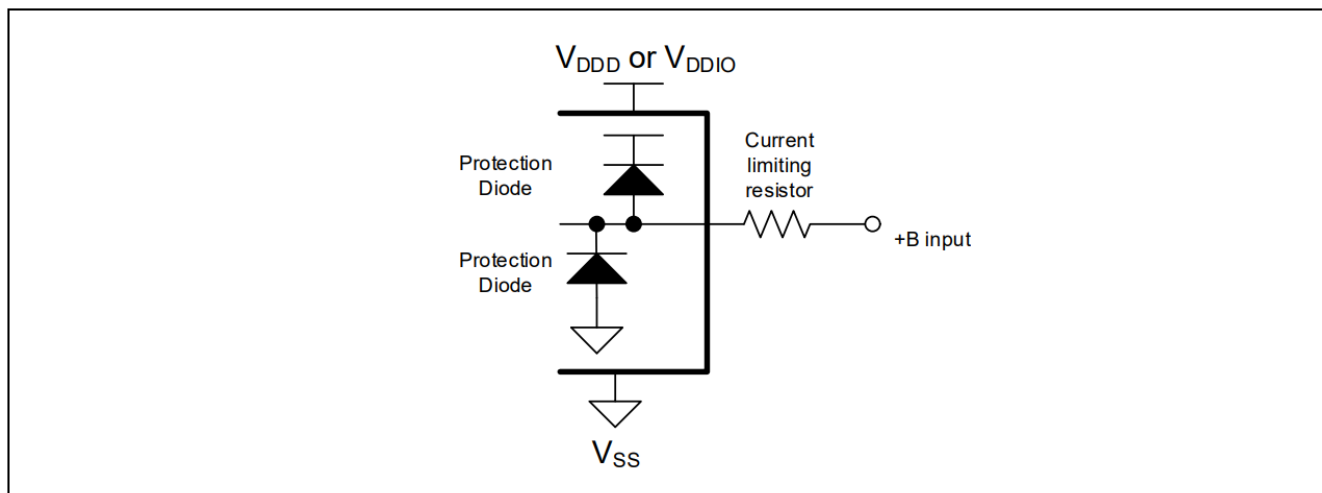


图 26-1 推荐电路示例^[54]

警告:

半导体器件可能因施加超过绝对最大额定值的压力（包括但不限于电压、电流或温度）而导致永久损坏。不要超过任何这些额定值。

注:

⁵⁴. +B 是电池正极电压，约为 45 V。

26.2 器件级规范

表 26-2 推荐的工作条件

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID40	$V_{DDDD}, V_{DDDA}, V_{DDIO_1}, V_{DDIO_2}$	Power supply voltage ^[55]	2.7 ^[56]	–	5.5 ^[57]	V	
SID40A	$V_{DDIO_1_EFP}$	Power supply voltage for eFuse programming ^[58]	3	–	5.5	V	
SID40B	V_{DDIO_3}	Power supply voltage	2.7	–	3.6	V	
SID40C	V_{CCD}	External V_{CCD} power supply	1.10	1.15	1.20	V	External V_{CCD} power supply range when externally supplying V_{CCD}
SID41	C_{S1}	Smoothing capacitor ^[59, 60]	6.79	–	22	μF	

推荐的工作条件

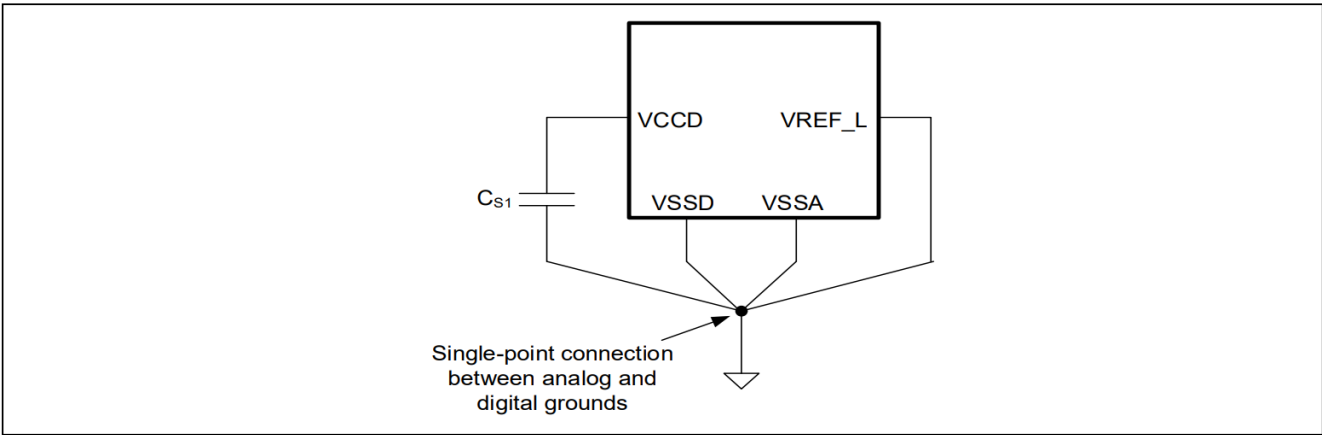


图 26-2 平滑电容器

平滑电容器应尽可能靠近 V_{CCD} 引脚放置。

注：

- 55. V_{DDDD} 、 V_{DDIO_1} 、 V_{DDIO_2} 、 V_{DDIO_3} 和 V_{DDDA} 没有任何顺序限制，可以按任意顺序建立。这些电源（ V_{DDDA} 和 V_{DDIO_2} ）的电压电平是独立的。使用 ADC 单元时，请参阅 12 位 SAR ADC DC 规格。
- 56. 3.0 V $\pm 10\%$ 支持 V_{DDDD} 和 V_{DDDA} 的较低 BOD 设置选项。此设置可为内部时序提供强大的保护，但 BOD 复位发生在低于指定工作条件的电压下。更高的 BOD 设置选项可用（与低至 3.0 V 一致）并确保满足所有工作条件。
- 57. 5.0 V $\pm 10\%$ 的过电压保护可通过更高的 OVD V_{DDDD} 和 V_{DDDA} 保护设置选项实现。此设置可为内部和接口时序提供强大的保护，但 OVD 复位发生在电压高于指定运行条件时。较低的 OVD 设置选项可用（与高至 5.0 V 一致），并保证满足所有运行条件。允许将 OVD V_{DDDD} 和 V_{DDDA} 过电压保护设置为更高的 OVD 设置范围，前提是累计持续时间小于 2 小时。注意，在过电压条件下，电气参数无法得到保证。
- 58. eFuse 编程必须在部件处于“安静”状态时进行，尽量减少活动（最好只有 JTAG 或单个 LIN/CAN 通道在 V_{DDDD} 域， V_{DDIO_1} 上无活动）。
- 59. 每个芯片都需要一个平滑电容器 C_{S1} （而不是每个 V_{CCD} 引脚）。 V_{CCD} 引脚必须连接在一起，以确保低阻抗连接（请参阅图 26-2）。
- 60. 用于电源去耦或滤波的电容器在连续直流偏置下运行。许多使用直流电源的电容器提供的电容小于其目标电容值，并且其电容价值在其工作电压范围内不是恒定的。选择用于此器件的电容器时，请确保所选元件在设计中使用的特定温度和电压运行条件下提供所需的电容。虽然温度系数通常可以在零件目录中找到（例如 X7R、C0G、Y5V），但匹配的电压系数可能仅在组件数据表上提供或直接从制造商处获得。在实际运行条件下使用不能提供所需电容的组件可能会导致器件运行不符合数据表规格。

26.3 直流规范

表 26-3 DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
运行/睡眠模式							
SID49C14	$I_{DD_VDDD_CM07_8_1_4M}$	V_{DD} current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are disabled)	–	9	13	mA	CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off. All peripherals are disabled. No IO toggling. CM0+ and CM7_0 executing Dhrystone from flash with cache enabled. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF)
SID49C4	$I_{DD_VDDD_CM07_8_4M}$	V_{DD} current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are enabled)	–	10	141	mA	CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off. All peripherals are enabled. No IO toggling. CM0+ and CM7_0 executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 105^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF)
SID49G1	$I_{DD1_VCCD_CM7_250}$	V_{CCD} current in external PMIC/transistor mode, Active mode (CM7_0 at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled)	–	82	240	mA	PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125^{\circ}\text{C}$, $V_{CCD} = 1.20\text{ V}$, process worst (FF)
SID49G2	$I_{DD1_VDDD_CM7_250}$	V_{DD} current in external PMIC/transistor mode, Active mode (CM7_0 at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled)	–	7	9	mA	PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max $T_A = 125^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF)

电气规格
表 26-3 直流规格、CPU 电流和转换时间规格 (续)

 除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID50G1	$I_{DD1_VCCD_F250}$	V_{CCD} current in external PMIC/transistor mode, Active mode (CM7 CPUs at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled)	–	124	287	mA	PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125^{\circ}\text{C}$, $V_{CCD} = 1.20\text{ V}$, process worst (FF)
SID50G2	$I_{DD1_VDDD_F250}$	V_{DDD} current in external PMIC/transistor mode, Active mode (CM7 CPUs at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled)	–	7	9.3	mA	PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, process worst (FF)
SID53A4	$I_{DD2_8_VDDD_4M}$	V_{DDD} current in internal regulator mode. CM7_1=OFF, Other CPUs in Sleep	–	7	140	mA	IMO clocked at 8 MHz. All peripherals, PLL, FLL, peripheral clocks, interrupts, CSV, DMA are disabled. No IO toggling. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 105^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, process worst (FF)

电气规格

表 26-3 直流规格、CPU 电流和转换时间规格 (续)

除非另有说明, 所有规格均适用于 $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID58A	I_{DD_CWU2}	Average current for cyclic wake-up operation. This is the average current for the specified LPACTIVE mode and DeepSleep mode (RTC, WDT, and Event Generator operating).	–	60	198	μA	$T_A = 25\text{ }^{\circ}\text{C}$, 64-KB SRAM retention, Event generator operates with ILO0 in DeepSleep and LP Active, Smart I/O operates with ILO0, CM0+, CM7_0: Retain, CM7_1: OFF. Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $V_{DD} = 5.5\text{ V}$, process worst (FF) This average current is achieved under the following conditions. 1. MCU repetitively goes from DeepSleep to LP Active with a period of 32 ms. 2. One of the I/Os is toggled using Smart I/O to activate an external sensor connected to an analog input of A/D in DeepSleep 3. After 200 μs delay, the CM7_0 wakes up by Event generator trigger to LP Active mode with IMO and A/D conversion is triggered by software. 4. Group A/D conversion is performed on 5 channels with the sampling time of 1 μs each. 5. Once the group A/D conversion is finished, and the results fit in the window of the range comparator, the I/O is toggled back by software to de-activate the sensor and the CM7_0 goes back to DeepSleep.

深度睡眠模式

SID64A4	I_{DD_DS64A4}	64-KB SRAM retention, ILO0 operation	–	50	138	μA	DeepSleep Mode (RTC, WDT and event generator operating, all other peripherals are off except for retention registers) CM0+, CM7_0: Retained $T_A = 25\text{ }^{\circ}\text{C}$ Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $V_{DD} = 5.5\text{ V}$, process worst (FF)
SID64C	I_{DD_DS64C}	64 KB SRAM retention, ILO0 operation	–	1.4	5.5	mA	DeepSleep Mode steady state at $T_A = 125\text{ }^{\circ}\text{C}$ (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), CM0+, CM7_0: Retained Typ: $V_{DD} = 5.0\text{ V}$, process worst (TT) Max: $V_{DD} = 5.5\text{ V}$, process worst (FF)

休眠模式

SID66	I_{DD_HIB1}	Hibernate Mode	–	8	–	μA	ILO0/WDT operating. All other peripherals, and all CPUs are off. $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, Process typ (TT)
SID66A	I_{DD_HIB2}	Hibernate Mode	–	–	180	μA	ILO0/WDT operating. All other peripherals, and all CPUs are off. $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, Process worst (FF)

电气规格

表 26-3 直流规格、CPU 电流和转换时间规格 (续)

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
功耗模式转型时间							
SID69	$t_{\text{ACT_DS}}$	Power down time from Active to DeepSleep	–	–	2.8	μs	When the IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID67	$t_{\text{DS_ACT}}$	DeepSleep to Active transition time (IMO clock)	–	–	$10^{[61]}$	μs	When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until wakeup.
SID67C	$t_{\text{DS_ACT1}}$	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	$26^{[61]}$	μs	When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.
SID67A	$t_{\text{DS_ACT_FLL}}$	DeepSleep to Active transition time (FLL clock)	–	–	$15^{[61]}$	μs	When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the FLL locks.
SID67D	$t_{\text{DS_ACT_FLL1}}$	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	$26^{[61]}$	μs	When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.
SID67B	$t_{\text{DS_ACT_PLL}}$	DeepSleep to Active transition time (PLL clock)	–	–	$60^{[61]}$	μs	When using the PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the PLL locks.
SID68	$t_{\text{HVR_ACT}}$	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) release until CM0+ begins executing ROM boot	–	–	265	μs	Without boot runtime, guaranteed by design
SID68A	$t_{\text{LVR_ACT}}$	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot	–	–	10	μs	Without boot runtime. Guaranteed by design
SID68B	$t_{\text{LVR_DS}}$	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	μs	Without boot runtime. Guaranteed by design
SID80A	$t_{\text{RB_N}}$	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	1640	μs	Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later)
SID80B	$t_{\text{RB_S}}$	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	2330	μs	Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later)
SID81A	t_{FB}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	80	μs	Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later), Listen window = 0 ms
SID81B	$t_{\text{FB_A}}$	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	5000	μs	Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later), Listen window = 0 ms, Public key exponent $e = 0x010001$, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-2048.

注:

61. 在低温 -5°C 至 -40°C 下，深度睡眠到运行模式的转换时间可能比指示的最大时间高出 20 μs 。

电气规格

表 26-3 直流规格、CPU 电流和转换时间规格 (续)

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID80A_2	$t_{RB_N_2}$	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	2640	μs	Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554)
SID80B_2	$t_{RB_S_2}$	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	3890	μs	Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554)
SID81A_2	t_{FB_2}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	200	μs	Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554), Listen window = 0 ms
SID81B_2	$t_{FB_A_2}$	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	10000	μs	Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-2048.

稳压器规格

SID600	V_{CCD}	Core supply voltage (transient range)	1.05	1.1	1.15	V	
SID600A	$V_{\text{CCD_S}}$	Core supply voltage (static range, no load)	1.075	1.1	1.125	V	Guaranteed by design
SID601	$I_{\text{DDD_ACT}}$	Regulator operating current in Active/Sleep mode	–	900	1500	μA	Guaranteed by design
SID602	$I_{\text{DDD_DPSLP}}$	Regulator operating current in DeepSleep mode	–	1.5	20	μA	Guaranteed by design
SID603	I_{RUSH}	In-rush current	–	–	850	mA	Average V_{DDD} current until C_{s1} (connected to V_{CCD} pin) is charged after Active regulator is turned on
SID604	I_{ILDOUT}	Internal regulator output current for operation	–	–	300	mA	
SID605	I_{HCROUT}	High current regulator output current for operation	–	–	600	mA	Using an external pass transistor
SID606	$V_{\text{OL_HCR}}$	Output voltage LOW level for external PMIC enable output (EXT_PS_CTL1)	–	–	0.5	V	$I_{\text{OL}} = 1 \text{ mA}$
SID606A	$V_{\text{OH_HCR}}$	Output voltage HIGH level for external PMIC enable output (EXT_PS_CTL1)	$V_{\text{DDD}} - 0.5$	–	–	V	$I_{\text{OH}} = -1 \text{ mA}$
SID607	$V_{\text{IH_HCR}}$	Input voltage HIGH threshold for external PMIC power OK input (EXT_PS_CTL0)	$0.7 \times V_{\text{DDD}}$	–	–	V	
SID607A	$V_{\text{IL_HCR}}$	Input voltage LOW threshold for external PMIC power OK input (EXT_PS_CTL0)	–	–	$0.3 \times V_{\text{DDD}}$	V	
SID607B	$V_{\text{HYS_HCR}}$	Hysteresis for external PMIC power OK input (EXT_PS_CTL0)	$0.05 \times V_{\text{DDD}}$	–	–	V	
SID608	$I_{\text{DRV_OUT}}$	DRV_VOUT pin output current to external NPN base current	–	–	9	mA	See Architecture TRM for external NPN transistor selection

26.4 复位规格

除非另有说明，所有规格均适用于-40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 26-4 XRES_L复位

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
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XRES_L DC 规格

SID73	I _{IDD_XRES}	I _{DD} when XRES_L asserted	–	–	2.5	mA	Max: T _A = 125 °C, V _{DDD} = 5.5 V, V _{CCD} = 1.15 V, process worst (FF)
SID74	V _{IH}	Input voltage HIGH threshold	0.7 × V _{DDD}	–	–	V	CMOS Input
SID75	V _{IL}	Input voltage LOW threshold	–	–	0.3 × V _{DDD}	V	CMOS Input
SID76	R _{PULLUP}	Pull-up resistor	7	–	20	kΩ	
SID77	C _{IN}	Input capacitance	–	–	5	pF	
SID78	V _{HYSXRES}	Input voltage hysteresis	0.05 × V _{DDD}	–	–	V	

XRES_L AC 规格

SID70	t _{XRES_ACT}	XRES_L deasserted to Active transition time	–	–	265	μs	Without boot runtime Guaranteed by design
SID71	t _{XRES_PW}	XRES_L pulse width	5	–	–	μs	
SID72	t _{XRES_FT}	Pulse suppression width	100	–	–	ns	

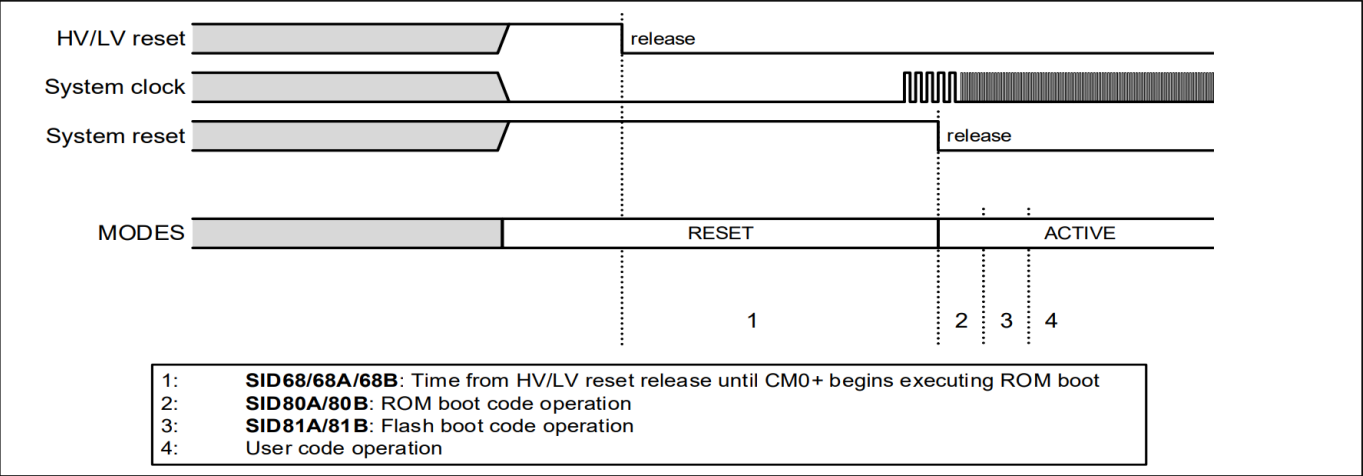


图 26-3 复位顺序

电气规格

26.5 I/O

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 26-5 I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
端口 P1 至 P23、P26 至 P32 的 GPIO_STD 规格							
SID650	$V_{OL1_GPIO_STD}$	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 6\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b0X$, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID650C	$V_{OL1C_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 5\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b0X$, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID651	$V_{OL2_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 2\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b0X$, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} < 4.5\text{ V}$
SID652	$V_{OL3_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 1\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b10$, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} < 4.5\text{ V}$
SID652C	$V_{OL3C_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 2\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b10$, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID653	$V_{OL4_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 0.5\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b11$, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} < 4.5\text{ V}$
SID653C	$V_{OL4C_GPIO_STD}$	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 1\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b11$, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID654	$V_{OH1_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -2\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b0X$, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} < 4.5\text{ V}$
SID655	$V_{OH2_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -5\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b0X$, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID656	$V_{OH3_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -1\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b10$, $2.7\text{ V} \leq (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) < 4.5\text{ V}$
SID656C	$V_{OH3C_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -2\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b10$, $4.5\text{ V} \leq (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) \leq 5.5\text{ V}$
SID657	$V_{OH4_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -0.5\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b11$, $2.7\text{ V} \leq (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) < 4.5\text{ V}$
SID657C	$V_{OH4C_GPIO_STD}$	Output voltage HIGH level	$(V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) - 0.5$	–	–	V	$I_{OH} = -1\text{ mA}$ $\text{drive_sel} < 1:0 > = 0b11$, $4.5\text{ V} \leq (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2}) \leq 5.5\text{ V}$
SID658	$R_{PD_GPIO_STD}$	Pull-down resistance	25	50	100	k Ω	
SID659	$R_{PU_GPIO_STD}$	Pull-up resistance	25	50	100	k Ω	
SID660	$V_{IH_CMOS_GPIO_STD}$	Input voltage HIGH threshold in CMOS mode	$0.7 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	–	–	V	
SID661	$V_{IH_TTL_GPIO_STD}$	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	
SID662	$V_{IH_AUTO_GPIO_STD}$	Input voltage HIGH threshold in AUTO mode	$0.8 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	–	–	V	

电气规格

表 26-5 I/O 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID663	$V_{IL_CMOS_GPIO_STD}$	Input voltage LOW threshold in CMOS mode	–	–	$0.3 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	V	
SID664	$V_{IL_TTL_GPIO_STD}$	Input voltage LOW threshold in TTL mode	–	–	0.8	V	
SID665	$V_{IL_AUTO_GPIO_STD}$	Input voltage LOW threshold in AUTO mode	–	–	$0.5 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	V	
SID666	$V_{HYST_CMOS_GPIO_STD}$	Hysteresis in CMOS mode	$0.05 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	–	–	V	
SID668	$V_{HYST_AUTO_GPIO_STD}$	Hysteresis in AUTO mode	$0.05 \times (V_{DD}, V_{DDIO_1}, \text{ or } V_{DDIO_2})$	–	–	V	
SID669	$C_{in_GPIO_STD}$	Input pin capacitance	–	–	5	pF	For 10 MHz and 100 MHz
SID670	$I_{IL_GPIO_STD}$	Input leakage current	–250	0.02	250	nA	For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4. $V_{DDIO_1} = V_{DDIO_2} = V_{DD} = V_{DDA} = 5.5\text{ V}$, $V_{SSD} < V_I < V_{DD}, V_{DDIO_1}, V_{DDIO_2}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ Typ: $T_A = 25^\circ\text{C}$, $V_{DDIO_1} = V_{DDIO_2} = V_{DD} = V_{DDA} = 5.0\text{ V}$
SID670C	$I_{IL_GPIO_STD_B}$	Input leakage current	–700	0.02	700	nA	Only for P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4. $V_{DDIO_1} = V_{DDIO_2} = V_{DD} = V_{DDA} = 5.5\text{ V}$, $V_{SSD} < V_I < V_{DD}, V_{DDIO_1}, V_{DDIO_2}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ Typ: $T_A = 25^\circ\text{C}$, $V_{DDIO_1} = V_{DDIO_2} = V_{DD} = V_{DDA} = 5.0\text{ V}$
SID671	$t_R \text{ or } t_F \text{ (fast)}_{20_0_GPIO_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	10	ns	20-pF load, drive_sel<1:0>= 0b00
SID672	$t_R \text{ or } t_F \text{ (fast)}_{50_0_GPIO_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	50-pF load, drive_sel<1:0>= 0b00
SID673	$t_R \text{ or } t_F \text{ (fast)}_{20_1_GPIO_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	20-pF load, drive_sel<1:0>= 0b01
SID674	$t_R \text{ or } t_F \text{ (fast)}_{10_2_GPIO_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	10-pF load, drive_sel<1:0>= 0b10
SID675	$t_R \text{ or } t_F \text{ (fast)}_{6_3_GPIO_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	6-pF load, drive_sel<1:0>= 0b11
SID676	$t_F \text{ (fast)}_{100_GPIO_STD}$	Fall time (30% to 70% of V_{DDIO})	0.35	–	250	ns	10-pF to 400-pF load, $R_{PU} = 767\ \Omega$, drive_sel<1:0>= 0b00, Freq = 100 kHz
SID677	$t_F \text{ (fast)}_{400_GPIO_STD}$	Fall time (30% to 70% of V_{DDIO})	0.35	–	250	ns	10-pF to 400-pF load, $R_{PU} = 350\ \Omega$, drive_sel<1:0>= 0b00, Freq = 400 kHz
SID678	$f_{in_GPIO_STD}$	Input frequency	–	–	100	MHz	
SID679	$f_{OUT_GPIO_STD0H}$	Output frequency	–	–	50	MHz	20-pF load, drive_sel<1:0>= 00, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} \leq 5.5\text{ V}$
SID680	$f_{OUT_GPIO_STD0L}$	Output frequency	–	–	32	MHz	20-pF load, drive_sel<1:0>= 00, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO_1} \text{ or } V_{DDIO_2} < 4.5\text{ V}$

电气规格

表 26-5 I/O 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID681	$f_{\text{OUT_GPIO_STD1H}}$	Output frequency	–	–	25	MHz	20-pF load, drive_sel<1:0>= 01, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V
SID682	$f_{\text{OUT_GPIO_STD1L}}$	Output frequency	–	–	15	MHz	20-pF load, drive_sel<1:0>= 01, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V
SID683	$f_{\text{OUT_GPIO_STD2H}}$	Output frequency	–	–	25	MHz	10-pF load, drive_sel<1:0>= 10, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V
SID684	$f_{\text{OUT_GPIO_STD2L}}$	Output frequency	–	–	15	MHz	10-pF load, drive_sel<1:0>= 10, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V
SID685	$f_{\text{OUT_GPIO_STD3H}}$	Output frequency	–	–	15	MHz	6-pF load, drive_sel<1:0>= 11, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V
SID686	$f_{\text{OUT_GPIO_STD3L}}$	Output frequency	–	–	10	MHz	6-pF load, drive_sel<1:0>= 11, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V

P0 的 GPIO_ENH 规格

SID650A	V _{OL1_GPIO_ENH}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA drive_sel<1:0>= 0b0X, 2.7 V ≤ V _{DD} ≤ 5.5 V
SID650D	V _{OL1D_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA drive_sel<1:0>= 0b0X, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID651A	V _{OL2_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA drive_sel<1:0>= 0b0X, 2.7 V ≤ V _{DD} < 4.5 V
SID652A	V _{OL3_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA drive_sel<1:0>= 0b10, 2.7 V ≤ V _{DD} < 4.5 V
SID652D	V _{OL3D_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA drive_sel<1:0>= 0b10, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID653A	V _{OL4_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA drive_sel<1:0>= 0b11, 2.7 V ≤ V _{DD} < 4.5 V
SID653D	V _{OL4D_GPIO_ENH}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA drive_sel<1:0>= 0b11, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID654A	V _{OH1_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –2 mA drive_sel<1:0>= 0b0X, 2.7 V ≤ V _{DD} < 4.5 V
SID655A	V _{OH2_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –5 mA drive_sel<1:0>= 0b0X, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID656A	V _{OH3_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –1 mA drive_sel<1:0>= 0b10, 2.7 V ≤ V _{DD} < 4.5 V
SID656D	V _{OH3D_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –2 mA drive_sel<1:0>= 0b10, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID657A	V _{OH4_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –0.5 mA drive_sel<1:0>= 0b11, 2.7 V ≤ V _{DD} < 4.5 V
SID657D	V _{OH4D_GPIO_ENH}	Output voltage HIGH level	V _{DD} – 0.5	–	–	V	I _{OH} = –1 mA drive_sel<1:0>= 0b11, 4.5 V ≤ V _{DD} ≤ 5.5 V
SID658A	R _{PD_GPIO_ENH}	Pull-down resistance	25	50	100	kΩ	

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表 26-5 I/O 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID659A	$R_{PU_GPIO_ENH}$	Pull-up resistance	25	50	100	k Ω	
SID660A	$V_{IH_CMOS_GPIO_ENH}$	Input voltage HIGH threshold in CMOS mode	$0.7 \times V_{DD}$	–	–	V	
SID661A	$V_{IH_TTL_GPIO_ENH}$	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	
SID662A	$V_{IH_AUTO_GPIO_ENH}$	Input voltage HIGH threshold in AUTO mode	$0.8 \times V_{DD}$	–	–	V	
SID663A	$V_{IL_CMOS_GPIO_ENH}$	Input voltage LOW threshold in CMOS mode	–	–	$0.3 \times V_{DD}$	V	
SID664A	$V_{IL_TTL_GPIO_ENH}$	Input voltage LOW threshold in TTL mode	–	–	0.8	V	
SID665A	$V_{IL_AUTO_GPIO_ENH}$	Input voltage LOW threshold in AUTO mode	–	–	$0.5 \times V_{DD}$	V	
SID666A	$V_{HYST_CMOS_GPIO_ENH}$	Hysteresis in CMOS mode	$0.05 \times V_{DD}$	–	–	V	
SID668A	$V_{HYST_AUTO_GPIO_ENH}$	Hysteresis in AUTO mode	$0.05 \times V_{DD}$	–	–	V	
SID669A	$C_{in_GPIO_ENH}$	Input pin capacitance	–	–	5	pF	For 10 MHz and 100 MHz
SID670A	$I_{IL_GPIO_ENH}$	Input leakage current	–350	0.055	350	nA	$V_{DD} = V_{DDA} = 5.5\text{ V}$, $V_{SSD} < V_I < V_{DD}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ Typ: $T_A = 25^\circ\text{C}$, $V_{DD} = V_{DDA} = 5.0\text{ V}$
SID671A	t_R or t_F (fast) _{_20_0_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	10	ns	20-pF load, drive_sel<1:0> = 0b00, slow = 0
SID672A	t_R or t_F (fast) _{_50_0_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	50-pF load, drive_sel<1:0> = 0b00, slow = 0
SID673A	t_R or t_F (fast) _{_20_1_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	20-pF load, drive_sel<1:0> = 0b01, slow = 0
SID674A	t_R or t_F (fast) _{_10_2_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	10-pF load, drive_sel<1:0> = 0b10, slow = 0
SID675A	t_R or t_F (fast) _{_6_3_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	6-pF load, drive_sel<1:0> = 0b11, slow = 0
SID676A	t_{F_I2C} (slow) _{_GPIO_ENH}	Fall time (30% to 70% of V_{DDIO})	$20 \times (V_{DD} / 5.5)$	–	250	ns	10-pF to 400-pF load, drive_sel<1:0> = 0b00, slow = 1, minimum $R_{PU} = 400\ \Omega$
SID677A	t_R or t_F (slow) _{_20_GPI- O_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	$20 \times (V_{DD} / 5.5)$	–	160	ns	20-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 1 MHz
SID678A	t_R or t_F (slow) _{_400_G- PIO_ENH}	Rise time or fall time (10% to 90% of V_{DDIO})	$20 \times (V_{DD} / 5.5)$	–	250	ns	400-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 400 kHz
SID679A	$f_{IN_GPIO_ENH}$	Input frequency	–	–	100	MHz	
SID680A	$f_{OUT_GPIO_ENH0H}$	Output frequency	–	–	50	MHz	20-pF load, drive_sel<1:0> = 0b00, $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
SID681A	$f_{OUT_GPIO_ENH0L}$	Output frequency	–	–	32	MHz	20-pF load, drive_sel<1:0> = 0b00, $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$
SID682A	$f_{OUT_GPIO_ENH1H}$	Output frequency	–	–	25	MHz	20-pF load, drive_sel<1:0> = 0b01, $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
SID683A	$f_{OUT_GPIO_ENH1L}$	Output frequency	–	–	15	MHz	20-pF load, drive_sel<1:0> = 0b01, $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$
SID684A	$f_{OUT_GPIO_ENH2H}$	Output frequency	–	–	25	MHz	10-pF load, drive_sel<1:0> = 0b10, $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$

电气规格

表 26-5 I/O 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID685A	$f_{\text{OUT_GPIO_ENH2L}}$	Output frequency	–	–	15	MHz	10-pF load, drive_sel<1:0>= 0b10, $2.7\text{ V} \leq V_{\text{DD}} < 4.5\text{ V}$
SID686A	$f_{\text{OUT_GPIO_ENH3H}}$	Output frequency	–	–	15	MHz	6-pF load, drive_sel<1:0>= 0b11, $4.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$
SID687A	$f_{\text{OUT_GPIO_ENH3L}}$	Output frequency	–	–	10	MHz	6-pF load, drive_sel<1:0>= 0b11, $2.7\text{ V} \leq V_{\text{DD}} < 4.5\text{ V}$
端口 P24、P25 的 HSIO 规格							
SID651B	$V_{\text{OL_HB_HSSPI}}$	Output LOW voltage	–	–	0.2	V	$I_{\text{OL}} = 0.1\text{ mA}$, drive_sel<1:0>= 0b00
SID652B	$V_{\text{OL_eMMC}}$	Output LOW voltage	–	–	$0.125 \times V_{\text{DDIO_3}}$	V	$I_{\text{OL}} = 0.1\text{ mA}$, drive_sel<1:0>= 0b00
SID653B	$V_{\text{OL_SD}}$	Output LOW voltage	–	–	$0.125 \times V_{\text{DDIO_3}}$	V	$I_{\text{OL}} = 2\text{ mA}$, drive_sel<1:0>= 0b00
SID654B	V_{OL1}	Output LOW voltage	–	–	0.4	V	$I_{\text{OL}} = 10\text{ mA}$, drive_sel<1:0>= 0b00, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID655B	V_{OL2}	Output LOW voltage	–	–	0.4	V	$I_{\text{OL}} = 2\text{ mA}$, drive_sel<1:0>= 0b01, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID656B	V_{OL3}	Output LOW voltage	–	–	0.4	V	$I_{\text{OL}} = 1\text{ mA}$, drive_sel<1:0>= 0b10, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID656E	V_{OL4}	Output LOW voltage	–	–	0.4	V	$I_{\text{OL}} = 0.5\text{ mA}$, drive_sel<1:0>= 0b11, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID658B	$V_{\text{OH_HB_HSSPI}}$	Output HIGH voltage	$V_{\text{DDIO_3}} - 0.2$	–	–	V	$I_{\text{OH}} = -0.1\text{ mA}$ drive_sel<1:0>= 0b00
SID659B	$V_{\text{OH_eMMC}}$	Output HIGH voltage	$V_{\text{DDIO_3}} - (0.25 \times V_{\text{DDIO_3}})$	–	–	V	$I_{\text{OH}} = -0.1\text{ mA}$ drive_sel<1:0>= 0b00
SID660B	$V_{\text{OH_SD}}$	Output HIGH voltage	$V_{\text{DDIO_3}} - (0.25 \times V_{\text{DDIO_3}})$	–	–	V	$I_{\text{OH}} = -2\text{ mA}$ drive_sel<1:0>= 0b00
SID661B	V_{OH1}	Output HIGH voltage	$V_{\text{DDIO_3}} - 0.5$	–	–	V	$I_{\text{OH}} = -10\text{ mA}$ drive_sel<1:0>= 0b00, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID662B	V_{OH2}	Output HIGH voltage	$V_{\text{DDIO_3}} - 0.5$	–	–	V	$I_{\text{OH}} = -2\text{ mA}$ drive_sel<1:0>= 0b01, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID663B	V_{OH3}	Output HIGH voltage	$V_{\text{DDIO_3}} - 0.5$	–	–	V	$I_{\text{OH}} = -1\text{ mA}$ drive_sel<1:0>= 0b10, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID663E	V_{OH4}	Output HIGH voltage	$V_{\text{DDIO_3}} - 0.5$	–	–	V	$I_{\text{OH}} = -0.5\text{ mA}$ drive_sel<1:0>= 0b11, $V_{\text{DDIO_3}} = 2.7\text{ V}$
SID664B	R_{PD}	Pull-down resistance	25	50	100	k Ω	
SID665B	R_{PU}	Pull-up resistance	25	50	100	k Ω	
SID666B	$V_{\text{IH_CMOS}}$	Input HIGH voltage for HYPERBUS™ and HSSPI in CMOS mode	$0.7 \times V_{\text{DDIO_3}}$	–	–	V	vtrip_sel<1:0>= 0b00
SID668E	$V_{\text{IH_TTL}}$	Input Voltage HIGH threshold for TTL mode	2	–	–	V	vtrip_sel<1:0>= 0b01
SID669B	$V_{\text{IH_SD_eMMC}}$	Input HIGH voltage for SD and eMMC in CMOS mode	$0.625 \times V_{\text{DDIO_3}}$	–	–	V	vtrip_sel<1:0>= 0b00
SID669E	$V_{\text{IH_AUTO}}$	Input Voltage HIGH threshold in AUTO mode	$0.8 \times V_{\text{DDIO_3}}$	–	–	V	vtrip_sel<1:0>= 0b10
SID670B	$V_{\text{IL_CMOS}}$	Input LOW voltage for HYPERBUS™ and HSSPI in CMOS mode	–	–	$0.3 \times V_{\text{DDIO_3}}$	V	vtrip_sel<1:0>= 0b00



电气规格

表 26-5 I/O 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID672E	V_{IL_TTL}	Input Voltage LOW threshold for TTL mode	–	–	0.8	V	$vtrip_sel<1:0> = 0b01$
SID673B	$V_{IL_SD_eMMC}$	Input LOW voltage for SD and eMMC in CMOS mode	–	–	$0.25 \times V_{DDIO_3}$	V	$vtrip_sel<1:0> = 0b00$
SID673E	V_{IL_AUTO}	Input Voltage LOW threshold in AUTO mode	–	–	$0.5 \times V_{DDIO_3}$	V	$vtrip_sel<1:0> = 0b10$
SID674B	V_{HYST_CMOS}	Hysteresis in CMOS mode	$0.05 \times V_{DDIO_3}$	–	–	V	$vtrip_sel<1:0> = 0b00$
SID674F	V_{HYST_AUTO}	Hysteresis in AUTO mode	$0.05 \times V_{DDIO_3}$	–	–	V	$vtrip_sel<1:0> = 0b10$
SID675B	C_{IN}	Input pin capacitance	–	–	5	pF	For 10 MHz and 100 MHz
SID676B	I_{IL}	Input leakage current	–450	1.02	450	nA	$V_{DDIO_3} = 3.6\text{ V}$, $V_{SSIO_3} < V_I < V_{DDIO_3} - 40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDIO_3} = 3.3\text{ V}$
SID679B	$f_{IN_HB_HSSPI}$	Input frequency	–	–	100	MHz	
SID680B	f_{IN_eMMC}	Input frequency	–	–	52	MHz	
SID681B	f_{IN_SD}	Input frequency	–	–	50	MHz	
SID683B	$f_{OUT_HB_HSSPI}$	Output frequency	–	–	100	MHz	
SID684B	f_{OUT_eMMC}	Output frequency	–	–	52	MHz	
SID685B	f_{OUT_SD}	Output frequency	–	–	50	MHz	

GPIO输入规格

SID98	t_{FT}	Analog glitch filter (pulse suppression width)	–	–	$50^{[62]}$	ns	One filter per port
SID99	t_{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

注:

62. 如果需要更长的脉冲宽度抑制, 请使用智能 I/O。

26.6 模拟外设

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

26.6.1 SAR ADC

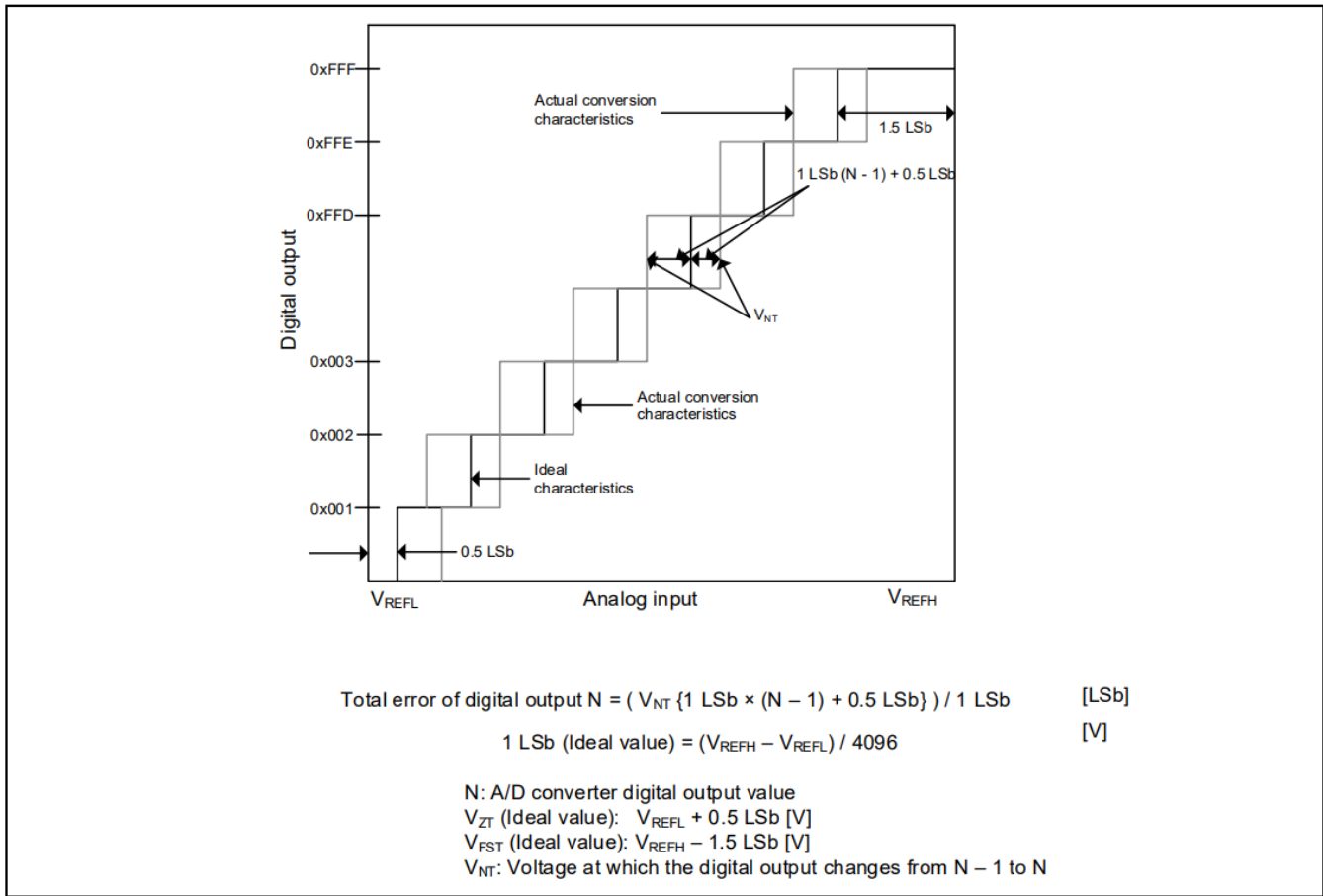


图 26-4 ADC特性及误差说明



电气规格

表 26-6 12 位 SAR ADC DC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	–	–	12	bits	
SID101	A_V _{INS}	Input voltage range	V _{REFL}	–	V _{REFH}	V	
SID102A	A_V _{DDA} ^[63]	V _{DDA} voltage range	2.7	–	5.5	V	
SID102	A_V _{REFH}	V _{REFH} voltage range	2.7	–	V _{DDA}	V	ADC performance degrades when high reference is higher than supply (V _{DDA})
SID103	A_V _{REFL}	V _{REFL} voltage range	V _{SSA}	–	V _{SSA}	V	ADC performance degrades when low reference is lower than ground
SID103A	V _{band_gap}	Internal band gap reference voltage	0.882	0.9	0.918	V	
SID19A	CLAMP_COUPLING_RATIO_POS	Ratio of current collected on a pin to the positive current injected into a neighboring pin	–	–	0.1	%	
SID19B	CLAMP_COUPLING_RATIO_NEG	Ratio of current collected on a pin to the negative current injected into a neighboring pin	–	–	1.2	%	
SID19C	R _{CLAMP_INTERNAL}	Internal pin resistance to current collection point	–	–	50	Ω	

26.6.2 计算相邻引脚的影响

基于SID19A，SID19B和SID19C的三个ADC规格可用于计算引脚泄漏以及由注入电流引起的ADC偏移，公式如下：

$$I_{LEAK} = I_{INJECTED} \times CLAMP_COUPLING_RATIO$$

$$V_{ERROR} = I_{LEAK} \times (R_{CLAMP_INTERNAL} + R_{SOURCE})$$

$$Code\ Error = V_{ERROR} \times 2^{12} / V_{REF}$$

其中

I_{INJECTED}是注入电流，单位为 mA。

I_{LEAK}是计算出的漏电流（单位为 mA）。

V_{ERROR}是由于漏电流而计算出的电压误差（以 V 为单位）。

V_{REF}是 ADC 基准电压（以 V 为单位）。

注：

63. 当 ADC[2] 启用时，V_{DDO} 必须大于 0.8 × V_{DDA}。当 ADC[0] 启用时，V_{DDIO_1} 必须大于 0.8 × V_{DDA}。

电气规格

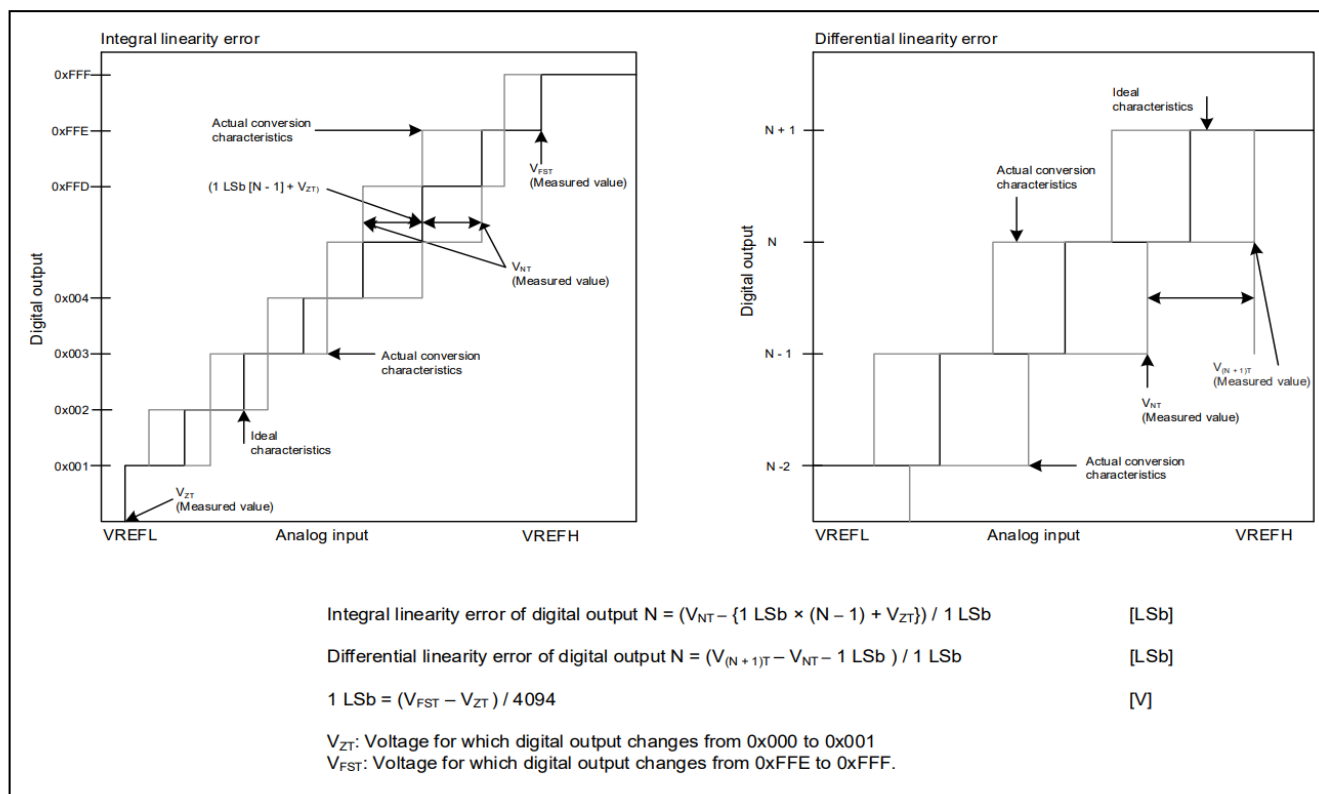


图26-5 积分和微分线性误差

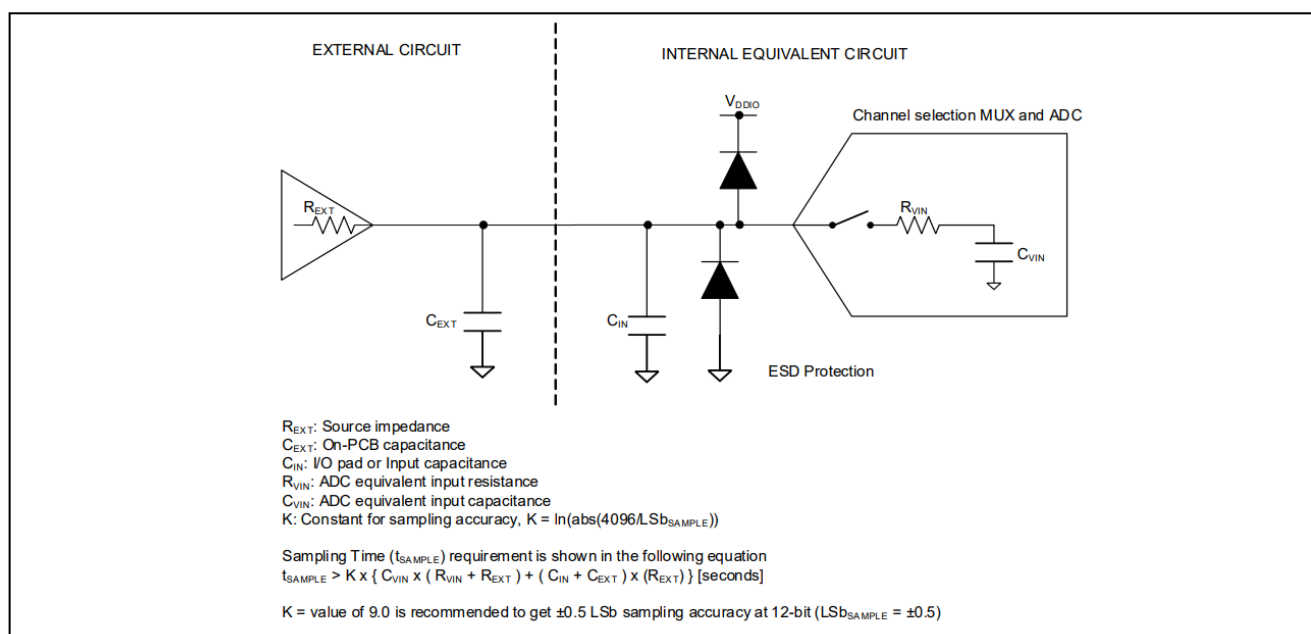


图 26-6 ADC 模拟输入等效电路

电气规格

表 26-7 SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V_{ZT}	Zero transition voltage	-20	-	20	mV	$V_{DDA} = 2.7\text{ V to } 5.5\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ before offset adjustment
SID105	V_{FST}	Full-scale transition voltage	-20	-	20	mV	$V_{DDA} = 2.7\text{ V to } 5.5\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ before offset adjustment
SID114	f_{ADC_4P5}	ADC operating frequency	2	-	26.67	MHz	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$
SID114A	f_{ADC_2P7}	ADC operating frequency	2	-	13.34	MHz	$2.7\text{ V} \leq V_{DDA} \leq 4.5\text{ V}$
SID113	t_{S_4P5}	Analog input sample time for channels of own SARMUX ($4.5\text{ V} \leq V_{DDA}$)	412	-	-	ns	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$, guaranteed by design
SID113A	t_{S_2P7}	Analog input sample time for channels of own SARMUX ($2.7\text{ V} \leq V_{DDA}$)	600	-	-	ns	$2.7\text{ V} \leq V_{DDA} \leq 4.5\text{ V}$, guaranteed by design
SID113B	$t_{S_DR_4P5}$	Analog input sample time when input is from diagnostic reference ($4.5\text{ V} \leq V_{DDA}$)	2	-	-	μs	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$, guaranteed by design
SID113C	$t_{S_DR_2P7}$	Analog input sample time when input is from diagnostic reference ($2.7\text{ V} \leq V_{DDA}$)	2.5	-	-	μs	$2.7\text{ V} \leq V_{DDA} \leq 4.5\text{ V}$, guaranteed by design
SID113D	t_{S_TS}	Analog input sample time for temperature sensor	7	-	-	μs	$2.7\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$ Guaranteed by design
SID113E	$t_{S_4P5_A}$	Analog input sample time for channels of another SARMUXn ($n=1,2$)	824	-	-	ns	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$ When ADC0 borrows the SARMUX of another ADC, guaranteed by design
SID113F	$t_{S_2P7_A}$	Analog input sample time for channels of another SARMUXn ($n=1,2$)	1648	-	-	ns	$2.7\text{ V} \leq V_{DDA} < 4.5\text{ V}$ When ADC0 borrows the SARMUX of another ADC, guaranteed by design
SID106	t_{ST_4P5}	ADC max throughput (samples per second) when using the SARMUX of own ADC	-	-	1	Msp/s	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$, $80\text{ MHz} / 3 = 26.67\text{ MHz}$, 11 sampling cycles, 15 conversion cycles
SID106A	t_{ST_2P7}	ADC max throughput (samples per second) when using the SARMUX of own ADC	-	-	0.5	Msp/s	$2.7\text{ V} \leq V_{DDA} < 4.5\text{ V}$ $80\text{ MHz} / 6 = 13.3\text{ MHz}$, 11 sampling cycles, 15 conversion cycles
SID106B	$t_{ST_4P5_A}$	ADC0 max throughput (samples per second) when borrowing the SARMUXn of another ADC ($n=1,2$)	-	-	0.5	Msp/s	$4.5\text{ V} \leq V_{DDA} \leq 5.5\text{ V}$, $80\text{ MHz} / 6 = 13.3\text{ MHz}$, 11 sampling cycles, 15 conversion cycles
SID106C	$t_{ST_2P7_A}$	ADC0 max throughput (samples per second) when borrowing the SARMUXn of another ADC ($n=1,2$)	-	-	0.25	Msp/s	$2.7\text{ V} \leq V_{DDA} < 4.5\text{ V}$, $80\text{ MHz} / 12 = 6.67\text{ MHz}$, 11 sampling cycles, 15 conversion cycles
SID107	C_{VIN}	ADC input sampling capacitance	-	-	4.8	pF	Guaranteed by design
SID108	R_{VIN1}	Input path ON resistance ($4.5\text{ V to } 5.5\text{ V}$)	-	-	9.4	k Ω	Guaranteed by design

电气规格

表 26-7 SAR ADC AC规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID108A	R _{VIN2}	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	R _{DREF1}	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	R _{DREF2}	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	
SID109	A_TE	Total error	–5	–	5	LSb	V _{DDA} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA} –40 °C ≤ T _A ≤ 125 °C Total Error after offset and gain adjustment at 12-bit resolution mode
SID109A	A_TEB	Total error	–12	–	12	LSb	V _{DDA} = V _{REFH} = 2.7 V to 5.5 V, V _{REFL} = V _{SSA} –40 °C ≤ T _A ≤ 125 °C Total error before offset and gain adjustment at 12 bit resolution mode
SID110	A_INL	Integral nonlinearity	–2.5	–	2.5	LSb	V _{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T _A ≤ 125 °C
SID111	A_DNL	Differential nonlinearity	–0.99	–	1.9	LSb	V _{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T _A ≤ 125 °C
SID112	A_CE	Channel to channel variation (for channels connected to same ADC)	–1	–	1	LSb	V _{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T _A ≤ 125 °C
SID115	I _{AIC}	Analog input leakage current	–350	70	350	nA	When input pad is selected for conversion
SID116	I _{DIAGREF}	Diagnostic reference current	–	–	70	μA	
SID117	I _{VDDA}	Analog power supply current while ADC is operating	–	360	550	μA	Per enabled ADC
SID117A	I _{VDDA_DS}	Analog power supply current while ADC is not operating	–	1	21	μA	Per enabled ADC
SID118	I _{VREF}	Analog reference voltage current while ADC is operating	–	360	550	μA	Per enabled ADC
SID118A	I _{VREF_LEAK}	Analog reference voltage current while ADC is not operating	–	1.8	5	μA	Per enabled ADC

表 26-8 度感应器的规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201	T _{SENSACC2}	Temperature sensor accuracy 2	-5	-	5	°C	-40 °C ≤ T _J ≤ 150 °C This spec is valid when using ADC[0] (V _{DDIO_1}), ADC[1] (V _{DDIO_2}) or ADC[2] (V _{DDD}) with the following conditions: a. 3.0 V ≤ V _{DDD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 3.6 V or b. 4.5 V ≤ V _{DDD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 5.5 V
SID201A	T _{SENSACC3}	Temperature sensor accuracy 3	-10	-	10	°C	-40 °C ≤ T _J ≤ 150 °C This spec is valid when using ADC[0] (V _{DDIO_1}) or ADC[2] (V _{DDD}) with the following condition: 2.7 V ≤ V _{DDD} or V _{DDIO_1} ≤ 5.5 V and 2.7 V ≤ V _{DDA} = V _{REFH} ≤ 5.5 V and 0.8 × V _{DDA} < V _{DDD} or V _{DDIO_1}

26.6.3 分压器准确度

表 26-9 分压器准确度

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID202	V _{MONDIV}	Uncorrected monitor voltage divider accuracy (measured by ADC), compared to ideal supply/2	-20	2	20	%	Any HV supply pad within 2.7 V–5.5 V operating range

26.7 交流规范

除非另有说明，时间定义按照 图 26-7 中提到的指导原则

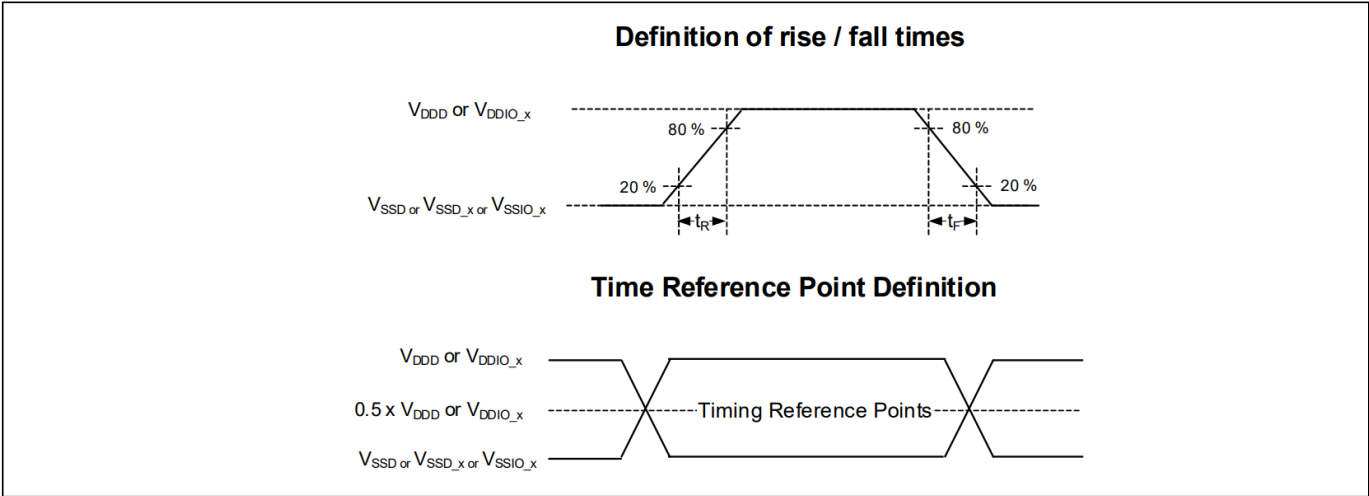


图 26-7 AC时序规格

26.8 数字外设

除非另有说明，所有规格均适用于 $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 26-10 定时器/计数器/PWM (TCPWM) 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID120	f_C	TCPWM operating frequency	–	–	100	MHz	f_C = peripheral clock
SID121	t_{PWMENEXT}	Input trigger pulse width for all trigger events	$2 / f_C$	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMEXT}	Output trigger pulse widths	$2 / f_C$	–	–	ns	Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs
SID123	t_{CRES}	Resolution of counter	$1 / f_C$	–	–	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	$1 / f_C$	–	–	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	$2 / f_C$	–	–	ns	Minimum pulse width between Quadrature phase inputs.

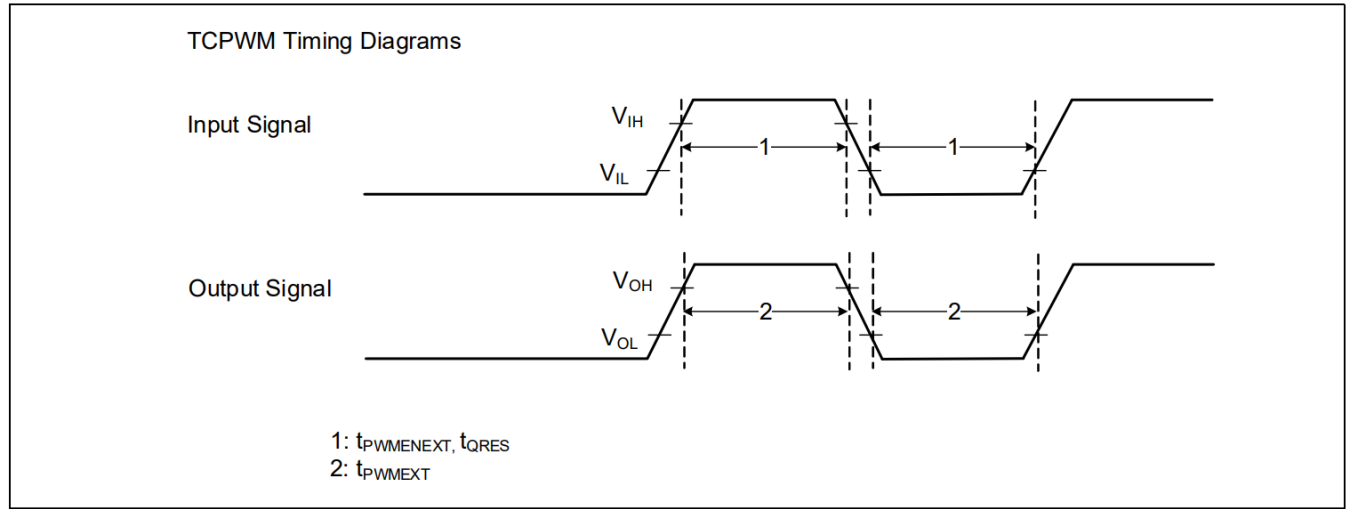


图 26-8 TCPWM 时序图

电气规格

表 26-11 串行通讯功能块 (SCB) 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID129	f_{SCB}	SCB operating frequency	–	–	100	MHz	
I²C 接口-标准模式							
SID130	f_{SCL}	SCL clock frequency	–	–	100	kHz	
SID131	$t_{\text{HD;STA}}$	Hold time, START condition	4000	–	–	ns	
SID132	t_{LOW}	Low period of SCL	4700	–	–	ns	
SID133	t_{HIGH}	High period of SCL	4000	–	–	ns	
SID134	$t_{\text{SU;STA}}$	Setup time for a repeated START	4700	–	–	ns	
SID135	$t_{\text{HD;DAT}}$	Data hold time, for receiver	0	–	–	ns	
SID136	$t_{\text{SU;DAT}}$	Data setup time	250	–	–	ns	
SID138	t_{F}	Fall time of SCL and SDA	–	–	300	ns	Input and output
SID139	$t_{\text{SU;STO}}$	Setup time for STOP	4000	–	–	ns	
SID140	t_{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C_{B}	Capacitive load for each bus line	–	–	400	pF	
SID142	$t_{\text{VD;DAT}}$	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	$t_{\text{VD;ACK}}$	Data valid acknowledge time	–	–	3450	ns	
SID144	V_{OL}	LOW level output voltage	0	–	0.4	V	Open drain at 3-mA sink current
SID145	I_{OL}	LOW level output current	3	–	–	mA	$V_{\text{OL}} = 0.4 \text{ V}$
I²C 接口快速模式							
SID150	$f_{\text{SCL_F}}$	SCL clock frequency	–	–	400	kHz	
SID151	$t_{\text{HD;STA_F}}$	Hold time, START condition	600	–	–	ns	
SID152	$t_{\text{LOW_F}}$	Low period of SCL	1300	–	–	ns	
SID153	$t_{\text{HIGH_F}}$	High period of SCL	600	–	–	ns	
SID154	$t_{\text{SU;STA_F}}$	Setup time for a repeated START	600	–	–	ns	
SID155	$t_{\text{HD;DAT_F}}$	Data hold time, for receiver	0	–	–	ns	
SID156	$t_{\text{SU;DAT_F}}$	Data setup time	100	–	–	ns	
SID158	$t_{\text{F_F}}$	Fall time of SCL and SDA	$20 \times (V_{\text{DD}} / 5.5)$	–	300	ns	Input and output, GPIO_ENH: slow mode, 400 pF load
SID158A	$t_{\text{FA_F}}$	Fall time of SCL and SDA	0.35	–	300	ns	Input and output GPIO_STD: drive_sel<1:0>= 0b00 MIN: 10 pF load, $R_{\text{PU}} = 35.41 \text{ k}\Omega$ Max: 400 pF load, $R_{\text{PU}} = 350 \Omega$
SID159	$t_{\text{SU;STO_F}}$	Setup time for STOP	600	–	–	ns	Input and output
SID160	$t_{\text{BUF_F}}$	Bus free time between START and STOP	1300	–	–	ns	
SID161	$C_{\text{B_F}}$	Capacitive load for each bus line	–	–	400	pF	

电气规格

表 26-11 串行通讯功能块 (SCB) 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID162	$t_{VD;DAT_F}$	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	$t_{VD;ACK_F}$	Data valid acknowledge time	–	–	900	ns	
SID164	t_{SP_F}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
SID165	V_{OL_F}	LOW level output voltage	0	–	0.4	V	Open-drain at 3 mA sink current
SID165	I_{OL_F}	LOW level output current	3	–	–	mA	$V_{OL} = 0.4\text{ V}$
SID167	I_{OL2_F}	LOW level output current	6	–	–	mA	$V_{OL} = 0.6\text{ V}^{[64]}$

I²C 接口-超快速模式

SID170	f_{SCL_FP}	SCL clock frequency	–	–	1	MHz	
SID171	$t_{HD;STA_FP}$	Hold time, START condition	260	–	–	ns	
SID172	t_{LOW_FP}	Low period of SCL	500	–	–	ns	
SID173	t_{HIGH_FP}	High period of SCL	260	–	–	ns	
SID174	$t_{SU;STA_FP}$	Setup time for a repeated START	260	–	–	ns	
SID175	$t_{HD;DAT_FP}$	Data hold time, for receiver	0	–	–	ns	
SID176	$t_{SU;DAT_FP}$	Data setup time	50	–	–	ns	
SID178	t_{F_FP}	Fall time of SCL and SDA	$20 \times (V_{DD}/5.5)$	–	160	ns	Input and output 20-pF load GPIO_ENH: slow mode
SID179	$t_{SU;STO_FP}$	Setup time for STOP	260	–	–	ns	Input and output
SID180	t_{BUF_FP}	Bus free time between START and STOP	500	–	–	ns	
SID181	C_{B_FP}	Capacitive load for each bus line	–	–	20	pF	
SID182	$t_{VD;DAT_FP}$	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	$t_{VD;ACK_FP}$	Data valid acknowledge time	–	–	450	ns	
SID184	t_{SP_FP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
SID186	V_{OL_FP}	LOW level output voltage	0	–	0.4	V	Open-drain at 3 mA sink current
SID187	I_{OL_FP}	LOW level output current	$3^{[65]}$	–	–	mA	$V_{OL} = 0.4\text{ V}^{[65]}$

SPI 接口主机 (全时钟模式: LATE_MISO_SAMPLE = 1) [条件: drive_sel<1:0>= 0x]

SID190	f_{SPI}	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0
SID191	t_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns	

注:

64. 为了以 400 kHz 的频率驱动满总线负载, 在 $0.6\text{ V }V_{OL}$ 时需要 $6\text{ mA }I_{OL}$ 。65. 为了以 1 MHz 的频率驱动满总线负载, 在 $0.4\text{ V }V_{OL}$ 时需要 $20\text{ mA }I_{OL}$ 。但是, 该器件不支持它。

电气规格

表 26-11 串行通讯功能块 (SCB) 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID192	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	40	–	–	ns	
SID193	t_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	
SID194	$t_{W_SCLK_H_L}$	SPI SCLK pulse width HIGH or LOW	$0.4 \times (1/f_{SPI})$	$0.5 \times (1/f_{SPI})$	$0.6 \times (1/f_{SPI})$	ns	
SID196	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	
SID198	t_{EN_SETUP}	SSEL valid, before the first SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID199	t_{EN_SHOLD}	SSEL hold, after the last SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID195	C_{SPIM_MS}	SPI capacitive load	–	–	10	pF	

SPI 接口从机 (内部时钟) [条件: $drive_sel<1:0>=0x$]

SID205	f_{SPI_INT}	SPI operating frequency	–	–	10	MHz	
SID206	t_{DMI_INT}	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	
SID207	t_{DSO_INT}	SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	62	ns	
SID208	t_{HSP}	SPI Slave: Previous MISO data hold time	3	–	–	ns	
SID209	$t_{EN_SETUP_INT}$	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	
SID210	$t_{EN_HOLD_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	
SID211	$t_{EN_SETUP_PRE}$	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	
SID212	$t_{EN_HOLD_PRE}$	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	
SID213	$t_{EN_SETUP_CO}$	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	
SID214	$t_{EN_HOLD_CO}$	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	
SID215	$t_{W_DIS_INT}$	SPI Slave Select inactive time	40	–	–	ns	
SID216	$t_{W_SCLKH_INT}$	SPI SCLK pulse width HIGH	20	–	–	ns	
SID217	$t_{W_SCLKL_INT}$	SPI SCLK pulse width LOW	20	–	–	ns	
SID218	t_{SIH_INT}	SPI MOSI hold from SCLK	12	–	–	ns	
SID219	C_{SPIS_INT}	SPI Capacitive Load	–	–	10	pF	

SPI 接口从机 (外部时钟) [条件: $drive_sel<1:0>=0x$]

SID220	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	
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电气规格

表 26-11 串行通讯功能块 (SCB) 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID221	t _{DMI_EXT}	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	
SID222	t _{DSO_EXT}	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	32	ns	
SID223	t _{HSO_EXT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	
SID224	t _{EN_SET-UP_EXT}	SPI Slave: SSEL valid to first SCK valid edge	40	–	–	ns	
SID225	t _{EN_HOLD_EXT}	SPI Slave Select active (LOW) from last SCLK hold	40	–	–	ns	
SID226	t _{W_DIS_EXT}	SPI Slave Select inactive time	80	–	–	ns	
SID227	t _{W_SCLKH_EXT}	SPI SCLK pulse width HIGH	34	–	–	ns	
SID228	t _{W_SCLKL_EXT}	SPI SCLK pulse width LOW	34	–	–	ns	
SID229	t _{SIH_EXT}	SPI MOSI hold from SCLK	20	–	–	ns	
SID230	C _{SPIS_EXT}	SPI Capacitive Load	–	–	10	pF	
SID231	t _{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	

UART接口

SID240	f _{BPS}	Data rate	–	–	10	Mbps	
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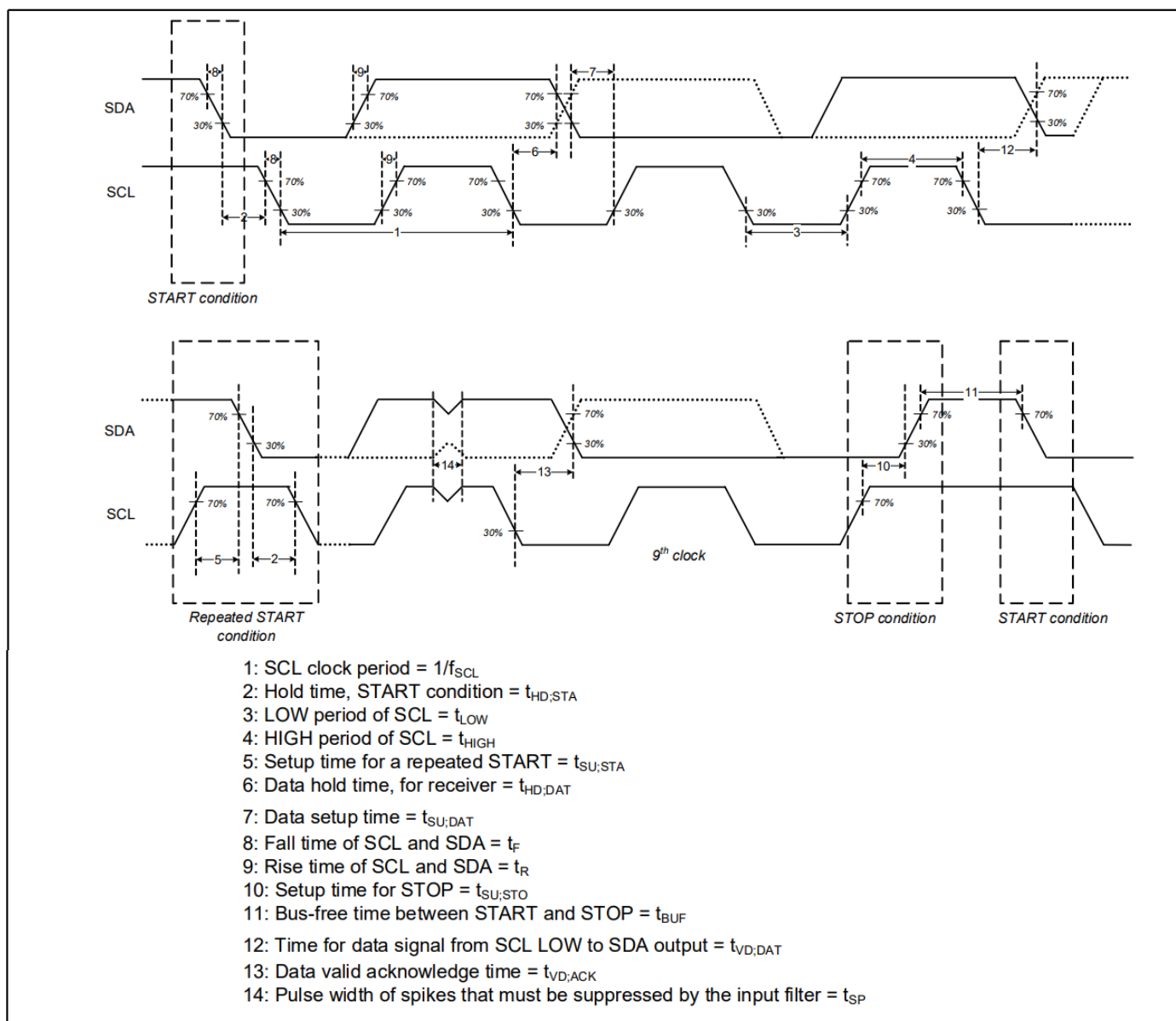


Figure 26-9 I²C 时序图

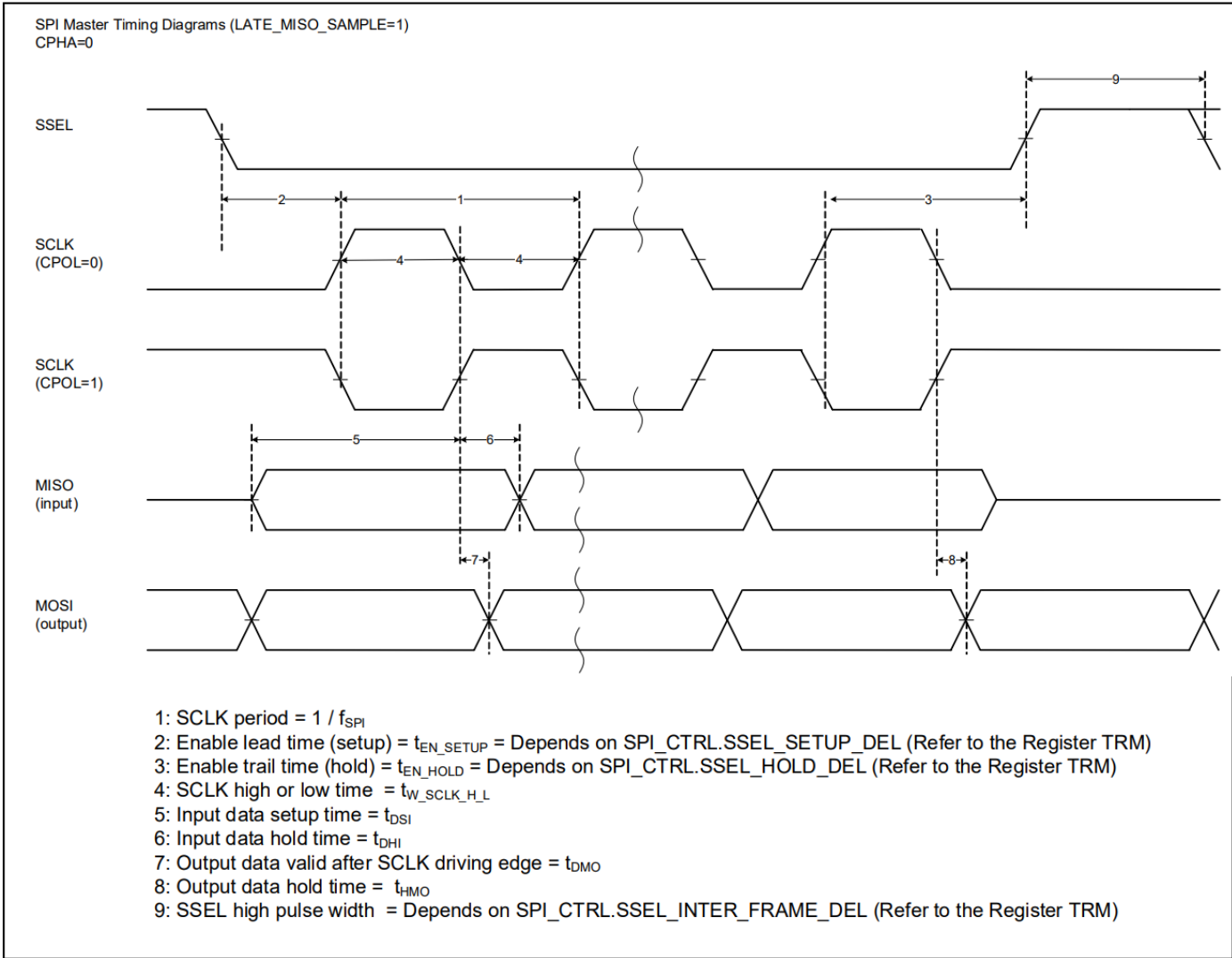


图 26-10 SPI 主机时序图（低时钟相位）

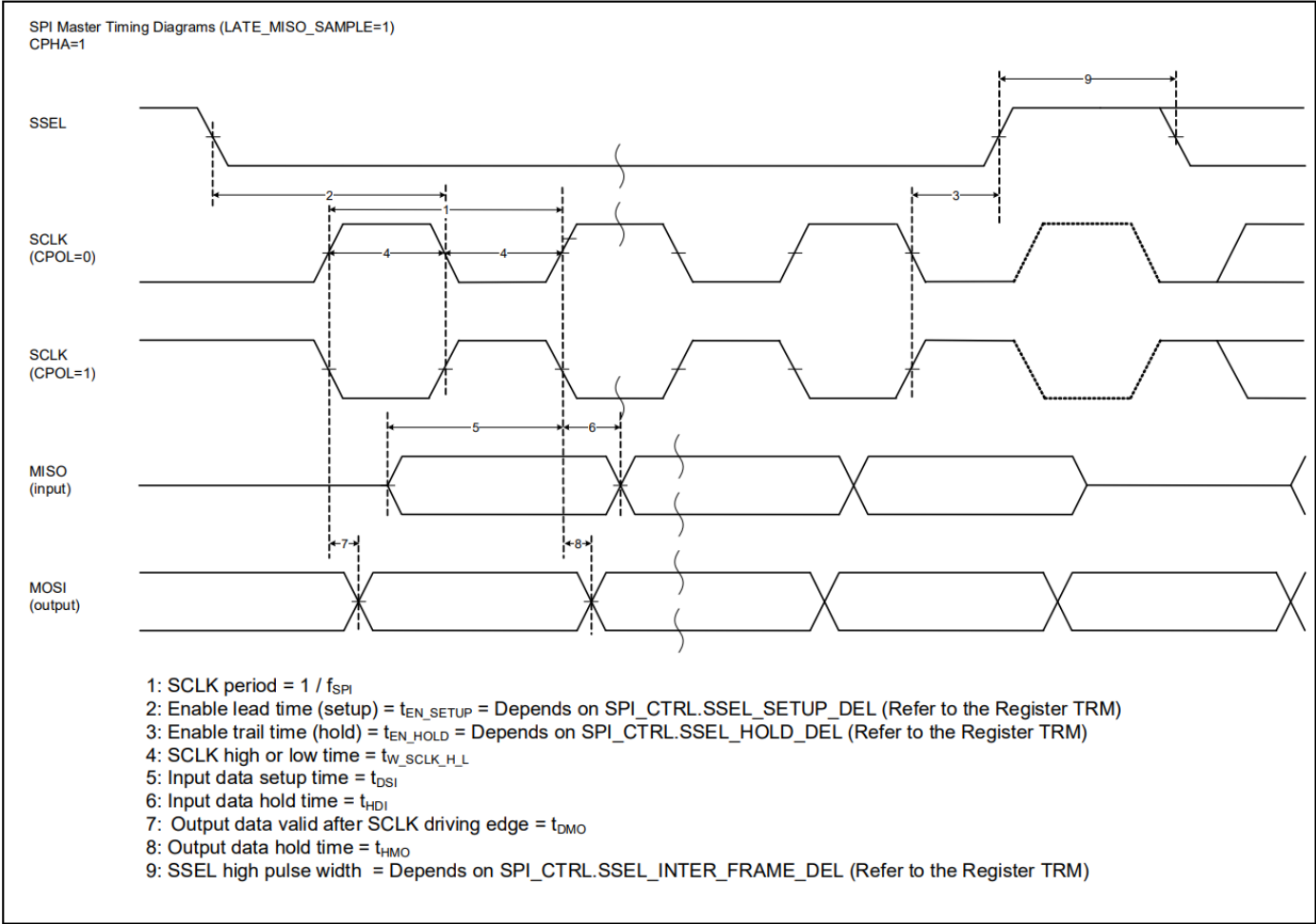


图 26-11 SPI 主机时序图（高时钟相位）

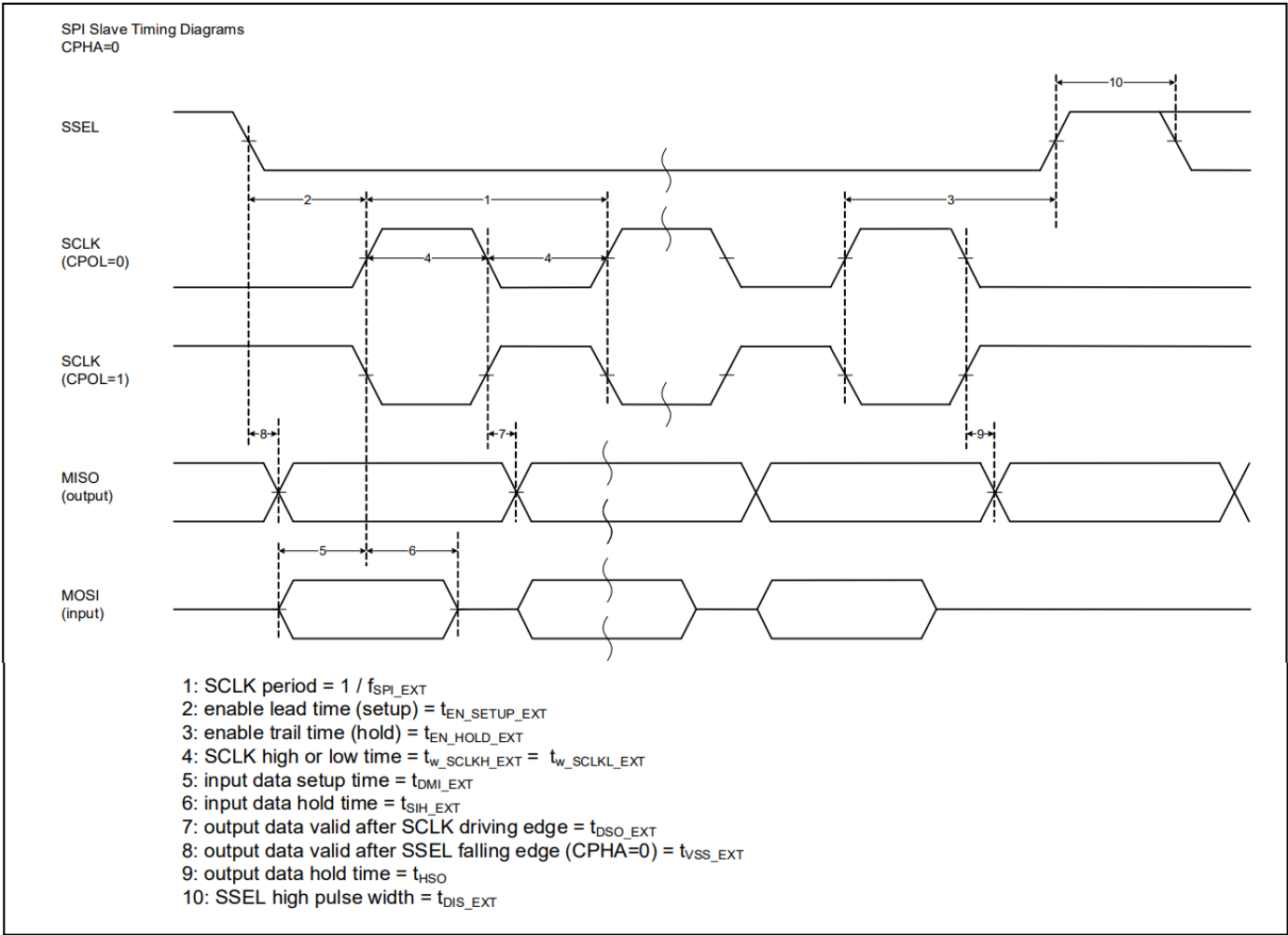


图 26-12 SPI 从机时序图（低时钟相位）

电气规格

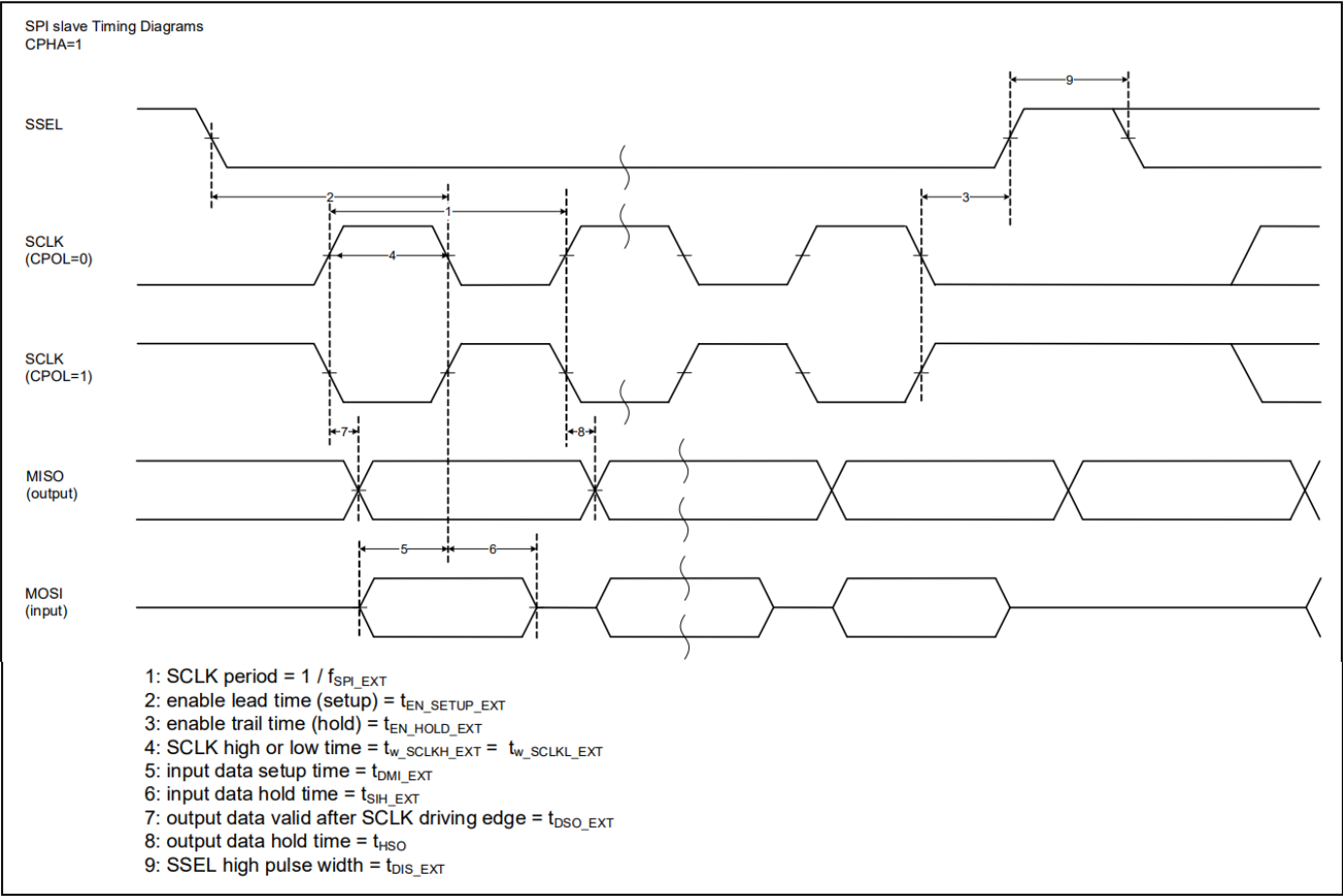


图 26-13 SPI 从机时序图（高时钟相位） 表 26-12 CAN

FD 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID630	f_{HCLK}	System clock frequency	–	–	100	MHz	$f_{\text{CCLK}} \leq f_{\text{HCLK}}$, guaranteed by design
SID631	f_{CCLK}	CAN clock frequency	–	–	100	MHz	$f_{\text{CCLK}} \leq f_{\text{HCLK}}$, guaranteed by design

表 26-13 LIN 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID249	f_{LIN}	Internal clock frequency to the LIN block	–	–	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	Guaranteed by design

电气规格

26.9 存储器

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 26-14 闪存 DC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID260	V_{PE}	Erase and program voltage	2.7	–	5.5	V	

表26-15 闪存 AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257	f_{FO}	Maximum flash memory operation frequency	–	–	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 250 MHz
SID254	t_{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	–	–	37.5	μs	
SID255	$t_{ERS_RES_SUS}$	Minimum time allowed from erase resume to erase suspend	250	–	–	μs	Guaranteed by design
SID258	t_{BC_WF}	Blank check time for N-bytes of work-flash	–	–	$10 + 0.3 \times N$	μs	At 100 MHz, $N \geq 4$ and multiple of 4, excludes system overhead time
SID259	$t_{SECTORERASE1}$	Sector erase time (code-flash: 32 KB)	–	45	90	ms	Includes internal preprogramming time
SID259A	$t_{SECTORERASE2}$	Sector erase time (code-flash: 8 KB)	–	15	30	ms	Includes internal preprogramming time
SID261	$t_{SECTORERASE3}$	Sector erase time (work-flash, 2 KB)	–	80	160	ms	Includes internal preprogramming time
SID262	$t_{SECTORERASE4}$	Sector erase time (work-flash, 128 B)	–	5	15	ms	Includes internal preprogramming time
SID263	t_{WRITE1}	64-bit write time (code-flash)	–	30	60	μs	Excludes system overhead time
SID264	t_{WRITE2}	256-bit write time (code-flash)	–	40	70	μs	Excludes system overhead time
SID265	t_{WRITE3}	4096-bit write time (code-flash) ^[66]	–	320	1200	μs	Excludes system overhead time
SID266	t_{WRITE4}	32-bit write time (work-flash)	–	30	60	μs	Excludes system overhead time
SID267	t_{FRET1}	Code-flash retention. 1000 program/erase cycles	20	–	–	years	T_A (power on and off) $\leq 85^{\circ}\text{C}$ average
SID268	t_{FRET3}	Work-flash retention. 125,000 program/erase cycles	20	–	–	years	T_A (power on and off) $\leq 85^{\circ}\text{C}$ average
SID269	t_{FRET4}	Work-flash retention. 250,000 program/erase cycles	10	–	–	years	T_A (power on and off) $\leq 85^{\circ}\text{C}$ average

注:

66. 代码闪存包括 4096 位的写入缓冲。如果应用软件多次写入该缓冲器，要获得总写入时间，请将一个扇区写入时间乘以相应的因子（假设因子为 64，例如 $64 \times 512 \text{ B} = 32 \text{ KB}$ [一个扇区]）。

电气规格
表 26-15 闪存 AC 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID612	I_{CC_ACT2}	Program operating V_{CCD} current (code or work-flash)	–	7	58	mA	Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, $V_{CCD} = 1.2\text{ V}$, process worst (FF) Guaranteed by design
SID613	I_{CC_ACT3}	Erase operating V_{CCD} current (code- or work-flash)	–	7	52	mA	Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, $V_{CCD} = 1.2\text{ V}$, process worst (FF) Guaranteed by design
SID612A	I_{CC_ACT2A}	Program operating V_{DDD} current (code or work-flash)	–	8	10	mA	Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, $V_{CCD} = 1.2\text{ V}$, process worst (FF) Guaranteed by design
SID613A	I_{CC_ACT3A}	Erase operating V_{DDD} current (code- or work-flash)	–	8	16	mA	Typ: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.0\text{ V}$, $V_{CCD} = 1.15\text{ V}$, process typ (TT) Max: $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DDD} = 5.5\text{ V}$, $V_{CCD} = 1.2\text{ V}$, process worst (FF) Guaranteed by design

26.10 系统资源

除非另有说明，所有规格均适用于 $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表26-16 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
上电复位规格							
SID270	V _{POR_D}	V _{DD} rising voltage to de assert POR	1.5	–	2.35	V	Guaranteed by design
SID276	V _{POR_A}	V _{DD} falling voltage to assert POR	1.45	–	2.1	V	
SID271	V _{POR_H}	Level detection hysteresis	20	–	300	mV	
SID272	t _{DLY_POR}	Delay between V _{DD} rising through 2.3 V and internal deassertion of POR	–	–	3	μs	Guaranteed by design
SID273	t _{POFF}	V _{DD} Power off time	100	–	–	μs	V _{DD} < 1.45 V
SID274	POR_RR1	V _{DD} power ramp rate with robust BOD (BOD operation is guaranteed)	–	–	100	mV/μs	This ramp supports robust BOD
SID275	POR_RR2	V _{DD} power ramp rate without robust BOD	–	–	1000	mV/μs	This ramp does not support robust BOD t _{POFF} must be satisfied.
高压 BOD (HV BOD) 规格							
SID500	V _{TR_2P7_R}	HV BOD 2.7 V rising detection point for V _{DD} and V _{DDA} (default)	2.474	2.55	2.627	V	
SID501	V _{TR_2P7_F}	HV BOD 2.7 V falling detection point for V _{DD} and V _{DDA} (default)	2.449	2.525	2.601	V	
SID502	V _{TR_3P0_R}	HV BOD 3.0 V rising detection point for V _{DD} and V _{DDA}	2.765	2.85	2.936	V	
SID503	V _{TR_3P0_F}	HV BOD 3.0 V falling detection point for V _{DD} and V _{DDA}	2.74	2.825	2.91	V	
SID505	HVBOD_RR_A	Power ramp rate: V _{DD} and V _{DDA} (Active)	–	–	100	mV/μs	
SID506	HVBOD_RR_DS	Power ramp rate: V _{DD} and V _{DDA} (DeepSleep)	–	–	10	mV/μs	
SID507	t _{DLY_ACT_HVBOD}	Active mode delay between V _{DD} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning	–	–	0.5	μs	Guaranteed by design
SID507A	t _{DLY_ACT_HVBOD}	Active mode delay between V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and internal HV BOD signal transitioning	–	–	1	μs	Guaranteed by design
SID507B	t _{DLY_DS_HVBOD}	DeepSleep mode delay between V _{DD} /V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning	–	–	4	μs	Guaranteed by design
SID508	t _{RES_HVBOD}	Response time of HV BOD, V _{DD} /V _{DDA} supply. (For falling-then-rising supply at max ramp rate; threshold is V _{TR_2P7_F} or V _{TR_3P0_F})	100	–	–	ns	Guaranteed by design
低压 BOD (LV BOD) 规格							
SID510	V _{TR_R_LVBOD}	LV BOD rising detection point for V _{CCD}	0.917	0.945	0.973	V	
SID511	V _{TR_F_LVBOD}	LV BOD falling detection point for V _{CCD}	0.892	0.920	0.948	V	
SID515	t _{DLY_ACT_LVBOD}	Active delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD signal transitioning	–	–	1	μs	Guaranteed by design
SID515A	t _{DLY_DS_LVBOD}	DeepSleep mode delay between V _{CCD} falling/rising through V _{TR_R/F_LVBOD} and an internal LV BOD signal transitioning	–	–	12	μs	Guaranteed by design
SID516	t _{RES_LVBOD}	Response time of LV BOD (for falling-then-rising supply at max ramp rate; threshold is V _{TR_F_LVBOD})	100	–	–	ns	Guaranteed by design

电气规格

表 26-16 系统资源 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
低压检测器 (LVD) DC规格							
SID520	V _{TR_2P8_F}	LVD 2.8 V falling detection point for V _{DDD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	V _{TR_2P9_F}	LVD 2.9 V falling detection point for V _{DDD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	V _{TR_3P0_F}	LVD 3.0 V falling detection point for V _{DDD}	Typ – 4%	3000	Typ + 4%	mV	
SID523	V _{TR_3P1_F}	LVD 3.1 V falling detection point for V _{DDD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	V _{TR_3P2_F}	LVD 3.2 V falling detection point for V _{DDD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	V _{TR_3P3_F}	LVD 3.3 V falling detection point for V _{DDD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	V _{TR_3P4_F}	LVD 3.4 V falling detection point for V _{DDD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	V _{TR_3P5_F}	LVD 3.5 V falling detection point for V _{DDD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	V _{TR_3P6_F}	LVD 3.6 V falling detection point for V _{DDD}	Typ – 4%	3600	Typ + 4%	mV	
SID529	V _{TR_3P7_F}	LVD 3.7 V falling detection point for V _{DDD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	V _{TR_3P8_F}	LVD 3.8 V falling detection point for V _{DDD}	Typ – 4%	3800	Typ + 4%	mV	
SID531	V _{TR_3P9_F}	LVD 3.9 V falling detection point for V _{DDD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	V _{TR_4P0_F}	LVD 4.0 V falling detection point for V _{DDD}	Typ – 4%	4000	Typ + 4%	mV	
SID533	V _{TR_4P1_F}	LVD 4.1 V falling detection point for V _{DDD}	Typ – 4%	4100	Typ + 4%	mV	
SID534	V _{TR_4P2_F}	LVD 4.2 V falling detection point for V _{DDD}	Typ – 4%	4200	Typ + 4%	mV	
SID535	V _{TR_4P3_F}	LVD 4.3 V falling detection point for V _{DDD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	V _{TR_4P4_F}	LVD 4.4 V falling detection point for V _{DDD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	V _{TR_4P5_F}	LVD 4.5 V falling detection point for V _{DDD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	V _{TR_4P6_F}	LVD 4.6 V falling detection point for V _{DDD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	V _{TR_4P7_F}	LVD 4.7 V falling detection point for V _{DDD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	V _{TR_4P8_F}	LVD 4.8 V falling detection point for V _{DDD}	Typ – 4%	4800	Typ + 4%	mV	
SID541	V _{TR_4P9_F}	LVD 4.9 V falling detection point for V _{DDD}	Typ – 4%	4900	Typ + 4%	mV	
SID542	V _{TR_5P0_F}	LVD 5.0 V falling detection point for V _{DDD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	V _{TR_5P1_F}	LVD 5.1 V falling detection point for V _{DDD}	Typ – 4%	5100	Typ + 4%	mV	
SID544	V _{TR_5P2_F}	LVD 5.2 V falling detection point for V _{DDD}	Typ – 4%	5200	Typ + 4%	mV	
SID545	V _{TR_5P3_F}	LVD 5.3 V falling detection point for V _{DDD}	Typ – 4%	5300	Typ + 4%	mV	
SID546	V _{TR_2P8_R}	LVD 2.8 V rising detection point for V _{DDD}	Typ – 4%	2825	Typ + 4%	mV	Same as V _{TR_2P8_F} + 25 mV
SID547	V _{TR_2P9_R}	LVD 2.9 V rising detection point for V _{DDD}	Typ – 4%	2925	Typ + 4%	mV	Same as V _{TR_2P9_F} + 25 mV
SID548	V _{TR_3P0_R}	LVD 3.0 V rising detection point for V _{DDD}	Typ – 4%	3025	Typ + 4%	mV	Same as V _{TR_3P0_F} + 25 mV

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表 26-16 系统资源 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID549	V _{TR_3P1_R}	LVD 3.1 V rising detection point for V _{DDD}	Typ – 4%	3125	Typ + 4%	mV	Same as V _{TR_3P1_F} + 25 mV
SID550	V _{TR_3P2_R}	LVD 3.2 V rising detection point for V _{DDD}	Typ – 4%	3225	Typ + 4%	mV	Same as V _{TR_3P2_F} + 25 mV
SID551	V _{TR_3P3_R}	LVD 3.3 V rising detection point for V _{DDD}	Typ – 4%	3325	Typ + 4%	mV	Same as V _{TR_3P3_F} + 25 mV
SID552	V _{TR_3P4_R}	LVD 3.4 V rising detection point for V _{DDD}	Typ – 4%	3425	Typ + 4%	mV	Same as V _{TR_3P4_F} + 25 mV
SID553	V _{TR_3P5_R}	LVD 3.5 V rising detection point for V _{DDD}	Typ – 4%	3525	Typ + 4%	mV	Same as V _{TR_3P5_F} + 25 mV
SID554	V _{TR_3P6_R}	LVD 3.6 V rising detection point for V _{DDD}	Typ – 4%	3625	Typ + 4%	mV	Same as V _{TR_3P6_F} + 25 mV
SID555	V _{TR_3P7_R}	LVD 3.7 V rising detection point for V _{DDD}	Typ – 4%	3725	Typ + 4%	mV	Same as V _{TR_3P7_F} + 25 mV
SID556	V _{TR_3P8_R}	LVD 3.8 V rising detection point for V _{DDD}	Typ – 4%	3825	Typ + 4%	mV	Same as V _{TR_3P8_F} + 25 mV
SID557	V _{TR_3P9_R}	LVD 3.9 V rising detection point for V _{DDD}	Typ – 4%	3925	Typ + 4%	mV	Same as V _{TR_3P9_F} + 25 mV
SID558	V _{TR_4P0_R}	LVD 4.0 V rising detection point for V _{DDD}	Typ – 4%	4025	Typ + 4%	mV	Same as V _{TR_4P0_F} + 25 mV
SID559	V _{TR_4P1_R}	LVD 4.1 V rising detection point for V _{DDD}	Typ – 4%	4125	Typ + 4%	mV	Same as V _{TR_4P1_F} + 25 mV
SID560	V _{TR_4P2_R}	LVD 4.2 V rising detection point for V _{DDD}	Typ – 4%	4225	Typ + 4%	mV	Same as V _{TR_4P2_F} + 25 mV
SID561	V _{TR_4P3_R}	LVD 4.3 V rising detection point for V _{DDD}	Typ – 4%	4325	Typ + 4%	mV	Same as V _{TR_4P3_F} + 25 mV
SID562	V _{TR_4P4_R}	LVD 4.4 V rising detection point for V _{DDD}	Typ – 4%	4425	Typ + 4%	mV	Same as V _{TR_4P4_F} + 25 mV
SID563	V _{TR_4P5_R}	LVD 4.5 V rising detection point for V _{DDD}	Typ – 4%	4525	Typ + 4%	mV	Same as V _{TR_4P5_F} + 25 mV
SID564	V _{TR_4P6_R}	LVD 4.6 V rising detection point for V _{DDD}	Typ – 4%	4625	Typ + 4%	mV	Same as V _{TR_4P6_F} + 25 mV
SID565	V _{TR_4P7_R}	LVD 4.7 V rising detection point for V _{DDD}	Typ – 4%	4725	Typ + 4%	mV	Same as V _{TR_4P7_F} + 25 mV
SID566	V _{TR_4P8_R}	LVD 4.8 V rising detection point for V _{DDD}	Typ – 4%	4825	Typ + 4%	mV	Same as V _{TR_4P8_F} + 25 mV
SID567	V _{TR_4P9_R}	LVD 4.9 V rising detection point for V _{DDD}	Typ – 4%	4925	Typ + 4%	mV	Same as V _{TR_4P9_F} + 25 mV
SID568	V _{TR_5P0_R}	LVD 5.0 V rising detection point for V _{DDD}	Typ – 4%	5025	Typ + 4%	mV	Same as V _{TR_5P0_F} + 25 mV
SID569	V _{TR_5P1_R}	LVD 5.1 V rising detection point for V _{DDD}	Typ – 4%	5125	Typ + 4%	mV	Same as V _{TR_5P1_F} + 25 mV
SID570	V _{TR_5P2_R}	LVD 5.2 V rising detection point for V _{DDD}	Typ – 4%	5225	Typ + 4%	mV	Same as V _{TR_5P2_F} + 25 mV
SID571	V _{TR_5P3_R}	LVD 5.3 V rising detection point for V _{DDD}	Typ – 4%	5325	Typ + 4%	mV	Same as V _{TR_5P3_F} + 25 mV
SID573	LVD_RR_A	Power ramp rate: V _{DDD} (Active)	–	–	100	mV/μs	
SID574	LVD_RR_DS	Power ramp rate: V _{DDD} (DeepSleep)	–	–	10	mV/μs	
SID575	t _{DLY_ACT_LVD}	Active mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning	–	–	1	μs	Guaranteed by design
SID575A	t _{DLY_DS_LVD}	DeepSleep mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning	–	–	4	μs	Guaranteed by design
SID576	t _{RES_LVD}	Response time of LVD, V _{DDD} supply. (For falling-then-rising supply at max ramp rate; threshold is LVD falling point)	100	–	–	ns	Guaranteed by design

电气规格

表 26-16 系统资源 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
高压 OVD 规格							
SID580	$V_{TR_5P0_R}$	HV OVD 5.0-V rising detection point for V_{DD} and V_{DDA}	5.049	5.205	5.361	V	
SID581	$V_{TR_5P0_F}$	HV OVD 5.0-V falling detection point for V_{DD} and V_{DDA}	5.025	5.18	5.335	V	
SID582	$V_{TR_5P5_R}$	HV OVD 5.5-V rising detection point for V_{DD} and V_{DDA} (default)	5.548	5.72	5.892	V	
SID583	$V_{TR_5P5_F}$	HV OVD 5.5-V falling detection point for V_{DD} and V_{DDA} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V_{DD} and V_{DDA} (Active)	–	–	100	mV/μs	
SID586	HVOVD_RR_DS	Power ramp rate: V_{DD} and V_{DDA} (DeepSleep)	–	–	10	mV/μs	
SID587	$t_{DLY_ACT_HVOVD}$	Active mode delay between V_{DD} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning	–	–	1	μs	Guaranteed by design
SID587A	$t_{DLY_ACT_HVOVD_A}$	Active mode delay between V_{DDA} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning	–	–	1.5	μs	Guaranteed by design
SID587B	$t_{DLY_DS_HVOVD}$	DeepSleep mode delay between V_{DD}/V_{DDA} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning	–	–	4	μs	Guaranteed by design
SID588	t_{RES_HVOVD}	Response time of HV OVD (for rising-then-falling supply at max ramp rate; threshold is $V_{TR_5P0_R}$ or $V_{TR_5P5_R}$)	100	–	–	ns	Guaranteed by design
低压 OVD 规格							
SID590	$V_{TR_R_LVOVD}$	LV OVD rising detection point for V_{CCD}	1.261	1.3	1.339	V	
SID591	$V_{TR_F_LVOVD}$	LV OVD falling detection point for V_{CCD}	1.237	1.275	1.313	V	
SID595	$t_{DLY_ACT_LVOVD}$	Active mode delay between V_{CCD} falling/rising through $V_{TR_F_R_LVOVD}$ and an internal LV OVD signal transitioning	–	–	1	μs	Guaranteed by design
SID595A	$t_{DLY_DS_LVOVD}$	DeepSleep mode delay between V_{CCD} falling/rising through $V_{TR_F_R_LVOVD}$ and an internal LV OVD signal transitioning	–	–	12	μs	Guaranteed by design
SID596	t_{RES_LVOVD}	Response time of LV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR_R_LVOVD}$)	100	–	–	ns	Guaranteed by design
过流检测 (OCD) 规格							
SID598A	I_{OCD_LDO}	Over current detection range for internal Active regulator	312	–	630	mA	Guaranteed by design
SID598B	I_{OCD_EXT}	Over current detection range for external transistor mode	675	–	825	mA	
SID599	I_{OCD_DPSLP}	Over current detection range for internal DeepSleep regulator	18	–	72	mA	

电气规格

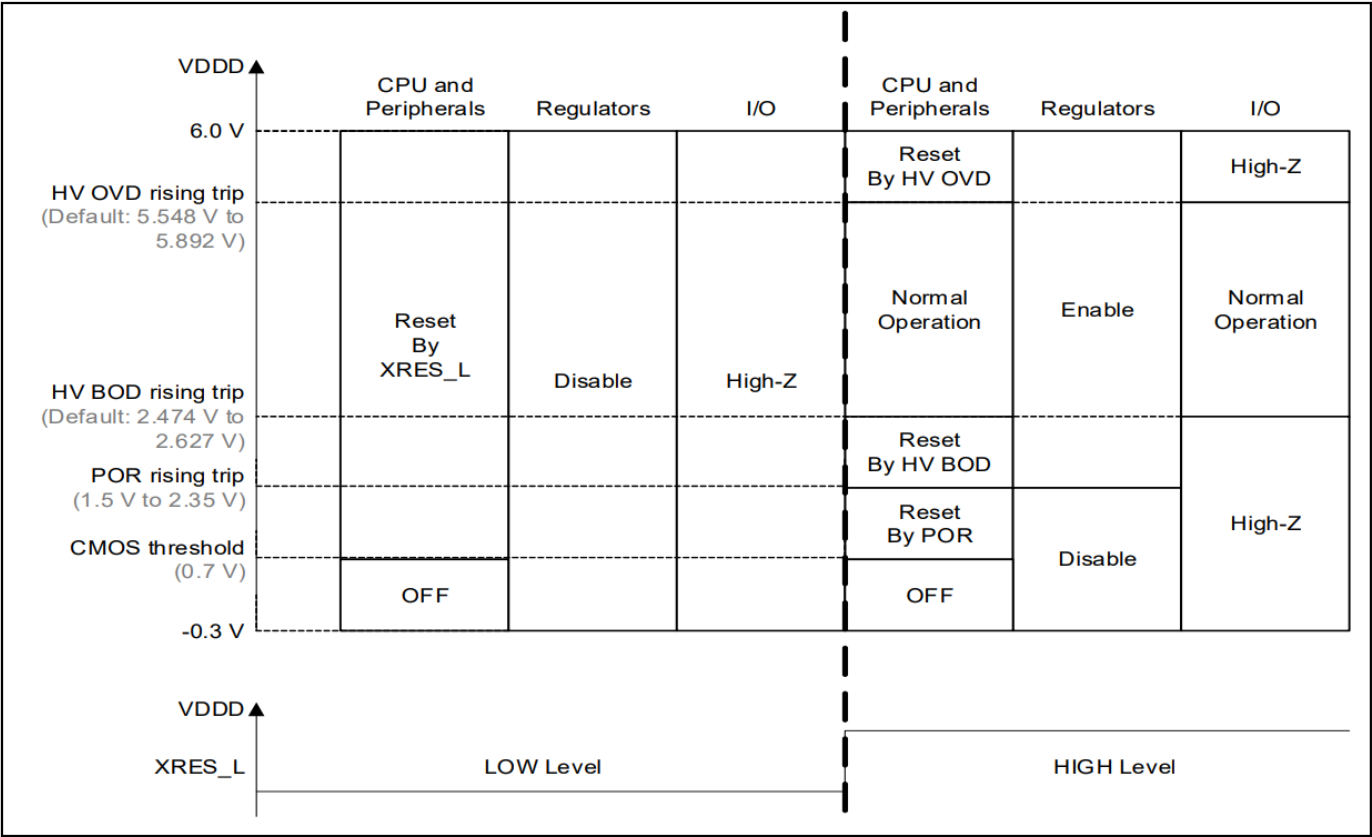


图 26-14 器件操作电源范围

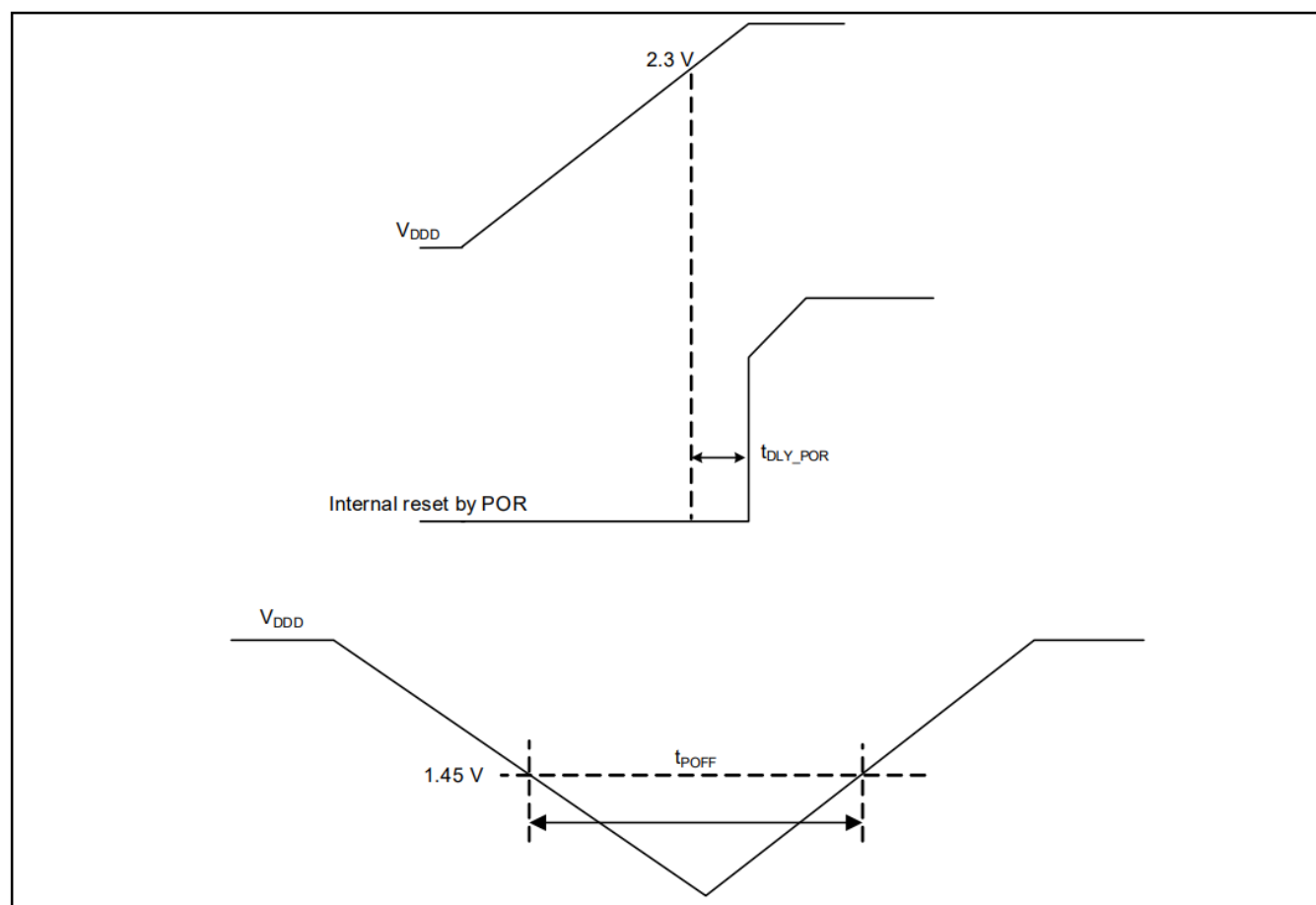


图 26-15 POR 规格

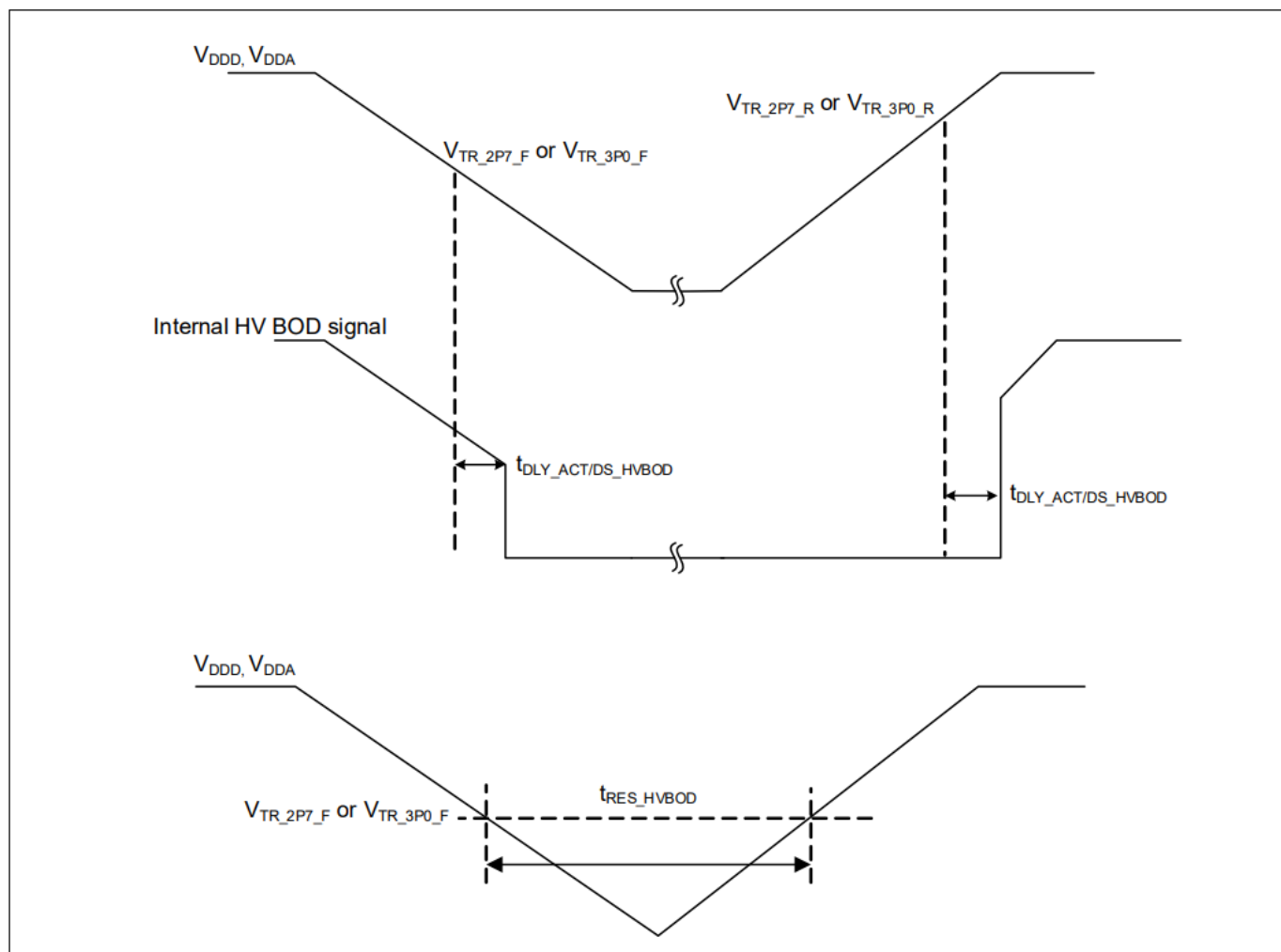


图26-16 高压BOD规格

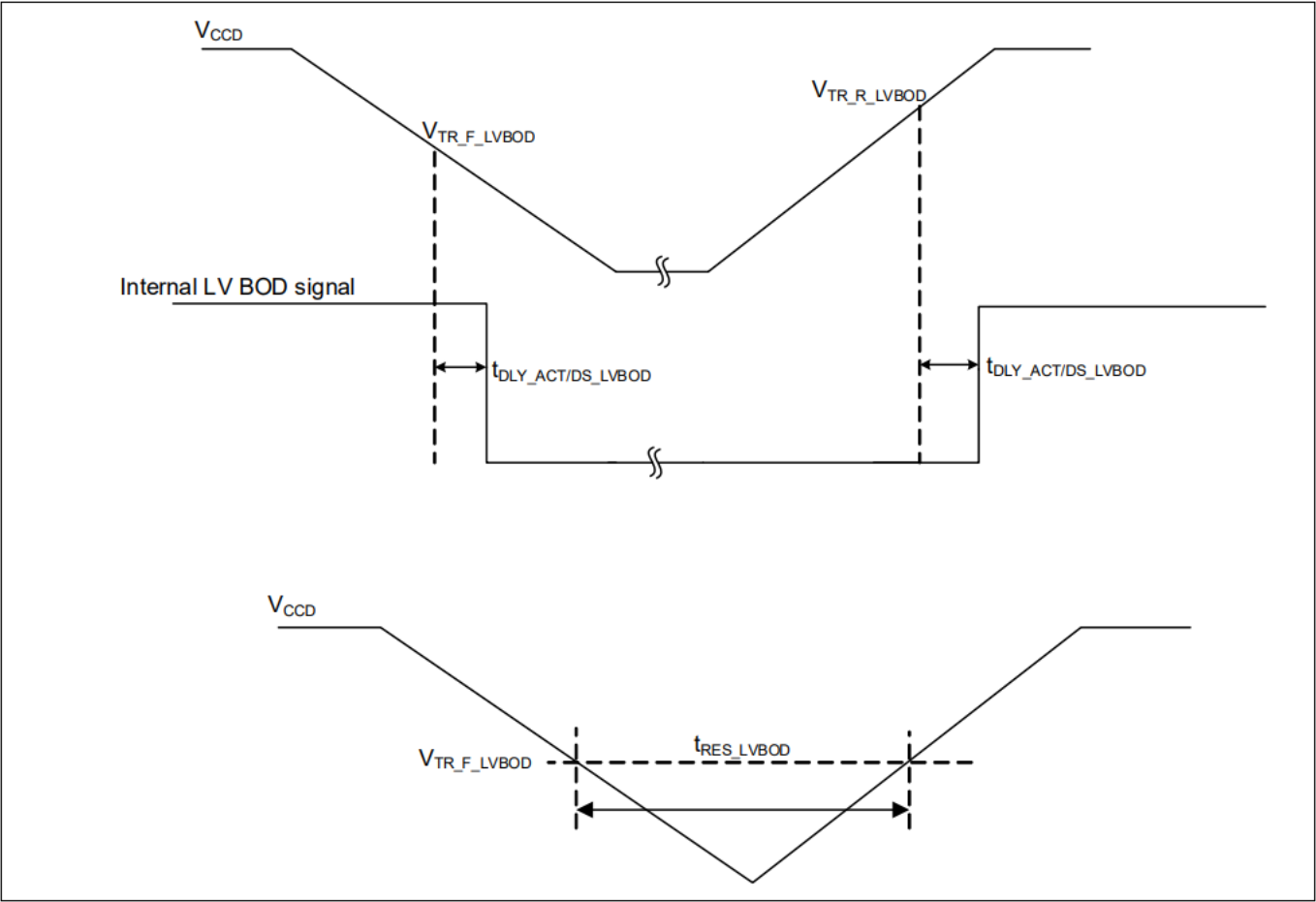


图 26-17 低压 BOD 规格

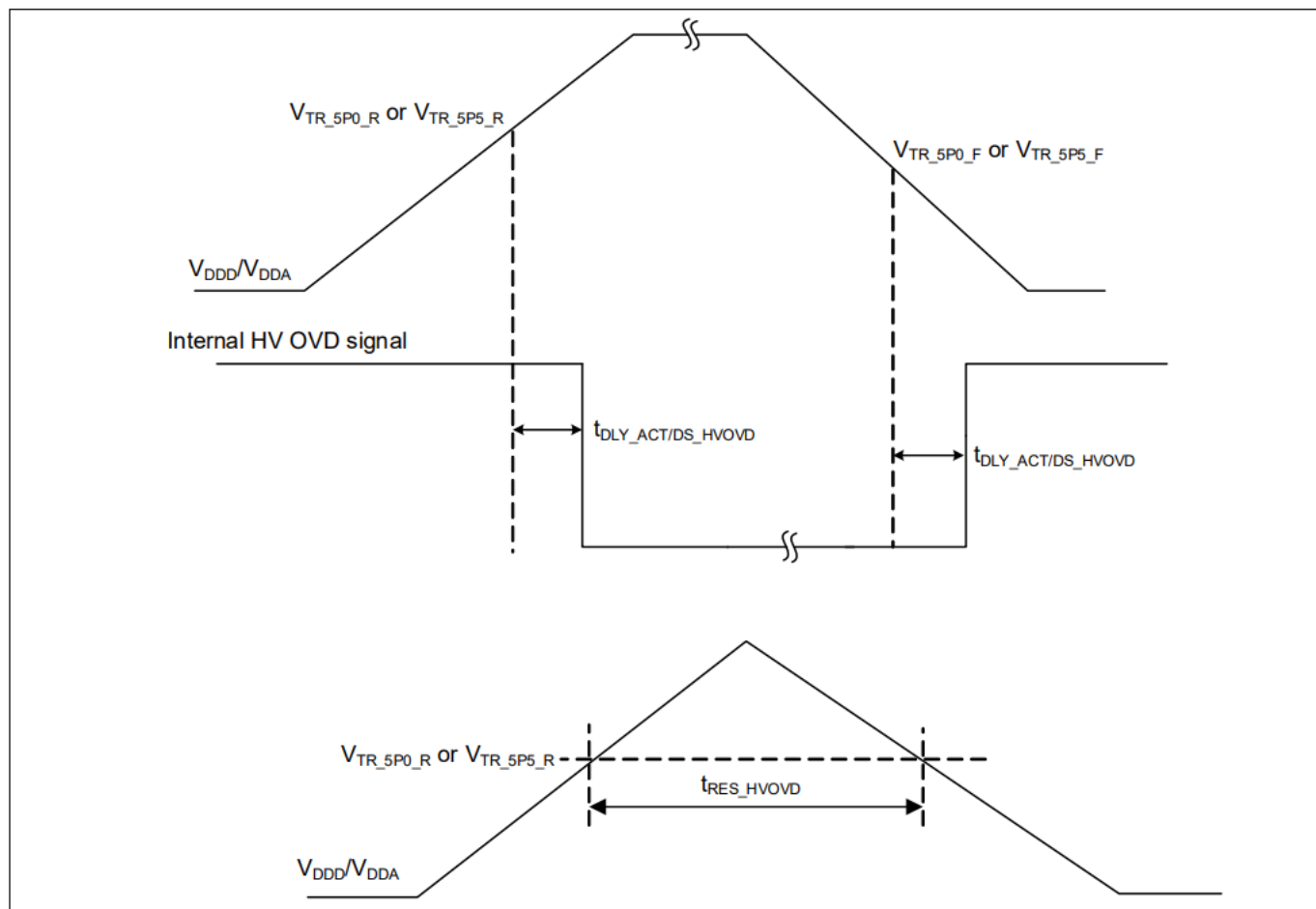


图 26-18 高压 OVD 规格

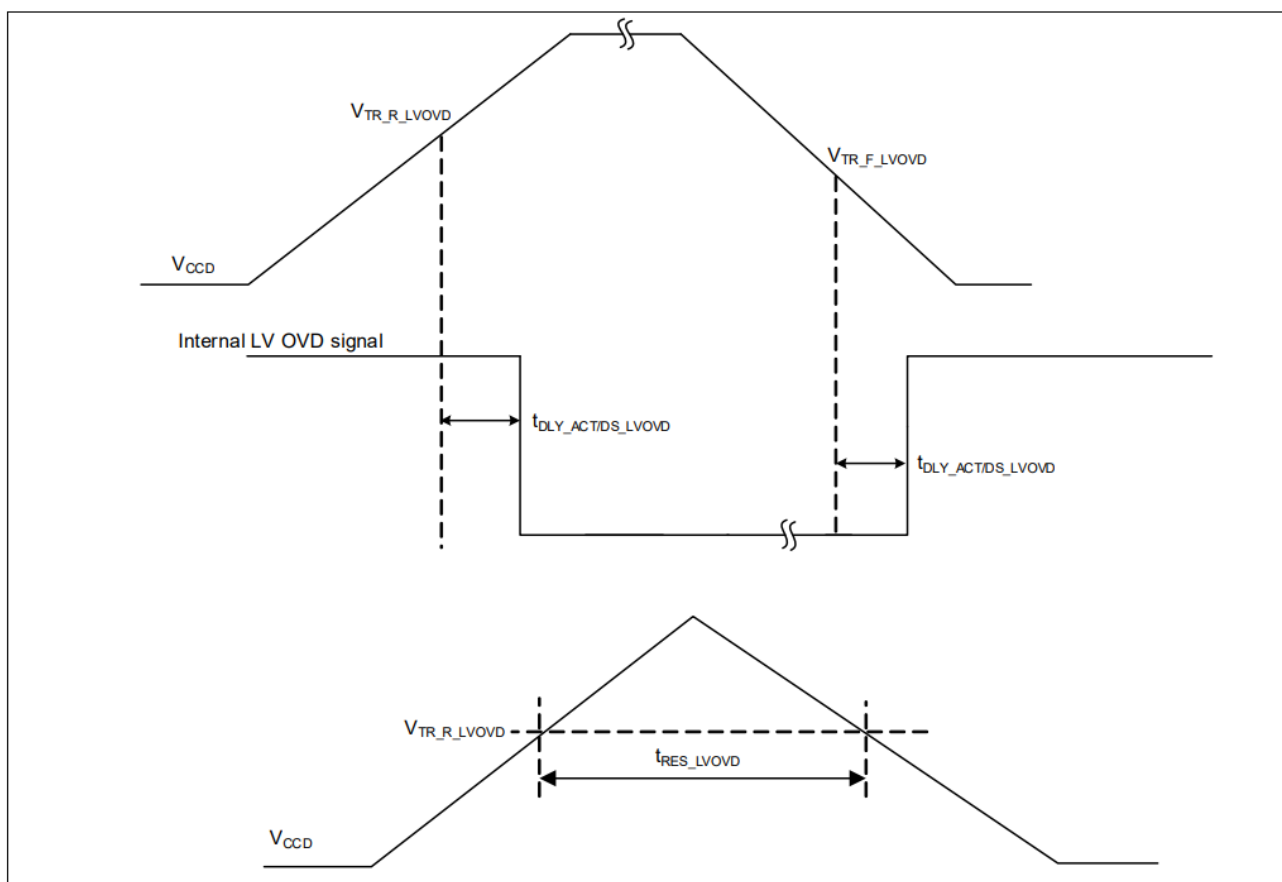


图 26-19 低压 OVD 规格

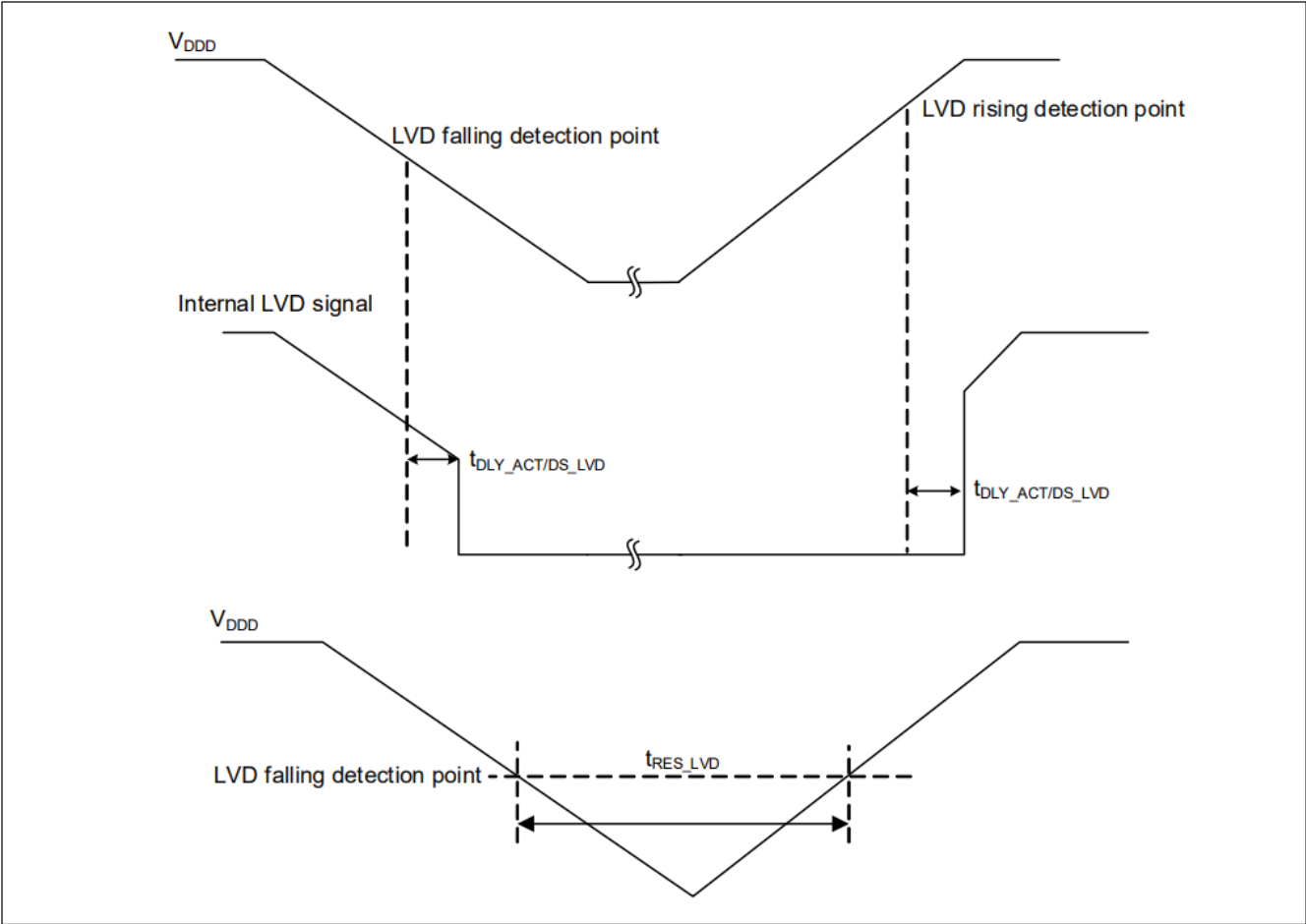


图 26-20 LVD 规格

26.10.1 SWD 接口

表 26-17 SWD 接口规格 [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID300	f _{SWDCLK}	SWD clock input frequency	–	–	10	MHz	2.7 V ≤ V _{DD} ≤ 5.5 V
SID301	t _{SWDI_SETUP}	SWDI setup time	0.25 × T	–	–	ns	T = 1 / f _{SWDCLK}
SID302	t _{SWDI_HOLD}	SWDI hold time	0.25 × T	–	–	ns	T = 1 / f _{SWDCLK}
SID303	t _{SWDO_VALID}	SWDO valid time	–	–	0.5 × T	ns	T = 1 / f _{SWDCLK}
SID304	t _{SWDO_HOLD}	SWDO hold time	1	–	–	ns	T = 1 / f _{SWDCLK}

表26-18 JTAG AC规格 【条件: drive_sel<1:0>= 00】

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID620	t _{JCKH}	TCK HIGH time	30	–	–	ns	30-pF load
SID621	t _{JCKL}	TCK LOW time	30	–	–	ns	30-pF load
SID622	t _{JCP}	TCK clock period	66.7	–	–	ns	30-pF load
SID623	t _{JSU}	TDI/TMS setup time	12	–	–	ns	30-pF load
SID624	t _{JH}	TDI/TMS hold time	12	–	–	ns	30-pF load

表 26-18 JTAG AC规格 [条件: drive_sel<1:0>= 00] (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID625	t_{JZX}	TDO High-Z to active	–	–	30	ns	30-pF load
SID626	t_{JXZ}	TDO active to High-Z	–	–	30	ns	30-pF load
SID627	t_{JCO}	TDO clock to output	–	–	30	ns	30-pF load

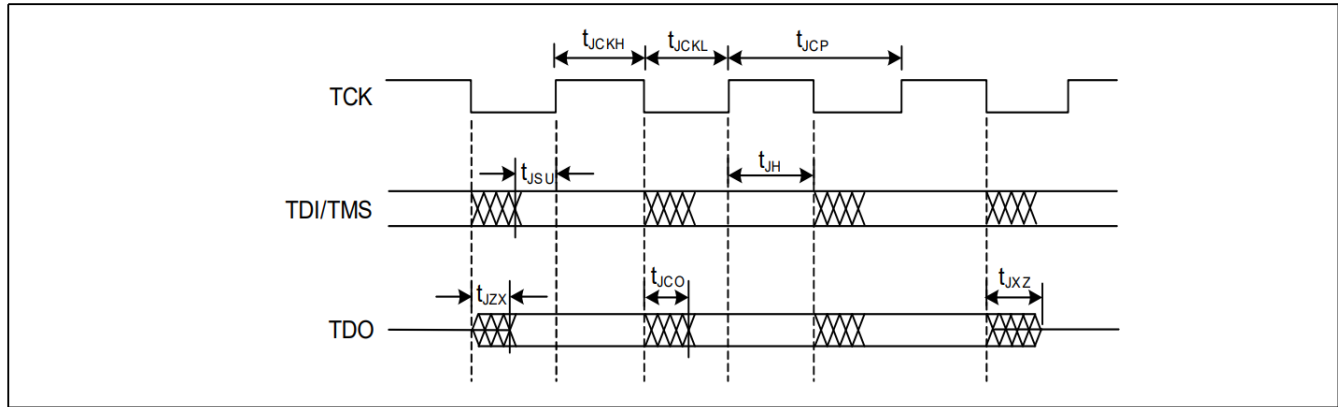


图 26-21 JTAG 规格

表 26-19 跟踪规格 [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1412A	C_{TRACE}	Trace capacitive load	–	–	30	pF	
SID1412	t_{TRACE_CYC}	Trace clock period	40	–	–	ns	Trace clock cycle time for 25 MHz
SID1413	t_{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width
SID1414	t_{TRACE_CLKH}	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width
SID1415A	t_{TRACE_SETUP}	Trace data setup time	3	–	–	ns	Trace data setup time
SID1416A	t_{TRACE_HOLD}	Trace data hold time	2	–	–	ns	Trace data hold time



时钟规格

26.11

除非另有说明，所有规格均适用于-40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表26-20 根时钟和中间时钟^[67]

Clock	Max permitted clock frequency (MHz) ^[68]	Source	Maximum permitted clock frequency setting (MHz) ^[68]						Description
			PLL/FLL Clock source: ECO ^[69]			PLL/FLL Clock source: IMO ^[70]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF0	160	PLL200#0	160	NA	NA	155	NA	NA	Root clock for CPUSS, PERI
		FLL	100	NA	NA	96	NA	NA	
	100	PLL200#0	100	NA	NA	98	NA	NA	
		FLL	100	NA	NA	96	NA	NA	
CLK_HF1	250	PLL400#0	250	240	250	242	237	239	CM7 CPU Core#0, CM7 CPU Core#1 clock
		FLL	100	NA	NA	96	NA	NA	
CLK_HF2	100	PLL200#1	100	NA	NA	98	NA	NA	Peripheral clock root other than CLK_PERI
		FLL	100	NA	NA	96	NA	NA	
CLK_HF3	100	PLL200#1	100	NA	NA	98	NA	NA	Event generator (CLK_REF), clock output on EXT_CLK pins (when used as output)
		FLL	100	NA	NA	96	NA	NA	
CLK_HF4	50	PLL200#1	50	NA	NA	48	NA	NA	Ethernet Channel#0, Ethernet Channel#1 internal clock
		FLL	50	NA	NA	48	NA	NA	
CLK_HF5	196.608	PLL400#1	196.608	193	196.608	189	185	187	I ² S channel#0, I ² S channel#1, I ² S channel#2 interface clock, Ethernet Channel#0 TSU
		FLL	100	NA	NA	96	NA	NA	
CLK_HF6	200	PLL200#1	200	NA	NA	190	NA	NA	Root clock for SDHC, SMIF interface clock
		FLL	100	NA	NA	96	NA	NA	
CLK_HF7	8	ILO	NA	NA	NA	NA	NA	NA	CSV
CLK_FAST_0	250	PLL400#0	250	240	250	242	237	239	Generated by clock gating CLK_HF1, CM7 CPU Core#0, intermediate clock
		FLL	100	NA	NA	96	NA	NA	
CLK_FAST_1	250	PLL400#0	250	240	250	242	237	239	Generated by clock gating CLK_HF1, CM7 CPU Core#1, intermediate clock
		FLL	100	NA	NA	96	NA	NA	

注：

67. 未列出的中间时钟具有与其父时钟相同的限制。
68. 相应时钟源 (PLL/FLL + 分频器) 之后的最大时钟频率。所有内部公差和影响都包含在这些频率内。
69. 对于 ECO：设计可容忍外部时钟源高达 ±150 ppm 的不确定度。
70. IMO操作频率公差包括在内。 当不使用深度睡眠模式时，时钟源 IMO 情况下的最大允许时钟频率设置等于时钟源 ECO 情况下的最大允许时钟频率设置。
71. CLOCK_SLOW 和 CLK_HF0 通过整数频率比关联（即 1:1、1:2、1:3 等）。



表26-20 根时钟和中间时钟^[67]

Clock	Max permitted clock frequency (MHz) ^[68]	Source	Maximum permitted clock frequency setting (MHz) ^[68]						Description
			PLL/FLL Clock source: ECO ^[69]			PLL/FLL Clock source: IMO ^[70]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_MEM	160	PLL200#0	160	NA	NA	155	NA	NA	Generated by clock gating CLK_HF0, intermediate clock for SMIF, Flash
		FLL	100	NA	NA	96	NA	NA	
	100	PLL200#0	100	NA	NA	98	NA	NA	
		FLL	100	NA	NA	96	NA	NA	
CLK_SLOW	100	PLL200#0	100	NA	NA	98	NA	NA	Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, SDHC, Ethernet
		FLL	100	NA	NA	96	NA	NA	
CLK_PERI	100	PLL200#0	100	NA	NA	98	NA	NA	Generated by clock gating CLK_HF0, intermediate clock for IOSS, TCPWM0, CPU trace, SMIF
		FLL	100	NA	NA	96	NA	NA	

电气规格

表 26-21 CLK_HF0 和 CLK_SLOW 之间的关系（示例）^[71]

CLK_HF0 (MHz)	CLK_SLOW (MHz)
160	80
120	60
100	100
80	80

表 26-22 PLL400 操作模式

PLL400 operation mode	Spread spectrum clock generation (SSCG)	Fractional
Integer	OFF	OFF
SSCG	ON	OFF
Fractional	OFF	ON

表 26-23 IMO AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID310	f _{IMOTOL}	IMO operating frequency	7.68	8	8.32	MHz	
SID311	t _{STARTIMO}	IMO start-up time	–	–	7.5	μs	Start-up time to 90% of final frequency
SID312	I _{IMO_ACT}	IMO current	–	13.5	22	μA	

表 26-24 ILO AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID320	f _{ILOTRIM}	ILO operating frequency	30.47424	32.768	35.06176	kHz	
SID321	t _{STARTILO}	ILO start-up time	–	8	12	μs	Start-up time to 90% of final frequency
SID323	I _{ILO}	ILO current	–	500	2800	nA	

表 26-25 ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID330	f _{ECO}	Crystal frequency range	8	–	33.34	MHz	
SID332	R _{FDBK}	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100-kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design
SID333	I _{ECO3}	ECO current at T _J = 150 °C	–	–	2000	μA	Maximum operation current with a 33-MHz crystal, 18-pF load

电气规格

表 26-25 ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID334	$t_{\text{START_8M}}$	8-MHz ECO start-up time ^[72]	–	–	10	ms	Time from set CLK_ECO_-CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams)
SID335	$t_{\text{START_33M}}$	33-MHz ECO start-up time ^[72]	–	–	1	ms	Time from set CLK_ECO_-CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams)

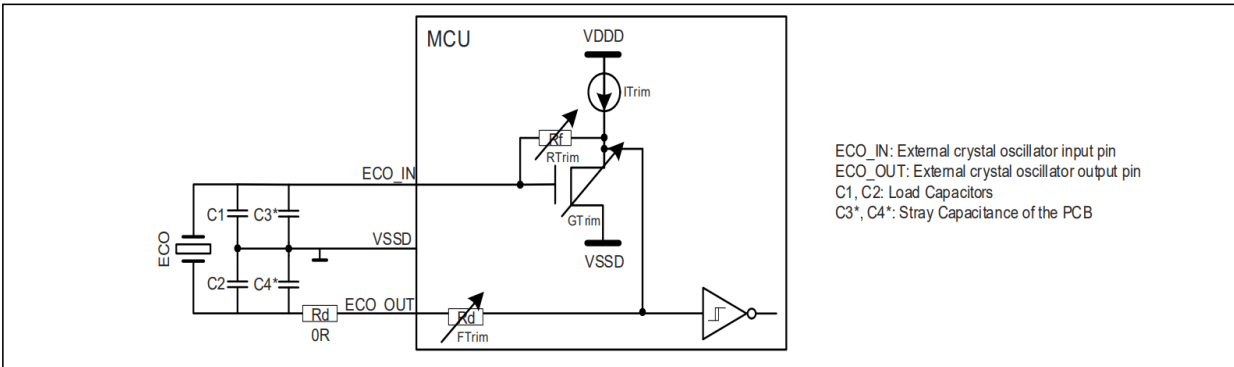


图 26-22 ECO连接方案^[73]
表 26-26 PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
PLL (without SSCG and fractional divider) specifications for 200 MHz							
SID340	$t_{\text{PLL200_LOCK}}$	Time to achieve PLL lock	–	–	35	μs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SID341	$f_{\text{PLL_OUT}}$	Output frequency from PLL block	11	–	200	MHz	
SID342	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO

注:

72. 主要看外部晶振。

73. 有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-24401，TRAVEO™ T2G Automotive MCU body controller high architecture technical reference manual）。

电气规格

表 26-26 PLL 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID343	PLL_LJIT2	Long term jitter	-0.5	-	0.5	ns	For 500 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SID344	PLL_LJIT3	Long term jitter	-0.5	-	0.5	ns	For 1000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SID345A1	PLL_LJIT5	Long term jitter	-0.75	-	0.75	ns	For 10000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SID346	$f_{\text{PLL_IN}}$	PLL input frequency	3.988	-	33.34	MHz	
SID347	$I_{\text{PLL_200M}}$	PLL operating current ($f_{\text{OUT}} = 200$ MHz)	-	0.87	1.8	mA	$f_{\text{OUT}} = 200$ MHz
SID348C	$f_{\text{PLL_VCO}}$	VCO frequency	170	-	400	MHz	
SID349C	$f_{\text{PLL_PFD}}$	PFD frequency	3.988	-	8	MHz	
PLL (with SSCG and fractional divider) specifications for 400 MHz							
SID340A	$t_{\text{PLL400_LOCK}}$	Time to achieve PLL lock	-	-	50	μs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SID341A4	$f_{\text{OUT0_4M}}$	Programmed output frequency from PLL Block	25	-	250	MHz	Integer mode
SID341B4	$f_{\text{OUT1_4M}}$	Programmed output frequency from PLL Block	25	-	240	MHz	SSCG mode
SID343A	SPREAD_D	Spread spectrum modulation depth	0.5	-	3	%	Downspread only, triangle modulation
SID343B	$f_{\text{SPREAD_MR}}$	Spread spectrum modulation rate	-	-	32	kHz	Selected by modulation divider from f_{PFD}
SID342D14	PLL400_L-JIT14	Long term jitter	-0.25	-	0.25	ns	For 125 ns Guaranteed by design f_{VCO} : 800 MHz or 500 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 250 MHz

电气规格
表 26-26 PLL 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID343D14	PLL400_L-JIT24	Long term jitter	-0.5	-	0.5	ns	For 500 ns Guaranteed by design f_{VCO} : 800 MHz or 500 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 250 MHz
SID344D14	PLL400_L-JIT34	Long term jitter	-1	-	1	ns	For 1000 ns Guaranteed by design f_{VCO} : 800 MHz or 500 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 250 MHz
SID345E14	PLL400_L-JIT54	Long term jitter	-1.5	-	1.5	ns	For 10000 ns Guaranteed by design f_{VCO} : 800 MHz or 500 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 250 MHz
SID345A	f_{VCO}	VCO frequency	400	-	800	MHz	
SID346A	f_{IN}	PLL input frequency	3.988	-	33.34	MHz	
SID347A	I_{PLL_400M}	PLL operating current ($f_{OUT} = 400$ MHz)	-	1.4	2.2	mA	$f_{OUT} = 400$ MHz
SID348A	f_{PFD_S}	PFD Frequency (f_{IN} / Reference divider)	3.988	-	20	MHz	Integer/SSCG mode
SID349A	f_{PFD_F}	PFD Frequency (f_{IN} / Reference divider)	8	-	20	MHz	Fractional operation
SID341C	$f_{OUT_400_8S1}$	Output frequency from PLL Block (SSCG mode)	93	-	105	MHz	$f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 512$, Modulation depth: 3%
SID342C	$t_{PLL_C-JIT400_8S1}$	Cycle-to-cycle jitter (SSCG mode)	-710	-	710	ps	$f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 512$, Modulation depth: 3%
SID341D	$f_{OUT_400_8S2}$	Output frequency from PLL Block (SSCG mode)	93	-	105	MHz	$f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 256$, Modulation depth: 3%
SID342D	$t_{PLL_C-JIT400_8S2}$	Cycle-to-cycle jitter (SSCG mode)	-710	-	710	ps	$f_{PFD} = 8$ MHz, $f_{VCO} = 400$ MHz, $f_{OUT} = 100$ MHz, Modulation frequency: $f_{PFD} / 256$, Modulation depth: 3%



电气规格

表 26-27 FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	–	–	5	μs	Wakeup with < 10 °C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value
SID351	f_{FLL_OUT}	Output frequency from FLL block	24	–	100	MHz	Output range of FLL divided-by-2 output
SID352	FLL_CJIT	FLL frequency accuracy	–1	–	1	%	This is added to the error of the source
SID353	f_{FLL_IN}	Input frequency	0.25	–	80	MHz	
SID354	I_{FLL}	FLL operating current	–	250	360	μA	Reference clock: IMO, CCO frequency: 200 MHz, FLL frequency: 100 MHz, guaranteed by design

电气规格

表 26-28 WCO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	f_{WCO}	Crystal frequency	–	32.768	–	kHz	Maximum drive level: 0.5 μ W
SID361	WCO_DC	WCO duty cycle	10	–	90	%	
SID362	t_{START_WCO}	WCO start up time ^[74]	–	–	1000	ms	For Grade-S devices Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams)
SID362E	t_{START_WCOE}	WCO start-up time ^[74]	–	–	1400	ms	For Grade-E devices Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams)
SID363	I_{WCO}	WCO current	–	1.4	–	μ A	

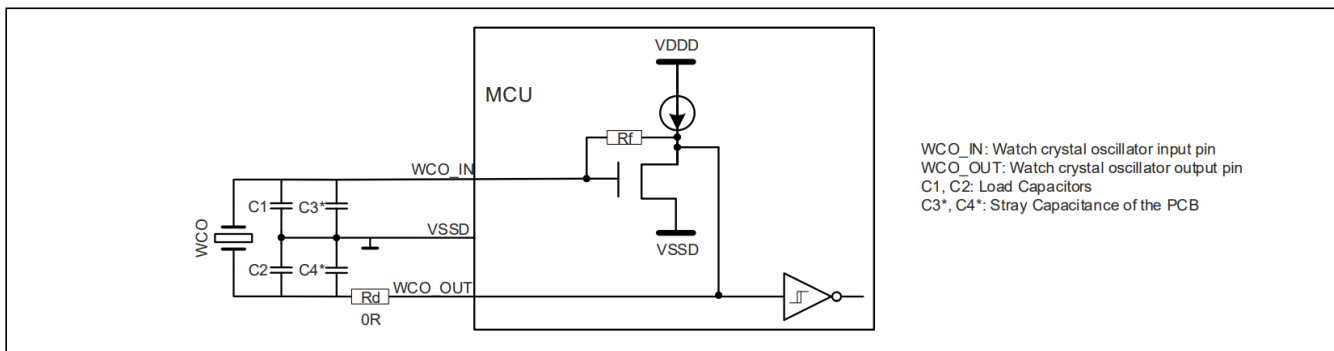


图 26-23 WCO连接方案^[75]

表 26-29 外部时钟输入规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f_{EXT}	External clock input frequency	0.25	–	80	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	External clock duty cycle	45	–	55	%	

注:

74. 主要看外部晶振。

75. 有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-24401， TRAVEO™ T2G Automotive MCU body controller high architecture technical reference manual）。



电气规格

表26-30 MCWDT超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID410	t _{MCWDT1}	Minimum MCWDT timeout	57	–	–	μs	When using the ILO (32.768 kHz + 7%) and 16-bit MCWDT counter Guaranteed by design
SID411	t _{MCWDT2}	Maximum MCWDT timeout	–	–	2.15	s	When using the ILO (32.768 kHz – 7%) and 16-bit MCWDT counter Guaranteed by design

表 26-31 WDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID412	t _{WDT1}	Minimum WDT timeout	57	–	–	μs	When using the ILO (32.768 kHz + 7%) and 32-bit WDT counter, guaranteed by design
SID413	t _{WDT2}	Maximum WDT timeout	–	–	39.15	h	When using the ILO (32.768 kHz – 7%) and 32-bit WDT counter, guaranteed by design
SID414	t _{WDT3}	Default WDT timeout	–	1000	–	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design

26.12 时钟时序图

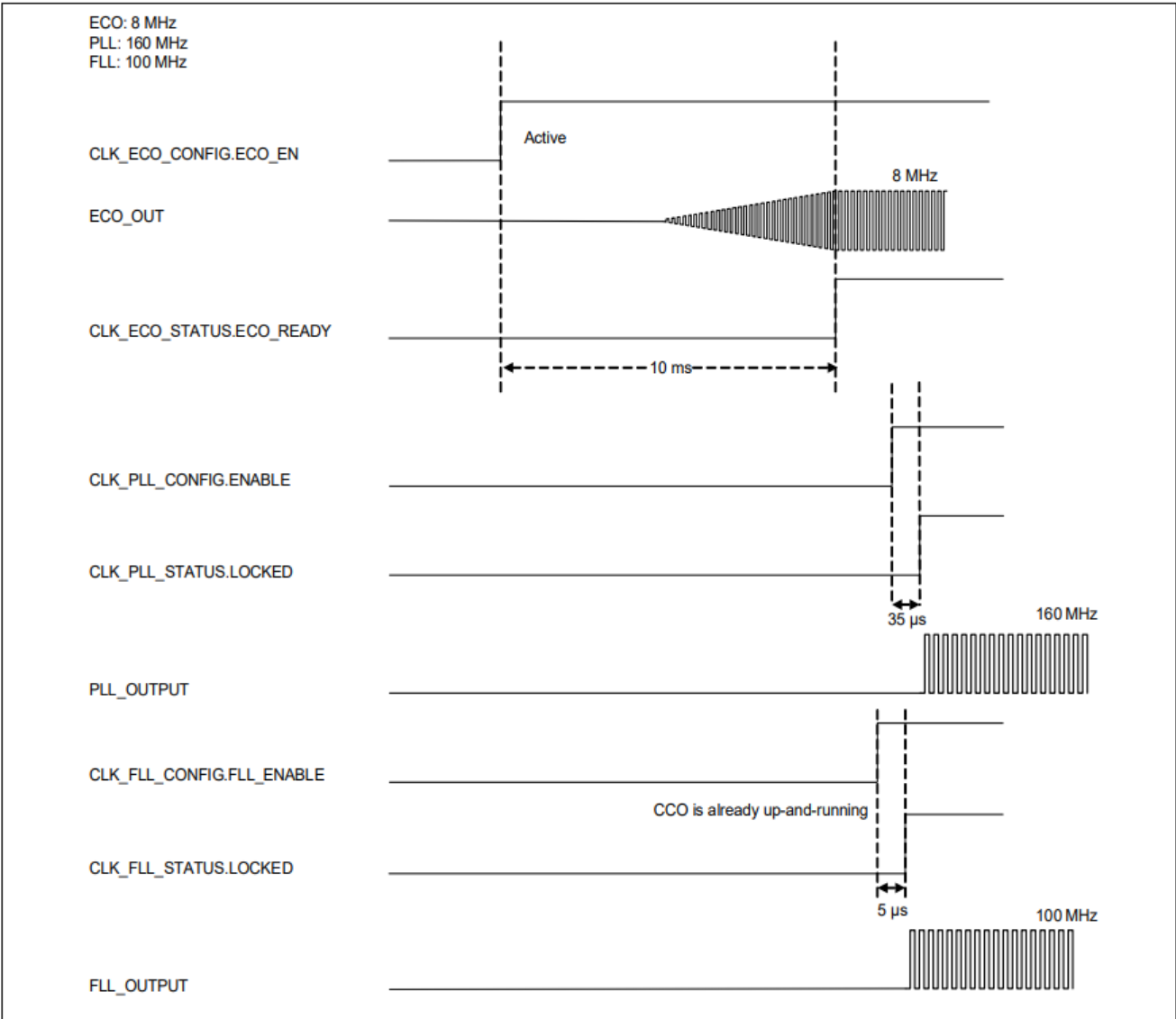


图 26-24 ECO 至 PLL 或 FLL 图



电气规格

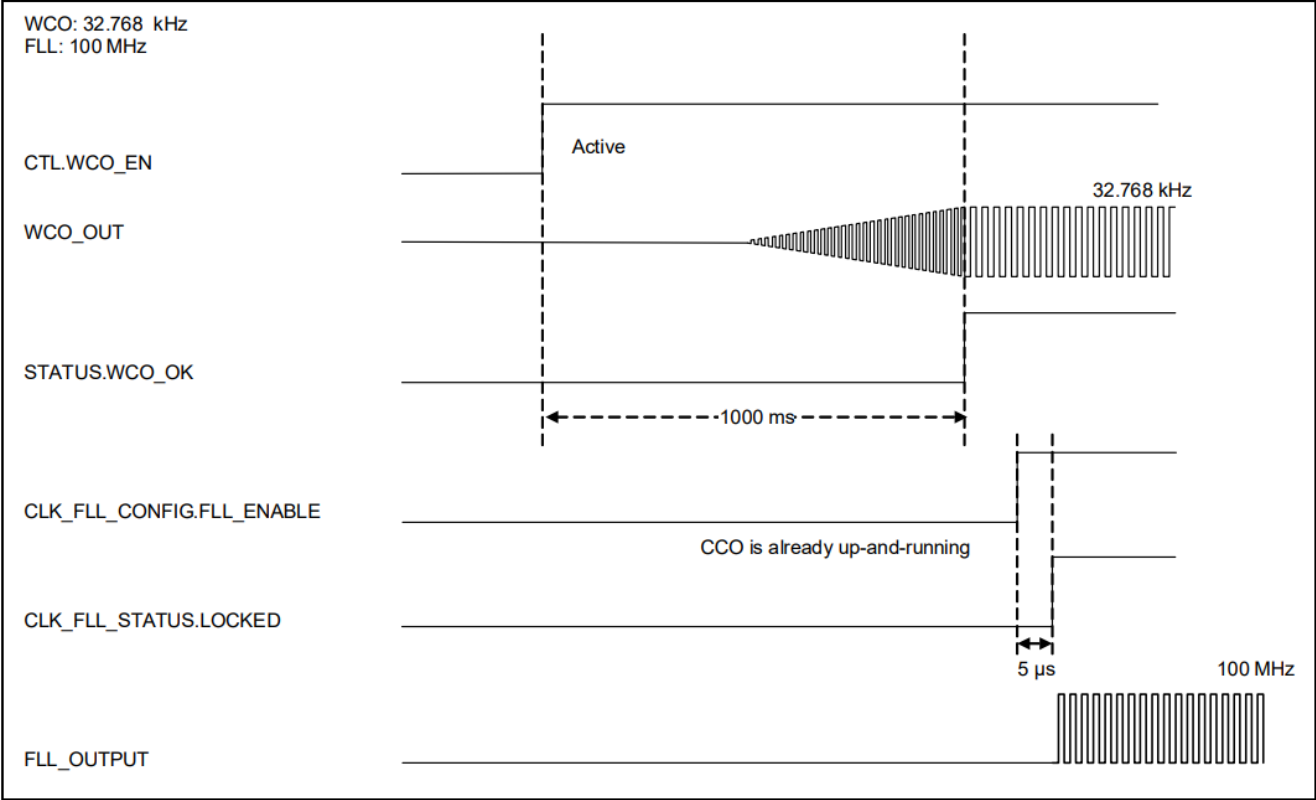


图 26-25 WCO 至 FLL 图

电气规格
26.13 以太网规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 26-32 以太网规格[条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
以太网通用规格							
SID368	f _{SYS}	System clock max frequency	–	–	100	MHz	Guaranteed by design
SID399	V _{ETH}	Ethernet MAC I/O supply voltage	3.0	–	3.6	V	For V _{DDD}
SID364A	C _{L_MD}	Load capacitance	–	–	25	pF	For MDIO all signals between MAC and PHY using GPIO_STD
SID364A2	C _{L_MG}	Load capacitance	–	–	15	pF	For MII and RMII all signals between MAC and PHY using GPIO_STD
SID365A	t _{RF}	Rise / fall time (For input pins)	–	–	2	ns	20% to 80%, for MII and RMII using GPIO_STD

GPIO_STD 的以太网 MII 规格

SID375	f _{TXRX_CLK}	MII TX/RX_CLK Clock frequency at 100 Mbps	–100 ppm	25	100 ppm	MHz	
SID376	DUTY_TX-RX_CLK	TX/RX Clock Duty cycle	35	–	65	%	
SID372	t _{SKEWT}	MII Transmit data (TX_CTL, TXD, TX_ER) valid after TX_CLK	0.5	–	25	ns	
SID373	t _{SUR}	MII Receive data setup to RX_CLK rising edge	10	–	–	ns	
SID374	t _{HOLDR}	MII Receive data hold to RX_CLK rising edge	10	–	–	ns	

GPIO_STD 的以太网 RMII 规格

SID375A	f _{REF_CLK}	RMII reference Clock frequency (input)	–50ppm	50	50ppm	MHz	External clock
SID376A	DUTY_REF_CLK	Duty cycle of reference clock (input)	35	–	65	%	
SID377	t _{SU}	RX_CTL, RXD[1:0], RX_ER Data Setup to REF_CLK rising edge	4	–	–	ns	
SID378	t _{HOLD}	RX_CTL, RXD[1:0], RX_ER, Data hold from REF_CLK rising edge	2	–	–	ns	
SID393	t _{TXOUT}	TX_CTL, TXD[1:0], Data output delay from REF_CLK rising edge	2	–	14.6	ns	For GPIO_STD

GPIO_STD 的以太网 MDIO 规格

SID395	t _{MDCYC}	MDC clock cycle	400	–	–	ns	
SID395A	t _{HL_MDCYC}	The minimum HIGH and LOW times for MDC	160	–	–	ns	
SID396	t _{MDIS}	MDIO input setup time to MDC rising edge	100	–	–	ns	

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表 26-32 以太网规格 (续) [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID397	t_{MDIH}	MDIO input hold time to MDC rising edge	0	–	–	ns	
SID398	t_{MDIO}	MDIO output skew from MDC rising edge	10	–	390	ns	

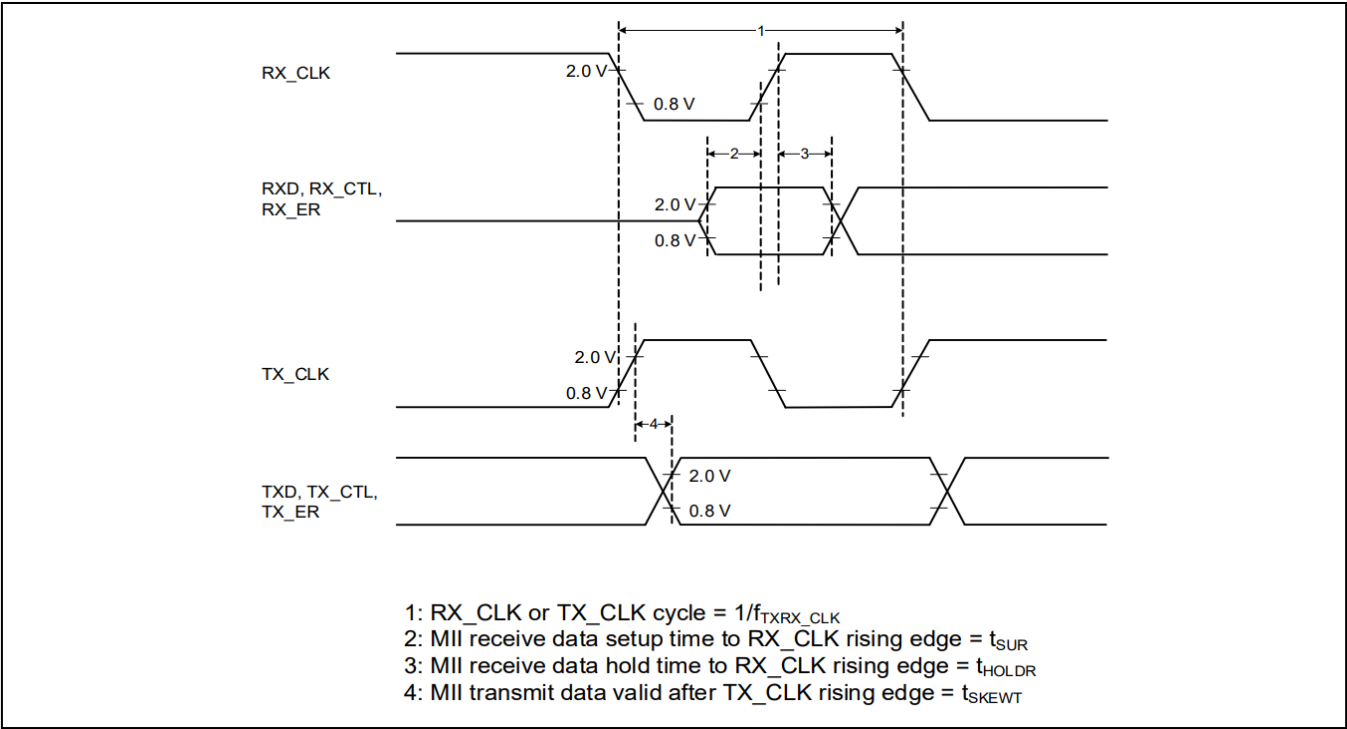


图 26-26 MII 时序图

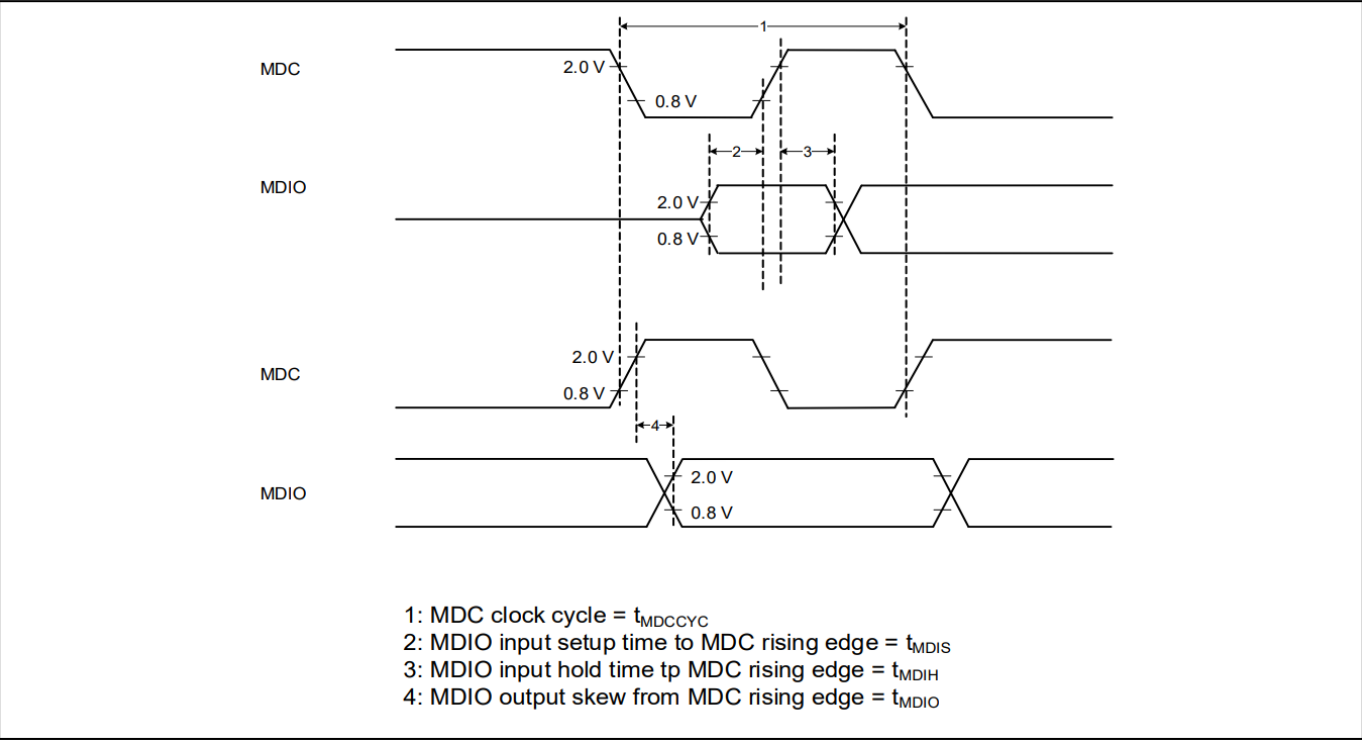


图 26-27 MDIO 时序图

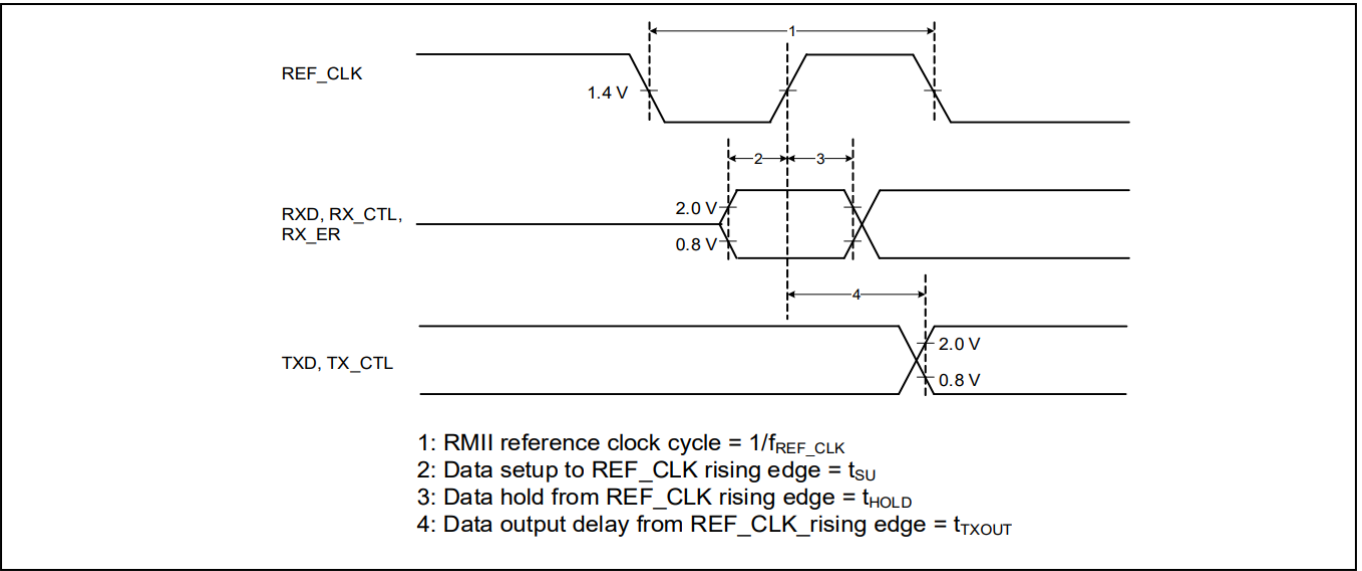


图 26-28 RMII 时序图



26.13.1 最低总线频率要求

下表详细列出了所有可能的以太网配置和MAC速度所需的最低工作频率。以太网模块使用**AHB** -Lite 接口进行 DMA 访问。

表 26-33 MAC 速度的最小 AHB 频率

DMA bus width	MAC rate	Minimum AHB frequency
32	100 Mbps	15 MHz
32	10 Mbps	10 MHz

电气规格

26.14 SDHC规格

除非另有说明，所有规格均在 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V 的条件下有效。

表26-34 SDHC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SDHC 和 eMMC 规格（时钟源必须除以 2 或更多在 DDR 模式下）							
SID801	V_{SDHC}	SDHC IO supply voltage	2.7	–	3.6	V	For V_{DDIO_1} or V_{DDIO_3}
SID802	I_{ODS}	I/O drive select	8	–	8	mA	drive_sel<1:0>= 0b00 for all modes
SID803	t_{IT}	Input transition time	0.7	–	3	ns	
SD: GPIO_STD/HSIO_STD 的 DS 时序规格							
SID810	f_{LP}	Interface clock period	–	–	25	MHz	40-ns period
SID812	C_{D}	I/O loading at DATA/CMD pins	–	–	40	pF	
SID813	C_{C}	I/O loading at CLK pins	–	–	40	pF	
SID814	t_{OS}	Output setup time of CMD/DAT prior to CLK	5.5	–	–	ns	
SID815	t_{OH}	Output hold time of CMD/DAT after CLK	5.5	–	–	ns	
SID816	$t_{\text{IS_LP}}$	Input setup time of CMD/DAT prior to CLK	24	–	–	ns	Clock period - Output delay
SID818	t_{IH}	Input hold time of CMD/DAT after CLK	0	–	–	ns	
SD: GPIO_STD/HSIO_STD 的 HS 时序规格							
SID820	$f_{\text{LP_SD_HS}}$	Interface clock period	–	–	50	MHz	20-ns period
SID822	$C_{\text{D_SD_HS}}$	I/O loading at DATA/CMD pins	–	–	40	pF	
SID823	$C_{\text{C_SD_HS}}$	I/O loading at CLK pins	–	–	40	pF	
SID824	$t_{\text{OS_SD_HS}}$	Output setup time of CMD/DAT prior to CLK	6.5	–	–	ns	
SID825	$t_{\text{OH_SD_HS}}$	Output hold time of CMD/DAT after CLK	2.5	–	–	ns	
SID826	$t_{\text{IS_LP_SD_HS}}$	Input setup time of CMD/DAT prior to CLK	4	–	–	ns	Clock period less output delay
SID828	$t_{\text{IH_SD_HS}}$	Input hold time of CMD/DAT after CLK	2.5	–	–	ns	
eMMC: GPIO_STD/HSIO_STD 的 BWC 时序规格							
SID870	$f_{\text{LP_eMMC_BWC}}$	Interface clock period	–	–	26	MHz	38.4-ns period
SID872	$C_{\text{D_eMMC_BWC}}$	I/O loading at DATA/CMD pins	–	–	30	pF	
SID873	$C_{\text{C_eMMC_BWC}}$	I/O loading at CLK pins	–	–	30	pF	
SID874	$t_{\text{OS_eM-MC_BWC}}$	Output setup time of CMD/DAT prior to CLK	3.5	–	–	ns	
SID875	$t_{\text{OH_eM-MC_BWC}}$	Output hold time of CMD/DAT after CLK	3.5	–	–	ns	
SID876	$t_{\text{IS_LP_eM-MC_BWC}}$	Input setup time of CMD/DAT prior to CLK	9.7	–	–	ns	Clock period less output delay
SID878	$t_{\text{IH_eMMC_BWC}}$	Input hold time of CMD/DAT after CLK	8.3	–	–	ns	

电气规格

表 26-34 SDHC 规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
eMMC: HSIO_STD 的 SDR 时序规格							
SID880	$f_{LP_eMMC_SDR}$	Interface clock period	–	–	52	MHz	19.2-ns period
SID882	$C_{D_eMMC_SDR}$	I/O loading at DATA/CMD pins	–	–	30	pF	
SID883	$C_{C_eMMC_SDR}$	I/O loading at CLK pins	–	–	30	pF	
SID884	$t_{OS_eMMC_SDR}$	Output setup time of CMD/DAT prior to CLK	3.5	–	–	ns	
SID885	$t_{OH_eMMC_SDR}$	Output hold time of CMD/DAT after CLK	3.5	–	–	ns	
SID886	$t_{IS_LP_eMMC_SDR}$	Input setup time of CMD/DAT prior to CLK	3.5	–	–	ns	Clock period less output delay
SID888	$t_{IH_eMMC_SDR}$	Input hold time of CMD/DAT after CLK	2.5	–	–	ns	
eMMC: HSIO_STD 的 DDR 时序规格							
SID890	$f_{LP_eMMC_DDR}$	Interface clock period	–	–	52	MHz	19.2-ns period
SID892	DUTY_-CLK_eMMC_DDR	Duty cycle of output CLK	45	–	55	%	
SID893	$C_{D_eMMC_DDR}$	I/O loading at DATA/CMD pins	–	–	20	pF	
SID894	$C_{C_eMMC_DDR}$	I/O loading at CLK pins	–	–	20	pF	
SID895	$t_{OS_eMMC_DDR}$	Output setup time of CMD/DAT prior to CLK	2.6	–	–	ns	
SID896	$t_{OH_eMMC_DDR}$	Output hold time of CMD/DAT after CLK	2.6	–	–	ns	
SID897	$t_{IS_LP_eMMC_DDR}$	Input setup time of CMD/DAT prior to CLK	2.4	–	–	ns	Clock period less output delay
SID899	$t_{IH_eMMC_DDR}$	Input hold time of CMD/DAT after CLK	1.5	–	–	ns	

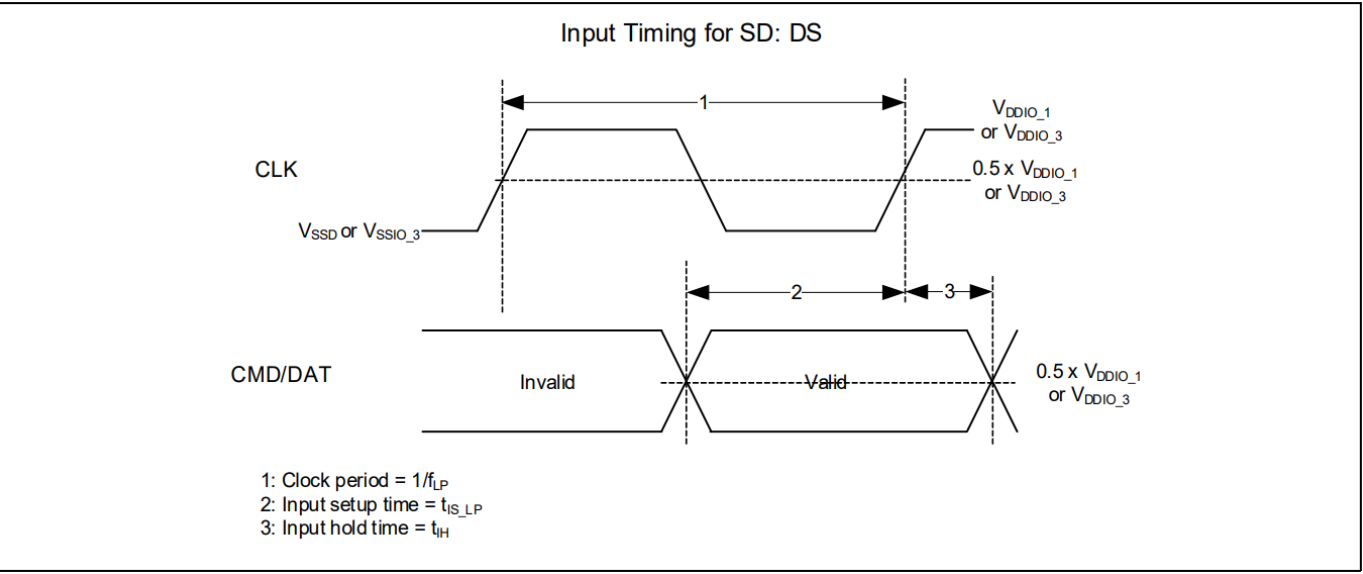


图26-29 SD默认速度输入时序

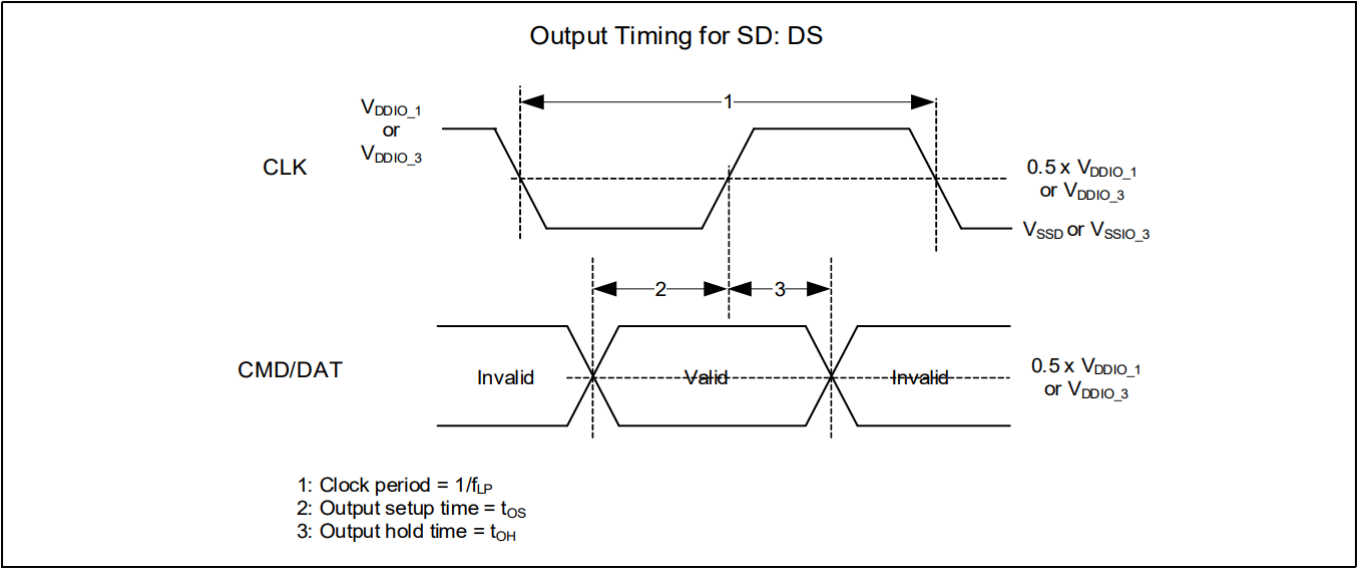


图 26-30 SD 默认速度输出时序

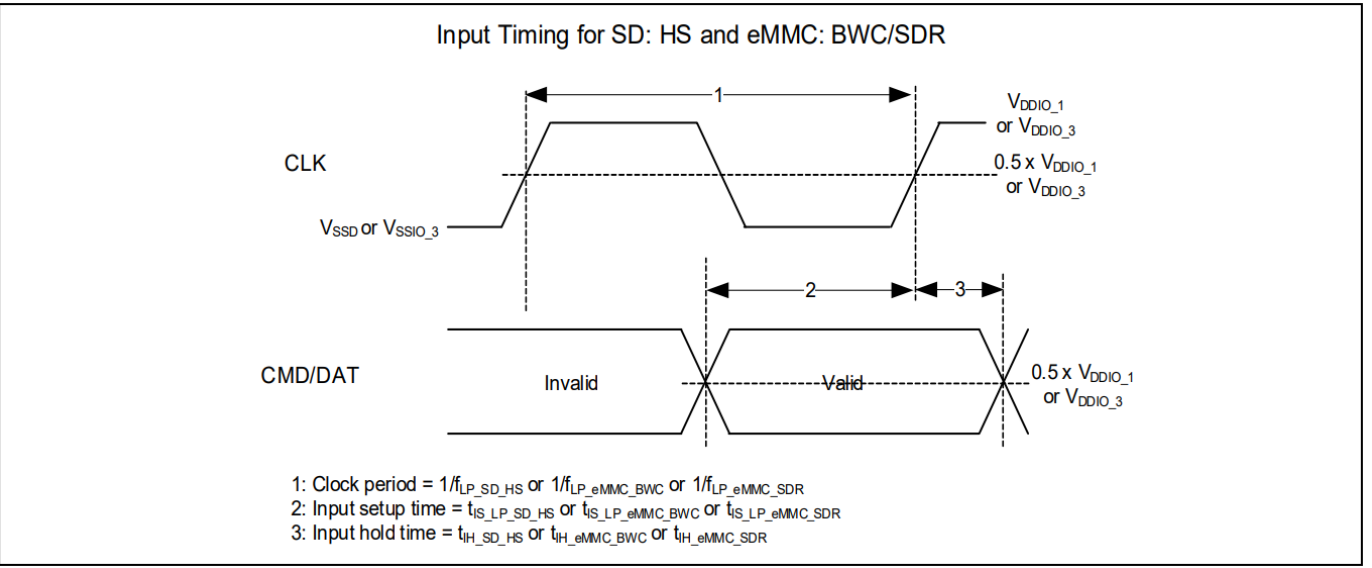


图 26-31 SD 高速和 eMMC BWC/SDR 输入时序

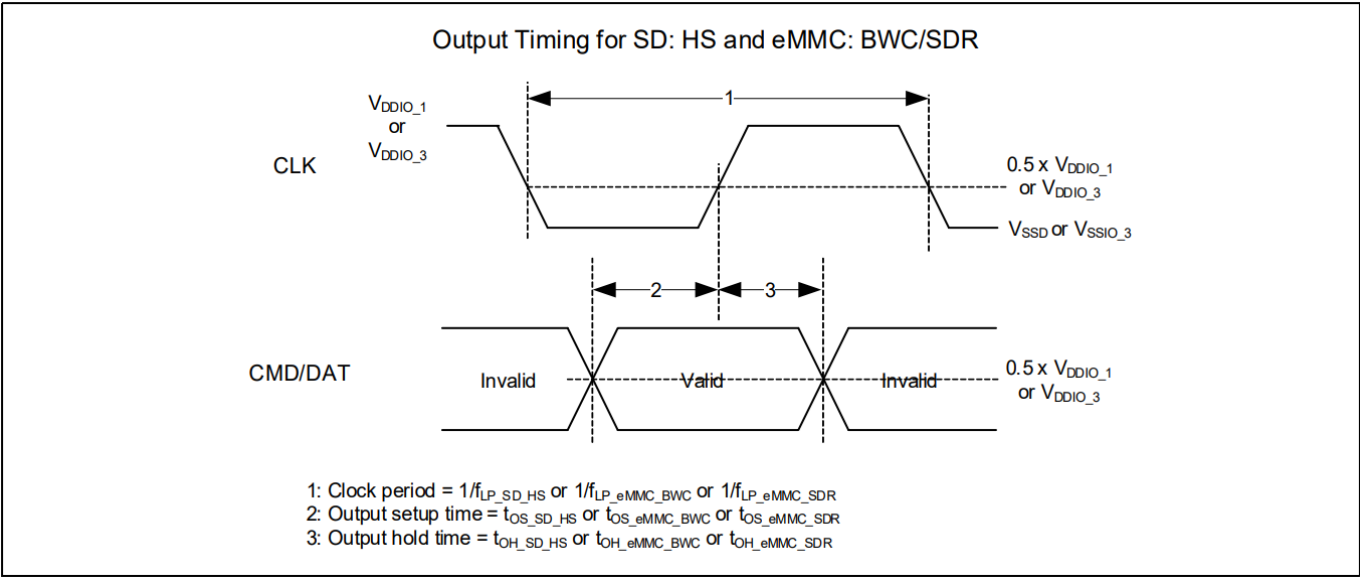


图 26-32 SD 高速和 eMMC BWC/SDR 输出时序

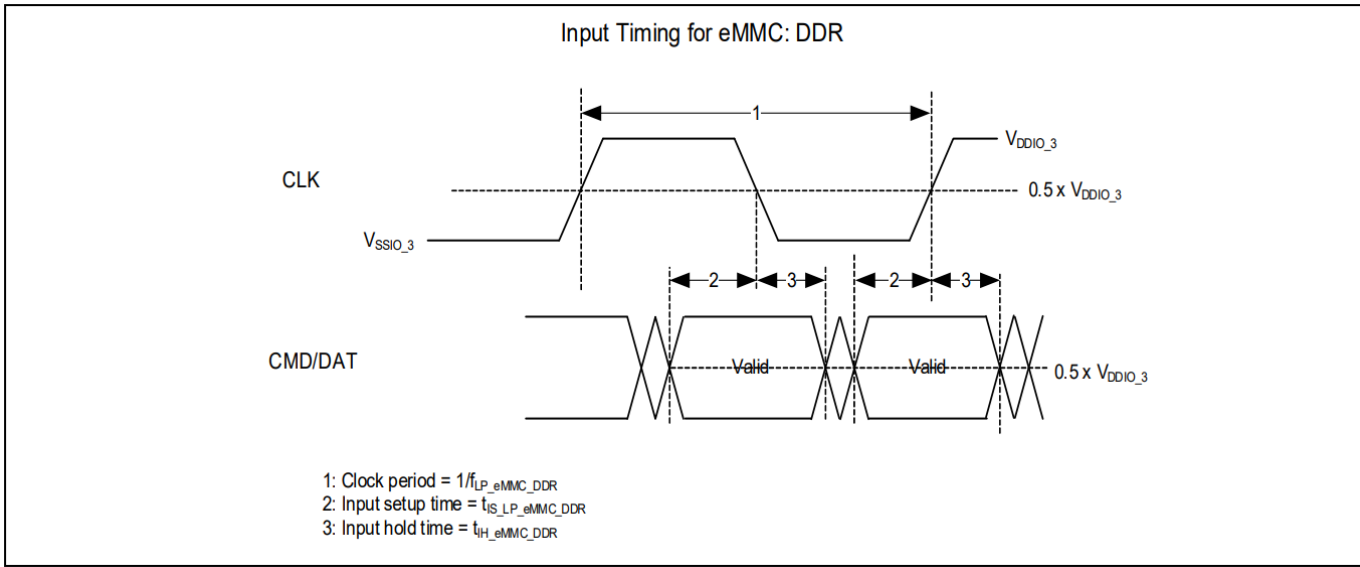


图 26-33 eMMC DDR输入时序

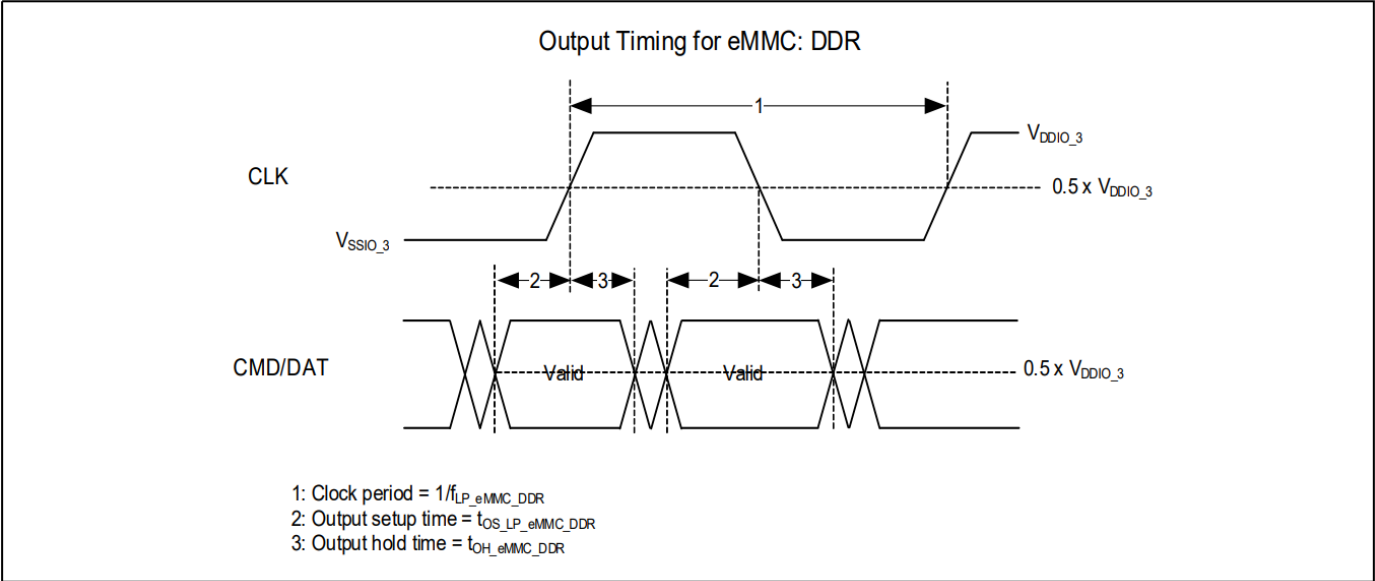


图 26 -34 eMMC DDR输出时序

电气规格

26.15 音频子系统规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 26-35 音频子系统规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID770	f_{AUDIO}	Audio subsystem frequency	–	–	200	MHz	Guaranteed by design
SID772	V_{AUDIO}	Audio subsystem I/O supply voltage	3.0	–	3.6	V	For V_{DDIO_2}
SID773	V_{OL_A}	Output voltage LOW level	–	–	0.4	V	drive_sel<1:0>= 0b0X, Pull-up, pull-down: off
SID774	V_{OH_A}	Output voltage HIGH level	$V_{\text{DDIO}_2} - 0.5$	–	–	V	drive_sel<1:0>= 0b0X, Pull-up, pull-down: off
SID775	$V_{\text{IH_CMOS}_A}$	Input voltage HIGH threshold in CMOS mode	$0.7 \times V_{\text{DDIO}_2}$	–	–	V	
SID776	$V_{\text{IL_CMOS}_A}$	Input Voltage LOW threshold in CMOS mode	–	–	$0.3 \times V_{\text{DDIO}_2}$	V	
I²S/TDM 字元时钟频率							
SID796	$f_{\text{WS_I2S}}$	WS Clock Rate in I ² S mode	8	–	192	kHz	Guaranteed by design
SID797	$f_{\text{WS_TDM}}$	WS Clock Rate in TDM mode	–	–	96	kHz	Guaranteed by design
SID798	Word	Length of I ² S Word	8	–	32	bit	Guaranteed by design
I²S/TDM 主模式							
SID740	$t_{\text{D_WS}}$	Delay Time of TX/RX_WS Output Transition from Falling Edge of TX/RX_SCK Output	–8	–	9	ns	Except TDM 96 kHz mode, TX/RX_WS output and TX/RX_SCK output with drive_sel<1:0>= 0b01, guaranteed by design
SID740A	$t_{\text{D_WS_TDM96A}}$	Delay Time of TX/RX_WS output Transition from Falling Edge of TX/RX_SCK output	–8	–	11	ns	TDM 96 kHz mode, TX/RX_WS output with drive_sel<1:0>= 0b01 and TX/RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design
SID741	$t_{\text{D_SDO}}$	Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output	–8	–	8	ns	TX_SDO and TX_SCK output with drive_sel<1:0>= 0b01 for except TDM 96 kHz mode, guaranteed by design
SID741A	$t_{\text{D_SDO_TDM96}}$	Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output	–8	–	8	ns	TX_SDO with drive_sel<1:0>= 0b01 and TX_SCK output with drive_sel<1:0>= 0b00 for TDM 96 kHz mode, guaranteed by design
SID742	$t_{\text{S_SDI}}$	RX_SDI Setup Time to the Following Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0)	11	–	–	ns	RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design
SID743	$t_{\text{H_SDI}}$	RX_SDI Hold Time to the Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0)	$t_{\text{MCLK_S}} - 0.9$	–	–	ns	RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design
SID744	$t_{\text{S_SDI1}}$	RX_SDI Setup Time to the Following Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1)	11	–	–	ns	RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design
SID745	$t_{\text{H_SDI1}}$	RX_SDI Hold Time to the Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1)	$t_{\text{MCLK_S}} - 0.9$	–	–	ns	RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design

电气规格

表 26-35 音频子系统规格 (续)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID746	t_{SCKCY}	TX/RX_SCK Output Bit Clock Duty Cycle	45	–	55	%	Guaranteed by design
SID748	f_{MCLK_SOC}	MCLK input clock frequency	1.024	–	196.608	MHz	Internal Fractional PLL, guaranteed by design
SID748A	$f_{MCLK_SOC_E}$	MCLK input clock frequency	1.024	–	98.304	MHz	External clock
SID749	t_{MCLK_SOC}	MCLK input clock period	5.086	–	976.563	ns	Guaranteed by design
SID750	t_{JITTER}	MCLK Input clock jitter tolerance	–200	–	200	ps	Guaranteed by design
SID748B	f_{MCLK}	MCLK output clock frequency	1.024	–	25	MHz	MCLK output with drive_sel<1:0> = 0b00 Guaranteed by design
SID748C	f_{MCLK1}	MCLK output clock frequency	1.024	–	15	MHz	MCLK output with drive_sel<1:0> = 0b01 Guaranteed by design
SID749B	f_{MCLK_DT}	MCLK output clock duty	45	–	55	%	Guaranteed by design

I²S/TDM 从模式

SID751	t_{S_WS}	TX/RX_WS Input Alignment Clock Setup Time to the following Rising Edge of TX/RX_SCK Input	5	–	–	ns	Guaranteed by design
SID752	t_{H_WS}	TX/RX_WS Input Alignment Clock Hold Time to the Rising Edge of TX/RX_SCK Input	$t_{MCLK_SOC} + 5.0$	–	–	ns	Guaranteed by design
SID753	t_{D_SDO}	Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 0)	$t_{MCLK_SOC} + 5.0$	–	$t_{MCLK_SOC} + 15$	ns	TX_SDO with drive_sel<1:0> = 0b00, guaranteed by design
SID754	t_{D_SDO1}	Delay Time of TX_SDO Transition from Rising Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 1)	$t_{MCLK_SOC} + 5.0$	–	$t_{MCLK_SOC} + 15$	ns	TX_SDO with drive_sel<1:0> = 0b00, guaranteed by design
SID755	t_{S_SDI}	RX_SDI Setup Time to the Following Rising Edge of RX_SCK Input	5	–	–	ns	Guaranteed by design
SID756	t_{H_SDI}	RX_SDI Hold Time to the Rising Edge of RX_SCK Input	$t_{MCLK_SOC} + 5.0$	–	–	ns	Guaranteed by design
SID757	t_{SCKCY}	TX/RX_SCK Input Bit Clock Duty Cycle	45	–	55	%	Guaranteed by design

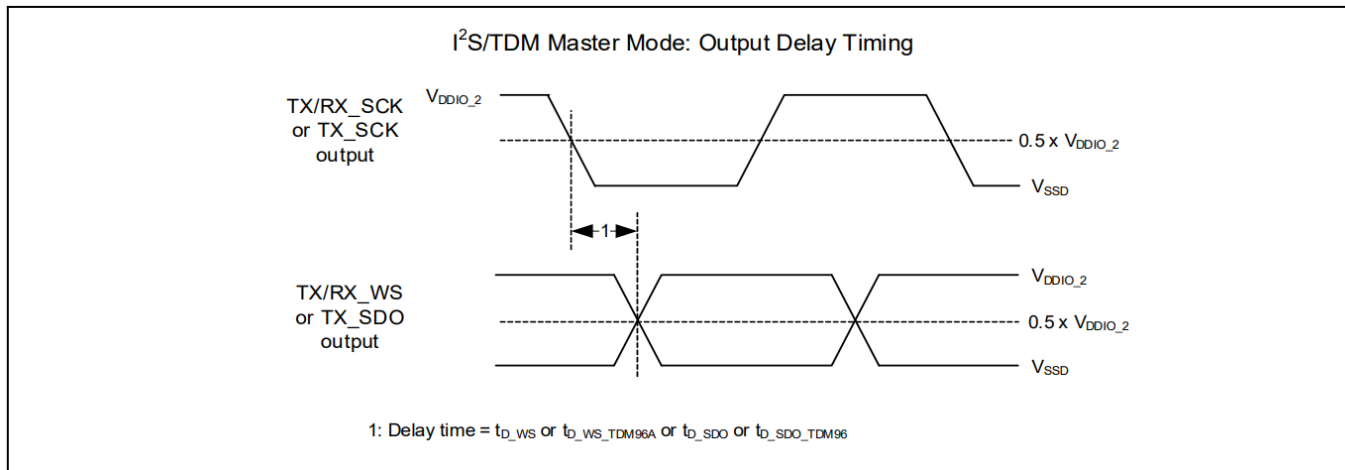


图 26-35 主输出延迟

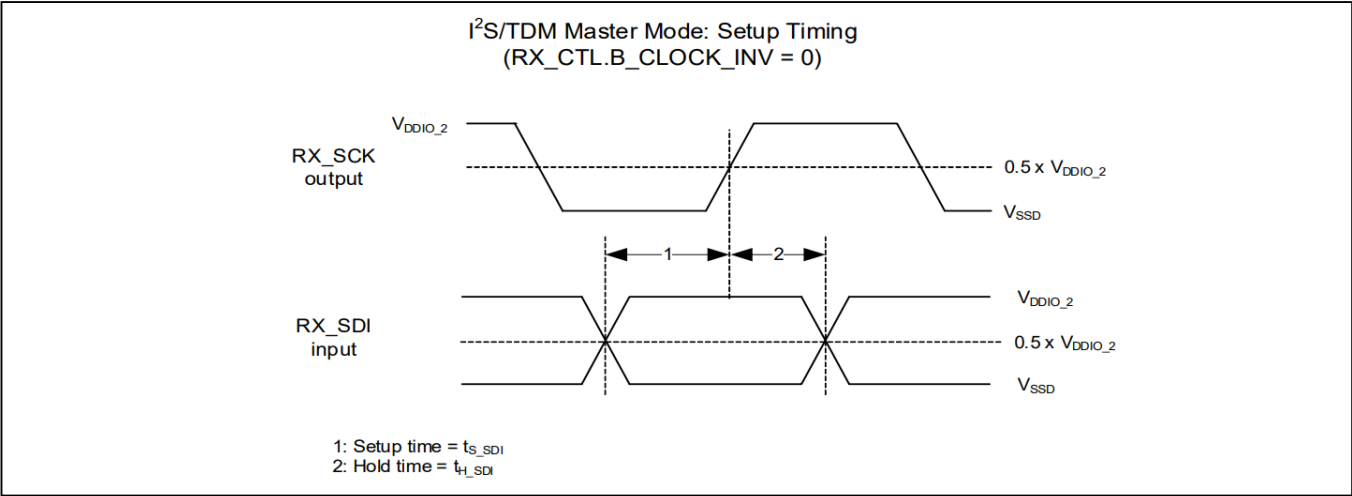


图 26-36 无时钟反转的主设置

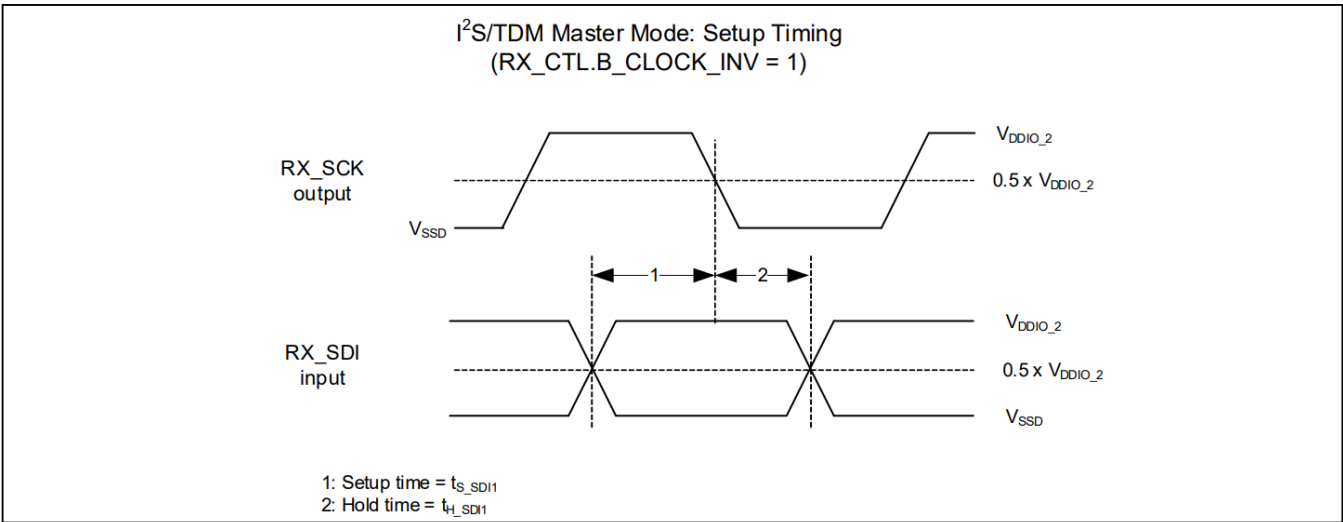


图 26-37 带时钟反转的主设置

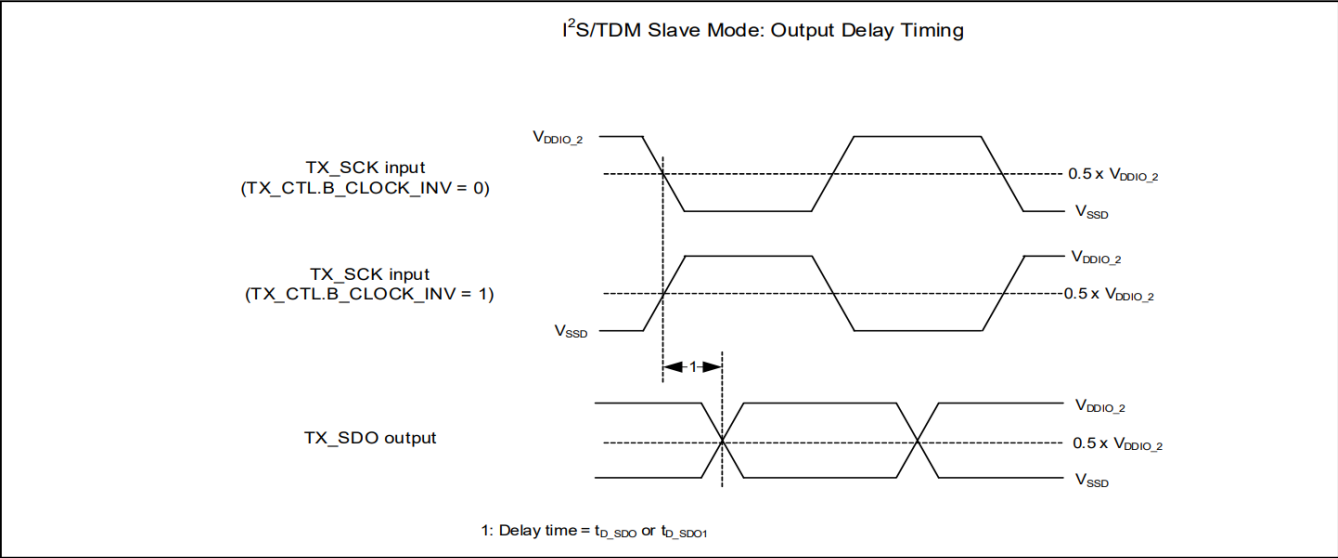


图 26-38 从机输出延时

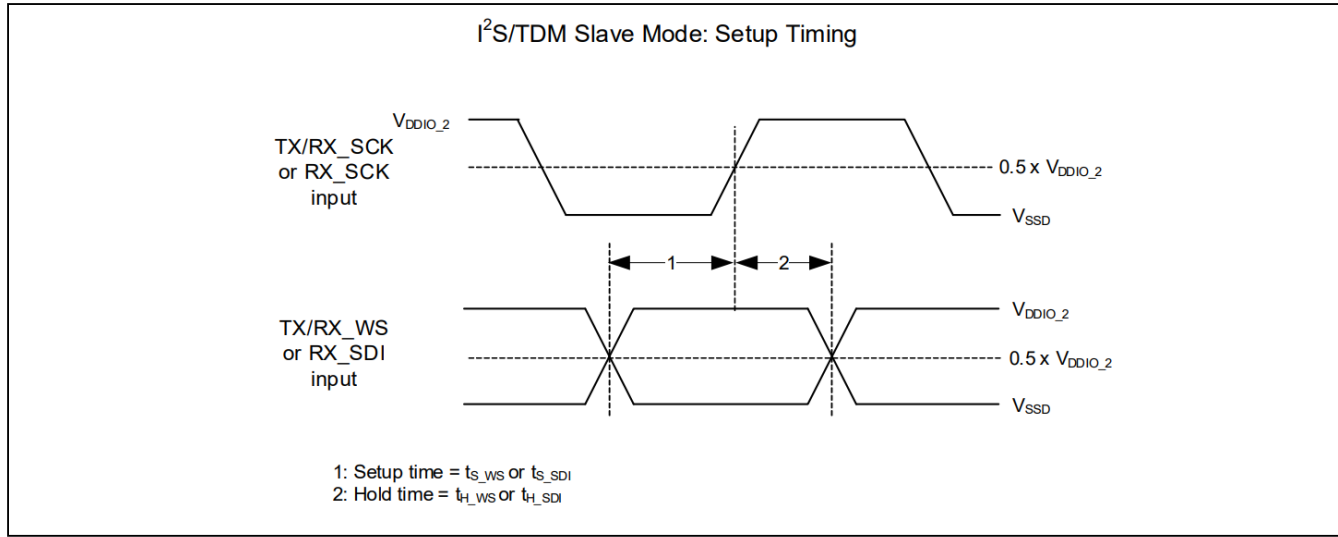


图 26-39 从机设置

电气规格

26.16 串行存储器接口规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ 和 2.7 V 至 5.5 V

表 26-36 SMIF规格 [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
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SMIF DC规格

SID785	V_{SMIF}	SMIF I/O supply voltage	2.7	–	3.6	V	For V_{DDIO_1} or V_{DDIO_3}
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HSIO_STD 的 SMIF HSSPI(SDR) 规格

SID760	$C_{\text{L_SDR_HSIO}}$	Load capacitance	–	–	30	pF	
SID761	SR_SDR_HSIO	Input rise and fall slew rates	1.5	–	–	V/ns	Guaranteed by design
SID762	$f_{\text{CK_SDR_HSIO}}$	Clock frequency	–	–	100	MHz	
SID763	$t_{\text{CK_SDR_HSIO}}$	Clock period	$1 / f_{\text{CK_SDR_HSIO}}$	–	–	ns	
SID764	DCK_SDR_HSIO	Clock duty	45	–	55	%	
SID765	CSR_SDR_HSIO	Clock rise and fall slew rates	1.5	–	–	V/ns	
SID766	$t_{\text{CS_SDR_HSIO}}$	Chip select HIGH time	10	–	–	ns	
SID767	$t_{\text{CSS_SDR_HSIO}}$	Chip select active setup time	3	–	–	ns	
SID768	$t_{\text{CSH_SDR_HSIO}}$	Chip select active hold time	5	–	–	ns	
SID769	$t_{\text{SU_SDR_HSIO}}$	Data setup time ($f_{\text{CK}} = 100 \text{ MHz}$)	1.5	–	–	ns	For other frequencies: $t_{\text{SU}} = t_{\text{SU_min}} + 0.45 \times (t_{\text{CK}} - t_{\text{CK_min}})$ $t_{\text{SU_min}} = \text{value at min of SID769}$ $t_{\text{CK_min}} = \text{value at min of SID763}$ $t_{\text{CK}} = \text{actual clock period}$
SID780	$t_{\text{HD_SDR_HSIO}}$	Data hold time ($f_{\text{CK}} = 100 \text{ MHz}$)	2	–	–	ns	For other frequencies: $t_{\text{HD}} = t_{\text{HD_min}} + 0.45 \times (t_{\text{CK}} - t_{\text{CK_min}})$ $t_{\text{HD_min}} = \text{value at min of SID780}$ $t_{\text{CK_min}} = \text{value at min of SID763}$ $t_{\text{CK}} = \text{actual clock period}$
SID781	$t_{\text{V_SDR_HSIO}}$	Clock LOW to input data valid	1.5	–	7.65	ns	
SID782	$t_{\text{HO_SDR_HSIO}}$	Input hold time	2	–	–	ns	
SID783	$t_{\text{DIS_SDR_HSIO}}$	Input disable time	0	–	7.5	ns	
SID784	$t_{\text{IO_SKEW_SDR_HSIO}}$	Data skew (first data bit to last data bit)	–	–	0.6	ns	Guaranteed by design

GPIO_STD 的 SMIF HSSPI(SDR) 规格

SID760A	$C_{\text{L_SDR_GPIO}}$	Load capacitance	–	–	30	pF	
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电气规格

表 26-36 SMIF 规格 (续) [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID761A	SR_SDR_GPIO	Input rise and fall slew rates	1	–	–	V/ns	Guaranteed by design
SID762A	f _{CK_SDR_GPIO}	Clock frequency	–	–	32	MHz	
SID763A	t _{CK_SDR_GPIO}	Clock period	$1 / f_{CK_S-DR_GPIO}$	–	–	ns	
SID764A	DCK_SDR_GPIO	Clock duty	45	–	55	%	
SID765A	CSR_SDR_GPIO	Clock rise and fall slew rates	1	–	–	V/ns	
SID766A	t _{CS_SDR_GPIO}	Chip select HIGH time	30	–	–	ns	
SID767A	t _{CSS_SDR_GPIO}	Chip select active setup time	9	–	–	ns	
SID768A	t _{CSH_SDR_GPIO}	Chip select active hold time	15	–	–	ns	
SID769A	t _{SU_SDR_GPIO}	Data setup time	4.5	–	–	ns	
SID780A	t _{HD_SDR_GPIO}	Data hold time	6	–	–	ns	
SID781A	t _{V_SDR_GPIO}	Clock LOW to input data valid	4.5	–	9	ns	
SID782A	t _{HO_SDR_GPIO}	Input hold time	2	–	–	ns	
SID783A	t _{DIS_SDR_GPIO}	Input disable time	0	–	22.5	ns	
SID784A	t _{IO_SKEW_S-DR_GPIO}	Data skew (first data bit to last data bit)	–	–	1.8	ns	Guaranteed by design

HSIO_STD 的 SMIF HSSPI(DDR) 规格

SID760B	C _{L_DDR_HSIO}	Load capacitance	–	–	15	pF	
SID761B	SR_DDR_HSIO	Input rise and fall slew rates	1.5	–	–	V/ns	Guaranteed by design
SID762B2	f _{CK_DDR_HSIO}	Clock frequency	–	–	90	MHz	
SID763B	t _{CK_DDR_HSIO}	Clock period	$1 / f_{CK_D-DR_HSIO}$	–	–	ns	
SID764B	DCK_D-DR_HSIO	Clock duty	45	–	55	%	
SID765B	CSR_DDR_HSIO	Clock rise and fall slew rates	1.5	–	–	V/ns	
SID766B	t _{CS_DDR_HSIO}	Chip select HIGH time	10	–	–	ns	
SID767B	t _{CSS_DDR_HSIO}	Chip select active setup time	4	–	–	ns	
SID768B	t _{CSH_DDR_HSIO}	Chip select active hold time	4	–	–	ns	
SID769B	t _{SU_DDR_HSIO}	Data setup time (f _{CK} = 90 MHz)	2	–	–	ns	For other frequencies: t _{SU} = t _{SU_min} + 0.225 × (t _{CK} - t _{CK_min}) t _{SU_min} = value at min of SID769B t _{CK_min} = value at min of SID763B t _{CK} = actual clock period

电气规格
表 26-36 SMIF 规格 (续) [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID780B	t _{HD_DDR_HSIO}	Data hold time (f _{CK} = 90 MHz)	1.2	–	–	ns	For other frequencies: $t_{HD} = t_{HD_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t _{HD_min} = value at min of SID780B t _{CK_min} = value at min of SID763B t _{CK} = actual clock period
SID781B	t _{V_DDR_HSIO}	Clock LOW to input data valid	0	–	6.5	ns	
SID782B	t _{HO_DDR_HSIO}	Input hold time	1	–	–	ns	
SID783B	t _{DIS_DDR_HSIO}	Input disable time	–	–	7.5	ns	
SID784B	t _{IO_SKEW_D-DR_HSIO}	Data skew (first data bit to last data bit)	–	–	0.6	ns	Guaranteed by design

GPIO_STD 的 SMIF HSSPI(DDR) 规格

SID760C	C _{L_DDR_GPIO}	Load capacitance	–	–	15	pF	
SID761C	SR _{DDR_GPIO}	Input rise and fall slew rates	1	–	–	V/ns	Guaranteed by design
SID762C	f _{CK_DDR_GPIO}	Clock frequency	–	–	32	MHz	
SID763C	t _{CK_DDR_GPIO}	Clock period	1 / f _{CK_D-DR_GPIO}	–	–	ns	
SID764C	DCK _{D-DR_GPIO}	Clock duty	45	–	55	%	
SID765C	CSR _{DDR_GPIO}	Clock rise and fall slew rates	1	–	–	V/ns	
SID766C	t _{CS_DDR_GPIO}	Chip select HIGH time	30	–	–	ns	
SID767C	t _{CSS_DDR_GPIO}	Chip select active setup time	5	–	–	ns	
SID768C	t _{CSH_DDR_GPIO}	Chip select active hold time	4	–	–	ns	
SID769C	t _{SU_DDR_GPIO}	Data setup time	5	–	–	ns	
SID780C	t _{HD_DDR_GPIO}	Data hold time	4.5	–	–	ns	
SID781C	t _{V_DDR_GPIO}	Clock LOW to input data valid	0	–	9	ns	
SID782C	t _{HO_DDR_GPIO}	Input hold time	3	–	–	ns	
SID783C	t _{DIS_DDR_GPIO}	Input disable time	–	–	22.5	ns	
SID784C	t _{IO_SKEW_D-DR_GPIO}	Data skew (first data bit to last data bit)	–	–	1.8	ns	Guaranteed by design

HSIO_STD 的 SMIF HYPERBUS™ 规格

SID785	C _{L_HB_HSIO}	Load capacitance	–	–	20	pF	
SID786	SRI _{HB_HSIO}	Input rise and fall slew rates	1	–	–	V/ns	For all signals, Guaranteed by design
SID787	SRO _{HB_HSIO}	Output rise and fall slew rates	1	–	–	V/ns	For all signals

时钟特性

SID700	f _{CK_HB_HSIO}	Clock frequency	–	–	100	MHz	
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电气规格

表 26-36 SMIF 规格 (续) [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID701	t _{CK_HB_HSIO}	Clock period	1 / f _{CK_H-B_HSIO}	-	-	ns	
SID702	DCK _{_HB_HSIO}	Clock duty	45	-	55	%	

交流参数

SID706	t _{CSHI_HB_HSIO}	Chip select HIGH between transactions	10	-	-	ns	Guaranteed by design
SID708	t _{CSS_HB_HSIO}	Chip select setup to next CK rising edge	3	-	-	ns	
SID709	t _{DSV_HB_HSIO}	Data strobe valid	-	-	12	ns	
SID710	t _{OSU_HB_HSIO}	DQ output setup	1	-	-	ns	
SID711	t _{OH_HB_HSIO}	DQ output hold	1	-	-	ns	
SID715	t _{CKD_HB_HSIO}	CK transition to DQ valid	1	-	5.5	ns	
SID718	t _{CKDS_HB_HSI O}	CK transition to RWDS valid	1	-	5.5	ns	
SID719	t _{DSS_HB_HSIO}	RWDS transition to input DQ valid	-0.8	-	0.8	ns	
SID720	t _{DSH_HB_HSIO}	Input DQ invalid to RWDS transition	-0.8	-	0.8	ns	
SID721	t _{CSH_HB_HSIO}	Chip select hold after CK falling edge	0	-	-	ns	

GPIO_STD 的SMIF HYPERBUS™规格

SID785A	C _{L_HB_GPIO}	Load capacitance	-	-	20	pF	
SID786A	SRI _{_HB_GPIO}	Input rise and fall slew rates	0.45	-	-	V/ns	For all signals, guaranteed by design
SID787A	SRO _{_HB_GPIO}	Output rise and fall slew rates	0.45	-	-	V/ns	For all signals

时钟特性

SID700A	f _{CK_HB_GPIO}	Clock frequency	-	-	32	MHz	
SID701A	t _{CK_HB_GPIO}	Clock period	1 / f _{CK_H-B_GPIO}	-	-	ns	
SID702A	DCK _{_HB_GPIO}	Clock duty	45	-	55	%	

交流参数

SID706A	t _{CSHI_HB_GPIO}	Chip select HIGH between transactions	30	-	-	ns	Guaranteed by design
SID708A	t _{CSS_HB_GPIO}	Chip select setup to next CK rising edge	9	-	-	ns	
SID709A	t _{DSV_HB_GPIO}	Data strobe valid	-	-	36	ns	Guaranteed by design
SID710A	t _{OSU_HB_GPIO}	DQ output setup	3	-	-	ns	
SID711A	t _{OH_HB_GPIO}	DQ output hold	3	-	-	ns	
SID715A	t _{CKD_HB_GPIO}	CK transition to DQ valid	3	-	16.5	ns	
SID718A	t _{CKDS_HB_GPIO}	CK transition to RWDS valid	3	-	16.5	ns	

电气规格

表 26-36 SMIF 规格 (续) [条件: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID719A	$t_{DSS_HB_GPIO}$	RWDS transition to input DQ valid	-2.4	-	2.4	ns	
SID720A	$t_{DSH_HB_GPIO}$	Input DQ invalid to RWDS transition	-2.4	-	2.4	ns	
SID721A	$t_{CSH_HB_GPIO}$	Chip select hold after CK falling edge	0	-	-	ns	

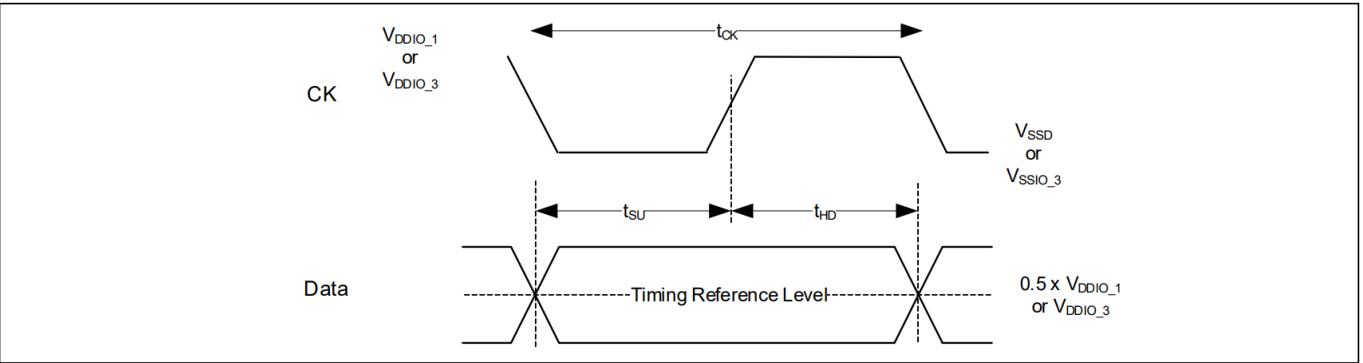


图 26-40 SDR 写入时序参考电平

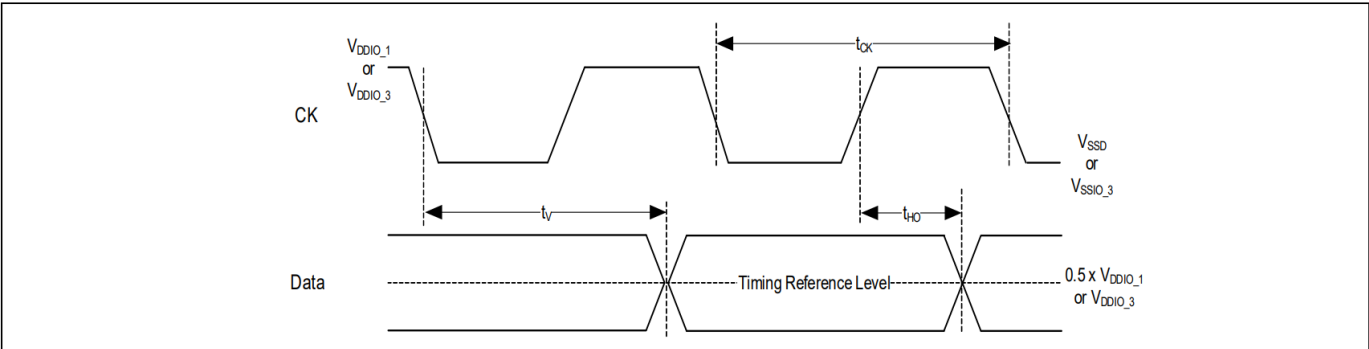
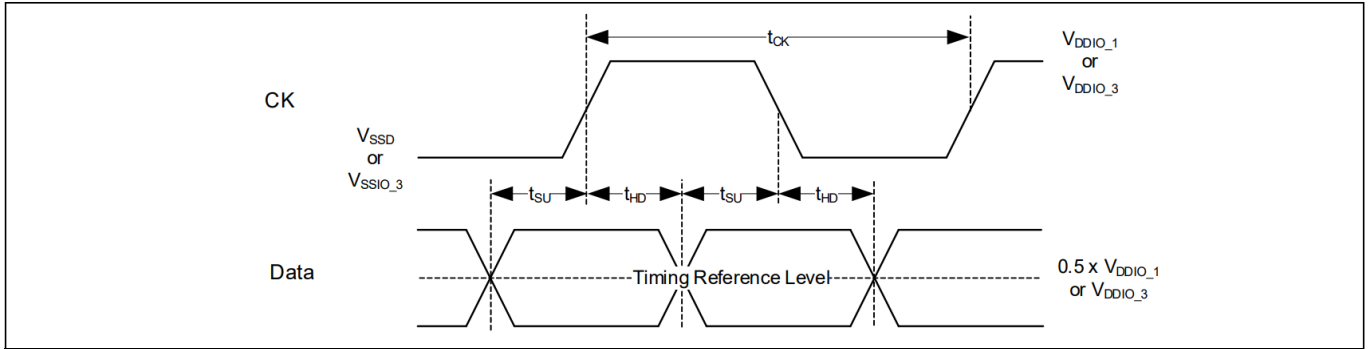


图 26-41 SDR 读取时序参考电平



电气规格

图 26-42 DDR 写入时序参考电平

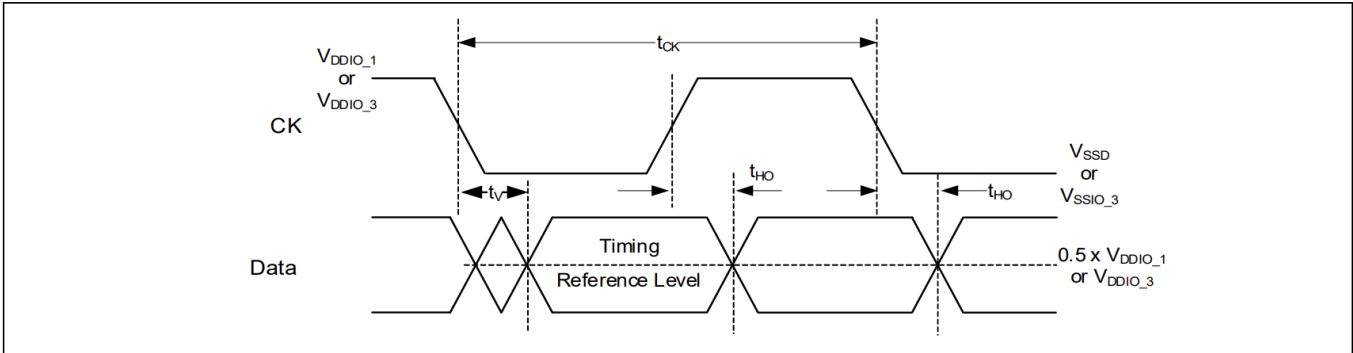


图 26-43 DDR 读取时序参考电平

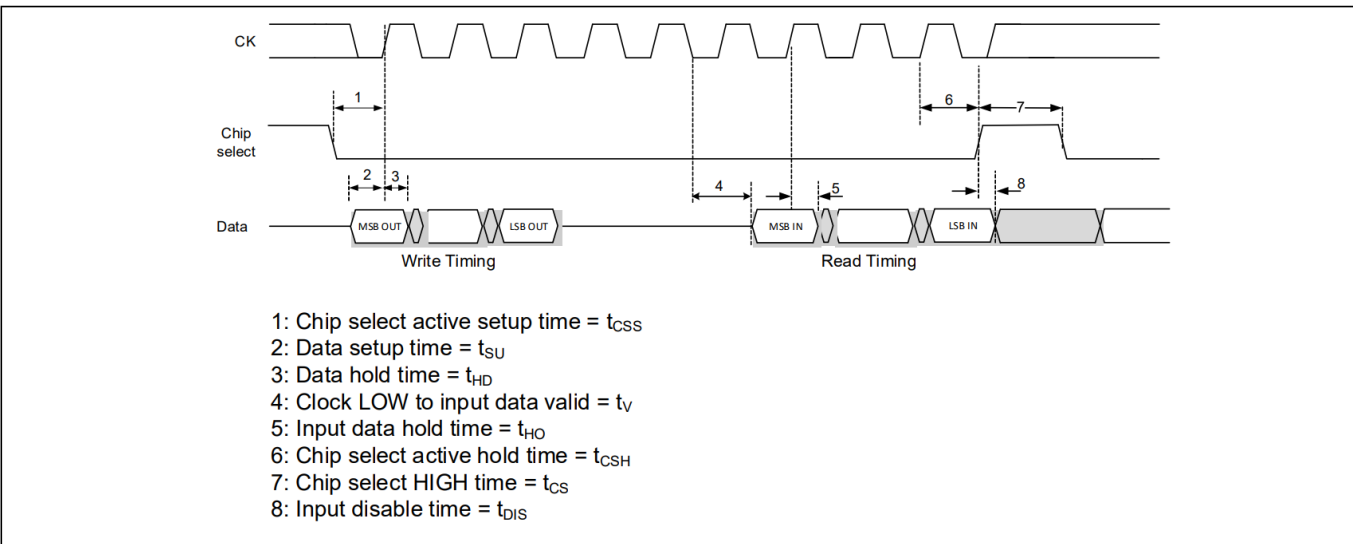


图 26 - 44 SDR写入、读取时序图

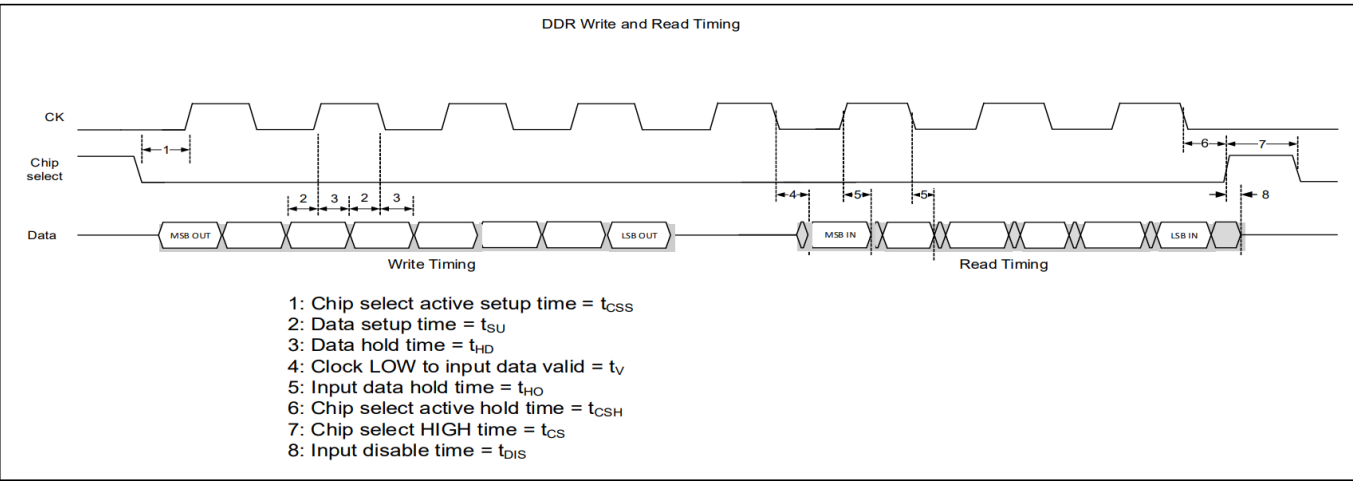


图26-45 DDR写入、读取时序图

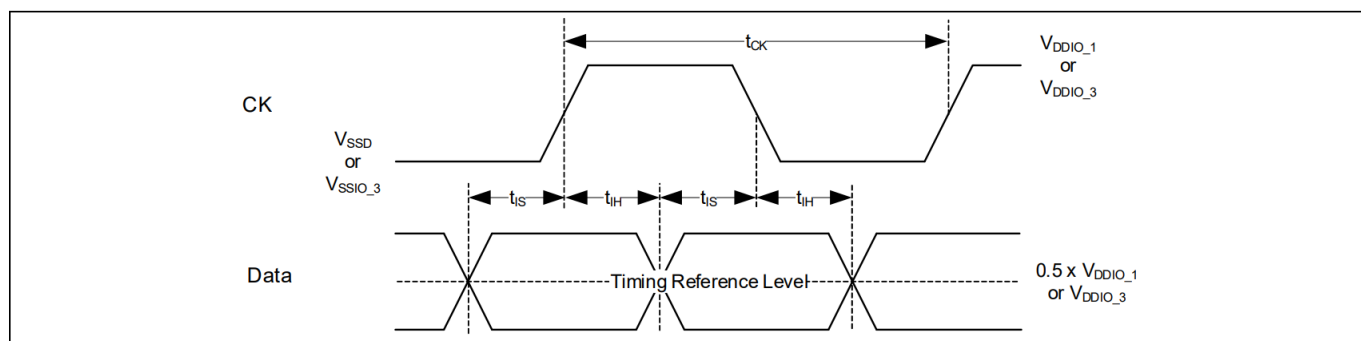


图 26-46 **HYPERBUS™时序参考电平**

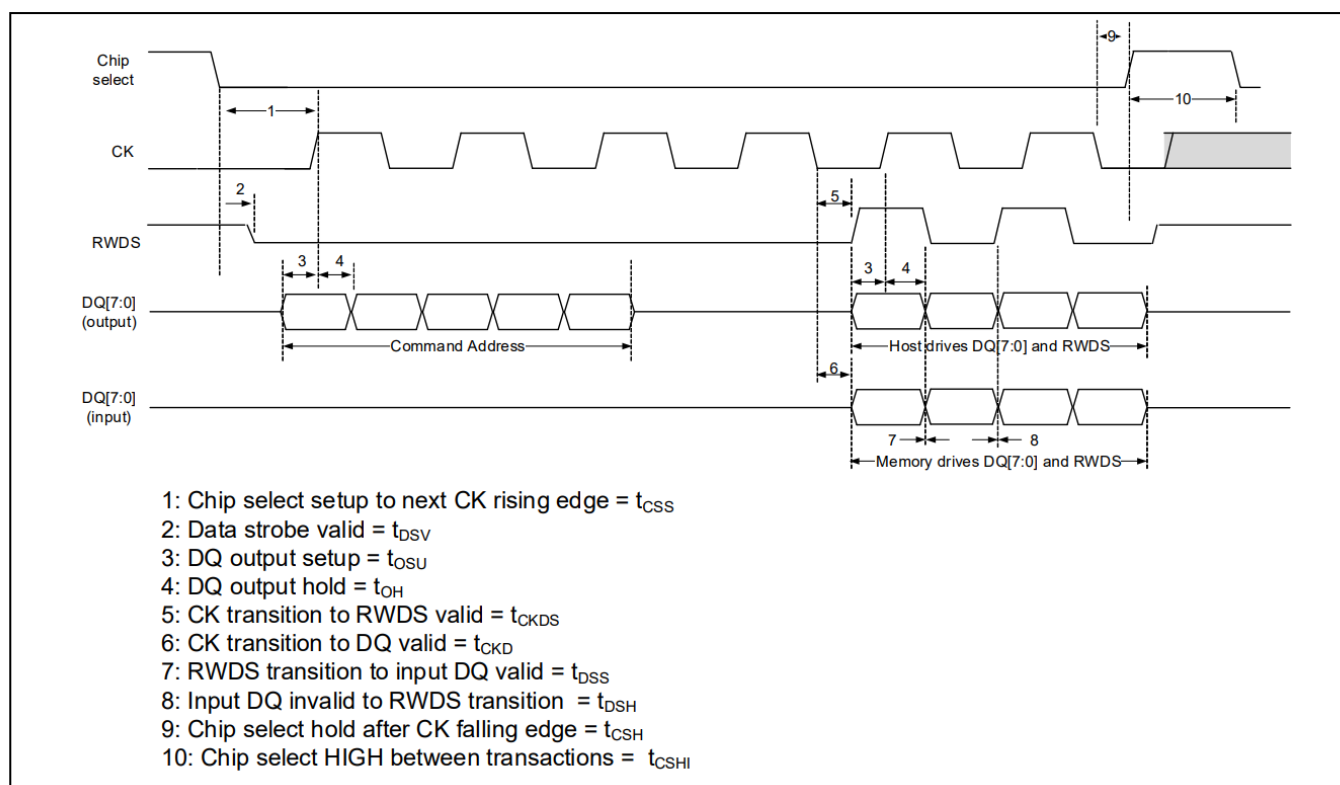


图 26-47 **HYPERBUS™时序图**



订购信息

CYT3BB/4BB 微控制器器件型号和功能列于 表27-1 中 .Arm®TAPJTAG ID 为 0x6BA0 0477。

表 27-1 CYT3BB/4BB 订购信息

Device Code	Ordering Code ^[76]	Package	CM7 Cores	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC Channel	SCB Channel	LIN Channel	I ² S Channel	Ethernet Channel	SD/eMMC	Temperature Grad	JTAG ID Code
CYT3BB5CES	CYT3BB5CEBQ1AESGS	100-TEQFP	1	4160 ^[77]	256 ^[78]	768	39	9	9	2	1	1	S ^[79]	0x1E919069 ^[82]
CYT3BB5CEE	CYT3BB5CEBQ1AEEGS	100-TEQFP	1	4160	256	768	39	9	9	2	1	1	E ^[80]	0x1E919069
CYT3BB7CES	CYT3BB7CEBQ1AESGS	144-TEQFP	1	4160	256	768	54	10	12	3	1	1	S	0x1E91A069
CYT3BB7CEE	CYT3BB7CEBQ1AEEGS	144-TEQFP	1	4160	256	768	54	10	12	3	1	1	E	0x1E91A069
CYT3BB8CES	CYT3BB8CEBQ1AESGS	176-TEQFP	1	4160	256	768	64	10	16	3	1	1	S	0x1E91B069
CYT3BB8CEE	CYT3BB8CEBQ1AEEGS	176-TEQFP	1	4160	256	768	64	10	16	3	1	1	E	0x1E91B069
CYT3BBBCES	CYT3BBBCEBQ1BZSGS	272-BGA	1	4160	256	768	72	11	16	3	1	1	S	0x1E91C069
CYT3BBBCEE	CYT3BBBCEBQ1BZEGS	272-BGA	1	4160	256	768	72	11	16	3	1	1	E	0x1E91C069
CYT4BB5CES	CYT4BB5CEBQ1AESGS	100-TEQFP	2	4160	256	768	39	9	9	2	1	1	S	0x1E91D069
CYT4BB5CEE ^[81]	CYT4BB5CEBQ1AEEGS	100-TEQFP	2	4160	256	768	39	9	9	2	1	1	E	0x1E91D069
CYT4BB7CES	CYT4BB7CEBQ1AESGS	144-TEQFP	2	4160	256	768	54	10	12	3	1	1	S	0x1E91E069
CYT4BB7CEE ^[81]	CYT4BB7CEBQ1AEEGS	144-TEQFP	2	4160	256	768	54	10	12	3	1	1	E	0x1E91E069
CYT4BB8CES	CYT4BB8CEBQ1AESGS	176-TEQFP	2	4160	256	768	64	10	16	3	1	1	S	0x1E91F069
CYT4BB8CEE ^[81]	CYT4BB8CEBQ1AEEGS	176-TEQFP	2	4160	256	768	64	10	16	3	1	1	E	0x1E91F069
CYT4BBBCES	CYT4BBBCEBQ1BZSGS	272-BGA	2	4160	256	768	72	11	16	3	1	1	S	0x1E920069
CYT4BBBCEE ^[81]	CYT4BBBCEBQ1BZEGS	272-BGA	2	4160	256	768	72	11	16	3	1	1	E	0x1E920069

注：

76. 支持的装运类型为“托盘”（默认）和“卷带包装”。在末尾添加字符'T'，获取“卷带包装”装运类型的订购代码。

77. 代码闪存大小 4160 KB = 32 KB × 126 (大扇区) + 8 KB × 16 (小扇区)。

78. 工作闪存大小 256 KB = 2 KB × 96 (大扇区) + 128 B × 512 (小扇区)。

79. .S级温度（-40°C至105°C）。

80. E 级温度（-40°C 至 125°C）。

81. 这些器件为工程样品。

82. JTAG ID CODE 位 12 至 27 代表器件的晶元 ID。



订购信息

27.1 料号命名法

表 27-2 器件代码命名规则

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family Name	3	TRAVEO™ T2G (Core M7 Single)
		4	TRAVEO™ T2G (Core M7 dual)
B	Application	B	Body
D	Code-flash/Work-flash/SRAM quantity	B	4160 KB / 256 KB / 768 KB
P	Packages	B	272-BGA
		8	176-TEQFP
		7	144-TEQFP
		5	100-TEQFP
H	Hardware Option	C	eSHE – on, HSM – on, RSA-2048
I	Marketing Option	E	Ethernet - 1 ch, eMMC - on
C	Temperature Grade	S	S-grade (–40 °C to 105 °C)
		E	E-grade (–40 °C to 125 °C)



订购信息

表 27-3 订购代码命名规则

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family Name	3	TRAVEO™ T2G (Core M7 Single)
		4	TRAVEO™ T2G (Core M7 dual)
B	Application	B	Body
D	Code-flash/Work-flash/SRAM quantity	B	4160 KB / 256 KB / 768 KB
P	Packages	B	272-BGA
		8	176-TEQFP
		7	144-TEQFP
		5	100-TEQFP
H	Hardware Option	C	eSHE – on, HSM – on, RSA-2048
I	Marketing Option	E	Ethernet - 1 ch, eMMC - on
R	Revision	A	First revision
		B	Second revision
F	Fab Location	Q	UMC (Fab 12i) Singapore
X	Reserved	0/1	Reserved
K	Package Code	AE	TEQFP
		BZ	BGA
C	Temperature Grade	S	S-grade (–40 °C to 105 °C)
		E	E-grade (–40 °C to 125 °C)
Q	Quality Grade	ES	Engineering samples
		GS	Standard grade of automotive
S	Shipment Type	Blank	Tray shipment
		T	Tape and Reel shipment

封装

28 封装

CYT3BB/4BB 采用 表 28-1 中列出的封装。

表 28-1 封装信息

Package	Dimensions ^[83]	Contact/Lead pitch	Coefficient of thermal expansion ^[88]	I/O pins
272-BGA	16 × 16 × 1.70 mm (max)	0.8-mm	a1 ^[84] = 6 ppm/°C, a2 ^[85] = 25 ppm/°C	220
176-TEQFP	24 × 24 × 1.60 mm (max)	0.5-mm	a1 = 9.5 ppm/°C, a2 = 37 ppm/°C	148
144-TEQFP	20 × 20 × 1.60 mm (max)	0.5-mm	a1 = 9.5 ppm/°C, a2 = 36.7 ppm/°C	116
100-TEQFP	14 × 14 × 1.60 mm (max)	0.5-mm	a1 = 9.4 ppm/°C, a2 = 36 ppm/°C	72

表 28-2 封装特性

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature	S-grade	-40	-	105	°C
T _A	Operating ambient temperature	E-grade	-40	-	125	°C
T _J	Operating junction temperature	-	-	-	150	°C
R _{θJA}	Package thermal resistance, junction to ambient θ _{JA} ^[86, 87]	272-BGA	-	-	21.6	°C/W
		176-TEQFP	-	-	17.8	°C/W
		144-TEQFP	-	-	17.4	°C/W
		100-TEQFP	-	-	18.3	°C/W
R _{θJB}	Package thermal resistance, junction to board θ _{JB}	272-BGA	-	-	12.8	°C/W
		176-TEQFP	-	-	13.0	°C/W
		144-TEQFP	-	-	12.3	°C/W
		100-TEQFP	-	-	10.4	°C/W
R _{θJC}	Package thermal resistance, junction to case θ _{JC}	272-BGA	-	-	10.4	°C/W
		176-TEQFP	-	-	8.0	°C/W
		144-TEQFP	-	-	8.1	°C/W
		100-TEQFP	-	-	8.5	°C/W

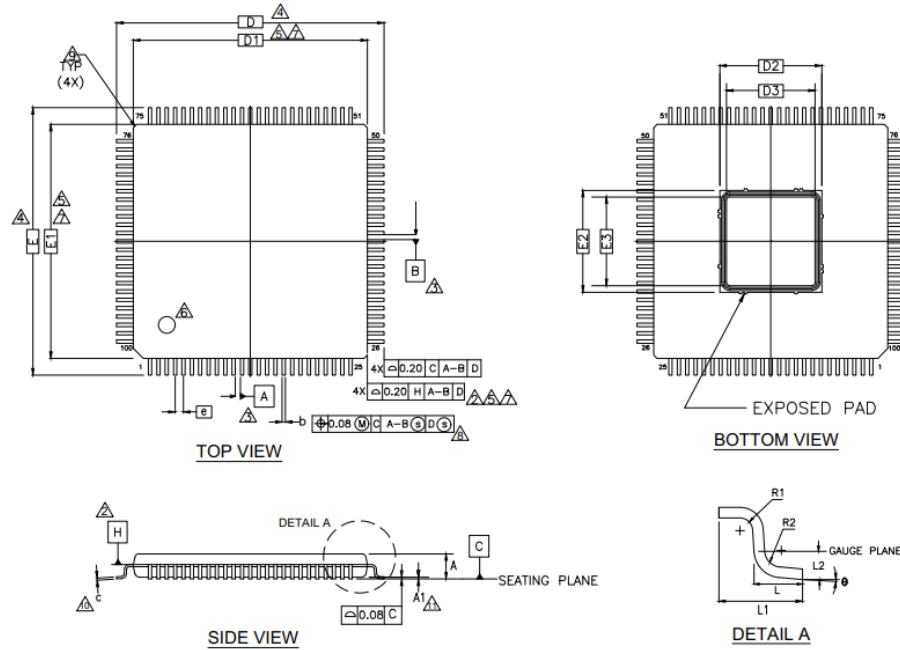
表 28-3 焊接回流温度、封装湿度敏感度水平 (MSL)、IPC / JEDEC J-STD-2

Package	Maximum peak temperature (°C)	Maximum time at peak temperature (sec- onds)	MSL
272-BGA	260	30	3
176-TEQFP	260	30	3
144-TEQFP	260	30	3
100-TEQFP	260	30	3

注:

- 83. 尺寸 (第 2 列) 适用于室温。
- 84. a1 = 低于 T_g 的 CTE (热膨胀系数) 值 (ppm/°C) (T_g 是玻璃化转变温度, 为 131°C)。
- 85. a2 = 高于 T_g 的 CTE 值 (ppm/°C)。
- 86. 所示的最大值°C/Watt 适用于 T_A = 125 °C。
- 87. 电路板条件符合 JESD51-7 (4层)。
- 88. 这些数字仅为基于仿真的估计值, 并且基于每种封装类型的单个物料清单组合。

封装



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
D	16.00 BSC		
D1	14.00 BSC		
D2	6.10 REF		
D3	5.30 REF		
E	16.00 BSC		
E1	14.00 BSC		
E2	6.10 REF		
E3	5.30 REF		
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	—	8°
c	0.09	0.127	0.20
b	0.15	—	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.50 BSC		

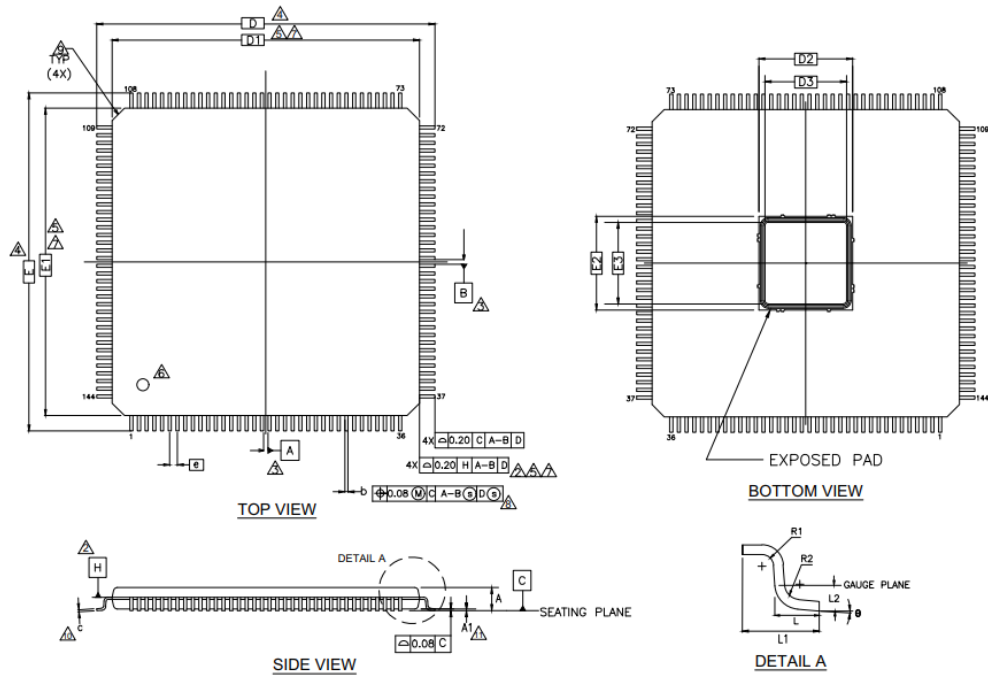
NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-28239 *B

图 28-1 封装外形 - 100-TEQFP

封装



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
D	22.00 BSC		
D1	20.00 BSC		
D2	6.10 REF		
D3	5.30 REF		
E	22.00 BSC		
E1	20.00 BSC		
E2	6.10 REF		
E3	5.30 REF		
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	—	8°
c	0.09	0.127	0.20
b	0.17	0.20	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

△ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

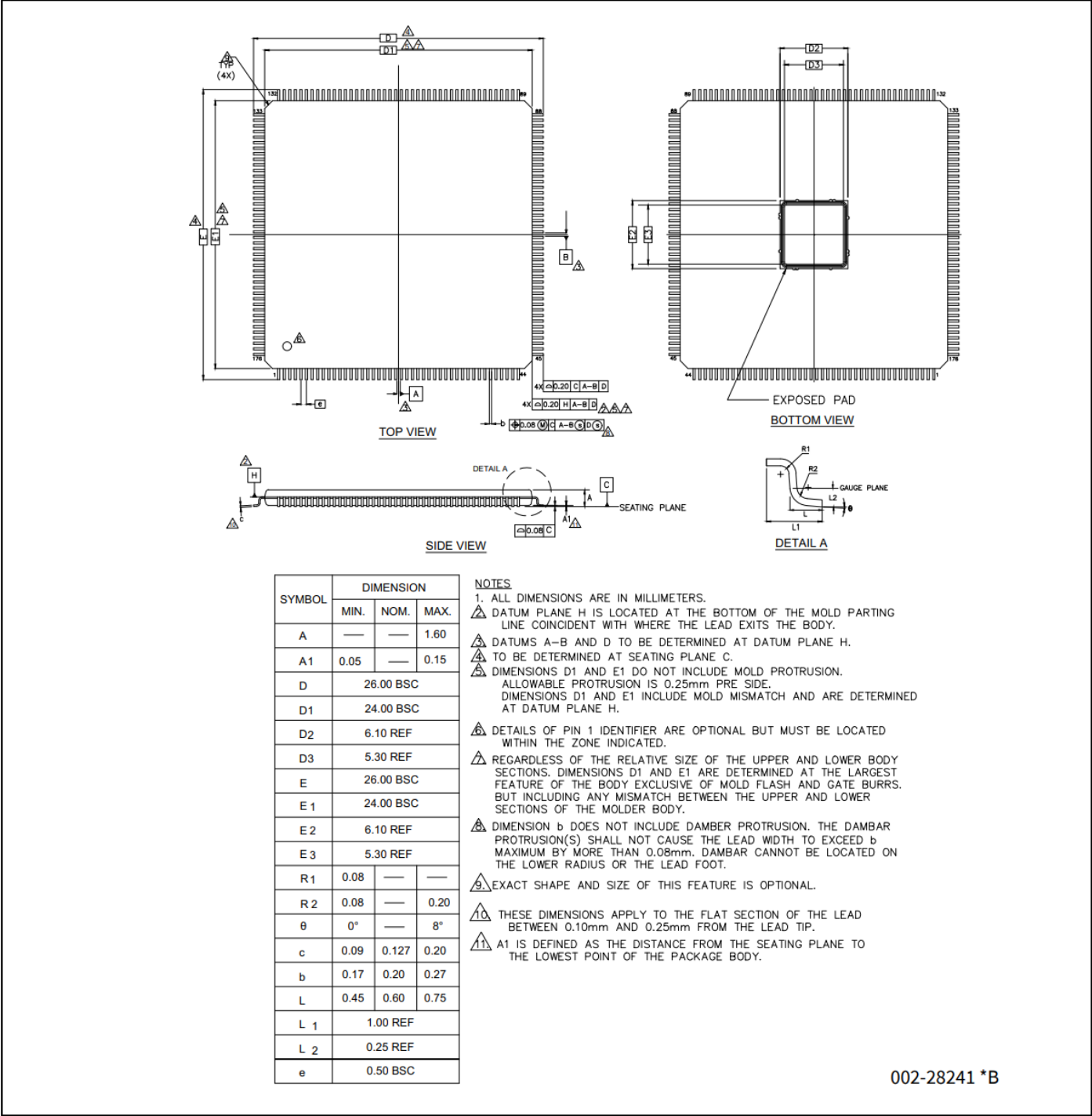
△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-28240 *B

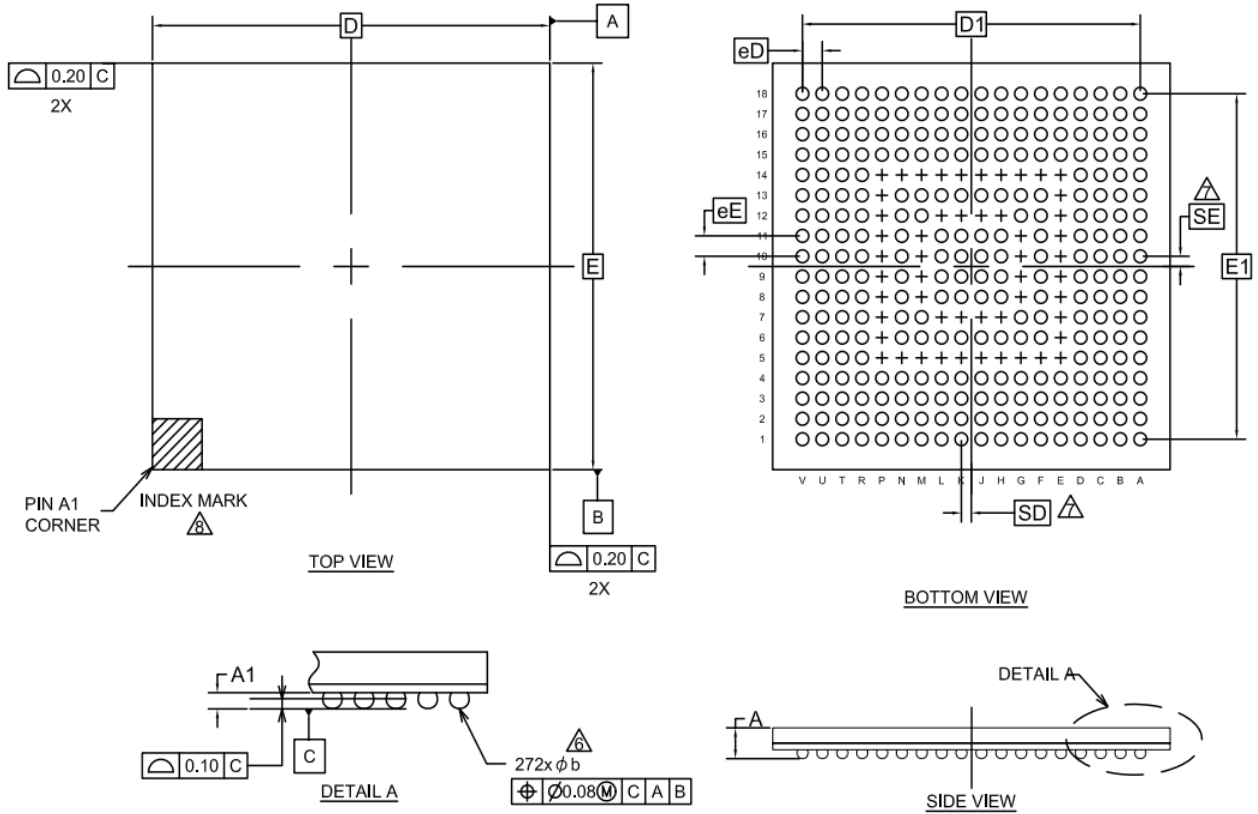
图 28-2 封装外形 - 144-TEQFP

封装



002-28241 *B

图 28-3 封装图 - 176-TEQFP



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.30	0.35	0.40
D	16.00 BSC		
E	16.00 BSC		
D1	13.60 BSC		
E1	13.60 BSC		
MD	18		
ME	18		
n	272		
Φb	0.40	0.45	0.50
eD	0.80 BSC		
eE	0.80 BSC		
SD / SE	0.40 BSC		

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-24865 *A

图 28-4 封装图 - 272-BGA

29 附录

29.1 引导加载程序或生产线末端 (EoL) 编程

- 如果应用触发条件，则在器件启动时触发
- 可以使用CAN或LIN通讯
- 引导加载程序在不同的时间帧上轮询CAN或LIN上的通讯，直到达到整体 300 秒超时
- 如果在任一通讯接口上收到引导加载程序指令，则轮询停止并且引导加载程序开始使用此接口

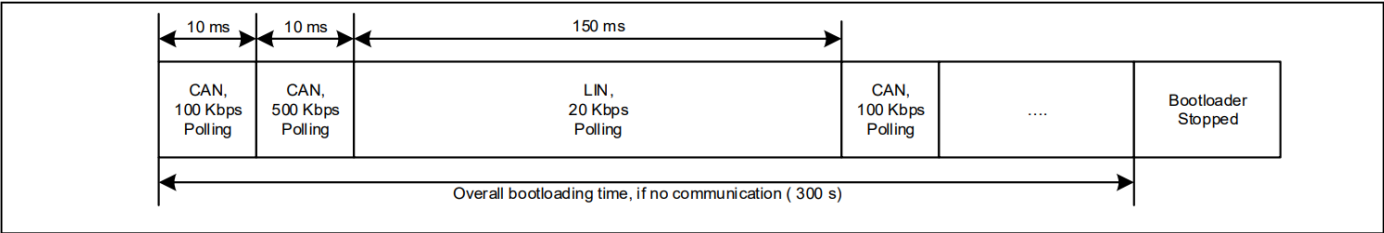


图 29-1 引导加载序列

表 29-1 CAN 接口详细信息

Sl. No.	CAN interface	Configuration
1	CAN Mode	Classic CAN
2	CAN Instance	CAN0, Channel#1
3	CAN TX	P0.2 / CAN0_1_TX
4	CAN RX	P0.3 / CAN0_1_RX
5	CAN Transceiver NSTB / EN (Low)	P23.3 (optional)
6	CAN Transceiver EN / EN (High)	P2.1 (optional)
7	CAN RX Message ID	0x1A1
8	CAN TX Message ID	0x1B1
9	Baud	100 or 500 kbps alternating

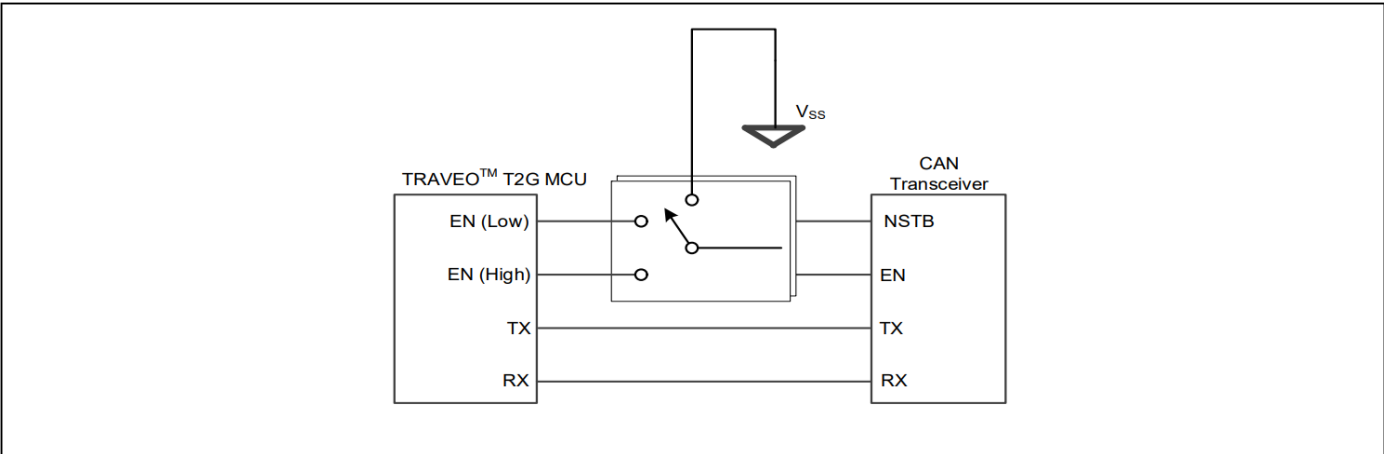


图 29-2 MCU到CAN收发器的连接

表 29-2 LIN 接口详细信息

Sl. No.	LIN Interface	Configuration
1	LIN Type	LIN0, Channel#1
2	LIN Mode	Slave
3	LIN Checksum Type	Classic
4	LIN TX	P0.1 / LIN1_TX
5	LIN RX	P0.0 / LIN1_RX
6	LIN EN / EN (High)	P2.1 (optional)
7	LIN EN (Low)	P23.3 (optional)
8	LIN TX PID	0x46
9	LIN RX PID	0x45
10	Baud	20 or 115.2 kbps
11	Break Field Length	11
12	Break Delimiter Length	1 bit

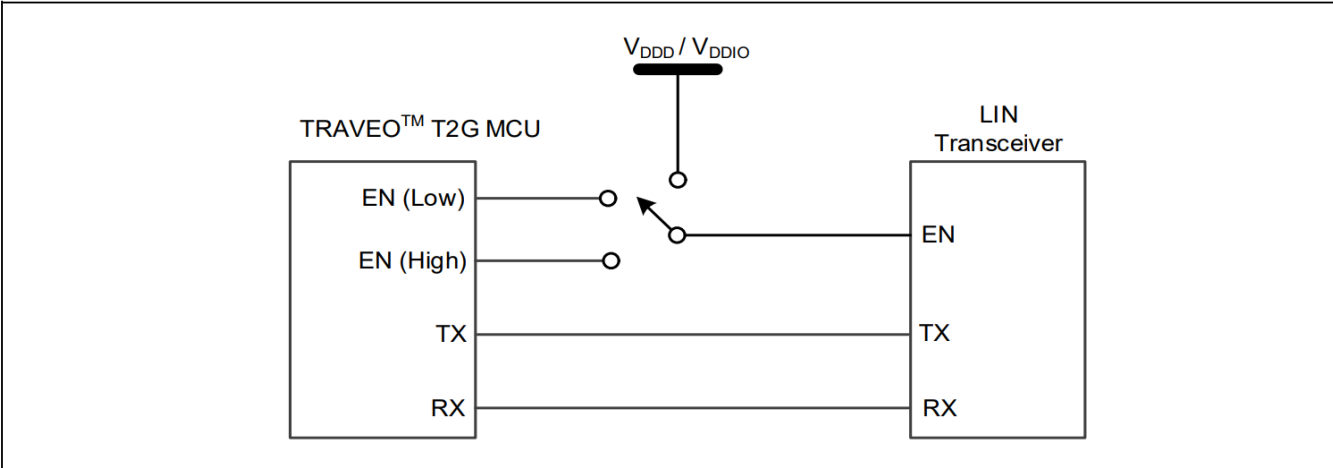


图 29-3 MCU 至 LIN 收发器连接

29.2 外部 IP 修订

表 29-3 IP 修订

Module	IP	Revision	Vendor
SDHC	mxsdhc	version 1.70a	Synopsys
CANFD	mxttcanfd	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex-M0+-r0p1	Arm®
Arm® Cortex®-M7	armcm7	Cortex-M7-r1p2	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100-r3p2	Arm®
Ethernet	mxeth	GEM_GXL r1p09	Cadence

缩略语

30 缩略语

表 30-1 本文档中使用的缩略语

Acronym	Description	Acronym	Description
A/D	Analog to Digital	PLL	Phase Locked Loop
ABS	Absolute	POR	Power-on reset
ADC	Analog to Digital converter	PPU	Peripheral protection unit
AES	Advanced encryption standard	PRNG	Pseudo-random number generator
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus	PSoC	Programmable system on chip
Arm®	Advanced RISC machine, a CPU architecture	PWM	Pulse-width modulation
ASIL	Automotive safety integrity level	MCU	Microcontroller Unit
BOD	Brown-out detection	MCWDT	Multi-counter watchdog timer
CAN FD	Controller Area Network with Flexible Data rate	M-DMA	Memory-Direct Memory Access
CMOS	Complementary metal-oxide-semiconductor	MISO	Master-in slave-out
CPU	Central Processing Unit	MMIO	Memory mapped I/O
CRC	Cyclic redundancy check, an error-checking protocol	MOSI	Master-out slave-in
CSV	Clock supervisor	MPU	Memory protection unit
CTI	Cross Trigger Interface	NVIC	Nested vectored interrupt controller
DES	Data encryption standard	RAM	Random access memory
ECC	Error correcting code	RISC	Reduced-instruction-set computing
ECO	External crystal oscillator	ROM	Read only memory
ETM	Embedded Trace Macrocell	RTC	Real-time clock
FLL	Frequency Locked Loop	SAR	Successive approximation register
FPU	Floating point unit	SCB	Serial communication block
GHS	Green hills tool chain with IDE	SCL	I²C serial clock
GPIO	General-purpose input/output	SDA	I²C serial data
HSM	Hardware security module	SHA	Secure hash algorithm
I/O	Input/output	SHE	Secure hardware extension
I²C	Inter-Integrated Circuit, a communications protocol	SMPU	Shared memory protection unit
I²S	Inter-Integrated Circuit Sound	SPI	Serial peripheral interface, a communications protocol
ILO	Internal low-speed oscillator	SRAM	Static random access memory
IMO	Internal main oscillator	SWD	Single wire debug
IPC	Inter-processor communication	TCM	Tightly Coupled Memory
IrDA	Infrared interface	TCPWM	Timer/Counter Pulse-width modulator
IRQ	Interrupt request	TTL	Transistor-transistor logic
JTAG	Joint test action group	TRNG	True random number generator



缩略语

表 30-1 本文档中使用的缩略语

Acronym	Description	Acronym	Description
LIN	Local Interconnect Network, a communications protocol	UART	Universal Asynchronous Transmitter Receiver, a communications protocol
LVD	Low voltage detection	WCO	Watch crystal oscillator
OTA	Over-the-air programming	WDT	Watchdog timer reset
OTP	One-time programmable	XIP	eXecute In Place
OVD	Overvoltage detection	XTAL	Crystal
PASS	Programmable Analog Subsystem		
P-DMA	Peripheral-Direct Memory Access		



31 勘误表

本节描述了 CYT3BB/4BB 产品系列的勘误表。 具体内容包括触发条件、影响范围、可用解决方案和芯片版本的适用性。 若有任何问题，请联系您当地英飞凌销售代表。

受影响的器件编号

器件编号
所有 CYT3BB/4BB 器件

CYT3BB/4BB 资格状态

生产样品

CYT3BB/4BB 勘误表摘要

勘误表

下表定义了 CYT3BB/4BB 系列设备的勘误表适用性。

Items	Errata ID	CYT3BB/4BB	Silicon rev.	Fix status
[1] CAN FD RX FIFO top pointer feature does not function as expected	96	CYT3BB5CEBQ0AESG S CYT3BB5CEBQ0AEEG S CYT3BB7CEBQ0AESG S CYT3BB7CEBQ0AEEG S CYT3BB8CEBQ0AESG S CYT3BB8CEBQ0AEEG S CYT3BBBCEBQ0BZSG S CYT3BBBCEBQ0BZEG S CYT4BB5CEBQ0AESG S CYT4BB5CEBQ0AEEG S CYT4BB7CEBQ0AESG S CYT4BB7CEBQ0AEEG S CYT4BB8CEBQ0AESG S CYT4BB8CEBQ0AEEG S CYT4BBBCEBQ0BZSG S CYT4BBBCEBQ0BZEG S	B	No silicon fix planned. Use workaround.
[2] CAN FD debug message handling state machine is not reset to Idle state when CANFD_CH_CCCR.INIT is set	97			No silicon fix planned. Use workaround.
[3] Limitation of the memory hole in SCB register space	124			No silicon fix planned. Use workaround.
[4] Limitation of the memory hole in Ethernet (ETH) register space	128			No silicon fix planned. Use workaround.
[5] CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID	147			No silicon fix planned. Use workaround.
[6] CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID	167			No silicon fix planned. Use workaround. TRM was updated.
[7] Misleading status is returned for Flash and eFuse system calls, if there are pending NC ECC faults in SRAM controller #0	175			No silicon fix planned. TRM was updated.
[8] WDT reset causes loss of SRAM retention	176			No silicon fix planned. TRM was updated.
[9] RMII TX output maximum delay spec change for GPIO_STD	177			No silicon fix planned.
[10] Crypto ECC errors may be set after boot with application authentication	185			No silicon fix planned. TRM was updated.
[11] Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode	198			Fixed to update the Flash settings from date code 240xxxxx.
[12] Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep	199			No silicon fix planned. TRM was updated.
[13] A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM	201			No silicon fix planned. TRM was updated.
[14] Limitation of clock configuration before entering DeepSleep mode	202			No silicon fix planned. TRM was updated.
[15] Several data retention information in the Register TRM are incorrect	203			No silicon fix planned. TRM was updated.
[16] SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally	204			No silicon fix planned. TRM was updated.
[17] Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode	206			No silicon fix planned. TRM will be updated.
[18] CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete	209			No silicon fix planned. Use workaround.
[19] Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet	212			No silicon fix planned. Datasheet will be updated.

勘误表

1. CAN FD RX FIFO top pointer feature does not function as expected	
Problem definition	RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should restart back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not restart back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA reading messages from the wrong address in Message RAM.
Parameters affected	NA
Trigger condition(s)	The RX FIFO top pointer function is used when RX FIFO n size is set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).
Scope of impact	Received message cannot be correctly read by using the RX FIFO top pointer function, when RX FIFO n size is set to 1 element.
Workaround	Any of the following can be used as a workaround: 1) Set RX FIFO n size to 2 or more when using RX FIFO top pointer function. 2) Do not use the RX FIFO top pointer function when RX FIFO n size is set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.
Fix status	No silicon fix planned. Use workaround.
2. CAN FD debug message handling state machine is not reset to Idle state when CANFD_CH_CCCR.INIT is set	
Problem definition	If either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters Bus-off state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.
Parameters affected	NA
Trigger condition(s)	Either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters Bus-off state.
Scope of impact	The errata is limited to the use case when the debug on CAN functionality is active. Normal operation of the CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the CANFD_CH_RXF1S.DMS bit. In case CANFD_CH_RXF1S.DMS is set to 0b11, the DMA request remains active. Bosch classifies this as a non-critical error with low severity, there is no fix for the IP. Bosch recommends the workaround listed here.
Workaround	In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.
Fix status	No silicon fix planned. Use workaround.
3. Limitation of the memory hole in SCB register space	
Problem definition	The memory hole [offset address: 0x1000 to 0xFFFF] inside SCB register space is not aligned to the below defined spec. The offset address bits [15:12] are ignored and treated as 4'b0000, so write/read access to offset address [0x1000 to 0xFFFF], will actually happen to [0x0000 to 0x0FFF]. - Access to address gaps in memory mapped space: writes are ignored and any read returns a zero.
Parameters affected	NA
Trigger condition(s)	Access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.
Scope of impact	The memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space is not aligned to other IP registers.
Workaround	Do not access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.
Fix status	No silicon fix planned.

勘误表

4. Limitation of the memory hole in Ethernet (ETH) register space	
Problem definition	The memory hole [offset address: 0x2000 to 0xFFFF] in ETH register space has the below mentioned original spec. However, when accessing to address gaps within [0x1000 to 0x1FFF], the offset address bits [15:13] are ignored and treated as 3'b000, so write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF]. - Access to address gaps within [0x0000 to 0x0FFF]: writes are ignored and any read returns a zero. - Access to address gaps within [0x1000 to 0x1FFF]: returns AHB ERROR.
Parameters affected	NA
Trigger condition(s)	Access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.
Scope of impact	Write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF].
Workaround	Do not access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.
Fix status	No silicon fix planned.

5. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID	
Problem definition	Configuration: Several Tx Buffers are configured with same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests. Expected behavior: When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first. Observed behavior: It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).
Parameters affected	NA
Trigger condition(s)	When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.
Scope of impact	In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).
Workaround	Any of the following: 1) First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request. 2) Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order. Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.
Fix status	No silicon fix planned. Use workaround.

勘误表

6. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID	
Problem definition	The following are the updated description in the sections "Dedicated Tx Buffers" and "Tx Queue" of the architecture TRM related to the transmission from multiple buffers configured with the same Message ID. Dedicated Tx buffers - TRM statement: If multiple Tx buffers are configured with the same Message ID, the Tx buffer with the lowest buffer number is transmitted first. - Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR. Tx queue - TRM statement: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first. - Replacement: In case that multiple Tx queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible. - TRM statement: An Add Request cyclically increments the Put Index to the next free Tx Buffer. - Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number.
Parameters affected	NA
Trigger condition(s)	Using multiple dedicated Tx buffers or Tx queue buffers configured with the same Message ID.
Scope of impact	In the case the dedicated Tx buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.
Workaround	In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.
Fix status	No silicon fix planned. Updated TRM.

7. Misleading status is returned for Flash and eFuse system calls, if there are pending NC ECC faults in SRAM controller #0	
Problem Definition	Flash and eFuse system calls will return misleading status of 0xF0000005 ("Page is write protected") even for non-protected row, or 0xF0000002 ("Invalid eFuse address") for valid eFuse address in case of pending NC ECC faults in SRAM controller #0.
Parameters Affected	Return status of Flash and eFuse system calls.
Trigger Condition(s)	NC ECC fault(s) pending in SRAM controller #0 and SWPUs are populated in the design.
Scope of Impact	Flash and eFuse system calls will not work until the NC ECC fault(s) pending in SRAM controller #0 is/are properly handled.
Workaround	If the NC ECC fault(s) are not due to HW malfunction (i.e. if the faults are due to usage of non-initialized SRAM or improper SRAM initialization), then clearing of these pending faults will resolve the issue.
Fix Status	No silicon fix planned. Updated TRM.

勘误表

8. WDT reset causes loss of SRAM retention	
Problem Definition	Architecture TRM Table on “Reset Cause Distribution” shows that, the WDT reset can retain SRAM if there is an orderly shutdown of the SRAM only during a warning interrupt. However, this is wrong. WDT reset causes loss of SRAM retention.
Parameters Affected	NA
Trigger Condition(s)	WDT reset
Scope of Impact	WDT reset causes loss of SRAM retention.
Workaround	None
Fix Status	No silicon fix planned. TRM was updated.

9. RMII TX output maximum delay spec change for GPIO_STD	
Problem Definition	RMII TX output maximum delay specification has been changed from 14 ns to 14.6 ns for GPIO_STD.
Parameters Affected	SID393
Trigger Condition(s)	Using GPIO_STD as RMII
Scope of Impact	This spec change will cause that the PCB delay budget between MCU and PHY cut down to 1.4 ns from 2 ns. [PCB delay budget = REF_CLK period (e.g. 20 ns) – SID393 (14.6 ns) – PHY RXD setup (e.g. 4 ns)]
Workaround	None
Fix Status	No silicon fix planned.

10. Crypto ECC errors may be set after boot with application authentication	
Problem Definition	Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication. In spite of the Crypto ECC errors, the result of the authentication is reliable.
Parameters Affected	N/A
Trigger Condition(s)	Boot device with application authentication.
Scope of Impact	Crypto ECC errors may be set after boot with application authentication.
Workaround	Clear or ignore Crypto ECC errors which were generated during boot with application authentication.
Fix Status	No silicon fix planned. Updated TRM.

11. Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode	
Problem Definition	Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allows users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue; Work Flash and Supervisory Flash (SFlash) are not impacted.
Parameters Affected	N/A
Trigger Condition(s)	Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.
Scope of Impact	When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.

勘误表

Workaround	Use any of the following: 1) User can use Non-Blocking mode for EraseSector, but must not interrupt the erase operation using Erase Suspend / Erase Resume. 2) If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector.
Fix Status	Fixed to update the Flash settings from date code 240xxxxx.

12. Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep

Problem Definition	The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.
Parameters Affected	N/A
Trigger Condition(s)	The port selects peripherals (except for LIN or CAN-FD), and MCU wakes up from DeepSleep.
Scope of Impact	Unexpected port output change might affect user system.
Workaround	If the port selects peripherals (except for LIN or CAN FD), and the port output value needed to be maintained after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx- _PORT_SEL.IOy_SEL back to the peripheral module as needed.
Fix Status	No silicon fix planned. TRM was updated.

13. A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM

Problem Definition	The following is missing from the PWR_CTL2.BGREF_LPMODE description in the existing register TRM. This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE = 1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.
Parameters Affected	N/A
Trigger Condition(s)	Using the PWR_CTL2.BGREF_LPMODE
Scope of Impact	PWR_CTL2.BGREF_LPMODE may not be set or cleared.
Workaround	Use the PWR_CTL2.BGREF_LPMODE according to the following description. This register will not set unless CLK_ILO0 - CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.
Fix Status	No silicon fix planned. TRM was updated.

14. Limitation of clock configuration before entering DeepSleep mode

Problem Definition	DeepSleep should not be entered while any FLL/PLL is enabled and uses ECO as its reference clock. Since the unstable ECO clock after wakeup is outside the allowed reference clock limits for FLL/PLL, there is possibility of failing the DeepSleep wakeup.
Parameters Affected	N/A
Trigger Condition(s)	DeepSleep transition while any FLL/PLL is enabled and using ECO as its reference clock.
Scope of Impact	There is a possibility of DeepSleep wakeup failing.
Workaround	If any FLL/PLL is operating with the ECO as its reference clock, change the clock to either ECO direct or IMO direct or IMO with FLL/PLL before entering DeepSleep.
Fix Status	No silicon fix planned. TRM was updated.

勘误表

15. Several data retention information in the Register TRM are incorrect

Problem Definition	The following registers are described as 'Retained' in the Register TRM while it is not guaranteed that the value before entering DeepSleep mode is still readable from the register: - SARADC: PASSx_SARy_CHz_RESULT - SRSS: PWR_LVD_STATUS - SRSS: PWR_LVD_STATUS2 - SRSS: CLK_CAL_CNT1 - SRSS: CLK_CAL_CNT2 - SRSS: CLK_FLL_STATUS - SRSS: WDT_INTR - SRSS: WDT_INTR_MASKED - SRSS: CLK_PLL400Mx_STATUS"
Parameters Affected	N/A
Trigger Condition(s)	Use of the related function and wakeup from DeepSleep mode.
Scope of Impact	The values before entering DeepSleep are not retained.
Workaround	For PASSx_SARy_CHz_RESULT, any of following can be used as a workaround: 1) Store the conversion values at another memory location before entering DeepSleep mode 2) Restart the conversion after wakeup from DeepSleep mode For the other registers: Rewrite the register value or read the status flags again after wakeup.
Fix Status	No silicon fix planned. TRM was updated.

16. SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally

Problem Definition	There is a possibility of setting the SCBx_INTR_TX.UNDERFLOW bit even if the FIFO is not empty.
Parameters Affected	N/A
Trigger Condition(s)	Using the TX FIFO for SCB when the AHB-Lite interface clock (CLK_GR6) frequency of the AHB bus is greater than 3x the SCB functionality clock (PCLK_SCBx_CLOCK).
Scope of Impact	SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally.
Workaround	Ignore the SCBx_INTR_TX.UNDERFLOW bit if the FIFO is not empty.
Fix Status	No silicon fix planned. TRM was updated.

勘误表

17. Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode	
Problem Definition	The following SROM APIs read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that, the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault occurrence based on the FLASHC_FLASH_CTL register settings. Affected SROM APIs: - ReadSWPU - WriteSWPU - GenerateHash - Checksum* - ComputeBasicHash* - CheckFactoryHash - ProgramWorkFlash** - SwitchOverRegulators - LoadRegulatorsTrims *: Do not call it to calculate on the bank where programming/erasing is in progress. **: Do not use it during non-blocking operation.
Parameters Affected	N/A
Trigger Condition(s)	Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Scope of Impact	The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Workaround	Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Fix Status	No silicon fix planned. TRM will be updated.
Impact on Infineon software	Impact: Limitation Related modules: S-LLD, HSM-Perf-Lib Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty.

18. CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Problem Definition

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).
The time needed for acceptance filtering and for storing of a received message depends on

- The Host clock frequency
- The worst-case latency of the read and write accesses to the external Message RAM
- The number of configured filter elements
- The workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).

	31	24												23	16												15	8								7	0							
R0	ESI	XTD	RTR	ID[28:0]																																								
R1A	ANMF	FIDX[6:0]												res	FDF	BRS	DLC[3:0]	RXTS[15:0]																										
R1B	ANMF	FIDX[6:0]												res	FDF	BRS	DLC[3:0]	res												TSC	RXTSP [3:0]													
R2	DB3[7:0]												DB2[7:0]												DB1[7:0]												DB0[7:0]							
R3	DB7[7:0]												DB6[7:0]												DB5[7:0]												DB4[7:0]							
...	...												...												...												...							
Rn	DBm[7:0]												DBm-1[7:0]												DBm-2[7:0]												DBm-3[7:0]							

Figure 1 Rx Buffer and FIFO Element

Under the following conditions, a received message has corrupted data while the received message is signaled as valid to the host.

- 1) The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
- 2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5).
- 3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:

- Rx FIFO: FIFO put index RXFnS.FnPI is updated.
- Dedicated Rx Buffer: New Data flag NDATn.NDxx is set.
- Interrupt flag IR.MRAF is not set.

The issue may occur in the FD Frame Format as well as in the Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

IFS ARB CTRL DATA CRC ACK EOF ESC

Arbitration Bit Rate Data Bit Rate Arbitration Bit Rate

cached data words

max. time for acceptance filtering and storage of R2 (DB3..DB0)

Original available time for acceptance filtering and storage of R2 (DB3..DB0)

Figure 2 CAN Frame with DLC > 4

勘误表

18. CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete
Table 1 TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs / 29-bit IDs 1,2	Number of active CAN channels in an instance	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32 / 16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
	4	6.9 MHz	12.7 MHz	23.5 MHz	40.8 MHz	13.8 MHz	25.3 MHz	46.9 MHz	56.5 MHz
64 / 32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz
	4	13.2 MHz	24.2 MHz	44.8 MHz	78.0 MHz	26.3 MHz	48.4 MHz	89.5 MHz	107.9 MHz ³
96 / 48	2	10.8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz	30.2 MHz	55.6 MHz	102.9 MHz ³	124.0 MHz ³
	4	19.4 MHz	35.7 MHz	66.1 MHz	115.1 MHz ³	38.8 MHz	71.4 MHz	132.2 MHz ³	159.3 MHz ³
128 / 64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz	28.4 MHz	52.5 MHz	97.2 MHz	117.2 MHz ³
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz ³	40.0 MHz	73.5 MHz	136.0 MHz ³	164.0 MHz ³
	4	25.7 MHz	47.2 MHz	87.5 MHz	152.3 MHz ³	51.4 MHz	94.4 MHz	174.9 MHz ³	210.8 MHz ³

1. M_TTCAN always starts at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.

2. Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element runs separately; only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.

3. Frequency is not reachable since the maximum host clock frequency for M_TTCAN in TRAVEO™ T2G is 100 MHz.

Parameters Affected	N/A
Trigger Condition(s)	Under the following conditions a received message has corrupted data while the received message is signaled as valid to the host: 1) The data length code (DLC) of the received message is greater than 4 (DLC > 4) 2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5). 3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.
Scope of Impact	The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in Table 1 . Corrupted data is written to the Rx FIFO element from the respective dedicated Rx Buffer. The received frame is nevertheless signaled as valid.

勘误表

18. CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Workaround	Check whether the minimum Host clock frequency (shown in Table 1) is below the Host clock frequency used in the actual device. If yes, there is no problem with the selected configuration. If no, use one of the following two workarounds. 1) Try a different configuration by changing the following parameters until the actual Host clock frequency (CLK_GR5) is above the minimum host frequency shown in Table 1: • Increase the CLK_GR5 frequency in the actual device • Reduce the CAN-FD data bit rate • Reduce the number of configured filter elements • Reduce the number of active CAN channels in an instance Also, use DLC ≥ 8 instead of DLCs 5, 6, and 7 in the CAN environment/system, as they place higher demands on the minimum Host clock frequency (the worst case is DLC = 5) or restrict your CAN environment/system to DLC 4. Note: While changing the actual host clock frequency, CLK_GR5 must always be equal to or higher than PCLK_CANFD[x]_CLOCK_CAN[y] for all configurations. 2) Due to condition 3) listed in “Trigger Conditions”, the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in the received frames.
Fix Status	No silicon fix planned. Use workaround.
Impact on Infineon software	Impact: Limitation Related modules: CAN, MCU Comment: The user must evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value. 1) For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time. 2) For the host clock frequency: In McuPeriGroupSettings, locate the setting with McuPeriGroup = MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency. 4) For the number of configured active filter element 11-bit IDs / 29-bit IDs: Use the corresponding values from the "Message RAM (...) linking table" in the generated <i>Can_PBcfg.h</i> file. Note that each CanController has its separate table. Take the maximum values. 5) For the arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers. 6) For the data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

19. Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet

Problem Definition	The existing datasheet shows the incorrect TCPWM input trigger selection (TR_IN_SEL) value, 'trig=2', in the description for PASS SARx to TCPWMx direct connect triggers one-to-one. The correct value to calculate is '4' as shown in the architecture TRM chapter 25 descriptions and table 25-2.
Parameters Affected	N/A
Trigger Condition(s)	Using the triggers one-to-one for PASS SARx to TCPWMx direct connect
Scope of Impact	The triggers one-to-one for PASS SARx to TCPWMx direct connect cannot work if TCPWM's input trigger selection is not correct.
Workaround	Use '4' as TCPWM's input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect
Fix Status	No silicon fix planned. Datasheet was updated.
Impact on Infineon software	Impact: No Related modules: PWM Comment: MCAL PWM module does not support one-to-one triggers.

修订记录

修订记录

Document revision	Date	Description of changes
**	2019-03-27	New datasheet
*A	2019-07-23	Updated Features list , CYT3BB/4BB address map , Peripheral I/O map . Updated Pin assignment , Alternate function pin assignments . Updated Trigger Group tables. Updated Peripheral clocks and Peripheral protection unit fixed structure pairs . Updated Bus masters and Miscellaneous configuration . Updated Electrical specifications . Updated Reset sequence and SPI Diagrams. Added Table 26-20 . Updated Ordering information and Packaging .
*B	2019-09-06	Updated Functional description . Updated Peripheral I/O map . Updated Pin assignment . Updated Alternate function pin assignments and Power pin assignments . Updated Miscellaneous configuration . Updated Development support . Updated Electrical specifications . Updated Ordering information . Updated Packaging .
*C	2019-11-15	Updated Ethernet MAC in Features list . Updated SRAM details in CYT3BB/4BB address map . Added Bootloading or End-of-line (EoL) Programming . Updated values of the following SIDs: 676B, 26C, 33C, 33D, 333, 216, 342A1, 342D1 to 345D1, 345E1, 342E1, 342, 343, 344, 345A1, 345, 342B1, 342A, 780C, 782C, 190A to 231A, 342E1, 679B, 683B, 342D1, 343D1, 344D1, 345E1, 345D1, 748B/C, 749B, 706/A
*D	2020-05-04	Updated Features list . Updated Functional description . Updated Power pin assignments . Updated Alternate function pin assignments . Updated Fault assignments . Updated ECO spec from 3.988 MHz to 8 MHz. Updated Electrical specifications . Updated Ordering information .
*E	2020-09-23	Updated Features and Features list . Updated Regulators . Updated Clock system . Updated Peripheral I/O map . Updated Pin function description . Updated Smoothing capacitor should be placed as close as possible to the VCCD pin . Updated Packaging . Updated Appendix . Added Errata . Updated Electrical specifications . Please refer to Revision history change log.

修订记录

Document revision	Date	Description of changes
*F	2021-10-27	Updated Features Updated Clock system Updated Power modes Updated Audio interface Updated I/Os Updated Pin assignment Updated High-speed I/O matrix connections Updated Alternate function pin assignments Updated Interrupts and wake-up assignments Updated Faults Updated Bus masters Updated Electrical specifications Updated Part number nomenclature Updated Errata
*G	2022-02-18	Updated System resources . Updated Serial memory interface specifications . Updated Part number nomenclature . Updated TQFP package diagrams. Updated Errata .
*H	2022-09-08	Updated Functional description . Updated Peripheral I/O map . Updated Electrical specifications . Updated Errata .
*I	2023-07-12	Updated Features list . Updated Communication peripheral instance list . Updated Peripherals and Peripheral I/O map . Updated Package pin list and alternate functions , Power pin assignments , and Alternate function pin assignments Updated Pin mux descriptions . Updated Electrical specifications . Added note in Packaging . Updated Errata .
*J	2024-01-25	Updated Ethernet MAC . Updated Figure 7-1 . Updated CYT3BB/4BB CPU start-up sequence . Updated Triggers one-to-one . Updated Clock specifications , Ethernet specifications , and Serial memory interface specifications . Updated Errata .

修订记录变更日志

修订记录变更日志

修订 *J 部分更新

Section	Change Description	Current Spec	New Spec	Reason for change
3.3.8. Ethernet MAC	Updated description	CYT3BB/4BB supports half/full-duplex data transport	CYT3BB/4BB supports full-duplex data transport	Correction
7. CYT3BB/4BB clock diagram	Figure 7-1	none	CLK_SLOW connect to Ethernet	Correction
8. CYT3BB/4BB CPU start-up sequence	Updated CLK_HF _x	ii. Sets clocks for CM7_0 (CLK_HF1) and CM7_1 (CLK_HF2)	ii. Sets clocks for CM7_0 (CLK_HF1) and CM7_1 (CLK_HF1)	Correction
19. Triggers one-to-one	MUX Group 6: PASS SAR _x to TCPWM0 direct connect Input: 0 : Input 71	Description: SAR0 ch#0, range violation to TCPWM0 Group #1 Counter #00 trig=2 : SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #51 trig=2	Description: SAR0 ch#0, range violation to TCPWM0 Group #1 Counter #00 trig=4 : SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #51 trig=4	Correction
26.11 Clock specifications	Table 26-20 CLK_MEM: Description	Generated by clock gating CLK_HF0, intermediate clock for SMIF, Flash, Ethernet	Generated by clock gating CLK_HF0, intermediate clock for SMIF, Flash	Correction
26.11 Clock specifications	Table 26-20 CLK_SLOW: Description	Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, SDHC	Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, SDHC, Ethernet	Correction
26.13 Ethernet specification	26.13.1 Minimum bus frequency requirements Table 26-33	Minimum AXI frequency	Minimum AHB frequency	Correction
26.16 Serial memory interface specifications	Figure 26-40	Figure of "Figure 26-12 SDR write timing reference level"	Figure of "Figure 26-40 SDR write timing reference level"	Correction
26.16 Serial memory interface specifications	Figure 26-41	Figure of "Figure 26-13 SDR read timing reference level"	Figure of "Figure 26-41 SDR read timing reference level"	Correction
26.16 Serial memory interface specifications	Figure 26-42	Figure of "Figure 26-14 DDR write timing reference level"	Figure of "Figure 26-42 DDR read timing reference level"	Correction
26.16 Serial memory interface specifications	Figure 26-43	Figure of "Figure 26-15 SDR read timing reference level"	Figure of "Figure 26-43 SDR read timing reference level"	Correction
26.16 Serial memory interface specifications	Figure 26-44	Figure of "Figure 26-16 SDR read timing reference level" 4: Clock LOW output valid = tV	Figure of "Figure 26-44 SDR read timing reference level" 4: Clock LOW to input data valid = tV	Correction
26.16 Serial memory interface specifications	Figure 26-45	Figure of "Figure 26-17 SDR read timing reference level" 4: Clock LOW output valid = tV none none	Figure of "Figure 26-45 SDR read timing reference level" 4: Clock LOW to input data valid = tV Write Timing Read Timing	Correction
27. Ordering information	Table 27-1	CYT3BB5CEBQ0AESGS CYT3BB5CEBQ0AEEGS CYT3BB7CEBQ0AESGS CYT3BB7CEBQ0AEEGS CYT3BB8CEBQ0AESGS CYT3BB8CEBQ0AEEGS CYT3BBBCEBQ0BZSGS CYT3BBBCEBQ0BZEGS CYT4BB5CEBQ0AESGS CYT4BB5CEBQ0AEEGS CYT4BB7CEBQ0AESGS CYT4BB7CEBQ0AEEGS CYT4BB8CEBQ0AESGS CYT4BB8CEBQ0AEEGS CYT4BBBCEBQ0BZSGS CYT4BBBCEBQ0BZEGS	CYT3BB5CEBQ1AESGS CYT3BB5CEBQ1AEEGS CYT3BB7CEBQ1AESGS CYT3BB7CEBQ1AEEGS CYT3BB8CEBQ1AESGS CYT3BB8CEBQ1AEEGS CYT3BBBCEBQ1BZSGS CYT3BBBCEBQ1BZEGS CYT4BB5CEBQ1AESGS CYT4BB5CEBQ1AEEGS CYT4BB7CEBQ1AESGS CYT4BB7CEBQ1AEEGS CYT4BB8CEBQ1AESGS CYT4BB8CEBQ1AEEGS CYT4BBBCEBQ1BZSGS CYT4BBBCEBQ1BZEGS	Updated Ordering information
27. Ordering information	Table 27-3	X: Reserved: 0: Reserved	X: Reserved: 0/1: Reserved	Updated Ordering code nomenclature
31. Errata	CYT3BB/4BB errata summary [17] Items: Fix Status:	Items: Hardfault may occur when calling ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode Fix Status: No silicon fix planned. TRM was updated.	Items: Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode Fix Status: No silicon fix planned. TRM will be updated.	Updated errata

修订记录变更日志

Section	Change Description	Current Spec	New Spec	Reason for change
31. Errata	CYT3BB/4BB errata summary [19] Items: Errata ID: Fix Status:	none	Items: Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet Errata ID: 212 Fix Status: No silicon fix planned. Datasheet will be updated.	Added errata
31. Errata	17. Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode Problem Definition: Trigger Condition(s): Scope of Impact: Workaround: Fix Status:	Problem Definition: ReadSWPU or WriteSWPU read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that, the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation will trigger a bus error, which can result in a hardfault occurrence based on FLASHC_FLASH_CTL register settings. Trigger Condition(s): Calling ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Scope of Impact: ReadSWPU or WriteSWPU cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Workaround: Do not use ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Fix Status: No silicon fix planned. TRM was updated. S-LLD, HSM-Perf-Lib: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty	Problem Definition: The following SROM APIs read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that, the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault occurrence based on the FLASHC_FLASH_CTL register settings. Affected SROM APIs: - ReadSWPU - WriteSWPU - GenerateHash - Checksum* - ComputeBasicHash* - CheckFactoryHash* - ProgramWorkFlash** - SwitchOverRegulators - LoadRegulatorsTrims *: Do not call it to calculate on the bank where programming/erasing is in progress. **: Do not use it during non-blocking operation. Trigger Condition(s): Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Scope of Impact: The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Workaround: Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Fix Status: No silicon fix planned. TRM will be updated. Impact: Limitation Related modules: S-LLD, HSM-Perf-Lib Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty	Updated errata
	19. Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet	none	Added "19. Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet"	Added errata

Rev. *J 电气规格更新

Spec ID	Description	Changed Item	Current Spec	New Spec	Reason for Change
SID69	Power down time from Active to DeepSleep	Max	Max: 2.5 μ s	Max: 2.8 μ s	Updated spec
SID194	SPI Master: MISO valid before SCLK capturing edge	Min Typ Max	Min: - Typ: 0.4 X (1 / fSPI) ns Max: -	Min: 0.4 X (1 / fSPI) ns Typ: 0.5 X (1 / fSPI) ns Max: 0.6 X (1 / fSPI) ns	Updated spec

修订记录变更日志

SID369	AXI clock max frequency	All	Parameter: fAXI Description: AXI clock max frequency Min: - Typ: - Max: 200 MHz Details/Conditions: Guaranteed by design	none	Removed spec
SID769	Data setup time (fCK = 100 MHz)	Description Details/Condi- tions	Description: Data setup time Details/Conditions: none	Description: Data setup time (fCK = 100 MHz) Details/Conditions: For other frequencies: $t_{SU} = t_{SU_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t_{SU_min} = value at min of SID769 t_{CK_min} = value at min of SID763 t_{CK} = actual clock period	Updated condition
SID769B	Data setup time (fCK = 90 MHz)	Description Details/Condi- tions	Description: Data setup time Details/Conditions: none	Description: Data setup time (fCK = 90 MHz) Details/Conditions: For other frequencies: $t_{SU} = t_{SU_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t_{SU_min} = value at min of SID769B t_{CK_min} = value at min of SID763B t_{CK} = actual clock period	Updated condition
SID780	Data hold time (fCK = 100 MHz)	Description Details/Condi- tions	Description: Data hold time Details/Conditions: none	Description: Data hold time (fCK = 100 MHz) Details/Conditions: For other frequencies: $t_{HD} = t_{HD_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t_{HD_min} = value at min of SID780 t_{CK_min} = value at min of SID763 t_{CK} = actual clock period	Updated condition
SID780B	Data hold time (fCK = 90 MHz)	Description Details/Condi- tions	Description: Data hold time Details/Conditions: none	Description: Data hold time (fCK = 90 MHz) Details/Conditions: For other frequencies: $t_{HD} = t_{HD_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t_{HD_min} = value at min of SID780B t_{CK_min} = value at min of SID763B t_{CK} = actual clock period	Updated condition
SID781	Clock LOW to input data valid	Description	Description: Clock LOW output valid	Description: Clock LOW to input data valid	Updated description
SID781A	Clock LOW to input data valid	Description	Description: Clock LOW output valid	Description: Clock LOW to input data valid	Updated description
SID781B	Clock LOW to input data valid	Description	Description: Clock LOW output valid	Description: Clock LOW to input data valid	Updated description
SID781C	Clock LOW to input data valid	Description	Description: Clock LOW output valid	Description: Clock LOW to input data valid	Updated description
SID812	I/O loading at DATA/CMD pins	Min	Min: 40 pF	Min: -	Updated condition
SID813	I/O loading at CLK pins	Min	Min: 40 pF	Min: -	Updated condition
SID822	I/O loading at DATA/CMD pins	Min	Min: 40 pF	Min: -	Updated condition
SID823	I/O loading at CLK pins	Min	Min: 40 pF	Min: -	Updated condition
SID872	I/O loading at DATA/CMD pins	Min	Min: 30 pF	Min: -	Updated condition
SID873	I/O loading at CLK pins	Min	Min: 30 pF	Min: -	Updated condition
SID882	I/O loading at DATA/CMD pins	Min	Min: 30 pF	Min: -	Updated condition
SID883	I/O loading at CLK pins	Min	Min: 30 pF	Min: -	Updated condition
SID893	I/O loading at DATA/CMD pins	Min	Min: 20 pF	Min: -	Updated condition
SID894	I/O loading at CLK pins	Min	Min: 20 pF	Min: -	Updated condition



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