

英飞凌 TRAVEO™ T2G 32 位车规级 MCU

基于 Arm® Cortex®-M4F 单核

概述

英飞凌 TRAVEO™ T2G 32 位车规级 MCU 是一款专为汽车应用设计的高性能、低功耗控制器，符合功能安全标准 ISO 26262 和网络安全标准 ISO 21434。CYT2CL 是 TRAVEO™ T2G 微控制器系列中的一款，主要面向仪表簇入门单元等汽车系统。CYT2CL 配备 Arm® Cortex®-M4F CPU 用于主处理，以及 Arm® Cortex®-M0+ CPU 用于外设和安全处理。这些设备内置了支持灵活数据速率控制器局域网络（CAN FD）、本地互连网络（LIN）、时钟扩展外设接口（CXPI）以及 LCD 控制器的嵌入式外设。

TRAVEO™ T2G 器件采用先进的 40 nm 工艺制造。CYT2CL 集成英飞凌低功耗闪存、多个高性能模拟和数字外设，并支持创建安全的计算平台。

特性

• 双 CPU 子系统

- 160 MHz（最大）32 位 Arm® Cortex®-M4F CPU，带有
 - 单周期乘法
 - 单精度浮点单元（FPU）
 - 存储器保护单元（MPU）
- 100 MHz（最大）32 位 Arm® Cortex®-M0+ CPU，带有
 - 单周期乘法
 - 存储器保护单元
- 处理器间硬件通信
- 三个 DMA 控制器
 - 外设 DMA 控制器 #0 (P-DMA0) 带有 76 个通道
 - 外设 DMA 控制器 #1 (P-DMA1) 带有 84 个通道
 - 内存 DMA 控制器 #0 (M-DMA0) 带有 4 个通道

• 集成存储器

- 高达 4160 KB 的代码闪存以及高达 128 KB 的工作闪存
 - 边读边写（RWW）允许在从闪存执行代码的同时对代码闪存/工作闪存进行更新
 - 单组和双组模式（专门用于无线固件更新 [FOTA]）
 - 通过 SWD/JTAG 接口对闪存进行编程
- 高达 512 KB 的 SRAM，具有可选的保留粒度

• 符合 ISO 21434 标准/EVITA Full¹⁾

- 支持增强安全硬件扩展（eSHE）和硬件安全模块（HSM）
- 安全启动和身份验证
 - 使用数字签名验证
 - 使用快速安全启动
- AES：128 位块，128/192/256 位密钥
- 3DES：64 位块，64 位密钥
- 向量单元支持非对称密钥加密算法（如 Rivest-Shamir-Adleman (RSA) 和 Elliptic Curve (ECC)）
- SHA-1/2/3：SHA-512、SHA-256、SHA-160，可变长度输入数据
- CRC：支持 CCITT CRC16 和 IEEE-802.3 CRC32

¹⁾ 部分 MPN 具有加密引擎功能。

特性

- 真随机数生成器 (TRNG) 和伪随机数生成器 (PRNG)
- 伽罗瓦/计数器模式 (GCM)
- **符合 ISO 26262 功能安全标准, 达到 ASIL-B 等级**
 - 存储器保护单元 (MPU)
 - 共享存储器保护单元 (SMPU)
 - 外设保护单元 (PPU)
 - 看门狗定时器 (WDT)
 - 多计数器看门狗定时器 (MCWDT)
 - 低电压检测器 (LVD)
 - 欠压检测器 (BOD)
 - 过压检测 (OVD)
 - 时钟监视器 (CSV)
 - 所有电源模式均受支持
 - 硬件纠错 (SECDED ECC) 覆盖所有安全关键存储器 (SRAM、闪存)
- **低功耗 2.7 V 至 5.5 V 操作**
 - 低功耗运行、睡眠、低功耗睡眠、深度睡眠和休眠模式, 可实现精细的电源管理
 - 可配置选项以实现稳健的电压欠压检测 (BOD)
 - 两个阈值电平 (2.7 V 和 3.0 V) 用于 V_{DD} 和 V_{DDA_ADC} 上的 BOD
 - 一个阈值电平 (1.1 V) 用于 V_{CCD} 上的 BOD
- **唤醒支持**
 - 最多四个引脚可将器件从休眠模式唤醒
 - 每个唤醒源的唤醒识别位
 - 最多 128 个 GPIO 引脚可将器件从睡眠模式唤醒
 - 事件发生器、SCB、看门狗计时器、RTC 警报可从深度睡眠模式中唤醒
- **时钟源**
 - 内部主振荡器 (IMO)
 - 内部低速振荡器 (ILO)
 - 外部晶体振荡器 (ECO)
 - 时钟晶体振荡器 (WCO)
 - 锁相环 (PLL)
 - 锁频环 (FLL)
 - 低功耗外部晶体振荡器 (LPECO)
- **LCD 控制器**
 - 最多可连接四个 LCD 控制器, 每个控制器具有 32 个段 (SEG) 和四个公共端 (COM)
 - 支持 A 型 (标准) 和 B 型 (低功耗) 驱动波形
 - 三种驱动模式
 - 1/2 偏置下的 PWM 驱动
 - 1/3 偏置下的 PWM 驱动
 - 数字相关性
 - 在工作、睡眠和深度睡眠功耗模式下运行
 - 数字对比度控制
- **声音子系统**
 - 两个时分复用 (TDM) 接口
 - 两种脉冲编码调制-脉冲宽度调制 (PCM - PWM) 接口
 - 最多五个声音发生器 (SG) 接口
 - 一个具有五个输入流的 PCM 音频流混频器

特性

• 通信接口

- 最多四个 CAN FD 通道
 - 与传统 CAN 相比，数据速率有所提高（高达 8 Mbps），但受物理层拓扑和收发器的限制
 - 符合 ISO 11898-1:2015 标准
 - 支持 Bosch CAN FD 规范 V1.0 对非 ISO CAN FD 的所有要求
 - ISO 16845:2015 证书可用
- 最多 12 个运行时可重新配置的串行通信模块（SCB）通道，每个模块可配置为 I²C、SPI、或 UART
- 最多两个独立 LIN 通道
 - LIN 协议符合 ISO 17987 标准
- 多达两个 CXPI 通道，数据传输速率高达 20 kbps

• 串行存储器接口（SMIF）

- 一个 SPI（单线、双线、四线或八线）、xSPI 接口
- 即时加密和解密
- 从外部存储器就地执行（XIP）

• 定时器

- 最多可使用 46 个 16 位和 16 个 32 位定时器/计数器脉冲宽度调制器 (TCPWM) 模块进行常规操作
 - 最多 12 个 16 位计数器，针对电机控制操作进行了优化（相当于 6 个具有 ZPD 和斜率控制功能的步进电机控制 [SMC] 通道）
 - 支持定时器、捕获、正交解码、脉冲宽度调制 (PWM)、带死区时间的 PWM (PWM_DT)、伪随机 PWM (PWM_PR) 和移位寄存器 (SR) 模式
- 最多 16 个事件生成 (EVTGEN) 定时器，支持从深度睡眠模式循环唤醒
 - 事件触发特定的设备操作（例如执行中断处理程序、SAR ADC 转换等）

• 实时时钟（RTC）

- 年/月/日、星期、小时：分钟：秒字段
- 支持 12 小时和 24 小时制
- 自动闰年校正

• I/O

- 最多 140 个可编程 I/O
- 两种 I/O 类型
 - GPIO 标准 (GPIO_STD)
 - GPIO 增强 (GPIO_ENH)
 - GPIO 步进电机控制 (GPIO_SMC)
 - 高速 I/O 标准低噪声 (HSIO_STDLN)

• 稳压器

- 从 2.7 V 至 5.5 V 输入电压生成 1.1 V 标称核心电压
- 稳压器的两种类型
 - 深度睡眠
 - 核心内部

• 可编程的模拟资源

- 一个 SAR 模数转换器
 - 每个 ADC 支持 32 个逻辑通道和 48 个外部通道。任何外部通道都可以连接到相应 SAR 中的任何逻辑通道
 - 12 位分辨率和高达 1 Msps 的采样率

特性

- 该 ADC 还支持六个内部模拟输入，如：
 - 带隙基准电压源用于提供绝对电压值
 - 用于结温计算的校准二极管
 - 两个 AMUXBUS 输入和两个用于监测电源电平的直接连接
- ADC 支持外部多路复用器的寻址
- ADC 具有一个序列器，支持对已配置通道进行自主扫描
- **智能 I/O**
 - 一个智能 I/O 模块，可对进出 I/O 的信号执行布尔运算
 - 支持最多八个 I/O (GPIO_STD)
- **与行业标准工具兼容**
 - **调试接口**
 - 符合 IEEE-1149.1-2001 的 JTAG 控制器和接口
 - Arm® SWD（串行线调试）端口
 - 支持 Arm® 嵌入式跟踪宏单元（ETM）跟踪
 - 使用 SWD 进行数据跟踪
 - 使用 JTAG 进行指令和数据跟踪
 - GHS/MULTI 或 IAR EWARM 用于代码开发和调试
- **封装**
 - 144-LQFP, 16 × 16 × 1.7 mm（最大），0.4 mm 引脚间距
 - 144-LQFP, 20 × 20 × 1.7 mm（最大），0.5 mm 引脚间距
 - 176-LQFP, 24 × 24 × 1.7 mm（最大），0.5 mm 引脚间距

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1 特性列表

1 特性列表

表 1 CYT2CL 所有封装特性列表

Features	Package	
	144-LQFP	176-LQFP
CPU		
Core	32-bit Arm® Cortex®-M4F CPU and 32-bit Arm® Cortex®-M0+ CPU	
Functional safety	ISO 26262 ASIL-B compliant	
Operation voltage for GPIO_STD	2.7 V to 5.5 V	
Operation voltage for GPIO_ENH	2.7 V to 5.5 V	
Operation voltage for GPIO_SMC	2.7 V to 5.5 V	
Operation voltage for HSIO_STDLN	3.0 V to 3.6 V	
Core voltage	1.05 V to 1.15 V	
Operating frequency	Arm® Cortex®-M4F 160 MHz (max) and Arm® Cortex®-M0+ 100 MHz (max), related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on)	
MPU, PPU	Supported	
FPU	Single precision (32-bit)	
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M4F CPU	
Memory		
Code-flash	4160 KB (4032 KB/Large Sectors + 128 KB/Small Sectors)	
Work-flash	128 KB (96 KB/Large Sectors + 32 KB/Small Sectors)	
SRAM (configurable for retention)	512 KB (SRAM0/256 KB + SRAM1/256 KB)	
ROM	32 KB	
Communication interfaces		
CAN0 (CAN-FD: Up to 8 Mbps)	2 ch	
CAN1 (CAN-FD: Up to 8 Mbps)	2 ch	
CAN RAM	16 KB per instance (2 ch), 32 KB in total	
Serial communication block (SCB)	12 ch	
LIN/UART master support	2 ch	
CXPI controller	2 ch	
Memory interfaces		
SMIF (Single SPI/Dual SPI/Quad SPI/ Octal SPI/xSPI)	1 ch (HSIO_STDLN at 100 MHz)	
Timers		
RTC	1 ch	
TCPWM (16-bit)	34 ch	
TCPWM (16-bit) SMC	12 ch	

(表格续下页.....)

1 特性列表

表 1 (续) CYT2CL 所有封装特性列表

Features	Package	
	144-LQFP	176-LQFP
TCPWM (32-bit)	16 ch	
External interrupts	108	140
Analog		
12-bit, 1 Msps SAR ADC	1 Unit (SAR0, 32 logical channels)	
	48 external channels	
	6 ch for Internal sampling	
Security - ISO 21434 compliant		
Flash security (program/work read protection)	Supported	
Flash chip erase enable	Configurable	
eSHE/HSM	By separate firmware ¹⁾	
Sound		
Mixer	1 ch (5 mixer sources)	
PCM-PWM	2 ch	
TDM	2 TDM structures (TDM0/1 with up to 16 ch)	
Sound generator (SG)	5 ch	
LCD controller		
Common	4	
Segments	Up to 32 segments	
Type	Type A and Type B	
System		
DMA controller	P-DMA0 with 76 channels (32 general purpose), P-DMA1 with 84 channels (16 general purpose), and M-DMA0 with 4 channels	
Internal main oscillator	8 MHz	
Internal low-speed oscillator	32.768 kHz (nominal)	
PLL	Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 160 MHz	
FLL	Input frequency: 0.25 to 80 MHz, FLL output frequency: up to 100 MHz	
Watchdog timer and multi-counter Watchdog timer	Supported (WDT + 2× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM4	
Clock supervisor	Supported	
Cyclic wakeup	Supported	
GPIO standard (GPIO_STD)	66	96

(表格续下页.....)

1 特性列表

表 1 (续) CYT2CL 所有封装特性列表

Features	Package	
	144-LQFP	176-LQFP
GPIO enhanced (GPIO_ENH)	6	8
GPIO SMC (GPIO_SMC)	24	
HSIO standard low noise (HSIO_STDLN)	12	
Smart I/O (Blocks)	1 block, mapped through 8 I/Os	
Low-voltage detect	Two, 26 selectable levels	
Maximum ambient temperature	105°C for S-grade	
Debug interface	SWD/JTAG	
Debug trace	Arm® Cortex®-M4F ETB size of 8 KB, Arm® Cortex®-M0+ MTB size of 4 KB	

1) 增强安全硬件扩展 (eSHE) 和硬件安全模块 (HSM) 支持由第三方固件实现。

1.1 外设实例列表

表 2 列出了通讯外设在每个封装下支持的实例，根据实现功能所需的最少引脚数。

表 2 外设实例列表

Module	144-LQFP	176-LQFP	Minimum pin function set
CXPI	0/1	0/1	TX, RX
CAN0	0/1	0/1	TX, RX
CAN1	0/1	0/1	TX, RX
LIN0	0/1	0/1	TX, RX
SCB/UART	0 to 11	0 to 11	TX, RX
SCB/I2C	0 to 11	0 to 11	SCL, SDA
SCB/SPI	0 to 11	0 to 11	MISO, MOSI, CLK, SELECT0
TDM/RX	0/1	0/1	MCK, FSYNC, SCK, SD
TDM/TX	0/1	0/1	MCK, FSYNC, SCK, SD
SG	0 to 4	0 to 4	TONE, AMPL
PWM	0/1	0/1	LINE1/2_P/N

3 功能描述

3 功能描述

3.1 CPU 子系统

3.1.1 CPU

CYT2CL CPU 子系统包含一个 32 位 Arm®Cortex®-M0+ CPU（带 MPU）、一个 32 位 Arm®Cortex®-M4F CPU（带 MPU）和单精度 FPU。该子系统还包括 P-/M-DMA 控制器、加密加速器、高达 4160 KB 的代码闪存、128 KB 的工作闪存、高达 512 KB 的 SRAM 和 32 KB 的 ROM。

Cortex®-M0+ CPU 提供了安全、不可中断的启动功能。这保证了启动功能完成后，系统完整性有效且权限得到强制执行。共享资源（闪存、SRAM、外设等）可以通过总线仲裁进行访问，并且使用硬件信号量的处理器间通讯（IPC）机制来支持独占访问。

3.1.2 DMA 控制器

CYT2CL 有三个 DMA 控制器：具有 32 个通用通道和 44 个专用通道的 P-DMA0、具有 16 个通用通道和 68 个专用通道的 P-DMA1 以及具有四个通道的 M-DMA0。P-DMA 用于外设到存储器和存储器到外设的数据传输，并为大量通道提供低延迟。

每个 P-DMA 控制器使用单个数据传输引擎并由相关通道共享。通用通道具有丰富的互连矩阵，包括 P-DMA 交叉触发，可满足苛刻的数据传输场景的要求。专用通道具有单个触发输入（例如 ADC 通道）来处理常见的传输需求。M-DMA 用于存储器到存储器的数据传输，并为少量通道提供高内存带宽。M-DMA 为每个通道使用专用的数据传输引擎。

它们支持通过 AHB 多层总线独立访问外设。

3.1.3 闪存

CYT2CL 具有高达 4160 KB（4032 KB 扇区大小为 32 KB，128 KB 扇区大小为 8 KB）的代码闪存，以及额外的工作闪存高达 128 KB（96 KB 扇区大小为 2 KB，32 KB 扇区大小为 128 B）。工作闪存经过了优化，可以比代码闪存进行更多次重新编程。代码闪存支持边读边写（RWW）操作，允许在 CPU 工作模式时更新闪存。代码闪存和工作闪存区域均支持用于远程（OTA）编程的双组操作。

3.1.4 SRAM

CYT2CL 具有高达 512 KB 的 SRAM（512 KB）和两个独立的控制器。第一个控制器 SRAM0 以 32 KB 的增量提供在深度睡眠模式下的数据保留，而 SRAM1 可在完全保留或不保留之间选择。

3.1.5 ROM

CYT2CL 具有 32 KB 的 ROM，其中包含启动和配置例程。该 ROM 可实现安全启动和用户的闪存验证，以保证系统的安全。

3.1.6 安全加密加速器

密码加速器实现（3）DES 功能块密码、AES 功能块密码、SHA 散列、循环冗余校验、伪随机数生成、真随机数生成、伽罗瓦/计数器模式和向量单元以支持 RSA 和 ECC 等非对称密钥密码。

3 功能描述

根据料号的不同，此功能块可能完全可用、部分可用或完全不可用。详情参见[订购信息](#)。

3.2 系统资源

3.2.1 电源系统

电源系统确保电源电压电平满足每种电源模式的要求，并在这些电平无效时提供全系统复位。内部上电复位（POR）保证初始电源上升期间的全芯片复位。

三个欠压检测（BOD）电路用于监测外部电源电压（ V_{DD0} 、 V_{DDA_ADC} 、 V_{CC0} ）。 V_{DD0} 和 V_{CC0} 上的 BOD 初始状态为启用，且无法禁用。 V_{DDA_ADC} 上的 BOD 初始状态为禁用，可由用户启用。对于外部电源 V_{DD0} 和 V_{DDA_ADC} ，BOD 电路可通过软件配置，提供两种设置：一种是 2.7 V 最小电压，对所有内部信号均具有稳健性；另一种是 3.0 V 最小电压，对所有 I/O 规范同样具有稳健性（I/O 规范在 2.7 V 时得到保证）。 V_{CC0} 上的 BOD 仅作为安全措施提供，并非可靠的检测器。

提供三个过压检测（OVD）电路用于监控外部电源（ V_{DD0} 、 V_{DDA_ADC} 、 V_{CC0} ），以及过流检测电路（OCD）用于监控内部和外部稳压器。 V_{DD0} 和 V_{DDA_ADC} 上的 OVD 阈值可配置为两种设置：5.0 V 和 5.5 V 最大电压。

提供了两个电压检测电路来监控外部电源电压（ V_{DD0} ）的下降和上升电平，每个电路均可配置为 26 个可选电平之一。

V_{DD0} 和 V_{CC0} 上的所有 BOD、OVD 和 OCD 电路都会产生复位，因为它们用于保护 CPU 和故障逻辑。 V_{DDA_ADC} 上的 BOD 和 OVD 电路可以配置为产生复位或故障。

3.2.2 稳压器

CYT2CL 包含两个稳压器，为低压核晶体管提供电源：深度睡眠和核内稳压器。这些稳压器接受 2.7 V 至 5.5 V V_{DD0} 供电，并为器件的各个部分提供低噪声的 1.1 V 供电。这些稳压器在切换电源模式时由硬件和固件自动启用和禁用。核内稳压器在工作模式下工作，为 CPU 子系统及相关外设供电。

3.2.2.1 深度睡眠

深度睡眠稳压器用于在深度睡眠模式下维持供电给少数模块。这些模块包括 ILO 和 WDT 定时器、BOD 检测器、SCB0、SRAM 存储器、智能 I/O 和其他配置存储器。深度睡眠稳压器在深度睡眠模式下启用，此时核内稳压器被禁用。当 XRES_L 有效（低电平）时，或当核内稳压器被禁用时，深度睡眠稳压器也被禁用。

3.2.2.2 核心内部

核内稳压器支持高达 150 mA 的负载电流，并且在器件启动（启动过程）期间以及在工作/睡眠模式下运行。

3.2.3 时钟系统

CYT2CL 时钟系统为所有需要时钟的子系统提供时钟，并在不同时钟源之间实现无毛刺切换。此外，它还确保不发生亚稳态。

CYT2CL 的时钟系统由 8 MHz IMO、两个 ILO、三个看门狗定时器、三个 PLL、一个 FLL、五个时钟监视器（CSV）、一个 7.2 至 33.34 MHz ECO、一个 4 至 8 MHz LPECO 和一个 32.768 kHz WCO 组成。

3 功能描述

时钟系统支持两个主时钟域：CLK_HF 和 CLK_LF。

- CLK_HF_x 是运行域时钟。每个都可以使用任何高频时钟源，包括 IMO、EXT_CLK、ECO、LPECO、FLL 或 PLL。
- CLK_LF 是深度睡眠域时钟，为 MCWDT 或 RTC 模块提供源。CLK_LF 域的基准时钟可以从 ILO0、ILO1、WCO 中选择，也可禁用。

表 3 CLK_HF 目标

Name	Description
CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure
CLK_HF1	Event Generator, also available in HSIOM as an output
CLK_HF2	Sound Subsystem #0
CLK_HF3	Sound Subsystem #1
CLK_HF4	Sound Subsystem #2
CLK_HF5	SMIF #0

3.2.3.1 IMO 时钟源

当没有外部基准可用或被使能时，IMO 是 CYT2CL 的频率基准。IMO 的运行频率约为 8 MHz。

3.2.3.2 ILO 时钟源

ILO 是一种低功耗振荡器，标称频率为 32.768 kHz，在深度睡眠模式下为看门狗定时器产生时钟。有两个 ILO 可确保深度睡眠模式下的时钟监视器（CSV）功能。可以根据 IMO、WCO 或 ECO 来校准 ILO 驱动的计数器，以提高其精度。ILO1 也用于时钟监视。

3.2.3.3 PLL 和 FLL

可以使用 PLL（两个 200 MHz 和一个 400 MHz）或 FLL 来从 IMO、ECO 或 EXT_CLK 生成高速时钟。与锁相环相比，FLL 提供的锁定速度要快得多（5 μ s 而不是 35 μ s），但会引入少量频率误差⁴以及较低的最大输出频率（100 MHz，而不是高达 400 MHz）。400 MHz PLL 支持具有向下展频的展频时钟生成（SSCG）。

3.2.3.4 时钟监视器

每个时钟监视器（CSV）允许一个时钟（基准）监控另一个时钟（被监控）的行为。每个 CSV 都有用于监控和参考时钟的计数器。每个计数器的参数决定基准时钟的频率以及受监控时钟的频率上限和下限。如果频率范围比较器检测到停止的时钟或指定频率范围之外的时钟，则会发出异常状态信号并产生复位或中断。

3.2.3.5 EXT_CLK

两个 I/O 中的一个可用于提供高达 100 MHz 的外部时钟输入。该时钟可以用作 PLL 或 FLL 的源时钟，也可以直接由 CLK_HF 域使用。

⁴ 由于频率误差，不建议使用基于 FLL 的参考源来操作参考定时外设（例如 UART）。

3 功能描述

3.2.3.6 ECO

ECO 使用连接到 ECO_IN 和 ECO_OUT 引脚的外部晶体提供高频时钟。它支持基模（非泛音）石英晶体，范围为 7.2 至 33.34 MHz。与 PLL 结合使用时，它可为 CPU 和外设生成最高达器件最大频率的时钟。ECO 精度取决于所选的晶体。如果 ECO 被禁用，则相关引脚可用于任何可用的 I/O 功能。

3.2.3.7 LPECO

LPECO 使用连接到 LPECO_IN 和 LPECO_OUT 引脚的外部晶体提供高频时钟。它支持基模（非泛音）石英晶体，范围为 3.99 至 8.01 MHz。LPECO 可以在深度睡眠和休眠模式下运行，电流消耗显著降低。它还可用于实时时钟应用。与 PLL 结合使用时，它可为 CPU 和外设生成最高达器件最大频率的时钟。

3.2.3.8 WCO

WCO 是一款低功耗时钟晶体振荡器，适用于实时时钟应用。它需要一个外部 32.768-kHz 晶体连接到 WCO_IN 和 WCO_OUT 引脚。WCO 还可以配置为 CLK_LF 的时钟基准，CLK_LF 是 MCWDT 和 RTC 的时钟源。

3.2.4 复位

CYT2CL 可以从多种来源复位，包括软件。复位事件是异步的，并确保器件恢复到一个已知状态。复位原因（POR、BOD、OVD、过流、XRES_L、WDT、MCWDT、软件复位、故障、CSV、休眠唤醒、调试）记录在一个寄存器中，该寄存器在复位后不会被清零，并允许软件确定复位的原因。XRES_L 引脚可用于外部复位。

3.2.5 看门狗定时器

CYT2CL 具有一个看门狗定时器（WDT）和两个多计数器看门狗定时器（MCWDT）。

WDT 是一个自由运行的计数器，仅由 ILO0 提供时钟，因此可以将其用作休眠模式的唤醒源。这允许在所有电源模式下进行看门狗操作，需要在配置的窗口期间进行喂狗操作，否则将在超时发生前未喂狗时产生看门狗复位。看门狗复位被记录在复位原因寄存器中。

每个 CPU 核都有一个 MCWDT。这些定时器提供比 WDT 更多的功能，并且仅在运行、睡眠和深度睡眠模式下可用。这些定时器有多个计数器，可以单独使用或级联使用来触发中断和/或复位。它们由 ILO0 或 WCO 提供时钟。

3.2.6 功耗模式

CYT2CL 有六种功耗模式。

- 运行 - 所有外设均可用
- 低功耗运行（LPACTIVE） - 工作模式低功耗配置，其中所有外设和 CPU 均可用，但功能有限
- 睡眠 - 除 CPU 外的所有外设均可用
- 低功耗睡眠（LPSLEEP） - 睡眠模式低功耗配置，其中除 CPU 之外的所有外设均可用，但功能有限
- 深度睡眠 - 仅可使用与 CLK_LF 配合使用的外设
- 休眠 - 器件和 I/O 状态被冻结，器件在唤醒时会复位

3 功能描述

3.3 外设

3.3.1 外设时钟分频器

提供整数和小数时钟分频器用于外设和定时目的。

表 4 时钟分频器

Divider	Count	Description
div_8	11	Integer divider, 8 bits
div_16	16	Integer divider, 16 bits
div_16_5	4	Fractional divider, 16.5 bits (16 integer bits, 5 fractional bits)
div_24_5	11	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 外设保护单元

外设保护单元 (PPU) 控制和监视从所有主设备 (CPU、P-/M-DMA、加密和任何启用的调试接口) 到外设的未经授权的访问。它允许或限制总线基础设施上的数据传输。访问规则是根据传输的特定属性来强制执行的，例如传输的地址范围和访问属性 (例如读/写、用户/特权和安全/非安全)。

3.3.3 12 位 SAR ADC

CYT2CL 包含一个 1-Msps SAR ADC。该 ADC 的时钟频率高达 26.67 MHz，可在 26 个时钟周期内提供 12 位结果。

SAR ADC 的参考信号来自一对专用输入：VREFH 和 VREFL⁵。

CYT2CL 支持 32 个逻辑 ADC 通道，可从 54 个输入源中选择一个。信号源包括来自 I/O 的 48 个外部输入，以及用于诊断和监测的六个内部连接。

表 1 中列出了 ADC 通道数 (每个 ADC 和封装类型)。

SAR ADC 具有一个序列器，能够自主循环扫描已配置的通道 (序列扫描)，且切换开销为零 (也就是说，当时钟频率为 26.67 MHz 时，无论用于单个通道还是分布在多个通道上，总采样率都等于 1 Msps)。序列器切换通过状态机或固件控制。序列器对触发请求进行优先级排序，启用适当的模拟通道，控制 ADC 采样，启动 ADC 数据转换，管理结果，并启动后续的重转换或组转换，而无需 CPU 干预。

SAR ADC 具有两个模拟多路复用器，用于将待测信号连接到 ADC。其中一个 SARMUX0，它有 24 个 GPIO_STD 输入 (ADC[0]_0 至 ADC[0]_23)，以及六个额外的输入，用于测量内部信号，例如带隙基准、温度传感器、V_{CCD}、V_{DDA_ADC} 电源和 AMUXBUSA/B 信号。另一个多路复用器是 SARMUX1，它有 24 个 GPIO_SMC 输入 (ADC[1]_0 至 ADC[1]_23)。

CYT2CL 有一个温度传感器。需要软件后处理将温度传感器读数转换为开尔文或摄氏度值。

为了适应各种源阻抗和频率的信号，每个通道可以编程不同的采样时间。ADC 还支持范围比较功能，无需等待定序器扫描完成，也无需等待 CPU 固件评估测量值是否超出量程，即可快速检测出超出范围的数值。

ADC 不能用于深度睡眠和休眠模式，因为它们需要高速时钟。ADC 输入基准电压 VREFH 范围为 2.7 V 至 V_{DDA_ADC}，VREFL 为 V_{SSA_ADC}。

⁵ VREF_L 可防止 VSSIO 和 VSSA_ADC 路径中的 IR 压降影响测量。当 VREF_L 正确连接时，可以降低或消除 VSSIO 和 VSSA_ADC 路径中的 IR 压降对测量的影响。

3 功能描述

3.3.4 定时器/计数器/脉宽调制器模块 (TCPWM)

TCPWM 功能块由 16 位（46 个通道）和 32 位（16 个通道）计数器组成，具有用户可编程周期。其中十二个 16 位计数器针对 DC 电机和步进电机控制操作进行了优化。每个 TCPWM 计数器包含一个捕获寄存器，用于记录发生事件时的计数值，一个周期寄存器（用于在计数值等于周期寄存器值时停止或自动重载计数器）和比较寄存器，用于生成作为 PWM 占空比输出的信号。

TCPWM 模块内的每个计数器都支持多种功能模式，例如定时器、捕获、正交、PWM、带死区插入的 PWM（PWM_DT，8 位）、伪随机 PWM（PWM_PR）和移位寄存器。

TCPWM 模块还提供正相输出和互补输出，两者之间的偏移量可编程控制，以允许将其用作死区互补 PWM 输出。TCPWM 模块还具有 Kill 输入（仅适用于 PWM 模式）用于强制输出进入预定状态；例如，在电机驱动系统中，当出现过流状态时，需要立即使用它来关闭驱动 FET 的 PWM（没有时间用于软件干预）。

十二个 16 位计数器针对 DC 和步进电机控制操作进行了优化，还具有 ZPD（零点检测）和斜率控制功能。其中每两个 TCPWM 通道构成一个 SMC 通道。

3.3.5 串行通信模块 (SCB)

CYT2CL 包含 12 个串行通信模块，每个模块可配置为 I²C、UART 或 SPI。

3.3.5.1 I²C 接口

SCB 可配置为实现完整的 I²C 主机（支持多主仲裁）或从机接口。每个配置为 I²C 的 SCB 最高工作速率可达 1 Mbps（快速模式 Plus⁶⁾），并具有灵活的缓冲选项，以减少 CPU 的中断开销和延迟。此外，每个 SCB 均支持接收和发送数据的 FIFO 缓冲器，通过延长 CPU 读取数据的时间，从而减少了时钟拉伸的需求。该 I²C 接口与 NXP I²C 总线规范和用户手册 (UM10204) 中规定的标准模式、快速模式和快速模式 Plus 设备兼容。I²C 总线 I/O 通过处于开漏模式的 GPIO 实现⁷⁾，⁸⁾。

3.3.5.2 UART 接口

当配置为 UART，每个 SCB 提供全功能 UART，其最大速率由配置的外设时钟频率和过采样率确定。它支持红外接口 (IrDA) 和智能卡 (ISO 7816) 协议，这些协议是 UART 协议的小变种。此外，它还支持 9 位多处理器模式，此模式允许寻址连接到通用 RX 和 TX 线的外设。

支持通用 UART 功能，如奇偶校验、停止位的数量、断帧检测和帧错误。发送和接收数据的 FIFO 缓冲允许容忍更大的 CPU 服务延迟。

LIN 协议由 UART 支持。LIN 基于单主多从拓扑结构。LIN 总线上有一个主节点和多个从机节点。SCB UART 仅支持 LIN 从机功能。

与专用 LIN 模块相比，以 SCB/UART 用作 LIN 需要更高水平的软件交互和增加 CPU 负载。

⁶⁾ I/O 驱动电平不支持快速模式 Plus 速度下的完整总线电容。

⁷⁾ 这并非 100% 符合 I²C-总线规范；I/O 不符合高压标准，不支持快速模式 Plus 的 20 mA 灌电流要求，并且在不供电的情况下违反泄漏规范。

⁸⁾ 有关支持的 I/O 单元和 I²C 模式，参见表 37。

3 功能描述

3.3.5.3 SPI 接口

SPI 配置支持完整的 Motorola SPI、TI 同步串行协议 (SSP，本质上是添加启动脉冲用于同步基于 SPI 的编解码) 和 National Microwire (SPI 的半双工形式)。SPI 接口可以使用 FIFO。SPI 接口以高达 12.5 MHz 的 SPI 时钟运行。SCB 还支持 EZSPI⁹ 模式。

SCB0 支持以下附加特性：

- 在深度睡眠模式下可作为从机操作
- I²C 从机 EZ (EZI2C¹⁰) 模式，最多可容纳 256 B 数据缓冲，无需 CPU 干预即可实现多字节通讯
- I²C 从机外部时钟操作
- 具有 512 B 数据缓冲区的命令/响应模式，可进行多字节通信，无需 CPU 干预

3.3.6 CAN FD

CYT2CL 支持两个 CAN FD 控制器模块，每个模块支持两个 CAN FD 通道。所有 CAN FD 控制器均符合 ISO 11898-1:2015 标准；可提供 ISO 16845:2015 证书。它还在硬件中完全实现了 ISO 11898-4 (TTCAN 协议级别 1 和 2) 中指定的时间触发 CAN (TTCAN) 协议。所有与信息处理有关的功能均由 Rx 和 Tx 处理程序实现。Rx 处理器管理报文验收过滤、将接收到的消息从 CAN 核心传输到消息 RAM，并提供接收消息状态。Tx 处理器负责将发送消息从消息 RAM 传输到 CAN 核心，并提供发送消息状态。

3.3.7 本地互连网络 (LIN)

CYT2CL 含有多达两个 LIN 通道。每个通道都支持按照 ISO 标准 17987 的 LIN 协议传输/接收数据。每个 LIN 通道通过 3 引脚接口 (包括使能功能) 连接到外部收发器，并支持主机和从机功能。每个通道还支持经典和增强的校验和，以及消息接收和唤醒信令期间的断帧检测。断帧检测、同步场、校验和计算以及错误中断均由硬件处理。

3.3.8 时钟扩展外设接口 (CXPI)

CYT2CL 包含多达两个符合 JASO D015 和 ISO 标准 20794 (包括控制器规范) 的 CXPI 通道。

每个通道支持：

- 主机和从机功能
- 针对正常帧和长帧的轮询和事件触发方法
- 非归零编码 (NRZ) 和 PWM 信号模式
- 碰撞解析以及载波监听多路访问机制
- 唤醒脉冲的生成和检测
- 正常帧和长帧的 CRC8 和 CRC16
- 错误检测
- 用于发送和接收的专用 FIFO (16 B)

⁹ Easy SPI (EZSPI) 协议基于摩托罗拉 SPI，可在任何模式 (0、1、2 或 3) 下运行。它允许主机和从机之间进行通信，同时减少 CPU 干预的需要。

¹⁰ Easy I²C (EZI2C) 协议是英飞凌在 I²C 协议基础上构建的独特通信方案。它使用标准 I²C 协议的元协议，使用索引内存传输与 I²C 从机进行通信。这减少了对 CPU 干预的需要。

3 功能描述

3.3.9 串行存储器接口

除了内部闪存外，CYT2CL 还支持直接连接多达 128 MB 的外部快闪式存储器或 RAM 存储器。此连接通过 xSPI 或串行外设接口 (SPI) 建立。xSPI 允许连接 HYPERFLASH™ 和 HYPERRAM™ 设备，而 SPI (单线、双线、四线或八线 SPI) 可以连接串行闪存。通过该接口连接的内存中存储的代码允许就地执行 (XIP) 操作，该操作不需要先将指令复制到内部内存，并且对于需要安全外部数据和代码的环境可以进行即时加密和解密。

3.3.10 声音子系统

CYT2CL 支持以下功能：

- 最多两个时分复用 (TDM) 接口
 - 全双工发射器和接收器操作
 - 独立发送或接收操作，每个支持主模式或从模式
 - 最多 16 个通道，每个通道可单独启用或禁用
- 最多两个脉冲编码调制-脉冲宽度调制 (PCM - PWM) 接口
 - 将 PCM 音频流转换为 PWM 信号
 - 高达 32 位输出样本分辨率
 - 支持 E 桥和 H 桥格式
 - 死区时间插入
- 最多五个声音发生器 (SG) 接口
 - PWM 调制 (振幅、音调) 声音生成
 - 单独的音量和频率控制 (两个信号) 以及音量和频率组合控制 (一个信号) 格式
- 一台混频器支持五种输入源
 - 将多个 PCM 源流合并为一个 PCM 目标流
 - PCM 音源流可以进行增益/音量控制。
 - 固定 PCM 采样格式 (16 位成对)
 - 通过 FIR 滤波器支持 LPF
 - 对源 PCM 流和目标 PCM 流进行淡入淡出控制

3.3.11 一次性可编程 (OTP) eFuse

CYT2CL 包含一个 1024 位 OTP eFuse 存储器，可用于存储和访问每个器件的唯一且不可更改的标识符或序列号。eFuse 还用于控制设备生命周期 (制造、编程、正常运行、寿命终止等) 和安全状态。在 1024 位中，有 192 位可供用户使用。

3.3.12 事件发生器

事件发生器支持在工作模式下产生中断和触发，以及在深度睡眠模式下产生中断。事件发生器用于触发特定的器件操作 (执行中断处理程序、SAR ADC 转换等) 并提供从深度睡眠模式的循环唤醒机制。它们为器件功能提供无需 CPU 的触发器，减少 CPU 在触发器件功能时的参与，从而降低总体功率消耗和处理开销。

3 功能描述

3.3.13 触发多路复用器

CYT2CL 支持使用触发信号连接各种外设。触发器用于通知外设事件的发生或状态的改变。这些触发器用于影响或启动其他外设的某些操作。触发多路复用器用于将触发器从来源外设路由到目的地。触发器提供有效的逻辑功能，并且通常在工作模式下受支持。

3.3.14 LCD 控制器

CYT2CL 支持以下功能：

- 最多 32 个网段 (SEG) 和四个公共网段 (COM)
- A 型 (标准) 和 B 型 (低功耗) 驱动波形
- 将任何 GPIO 引脚配置为公共端或段
- 三种驱动方式：
 - 数字相关性
 - 1/2 偏置下的 PWM
 - 1/3 偏置下的 PWM
- 运行、睡眠和深度睡眠模式操作
- 数字对比度控制

3.4 I/Os

CYT2CL 具有多达 140 个可编程 I/O。

I/O 被组织为称为端口的逻辑实体，其最大宽度为 8 位。在上电和复位期间，I/O 被强制进入 High-Z 状态。在休眠模式期间，I/O 被冻结。

每个 I/O 引脚都能生成一个中断（如果被启用），并且每个 I/O 端口都有一个与其相关的中断请求 (IRQ) 和中断服务程序 (ISR)。

I/O 端口功率源映射列于表 5 中。相关电源决定了配置为 CMOS 和汽车阈值时的 V_{OH} 、 V_{OL} 、 V_{IH} 和 V_{IL} 电平。

表 5 I/O 端口电源

Supply	Ports
VDDD	P0, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19
VDDIO_GPIO	P1, P2, P3, P4
VDDIO_HSIO	P8, P9
VDDIO_SMC	P5, P6, P7

每个 I/O 实施以下内容：

- 可编程驱动模式
 - 高阻态
 - 电阻上拉
 - 电阻下拉
 - 开漏带强下拉
 - 开漏带强上拉
 - 强上拉或下拉
 - 弱上拉或下拉

3 功能描述

CYT2CL 有四种类型的可编程 GPIO：GPIO 标准、GPIO 增强、GPIO SMC、HSIO 标准低噪声。只有 GPIO_STD、GPIO_ENH 和 GPIO_SMC 能够将器件从深度睡眠模式中唤醒。

3.4.1 GPIO

支持三种类型的 GPIO：

- GPIO_STD, GPIO_ENH, 和 GPIO_SMC

这些 GPIO 实现以下功能：

- 可配置输入阈值（CMOS、TTL 或汽车）
- 保持模式，用于锁存先前状态（用于在深度睡眠模式下保持 I/O 状态）
- 模拟输入模式（输入和输出缓冲器禁用）
- 基于引脚，可配置为上升沿、下降沿或双边沿触发的中断

3.4.1.1 GPIO 标准 (GPIO_STD)

支持 2.7 V 至 5.5 V V_{DDIO} 范围内的标准汽车信号。GPIO 标准 I/O 具有多个可配置的驱动级别、驱动模式和可选的输入级别。

3.4.1.2 GPIO 增强 (GPIO_ENH)

支持 2.7 V 至 5.5 V V_{DDIO} 范围内的扩展功能汽车信号，可在较低电压下提供更高的电流（完全 I²C 时序支持、斜率控制）。

3.4.1.3 GPIO SMC (GPIO_SMC)

提供比 GPIO_STD 和 GPIO_ENH 更强的驱动力（支持 30 mA 驱动）。

3.4.2 HSIO

这些 I/O 专门针对高速信号传输进行了优化，不支持斜率控制、深度睡眠模式操作、POR 模式控制、模拟连接或非 CMOS 信号传输级别。HSIO 还支持可编程驱动强度。它们仅在工作模式下可用。

3.4.2.1 HSIO 标准低噪声 (HSIO_STDLN)

支持高达 100 MHz 的时钟和信号传输。还支持在深度睡眠模式下保持状态。低噪声版本通过为每个接口提供特定模式来优化产生的噪声。

3.4.3 端口命名规则

Px.y 描述 I/O 端口“x”内可用的特定位“y”。

- 例如，P4.2 的含义是“端口 4，位 2”

3.4.4 智能 I/O

智能 I/O 允许对从芯片子系统发送到 I/O 的信号或进入芯片的信号进行布尔运算。CYT2CL 有一个智能 I/O 功能块。操作可以是同步或异步，并且块可以在除休眠之外的所有器件功耗模式下操作。

4 CYT2CL 地址映射

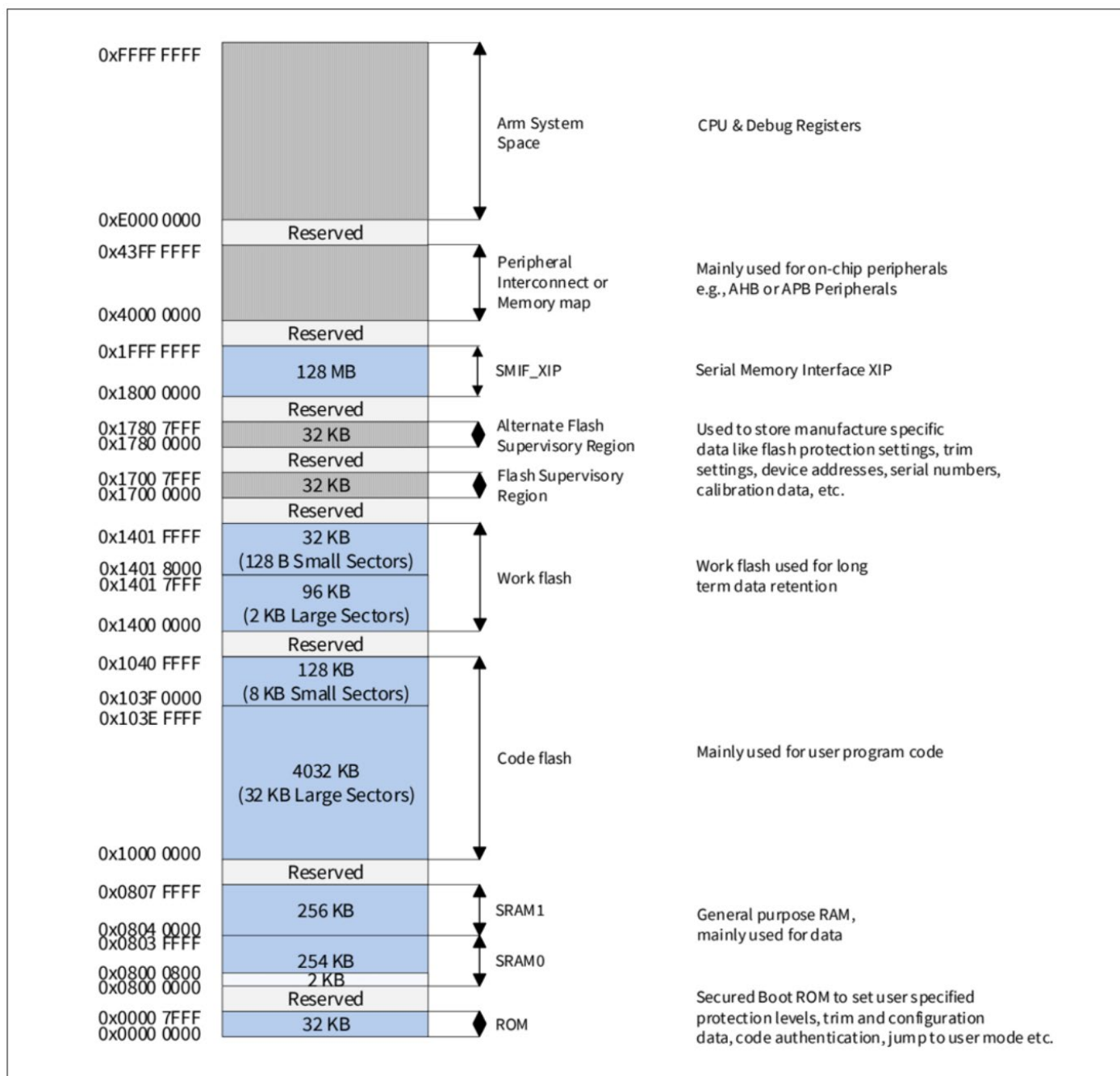
4 CYT2CL 地址映射

CYT2CL 微处理器支持的存储空间如[图 2](#)所示：

- 代码闪存
 - 4160 KB (4032 KB + 128 KB) 代码闪存，根据闪存控制寄存器中的相关位，可工作于单组或双组模式
 - 单组模式 - 4160 KB
 - 双组模式 - 每组 2080 KB
- 工作闪存
 - 128 KB (96 KB + 32 KB) 工作闪存，根据闪存控制寄存器中的相关位，可工作于单组或双组模式
 - 单组模式 - 128 KB
 - 双组模式 - 每组 64 KB
- 32 KB 安全 ROM
- 512 KB SRAM (前 2 KB 保留供内部使用)
- 128 MB SMIF XIP

4 CYT2CL 地址映射

图 2 CYT2CL 地址映射¹¹⁾, ¹²⁾



¹¹⁾ 尺寸不是等比例缩放。

¹²⁾ 第一个 2KB SRAM 被保留，不供用户使用。用户必须在所有工作、低功耗工作、睡眠、低功耗睡眠和深度睡眠模式下，保持 SRAM0 前 32 KB 功能块的供电处于使能或保留状态。

5 闪存基地址映射

5 闪存基地址映射

表 6 至表 11 提供有关代码和工作闪存区域的扇区映射及其各自基地址的信息。

表 6 单组模式下代码闪存地址映射

Code-flash size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large sector base address	Small sector base address
4160	32 KB × 126	8 KB × 16	0x1000 0000	0x103F 0000

表 7 单组模式下工作闪存地址映射

Work-flash size (KB)	Large sectors	Small sectors	Large sector base address	Small sector base address
128	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000

表 8 双组模式下的代码闪存地址映射（映射 A）

Code-flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1000 0000	0x101F 8000	0x1200 0000	0x121F 8000

表 9 双组模式下的代码闪存地址映射（映射 B）

Code-flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First Half LS base address	First half SS base address	Second half LS base address	Second half SS base address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1200 0000	0x121F 8000	0x1000 0000	0x101F 8000

表 10 双组模式下工作闪存地址映射（映射 A）

Work-flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1400 0000	0x1400 C000	0x1500 0000	0x1500 C000

5 闪存基地址映射

表 11 双组模式下工作闪存地址映射（映射 B）

Work- flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1500 0000	0x1500 C000	0x1400 0000	0x1400 C000

6 外设 I/O 映射

6 外设 I/O 映射

表 12 CYT2CL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	group	slave
PERI	Peripheral interconnect	0x4000 0000			0	
	Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9)	0x4000 4000	9	0x20		0
	Peripheral trigger group	0x4000 8000	13	0x400		
	Peripheral 1:1 trigger group	0x4000 C000	13	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4001 0000			0	
	PERI Programmable PPU	0x4001 0000	61)	0x40		1
	PERI Fixed PPU	0x4001 0800	450	0x40		
Crypto	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000				
	IPC structures	0x4022 0000	8	0x20	2	2
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000				
	Shared memory protection unit structures	0x4023 2000	16	0x40	2	3
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	Flash controller	0x4024 0000			2	4
SRSS	System Resources Sub-System Core Registers	0x4026 0000			2	
	Clock Supervision High Frequency	0x4026 1400	3	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			5
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Multi Counter WDT	0x4026 8000	2	0x100		
	Free Running WDT	0x4026 C000	1			
BACKUP	SRSS Backup Domain/RTC	0x4027 0000				6
	Backup Register	0x4027 1000	4	0x04	2	
P-DMA	P-DMA0 Controller	0x4028 0000				
	P-DMA0 channel structures	0x4028 8000	76	0x40	2	7
	P-DMA1 Controller	0x4029 0000				
	P-DMA1 channel structures	0x4029 8000	84	0x40	2	8

(表格续下页.....)

6 外设 I/O 映射

表 12 (续) CYT2CL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	group	slave
M-DMA	M-DMA0 Controller	0x402A 0000				
	M-DMA0 channels	0x402A 1000	4	0x100	2	9
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	10
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	20	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	20	0x80	3	1
SMARTIO	Programmable I/O configuration	0x4032 0000			3	2
	SMART I/O port configuration	0x4032 0C00	1	0x100		
	Timer/Counter/PWM 0 (TCPWM0)	0x4038 0000				
TCPWM	TCPWM0 group #0 (16-bit)	0x4038 0000	34	0x80	3	3
	TCPWM0 group #1 (16-bit, Motor control)	0x4038 8000	12	0x80		
	TCPWM0 group #2 (32-bit)	0x4039 0000	16	0x80		
LCD	LCD Controller	0x403B 0000			3	4
	LCD Data	0x403B 0100	4	0x100		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	5
	Event generator 0 comparator structures	0x403F 0800	16	0x20		
SMIF	Serial Memory Interface 0 (SMIF0)	0x4042 0000			4	0
	SMIF0 Devices	0x4042 0800	2	0x80		
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	2	0x100		
	Clock Extension Peripheral Interface 0 (CXPI0)	0x4051 0000			5	1
CXPI	CXPI0 Channels	0x4051 8000	2	0x100		
TTCANFD	CAN0 controller	0x4052 0000	2	0x200	5	2
	Message RAM CAN0	0x4053 0000		0x2000		
	CAN1 controller	0x4054 0000	2	0x200	5	3
	Message RAM CAN1	0x4055 0000		0x2000		
	Serial Communications Block (SPI/UART/I2C)	0x4060 0000	12	0x10000	6	0-11
SCB	Time Division Multiplexer 0 (TDM0)	0x4081 0000			8	0
Sound	TDM0 Structures	0x4081 8000	2	0x200		
	Sound Generator 0 (SG0)	0x4082 0000				
	SG0 Structures	0x4082 8000	5	0x100	8	1

(表格续下页.....)

6 外设 I/O 映射

表 12 (续) CYT2CL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	group	slave
	Pulse Width Modulation 0 (PWM0)	0x4083 0000				
	PWM0 Structures	0x4083 8000	2	0x100	8	2
	Mixer0	0x4088 0000				
	Mixer0 Source Structures	0x4088 8000	5	0x100	8	4
	Mixer0 Destination Structures	0x4088 C000	1			
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR0 channel structures	0x4090 0800	24	0x40		
	SAR1 channel structures	0x4090 1800	24	0x40		

- 1) 这六个可编程 PPU 由 Boot ROM 配置，并根据访问权限供用户使用。请参阅特定于设备的 TRM 以了解有关这些可编程 PPU 的配置的更多信息。

7 CYT2CL 时钟图

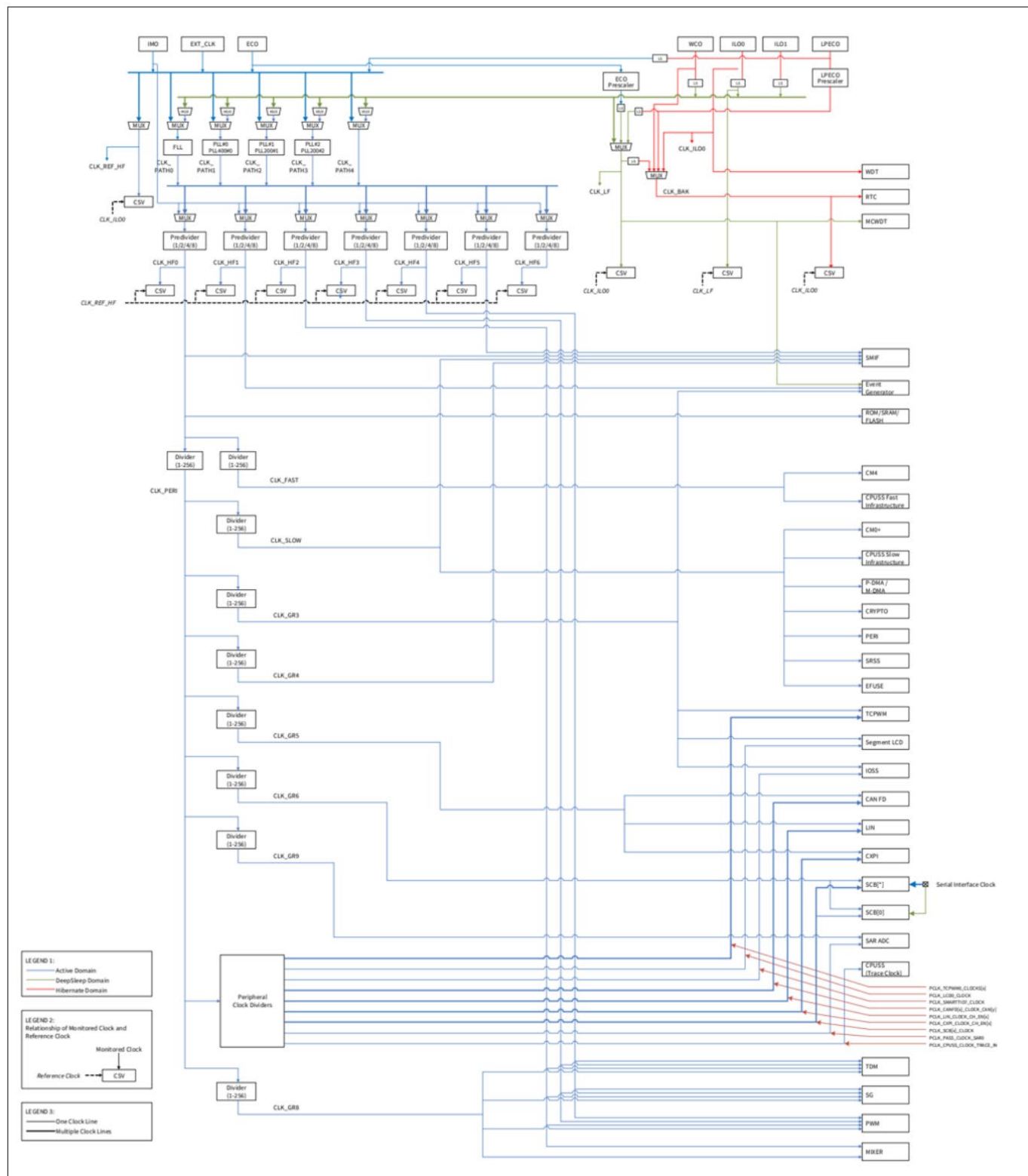


图 3 **CYT2CL 时钟图**

8 CYT2CL CPU 启动序列

以下步骤描述了启动序列：

1. 系统复位 (@0x0000 0000)
2. CM0+ 执行 ROM 启动 (@0x0000 0004)
 - a. 应用调整
 - b. 根据 eFuse 和监督闪存中的内容，应用调试访问端口 (DAP) 访问限制和系统保护
 - c. 验证闪存启动 (仅在安全生命周期阶段) 并将控制权转移给闪存启动
3. CM0+ 执行闪存启动 (来自监督闪存 @0x1700 2000)
 - a. 调试引脚根据 SWD/JTAG 规范配置 ¹³⁾
 - b. 将 CM0+ 向量表基址寄存器 (CPUSS_CM0_VECTOR_TABLE_BASE - CPU 子系统的一部分) 设置为闪存起始位置 (@0x1000 0000)
 - c. CM0+ 分支到其复位处理程序
4. CM0+ 开始执行
 - a. 将 CM0+ 向量表移至 SRAM (更新 CM0+ 向量表基址)
 - b. 将 CM4_VECTOR_TABLE_BASE (@0x0000 0200) 设置为闪存中提到的 CM4 向量表的位置 (在 CM4 linker definition 文件中指定)。
 - c. 从复位释放 CM4
 - d. 继续执行 CM0+ 用户应用程序
5. CM4 直接从代码闪存或 SRAM 执行
 - a. CM4 分支到其复位处理程序
 - b. 继续执行 CM4 用户应用程序

¹³⁾ 在启动完成后 SWD/JTAG 引脚的端口配置将从默认的 GPIO 模式更改为支持调试，参见表 14 了解引脚分配。

9 引脚分配

9 引脚分配

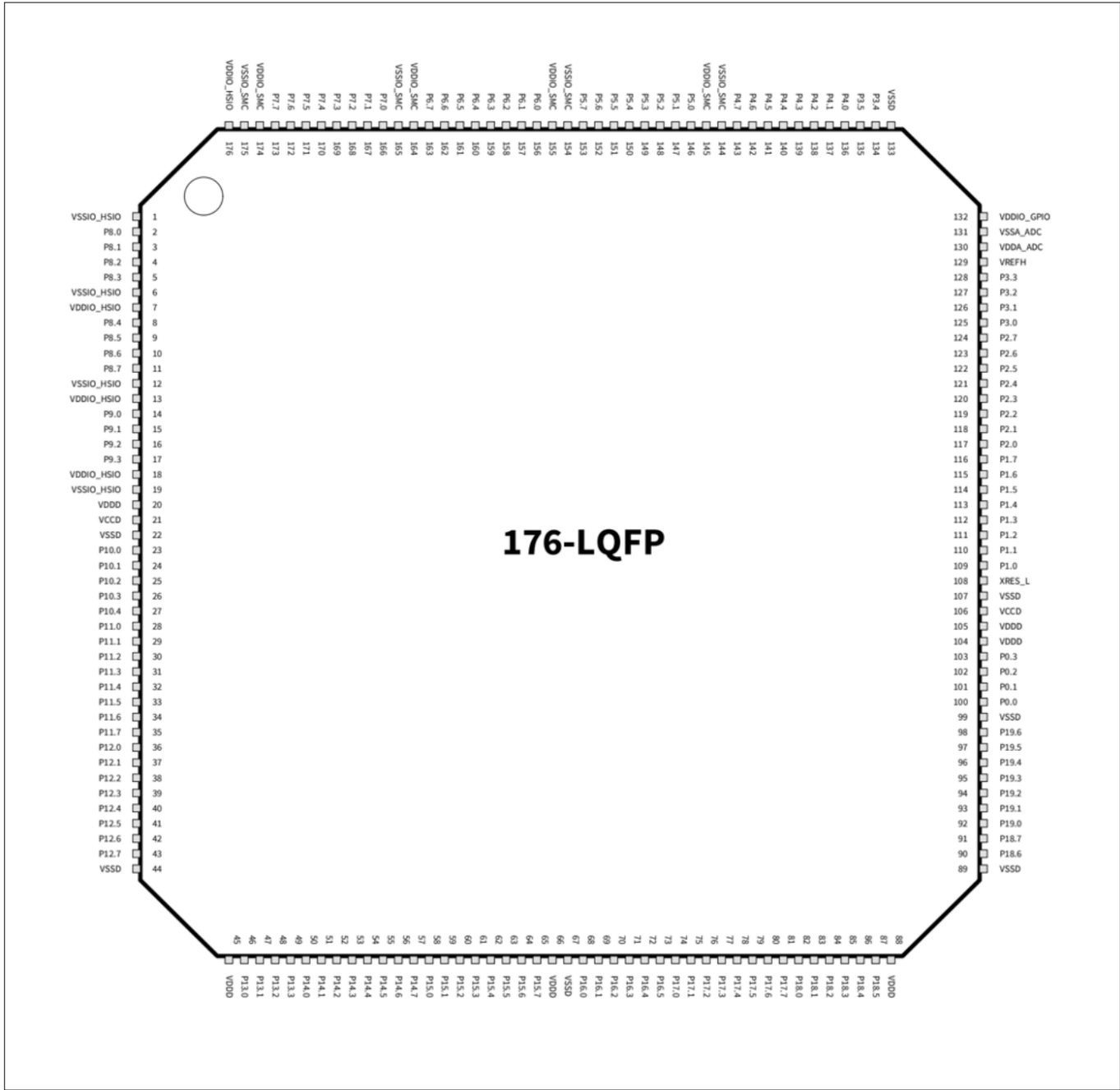


图 4 176-LQFP 引脚分配

9 引脚分配

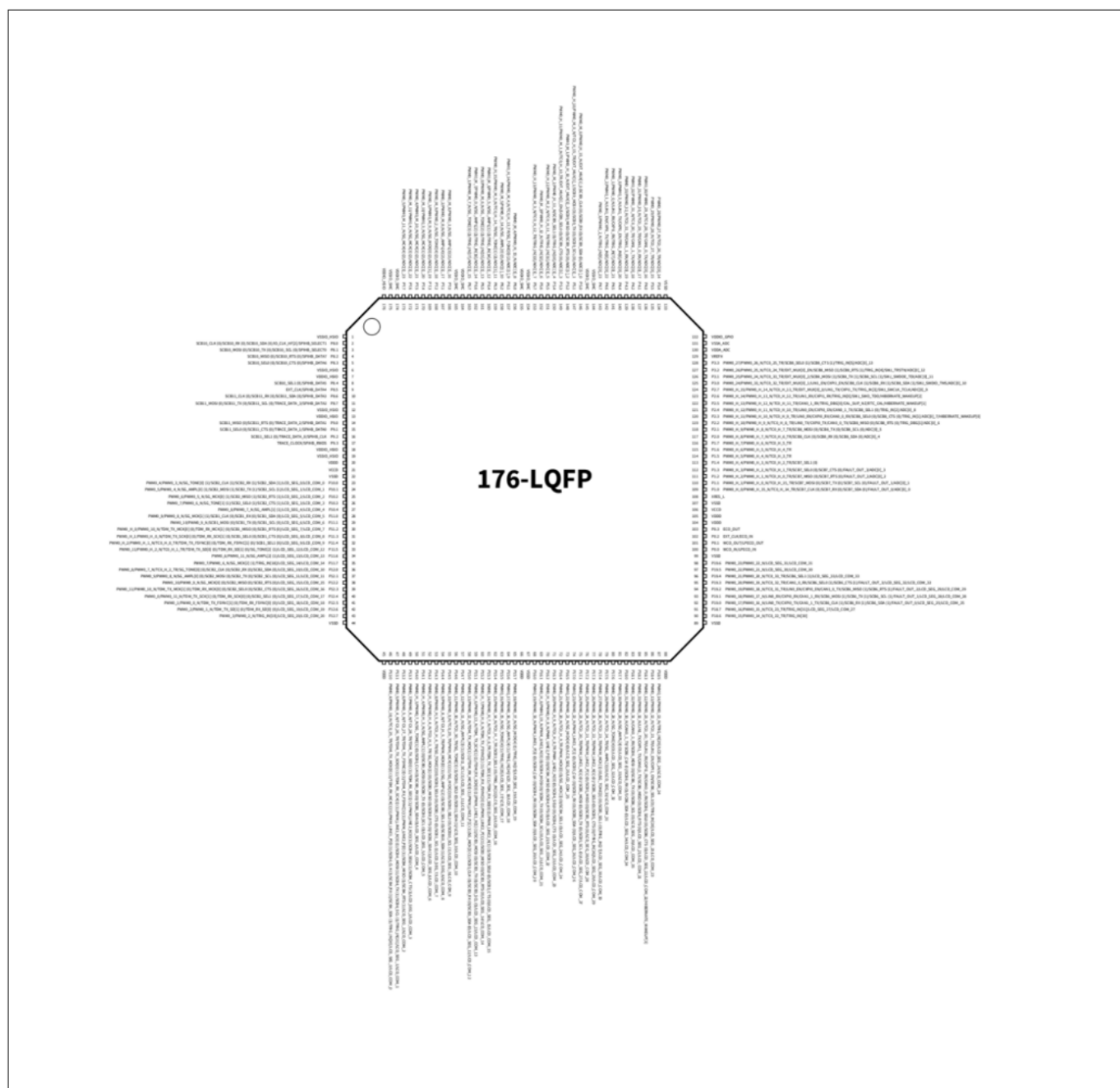


图 5 176-LQFP 引脚分配及复用功能

图 6 **144-LQFP 引脚分配**

9 引脚分配

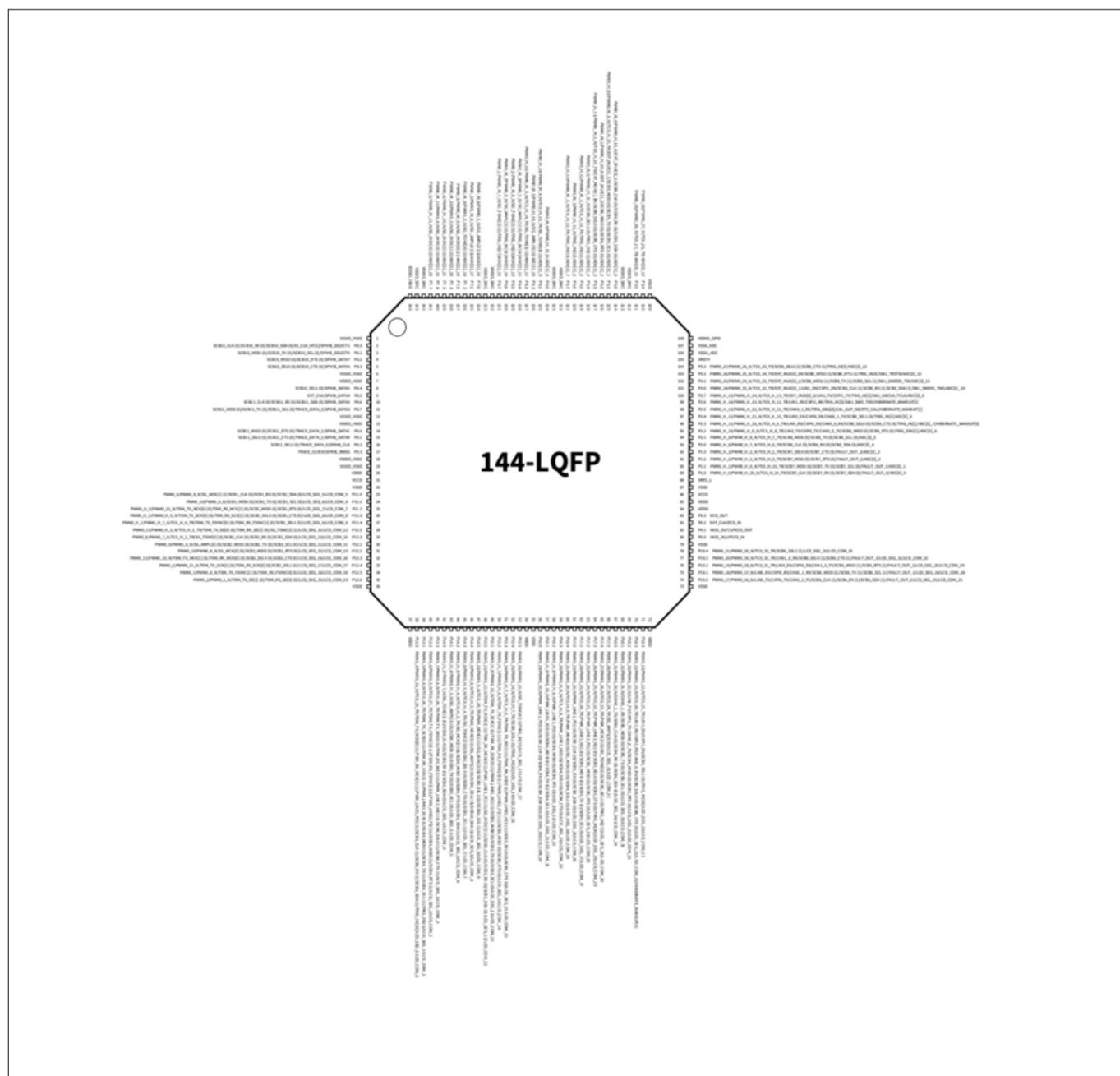


图 7 144-LQFP 引脚分配及复用功能

10 高速 I/O 矩阵连接

表 13 HSIOM 连接参考

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7

11 封装引脚列表和备用功能

大多数引脚具有备用功能，如表 14 所示。

表 14 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9		
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5		
P0.0	100	80	GPIO_ST D							WCO_IN, LPECO_IN ⁶⁾	Not supported
P0.1	101	81	GPIO_ST D							WCO_OUT, LPECO_OUT ⁶⁾	
P0.2	102	82	GPIO_ST D							ECO_IN ⁶⁾	
P0.3	103	83	GPIO_ST D							ECO_OUT ⁶⁾	
P1.0	109	89	GPIO_ST D							ADC[0]_0	Supported
P1.1	110	90	GPIO_ST D							ADC[0]_1	
P1.2	111	91	GPIO_ST D							ADC[0]_2	
P1.3	112	92	GPIO_ST D							ADC[0]_3	
P1.4	113	NA	GPIO_ST D								Supported
P1.5	114	NA	GPIO_ST D								
P1.6	115	NA	GPIO_ST D								

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P1.7	116	NA	GPIO_ST D								
P2.0	117	93	GPIO_ST D						ADC[0]_4		Supported
P2.1	118	94	GPIO_ST D						ADC[0]_5		
P2.2	119	95	GPIO_ST D						ADC[0]_6		
P2.3	120	96	GPIO_ST D						ADC[0]_7 HIBERNATE_WAKEU P[0]		
P2.4	121	97	GPIO_ST D						ADC[0]_8		Not supported
P2.5	122	98	GPIO_ST D					RTC_CAL	HIBERNATE_WAKEU P[1]		
P2.6	123	99	GPIO_ST D					SWJ_SW O_TDO	HIBERNATE_WAKEU P[2]		
P2.7	124	100	GPIO_ST D					SWJ_SW CLK_TC LK	ADC[0]_9		Supported
P3.0	125	101	GPIO_ST D					SWJ_SW DIO_TMS	ADC[0]_10		

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P3.1	126	102	GPIO_ST D					SWJ_SW DOE_TDI	ADC[0]_11		
P3.2	127	103	GPIO_ST D					SWJ_TRS TN	ADC[0]_12		
P3.3	128	104	GPIO_ST D						ADC[0]_13		
P3.4	134	110	GPIO_ST D						ADC[0]_14		
P3.5	135	111	GPIO_ST D						ADC[0]_15		
P4.0	136	NA	GPIO_ST D						ADC[0]_16		Supported
P4.1	137	NA	GPIO_ST D						ADC[0]_17		
P4.2	138	NA	GPIO_ST D						ADC[0]_18		
P4.3	139	NA	GPIO_ST D						ADC[0]_19		
P4.4	140	NA	GPIO_ST D						ADC[0]_20		
P4.5	141	NA	GPIO_ST D						ADC[0]_21		

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P4.6	142	NA	GPIO_ST D						ADC[0]_22		
P4.7	143	NA	GPIO_ST D						ADC[0]_23		
P5.0	146	114	GPIO_SM C						ADC[1]_0		Supported
P5.1	147	115	GPIO_SM C						ADC[1]_1		
P5.2	148	116	GPIO_SM C						ADC[1]_2		
P5.3	149	117	GPIO_SM C						ADC[1]_3		
P5.4	150	118	GPIO_SM C						ADC[1]_4		
P5.5	151	119	GPIO_SM C						ADC[1]_5		
P5.6	152	120	GPIO_SM C						ADC[1]_6		
P5.7	153	121	GPIO_SM C						ADC[1]_7		
P6.0	156	124	GPIO_SM C						ADC[1]_8		Supported

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P6.1	157	125	GPIO_SM C						ADC[1]_9		
P6.2	158	126	GPIO_SM C						ADC[1]_10		
P6.3	159	127	GPIO_SM C						ADC[1]_11		
P6.4	160	128	GPIO_SM C						ADC[1]_12		
P6.5	161	129	GPIO_SM C						ADC[1]_13		
P6.6	162	130	GPIO_SM C						ADC[1]_14		
P6.7	163	131	GPIO_SM C						ADC[1]_15		
P7.0	166	134	GPIO_SM C						ADC[1]_16	SMARTI 07_0	
P7.1	167	135	GPIO_SM C						ADC[1]_17	SMARTI 07_1	
P7.2	168	136	GPIO_SM C						ADC[1]_18	SMARTI 07_2	
P7.3	169	137	GPIO_SM C						ADC[1]_19	SMARTI 07_3	

(表格续下页……)

11 封装引脚列表和备用功能

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P7.4	170	138	GPIO_SM C						ADC[1]_20	SMARTI O7_4	
P7.5	171	139	GPIO_SM C						ADC[1]_21	SMARTI O7_5	
P7.6	172	140	GPIO_SM C						ADC[1]_22	SMARTI O7_6	
P7.7	173	141	GPIO_SM C						ADC[1]_23	SMARTI O7_7	
P8.0	2	2	HSIO_ST DLN								Not supported
P8.1	3	3	HSIO_ST DLN								
P8.2	4	4	HSIO_ST DLN								
P8.3	5	5	HSIO_ST DLN								
P8.4	8	8	HSIO_ST DLN								
P8.5	9	9	HSIO_ST DLN								
P8.6	10	10	HSIO_ST DLN								

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9			
	Pin	Pin		DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5			
P8.7	11	11	HSIO_ST DLN								
P9.0	14	14	HSIO_ST DLN								
P9.1	15	15	HSIO_ST DLN								
P9.2	16	16	HSIO_ST DLN								
P9.3	17	17	HSIO_ST DLN								
P10.0	23	NA	GPIO_ST D	LCD_SEG _0	LCD_CO M_0						Supported
P10.1	24	NA	GPIO_ST D	LCD_SEG _1	LCD_CO M_1						
P10.2	25	NA	GPIO_ST D	LCD_SEG _2	LCD_CO M_2						
P10.3	26	NA	GPIO_ST D	LCD_SEG _3	LCD_CO M_3						
P10.4	27	NA	GPIO_ST D	LCD_SEG _4	LCD_CO M_4						
P11.0	28	23	GPIO_ST D	LCD_SEG _5	LCD_CO M_5						

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9		
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5		
P11.1	29	24	GPIO_ST D	LCD_SEG _6	LCD_CO M_6						
P11.2	30	25	GPIO_ST D	LCD_SEG _7	LCD_CO M_7						
P11.3	31	26	GPIO_ST D	LCD_SEG _8	LCD_CO M_8						
P11.4	32	27	GPIO_ST D	LCD_SEG _9	LCD_CO M_9						
P11.5	33	28	GPIO_ST D	LCD_SEG _12	LCD_CO M_12						
P11.6	34	NA	GPIO_ST D	LCD_SEG _13	LCD_CO M_13						
P11.7	35	NA	GPIO_ST D	LCD_SEG _14	LCD_CO M_14						
P12.0	36	29	GPIO_ST D	LCD_SEG _10	LCD_CO M_10						
P12.1	37	30	GPIO_ST D	LCD_SEG _11	LCD_CO M_11						
P12.2	38	31	GPIO_ST D	LCD_SEG _15	LCD_CO M_15						
P12.3	39	32	GPIO_ST D	LCD_SEG _16	LCD_CO M_16						

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9		
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5		
P12.4	40	33	GPIO_ST D	LCD_SEG _17	LCD_CO M_17						
P12.5	41	34	GPIO_ST D	LCD_SEG _18	LCD_CO M_18						
P12.6	42	35	GPIO_ST D	LCD_SEG _19	LCD_CO M_19						
P12.7	43	NA	GPIO_ST D	LCD_SEG _20	LCD_CO M_20						
P13.0	46	38	GPIO_ST D	LCD_SEG _0	LCD_CO M_0						
P13.1	47	39	GPIO_ST D	LCD_SEG _1	LCD_CO M_1						
P13.2	48	40	GPIO_ST D	LCD_SEG _2	LCD_CO M_2						
P13.3	49	41	GPIO_ST D	LCD_SEG _3	LCD_CO M_3						
P14.0	50	42	GPIO_EN H	LCD_SEG _4	LCD_CO M_4	SCB0_CL K (0)	SCB0_SD A (0)				
P14.1	51	43	GPIO_EN H	LCD_SEG _5	LCD_CO M_5	SCB0_M OSI (0)	SCB0_SC L (0)				
P14.2	52	44	GPIO_EN H	LCD_SEG _6	LCD_CO M_6	SCB0_MI SO (0)					

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9		
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5		
P14.3	53	45	GPIO_EN H	LCD_SEG _7	LCD_CO M_7	SCB0_SE L0 (0)					
P14.4	54	46	GPIO_EN H	LCD_SEG _8	LCD_CO M_8	SCB0_SE L1 (0)					
P14.5	55	47	GPIO_EN H	LCD_SEG _9	LCD_CO M_9	SCB0_SE L2 (0)					
P14.6	56	NA	GPIO_EN H	LCD_SEG _10	LCD_CO M_10	SCB0_SE L3 (0)					
P14.7	57	NA	GPIO_EN H	LCD_SEG _11	LCD_CO M_11						
P15.0	58	48	GPIO_ST D	LCD_SEG _12	LCD_CO M_12						
P15.1	59	49	GPIO_ST D	LCD_SEG _13	LCD_CO M_13						
P15.2	60	50	GPIO_ST D	LCD_SEG _14	LCD_CO M_14						
P15.3	61	51	GPIO_ST D	LCD_SEG _15	LCD_CO M_15						
P15.4	62	52	GPIO_ST D	LCD_SEG _16	LCD_CO M_16						
P15.5	63	53	GPIO_ST D	LCD_SEG _17	LCD_CO M_17						

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5			
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3			
P15.6	64	NA	GPIO_ST D	LCD_SEG _18	LCD_CO M_18						
P15.7	65	NA	GPIO_ST D	LCD_SEG _19	LCD_CO M_19						
P16.0	68	56	GPIO_ST D	LCD_SEG _20	LCD_CO M_20						
P16.1	69	57	GPIO_ST D	LCD_SEG _21	LCD_CO M_21						
P16.2	70	58	GPIO_ST D	LCD_SEG _22	LCD_CO M_22						
P16.3	71	59	GPIO_ST D	LCD_SEG _23	LCD_CO M_23						
P16.4	72	60	GPIO_ST D	LCD_SEG _24	LCD_CO M_24						
P16.5	73	NA	GPIO_ST D	LCD_SEG _25	LCD_CO M_25						
P17.0	74	61	GPIO_ST D	LCD_SEG _26	LCD_CO M_26						
P17.1	75	62	GPIO_ST D	LCD_SEG _27	LCD_CO M_27						
P17.2	76	63	GPIO_ST D	LCD_SEG _28	LCD_CO M_28						

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5	HCon#2 9		
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3	DS#5		
P17.3	77	64	GPIO_ST D	LCD_SEG _29	LCD_CO M_29						
P17.4	78	65	GPIO_ST D	LCD_SEG _30	LCD_CO M_30						
P17.5	79	66	GPIO_ST D	LCD_SEG _31	LCD_CO M_31						
P17.6	80	NA	GPIO_ST D	LCD_SEG _32	LCD_CO M_32						
P17.7	81	NA	GPIO_ST D	LCD_SEG _33	LCD_CO M_33						
P18.0	82	67	GPIO_ST D	LCD_SEG _34	LCD_CO M_34						
P18.1	83	68	GPIO_ST D	LCD_SEG _35	LCD_CO M_35						
P18.2	84	69	GPIO_ST D	LCD_SEG _21	LCD_CO M_21						
P18.3	85	70	GPIO_ST D	LCD_SEG _22	LCD_CO M_22				HIBERNATE_WAKEUP[3]		
P18.4	86	71	GPIO_ST D	LCD_SEG _23	LCD_CO M_23						
P18.5	87	NA	GPIO_ST D	LCD_SEG _24	LCD_CO M_24						

(表格续下页……)

表 14 (续) 深度睡眠 (DS) 模式、模拟、智能 I/O¹⁾ 下的引脚选择器和备用引脚功能

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O	+B input ²⁾
	176-LQFP	144-LQFP		HCon#0	HCon#1 2 ³⁾	HCon#1 3	HCon#1 4	HCon#1 5			
	Pin	Pin			DS#0 ⁴⁾ , ⁵⁾	DS#1	DS#2	DS#3			
P18.6 ⁷⁾	90	NA	GPIO_ST D								Not supported
P18.7	91	NA	GPIO_ST D	LCD_SEG _27	LCD_CO M_27						Supported
P19.0	92	74	GPIO_ST D	LCD_SEG _25	LCD_CO M_25						
P19.1	93	75	GPIO_ST D	LCD_SEG _28	LCD_CO M_28						
P19.2	94	76	GPIO_ST D	LCD_SEG _29	LCD_CO M_29						
P19.3	95	77	GPIO_ST D	LCD_SEG _32	LCD_CO M_32						
P19.4	96	78	GPIO_ST D	LCD_SEG _33	LCD_CO M_33						
P19.5	97	NA	GPIO_ST D	LCD_SEG _30	LCD_CO M_30						
P19.6	98	NA	GPIO_ST D	LCD_SEG _31	LCD_CO M_31						
XRES_L	108	88									Not supported

1) 对于任何标有标识符 (n) 的功能, AC 时序仅在相应的组“n”内得到保证。

2) 有关 +B 条件和钳位电流规格, 请参阅绝对最大额定值章节。

3) 高速 I/O 矩阵连接 (HCon) 基准请参见表 13。

4) 深度睡眠排序 (DS#0、DS#1、DS#2) 对选择任何备用功能没有任何影响; HSIOM 模块负责处理各个备用功能的分配。

5) 所有在深度睡眠模式下可用的端口引脚功能在工作模式下也可用。

11 封装引脚列表和备用功能

- 6) 如果振荡器是启用的，则支持振荡器功能（WCO 或 ECO）的 I/O 引脚必须配置为高阻。
 - 7) 当 VDDD 低于 POR 阈值时，此 I/O 将出现增大的对地漏电流。
-

12 电源引脚分配

12 电源引脚分配

表 15 电源引脚分配

Name	Package		Remarks
	176-LQFP	144-LQFP	
VDDD	105, 104, 88, 66, 45, 20	85, 84, 72, 54, 37, 20	Main digital supply
VSS	133, 107, 99, 89, 67, 44, 22	109, 87, 79, 73, 55, 36, 22	Main digital ground
VDDIO_GPIO	132	108	Supply for GPIO_STD (2.7 - 5.5 V)
VDDIO_HSIO	176, 18, 13, 7	144, 18, 13, 7	Supply for HSIO_STDLN (3.0 - 3.6 V)
VSSIO_HSIO	19, 12, 6, 1	19, 12, 6, 1	HSIO_STDLN ground
VDDIO_SMC	174, 164, 155, 145	142, 132, 123, 113	Supply for GPIO_SMC (2.7 - 5.5 V)
VSSIO_SMC	175, 165, 154, 144	143, 133, 122, 112	GPIO_SMC ground
VCCD ¹⁾	106, 21	86, 21	Main regulated supply. Driven by LDO regulator
VREFH	129	105	High reference voltage for SAR
VDDA_ADC	130	106	Main analog supply (for PASS/SAR)
VSSA_ADC	131	107	Main analog ground (VREFL is shared with VSSA_ADC)

1) V_{CCD} 引脚必须连接在一起，以确保低阻抗连接。（参见图 11 中的要求）。

13 备用功能引脚分配

13 备用功能引脚分配

表 16 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P0.0															
P0.1															
P0.2														EXT_C LK	
P0.3															
P1.0	PWM0_ H_0	PWM0_ H_15_ N	TC0_H _14_TR							SCB7_ CLK (0)	SCB7_ RX (0)	SCB7_ SDA (0) ³⁾			FAULT _ OUT_0
P1.1	PWM0_ H_1	PWM0_ H_0_N	TC0_H _15_TR							SCB7_ MOSI (0)	SCB7_ TX (0)	SCB7_ SCL (0) ³⁾			FAULT _ OUT_1
P1.2	PWM0_ H_2	PWM0_ H_1_N	TC0_H _0_TR							SCB7_ MISO (0)	SCB7_ RTS (0)				FAULT _ OUT_2
P1.3	PWM0_ H_3	PWM0_ H_2_N	TC0_H _1_TR							SCB7_ SEL0 (0)	SCB7_ CTS (0)				FAULT _ OUT_3
P1.4	PWM0_ H_4	PWM0_ H_3_N	TC0_H _2_TR							SCB7_ SEL1 (0)					
P1.5	PWM0_ H_5	PWM0_ H_4_N	TC0_H _3_TR												
P1.6	PWM0_ H_6	PWM0_ H_5_N	TC0_H _4_TR												

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P1.7	PWM0_H_7	PWM0_H_6_N	TC0_H_5_TR												
P2.0	PWM0_H_8	PWM0_H_7_N	TC0_H_6_TR							SCB8_CLK (0)	SCB8_RX (0)	SCB8_SDA (0) ³⁾			
P2.1	PWM0_H_9	PWM0_H_8_N	TC0_H_7_TR							SCB8_MOSI (0)	SCB8_TX (0)	SCB8_SCL (0) ³⁾			
P2.2	PWM0_H_10	PWM0_H_9_N	TC0_H_8_TR		LIN0_TX	CXPI0_TX	CAN0_0_TX			SCB8_MISO (0)	SCB8_RTS (0)		TRIG_DBG[1]		
P2.3	PWM0_H_11	PWM0_H_10_N	TC0_H_9_TR		LIN0_RX	CXPI0_RX	CAN0_0_RX			SCB8_SEL0 (0)	SCB8_CTS (0)		TRIG_IN[1]		
P2.4	PWM0_H_12	PWM0_H_11_N	TC0_H_10_TR		LIN0_EN	CXPI0_EN	CAN0_1_TX			SCB8_SEL1 (0)			TRIG_IN[2]		
P2.5	PWM0_H_13	PWM0_H_12_N	TC0_H_11_TR				CAN0_1_RX						TRIG_DBG[0]		CAL_SUP_NZ
P2.6	PWM0_H_14	PWM0_H_13_N	TC0_H_12_TR		LIN1_RX	CXPI1_RX							TRIG_IN[0]		

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P2.7	PWM0_H_15	PWM0_H_14_N	TC0_H_13_TR	EXT_MUX[0]_0	LIN1_TX	CXPI1_TX							TRIG_IN[3]		
P3.0	PWM0_24	PWM0_33_N	TC0_32_TR	EXT_MUX[0]_1	LIN1_EN	CXPI1_EN				SCB8_CLK (1)	SCB8_RX (1)	SCB8_SDA (1) ³⁾			
P3.1	PWM0_25	PWM0_24_N	TC0_33_TR	EXT_MUX[0]_2						SCB8_MOSI (1)	SCB8_TX (1)	SCB8_SCL (1) ³⁾			
P3.2	PWM0_26	PWM0_25_N	TC0_24_TR	EXT_MUX[0]_EN						SCB8_MISO (1)	SCB8_RTS (1)		TRIG_IN[4]		
P3.3	PWM0_27	PWM0_26_N	TC0_25_TR							SCB8_SELO (1)	SCB8_CTS (1)		TRIG_IN[5]		
P3.4	PWM0_28	PWM0_27_N	TC0_26_TR												
P3.5	PWM0_29	PWM0_28_N	TC0_27_TR												
P4.0	PWM0_30	PWM0_29_N	TC0_28_TR				CAN1_0_TX								
P4.1	PWM0_31	PWM0_30_N	TC0_29_TR				CAN1_0_RX								

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P4.2	PWM0_32	PWM0_31_N	TC0_30_TR				CAN1_1_TX								
P4.3	PWM0_33	PWM0_32_N	TC0_31_TR				CAN1_1_RX								
P4.4	PWM0_0	PWM0_3_N			LIN1_TX	CXPI1_EN							TRIG_IN[6]		
P4.5	PWM0_1	PWM0_0_N			LIN1_RX	CXPI1_RX							TRIG_IN[7]		
P4.6	PWM0_2	PWM0_1_N			LIN1_EN	CXPI1_TX							TRIG_IN[8]		
P4.7	PWM0_3	PWM0_2_N											TRIG_IN[9]		
P5.0	PWM0_M_0	PWM0_H_15_N		EXT_MUX[1]_0						SCB9_CLK (0)	SCB9_RX (0)	SCB9_SDA (0) ³⁾			
P5.1	PWM0_H_10	PWM0_M_0_N	TC0_H_15_TR	EXT_MUX[1]_1						SCB9_MOSI (0)	SCB9_TX (0)	SCB9_SCL (0) ³⁾			
P5.2	PWM0_M_1	PWM0_H_10_N		EXT_MUX[1]_2						SCB9_MISO (0)	SCB9_RTS (0)				
P5.3	PWM0_H_11	PWM0_M_1_N	TC0_H_10_TR	EXT_MUX[1]_EN						SCB9_SEL0 (0)	SCB9_CTS (0)				

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P5.4	PWM0_M_2	PWM0_H_11_N								SCB9_SEL1 (0)			TRIG_IN[10]		
P5.5	PWM0_H_12	PWM0_M_2_N	TC0_H_11_TR										TRIG_IN[11]		
P5.6	PWM0_M_3	PWM0_H_12_N											TRIG_IN[12]		
P5.7	PWM0_H_13	PWM0_M_3_N	TC0_H_12_TR										TRIG_IN[13]		
P6.0	PWM0_M_4	PWM0_H_13_N													
P6.1	PWM0_H_14	PWM0_M_4_N	TC0_H_13_TR						SG_TO_NE[0] (2)						
P6.2	PWM0_M_5	PWM0_H_14_N							SG_AMPL[0] (2)						
P6.3	PWM0_H_15	PWM0_M_5_N	TC0_H_14_TR						SG_TO_NE[1] (2)						

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P6.4	PWM0_M_6	PWM0_5_N							SG_AMPL[1] (2)				TRIG_IN[14]		
P6.5	PWM0_0	PWM0_M_6_N							SG_TO NE[2] (2)				TRIG_IN[15]		
P6.6	PWM0_M_7	PWM0_0_N							SG_AMPL[2] (2)				TRIG_IN[16]		
P6.7	PWM0_1	PWM0_M_7_N							SG_TO NE[3] (2)				TRIG_IN[17]		
P7.0	PWM0_M_8	PWM0_1_N							SG_AMPL[3] (2)						
P7.1	PWM0_2	PWM0_M_8_N							SG_AMPL[4] (2)						
P7.2	PWM0_M_9	PWM0_2_N							SG_TO NE[4] (2)						
P7.3	PWM0_3	PWM0_M_9_N							SG_MCK[0] (2)						

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P7.4	PWM0_M_10	PWM0_3_N							SG_MCK[1] (2)						
P7.5	PWM0_4	PWM0_M_10_N							SG_MCK[2] (2)						
P7.6	PWM0_M_11	PWM0_4_N							SG_MCK[3] (2)						
P7.7	PWM0_5	PWM0_M_11_N							SG_MCK[4] (2)						
P8.0										SCB10_CLK (0)	SCB10_RX (0)	SCB10_SDA (0) ³⁾		IO_CLK_HF[2]	SPIHB_SELECT 1
P8.1										SCB10_MOSI (0)	SCB10_TX (0)	SCB10_SCL (0) ³⁾			SPIHB_SELECT 0
P8.2										SCB10_MISO (0)	SCB10_RTS (0)				SPIHB_DATA7
P8.3										SCB10_SELO (0)	SCB10_CTS (0)				SPIHB_DATA6

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping															
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27	
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15	
P8.4										SCB10_ SEL1 (0)					SPIHB_ DATA5	
P8.5														EXT_ CLK	SPIHB_ DATA4	
P8.6										SCB11_ CLK (0)	SCB11_ RX (0)	SCB11_ SDA (0) ³⁾			SPIHB_ DATA3	
P8.7										SCB11_ MOSI (0)	SCB11_ TX (0)	SCB11_ _ SCL (0) ³⁾		TRACE_ DATA_ 3	SPIHB_ DATA2	
P9.0										SCB11_ MISO (0)	SCB11_ RTS (0)			TRACE_ DATA_ 2	SPIHB_ DATA1	
P9.1										SCB11_ _ SEL0 (0)	SCB11_ CTS (0)			TRACE_ DATA_ 1	SPIHB_ DATA0	
P9.2										SCB11_ _ SEL1 (0)				TRACE_ DATA_ 0	SPIHB_ _ CLK	
P9.3														TRACE_ CCLK	SPIHB_ RWDS	

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P10.0	PWM0_4	PWM0_3_N							SG_TO NE[0] (1)	SCB2_ CLK (1)	SCB2_ RX (1)	SCB2_ SDA (1) ³⁾			
P10.1	PWM0_5	PWM0_4_N							SG_AM PL[0] (1)	SCB2_ MOSI (1)	SCB2_ TX (1)	SCB2_ SCL (1) ³⁾			
P10.2	PWM0_6	PWM0_5_N							SG_MC K[0] (1)	SCB2_ MISO (1)	SCB2_ RTS (1)				
P10.3	PWM0_7	PWM0_6_N							SG_TO NE[1] (1)	SCB2_ SEL0 (1)	SCB2_ CTS (1)				
P10.4	PWM0_8	PWM0_7_N							SG_AM PL[1] (1)						
P11.0	PWM0_9	PWM0_8_N							SG_MC K[1] (1)	SCB1_ CLK (0)	SCB1_ RX (0)	SCB1_ SDA (0) ³⁾			
P11.1	PWM0_10	PWM0_9_N								SCB1_ MOSI (0)	SCB1_ TX (0)	SCB1_ SCL (0) ³⁾			
P11.2	PWM0_H_0	PWM0_10_N			TDM_T X_MCK[0] (0)	TDM_R X_MCK[1] (0)				SCB1_ MISO (0)	SCB1_ RTS (0)				

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P11.3	PWM0_H_1	PWM0_H_0_N			TDM_TX_SCK[0] (0)	TDM_RX_SCK[1] (0)				SCB1_SEL0 (0)	SCB1_CTS (0)				
P11.4	PWM0_H_2	PWM0_H_1_N	TC0_H_0_TR		TDM_TX_FSYNC[0] (0)	TDM_RX_FSYNC[1] (0)				SCB1_SEL1 (0)					
P11.5	PWM0_11	PWM0_H_2_N	TC0_H_1_TR		TDM_TX_SD[0] (0)	TDM_RX_SD[1] (0)			SG_TONE[2] (1)						
P11.6	PWM0_6	PWM0_11_N							SGAMPL[2] (1)						
P11.7	PWM0_7	PWM0_6_N							SG_MCK[2] (1)				TRIG_IN[18]		
P12.0	PWM0_8	PWM0_7_N	TC0_H_2_TR						SG_TONE[0] (0)	SCB2_CLK (0)	SCB2_RX (0)	SCB2_SDA (0) ³⁾			
P12.1	PWM0_9	PWM0_8_N							SGAMPL[0] (0)	SCB2_MOSI (0)	SCB2_TX (0)	SCB2_SCL (0) ³⁾			
P12.2	PWM0_10	PWM0_9_N							SG_MCK[0] (0)	SCB2_MISO (0)	SCB2_RTS (0)				

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P12.3	PWM0_11	PWM0_10_N			TDM_TX_MCK[1] (0)	TDM_RX_MCK[0] (0)				SCB2_SEL0 (0)	SCB2_CTS (0)				
P12.4	PWM0_0	PWM0_11_N			TDM_TX_SCK[1] (0)	TDM_RX_SCK[0] (0)				SCB2_SEL1 (0)					
P12.5	PWM0_1	PWM0_0_N			TDM_TX_FSYNC[1] (0)	TDM_RX_FSYNC[0] (0)									
P12.6	PWM0_2	PWM0_1_N			TDM_TX_SD[1] (0)	TDM_RX_SD[0] (0)									
P12.7	PWM0_3	PWM0_2_N											TRIG_IN[19]		
P13.0	PWM0_4	PWM0_18_N	TC0_25_TR		TDM_TX_MCK[0] (1)	TDM_RX_MCK[1] (1)		PWM_LINE1_P[0] (1)		SCB4_CLK (1)	SCB4_RX (1)	SCB4_SDA (1) ³⁾	TRIG_IN[20]		
P13.1	PWM0_5	PWM0_4_N	TC0_26_TR		TDM_TX_SCK[0] (1)	TDM_RX_SCK[1] (1)		PWM_LINE1_N[0] (1)		SCB4_MOSI (1)	SCB4_TX (1)	SCB4_SCL (1) ³⁾	TRIG_IN[21]		
P13.2	PWM0_6	PWM0_5_N	TC0_27_TR		TDM_TX_FSYNC[0] (1)	TDM_RX_FSYNC[1] (1)		PWM_LINE2_P[0] (1)		SCB4_MISO (1)	SCB4_RTS (1)				

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P13.3	PWM0_7	PWM0_6_N	TC0_28_TR		TDM_TX_SD[0] (1)	TDM_RX_SD[1] (1)		PWM_LINE2_N[0] (1)		SCB4_SEL0 (1)	SCB4_CTS (1)				
P14.0	PWM0_H_3	PWM0_7_N							SG_TONE[1] (0)		SCB0_RX (0)				
P14.1	PWM0_H_4	PWM0_H_3_N							SG_AMPL[1] (0)		SCB0_TX (0)				
P14.2	PWM0_H_5	PWM0_H_4_N	TC0_H_3_TR						SG_MCK[1] (0)		SCB0_RTS (0)	SCB1_SDA (1)			
P14.3	PWM0_8	PWM0_H_5_N	TC0_H_4_TR						SG_TONE[2] (0)		SCB0_CTS (0)	SCB1_SCL (1)			
P14.4	PWM0_9	PWM0_8_N	TC0_H_5_TR					PWM_MCK[0] (1)	SG_AMPL[2] (0)			SCB10_SDA (1)			
P14.5	PWM0_10	PWM0_9_N	TC0_29_TR					PWM_MCK[1] (1)	SG_MCK[2] (0)			SCB10_SCL (1)			
P14.6	PWM0_11	PWM0_10_N	TC0_30_TR						SG_TONE[3] (1)			SCB11_SDA (1)			

(表格续下页……)

13 备用功能引脚分配

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P14.7	PWM0_12	PWM0_11_N							SG_AMPL[3] (1)			SCB11_SCL (1)			
P15.0	PWM0_13	PWM0_12_N			TDM_TX_MCK[1] (1)	TDM_RX_MCK[0] (1)		PWM_LINE1_P[1] (1)	SG_MCK[3] (1)	SCB3_CLK (0)	SCB3_RX (0)	SCB3_SDA (0) ³⁾			
P15.1	PWM0_H_6	PWM0_13_N			TDM_TX_SCK[1] (1)	TDM_RX_SCK[0] (1)		PWM_LINE1_N[1] (1)		SCB3_MOSI (0)	SCB3_TX (0)	SCB3_SCL (0) ³⁾			
P15.2	PWM0_H_7	PWM0_H_6_N			TDM_TX_FSYN C[1] (1)	TDM_RX_FSYN C[0] (1)		PWM_LINE2_P[1] (1)		SCB3_MISO (0)	SCB3_RTS (0)				
P15.3	PWM0_14	PWM0_H_7_N	TC0_H_6_TR		TDM_TX_SD[1] (1)	TDM_RX_SD[0] (1)		PWM_LINE2_N[1] (1)		SCB3_SELO (0)	SCB3_CTS (0)				
P15.4	PWM0_15	PWM0_14_N	TC0_H_7_TR							SCB3_SEL1 (0)			TRIG_IN[22]		
P15.5	PWM0_16	PWM0_15_N							SG_TONE[4] (1)				TRIG_IN[23]		
P15.6	PWM0_17	PWM0_16_N							SG_AMPL[4] (1)				TRIG_IN[24]		

(表格续下页……)

13 备用功能引脚分配

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P15.7	PWM0_18	PWM0_17_N							SG_MCK[4] (1)				TRIG_IN[25]		
P16.0	PWM0_19	PWM0_33_N						PWM_LINE1_P[0] (0)		SCB4_CLK (0)	SCB4_RX (0)	SCB4_SDA (0) ³⁾			
P16.1	PWM0_H_8	PWM0_19_N						PWM_LINE1_N[0] (0)		SCB4_MOSI (0)	SCB4_TX (0)	SCB4_SCL (0) ³⁾			
P16.2	PWM0_H_9	PWM0_H_8_N						PWM_LINE2_P[0] (0)		SCB4_MISO (0)	SCB4_RTS (0)				
P16.3	PWM0_20	PWM0_H_9_N	TC0_H_8_TR					PWM_LINE2_N[0] (0)		SCB4_SEL0 (0)	SCB4_CTS (0)				
P16.4	PWM0_21	PWM0_20_N	TC0_H_9_TR					PWM_MCK[0] (0)	SG_MCK[3] (0)	SCB4_SEL1 (0)					
P16.5	PWM0_22	PWM0_21_N							SG_MCK[4] (0)						
P17.0	PWM0_23	PWM0_22_N						PWM_LINE1_P[1] (0)		SCB5_CLK (0)	SCB5_RX (0)	SCB5_SDA (0) ³⁾			

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P17.1	PWM0_24	PWM0_23_N	TC0_20_TR					PWM_LINE1_N[1] (0)		SCB5_MOSI (0)	SCB5_TX (0)	SCB5_SCL (0) ³⁾			
P17.2	PWM0_25	PWM0_24_N	TC0_21_TR					PWM_LINE2_P[1] (0)		SCB5_MISO (0)	SCB5_RTS (0)				
P17.3	PWM0_26	PWM0_25_N	TC0_22_TR					PWM_LINE2_N[1] (0)		SCB5_SEL0 (0)	SCB5_CTS (0)		TRIG_IN[26]		
P17.4	PWM0_27	PWM0_26_N	TC0_23_TR					PWM_MCK[1] (0)	SG_TO NE[3] (0)	SCB5_SEL1 (0)			TRIG_IN[27]		
P17.5	PWM0_28	PWM0_27_N	TC0_24_TR						SG_AM PL[3] (0)						
P17.6	PWM0_29	PWM0_28_N							SG_TO NE[4] (0)						
P17.7	PWM0_30	PWM0_29_N							SG_AM PL[4] (0)						
P18.0	PWM0_31	PWM0_30_N					CAN0_1_TX			SCB6_CLK (0)	SCB6_RX (0)	SCB6_SDA (0) ³⁾			

(表格续下页……)

13 备用功能引脚分配

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P18.1	PWM0_32	PWM0_31_N					CAN0_1_RX			SCB6_MOSI (0)	SCB6_TX (0)	SCB6_SCL (0) ³⁾			
P18.2	PWM0_33	PWM0_32_N			LIN1_TX	CXPI1_TX	CAN0_0_TX			SCB6_MISO (0)	SCB6_RTS (0)				
P18.3	PWM0_12	PWM0_23_N	TC0_20_TR		LIN1_RX	CXPI1_RX	CAN0_0_RX			SCB6_SEL0 (0)	SCB6_CTS (0)				
P18.4	PWM0_13	PWM0_12_N	TC0_21_TR		LIN1_EN	CXPI1_EN				SCB6_SEL1 (0)			TRIG_IN[28]		
P18.5	PWM0_14	PWM0_13_N											TRIG_IN[29]		
P18.6	PWM0_15	PWM0_14_N	TC0_22_TR										TRIG_IN[30]		
P18.7	PWM0_16	PWM0_15_N	TC0_23_TR										TRIG_IN[31]		
P19.0	PWM0_17	PWM0_16_N			LIN0_TX	CXPI0_TX	CAN1_1_TX			SCB6_CLK (1)	SCB6_RX (1)	SCB6_SDA (1) ³⁾			FAULT_OUT_0
P19.1	PWM0_18	PWM0_17_N			LIN0_RX	CXPI0_RX	CAN1_1_RX			SCB6_MOSI (1)	SCB6_TX (1)	SCB6_SCL (1) ³⁾			FAULT_OUT_1

(表格续下页……)

表 16 (续) 工作模式下的备用引脚功能

Name	Active Mapping														
	HCon# 8 ¹⁾	HCon# 9	HCon# 10	HCon# 11	HCon# 16	HCon# 17	HCon# 18	HCon# 20	HCon# 21	HCon# 22	HCon# 23	HCon# 24	HCon# 25	HCon# 26	HCon# 27
	ACT#0 ²⁾	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P19.2	PWM0_19	PWM0_18_N	TC0_31_TR		LIN0_EN	CXPI0_EN	CAN1_0_TX			SCB6_MISO(1)	SCB6_RTS(1)				FAULT_OUT_2
P19.3	PWM0_20	PWM0_19_N	TC0_32_TR				CAN1_0_RX			SCB6_SEL0(1)	SCB6_CTS(1)				FAULT_OUT_3
P19.4	PWM0_21	PWM0_20_N	TC0_33_TR							SCB6_SEL1(1)					
P19.5	PWM0_22	PWM0_21_N													
P19.6	PWM0_23	PWM0_22_N													

- 1) 高速 I/O 矩阵连接 (HCon) 基准参见表 13。
- 2) 工作模式顺序 (ACT#0、ACT#1 等) 对选择任何备用功能没有任何影响；HSIOM 模块负责处理各个备用功能的分配。
- 3) 有关支持的 IO 单元和 I2C 模式，可参见表 37。

13 备用功能引脚分配

注:

1. 所有在深度睡眠模式下可用的端口引脚功能在工作模式下也可用。
2. 有关使用的引脚多路复用器缩写的更多信息, 参见表 17。
3. 对于任何标有标识符 (n) 的功能, AC 时序仅在相应的组“n”内得到保证。

14 引脚功能描述

14 引脚功能描述

表 17 引脚功能描述

Sl. No.	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_M_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number
9	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
10	SCBx_RX	SCB	UART Receive, x-SCB block
11	SCBx_TX	SCB	UART Transmit, x-SCB block
12	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
13	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
14	SCBx_SDA	SCB	I2C Data line, x-SCB block
15	SCBx_SCL	SCB	I2C Clock line, x-SCB block
16	SCBx_MISO	SCB	SPI Master Input slave Output, x-SCB block
17	SCBx_MOSI	SCB	SPI Master Output slave Input, x-SCB block
18	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
19	SCBx_SELy	SCB	SPI slave Select, x-SCB block, y-select line
20	LINx_RX	LIN	LIN Receive line, x-LIN block
21	LINx_TX	LIN	LIN Transmit line, x-LIN block
22	LINx_EN	LIN	LIN Enable line, x-LIN block
23	CXPIx_RX	CXPI	CXPI Receive line, x-CXPI block

(表格续下页.....)

14 引脚功能描述

表 17 (续) 引脚功能描述

Sl. No.	Pin	Module	Description
24	CXPIx_TX	CXPI	CXPI Transmit line, x-CXPI block
25	CXPIx_EN	CXPI	CXPI Enable line, x-CXPI block
26	CANx_y_TX	CAN FD	CAN Transmit line, x-CAN block, y-channel number
27	CANx_y_RX	CAN FD	CAN Receive line, x-CAN block, y-channel number
28	CAL_SUP_NZ	CPUSS	ETAS Calibration support line
29	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
30	TRACE_DATA_x	SRSS	Trace dataout line x-0 to 3
31	TRACE_CLOCK	SRSS	Trace clock line
32	RTC_CAL	SRSS RTC	RTC calibration clock input
33	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
34	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
35	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
36	SWJ_SWDIO_TMS	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/Output)
37	SWJ_SWDOE_TDI	SRSS	JTAG Test data input
38	HIBERNATE_WAKEUP[x]	SRSS	Hibernate wakeup line x-0 to N (Check Table 14)
39	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
40	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
41	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
42	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
43	EXT_CLK	SRSS	External clock input or output
44	SG_AMPL[x]	SG	Sound generator (SG) amplitude output, x-SG module number
45	SG_MCK[x]	SG	Sound generator (SG) master clock input, x-SG module number
46	SG_TONE[x]	SG	Sound generator (SG) tone output, x-SG module number
47	PWM_LINEx_N[y]	PCM PWM	Audio PWM complementary output line, x-PWM module instance
48	PWM_LINEx_P[y]	PCM PWM	Audio PWM output line, x-PWM module instance
49	PWM_MCK[x]	PCM PWM	Audio PWM master clock input, x-PWM module instance
50	TDM_RX_FSYNC[x]	TDM	TDM receive frame sync, x-TDM module number
51	TDM_RX_MCK[x]	TDM	TDM receive master clock input, x-TDM module number

(表格续下页.....)

14 引脚功能描述

表 17 (续) 引脚功能描述

Sl. No.	Pin	Module	Description
52	TDM_RX_SCK[x]	TDM	TDM receive bit clock, x-TDM module number
53	TDM_RX_SD[x]	TDM	TDM receive serial data, x-TDM module number
54	TDM_TX_FSYNC[x]	TDM	TDM transmit frame sync, x-TDM module number
55	TDM_TX_MCK[x]	TDM	TDM transmit master clock input, x-TDM module number
56	TDM_TX_SCK[x]	TDM	TDM transmit bit clock, x-TDM module number
57	TDM_TX_SD[x]	TDM	TDM transmit serial data, x-TDM module number
58	SPIHB_CLK	SMIF	SMIF interface clock
59	SPIHB_RWDS	SMIF	SMIF (SPI/xSPI) read-write-data-strobe line
60	SPIHB_SELx	SMIF	SMIF (SPI/xSPI) memory select line, x-select line number
61	SPIHB_DATAx	SMIF	SMIF (SPI/xSPI) memory data read and write line, x-0 to 7 data lines
62	LCD_SEG_x	LCD	LCD segment lines x-0 to 35
63	LCD_COM_x	LCD	LCD common lines x-0 to 35
64	IO_CLK_HF[2]	SRSS	CLK_HF2 clock output
65	TRIG_IN[x]	HSIOM	HSIOM_IO_INPUT[x] of trigger inputs, x-0 to 31
66	TRIG_DBG[x]	HSIOM	HSIOM_IO_OUTPUT[x] of trigger outputs, x-0 to 1
67	WCO_IN	SRSS	Watch crystal oscillator input
68	WCO_OUT	SRSS	Watch crystal oscillator output
69	ECO_IN	SRSS	External crystal oscillator input
70	ECO_OUT	SRSS	External crystal oscillator output

15 中断和唤醒分配

15 中断和唤醒分配

表 18 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS inter process communication interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS inter process communication interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS inter process communication interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS inter process communication interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS inter process communication interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS inter process communication interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS inter process communication interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS inter process communication interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS fault structure #0 interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS fault structure #1 interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS fault structure #2 interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS fault structure #3 interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain interrupt
13	srss_interrupt_mcwdt_0_IRQn	DeepSleep	Multi counter watchdog timer #0 interrupt
14	srss_interrupt_mcwdt_1_IRQn	DeepSleep	Multi counter watchdog timer #1 interrupt
17	srss_interrupt_wdt_IRQn	DeepSleep	Hardware watchdog timer interrupt
18	srss_interrupt_IRQn	DeepSleep	Other combined interrupts for SRSS (LVD, CLK_CAL)
19	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event generator timer DeepSleep domain interrupt
20	scb_0_interrupt_IRQn	DeepSleep	Serial Communication block#0 (DeepSleep capable)
22	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Ssupply (V _{DDIO} , V _{DDA_ADC} , V _{DDD}) state change interrupt
23	ioss_interrupt_gpio_dpslp_IRQn	DeepSleep	Consolidated interrupt for DeepSleep ports
24	ioss_interrupts_gpio_0_IRQn	DeepSleep	GPIO_STD port #0 interrupt
25	ioss_interrupts_gpio_1_IRQn	DeepSleep	GPIO_STD port #1 interrupt
26	ioss_interrupts_gpio_2_IRQn	DeepSleep	GPIO_STD port #2 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
27	ioss_interrupts_gpio_3_IRQn	DeepSleep	GPIO_STD port #3 interrupt
28	ioss_interrupts_gpio_4_IRQn	DeepSleep	GPIO_STD port #4 interrupt
29	ioss_interrupts_gpio_5_IRQn	DeepSleep	GPIO_SMC port #5 interrupt
30	ioss_interrupts_gpio_6_IRQn	DeepSleep	GPIO_SMC port #6 interrupt
31	ioss_interrupts_gpio_7_IRQn	DeepSleep	GPIO_SMC port #7 interrupt
34	ioss_interrupts_gpio_10_IRQn	DeepSleep	GPIO_STD port #10 interrupt
35	ioss_interrupts_gpio_11_IRQn	DeepSleep	GPIO_STD port #11 interrupt
36	ioss_interrupts_gpio_12_IRQn	DeepSleep	GPIO_STD port #12 interrupt
37	ioss_interrupts_gpio_13_IRQn	DeepSleep	GPIO_STD port #13 interrupt
38	ioss_interrupts_gpio_14_IRQn	DeepSleep	GPIO_ENH port #14 interrupt
39	ioss_interrupts_gpio_15_IRQn	DeepSleep	GPIO_STD port #15 interrupt
40	ioss_interrupts_gpio_16_IRQn	DeepSleep	GPIO_STD port #16 interrupt
41	ioss_interrupts_gpio_17_IRQn	DeepSleep	GPIO_STD port #17 interrupt
42	ioss_interrupts_gpio_18_IRQn	DeepSleep	GPIO_STD port #18 interrupt
43	ioss_interrupts_gpio_19_IRQn	DeepSleep	GPIO_STD port #19 interrupt
50	ioss_interrupt_gpio_act_IRQn	Active	Consolidated interrupt for active I/O ports
52	ioss_interrupts_gpio_8_IRQn	Active	HSIO_STDLN port #8 interrupt
53	ioss_interrupts_gpio_9_IRQn	Active	HSIO_STDLN port #9 interrupt
70	cpuss_interrupt_crypto_IRQn	Active	Crypto accelerator interrupt
71	cpuss_interrupt_fm_IRQn	Active	FLASH macro interrupt
72	cpuss_interrupts_cm4_fp_IRQn	Active	CM4 floating point operation fault
74	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross trigger Interface) #0
75	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI#1
76	cpuss_interrupts_cm4_cti_0_IRQn	Active	CM4 CTI#0
77	cpuss_interrupts_cm4_cti_1_IRQn	Active	CM4 CTI#1
80	evtgen_0_interrupt_IRQn	Active	Event generator active domain interrupt
81	smif_0_interrupt_IRQn	Active	SMIF#0 interrupt
86	canfd_0_interrupt0_IRQn	Active	CAN#0, consolidated interrupt #0 for all three channels
87	canfd_0_interrupt1_IRQn	Active	CAN#0, consolidated interrupt #1 for all three channels
88	canfd_1_interrupt0_IRQn	Active	CAN#1, consolidated interrupt #0 for all three channels
89	canfd_1_interrupt1_IRQn	Active	CAN#1, consolidated interrupt #1 for all three channels

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
90	canfd_0_interrupts0_0_IRQn	Active	CAN#0, interrupt #0, channel #0
91	canfd_0_interrupts0_1_IRQn	Active	CAN#0, interrupt #0, channel #1
96	canfd_0_interrupts1_0_IRQn	Active	CAN#0, interrupt #1, channel #0
97	canfd_0_interrupts1_1_IRQn	Active	CAN#0, interrupt #1, channel #1
102	canfd_1_interrupts0_0_IRQn	Active	CAN#1, interrupt #0, channel #0
103	canfd_1_interrupts0_1_IRQn	Active	CAN#1, interrupt #0, channel #1
108	canfd_1_interrupts1_0_IRQn	Active	CAN#1, interrupt #1, channel #0
109	canfd_1_interrupts1_1_IRQn	Active	CAN#1, interrupt #1, channel #1
114	lin_0_interrupts_0_IRQn	Active	LIN#0, channel #0 interrupt
115	lin_0_interrupts_1_IRQn	Active	LIN#0, channel #1 interrupt
130	cspi_0_interrupts_0_IRQn	Active	CXPI#0 channel #0 interrupt
131	cspi_0_interrupts_1_IRQn	Active	CXPI#0 channel #1 interrupt
135	scb_1_interrupt_IRQn	Active	SCB#1 interrupt
136	scb_2_interrupt_IRQn	Active	SCB#2 interrupt
137	scb_3_interrupt_IRQn	Active	SCB#3 interrupt
138	scb_4_interrupt_IRQn	Active	SCB#4 interrupt
139	scb_5_interrupt_IRQn	Active	SCB#5 interrupt
140	scb_6_interrupt_IRQn	Active	SCB#6 interrupt
141	scb_7_interrupt_IRQn	Active	SCB#7 interrupt
142	scb_8_interrupt_IRQn	Active	SCB#8 interrupt
143	scb_9_interrupt_IRQn	Active	SCB#9 interrupt
144	scb_10_interrupt_IRQn	Active	SCB#10 interrupt
145	scb_11_interrupt_IRQn	Active	SCB#11 interrupt
160	pass_0_interrupts_sar_0_IRQn	Active	SAR#0, logical channel#0 interrupt
161	pass_0_interrupts_sar_1_IRQn	Active	SAR#0, logical channel#1 interrupt
162	pass_0_interrupts_sar_2_IRQn	Active	SAR#0, logical channel#2 interrupt
163	pass_0_interrupts_sar_3_IRQn	Active	SAR#0, logical channel#3 interrupt
164	pass_0_interrupts_sar_4_IRQn	Active	SAR#0, logical channel#4 interrupt
165	pass_0_interrupts_sar_5_IRQn	Active	SAR#0, logical channel#5 interrupt
166	pass_0_interrupts_sar_6_IRQn	Active	SAR#0, logical channel#6 interrupt
167	pass_0_interrupts_sar_7_IRQn	Active	SAR#0, logical channel#7 interrupt
168	pass_0_interrupts_sar_8_IRQn	Active	SAR#0, logical channel#8 interrupt
169	pass_0_interrupts_sar_9_IRQn	Active	SAR#0, logical channel#9 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
170	pass_0_interrupts_sar_10_IRQn	Active	SAR#0, logical channel#10 interrupt
171	pass_0_interrupts_sar_11_IRQn	Active	SAR#0, logical channel#11 interrupt
172	pass_0_interrupts_sar_12_IRQn	Active	SAR#0, logical channel#12 interrupt
173	pass_0_interrupts_sar_13_IRQn	Active	SAR#0, logical channel#13 interrupt
174	pass_0_interrupts_sar_14_IRQn	Active	SAR#0, logical channel#14 interrupt
175	pass_0_interrupts_sar_15_IRQn	Active	SAR#0, logical channel#15 interrupt
176	pass_0_interrupts_sar_16_IRQn	Active	SAR#0, logical channel#16 interrupt
177	pass_0_interrupts_sar_17_IRQn	Active	SAR#0, logical channel#17 interrupt
178	pass_0_interrupts_sar_18_IRQn	Active	SAR#0, logical channel#18 interrupt
179	pass_0_interrupts_sar_19_IRQn	Active	SAR#0, logical channel#19 interrupt
180	pass_0_interrupts_sar_20_IRQn	Active	SAR#0, logical channel#20 interrupt
181	pass_0_interrupts_sar_21_IRQn	Active	SAR#0, logical channel#21 interrupt
182	pass_0_interrupts_sar_22_IRQn	Active	SAR#0, logical channel#22 interrupt
183	pass_0_interrupts_sar_23_IRQn	Active	SAR#0, logical channel#23 interrupt
184	pass_0_interrupts_sar_24_IRQn	Active	SAR#0, logical channel#24 interrupt
185	pass_0_interrupts_sar_25_IRQn	Active	SAR#0, logical channel#25 interrupt
186	pass_0_interrupts_sar_26_IRQn	Active	SAR#0, logical channel#26 interrupt
187	pass_0_interrupts_sar_27_IRQn	Active	SAR#0, logical channel#27 interrupt
188	pass_0_interrupts_sar_28_IRQn	Active	SAR#0, logical channel#28 interrupt
189	pass_0_interrupts_sar_29_IRQn	Active	SAR#0, logical channel#29 interrupt
190	pass_0_interrupts_sar_30_IRQn	Active	SAR#0, logical channel#30 interrupt
191	pass_0_interrupts_sar_31_IRQn	Active	SAR#0, logical channel#31 interrupt
288	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA#0, channel#0 interrupt
289	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA#0, channel#1 interrupt
290	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA#0, channel#2 interrupt
291	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA#0, channel#3 interrupt
296	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA#0, channel#0 interrupt
297	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA#0, channel#1 interrupt
298	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA#0, channel#2 interrupt
299	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA#0, channel#3 interrupt
300	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA#0, channel#4 interrupt
301	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA#0, channel#5 interrupt
302	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA#0, channel#6 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
303	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA#0, channel#7 interrupt
304	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA#0, channel#8 interrupt
305	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA#0, channel#9 interrupt
306	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA#0, channel#10 interrupt
307	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA#0, channel#11 interrupt
308	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA#0, channel#12 interrupt
309	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA#0, channel#13 interrupt
310	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA#0, channel#14 interrupt
311	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA#0, channel#15 interrupt
312	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA#0, channel#16 interrupt
313	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA#0, channel#17 interrupt
314	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA#0, channel#18 interrupt
315	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA#0, channel#19 interrupt
316	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA#0, channel#20 interrupt
317	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA#0, channel#21 interrupt
318	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA#0, channel#22 interrupt
319	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA#0, channel#23 interrupt
320	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA#0, channel#24 interrupt
321	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA#0, channel#25 interrupt
322	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA#0, channel#26 interrupt
323	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA#0, channel#27 interrupt
324	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA#0, channel#28 interrupt
325	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA#0, channel#29 interrupt
326	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA#0, channel#30 interrupt
327	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA#0, channel#31 interrupt
328	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA#0, channel#32 interrupt
329	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA#0, channel#33 interrupt
330	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA#0, channel#34 interrupt
331	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA#0, channel#35 interrupt
332	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA#0, channel#36 interrupt
333	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA#0, channel#37 interrupt
334	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA#0, channel#38 interrupt
335	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA#0, channel#39 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
336	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA#0, channel#40 interrupt
337	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA#0, channel#41 interrupt
338	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA#0, channel#42 interrupt
339	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA#0, channel#43 interrupt
340	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA#0, channel#44 interrupt
341	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA#0, channel#45 interrupt
342	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA#0, channel#46 interrupt
343	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA#0, channel#47 interrupt
344	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA#0, channel#48 interrupt
345	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA#0, channel#49 interrupt
346	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA#0, channel#50 interrupt
347	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA#0, channel#51 interrupt
348	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA#0, channel#52 interrupt
349	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA#0, channel#53 interrupt
350	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA#0, channel#54 interrupt
351	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA#0, channel#55 interrupt
352	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA#0, channel#56 interrupt
353	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA#0, channel#57 interrupt
354	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA#0, channel#58 interrupt
355	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA#0, channel#59 interrupt
356	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA#0, channel#60 interrupt
357	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA#0, channel#61 interrupt
358	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA#0, channel#62 interrupt
359	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA#0, channel#63 interrupt
360	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA#0, channel#64 interrupt
361	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA#0, channel#65 interrupt
362	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA#0, channel#66 interrupt
363	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA#0, channel#67 interrupt
364	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA#0, channel#68 interrupt
365	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA#0, channel#69 interrupt
366	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA#0, channel#70 interrupt
367	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA#0, channel#71 interrupt
368	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA#0, channel#72 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
369	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA#0, channel#73 interrupt
370	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA#0, channel#74 interrupt
371	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA#0, channel#75 interrupt
424	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA#1, channel#0 interrupt
425	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA#1, channel#1 interrupt
426	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA#1, channel#2 interrupt
427	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA#1, channel#3 interrupt
428	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA#1, channel#4 interrupt
429	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA#1, channel#5 interrupt
430	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA#1, channel#6 interrupt
431	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA#1, channel#7 interrupt
432	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA#1, channel#8 interrupt
433	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA#1, channel#9 interrupt
434	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA#1, channel#10 interrupt
435	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA#1, channel#11 interrupt
436	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA#1, channel#12 interrupt
437	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA#1, channel#13 interrupt
438	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA#1, channel#14 interrupt
439	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA#1, channel#15 interrupt
440	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA#1, channel#16 interrupt
441	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA#1, channel#17 interrupt
442	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA#1, channel#18 interrupt
443	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA#1, channel#19 interrupt
444	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA#1, channel#20 interrupt
445	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA#1, channel#21 interrupt
446	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA#1, channel#22 interrupt
447	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA#1, channel#23 interrupt
448	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA#1, channel#24 interrupt
449	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA#1, channel#25 interrupt
450	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA#1, channel#26 interrupt
451	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA#1, channel#27 interrupt
452	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA#1, channel#28 interrupt
453	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA#1, channel#29 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
454	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA#1, channel#30 interrupt
455	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA#1, channel#31 interrupt
456	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA#1, channel#32 interrupt
457	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA#1, channel#33 interrupt
458	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA#1, channel#34 interrupt
459	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA#1, channel#35 interrupt
460	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA#1, channel#36 interrupt
461	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA#1, channel#37 interrupt
462	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA#1, channel#38 interrupt
463	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA#1, channel#39 interrupt
464	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA#1, channel#40 interrupt
465	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA#1, channel#41 interrupt
466	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA#1, channel#42 interrupt
467	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA#1, channel#43 interrupt
468	cpuss_interrupts_dw1_44_IRQn	Active	CPUSS P-DMA#1, channel#44 interrupt
469	cpuss_interrupts_dw1_45_IRQn	Active	CPUSS P-DMA#1, channel#45 interrupt
470	cpuss_interrupts_dw1_46_IRQn	Active	CPUSS P-DMA#1, channel#46 interrupt
471	cpuss_interrupts_dw1_47_IRQn	Active	CPUSS P-DMA#1, channel#47 interrupt
472	cpuss_interrupts_dw1_48_IRQn	Active	CPUSS P-DMA#1, channel#48 interrupt
473	cpuss_interrupts_dw1_49_IRQn	Active	CPUSS P-DMA#1, channel#49 interrupt
474	cpuss_interrupts_dw1_50_IRQn	Active	CPUSS P-DMA#1, channel#50 interrupt
475	cpuss_interrupts_dw1_51_IRQn	Active	CPUSS P-DMA#1, channel#51 interrupt
476	cpuss_interrupts_dw1_52_IRQn	Active	CPUSS P-DMA#1, channel#52 interrupt
477	cpuss_interrupts_dw1_53_IRQn	Active	CPUSS P-DMA#1, channel#53 interrupt
478	cpuss_interrupts_dw1_54_IRQn	Active	CPUSS P-DMA#1, channel#54 interrupt
479	cpuss_interrupts_dw1_55_IRQn	Active	CPUSS P-DMA#1, channel#55 interrupt
480	cpuss_interrupts_dw1_56_IRQn	Active	CPUSS P-DMA#1, channel#56 interrupt
481	cpuss_interrupts_dw1_57_IRQn	Active	CPUSS P-DMA#1, channel#57 interrupt
482	cpuss_interrupts_dw1_58_IRQn	Active	CPUSS P-DMA#1, channel#58 interrupt
483	cpuss_interrupts_dw1_59_IRQn	Active	CPUSS P-DMA#1, channel#59 interrupt
484	cpuss_interrupts_dw1_60_IRQn	Active	CPUSS P-DMA#1, channel#60 interrupt
485	cpuss_interrupts_dw1_61_IRQn	Active	CPUSS P-DMA#1, channel#61 interrupt
486	cpuss_interrupts_dw1_62_IRQn	Active	CPUSS P-DMA#1, channel#62 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
487	cpuss_interrupts_dw1_63_IRQn	Active	CPUSS P-DMA#1, channel#63 interrupt
488	cpuss_interrupts_dw1_64_IRQn	Active	CPUSS P-DMA#1, channel#64 interrupt
489	cpuss_interrupts_dw1_65_IRQn	Active	CPUSS P-DMA#1, channel#65 interrupt
490	cpuss_interrupts_dw1_66_IRQn	Active	CPUSS P-DMA#1, channel#66 interrupt
491	cpuss_interrupts_dw1_67_IRQn	Active	CPUSS P-DMA#1, channel#67 interrupt
492	cpuss_interrupts_dw1_68_IRQn	Active	CPUSS P-DMA#1, channel#68 interrupt
493	cpuss_interrupts_dw1_69_IRQn	Active	CPUSS P-DMA#1, channel#69 interrupt
494	cpuss_interrupts_dw1_70_IRQn	Active	CPUSS P-DMA#1, channel#70 interrupt
495	cpuss_interrupts_dw1_71_IRQn	Active	CPUSS P-DMA#1, channel#71 interrupt
496	cpuss_interrupts_dw1_72_IRQn	Active	CPUSS P-DMA#1, channel#72 interrupt
497	cpuss_interrupts_dw1_73_IRQn	Active	CPUSS P-DMA#1, channel#73 interrupt
498	cpuss_interrupts_dw1_74_IRQn	Active	CPUSS P-DMA#1, channel#74 interrupt
499	cpuss_interrupts_dw1_75_IRQn	Active	CPUSS P-DMA#1, channel#75 interrupt
500	cpuss_interrupts_dw1_76_IRQn	Active	CPUSS P-DMA#1, channel#76 interrupt
501	cpuss_interrupts_dw1_77_IRQn	Active	CPUSS P-DMA#1, channel#77 interrupt
502	cpuss_interrupts_dw1_78_IRQn	Active	CPUSS P-DMA#1, channel#78 interrupt
503	cpuss_interrupts_dw1_79_IRQn	Active	CPUSS P-DMA#1, channel#79 interrupt
504	cpuss_interrupts_dw1_80_IRQn	Active	CPUSS P-DMA#1, channel#80 interrupt
505	cpuss_interrupts_dw1_81_IRQn	Active	CPUSS P-DMA#1, channel#81 interrupt
506	cpuss_interrupts_dw1_82_IRQn	Active	CPUSS P-DMA#1, channel#82 interrupt
507	cpuss_interrupts_dw1_83_IRQn	Active	CPUSS P-DMA#1, channel#83 interrupt
552	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 group#0, counter#0 interrupt
553	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 group#0, counter#1 interrupt
554	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 group#0, counter#2 interrupt
555	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 group#0, counter#3 interrupt
556	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 group#0, counter#4 interrupt
557	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 group#0, counter#5 interrupt
558	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 group#0, counter#6 interrupt
559	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 group#0, counter#7 interrupt
560	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 group#0, counter#8 interrupt
561	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 group#0, counter#9 interrupt
562	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 group#0, counter#10 interrupt
563	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 group#0, counter#11 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
564	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 group#0, counter#12 interrupt
565	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 group#0, counter#13 interrupt
566	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 group#0, counter#14 interrupt
567	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 group#0, counter#15 interrupt
568	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 group#0, counter#16 interrupt
569	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 group#0, counter#17 interrupt
570	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 group#0, counter#18 interrupt
571	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 group#0, counter#19 interrupt
572	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 group#0, counter#20 interrupt
573	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 group#0, counter#21 interrupt
574	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 group#0, counter#22 interrupt
575	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 group#0, counter#23 interrupt
576	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 group#0, counter#24 interrupt
577	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 group#0, counter#25 interrupt
578	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 group#0, Counter#26 Interrupt
579	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 group#0, counter#27 interrupt
580	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 group#0, counter#28 interrupt
581	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 group#0, counter#29 interrupt
582	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 group#0, counter#30 interrupt
583	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 group#0, counter#31 interrupt
584	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 group#0, counter#32 interrupt
585	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 group#0, counter#33 interrupt
616	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 group#1, counter#0 interrupt
617	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 group#1, counter#1 interrupt
618	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 group#1, counter#2 interrupt
619	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 group#1, counter#3 interrupt
620	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 group#1, counter#4 interrupt
621	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 group#1, counter#5 interrupt
622	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 group#1, counter#6 interrupt
623	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 group#1, counter#7 interrupt
624	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 group#1, counter#8 interrupt
625	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 group#1, counter#9 interrupt
626	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 group#1, counter#10 interrupt

(表格续下页.....)

15 中断和唤醒分配

表 18 (续) 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
627	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 group#1, counter#11 interrupt
680	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 group#2, counter#0 interrupt
681	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 group#2, counter#1 interrupt
682	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 group#2, counter#2 interrupt
683	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 group#2, counter#3 interrupt
684	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 group#2, counter#4 interrupt
685	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 group#2, counter#5 interrupt
686	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 group#2, counter#6 interrupt
687	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 group#2, counter#7 interrupt
688	tcpwm_0_interrupts_520_IRQn	Active	TCPWM0 group#2, counter#8 interrupt
689	tcpwm_0_interrupts_521_IRQn	Active	TCPWM0 group#2, counter#9 interrupt
690	tcpwm_0_interrupts_522_IRQn	Active	TCPWM0 group#2, counter#10 interrupt
691	tcpwm_0_interrupts_523_IRQn	Active	TCPWM0 group#2, counter#11 interrupt
692	tcpwm_0_interrupts_524_IRQn	Active	TCPWM0 group#2, counter#12 interrupt
693	tcpwm_0_interrupts_525_IRQn	Active	TCPWM0 group#2, counter#13 interrupt
694	tcpwm_0_interrupts_526_IRQn	Active	TCPWM0 group#2, counter#14 interrupt
695	tcpwm_0_interrupts_527_IRQn	Active	TCPWM0 group#2, counter#15 interrupt
752	tdm_0_interrupts_tx_0_IRQn	Active	TDM0 TX #0 interrupt
753	tdm_0_interrupts_rx_0_IRQn	Active	TDM0 RX #0 interrupt
754	tdm_0_interrupts_tx_1_IRQn	Active	TDM0 TX #1 interrupt
755	tdm_0_interrupts_rx_1_IRQn	Active	TDM0 RX #1 interrupt
760	sg_0_interrupts_0_IRQn	Active	SG0 #0 interrupt
761	sg_0_interrupts_1_IRQn	Active	SG0 #1 interrupt
762	sg_0_interrupts_2_IRQn	Active	SG0 #2 interrupt
763	sg_0_interrupts_3_IRQn	Active	SG0 #3 interrupt
764	sg_0_interrupts_4_IRQn	Active	SG0 #4 interrupt
768	pwm_0_interrupts_0_IRQn	Active	PCM-PWM0 #0 interrupt
769	pwm_0_interrupts_1_IRQn	Active	PCM-PWM0 #1 interrupt
780	mixer_0_interrupt_dst_IRQn	Active	MIXER0 destination interrupt
781	mixer_0_interrupts_src_0_IRQn	Active	MIXER0 source #0 interrupt
782	mixer_0_interrupts_src_1_IRQn	Active	MIXER0 source #1 interrupt
783	mixer_0_interrupts_src_2_IRQn	Active	MIXER0 source #2 interrupt
784	mixer_0_interrupts_src_3_IRQn	Active	MIXER0 source #3 interrupt
785	mixer_0_interrupts_src_4_IRQn	Active	MIXER0 source #4 interrupt

16 核心中断类型

16 核心中断类型

表 19 核心中断类型

Interrupt	Source	Power mode	Description
0	CPUIntIdx0_IRQn ¹⁾	DeepSleep	CPU user interrupt #0
1	CPUIntIdx1_IRQn ¹⁾	DeepSleep	CPU user interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU user interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU user interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU user interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU user interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU user interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU user interrupt #7
8	Internal0_IRQn	Active	Internal software interrupt #0
9	Internal1_IRQn	Active	Internal software interrupt #1
10	Internal2_IRQn	Active	Internal software interrupt #2
11	Internal3_IRQn	Active	Internal software interrupt #3
12	Internal4_IRQn	Active	Internal software interrupt #4
13	Internal5_IRQn	Active	Internal software interrupt #5
14	Internal6_IRQn	Active	Internal software interrupt #6
15	Internal7_IRQn	Active	Internal software interrupt #7

1) 用户中断不能用于 CM0+ 应用程序，因为它由系统调用内部使用。请注意，这不会影响 CM4 应用程序。

17 触发多路复用器

17 触发多路复用器

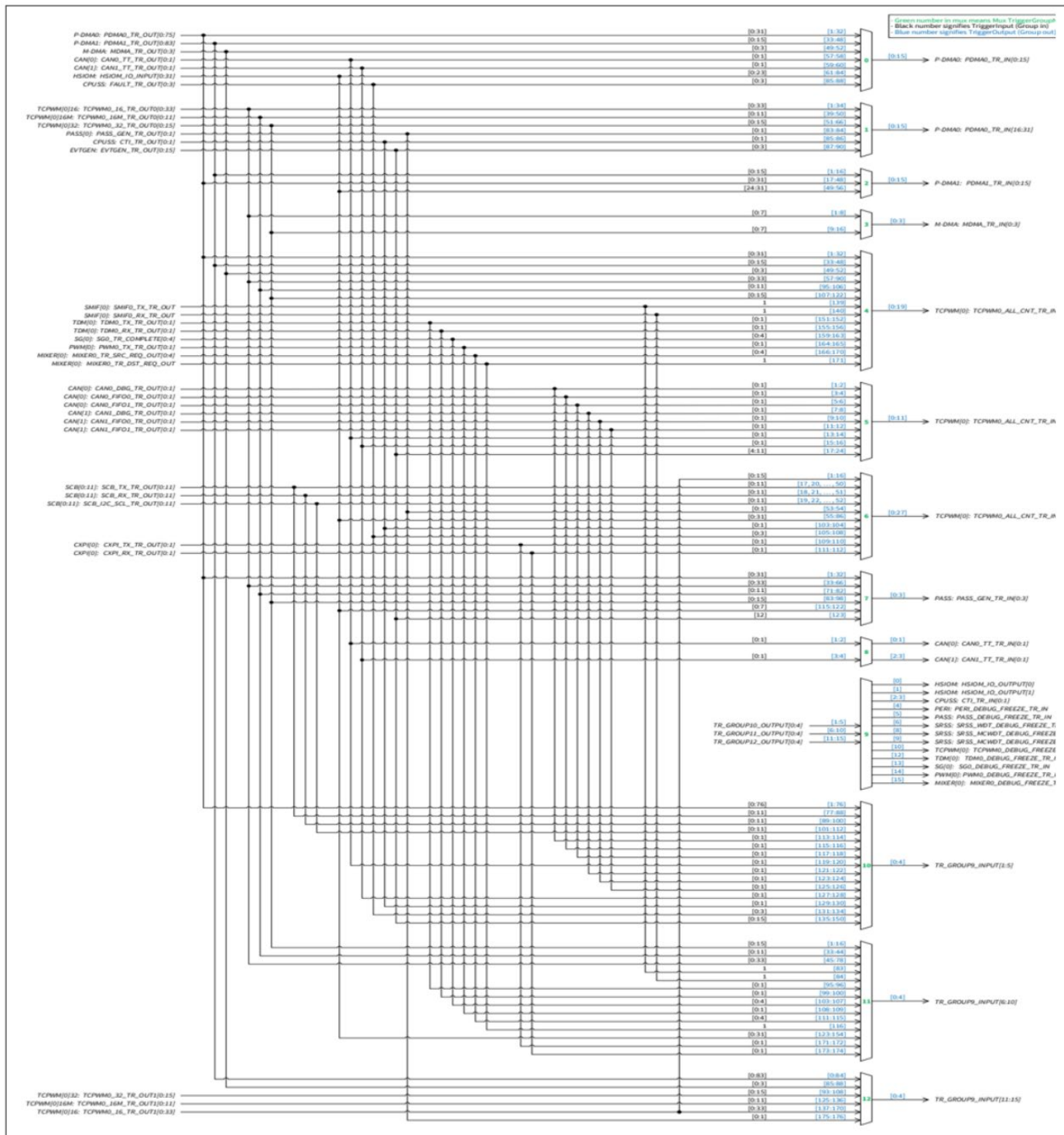


图 8 触发多路复用器¹⁴⁾

¹⁴⁾ 该图仅显示 TRIG_LABEL，最终触发形成基于公式 $TRIG_{\{PREFIX(IN/OUT)\}_{\{MUX_x\}_{\{TRIG_LABEL\}}}$ / $TRIG_{\{PREFIX(IN_1TO1/OUT_1TO1)\}_{\{x\}_{\{TRIG_LABEL\}}}$ (参见表 20、表 21 和表 22。)

17 触发多路复用器

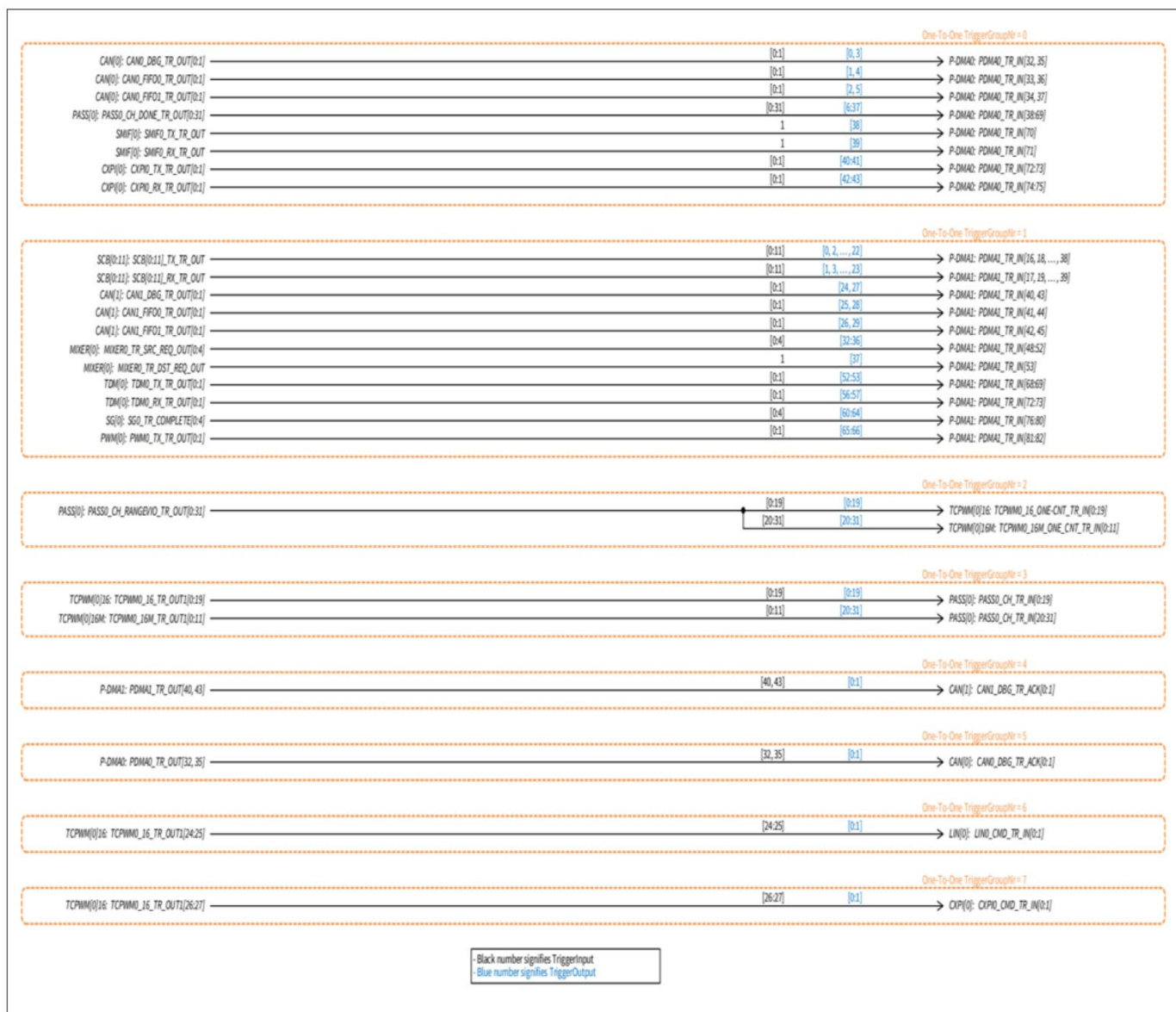


图 9 一对一触发器¹⁴⁾

¹⁴⁾ 该图仅显示 TRIG_LABEL，最终触发形成基于公式 $TRIG_ \{PREFIX(IN/OUT)\}_ \{MUX_x\}_ \{TRIG_LABEL\} / TRIG_ \{PREFIX(IN_1TO1/OUT_1TO1)\}_ \{x\}_ \{TRIG_LABEL\}$ (参见表 20、表 21 和表 22。)

18 触发器组输入

18 触发器组输入

表 20 触发输入

Input	trigger	Description
MUX group 0: P-DMA0_0_15 trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	Allow P-DMA#0 to chain to itself. Channels 0 - 32 are general purpose channels available for chaining ¹⁾
33:48	PDMA1_TR_OUT[0:15]	Cross connections from P-DMA#1 to P-DMA#0, Channels 0-15 are used
49:52	MDMA_TR_OUT[0:3]	Cross connections from M-DMA#0 to P-DMA#0
57:58	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
59:60	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
61:84	HSIOM_IO_INPUT[0:23]	I/O Inputs
85:88	FAULT_TR_OUT[0:3]	Fault events
MUX group 1: P-DMA0_16_31 trigger multiplexer		
1:34	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
39:50	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
51:66	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
83:84	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events
85:86	CTI_TR_OUT[0:1]	Trace events
87:90	EVTGEN_TR_OUT[0:3]	Event generator triggers
MUX group 2: P-DMA1_0_15 trigger multiplexer		
1:16	PDMA1_TR_OUT[0:15]	Allow P-DMA#1 to chain to itself. Channels 0-15 are dedicated for chaining
17:48	PDMA0_TR_OUT[0:31]	Cross connections from P-DMA#0 to P-DMA#1, channels 0-31 are used.
49:56	HSIOM_IO_INPUT[24:31]	I/O Inputs
MUX group 3: M-DMA0 trigger multiplexer		
1:8	TCPWM0_16_TR_OUT0[0:7]	16-bit TCPWM#0 counters
9:16	TCPWM0_32_TR_OUT0[0:7]	32-bit TCPWM#0 counters
MUX group 4: TCPWM0 trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA#0 triggers
33:48	PDMA1_TR_OUT[0:15]	General purpose P-DMA#1 triggers
49:52	MDMA_TR_OUT[0:3]	AHB M-DMA#0 triggers
57:90	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
95:106	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
107:122	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters

(表格续下页.....)

18 触发器组输入

表 20 (续) 触发输入

Input	trigger	Description
139	SMIF0_TX_TR_OUT	SMIF#0 TX trigger
140	SMIF0_RX_TR_OUT	SMIF#0 RX trigger
151:152	TDM0_TX_TR_OUT[0:1]	TDM#0 TX trigger
155:156	TDM0_RX_TR_OUT[0:1]	TDM#0 RX trigger
159:163	SG0_TX_TR_OUT[0:4]	SG#0 TX trigger
164:165	PWM0_TX_TR_OUT[0:1]	PWM#0 TX trigger
166:170	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER#0 SRC trigger
171	MIXER0_TR_DST_REQ_OUT	MIXER#0 DST trigger

MUX group 5: TCPWM0_20_31 trigger multiplexer

1:2	CAN0_DBG_TR_OUT[0:1]	CAN#0 DMA events
3:4	CAN0_FIFO0_TR_OUT[0:1]	CAN#0 FIFO0 events
5:6	CAN0_FIFO1_TR_OUT[0:1]	CAN#0 FIFO1 events
7:8	CAN1_DBG_TR_OUT[0:1]	CAN#1 DMA events
9:10	CAN1_FIFO0_TR_OUT[0:1]	CAN#1 FIFO0 events
11:12	CAN1_FIFO1_TR_OUT[0:1]	CAN#1 FIFO1 events
13:14	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
15:16	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
17:24	EVTGEN_TR_OUT[4:11]	Event generator triggers

MUX group 6: TCPWM0_32_59 trigger Multiplexer

1:16	TCPWM0_16_TR_OUT1[0:15]	16-bit TCPWM#0 counters
17	SCB_TX_TR_OUT[0]	SCB#0 TX trigger
18	SCB_RX_TR_OUT[0]	SCB#0 RX trigger
19	SCB_I2C_SCL_TR_OUT[0]	SCB#0 I2C trigger
20	SCB_TX_TR_OUT[1]	SCB#1 TX trigger
21	SCB_RX_TR_OUT[1]	SCB#1 RX trigger
22	SCB_I2C_SCL_TR_OUT[1]	SCB#1 I2C trigger
23	SCB_TX_TR_OUT[2]	SCB#2 TX trigger
24	SCB_RX_TR_OUT[2]	SCB#2 RX trigger
25	SCB_I2C_SCL_TR_OUT[2]	SCB#2 I2C trigger
26	SCB_TX_TR_OUT[3]	SCB#3 TX trigger
27	SCB_RX_TR_OUT[3]	SCB#3 RX trigger
28	SCB_I2C_SCL_TR_OUT[3]	SCB#3 I2C trigger
29	SCB_TX_TR_OUT[4]	SCB#4 TX trigger

(表格续下页.....)

18 触发器组输入

表 20 (续) 触发输入

Input	trigger	Description
30	SCB_RX_TR_OUT[4]	SCB#4 RX trigger
31	SCB_I2C_SCL_TR_OUT[4]	SCB#4 I2C trigger
32	SCB_TX_TR_OUT[5]	SCB#5 TX trigger
33	SCB_RX_TR_OUT[5]	SCB#5 RX trigger
34	SCB_I2C_SCL_TR_OUT[5]	SCB#5 I2C trigger
35	SCB_TX_TR_OUT[6]	SCB#6 TX trigger
36	SCB_RX_TR_OUT[6]	SCB#6 RX trigger
37	SCB_I2C_SCL_TR_OUT[6]	SCB#6 I2C trigger
38	SCB_TX_TR_OUT[7]	SCB#7 TX trigger
39	SCB_RX_TR_OUT[7]	SCB#7 RX trigger
40	SCB_I2C_SCL_TR_OUT[7]	SCB#7 I2C trigger
41	SCB_TX_TR_OUT[8]	SCB#8 TX trigger
42	SCB_RX_TR_OUT[8]	SCB#8 RX trigger
43	SCB_I2C_SCL_TR_OUT[8]	SCB#8 I2C trigger
44	SCB_TX_TR_OUT[9]	SCB#9 TX trigger
45	CB_RX_TR_OUT[9]	SCB#9 RX trigger
46	SCB_I2C_SCL_TR_OUT[9]	SCB#9 I2C trigger
47	SCB_TX_TR_OUT[10]	SCB#10 TX trigger
48	SCB_RX_TR_OUT[10]	SCB#10 RX trigger
49	SCB_I2C_SCL_TR_OUT[10]	SCB#10 I2C trigger
50	SCB_TX_TR_OUT[11]	SCB#11 TX trigger
51	SCB_RX_TR_OUT[11]	SCB#11 RX trigger
52	SCB_I2C_SCL_TR_OUT[11]	SCB#11 I2C trigger
53:54	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events
55:86	HSIOM_IO_INPUT[0:31]	I/O inputs
103:104	CTI_TR_IN[0:1]	Trace events
105:108	FAULT_TR_OUT[0:3]	Fault events
109:110	CXPI_TX_TR_OUT[0:1]	CXPI#0 transmit events
111:112	CXPI_RX_TR_OUT[0:1]	CXPI#0 receive events
MUX group 7: PASS0 SAR trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA#0 triggers
33:66	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
71:82	TCPWM0_16M_TR_OUT0[0:11]	16-bit motor enhanced TCPWM#0 counters

(表格续下页.....)

18 触发器组输入

表 20 (续) 触发输入

Input	trigger	Description
83:98	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
115:122	HSIOM_IO_INPUT[0:7]	I/O Inputs
123	EVTGEN_TR_OUT[12]	Event generator triggers
MUX group 8: CAN TT Sync		
1:2	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
3:4	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
MUX group 9: debug MUX		
1:5	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP11_OUTPUT[0:4]	Output from debug reduction multiplexer #2
11:15	TR_GROUP12_OUTPUT[0:4]	Output from debug reduction multiplexer #3
MUX group 10: Debug Reduction #1		
1:76	PDMA0_TR_OUT[0:75]	General purpose P-DMA#0 triggers
77:88	SCB_TX_TR_OUT[0:11]	SCB TX triggers
89:100	SCB_RX_TR_OUT[0:11]	SCB RX triggers
101:112	SCB_I2C_SCL_TR_OUT[0:11]	SCB I2C triggers
113:114	CAN0_DBG_TR_OUT[0:1]	CAN#0 DMA
115:116	CAN0_FIFO0_TR_OUT[0:1]	CAN#0 FIFO0
117:118	CAN0_FIFO1_TR_OUT[0:1]	CAN#0 FIFO1
119:120	CAN0_TT_TR_OUT[0:1]	CAN#0 TT sync outputs
121:122	CAN1_DBG_TR_OUT[0:1]	CAN#1 DMA
123:124	CAN1_FIFO0_TR_OUT[0:1]	CAN#1 FIFO0
125:126	CAN1_FIFO1_TR_OUT[0:1]	CAN#1 FIFO1
127:128	CAN1_TT_TR_OUT[0:1]	CAN#1 TT sync outputs
129:130	CTI_TR_OUT[0:1]	Trace events
131:134	FAULT_TR_OUT[0:3]	Fault events
135:150	EVTGEN_TR_OUT[0:15]	EVTGEN triggers
MUX group 11: Debug Reduction #2		
1:16	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
33:44	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
45:78	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
83	SMIF0_TX_TR_OUT	SMIF#0 TX trigger
84	SMIF0_RX_TR_OUT	SMIF#0 RX trigger
95:96	TDM0_TX_TR_OUT[0:1]	TDM#0 TX trigger

(表格续下页.....)

18 触发器组输入

表 20 (续) 触发输入

Input	trigger	Description
99:100	TDM0_RX_TR_OUT[0:1]	TDM#0 RX trigger
103:107	SG0_TX_TR_OUT[0:4]	SG#0 TX trigger
108:109	PWM0_TX_TR_OUT[0:1]	PWM#0 TX trigger
111:115	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER#0 SRC trigger
116	MIXER0_TR_DST_REQ_OUT	MIXER#0 DST trigger
123:154	HSIOM_IO_INPUT[0:31]	I/O inputs
171:172	CXPI_TX_TR_OUT[0:1]	CXPI#0 TX trigger
173:174	CXPI_RX_TR_OUT[0:1]	CXPI#0 RX trigger
MUX group 12: Debug Reduction #3		
1:84	PDMA1_TR_OUT[0:83]	General purpose P-DMA#1 triggers
85:88	MDMA_TR_OUT[0:3]	M-DMA#0 triggers
93:108	TCPWM0_32_TR_OUT1[0:15]	32-bit TCPWM#0 counters
125:136	TCPWM0_16M_TR_OUT1[0:11]	16-bit motor enhanced TCPWM#0 counters
137:170	TCPWM0_16_TR_OUT1[0:33]	16-bit TCPWM#0 counters
175:176	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events

1) “x:y” 表示从 “x” 到 “y” 的范围。

19 触发器组输出

19 触发器组输出

表 21 触发输出

Output	trigger	Description
MUX group 0: P-DMA0_0_15 trigger multiplexer		
0:15	PDMA0_TR_IN[0:15]	triggers to P-DMA#0[0:15]
MUX group 1: P-DMA0_16_31 trigger multiplexer		
0:15	PDMA0_TR_IN[16:31]	triggers to P-DMA#0[16:31]
MUX group 2: P-DMA1_0_15 trigger multiplexer		
0:15	PDMA1_TR_IN[0:15]	triggers to P-DMA#1
MUX group 3: M-DMA0 trigger multiplexer		
0:3	MDMA_TR_IN[0:3]	triggers to M-DMA#0
MUX group 4: TCPWM0 trigger multiplexer		
0:19	TCPWM0_ALL_CNT_TR_IN[0:19]	triggers to TCPWM#0
MUX group 5: TCPWM0_20_31 trigger multiplexer		
0:11	TCPWM0_ALL_CNT_TR_IN[20:31]	triggers to TCPWM#0
MUX group 6: TCPWM0_32_59 trigger multiplexer		
0:27	TCPWM0_ALL_CNT_TR_IN[32:59]	triggers to TCPWM#0
MUX group 7: PASS0 SAR trigger multiplexer		
0:3	PASS_GEN_TR_IN[0:3]	triggers to PASS#0 SAR
MUX group 8: CAN TT Sync		
0:1	CAN0_TT_TR_IN[0:1]	CAN#0 TT Sync Inputs
2:3	CAN1_TT_TR_IN[0:1]	CAN#1 TT Sync Inputs
MUX group 9: debug MUX		
0	HSIOM_IO_OUTPUT[0]	To HSIOM as an output
1	HSIOM_IO_OUTPUT[1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To the Cross trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze PASS#0 SAR operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1]	Signal to Freeze MCWDT#1 operation
9	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0]	Signal to Freeze MCWDT#0 operation
10	TCPWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM#0 operation
12	TDM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TDM#0 operation
13	SG0_DEBUG_FREEZE_TR_IN	Signal to Freeze SG0# operation
14	PWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze PWM#0 operation

(表格续下页.....)

19 触发器组输出

表 21 (续) 触发输出

Output	trigger	Description
15	MIXER0_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER#0 operation
MUX group 10: Debug Reduction #1		
0:4	TR_GROUP9_INPUT[1:5]	To main debug multiplexer
MUX group 11: Debug Reduction #2		
0:4	TR_GROUP9_INPUT[6:10]	To main debug multiplexer
MUX group 12: Debug Reduction #3		
0:4	TR_GROUP9_INPUT[11:15]	To main debug multiplexer

20 一对一触发器

20 一对一触发器

表 22 触发器 1:1

Input	trigger in	trigger out	Description
MUX group 0: CAN0 to P-DMA0 triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[32]	CAN0, channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[33]	CAN0, channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[34]	CAN0, channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[35]	CAN0, channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[36]	CAN0, channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[37]	CAN0, channel #1 FIFO1 trigger
6:37	PASS0_CH_DONE_TR_OUT[0:31]	PDMA0_TR_IN[38:69]	PASS0 SAR0 to P-DMA0 direct connect
38	SMIF0_TX_TR_OUT	PDMA0_TR_IN[70]	SMIF TX to P-DMA0 trigger
39	SMIF0_RX_TR_OUT	PDMA0_TR_IN[71]	SMIF RX to P-DMA0 trigger
40:41	CXPI0_TX_TR_OUT[0:1]	PDMA0_TR_IN[72:73]	CXPI 0 TX P-DMA0 triggers
42:43	CXPI0_RX_TR_OUT[0:1]	PDMA0_TR_IN[74:75]	CXPI 0 RX P-DMA0 triggers
MUX group 1: SCBx to P-DMA1 triggers			
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[16]	SCB0 to P-DMA1 trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[17]	SCB0 to P-DMA1 trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[18]	SCB1 to P-DMA1 trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[19]	SCB1 to P-DMA1 trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[20]	SCB2 to P-DMA1 trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[21]	SCB2 to P-DMA1 trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[22]	SCB3 to P-DMA1 trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[23]	SCB3 to P-DMA1 trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[24]	SCB4 to P-DMA1 trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[25]	SCB4 to P-DMA1 trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[26]	SCB5 to P-DMA1 trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[27]	SCB5 to P-DMA1 trigger
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[28]	SCB6 to P-DMA1 trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[29]	SCB6 to P-DMA1 trigger

(表格续下页.....)

20 一对一触发器

表 22 (续) 触发器 1:1

Input	trigger in	trigger out	Description
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[30]	SCB7 to P-DMA1 trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[31]	SCB7 to P-DMA1 trigger
16	SCB8_TX_TR_OUT	PDMA1_TR_IN[32]	SCB8 to P-DMA1 trigger
17	SCB8_RX_TR_OUT	PDMA1_TR_IN[33]	SCB8 to P-DMA1 trigger
18	SCB9_TX_TR_OUT	PDMA1_TR_IN[34]	SCB9 to P-DMA1 trigger
19	SCB9_RX_TR_OUT	PDMA1_TR_IN[35]	SCB9 to P-DMA1 trigger
20	SCB10_TX_TR_OUT	PDMA1_TR_IN[36]	SCB10 to P-DMA1 trigger
21	SCB10_RX_TR_OUT	PDMA1_TR_IN[37]	SCB10 to P-DMA1 trigger
22	SCB11_TX_TR_OUT	PDMA1_TR_IN[38]	SCB11 to P-DMA1 trigger
23	SCB11_RX_TR_OUT	PDMA1_TR_IN[39]	SCB11 to P-DMA1 trigger
24	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[40]	CAN1 channel #0 P-DMA1 trigger
25	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[41]	CAN1 channel #0 FIFO0 trigger
26	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[42]	CAN1 channel #0 FIFO1 trigger
27	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[43]	CAN1 channel #1 P-DMA1 trigger
28	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[44]	CAN1 channel #1 FIFO0 trigger
29	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[45]	CAN1 channel #1 FIFO1 trigger
32:36	MIXER0_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[48:52]	MIXER0 to P-DMA1 trigger
37	MIXER0_TR_DST_REQ_OUT	PDMA1_TR_IN[53]	MIXER0 to P-DMA1 trigger
52:53	TDM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[68:69]	TDM0 TX to P-DMA1 trigger
56:57	TDM0_RX_TR_OUT[0:1]	PDMA1_TR_IN[72:73]	TDM0 RX to P-DMA1 trigger
60:64	SG0_TX_TR_OUT[0:4]	PDMA1_TR_IN[76:80]	SG0 TX to P-DMA1 trigger
65:66	PWM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[81:82]	PWM0 TX to P-DMA1 trigger

MUX group 2: PASS SARx to TCPWM1 direct connect

0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16_ONE_CNT_TR_IN[0]	SAR0 ch#0, range violation to TCPWM0 group#0 Counter#00 trig=2
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16_ONE_CNT_TR_IN[1]	SAR0 ch#1, range violation to TCPWM0 group#0 counter#01 trig=2
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16_ONE_CNT_TR_IN[2]	SAR0 ch#2, range violation to TCPWM0 group#0 counter#02 trig=2

(表格续下页.....)

20 一对一触发器

表 22 (续) 触发器 1:1

Input	trigger in	trigger out	Description
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16_ONE_CNT_TR_IN[3]	SAR0 ch#3, range violation to TCPWM0 group#0 counter#03 trig=2
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16_ONE_CNT_TR_IN[4]	SAR0 ch#4, range violation to TCPWM0 group#0 counter#04 trig=2
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16_ONE_CNT_TR_IN[5]	SAR0 ch#5, range violation to TCPWM0 group#0 counter#05 trig=2
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16_ONE_CNT_TR_IN[6]	SAR0 ch#6, range violation to TCPWM0 group#0 counter#06 trig=2
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16_ONE_CNT_TR_IN[7]	SAR0 ch#7, range violation to TCPWM0 group#0 counter#07 trig=2
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16_ONE_CNT_TR_IN[8]	SAR0 ch#8, range violation to TCPWM0 group#0 counter#08 trig=2
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16_ONE_CNT_TR_IN[9]	SAR0 ch#9, range violation to TCPWM0 group#0 counter#09 trig=2
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16_ONE_CNT_TR_IN[10]	SAR0 ch#10, range violation to TCPWM0 group#0 counter#10 trig=2
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16_ONE_CNT_TR_IN[11]	SAR0 ch#11, range violation to TCPWM0 group#0 counter#11 trig=2
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16_ONE_CNT_TR_IN[12]	SAR0 ch#12, range violation to TCPWM0 group#0 counter#12 trig=2
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16_ONE_CNT_TR_IN[13]	SAR0 ch#13, range violation to TCPWM0 group#0 counter#13 trig=2
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16_ONE_CNT_TR_IN[14]	SAR0 ch#14, range violation to TCPWM0 group#0 counter#14 trig=2
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16_ONE_CNT_TR_IN[15]	SAR0 ch#15, range violation to TCPWM0 group#0 counter#15 trig=2
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16_ONE_CNT_TR_IN[16]	SAR0 ch#16, range violation to TCPWM0 group#0 counter#16 trig=2

(表格续下页……)

20 一对一触发器

表 22 (续) 触发器 1:1

Input	trigger in	trigger out	Description
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16_ONE_CNT_TR_IN[17]	SAR0 ch#17, range violation to TCPWM0 group#0 counter#17 trig=2
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#18, range violation to TCPWM0 group#0 counter#18 trig=2
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#19, range violation to TCPWM0 group#0 counter#19 trig=2
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#20, range violation to TCPWM0 group#1 counter#00 trig=2
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR0 ch#21, range violation to TCPWM0 group#1 counter#01 trig=2
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR0 ch#22, range violation to TCPWM0 group#1 counter#02 trig=2
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#23, range violation to TCPWM0 group#1 counter#03 trig=2
24	PASS0_CH_RANGEVIO_TR_OUT[24]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR0 ch#24, range violation to TCPWM0 group#1 counter#04 trig=2
25	PASS0_CH_RANGEVIO_TR_OUT[25]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR0 ch#25, range violation to TCPWM0 group#1 counter#05 trig=2
26	PASS0_CH_RANGEVIO_TR_OUT[26]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#26, range violation to TCPWM0 group#1 counter#06 trig=2
27	PASS0_CH_RANGEVIO_TR_OUT[27]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR0 ch#27, range violation to TCPWM0 group#1 counter#07 trig=2
28	PASS0_CH_RANGEVIO_TR_OUT[28]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR0 ch#28, range violation to TCPWM0 group#1 counter#08 trig=2
29	PASS0_CH_RANGEVIO_TR_OUT[29]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#29, range violation to TCPWM0 group#1 counter#09 trig=2
30	PASS0_CH_RANGEVIO_TR_OUT[30]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR0 ch#30, range violation to TCPWM0 group#1 counter#10 trig=2

(表格续下页……)

20 一对一触发器

表 22 (续) 触发器 1:1

Input	trigger in	trigger out	Description
31	PASS0_CH_RANGEVIO_TR_OUT[31]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR0 ch#31, range violation to TCPWM0 group#1 counter#11 trig=2
MUX group 3: TCPWM0 to PASS SARx			
0:19	TCPWM0_16_TR_OUT1[0:19]	PASS0_CH_TR_IN[0:19]	TCPWM0 group #0 counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#0 through SAR0 ch#19
20:31	TCPWM0_16M_TR_OUT1[0:11]	PASS0_CH_TR_IN[20:31]	TCPWM0 group #1 counter #00 through 11 (PWM0_M_0 to PWM0_M_11) to SAR0 ch#20 through SAR0 ch#31
MUX group 4: Acknowledge triggers from P-DMA1 to CAN1			
0	PDMA1_TR_OUT[40]	CAN1_DBG_TR_ACK[0]	CAN1 Channel#0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[43]	CAN1_DBG_TR_ACK[1]	CAN1 channel#1 P-DMA1 acknowledge
MUX group 5: Acknowledge triggers from P-DMA0 to CAN0			
0	PDMA0_TR_OUT[32]	CAN0_DBG_TR_ACK[0]	CAN0 channel#0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[35]	CAN0_DBG_TR_ACK[1]	CAN0 channel#1 P-DMA0 acknowledge
MUX group 6: TCPWM0 to LIN0 triggers			
0:1	TCPWM0_16_TR_OUT1[24:25]	LIN0_CMD_TR_IN[0:1]	TCPWM0 (group #0 counter #24 to #25) to LIN0
MUX group 7: TCPWM0_TO_CXPI (TCPWM0 to CXPI)			
0:1	TCPWM0_16_TR_OUT1[26:27]	CXPI0_CMD_TR_IN[0:1]	TCPWM0 (group #0 counter #24 to #25) to CXPI0

1) SAR ADC[x] 的每个逻辑通道都可以连接到任意 SAR ADC[x]_y 外部引脚。(x = 0, or 1, or, 2 and y=0 to max 31)

21 外设时钟

21 外设时钟

表 23 外设时钟分配

Output	Destination	Description
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO7_CLOCK	SMART I/O#7
2	PCLK_CANFD0_CLOCK_CAN0	CAN#0, channel#0
3	PCLK_CANFD0_CLOCK_CAN1	CAN#0, channel#1
4	PCLK_CANFD1_CLOCK_CAN0	CAN#1, channel#0
5	PCLK_CANFD1_CLOCK_CAN1	CAN#1, channel#1
6	PCLK_LIN0_CLOCK_CH_EN0	LIN#0, channel#0
7	PCLK_LIN0_CLOCK_CH_EN1	LIN#0, channel#1
8	PCLK_CXPI0_CLOCK_CH_EN0	CXPI#0 channel#0
9	PCLK_CXPI0_CLOCK_CH_EN1	CXPI#0 channel#1
10	PCLK_SCB0_CLOCK	SCB#0
11	PCLK_SCB1_CLOCK	SCB#1
12	PCLK_SCB2_CLOCK	SCB#2
13	PCLK_SCB3_CLOCK	SCB#3
14	PCLK_SCB4_CLOCK	SCB#4
15	PCLK_SCB5_CLOCK	SCB#5
16	PCLK_SCB6_CLOCK	SCB#6
17	PCLK_SCB7_CLOCK	SCB#7
18	PCLK_SCB8_CLOCK	SCB#8
19	PCLK_SCB9_CLOCK	SCB#9
20	PCLK_SCB10_CLOCK	SCB#10
21	PCLK_SCB11_CLOCK	SCB#11
22	PCLK_PASS0_CLOCK_SAR0	SAR#0
23	PCLK_LCD0_CLOCK	LCD controller
24	PCLK_TCPWM0_CLOCKS0	TCPWM#0 group #0, counter #0
25	PCLK_TCPWM0_CLOCKS1	TCPWM#0 group #0, counter #1
26	PCLK_TCPWM0_CLOCKS2	TCPWM#0 group #0, counter #2
27	PCLK_TCPWM0_CLOCKS3	TCPWM#0 group #0, counter #3
28	PCLK_TCPWM0_CLOCKS4	TCPWM#0 group #0, counter #4
29	PCLK_TCPWM0_CLOCKS5	TCPWM#0 group #0, counter #5
30	PCLK_TCPWM0_CLOCKS6	TCPWM#0 group #0, counter #6
31	PCLK_TCPWM0_CLOCKS7	TCPWM#0 group #0, counter #7

(表格续下页.....)

21 外设时钟

表 23 (续) 外设时钟分配

Output	Destination	Description
32	PCLK_TCPWM0_CLOCKS8	TCPWM#0 group #0, counter #8
33	PCLK_TCPWM0_CLOCKS9	TCPWM#0 group #0, counter #9
34	PCLK_TCPWM0_CLOCKS10	TCPWM#0 group #0, counter #10
35	PCLK_TCPWM0_CLOCKS11	TCPWM#0 group #0, counter #11
36	PCLK_TCPWM0_CLOCKS12	TCPWM#0 group #0, counter #12
37	PCLK_TCPWM0_CLOCKS13	TCPWM#0 group #0, counter #13
38	PCLK_TCPWM0_CLOCKS14	TCPWM#0 group #0, counter #14
39	PCLK_TCPWM0_CLOCKS15	TCPWM#0 group #0, counter #15
40	PCLK_TCPWM0_CLOCKS16	TCPWM#0 group #0, counter #16
41	PCLK_TCPWM0_CLOCKS17	TCPWM#0 group #0, counter #17
42	PCLK_TCPWM0_CLOCKS18	TCPWM#0 group #0, counter #18
43	PCLK_TCPWM0_CLOCKS19	TCPWM#0 group #0, counter #19
44	PCLK_TCPWM0_CLOCKS20	TCPWM#0 group #0, counter #20
45	PCLK_TCPWM0_CLOCKS21	TCPWM#0 group #0, counter #21
46	PCLK_TCPWM0_CLOCKS22	TCPWM#0 group #0, counter #22
47	PCLK_TCPWM0_CLOCKS23	TCPWM#0 group #0, counter #23
48	PCLK_TCPWM0_CLOCKS24	TCPWM#0 group #0, counter #24
49	PCLK_TCPWM0_CLOCKS25	TCPWM#0 group #0, counter #25
50	PCLK_TCPWM0_CLOCKS26	TCPWM#0 group #0, counter #26
51	PCLK_TCPWM0_CLOCKS27	TCPWM#0 group #0, counter #27
52	PCLK_TCPWM0_CLOCKS28	TCPWM#0 group #0, counter #28
53	PCLK_TCPWM0_CLOCKS29	TCPWM#0 group #0, counter #29
54	PCLK_TCPWM0_CLOCKS30	TCPWM#0 group #0, counter #30
55	PCLK_TCPWM0_CLOCKS31	TCPWM#0 group #0, counter #31
56	PCLK_TCPWM0_CLOCKS32	TCPWM#0 group #0, counter #32
57	PCLK_TCPWM0_CLOCKS33	TCPWM#0 group #0, counter #33
58	PCLK_TCPWM0_CLOCKS256	TCPWM#0 group #1, counter #0
59	PCLK_TCPWM0_CLOCKS257	TCPWM#0 group #1, counter #1
60	PCLK_TCPWM0_CLOCKS258	TCPWM#0 group #1, counter #2
61	PCLK_TCPWM0_CLOCKS259	TCPWM#0 group #1, counter #3
62	PCLK_TCPWM0_CLOCKS260	TCPWM#0 group #1, counter #4
63	PCLK_TCPWM0_CLOCKS261	TCPWM#0 group #1, counter #5
64	PCLK_TCPWM0_CLOCKS262	TCPWM#0 group #1, counter #6

(表格续下页.....)

21 外设时钟

表 23 (续) 外设时钟分配

Output	Destination	Description
65	PCLK_TCPWM0_CLOCKS263	TCPWM#0 group #1, counter #7
66	PCLK_TCPWM0_CLOCKS264	TCPWM#0 group #1, counter #8
67	PCLK_TCPWM0_CLOCKS265	TCPWM#0 group #1, counter #9
68	PCLK_TCPWM0_CLOCKS266	TCPWM#0 group #1, counter #10
69	PCLK_TCPWM0_CLOCKS267	TCPWM#0 group #1, counter #11
70	PCLK_TCPWM0_CLOCKS512	TCPWM#0 group #2, counter #0
71	PCLK_TCPWM0_CLOCKS513	TCPWM#0 group #2, counter #1
72	PCLK_TCPWM0_CLOCKS514	TCPWM#0 group #2, counter #2
73	PCLK_TCPWM0_CLOCKS515	TCPWM#0 group #2, counter #3
74	PCLK_TCPWM0_CLOCKS516	TCPWM#0 group #2, counter #4
75	PCLK_TCPWM0_CLOCKS517	TCPWM#0 group #2, counter #5
76	PCLK_TCPWM0_CLOCKS518	TCPWM#0 group #2, counter #6
77	PCLK_TCPWM0_CLOCKS519	TCPWM#0 group #2, counter #7
78	PCLK_TCPWM0_CLOCKS520	TCPWM#0 group #2, counter #8
79	PCLK_TCPWM0_CLOCKS521	TCPWM#0 group #2, counter #9
80	PCLK_TCPWM0_CLOCKS522	TCPWM#0 group #2, counter #10
81	PCLK_TCPWM0_CLOCKS523	TCPWM#0 group #2, counter #11
82	PCLK_TCPWM0_CLOCKS524	TCPWM#0 group #2, counter #12
83	PCLK_TCPWM0_CLOCKS525	TCPWM#0 group #2, counter #13
84	PCLK_TCPWM0_CLOCKS526	TCPWM#0 group #2, counter #14
85	PCLK_TCPWM0_CLOCKS527	TCPWM#0 group #2, counter #15

22 故障

22 故障

表 24 故障分配

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ MPU/SMPU violation. DATA0[31:0]: violating address. DATA1[0]: user read. DATA1[1]: user write. DATA1[2]: user execute. DATA1[3]: privileged read. DATA1[4]: privileged write. DATA1[5]: privileged execute. DATA1[6]: non-secure. DATA1[11:8]: master identifier. DATA1[15:12]: protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation.
1	CPUSS_MPU_VIO_1	CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA#0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA#1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA#0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_MPU_VIO_16	CM4 system bus AHB-Lite interface MPU violation. See CPUSS_MPU_VIO_0 description.
17	CPUSS_MPU_VIO_17	CM4 code bus AHB-Lite interface MPU violation for non flash controller accesses. See CPUSS_MPU_VIO_0 description.
18	CPUSS_MPU_VIO_18	CM4 code bus AHB-Lite interface MPU violation for flash controller accesses. See CPUSS_MPU_VIO_0 description.
26	PERI_PERI_C_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: violating address. DATA1[7:0]: syndrome of SRAM word.
27	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation

(表格续下页.....)

22 故障

表 24 (续) 故障分配

Fault	Source	Description
28	PERI_MS_VIO_0	CM0+ peripheral master interface PPU violation DATA0[31:0]: violating address. DATA1[0]: user read. DATA1[1]: user write. DATA1[2]: user execute. DATA1[3]: privileged read. DATA1[4]: privileged write. DATA1[5]: privileged execute. DATA1[6]: non-secure. DATA1[11:8]: master identifier. DATA1[15:12]: protection context identifier. DATA1[31:28]: “0”: master interface, PPU violation, “1”: timeout detected, “2”: bus error, other: undefined.
29	PERI_MS_VIO_1	CM4 peripheral master interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_2	P-DMA0 peripheral master interface PPU violation. See PERI_MS_VIO_0 description.
31	PERI_MS_VIO_3	P-DMA1 peripheral master interface PPU violation. See PERI_MS_VIO_0 description.
32	PERI_GROUP_VIO_0	Peripheral group #0 violation DATA0[31:0]: violating address. DATA1[0]: user read. DATA1[1]: user write. DATA1[2]: user execute. DATA1[3]: privileged read. DATA1[4]: privileged write. DATA1[5]: privileged execute. DATA1[6]: non-secure. DATA1[11:8]: master identifier. DATA1[15:12]: protection context identifier. DATA1[31:28]: “0”: decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral group #3 violation. See PERI_GROUP_VIO_0 description.

(表格续下页.....)

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表 24 (续) 故障分配

Fault	Source	Description
36	PERI_GROUP_VIO_4	Peripheral group #4 violation. See PERI_GROUP_VIO_0 description.
37	PERI_GROUP_VIO_5	Peripheral group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral group #6 violation. See PERI_GROUP_VIO_0 description.
40	PERI_GROUP_VIO_8	Peripheral group #8 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral group #9 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERROR	Flash controller main flash bus error FAULT_DATA0[26:0]: violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERROR	Flash controller work flash bus error FAULT_DATA0[26:0]: violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: master identifier.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation DATA0[26:0]: violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: syndrome of 32-bit word.

(表格续下页.....)

22 故障

表 24 (续) 故障分配

Fault	Source	Description
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation DATA0[26:0]: violating address. DATA1[6:0]: syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: syndrome of 32-bit SRAM word (at address offset 0xC).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
56	CPUSS_FLASHC_CM4_CA_C_ECC	Flash controller CM4 cache correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
57	CPUSS_FLASHC_CM4_CA_NC_ECC	Flash controller CM4 cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation DATA0[31:0]: violating address. DATA1[6:0]: syndrome of 32-bit SRAM code word.
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.

(表格续下页.....)

22 故障

表 24 (续) 故障分配

Fault	Source	Description
64	CPUSS_CRYPTOC_C_ECC	Crypto memory correctable ECC violation DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of least significant 32-bit SRAM. DATA1[14:8]: Syndrome of most significant 32-bit SRAM.
65	CPUSS_CRYPTONC_ECC	CRYPTO memory non-correctable ECC violation. See CPUSS_CRYPTOC_C_ECC description.
70	CPUSS_DW0_C_ECC	Dataview0 memory correctable ECC violation DATA0[11:0]: violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: syndrome of 32-bit SRAM code word.
71	CPUSS_DW0_NC_ECC	P-DMA#0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
72	CPUSS_DW1_C_ECC	P-DMA#1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
73	CPUSS_DW1_NC_ECC	P-DMA#1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
74	CPUSS_FM_SRAM_C_ECC	Flash code storage SRAM memory correctable ECC violation DATA0[15:0]: address location in the eCT Flash SRAM. DATA1[6:0]: syndrome of 32-bit SRAM word.
75	CPUSS_FM_SRAM_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.
80	CANFD_0_CAN_C_ECC	CAN#0 message buffer correctable ECC violation DATA0[15:0]: violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: master ID: 0-7 = CAN channel ID within cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.

(表格续下页.....)

22 故障

表 24 (续) 故障分配

Fault	Source	Description
81	CANFD_0_CAN_NC_ECC	CAN#0 message buffer non-correctable ECC violation DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for address error). DATA0[27:24]: master ID: 0-7 = CAN channel ID within cluster, 8 = AHB I/F DATA0[30]: write access, only possible for address error DATA0[31]: address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for address error).
82	CANFD_1_CAN_C_ECC	CAN#1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description.
83	CANFD_1_CAN_NC_ECC	CAN#1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CSV violation occurred on corresponding CLK_HF* root clock DATA0[24]: CSV violation occurred on reference clock for CLK_HF CSVs DATA0[25]: CSV violation occurred on CLK_LF DATA0[26]: CSV violation occurred on CLK_ILOO DATA0[27]: CSV violation occurred on CLK_BAK
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple counters can detect a violation at the same time. DATA0[0]: BOD detected on VDDA_ADC DATA0[1]: OVD detected on VDDA_ADC DATA0[16]: violation detected on LVD/HVD #1 DATA0[17]: violation detected on LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT#0 (all sub-counters). Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT

(表格续下页.....)

22 故障

表 24 (续) 故障分配

Fault	Source	Description
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT#1 (all sub-counters). See SRSS_FAULT_MCWDT#0 description.

23 外设保护单位固定结构对

23 外设保护单元固定结构对

保护对由一对 PPU 结构组成，包括一个主结构和一个从结构。主结构保护从结构，从结构保护外设寄存器等资源，或外设本身。

表 25 PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
0	PERI_MAIN	0x40000000	0x00002000	Peripheral interconnect main
1	PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral group #0 main
3	PERI_GR1_GROUP	0x40004030	0x00000004	Peripheral group #1 main
4	PERI_GR2_GROUP	0x40004050	0x00000004	Peripheral group #2 main
5	PERI_GR3_GROUP	0x40004060	0x00000020	Peripheral group #3 main
6	PERI_GR4_GROUP	0x40004080	0x00000020	Peripheral group #4 main
7	PERI_GR5_GROUP	0x400040A0	0x00000020	Peripheral group #5 main
8	PERI_GR6_GROUP	0x400040C0	0x00000020	Peripheral group #6 main
9	PERI_GR8_GROUP	0x40004100	0x00000020	Peripheral group #8 main
10	PERI_GR9_GROUP	0x40004120	0x00000020	Peripheral group #9 main
11	PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
12	CRYPTO_MAIN	0x40100000	0x00000400	Crypto main
13	CRYPTO_CRYPT0	0x40101000	0x00000800	Crypto MMIO (Memory mapped I/O)
14	CRYPTO_BOOT	0x40102000	0x00000100	Crypto boot
15	CRYPTO_KEY0	0x40102100	0x00000004	Crypto Key #0
16	CRYPTO_KEY1	0x40102120	0x00000004	Crypto Key #1
17	CRYPTO_BUF	0x40108000	0x00002000	Crypto buffer
18	CPUSS_CM4	0x40200000	0x00000400	CM4 CPU core
19	CPUSS_CM0	0x40201000	0x00001000	CM0+ CPU core
20	CPUSS_BOOT ¹⁾	0x40202000	0x00000200	CPUSS boot
21	CPUSS_CM0_INT	0x40208000	0x00001000	CPUSS CM0+ interrupts
22	CPUSS_CM4_INT	0x4020A000	0x00001000	CPUSS CM4 interrupts
23	FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUSS fault structure #0 main
24	FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUSS fault structure #1 main
25	FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS fault structure #2 main
26	FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS fault structure #3 main
27	IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC structure #0
28	IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC structure #1
29	IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC structure #2

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
30	IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC structure #3
31	IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC structure #4
32	IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC structure #5
33	IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC structure #6
34	IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC structure #7
35	IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC interrupt structure #0
36	IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC interrupt structure #1
37	IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC interrupt structure #2
38	IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC interrupt structure #3
39	IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC interrupt structure #4
40	IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC interrupt structure #5
41	IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC interrupt structure #6
42	IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC interrupt structure #7
43	PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection S MPU main
44	PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
45	PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
46	PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
47	FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
48	FLASHC_CMD	0x40240008	0x00000004	Flash controller command
49	FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
50	FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
51	FLASHC_CM4	0x40240480	0x00000080	Flash controller CM4
52	FLASHC_CRYPT0	0x40240500	0x00000004	Flash controller Crypto
53	FLASHC_DW0	0x40240580	0x00000004	Flash controller P-DMA#0
54	FLASHC_DW1	0x40240600	0x00000004	Flash controller P-DMA#1
55	FLASHC_DM4C	0x40240680	0x00000004	Flash controller M-DMA#0
56	FLASHC_FlashMgmt	0x4024F000	0x00000080	Flash management
57	FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller main safety
58	FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work safety
59	SRSS_GENERAL	0x40260000	0x00000400	SRSS general
60	SRSS_MAIN	0x40261000	0x00001000	SRSS main

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
61	SRSS_SECURE	0x40262000	0x00002000	SRSS secure
62	MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
63	MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
64	MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
65	MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
66	WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
67	WDT_MAIN	0x4026C040	0x00000020	System WDT main
68	BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
69	DW0_DW	0x40280000	0x00000100	P-DMA#0 main
70	DW1_DW	0x40290000	0x00000100	P-DMA#1 main
71	DW0_DW_CRC	0x40280100	0x00000080	P-DMA#0 CRC
72	DW1_DW_CRC	0x40290100	0x00000080	P-DMA#1 CRC
73	DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA#0 channel #0
74	DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA#0 channel #1
75	DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA#0 channel #2
76	DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA#0 channel #3
77	DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA#0 channel #4
78	DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA#0 channel #5
79	DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA#0 channel #6
80	DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA#0 channel #7
81	DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA#0 channel #8
82	DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA#0 channel #9
83	DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA#0 channel #10
84	DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA#0 channel #11
85	DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA#0 channel #12
86	DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA#0 channel #13
87	DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA#0 channel #14
88	DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA#0 channel #15
89	DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA#0 channel #16
90	DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA#0 channel #17
91	DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA#0 channel #18
92	DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA#0 channel #19
93	DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA#0 channel #20

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
94	DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA#0 channel #21
95	DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA#0 channel #22
96	DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA#0 channel #23
97	DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA#0 channel #24
98	DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA#0 channel #25
99	DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA#0 channel #26
100	DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA#0 channel #27
101	DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA#0 channel #28
102	DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA#0 channel #29
103	DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA#0 channel #30
104	DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA#0 channel #31
105	DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA#0 channel #32
106	DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA#0 channel#33
107	DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA#0 channel #34
108	DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA#0 channel #35
109	DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA#0 channel #36
110	DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA#0 channel#37
111	DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA#0 channel #38
112	DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA#0 channel #39
113	DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA#0 channel#40
114	DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA#0 channel #41
115	DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA#0 channel #42
116	DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA#0 channel #43
117	DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA#0 channel #44
118	DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA#0 channel #45
119	DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA#0 channel #46
120	DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA#0 channel #47
121	DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA#0 channel #48
122	DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA#0 channel #49
123	DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA#0 channel #50
124	DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA#0 channel #51
125	DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA#0 channel #52
126	DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA#0 channel #53

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
127	DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA#0 channel #54
128	DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA#0 channel #55
129	DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA#0 channel #56
130	DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA#0 channel #57
131	DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA#0 channel #58
132	DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA#0 channel #59
133	DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA#0 channel #60
134	DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA#0 channel #61
135	DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA#0 channel #62
136	DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA#0 channel #63
137	DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA#0 channel #64
138	DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA#0 channel #65
139	DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA#0 channel #66
140	DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA#0 channel #67
141	DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA#0 channel #68
142	DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA#0 channel #69
143	DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA#0 channel #70
144	DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA#0 channel #71
145	DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA#0 channel #72
146	DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA#0 channel #73
147	DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA#0 channel #74
148	DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA#0 channel #75
149	DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA#1 channel #0
150	DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA#1 channel #1
151	DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA#1 channel #2
152	DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA#1 channel #3
153	DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA#1 channel #4
154	DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA#1 channel #5
155	DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA#1 channel #6
156	DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA#1 channel #7
157	DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA#1 channel #8
158	DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA#1 channel #9
159	DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA#1 channel #10

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
160	DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA#1 channel #11
161	DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA#1 channel #12
162	DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA#1 channel #13
163	DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA#1 channel #14
164	DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA#1 channel #15
165	DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA#1 channel #16
166	DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA#1 channel #17
167	DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA#1 channel #18
168	DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA#1 channel #19
169	DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA#1 channel #20
170	DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA#1 channel #21
171	DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA#1 channel #22
172	DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA#1 channel #23
173	DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA#1 channel #24
174	DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA#1 channel #25
175	DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA#1 channel #26
176	DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA#1 channel #27
177	DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA#1 channel #28
178	DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA#1 channel #29
179	DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA#1 channel #30
180	DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA#1 channel #31
181	DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA#1 channel #32
182	DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA#1 channel #33
183	DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA#1 channel #34
184	DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA#1 channel #35
185	DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA#1 channel #36
186	DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA#1 channel #37
187	DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA#1 channel #38
188	DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA#1 channel #39
189	DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA#1 channel #40
190	DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA#1 channel #41
191	DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA#1 channel #42
192	DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA#1 channel #43

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23 外设保护单位固定结构对

表 25 (续) **PPU 固定结构对**

Pair No.	PPU fixed structure pair	Address	Size	Description
193	DW1_CH_STRUCT44_CH	0x40298B00	0x00000040	P-DMA#1 channel #44
194	DW1_CH_STRUCT45_CH	0x40298B40	0x00000040	P-DMA#1 channel #45
195	DW1_CH_STRUCT46_CH	0x40298B80	0x00000040	P-DMA#1 channel #46
196	DW1_CH_STRUCT47_CH	0x40298BC0	0x00000040	P-DMA#1 channel #47
197	DW1_CH_STRUCT48_CH	0x40298C00	0x00000040	P-DMA#1 channel #48
198	DW1_CH_STRUCT49_CH	0x40298C40	0x00000040	P-DMA#1 channel #49
199	DW1_CH_STRUCT50_CH	0x40298C80	0x00000040	P-DMA#1 channel #50
200	DW1_CH_STRUCT51_CH	0x40298CC0	0x00000040	P-DMA#1 channel #51
201	DW1_CH_STRUCT52_CH	0x40298D00	0x00000040	P-DMA#1 channel #52
202	DW1_CH_STRUCT53_CH	0x40298D40	0x00000040	P-DMA#1 channel #53
203	DW1_CH_STRUCT54_CH	0x40298D80	0x00000040	P-DMA#1 channel #54
204	DW1_CH_STRUCT55_CH	0x40298DC0	0x00000040	P-DMA#1 channel #55
205	DW1_CH_STRUCT56_CH	0x40298E00	0x00000040	P-DMA#1 channel #56
206	DW1_CH_STRUCT57_CH	0x40298E40	0x00000040	P-DMA#1 channel #57
207	DW1_CH_STRUCT58_CH	0x40298E80	0x00000040	P-DMA#1 channel #58
208	DW1_CH_STRUCT59_CH	0x40298EC0	0x00000040	P-DMA#1 channel #59
209	DW1_CH_STRUCT60_CH	0x40298F00	0x00000040	P-DMA#1 channel #60
210	DW1_CH_STRUCT61_CH	0x40298F40	0x00000040	P-DMA#1 channel #61
211	DW1_CH_STRUCT62_CH	0x40298F80	0x00000040	P-DMA#1 channel #62
212	DW1_CH_STRUCT63_CH	0x40298FC0	0x00000040	P-DMA#1 channel #63
213	DW1_CH_STRUCT64_CH	0x40299000	0x00000040	P-DMA#1 channel #64
214	DW1_CH_STRUCT65_CH	0x40299040	0x00000040	P-DMA#1 channel #65
215	DW1_CH_STRUCT66_CH	0x40299080	0x00000040	P-DMA#1 channel #66
216	DW1_CH_STRUCT67_CH	0x402990C0	0x00000040	P-DMA#1 channel #67
217	DW1_CH_STRUCT68_CH	0x40299100	0x00000040	P-DMA#1 channel #68
218	DW1_CH_STRUCT69_CH	0x40299140	0x00000040	P-DMA#1 channel #69
219	DW1_CH_STRUCT70_CH	0x40299180	0x00000040	P-DMA#1 channel #70
220	DW1_CH_STRUCT71_CH	0x402991C0	0x00000040	P-DMA#1 channel #71
221	DW1_CH_STRUCT72_CH	0x40299200	0x00000040	P-DMA#1 channel #72
222	DW1_CH_STRUCT73_CH	0x40299240	0x00000040	P-DMA#1 channel #73
223	DW1_CH_STRUCT74_CH	0x40299280	0x00000040	P-DMA#1 channel #74
224	DW1_CH_STRUCT75_CH	0x402992C0	0x00000040	P-DMA#1 channel #75
225	DW1_CH_STRUCT76_CH	0x40299300	0x00000040	P-DMA#1 channel #76

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23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
226	DW1_CH_STRUCT77_CH	0x40299340	0x00000040	P-DMA#1 channel #77
227	DW1_CH_STRUCT78_CH	0x40299380	0x00000040	P-DMA#1 channel #78
228	DW1_CH_STRUCT79_CH	0x402993C0	0x00000040	P-DMA#1 channel #79
229	DW1_CH_STRUCT80_CH	0x40299400	0x00000040	P-DMA#1 channel #80
230	DW1_CH_STRUCT81_CH	0x40299440	0x00000040	P-DMA#1 channel #81
231	DW1_CH_STRUCT82_CH	0x40299480	0x00000040	P-DMA#1 channel #82
232	DW1_CH_STRUCT83_CH	0x402994C0	0x00000040	P-DMA#1 channel #83
233	DMAC_TOP	0x402A0000	0x00000010	M-DMA#0 main
234	DMAC_CH0_CH	0x402A1000	0x00000100	M-DMA#0 channel #0
235	DMAC_CH1_CH	0x402A1100	0x00000100	M-DMA#0 channel #1
236	DMAC_CH2_CH	0x402A1200	0x00000100	M-DMA#0 channel #2
237	DMAC_CH3_CH	0x402A1300	0x00000100	M-DMA#0 channel #3
238	EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
239	EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
240	BIST	0x402F0000	0x00001000	Built-in self test
241	HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOM port #0
242	HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOM port #1
243	HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOM port #2
244	HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOM port #3
245	HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOM port #4
246	HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOM port #5
247	HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOM port #6
248	HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOM port #7
249	HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOM port #8
250	HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOM port #9
251	HSIOM_PRT10_PRT	0x403000A0	0x00000008	HSIOM port #10
252	HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOM port #11
253	HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOM port #12
254	HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOM port #13
255	HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOM port #14
256	HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOM port #15
257	HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOM port #16
258	HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOM port #17

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
259	HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOM port #18
260	HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOM port #19
261	HSIOM_AMUX	0x40302000	0x00000010	HSIOM analog multiplexer
262	HSIOM_MON	0x40302200	0x00000010	HSIOM monitor
263	GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_STD port #0
264	GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD port #1
265	GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD port #2
266	GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_STD port #3
267	GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD port #4
268	GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_SMC port #5
269	GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_SMC port #6
270	GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_SMC port #7
271	GPIO_PRT8_PRT	0x40310400	0x00000040	HSIO_STDLN port #8
272	GPIO_PRT9_PRT	0x40310480	0x00000040	HSIO_STDLN port #9
273	GPIO_PRT10_PRT	0x40310500	0x00000040	GPIO_STD port #10
274	GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_STD port #11
275	GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_STD port #12
276	GPIO_PRT13_PRT	0x40310680	0x00000040	GPIO_STD port #13
277	GPIO_PRT14_PRT	0x40310700	0x00000040	GPIO_ENH port #14
278	GPIO_PRT15_PRT	0x40310780	0x00000040	GPIO_STD port #15
279	GPIO_PRT16_PRT	0x40310800	0x00000040	GPIO_STD port #16
280	GPIO_PRT17_PRT	0x40310880	0x00000040	GPIO_STD port #17
281	GPIO_PRT18_PRT	0x40310900	0x00000040	GPIO_STD port #18
282	GPIO_PRT19_PRT	0x40310980	0x00000040	GPIO_STD port #19
283	GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_STD port #0 configuration
284	GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD port #1 configuration
285	GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD port #2 configuration
286	GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_STD port #3 configuration
287	GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD port #4 configuration
288	GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_SMC port #5 configuration
289	GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_SMC port #6 configuration
290	GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_SMC port #7 configuration
291	GPIO_PRT8_CFG	0x40310440	0x00000040	HSIO_STDLN port #8 configuration

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
292	GPIO_PRT9_CFG	0x403104C0	0x00000040	HSIO_STDLN port #9 configuration
293	GPIO_PRT10_CFG	0x40310540	0x00000020	GPIO_STD port #10 configuration
294	GPIO_PRT11_CFG	0x403105C0	0x00000020	GPIO_STD port #11 configuration
295	GPIO_PRT12_CFG	0x40310640	0x00000020	GPIO_STD port #12 configuration
296	GPIO_PRT13_CFG	0x403106C0	0x00000020	GPIO_STD port #13 configuration
297	GPIO_PRT14_CFG	0x40310740	0x00000020	GPIO_ENH port #14 configuration
298	GPIO_PRT15_CFG	0x403107C0	0x00000020	GPIO_STD port #15 configuration
299	GPIO_PRT16_CFG	0x40310840	0x00000020	GPIO_STD port #16 configuration
300	GPIO_PRT17_CFG	0x403108C0	0x00000020	GPIO_STD port #17 configuration
301	GPIO_PRT18_CFG	0x40310940	0x00000020	GPIO_STD port #18 configuration
302	GPIO_PRT19_CFG	0x403109C0	0x00000020	GPIO_STD port #19 configuration
303	GPIO_GPIO	0x40314000	0x00000040	GPIO main
304	GPIO_TEST	0x40315000	0x00000008	GPIO test
305	SMARTIO_PRT7_PRT	0x40320700	0x00000100	SMART I/O #7
306	TCPWM0_GRP0_CNT0_CNT	0x40380000	0x00000080	TCPWM#0 group #0, counter #0
307	TCPWM0_GRP0_CNT1_CNT	0x40380080	0x00000080	TCPWM#0 group #0, counter #1
308	TCPWM0_GRP0_CNT2_CNT	0x40380100	0x00000080	TCPWM#0 group #0, counter #2
309	TCPWM0_GRP0_CNT3_CNT	0x40380180	0x00000080	TCPWM#0 group #0, counter #3
310	TCPWM0_GRP0_CNT4_CNT	0x40380200	0x00000080	TCPWM#0 group #0, counter #4
311	TCPWM0_GRP0_CNT5_CNT	0x40380280	0x00000080	TCPWM#0 group #0, counter #5
312	TCPWM0_GRP0_CNT6_CNT	0x40380300	0x00000080	TCPWM#0 group #0, counter #6
313	TCPWM0_GRP0_CNT7_CNT	0x40380380	0x00000080	TCPWM#0 group #0, counter #7
314	TCPWM0_GRP0_CNT8_CNT	0x40380400	0x00000080	TCPWM#0 group #0, counter #8
315	TCPWM0_GRP0_CNT9_CNT	0x40380480	0x00000080	TCPWM#0 group #0, counter #9
316	TCPWM0_GRP0_CNT10_CNT	0x40380500	0x00000080	TCPWM#0 group #0, counter #10
317	TCPWM0_GRP0_CNT11_CNT	0x40380580	0x00000080	TCPWM#0 group #0, counter #11
318	TCPWM0_GRP0_CNT12_CNT	0x40380600	0x00000080	TCPWM#0 group #0, counter #12
319	TCPWM0_GRP0_CNT13_CNT	0x40380680	0x00000080	TCPWM#0 group #0, counter #13
320	TCPWM0_GRP0_CNT14_CNT	0x40380700	0x00000080	TCPWM#0 group #0, counter #14
321	TCPWM0_GRP0_CNT15_CNT	0x40380780	0x00000080	TCPWM#0 group #0, counter #15
322	TCPWM0_GRP0_CNT16_CNT	0x40380800	0x00000080	TCPWM#0 group #0, counter #16
323	TCPWM0_GRP0_CNT17_CNT	0x40380880	0x00000080	TCPWM#0 group #0, counter #17
324	TCPWM0_GRP0_CNT18_CNT	0x40380900	0x00000080	TCPWM#0 group #0, counter #18

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) **PPU 固定结构对**

Pair No.	PPU fixed structure pair	Address	Size	Description
325	TCPWM0_GRP0_CNT19_CNT	0x40380980	0x00000080	TCPWM#0 group #0, counter #19
326	TCPWM0_GRP0_CNT20_CNT	0x40380A00	0x00000080	TCPWM#0 group #0, counter #20
327	TCPWM0_GRP0_CNT21_CNT	0x40380A80	0x00000080	TCPWM#0 group #0, counter #21
328	TCPWM0_GRP0_CNT22_CNT	0x40380B00	0x00000080	TCPWM#0 group #0, counter #22
329	TCPWM0_GRP0_CNT23_CNT	0x40380B80	0x00000080	TCPWM#0 group #0, counter #23
330	TCPWM0_GRP0_CNT24_CNT	0x40380C00	0x00000080	TCPWM#0 group #0, counter #24
331	TCPWM0_GRP0_CNT25_CNT	0x40380C80	0x00000080	TCPWM#0 group #0, counter #25
332	TCPWM0_GRP0_CNT26_CNT	0x40380D00	0x00000080	TCPWM#0 group #0, counter #26
333	TCPWM0_GRP0_CNT27_CNT	0x40380D80	0x00000080	TCPWM#0 group #0, counter #27
334	TCPWM0_GRP0_CNT28_CNT	0x40380E00	0x00000080	TCPWM#0 group #0, counter #28
335	TCPWM0_GRP0_CNT29_CNT	0x40380E80	0x00000080	TCPWM#0 group #0, counter #29
336	TCPWM0_GRP0_CNT30_CNT	0x40380F00	0x00000080	TCPWM#0 group #0, counter #30
337	TCPWM0_GRP0_CNT31_CNT	0x40380F80	0x00000080	TCPWM#0 group #0, counter #31
338	TCPWM0_GRP0_CNT32_CNT	0x40381000	0x00000080	TCPWM#0 group #0, counter #32
339	TCPWM0_GRP0_CNT33_CNT	0x40381080	0x00000080	TCPWM#0 group #0, counter #33
340	TCPWM0_GRP1_CNT0_CNT	0x40388000	0x00000080	TCPWM#0 group #1, counter #0
341	TCPWM0_GRP1_CNT1_CNT	0x40388080	0x00000080	TCPWM#0 group #1, counter #1
342	TCPWM0_GRP1_CNT2_CNT	0x40388100	0x00000080	TCPWM#0 group #1, counter #2
343	TCPWM0_GRP1_CNT3_CNT	0x40388180	0x00000080	TCPWM#0 group #1, counter #3
344	TCPWM0_GRP1_CNT4_CNT	0x40388200	0x00000080	TCPWM#0 group #1, counter #4
345	TCPWM0_GRP1_CNT5_CNT	0x40388280	0x00000080	TCPWM#0 group #1, counter #5
346	TCPWM0_GRP1_CNT6_CNT	0x40388300	0x00000080	TCPWM#0 group #1, counter #6
347	TCPWM0_GRP1_CNT7_CNT	0x40388380	0x00000080	TCPWM#0 group #1, counter #7
348	TCPWM0_GRP1_CNT8_CNT	0x40388400	0x00000080	TCPWM#0 group #1, counter #8
349	TCPWM0_GRP1_CNT9_CNT	0x40388480	0x00000080	TCPWM#0 group #1, counter #9
350	TCPWM0_GRP1_CNT10_CNT	0x40388500	0x00000080	TCPWM#0 group #1, counter #10
351	TCPWM0_GRP1_CNT11_CNT	0x40388580	0x00000080	TCPWM#0 group #1, counter #11
352	TCPWM0_GRP2_CNT0_CNT	0x40390000	0x00000080	TCPWM#0 group #2, counter #0
353	TCPWM0_GRP2_CNT1_CNT	0x40390080	0x00000080	TCPWM#0 group #2, counter #1
354	TCPWM0_GRP2_CNT2_CNT	0x40390100	0x00000080	TCPWM#0 group #2, counter #2
355	TCPWM0_GRP2_CNT3_CNT	0x40390180	0x00000080	TCPWM#0 group #2, counter #3
356	TCPWM0_GRP2_CNT4_CNT	0x40390200	0x00000080	TCPWM#0 group #2, counter #4
357	TCPWM0_GRP2_CNT5_CNT	0x40390280	0x00000080	TCPWM#0 group #2, counter #5

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) **PPU 固定结构对**

Pair No.	PPU fixed structure pair	Address	Size	Description
358	TCPWM0_GRP2_CNT6_CNT	0x40390300	0x00000080	TCPWM#0 group #2, counter #6
359	TCPWM0_GRP2_CNT7_CNT	0x40390380	0x00000080	TCPWM#0 group #2, counter #7
360	TCPWM0_GRP2_CNT8_CNT	0x40390400	0x00000080	TCPWM#0 group #2, counter #8
361	TCPWM0_GRP2_CNT9_CNT	0x40390480	0x00000080	TCPWM#0 group #2, counter #9
362	TCPWM0_GRP2_CNT10_CNT	0x40390500	0x00000080	TCPWM#0 group #2, counter #10
363	TCPWM0_GRP2_CNT11_CNT	0x40390580	0x00000080	TCPWM#0 group #2, counter #11
364	TCPWM0_GRP2_CNT12_CNT	0x40390600	0x00000080	TCPWM#0 group #2, counter #12
365	TCPWM0_GRP2_CNT13_CNT	0x40390680	0x00000080	TCPWM#0 group #2, counter #13
366	TCPWM0_GRP2_CNT14_CNT	0x40390700	0x00000080	TCPWM#0 group #2, counter #14
367	TCPWM0_GRP2_CNT15_CNT	0x40390780	0x00000080	TCPWM#0 group #2, counter #15
368	LCD0	0x403B0000	0x00010000	Segment LCD Controller#0
369	EVTGEN0	0x403F0000	0x00001000	Event generator #0
370	SMIF0_MAIN	0x40420000	0x00001000	Serial Memory Interface #0
371	LIN0_MAIN	0x40500000	0x00000008	LIN#0, main
372	LIN0_CH0_CH	0x40508000	0x00000100	LIN#0, channel #0
373	LIN0_CH1_CH	0x40508100	0x00000100	LIN#0, channel #1
374	CXPI0_MAIN	0x40510000	0x00000008	CXPI#0, main
375	CXPI0_CH0_CH	0x40518000	0x00000100	CXPI#0, channel #0
376	CXPI0_CH1_CH	0x40518100	0x00000100	CXPI#0, channel #1
377	CANFD0_CH0_CH	0x40520000	0x00000200	CAN#0, channel #0
378	CANFD0_CH1_CH	0x40520200	0x00000200	CAN#0, channel #1
379	CANFD1_CH0_CH	0x40540000	0x00000200	CAN#1, channel #0
380	CANFD1_CH1_CH	0x40540200	0x00000200	CAN#1, channel #1
381	CANFD0_MAIN	0x40521000	0x00000100	CAN#0 main
382	CANFD1_MAIN	0x40541000	0x00000100	CAN#1 main
383	CANFD0_BUF	0x40530000	0x00010000	CAN#0 buffer
384	CANFD1_BUF	0x40550000	0x00010000	CAN#1 buffer
385	SCB0	0x40600000	0x00010000	Serial communication block#0
386	SCB1	0x40610000	0x00010000	Serial communication block#1
387	SCB2	0x40620000	0x00010000	Serial communication block#2
388	SCB3	0x40630000	0x00010000	Serial communication block#3
389	SCB4	0x40640000	0x00010000	Serial communication block#4
390	SCB5	0x40650000	0x00010000	Serial communication block#5

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) PPU 固定结构对

Pair No.	PPU fixed structure pair	Address	Size	Description
391	SCB6	0x40660000	0x00010000	Serial communication block#6
392	SCB7	0x40670000	0x00010000	Serial communication block#7
393	SCB8	0x40680000	0x00010000	Serial communication block#8
394	SCB9	0x40690000	0x00010000	Serial communication block#9
395	SCB10	0x406A0000	0x00010000	Serial communication block#10
396	SCB11	0x406B0000	0x00010000	Serial communication block#11
397	TDM0_TDM_STRUCT0_TDM_TX_S TRUCT_TX	0x40818000	0x00000100	TDM#0 TX structure #0
398	TDM0_TDM_STRUCT1_TDM_TX_S TRUCT_TX	0x40818200	0x00000100	TDM#0 TX structure #1
399	TDM0_TDM_STRUCT0_TDM_RX_S TRUCT_RX	0x40818100	0x00000100	TDM#0 RX structure #0
400	TDM0_TDM_STRUCT1_TDM_RX_S TRUCT_RX	0x40818300	0x00000100	TDM#0 RX structure #1
401	SG0_SG_STRUCT0_TX	0x40828000	0x00000100	SG#0 TX structure #0
402	SG0_SG_STRUCT1_TX	0x40828100	0x00000100	SG#0 TX structure #1
403	SG0_SG_STRUCT2_TX	0x40828200	0x00000100	SG#0 TX structure #2
404	SG0_SG_STRUCT3_TX	0x40828300	0x00000100	SG#0 TX structure #3
405	SG0_SG_STRUCT4_TX	0x40828400	0x00000100	SG#0 TX structure #4
406	PWM0_MAIN	0x40830000	0x00000010	PWM#0 Main
407	PWM0_TX0_TX	0x40838000	0x00000100	PWM#0 TX0
408	PWM0_TX1_TX	0x40838100	0x00000100	PWM#0 TX1
409	MIXER0_MIXER_SRC_STRUCT0_S RC	0x40888000	0x00000100	MIXER#0 source structure #0
410	MIXER0_MIXER_SRC_STRUCT1_S RC	0x40888100	0x00000100	MIXER#0 source structure #1
411	MIXER0_MIXER_SRC_STRUCT2_S RC	0x40888200	0x00000100	MIXER#0 source structure #2
412	MIXER0_MIXER_SRC_STRUCT3_S RC	0x40888300	0x00000100	MIXER#0 source structure #3
413	MIXER0_MIXER_SRC_STRUCT4_S RC	0x40888400	0x00000100	MIXER#0 source structure #4
414	MIXER0_MIXER_DST_STRUCT_D S T	0x4088C000	0x00000100	MIXER#0 destination structure
415	PASS0_SAR0_SAR	0x40900000	0x00000400	PASS SAR#0
416	PASS0_SAR1_SAR	0x40901000	0x00000008	PASS SAR#1

(表格续下页.....)

23 外设保护单位固定结构对

表 25 (续) **PPU 固定结构对**

Pair No.	PPU fixed structure pair	Address	Size	Description
417	PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR#0, channel #0
418	PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR#0, channel #1
419	PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR#0, channel #2
420	PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR#0, channel #3
421	PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR#0, channel #4
422	PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR#0, channel #5
423	PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR#0, channel #6
424	PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR#0, channel #7
425	PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR#0, channel #8
426	PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR#0, channel #9
427	PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR#0, channel #10
428	PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR#0, channel #11
429	PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR#0, channel #12
430	PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR#0, channel #13
431	PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR#0, channel #14
432	PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR#0, channel #15
433	PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR#0, channel #16
434	PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR#0, channel #17
435	PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR#0, channel #18
436	PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR#0, channel #19
437	PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR#0, channel #20
438	PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR#0, channel #21
439	PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR#0, channel #22
440	PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR#0, channel #23
441	PASS0_SAR0_CH24_CH	0x40900E00	0x00000040	SAR#0, channel #24
442	PASS0_SAR0_CH25_CH	0x40900E40	0x00000040	SAR#0, channel #25
443	PASS0_SAR0_CH26_CH	0x40900E80	0x00000040	SAR#0, channel #26
444	PASS0_SAR0_CH27_CH	0x40900EC0	0x00000040	SAR#0, channel #27
445	PASS0_SAR0_CH28_CH	0x40900F00	0x00000040	SAR#0, channel #28
446	PASS0_SAR0_CH29_CH	0x40900F40	0x00000040	SAR#0, channel #29
447	PASS0_SAR0_CH30_CH	0x40900F80	0x00000040	SAR#0, channel #30
448	PASS0_SAR0_CH31_CH	0x40900FC0	0x00000040	SAR#0, channel #31
449	PASS0_TOP	0x409F0000	0x00001000	PASS0 SAR main

1) 固定 PPU 在启动内部配置, 用户不得更改此 PPU 的属性。

24 总线主控器

24 总线主控器

仲裁器（闪存控制器的一部分）根据主控标识符执行基于优先级的仲裁。每个总线主控都有一个专用的 4 位主控标识符。该主控标识符用于总线仲裁和 IPC 功能。

表 26 用于访问和保护控制的总线主控器

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for Cortex®-M0+ CPU
1	CPUSS_MS_ID_CRYPT0	Master ID for crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA#0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA#1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA#0
14	CPUSS_MS_ID_CM4	Master ID for Cortex®-M4F CPU
15	CPUSS_MS_ID_TC	Master ID for DAP tap controller

25 杂项配置

25 杂项配置

表 27 CYT2CL 器件的杂项配置

Sl. No.	Configuration	Number/ instances	Description
0	SRSS_NUM_CLKPATH	6	Number of clock paths. One for each of FLL, PLL, Direct and CSV
1	SRSS_NUM_HFROOT	6	Number of CLK_HFs roots present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_CLOCK_NR	85	Number of programmable clocks (outputs)
4	PERI_DIV_8_NR	11	Number of divide-by-8 clock dividers
5	PERI_DIV_16_NR	16	Number of divide-by-16 clock dividers
	PERI_DIV_16_5_NR	4	Number of divide-by-16.5 clock dividers
6	PERI_DIV_24_5_NR	11	Number of divide-by-24.5 clock dividers
7	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
8	CPUSS_CM4_MPU_NR	8	Number of MPU regions in CM4
9	CPUSS_CRYPT0_BUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
10	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
11	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM4 access 2 - Reserved for DAP access Remaining for user purposes
12	SCB0_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode
13	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of SMPU protection structures
14	TCPWM_TR_ONE_CNT_NR	1	Number of input triggers per counter, routed to one counter
15	TCPWM_TR_ALL_CNT_NR	60	Number of input triggers routed to all counters, based on the pin package
16	TCPWM_GRP_NR	3	Number of TCPWM#0 counter groups
17	TCPWM_GRP_NR0_GRP_GRP_CNT_N R	34	Number of counters per TCPWM#0 group #0

(表格续下页.....)

25 杂项配置

表 27 (续) CYT2CL 器件的杂项配置

Sl. No.	Configuration	Number/ instances	Description
18	TCPWM_GRP_NR0_CNT_GRP_CNT_W IDTH	16	Counter width in number of bits per TCPWM#0 group #0
19	TCPWM_GRP_NR1_GRP_GRP_CNT_N R	12	Number of counters per TCPWM#0 group #1
20	TCPWM_GRP_NR1_CNT_GRP_CNT_W IDTH	16	Counter width in number of bits per TCPWM#0 group #1
21	TCPWM_GRP_NR2_GRP_GRP_CNT_N R	16	Number of counters per TCPWM#0 group #2
22	TCPWM_GRP_NR2_CNT_GRP_CNT_W IDTH	32	Counter width in number of bits per TCPWM#0 group #2
23	CANFD0_MRAM_SIZE/ CANFD1_MRAM_SIZE	16	Message RAM size in kB shared by all the channels
24	EVTGEN_COMP_STRUCT_NR	16	Number of event generator comparator structures

26 开发支持

CYT2CL 拥有丰富的文档、编程工具和在线资源，协助开发过程。请访问 www.infineon.com 了解更多信息。

26.1 文档

一系列文档支持 CYT2CL，确保您能够快速找到问题的答案。本节列出了一些关键文档。

26.1.1 软件用户指南

使用示例驱动程序库以及第三方 IDE（例如 IAR EWARM 和 GHS Multi）的分步指南。

26.1.2 技术参考手册

技术参考手册（TRM）包含使用 CYT2CL 器件所需的所有技术细节，包括所有寄存器的完整描述。TRM 可在 www.infineon.com 的文档部分找到。

26.2 工具

CYT2CL 受第三方开发工具生态系统（如 IAR 和 GHS）支持。英飞凌的编程工具也支持 CYT2CL，可使用英飞凌的 MiniProg4 或 Segger J-link 进行编程、擦除或读取。更多详细信息请参阅 www.infineon.com 中的文档部分。

27 电气规范

27 电气规格

27.1 绝对最大额定值

在表 28 所列最小和最大限制之外的条件下使用本设备，可能会对设备造成永久性损坏。长时间暴露在表 28 限制范围内但超出正常操作限制的条件下，可能会影响器件的可靠性。最高存储温度为 150°C，符合 JEDEC 标准 JESD22-A103 "高温存储寿命"。如果在表 28 的限制条件下运行，但超出正常运行的限制条件，器件可能无法按规格运行。

功率考虑因素

平均芯片结温 T_J 以 °C 为单位可采用公式 1 计算：

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

其中：

T_A 是环境温度，单位为 °C。

θ_{JA} 是封装结点至环境的热阻，单位为 °C/W。 P_D 是 P_{INT} 与 P_{IO} 之和 ($P_D = P_{INT} + P_{IO}$)。

P_{INT} 是芯片内部功率。 ($P_{INT} = V_{DDD} \times I_{DD} + V_{DDA_ADC} \times I_{VDDA}$)

P_{IO} 表示输入和输出引脚上的功耗；由用户确定。对于大多数应用， $P_{IO} < P_{INT}$ 可以被忽略。

另一方面，如果器件配置为连续驱动外部模块和/或存储器，则 P_{IO} 可能很重要。

表 28 绝对最大额定值

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID10	VDDD_ABS	Power supply voltage (V _{DDD}) ¹⁾	V _{SS} - 0.3	–	V _{SS} + 6.0	V	See for assignment of ports to supply domains
SID10A	VDDIO_GPIO_ABS	Power supply voltage (V _{DDIO_GPIO}) ¹⁾	V _{SS} - 0.3	–	V _{SS} + 6.0	V	See Table 5 for assignment of ports to supply domains
SID10B	VDDIO_SMC_ABS	Power supply voltage (V _{DDIO_SMC}) ¹⁾	V _{SS} - 0.3	–	V _{SS} + 6.0	V	See Table 5 for assignment of ports to supply domains
SID10C	VDDIO_HSIO_ABS	Power supply voltage (V _{DDIO_HSIO}) ¹⁾	V _{SS} - 0.3	–	V _{SS} + 6.0	V	See Table 5 for assignment of ports to supply domains
SID11	VDDA_ADC_ABS	Analog power supply voltage (V _{DDA_ADC}) ¹⁾ Supply for SAR ADC	V _{SSA_ADC} - 0.3	–	V _{SSA_ADC} + 6.0	V	

(表格续下页.....)

27 电气规范

表 28 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID12	VREFH_ABS	SAR analog reference voltage, HIGH ¹⁾	$V_{SSA_ADC} - 0.3$	–	$V_{SSA_ADC} + 6.0$	V	$V_{REFH} \leq V_{DDA_ADC} + 0.3 \text{ V}$
SID12A	VREFL_ABS	SAR analog reference voltage, LOW ¹⁾	$V_{SSA_ADC} - 0.3$	–	$V_{SSA_ADC} + 0.3$	V	
SID13	VCCD_ABS	Power supply voltage (V_{CCD})	$V_{SS} - 0.3$	–	$V_{SS} + 1.21$	V	
SID15A	VI_GPIO_ABS	Input voltage ¹⁾	$V_{SS} - 0.5$	–	$V_{DDIO_GP_{IO}} + 0.5$	V	See Table 5 for assignment of ports to supply domains
SID15B	VI_SMC_ABS	Input voltage ¹⁾	$V_{SS} - 0.5$	–	$V_{DDIO_S_{MC}} + 0.5$	V	See Table 5 for assignment of ports to supply domains
SID15C	VI_HSIO_ABS	Input voltage ¹⁾	$V_{SS} - 0.5$	–	$V_{DDIO_HS_{IO}} + 0.5$	V	See Table 5 for assignment of ports to supply domains
SID16	VI_ADC_ABS	Analog input voltage ¹⁾	$V_{SSA_ADC} - 0.3$	–	$V_{DDA_ADC} + 0.3$	V	See Table 5 for assignment of ports to supply domains
SID17A	VO_GPIO_ABS	Output voltage ¹⁾	$V_{SS} - 0.3$	–	$V_{DDIO_GP_{IO}} + 0.3$	V	See Table 5 for assignment of ports to supply domains
SID17B	VO_SMC_ABS	Output voltage ¹⁾	$V_{SS} - 0.3$	–	$V_{DDIO_S_{MC}} + 0.3$	V	See Table 5 for assignment of ports to supply domains
SID17C	VO_HSIO_ABS	Output voltage ¹⁾	$V_{SS} - 0.3$	–	$V_{DDIO_HS_{IO}} + 0.3$	V	See Table 5 for assignment of ports to supply domains
SID18	I _{CLAMP_ABS}	Maximum clamp current ^{2), 3), 4), 5)}	–5	–	5	mA	Applicable to GPIO pins
SID18A	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to GPIO pins in total for V_{DDIO_GPIO}
SID18B	I _{CLAMP_ABS}	Maximum clamp current ^{2), 3), 4), 5)}	–52	–	52	mA	Applicable to SMC I/O pins

(表格续下页.....)

27 电气规范

表 28 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID18C	ΣI_{CLAMP_ABS}	Total maximum clamp current	-624	-	624	mA	Applicable to SMC I/O pins clamping current occurred by sudden switching-off of inductive load (stepper motor coil) in total for VDDIO_SMC
SID18D	$ I_{CLAMP_ABS} $	Maximum clamp current ^{2), 3), 4), 5)}	-5	-	5	mA	Applicable to HSIO_STDLN
SID18E	ΣI_{CLAMP_ABS}	Total maximum clamp current	-25	-	25	mA	Applicable to I/O pins in total for VDDIO_HSIO
SID20	IOL1_GPIO_ABS	LOW-level maximum output current for GPIO ⁶⁾	-	-	3.5	mA	Setting is 1 mA
SID21	IOL2_GPIO_ABS	LOW-level maximum output current for GPIO ⁶⁾	-	-	7	mA	Setting is 2 mA
SID22	IOL3_GPIO_ABS	LOW-level maximum output current for GPIO ⁶⁾	-	-	10	mA	Setting is 5 mA
SID22A	IOL4_GPIO_ABS	LOW-level maximum output current for GPIO ⁶⁾	-	-	10	mA	Setting is 6 mA
SID26	$\Sigma I_{OL_GPIO_ABS}$	LOW-level total output current for GPIO ⁷⁾	-	-	50	mA	
SID26A	IOL_SMC_ABS	LOW-level maximum output current for SMC ⁸⁾	-	-	52	mA	Setting is 30 mA at -40°C
SID26B	$\Sigma I_{OL_SMC_ABS}$	LOW-level total output current for SMC ⁹⁾	-	-	300	mA	25°C < T _A ≤ 105°C
SID26I	$\Sigma I_{OL_SMC_ABS}$	LOW-level total output current for GPIO_SMC ⁹⁾	-	-	450	mA	-40°C ≤ T _A ≤ 25°C
SID26G	IOL_HSIO_ABS	LOW-level maximum output current for HSIO ¹⁰⁾	-	-	15	mA	
SID26H	$\Sigma I_{OL_HSIO_ABS}$	LOW-level total output current for HSIO ¹¹⁾	-	-	150	mA	

(表格续下页.....)

27 电气规范

表 28 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID27	IOH1_GPIO_ABS	HIGH-level maximum output current for GPIO ⁶⁾	–	–	–3.5	mA	Setting is 1 mA
SID28	IOH2_GPIO_ABS	HIGH-level maximum output current for GPIO ⁶⁾	–	–	–7	mA	Setting is 2 mA
SID29	IOH3_GPIO_ABS	HIGH-level maximum output current for GPIO ⁶⁾	–	–	–10	mA	Setting is 5 mA
SID29A	IOH3_GPIO_ABS	HIGH-level maximum output current for GPIO ⁶⁾	–	–	–10	mA	Setting is 6 mA
SID33	Σ IOH1_GPIO_ABS	HIGH-level total output current for GPIO ⁷⁾	–	–	–50	mA	
SID33A	IOH_SMC_ABS	HIGH-level maximum output current for SMC ⁸⁾	–	–	–52	mA	Setting is 30 mA at –40°C
SID33B	Σ IOH_SMC_ABS	HIGH-level total output current for SMC ⁹⁾	–	–	–300	mA	25°C < T _A ≤ 105°C
SID33I	Σ IOH_SMC_ABS	HIGH-level total output current for SMC	–	–	–450	mA	–40°C < T _A ≤ 25°C
SID33G	IOH_HSIO_ABS	HIGH-level maximum output current for HSIO ¹⁰⁾	–	–	–15	mA	
SID33H	Σ IOH_HSIO_ABS	HIGH-level total output current for HSIO ¹¹⁾	–	–	–150	mA	
SID34_3	P _D	Power dissipation	–	–	1800	mW	
SID36	T _A	Operating ambient temperature	–40	–	105	°C	For S-grade devices
SID38	T _{STG}	Storage temperature	–55	–	150	°C	
SID39	T _J	Operating junction temperature	–40	–	150	°C	
SID39A	V _{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	

(表格续下页.....)

27 电气规范

表 28 (续) 绝对最大额定值

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID39B 1	VESD_CDM1	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B 2	VESD_CDM2	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	ILU	The maximum pin current the device can tolerate before triggering a latch-up	–100	–	100	mA	

- 1) 这些参数基于 $V_{SS} = V_{SSA_ADC} = 0.0\text{ V}$ 的条件。
- 2) 必须设置一个限流电阻器，以确保 I/O 引脚上的电流在任何时候都不超过额定值，包括电源瞬变期间。有关推荐电路的更多信息，可参见图 27-4。
- 3) VDDIO 必须有足够的负载或保护，以防止钳位电流将其拉高到正常工作范围之外。
- 4) 钳位电流只能在器件通电时施加，并且只能施加在每对 VDDIO/VSSIO 引脚之间的端口上（ADC 引脚、ECO_IN/OUT、LPECO_IN/LPECO_OUT、WCO_IN/OUT 和 XRES_L 除外）。
- 5) 当满足 2), 3), 4) 和 SID18/A/B/C/D/E 的条件时， $|I_{CLAMP_ABS}|$ 取代 V_{I_ABS} 。
- 6) 最大输出电流是流过任何一个 GPIO I/O 的峰值电流。
- 7) 总输出电流是流过所有 GPIO I/O (GPIO_STD 和 GPIO_ENH) 的最大电流。
- 8) 最大输出电流是流过任何一个 SMC I/O 的峰值电流。
- 9) 总输出电流是流过所有 SMC I/O (GPIO_SMC) 的最大电流。
- 10) 最大输出电流是流过任何一个 HSIO I/O 的峰值电流。
- 11) 总输出电流是流过所有 HSIO I/O (HSIO_STDLN) 的最大电流。

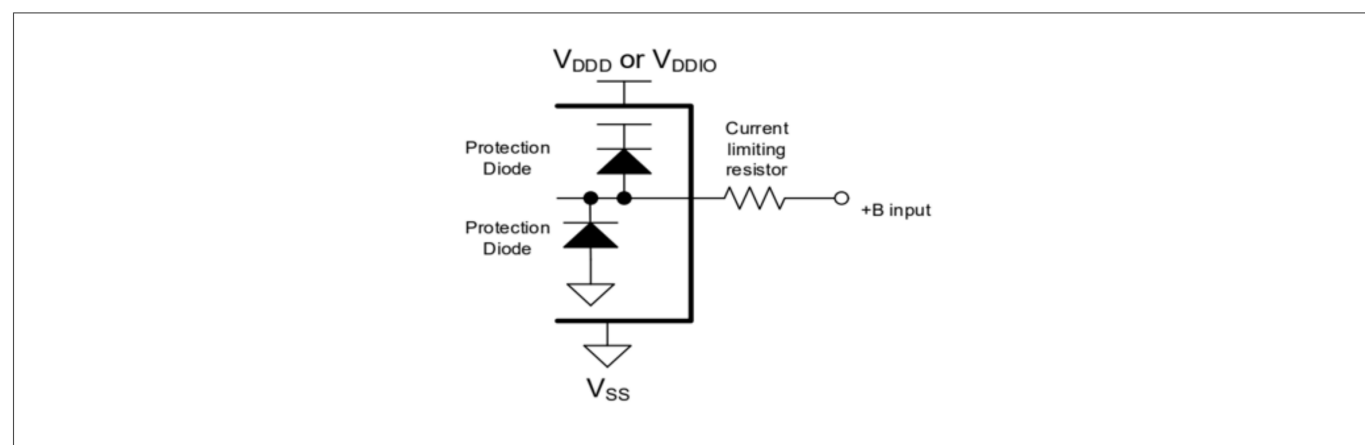


图 10 推荐电路示例 ¹⁵⁾

警告：

半导体器件可能因施加超过绝对最大额定值的压力（包括但不限于电压、电流或温度）而导致永久损坏。不要超过任何这些额定值。

¹⁵⁾ +B 是电池正极电压，约为 45 V。

27 电气规范

27.2 推荐工作条件

表 29 器件级规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
Recommended operating conditions							
SID40	V _{DDD} , V _{DDA_ADC} , V _{DDIO_GPIO} , V _{DDIO_SMC}	Power supply voltage ¹⁾	2.7 ²⁾	-	5.5 ³⁾	V	
SID40M	V _{DDD}	Power supply voltage	2.7 ²⁾	-	3.6	V	When using I2S or TDM or (PCM)PWM
SID40A	V _{DDIO_EFP}	Power supply voltage for eFuse programming ⁴⁾	3	-	5.5	V	V _{DDD} for this product, when programming eFuses
SID40B	V _{DDIO_HSIO}	Power supply voltage	3.0	3.3	3.6	V	
SID41A	C _{S1}	Smoothing capacitor ^{5), 6)}	3.76	10	11	μF	

- 1) 当 SARMUX0 启用时，确保 $V_{DDIO_GPIO} \geq 0.8 \times V_{DDA_ADC0}$
- 2) 支持 3.0 V ±10% 的电压范围，提供较低的 BOD 设置选项。此设置可为内部和接口时序提供稳健的保护，但 BOD 复位会在电压低于指定工作条件时发生。可提供更高的 BOD 设置选项（与低至 3.0 V 的电压一致），确保满足所有运行条件。
- 3) 5.0 V ±10% 支持更高的 OVD 设置选项。此设置可为内部和接口时序提供稳健的保护，但 OVD 复位会在电压高于指定工作条件时发生。可选择较低的 OVD 设置（最高 5.0 V），确保满足所有运行条件。允许 V_{DDD} 和 V_{DDA_ADC} 的电压过冲至更高的 OVD 设置范围，但累计持续时间不得超过 2 小时。注：在过冲电压条件下，电气参数无法得到保证。
- 4) eFuse 编程必须在部件处于“安静”状态时进行，尽量减少活动（最好只有 JTAG 或单个 LIN/CAN 通道在 V_{DDD} 域）。
- 5) 每个芯片都需要一个平滑电容 CS1（而不是每个 VCCD 引脚）。VCCD 引脚必须连接在一起，以确保低阻抗连接（参见图 11 中的要求）。
- 6) 用于电源去耦或滤波的电容器在连续直流偏置下运行。许多使用直流电源的电容器提供的电容小于其目标电容，并且其电容在其工作电压范围内不是恒定的。选择用于此设备的电容器时，请确保所选组件在设计中使用的特定温度和电压工作条件下提供所需的电容。虽然温度系数通常可以在零件目录中找到（例如 X7R、C0G、Y5V），但匹配的电压系数可能仅在组件数据表上提供或直接从制造商处获得。在实际运行条件下使用不能提供所需电容的组件可能会导致器件运行不符合数据表规格。

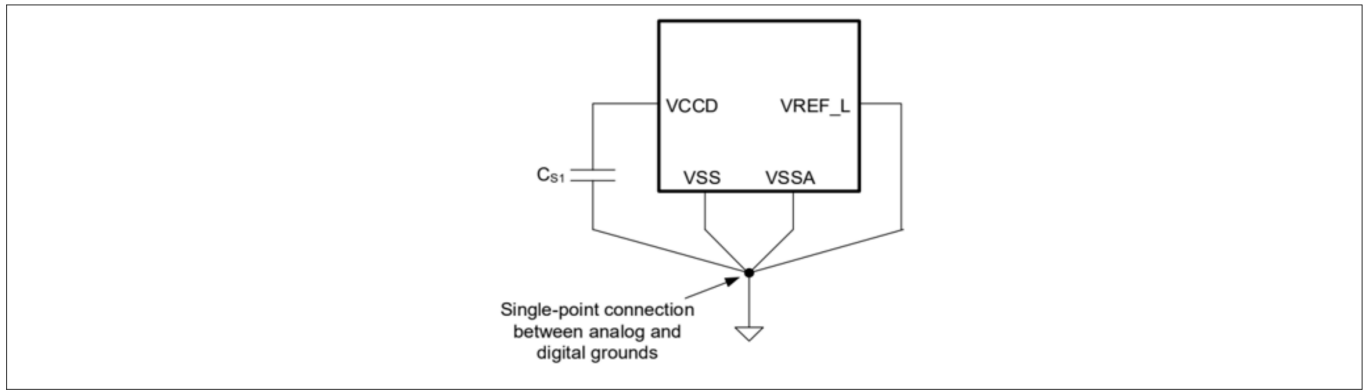


图 11 平滑电容器

27 电气规范

27.3 DC 规格

除非另有说明，所有规格均适用于 $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 和 2.7 V 至 5.5 V。

表 30 DC 规格、CPU 电流和转换时间规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Unit	Details/conditions
SID56_2	I _{DD1}	Execute from flash; Cortex®-M4F CPU in Active mode, all peripherals enabled	–	52	140	mA	Typ: $T_A = 25^{\circ}\text{C}$, $V_{\text{DDD}} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 105^{\circ}\text{C}$, $T_J = 150^{\circ}\text{C}$, $V_{\text{DDD}} = 5.5\text{ V}$, process worst (FF) (Maximum expected V_{DDD} when $T_J = 150^{\circ}\text{C}$ is reached due to self-heating)
SID50A_2	I _{DD1}	Cortex®-M4F/M0+ CPUs in Sleep mode	–	7	26	mA	Clocks running at max frequency, All CPUs in Sleep mode. All peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: $T_A = 25^{\circ}\text{C}$, $V_{\text{DDD}} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 85^{\circ}\text{C}$, $V_{\text{DDD}} = 5.5\text{ V}$, process worst (FF)
SID50C_2	I _{DD1}	Cortex®-M4F/M0+ CPUs in Sleep mode (room temp)	–	–	12	mA	Clocks running at max frequency, All CPUs in Sleep mode. All peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No I/O toggling. Max: $T_A = 25^{\circ}\text{C}$, $V_{\text{DDD}} = 5.5\text{ V}$, process worst (FF)
SID59_2	I _{DD_DS32A}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode	–	140	–	μA	Deep Sleep mode (RTC at 32 kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), Typ: $T_A = 25^{\circ}\text{C}$, $V_{\text{DDD}} = 5.0\text{ V}$, process typ (TT)
SID59A_2	I _{DD_DS32A}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode (room temp)	–	–	240	μA	Deep Sleep mode (RTC at 32 kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), Max: $V_{\text{DDD}} = 5.5\text{ V}$, $T_A = 25^{\circ}\text{C}$, process worst (FF)

(表格续下页.....)

27 电气规范

表 30 (续) DC 规格、CPU 电流和转换时间规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Unit	Details/conditions
SID60_2	I _{DD_DS32B}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode	–	–	920	μA	DeepSleep mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled), Max: V _{DD} = 5.5 V, T _A = 85°C, process worst (FF)
SID64_2	I _{DD_DS32C}	32 KB SRAM retention, ILO operation in DeepSleep mode	–	40	750	μA	DeepSleep mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) Typ: T _A = 25°C, V _{DD} = 5.0 V, process typ (TT) Max: T _A = 85°C, V _{DD} = 5.5 V, process worst (FF)
SID64A_2	I _{DD_DS32D}	32 KB SRAM retention, ILO operation in DeepSleep mode (room temp)	–	–	140	μA	DeepSleep mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) Max: T _A = 25°C, V _{DD} = 5.5 V, process worst (FF)

Hibernate mode

SID66	I _{DD_HIB1}	V _{DD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	20	μA	T _A = 25°C using ILO, V _{DD} = 5.0 V
SID66A	I _{DD_HIB2}	V _{DD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	40	μA	T _A = 25°C, using WCO, V _{DD} = 5.0 V
SID66B	I _{DD_HIB3}	V _{DD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	75	μA	T _A = 85°C, using WCO, V _{DD} = 5.5 V
SID66C	I _{DD_HIB4}	V _{DD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	150	μA	T _A = 25°C using LPECO 4 MHz, 20-pF load of LPECO, V _{DD} = 5.0 V
SID66D	I _{DD_HIB5}	V _{DD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	215	μA	T _A = 85°C, using LPECO 4 MHz, 20-pF load of LPECO, V _{DD} = 5.5 V

Power mode transition times

(表格续下页...)

27 电气规范

表 30 (续) DC 规格、CPU 电流和转换时间规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Unit	Details/conditions
SID69	t _{ACT_DS}	Power down time from ACTIVE to DEEPSLEEP (using the internal regulator)	–	–	2.5	μs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID67	t _{DS_ACT}	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	26	μs	When using 8 MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T _A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs
SID67A	t _{DS_ACT_FLL}	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	26	μs	When using FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T _A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs

(表格续下页.....)

27 电气规范

表 30 (续) DC 规格、CPU 电流和转换时间规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID67B	tDS_ACT_PLL	DeepSleep to Active transition time (PLL clock)	–	–	60	µs	When using PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until PLL locks. $T_A \geq -5^\circ\text{C}$ Note: <i>At temperatures below -5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs</i>
SID68	tHIB_ACT	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	265	µs	Without boot runtime. Guaranteed by design
SID68A	tLVR_ACT	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot	8	–	10	µs	Without boot runtime. Guaranteed by design
SID68B	tLVR_DS	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	µs	Without boot runtime. Guaranteed by design
SID79	tHIBWAKEUP_PW	Pulse width for wakeup from Hibernate mode on HIBERANTE_WAKEUP pins	90	–	–	ns	Guaranteed by design
SID80A_2	trB_N	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	2600	µs	FAST_BOOT = 0, CM0+ clocked at 50 MHz

(表格续下页.....)

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表 30 (续) DC 规格、CPU 电流和转换时间规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Unit	Details/conditions
SID80B_2	t _{RB_S}	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	3800	μs	FAST_BOOT = 0, CM0+ clocked at 50 MHz
SID81A_2	t _{FB}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	110	μs	FAST_BOOT = 0, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz, Listen window = 0 ms
SID81B_2	t _{FB_A}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	9800	μs	FAST_BOOT = 0, TOC2_FLAGS = 0x24F, CM0+ clocked at 50 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-2048.
SID81C_2	t _{FB_B}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	17000	μs	FAST_BOOT = 0, TOC2_FLAGS = 0x24F, CM0+ clocked at 50 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 384 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-3072.

Regulator specifications

SID600	V _{CCD}	Internal regulator core supply voltage (transient range)	1.05	1.1	1.15	V	
SID601_2	I _{DDD_ACT}	Regulator operating current in active/sleep mode	–	80	150	μA	Guaranteed by design
SID602	I _{DDD_DPSP}	Regulator operating current in DeepSleep mode	–	1.5	20	μA	Guaranteed by design
SID603_2	I _{RUSH}	In-rush current	–	–	375	mA	Average V _{DDD} current until C _{S1} (connected to V _{CCD} pin) is charged after Active regulator is turned on.
SID604_2	I _{OUT}	Internal regulator output current for operation	–	–	150	mA	Without triggering OVD

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27.4 复位规格

表 31 XRES_L 复位

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
XRES_L DC specifications							
SID73	I _{DD_XRES}	I _{DD} when XRES_L asserted	-	-	1.7	mA	Max: T _A = 105°C, V _{DDD} = 5.5 V, process worst (FF)
SID74	V _{IH}	Input voltage HIGH threshold	0.7 × V _{DDD}	-	-	V	CMOS input
SID75	V _{IL}	Input voltage LOW threshold	-	-	0.3 × V _{DDD}	V	CMOS input
SID76	R _{PULLUP}	Pull-up resistor	7	-	20	kΩ	
SID77	C _{IN}	Input capacitance	-	-	5	pF	
SID78	V _{HYSXRES}	Input voltage hysteresis	0.05 × V _{DDD}	-	-	V	
XRES_L AC specifications							
SID70	t _{XRES_ACT}	XRES_L release to active transition time	-	-	265	μs	Without boot runtime. Guaranteed by design
SID71	t _{XRES_PW}	XRES_L pulse width	5	-	-	μs	
SID72	t _{XRES_FT}	Pulse suppression width	100	-	-	ns	

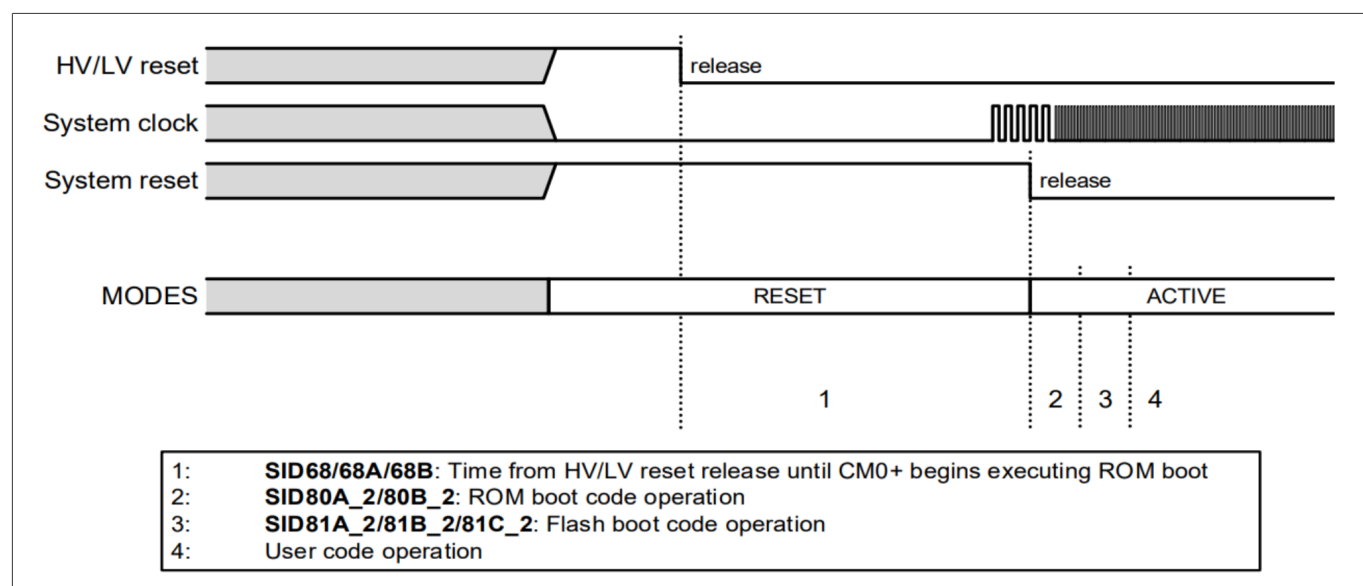


图 12 复位序列

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27.5 I/O 规格

表 32 I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
V_{DDIO_GPIO} (standard 5 V I/O) specifications for GPIO_STD ports except GPIO_ENH							
SID650	V _{OL1}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, V _{DDIO_GPIO} ≥ 4.5 V
SID651	V _{OL2}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, V _{DDIO_GPIO} ≥ 4.5 V
SID651D	V _{OL2}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID652	V _{OL3}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V _{DDIO_GPIO} ≥ 4.5 V
SID652D	V _{OL3}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID653	V _{OL4}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V _{DDIO_GPIO} ≥ 4.5 V
SID653D	V _{OL4}	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID654	V _{OH1}	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, V _{DDIO_GPIO} ≥ 4.5 V
SID654D	V _{OH1}	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID655	VOH2	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V _{DDIO_GPIO} ≥ 4.5 V
SID655D	VOH2	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID656	VOH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V _{DDIO_GPIO} ≥ 4.5 V
SID656D	VOH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID657	VOH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V _{DDIO_GPIO} ≥ 4.5 V
SID657D	VOH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID658	R _{PD}	Pull-down resistance	25	50	100	kΩ	
SID659	R _{PU}	Pull-up resistance	25	50	100	kΩ	
SID660	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID663	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V _{DDIO_GPI} 0	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID664	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b1
SID665	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V _{DDIO_GPI} 0	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPI} ≤ 5.5 V
SID666	V _{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V _{DDIO_GPI}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID668	V _{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V _{DDIO_GPI}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPI} ≤ 5.5 V
SID669	C _{in}	Input pin capacitance	–	–	5	pF	Test condition: 10/100 MHz
SID670	I _{IL}	Input leakage current	–1	–	1	μA	V _{DDIO_GPI} = V _{DDD} = V _{DDA_ADC} = 5.5 V, V _{SS} < V _I < V _{DDIO_GPI} –40°C ≤ T _A ≤ 105°C This is valid for the pin which do not have ADC input functionality.
SID671	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPI})	1	–	10	ns	CFG_OUT/DRIVE_SEL<1:0>= 0b00, 20-pF load, entire V _{DDIO_GPI} range
SID672	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPI})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0>= 0b00, 50-pF load, entire V _{DDIO_GPI} range, Guaranteed by design
SID673	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPI})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0>= 0b01, 20-pF load, entire V _{DDIO_GPI} range, Guaranteed by design

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID674	tr_F_FAST	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b10, 10-pF load, entire V _{DDIO_GPIO} range, Guaranteed by design
SID675	tr_F_FAST	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b11, 6-pF load, entire V _{DDIO_GPIO} range, Guaranteed by design

GPIO_SMC specifications (stepper motor control, 5 V I/Os)

SID650A	VOL2	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V _{DDIO_SMC} ≥ 4.5 V
SID651A	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V _{DDIO_SMC} ≥ 4.5 V
SID651E	VOL2	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID652A	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V _{DDIO_SMC} ≥ 4.5 V
SID652E	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID653A	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V _{DDIO_SMC} ≥ 4.5 V
SID653E	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID653B	VOL5	Output voltage LOW level	–	–	0.5	V	I _{OL} = 30 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, 25°C < T _A ≤ 105°C, V _{DDIO_SMC} ≥ 4.5 V
SID653C	VOL5	Output voltage LOW level	–	–	0.5	V	I _{OL} = 40 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –30°C < T _A ≤ 25°C, V _{DDIO_SMC} ≥ 4.5 V
SID653H	VOL5	Output voltage LOW level	–	–	0.5	V	I _{OL} = 52 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –40°C ≤ T _A ≤ –30°C, V _{DDIO_SMC} ≥ 4.5 V
SID654A	VOH2	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V _{DDIO_SMC} ≥ 4.5 V
SID654E	VOH2	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID656A	VOH3	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V _{DDIO_SMC} ≥ 4.5 V
SID656E	VOH3	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID657A	VOH4	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V _{DDIO_SMC} ≥ 4.5 V

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID657E	VOH4	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_SMC} < 4.5 V
SID657B	VOH5	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OL} = –30 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, 25°C < T _A ≤ 105°C, V _{DDIO_SMC} ≥ 4.5 V
SID657C	VOH5	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OL} = –40 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –30°C < T _A ≤ 25°C, V _{DDIO_SMC} ≥ 4.5 V
SID657I	VOH5	Output voltage HIGH level	V _{DDIO_SMC} – 0.5	–	–	V	I _{OL} = –52 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –40°C < T _A ≤ –30°C, V _{DDIO_SMC} ≥ 4.5 V
SID658A	R _{PD}	Pull-down resistance	25	50	100	kΩ	
SID659A	R _{PU}	Pull-up resistance	25	50	100	kΩ	
SID659B	V _{OUT}	Mid range voltage level	2.45	–	2.55	V	CFG/DRIVE_MODE<2:0> = 0b001
SID660A	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V _{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661A	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662A	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V _{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V _{DDIO_SMC} ≤ 5.5 V

(表格续下页.....)

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID663A	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V _{DDIO_SMC}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID664A	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b1
SID665A	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V _{DDIO_SMC}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_SMC} ≤ 5.5 V
SID666A	V _{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V _{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID668A	V _{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V _{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_SMC} ≤ 5.5 V
SID669A	C _{IN}	Input pin capacitance	–	–	7	pF	For 10 MHz and 100 MHz
SID670A	I _{IL}	Input leakage current	–2	–	2	μA	V _{DDIO_SMC} = V _{DDD} = 5.5 V, V _{SS} < V _I < V _{DDIO_SMC} –40°C ≤ T _A ≤ 105°C This is valid for the pin which do not have ADC input functionality.
SID673A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	–	20	ns	5-mA drive strength 20-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b01, CFG_OUT/SLOW<0:0>= 0b0, guaranteed by design
SID674A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	–	20	ns	2-mA drive strength 10-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b10, CFG_OUT/SLOW<0:0>= 0b0, guaranteed by design
SID675A	t _{R_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_SMC})	1	–	20	ns	1-mA drive strength 6-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b11, CFG_OUT/SLOW<0:0>= 0b0, guaranteed by design

(表格续下页.....)

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID676A	tr_F_SMC_SLOW	Fall time (10% to 90% of VDDIO_SMC)	15	–	80	ns	30-mA drive strength No load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676B	tr_F_SMC_SLOW	Rise time or fall time (10% to 90% of VDDIO_SMC)	25	–	100	ns	30-mA drive strength 85-pF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676C	tr_F_SMC_SLOW	Rise time or fall time (10% to 90% of VDDIO_SMC)	100	–	200	ns	30-mA drive strength 2.7-nF load, CFG_OUT/ DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1

GPIO_ENH specifications

SID650C	VOL1	Output voltage LOW level	–	–	0.6	V	I _{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, VDDIO_GPIO ≥ 4.5 V
SID650D	VOL1	Output voltage LOW level	–	–	0.4	V	I _{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, VDDIO_GPIO ≥ 4.5 V
SID651C	VOL1	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, 2.7 V ≤ VDDIO_GPIO < 4.5 V
SID652C	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, VDDIO_GPIO ≥ 4.5 V
SID652F	VOL3	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ VDDIO_GPIO < 4.5 V
SID653F	VOL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, VDDIO_GPIO ≥ 4.5 V

(表格续下页.....)

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID653G	VoL4	Output voltage LOW level	–	–	0.4	V	I _{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID654C	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, V _{DDIO_GPIO} ≥ 4.5 V
SID654G	VoH1	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID655C	VoH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V _{DDIO_GPIO} ≥ 4.5 V
SID656C	VoH3	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID657G	VoH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V _{DDIO_GPIO} ≥ 4.5 V
SID657H	VoH4	Output voltage HIGH level	V _{DDIO_GPIO} – 0.5	–	–	V	I _{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V _{DDIO_GPIO} < 4.5 V
SID658C	R _{PD}	Pull-down resistance	25	50	100	kΩ	
SID659C	R _{PU}	Pull-up resistance	25	50	100	kΩ	
SID660C	V _{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661C	V _{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID662C	V _{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V
SID663C	V _{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V _{DDIO_GPIO}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID664C	V _{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b1
SID665C	V _{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V _{DDIO_GPIO}	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V
SID666C	V _{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID668C	V _{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V _{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0>= 0b0 4.5 V ≤ V _{DDIO_GPIO} ≤ 5.5 V
SID669C	C _{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100 MHz
SID670C	I _{IL}	Input leakage current	–1	–	1	μA	V _{DDIO_GPIO} = V _{DDD} = 5.5 V, V _{SS} < V _I < V _{DDIO_GPIO} –40°C ≤ T _A ≤ 105°C
SID671C	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	10	ns	20-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b00, CFG_OUT/SLOW<0:0>= 0b0, entire V _{DDIO_GPIO} range
SID672C	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	50-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b00, CFG_OUT/SLOW<0:0>= 0b0, entire V _{DDIO_GPIO} range, Guaranteed by design
SID673C	t _{r_F_FAST}	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	20-pF load, CFG_OUT/ DRIVE_SEL<1:0>= 0b01, CFG_OUT/SLOW<0:0>= 0b0, entire V _{DDIO_GPIO} range, Guaranteed by design

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID674C	tr_F_FAST	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	10-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_OUT/SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range, Guaranteed by design
SID675C	tr_F_FAST	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	1	–	20	ns	6-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b11, CFG_OUT/SLOW<0:0> = 0b0, entire V _{DDIO_GPIO} range, Guaranteed by design
SID676E	tf_I2C_SLOW	Fall time (30% to 70% of V _{DDIO_GPIO})	20 × (V _{DDIO_GPIO} / 5.5)	–	250	ns	10-pF to 400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, minimum external R _{PU} = 400 Ω
SID677C	tr_F_SLOW	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	20 × (V _{DDIO_GPIO} / 5.5)	–	160	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 1 MHz
SID678C	tr_F_SLOW	Rise time or fall time (10% to 90% of V _{DDIO_GPIO})	20 × (V _{DDIO_GPIO} / 5.5)	–	250	ns	400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 400 kHz, Guaranteed by design

HSIO_STDLN specifications (3 V I/Os)

SID651F	VOL0	Output LOW voltage level	–	–	0.2	V	I _{OL} = 0.1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID654I	VOL1	Output LOW voltage level	–	–	0.4	V	I _{OL} = 10 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, 3.0 V ≤ V _{DDIO_HSIO} ≤ 3.6 V
SID655G	VOL2	Output LOW voltage level	–	–	0.4	V	I _{OL} = 2 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, 3.0 V ≤ V _{DDIO_HSIO} ≤ 3.6 V
SID656G	VOL3	Output LOW voltage level	–	–	0.4	V	I _{OL} = 1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, 3.0 V ≤ V _{DDIO_HSIO} ≤ 3.6 V

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27 电气规范

表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID656H	VoL4	Output LOW voltage level	–	–	0.4	V	$I_{OL} = 0.5 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b100, $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID658D	VoH0	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.2$	–	–	V	$I_{OH} = -0.1 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b000
SID661F	VoH1	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -10 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b001, $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID662F	VoH2	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -2 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b010, $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID663E	VoH3	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -1 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b011, $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID663F	VoH4	Output HIGH voltage level	$V_{DDIO_HSIO} - 0.4$	–	–	V	$I_{OH} = -0.5 \text{ mA}$, CFG_DRIVE_EXT<1:0>/ DRIVE_SEL_EXT<2:0> = 0b100, $3.0 \text{ V} \leq V_{DDIO_HSIO} \leq 3.6 \text{ V}$
SID664D	R _{PD}	Pull-down resistance	25	50	100	kΩ	
SID665F	R _{PU}	Pull-up resistance	25	50	100	kΩ	
SID667G	ViH0	Input Voltage HIGH threshold	$0.7 \times V_{DDIO_HSIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID667I	ViH1	Input Voltage HIGH threshold	2	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID671F	ViL0	Input Voltage LOW threshold	–	–	$0.3 \times V_{DDIO_HSIO}$	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID671G	ViL1	Input Voltage LOW threshold	–	–	0.8	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1

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表 32 (续) I/O 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID674D	VHYST_CMOS	Hysteresis in CMOS mode	$0.05 \times V_{DDIO_HSIO}$	–	–	V	CFG_IN_AUTOLVL/ VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0>= 0b0
SID675D	C _{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100 MHz
SID676H	I _{IL12}	Input leakage current	–1	–	1	μA	V _{DDIO_HSIO} = 3.6 V, V _{SS} < V _I < V _{DDIO_HSIO} –40°C ≤ T _A ≤ 105°C

GPIO input specifications

SID98	t _{FT}	Analog glitch filter (pulse suppression width)	–	–	50 ¹⁾	ns	One filter per port group (required for some I ² C speeds)
SID99	t _{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

1) 如果需要更长的脉冲宽度抑制, 请使用智能 I/O。

27 电气规范

27.6 模拟外设

27.6.1 SAR ADC

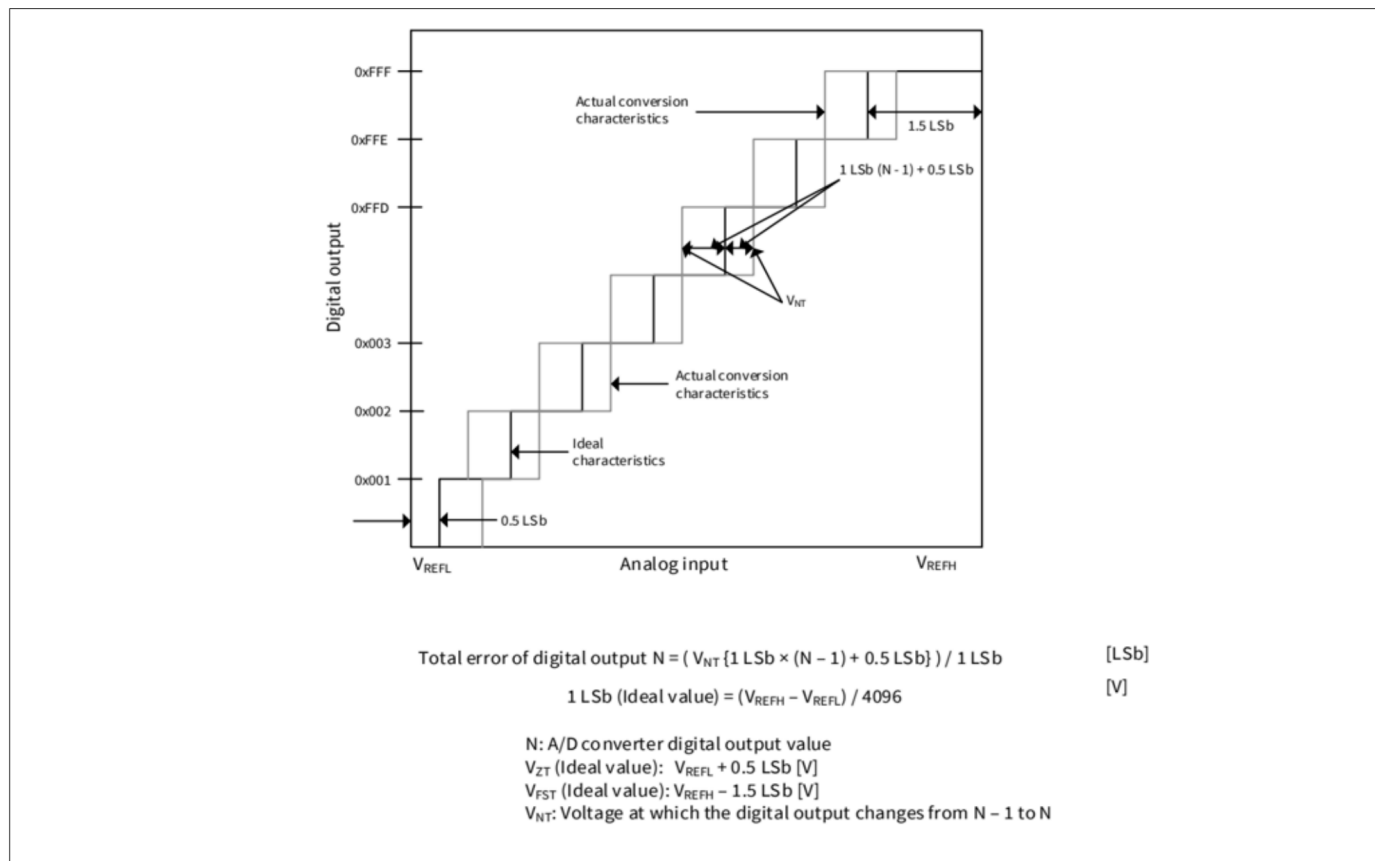


图 13 ADC 特性和误差定义

表 33 12 位 SAR ADC DC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	-	-	12	bits	
SID101	VA_INV	Input voltage range	V_{REFL}	-	V_{REFH}	V	
SID102	V_{REFH}	SAR ADC HIGH reference voltage range	2.7	-	V_{DDA_ADC}	V	ADC performance degrades when high reference is higher than supply
SID103	V_{REFL}	SAR ADC LOW reference voltage range	V_{SSA_ADC}	-	V_{SSA_ADC}	V	ADC performance degrades when low reference is lower than ground
SID103A	V_{BAND_GAP}	Internal band gap reference voltage	0.882	0.9	0.918	V	

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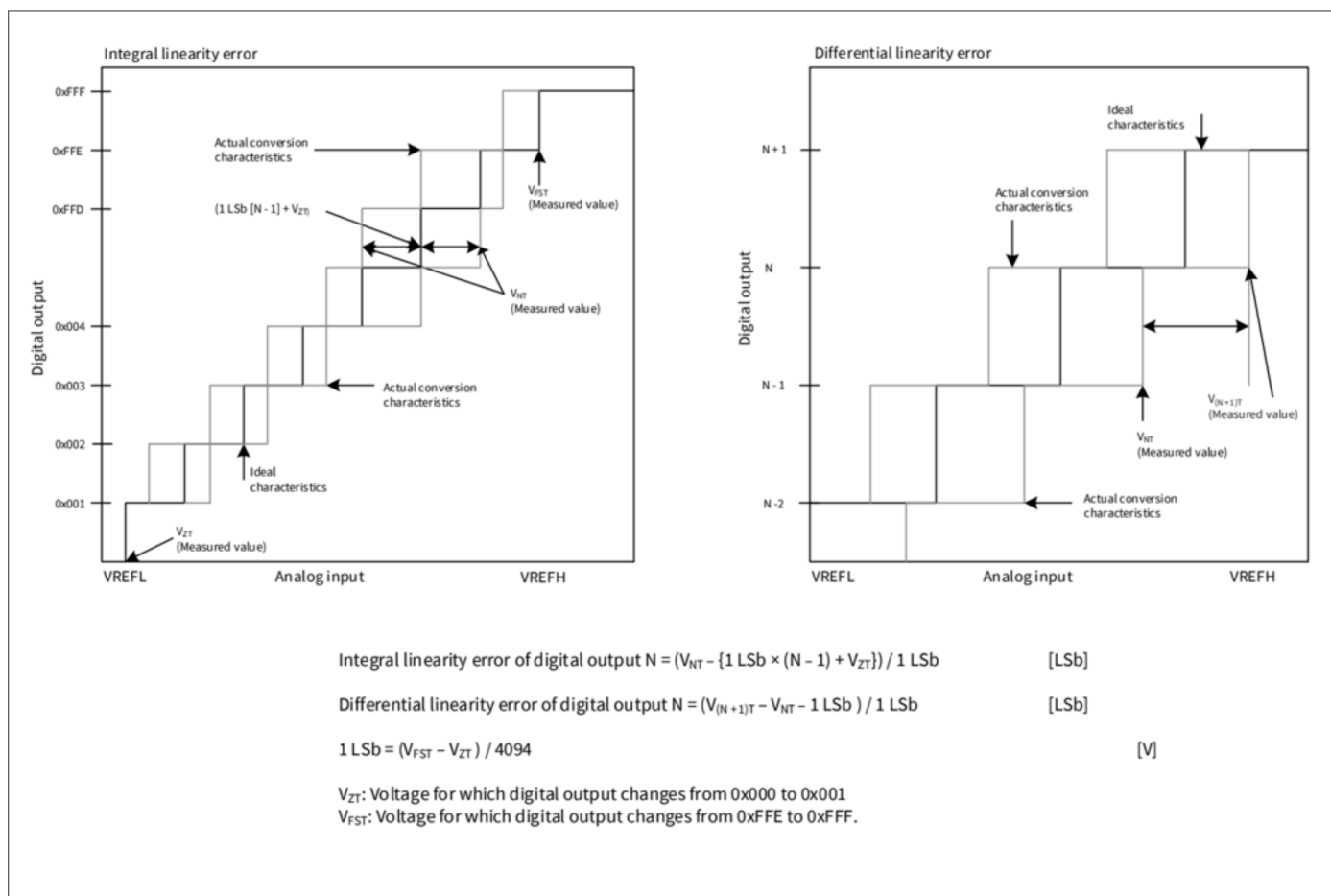


图 14 积分和微分线性误差

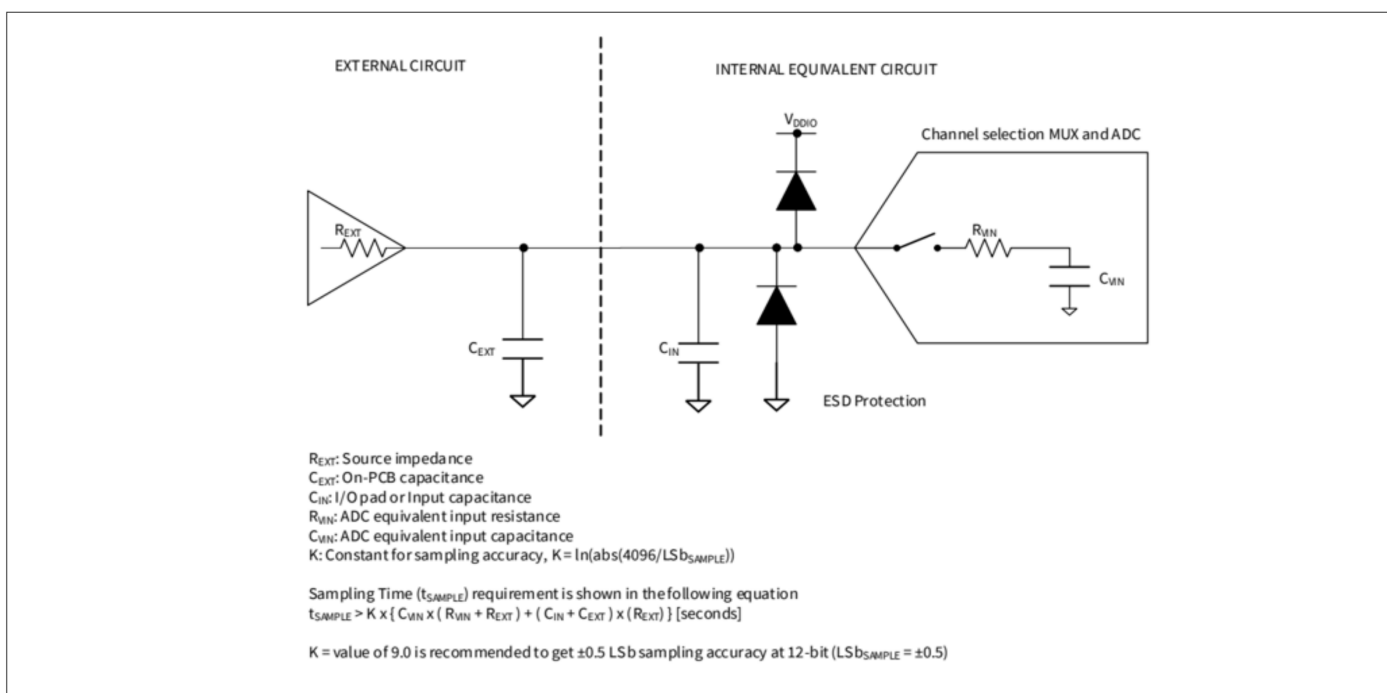


图 15 ADC 模拟输入等效电路

27 电气规范

表 34 SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V _{ZT}	Zero transition voltage	-20	-	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, -40°C ≤ T _A ≤ 105°C before offset adjustment
SID105	V _{FST}	Full-scale transition voltage	-20	-	20	mV	V _{DDA_ADC} = 2.7 V to 5.5 V, -40°C ≤ T _A ≤ 105°C before offset adjustment
SID114	f _{ADC}	ADC operating frequency	2	-	26.67	MHz	
SID113	ts _{4P5}	Analog input sample time (4.5 V ≤ V _{DDA_ADC}) for channels of SARMUX0	412	-	-	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113A	ts _{2P7}	Analog input sample time (2.7 V ≤ V _{DDA_ADC}) for channels of SARMUX0	824	-	-	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113B	ts _{DR_4P5}	Analog input sample time when input is from diagnostic reference (4.5 V ≤ V _{DDA_ADC})	2	-	-	μs	Guaranteed by design
SID113C	ts _{DR_2P7}	Analog input sample time when input is from diagnostic reference (2.7 V ≤ V _{DDA_ADC})	2.5	-	-	μs	Guaranteed by design
SID113D	ts _{TS}	Analog input sample time for temperature sensor	7	-	-	μs	Guaranteed by design
SID106	t _{ST1}	Max throughput (sample per second) for channels of SARMUX0	-	-	1	Msp/s	4.5 V ≤ V _{DDA_ADC} ≤ 5.5 V, 80 MHz/3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles
SID106A	t _{ST2}	Max throughput (sample per second) for channels of SARMUX0	-	-	0.5	Msp/s	2.7 V ≤ V _{DDA_ADC} < 4.5 V, 80 MHz/6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID107	C _{VIN}	ADC input sampling capacitance	-	-	4.8	pF	Guaranteed by design

(表格续下页.....)

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表 34 (续) SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID108	RVIN1	Input path ON resistance (4.5 V to 5.5 V)	–	–	9.4	kΩ	Guaranteed by design
SID108A	RVIN2	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	RDREF1	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	RDREF2	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	
SID109	A_TE	Total error	–5	–	5	LSb	$V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $V_{REFL} = V_{SSA_ADC}$ $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ Total Error after offset and gain adjustment at 12-bit resolution mode
SID109A	A_TEB	Total error	–12	–	12	LSb	$V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $V_{REFL} = V_{SSA_ADC}$ $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ Total Error before offset and gain adjustment at 12-bit resolution mode
SID110	A_INL	Integral nonlinearity	–2.5	–	2.5	LSb	$V_{DDA_ADC} = 2.7\text{ V to }5.5\text{ V}$, – $40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID111	A_DNL	Differential nonlinearity	–0.99	–	1.9	LSb	$V_{DDA_ADC} = 2.7\text{ V to }5.5\text{ V}$, – $40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID112	A_GE	Measure the ADC output with input switching through all input channels of one ADC	–7	–	7	LSb	$V_{DDA_ADC} = 2.7\text{ V to }5.5\text{ V}$, – $40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$

(表格续下页.....)

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表 34 (续) SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID115	IAIC	Analog input leakage current (GPIO_STD)	-350	-	350	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID115D	IAIC	Analog input leakage current (GPIO_SMC)	-1075	-	1075	nA	When input pad is selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID115A	IAIC2	Analog input leakage current (GPIO_STD)	-	-	165	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID115E	IAIC2	Analog input leakage current (GPIO_SMC)	-	-	1015	nA	When input pad is not selected for conversion, $V_{DDA_ADC} = V_{REFH} = 2.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID116	IDIAGREF	Diagnostic reference current	-	-	70	μA	
SID117	IVDDA	Analog power supply current while ADC is operating	-	360	550	μA	Per enabled ADC, without diagnosis
SID117A	IVDDA_DS	Analog power supply current while ADC is not operating	-	1	21	μA	Per enabled ADC
SID118	IVREF	Analog reference voltage current while ADC is operating	-	360	550	μA	Per enabled ADC, without diagnosis
SID118A	IVREF_LEAK	Analog reference voltage current while ADC is not operating	-	1.8	5	μA	Per enabled ADC
SID118B	ts_4P5_1	Analog input sample time ($4.5\text{ V} \leq V_{DDA_ADC}$) for channels of SARMUX1	824	-	-	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design

(表格续下页.....)

27 电气规范

表 34 (续) SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID118C	ts_2P7_1	Analog input sample time ($2.7\text{ V} \leq V_{\text{DDA_ADC}}$) for channels of SARMUX1	1648	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID119A	tST3	Max throughput (sample per second) for channels of SARMUX1	–	–	0.5	Msp/s	$4.5\text{ V} \leq V_{\text{DDA_ADC}} \leq 5.5\text{ V}$, 80 MHz/6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID119B	tST4	Max throughput (sample per second) for channels of SARMUX1	–	–	0.25	Msp/s	$2.7\text{ V} \leq V_{\text{DDA_ADC}} < 4.5\text{ V}$, 80 MHz/12 = 6.67 MHz, 11 sampling cycles, 15 conversion cycles

27.6.2 温度传感器

表 35 温度传感器规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID201	TSSENSACC_TR	Temperature sensor accuracy trimmed	-5	-	5	°C	This spec is valid for the following two conditions: 1. $3.0\text{ V} \leq V_{\text{DDA_ADC}} = V_{\text{REFH}} \leq 3.6\text{ V}$ and $3.0\text{ V} \leq V_{\text{DDD}} \leq 3.6\text{ V}$. 2. $3.6\text{ V} < V_{\text{DDA_ADC}} = V_{\text{REFH}} \leq 5.5\text{ V}$ and $4.5\text{ V} \leq V_{\text{DDD}} \leq 5.5\text{ V}$ (Calibrated accuracy by factory trimming)
SID202	TSSENSAC- CSTD	Temperature sensor accuracy standard	-10	-	10	°C	This spec applies to all valid combinations for $V_{\text{DDA_ADC}} = V_{\text{REFH}}$ and V_{DDD} , which are not covered by SID201 (Uncalibrated accuracy)

27.7 AC 规格

除非另有说明，时序均按照图 16 中提到的指导原则定义。

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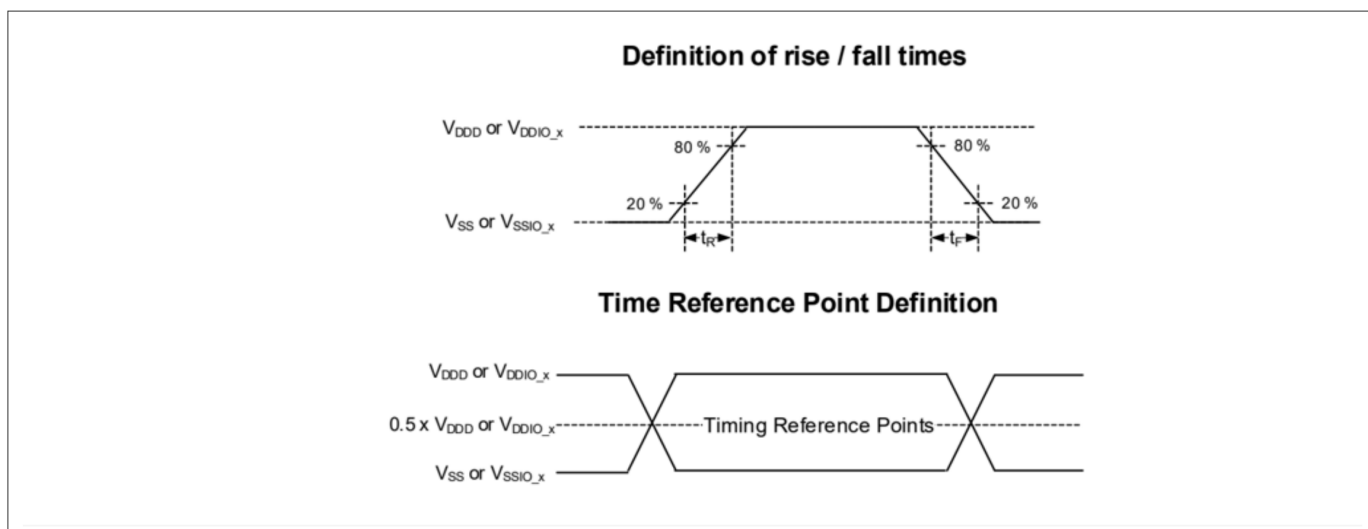


图 16 AC 时序规范

27.8 数字外设

表 36 定时器/计数器/PWM (TCPWM) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID120	f_c	TCPWM operating frequency	-	-	100	MHz	f_c = peripheral clock
SID121	t_{PWMENT}	Input trigger pulse width for all trigger events	$2/f_c$	-	-	ns	trigger events can be stop, start, reload, count, capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMENT}	Output trigger pulse widths	$2/f_c$	-	-	ns	Minimum possible width of overflow, underflow, and CC (Counter equals compare value) trigger outputs
SID123	t_{CRES}	Resolution of counter	$1/f_c$	-	-	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	$1/f_c$	-	-	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	$2/f_c$	-	-	ns	Minimum pulse width between quadrature phase inputs.

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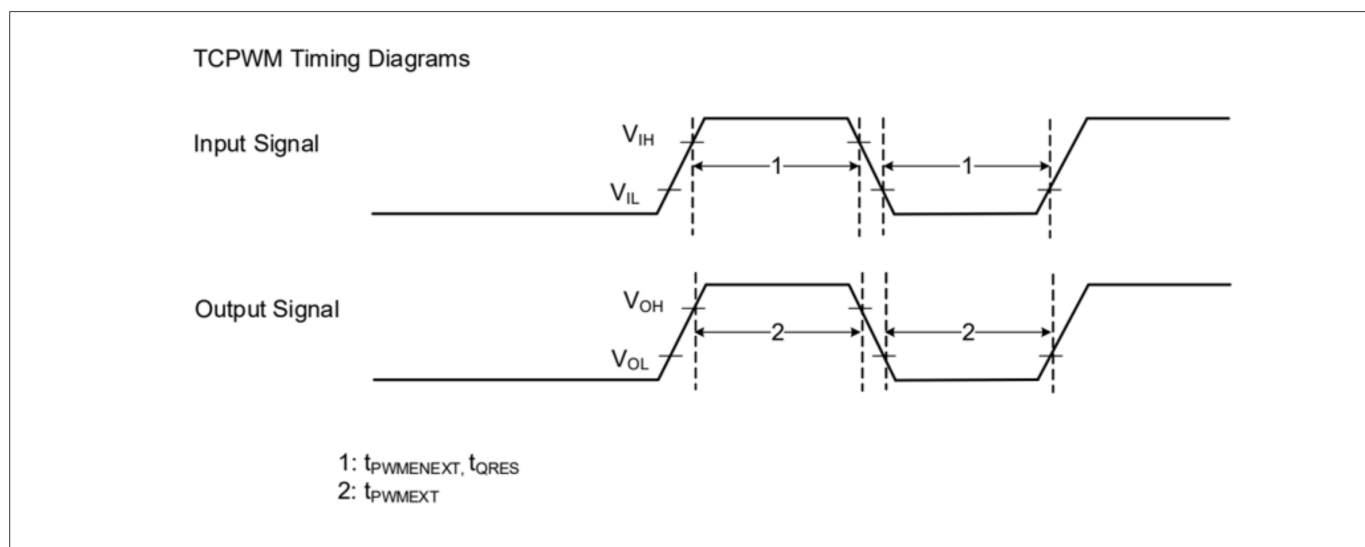


图 17 TCPWM 时序图

表 37 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID129	f _{SCB}	SCB operating frequency	–	–	100	MHz	
SID129_2	t _{SPI_TRANS}	SCB input transition in SPI mode	–	–	4	ns	
SID129_3	t _{SPI_TRANS}	SCB output transition in SPI mode	–	–	10	ns	Valid for HSIO_STDLN
SID129_4	t _{SPI_TRANS}	SCB output transition in SPI mode	–	–	20	ns	Valid for GPIO_STD, GPIO_ENH, GPIO_SMC

I2C 接口-标准-模式

推荐 I/O 配置: GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, , CFG_SLEW_EXT/SLEW<2:0> = 0b000 (注: SID138 对于 HSIO_STDLN 无效)

SID130	f _{SCL}	SCL clock frequency	–	–	100	kHz	
SID131	t _{HD;STA}	Hold time, START condition	4000	–	–	ns	

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID132	t _{LOW}	Low period of SCL	4700	–	–	ns	
SID133	t _{HIGH}	High period of SCL	4000	–	–	ns	
SID134	t _{SU;STA}	Setup time for a repeated START	4700	–	–	ns	
SID135	t _{HD;DAT}	Data hold time, for receiver	0	–	–	ns	
SID136	t _{SU;DAT}	Data setup time	250	–	–	ns	
SID138	t _F	Fall time of SCL and SDA	–	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC, GPIO_STD
SID139	t _{SU;STO}	Setup time for STOP	4000	–	–	ns	
SID140	t _{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C _B	Capacitive load for each bus line	–	–	400	pF	
SID142	t _{VD;DAT}	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	t _{VD;ACK}	Data valid acknowledge time	–	–	3450	ns	

I²C 接口-快速模式

推荐 I/O 配置: GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

注: SID158 对于 GPIO_STD 无效

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_SLEW_EXT/SLEW<2:0> = 0b000

注: SID158 对于 HSIO_STDLN 无效

SID150	f _{SCL_F}	SCL clock frequency	–	–	400 ¹⁾	kHz	
SID151	t _{HD;STA_F}	Hold time, START condition	600	–	–	ns	

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID152	t _{LOW_F}	Low period of SCL	1300	–	–	ns	
SID153	t _{HIGH_F}	High period of SCL	600	–	–	ns	
SID154	t _{SU;STA}	Setup time for a repeated START	600	–	–	ns	
SID155	t _{HD;DAT}	Data hold time, for receiver	0	–	–	ns	
SID156	t _{SU;DAT}	Data setup time	100	–	–	ns	
SID158	t _F	Fall time of SCL and SDA	20 × (V _{DDIO_GPIO} / 5.5)	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC
SID159	t _{SU;STO}	Setup time for STOP	600	–	–	ns	
SID160	t _{BUF}	Bus free time between START and STOP	1300	–	–	ns	
SID161	C _B	Capacitive load for each bus line	–	–	400	pF	
SID162	t _{VD;DAT}	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	t _{VD;ACK}	Data valid acknowledge time	–	–	900	ns	
SID164	t _{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	

I2C Interface Fast-Plus mode

(表格续下页...)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
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推荐 I/O 配置: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100

注: SID178 对于 GPIO_STD 无效

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0

注: SID178 对于 GPIO_SMC 无效

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 CFG_SLEW_EXT/SLEW<2:0> = 0b000

注: SID178 对于 HSIO_STDLN 无效

SID170	f _{SCL_FP}	SCL clock frequency	–	–	1 ^[55]	MHz	
SID171	t _{HD;STA_FP}	Hold time, START condition	260	–	–	ns	
SID172	t _{LOW_FP}	Low period of SCL	500	–	–	ns	
SID173	t _{HIGH_FP}	High period of SCL	260	–	–	ns	
SID174	t _{SU;STA}	Setup time for a repeated START	260	–	–	ns	
SID175	t _{HD;DAT}	Data hold time, for receiver	0	–	–	ns	
SID176	t _{SU;DAT}	Data setup time	50	–	–	ns	
SID178	t _F	Fall time of SCL and SDA	20 × (V _{DDIO_GPIO} / 5.5)	–	160	ns	Input and output, 20pF load Output: Only for GPIO_ENH
SID179	t _{SU;STO}	Setup time for STOP	260	–	–	ns	
SID180	t _{BUF}	Bus free time between START and STOP	500	–	–	ns	
SID181	C _B	Capacitive load for each bus line	–	–	20	pF	
SID182	t _{VD;DAT}	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	t _{VD;ACK}	Data valid acknowledge time	–	–	450	ns	

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID184	t _{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	

SPI Interface

建议 I/O 配置：（适用于以下所有 SPI 模式）

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> = 0b000

注：SID178 对于 HSIO_STDLN 无效

对于 SPI 速度 ≤ 12.5 MHz

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, GPIO)

SID190	f _{SPI}	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID191	t _{DMO}	SPI master: MOSI valid after SCLK driving edge	–	–	15	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID192	t _{DSI}	SPI master: MISO valid before SCLK capturing edge	40	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID193	t _{HMO}	SPI master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID194	tw_SCLK_H_L	SPI SCLK pulse width HIGH or LOW	$0.4 \times (1/f_{SPI})$	$0.5 \times (1/f_{SPI})$	$0.6 \times (1/f_{SPI})$	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID195	tvss	SPI master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID196	tdHI	SPI master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID198	tEN_SETUP	SSEL valid, before the first SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID199	tEN_HOLD	SSEL hold, after the last SCK capturing edge	$0.5 \times (1/f_{SPI})$	–	–	ns	Min is half clock period
SID197	CSPIIM_MS	SPI capacitive load	–	–	20	pF	

SPI interface master (Full-clock mode: LATE_MISO_SAMPLE = 1, HSIO)

SID190A	f _{SPI}	SPI operating frequency	–	–	20	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz. for instances on HSIO_STDLN
SID191A	tDMO	SPI master: MOSI valid after SCLK driving edge	–	–	9	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID192A	t _{DSI}	SPI master: MISO valid before SCLK capturing edge	25	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID193A	t _{HMO}	SPI master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID194A	t _{W_SCLK_H_L}	SPI SCLK pulse width HIGH or LOW	0.4 × (1/f _{SPI})	0.5 × (1/f _{SPI})	0.6 × (1/f _{SPI})	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID195A	t _{VSS}	SPI master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID196A	t _{DHI}	SPI master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f _{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID197A	C _{SPIM_MS}	SPI capacitive load	–	–	20	pF	
SID198A	t _{EN_SETUP}	SSEL valid, before the first SCK capturing edge	0.5 × (1/f _{SPI})	–	–	ns	Min is half clock period
SID199A	t _{EN_HOLD}	SSEL hold, after the last SCK capturing edge	0.5 × (1/f _{SPI})	–	–	ns	Min is half clock period

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SPI interface slave (internally clocked, GPIO and HSIO)							
SID205	f _{SPI_INT}	SPI operating frequency	–	–	12.5	MHz	SPI slave, internally clocked
SID206	t _{DMI_INT}	SPI slave: MOSI valid before S _{clock} capturing edge	5	–	–	ns	SPI slave, internally clocked
SID207	t _{DSO_INT}	SPI slave: MISO valid after S _{clock} driving edge, in the internal-clocked mode	–	–	60	ns	SPI slave, internally clocked
SID208	t _{HSO_INT}	SPI slave: previous MISO data hold time	3	–	–	ns	SPI slave, internally clocked
SID209	t _{EN_SETUP_INT}	SPI slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI slave, internally clocked
SID210	t _{EN_HOLD_INT}	SPI slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI slave, internally clocked
SID211	t _{EN_SETUP_PRE}	SPI slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI slave, internally clocked
SID212	t _{EN_HOLD_PRE}	SPI slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI slave, internally clocked
SID213	t _{EN_SETUP_CO}	SPI slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI slave, internally clocked
SID214	t _{EN_HOLD_CO}	SPI slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI slave, internally clocked
SID215	t _{W_DIS_INT}	SPI slave select inactive time	40	–	–	ns	SPI slave, internally clocked
SID216	t _{W_SCLKH_INT}	SPI SCLK pulse width HIGH	32	–	–	ns	SPI slave, internally clocked
SID217	t _{W_SCLKL_INT}	SPI SCLK pulse width LOW	32	–	–	ns	SPI slave, internally clocked

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID218	tSIH_INT	SPI MOSI hold from SCLK	20	–	–	ns	SPI slave, internally clocked
SID219	CSPI_INT	SPI capacitive load	–	–	20	pF	SPI slave, internally clocked
SPI interface slave (externally clocked, GPIO and HSIO)							
SID220	fSPI_EXT	SPI operating frequency	–	–	12.5	MHz	SPI slave, externally clocked: 12.5 Mbps
SID221	tDMI_EXT	SPI slave: MOSI Valid before Scklock capturing edge	8	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID222	tDSO_EXT	SPI slave: MISO Valid after Scklock driving edge, in the external-clocked mode	–	–	30	ns	SPI slave, externally clocked: 12.5 Mbps
SID223	tHSO_EXT	SPI slave: Previous MISO data hold time	5	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID224	tEN_SETUP_EXT	SPI slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID225	tEN_HOLD_EXT	SPI slave select active (LOW) from last SCLK hold	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID226	tW_DIS_EXT	SPI slave select inactive time	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID227	tW_SCLKH_EXT	SPI SCLK pulse width HIGH	32	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID228	tW_SCLKL_EXT	SPI SCLK pulse width LOW	32	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID229	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID230	CSPI_EXT	SPI capacitive Load	–	–	20	pF	SPI slave, externally clocked: 12.5 Mbps
SID231	tVSS_EXT	SPI slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	SPI slave, externally clocked: 12.5 Mbps
SPI interface slave (internally clocked, SMC I/O)							
SID205_2	fSPI_INT	SPI operating frequency	–	–	12.5	MHz	SPI slave, internally clocked

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID206_2	tDMI_INT	SPI slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI slave, internally clocked
SID207_2	tDSO_INT	SPI slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	64	ns	SPI slave, internally clocked
SID208_2	tHSO_INT	SPI slave: Previous MISO data hold time	3	–	–	ns	SPI slave, internally clocked
SID209_2	tEN_SETUP_IN T	SPI slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI slave, internally clocked
SID210_2	tEN_HOLD_IN T	SPI slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI slave, internally clocked
SID211_2	tEN_SETUP_P RE	SPI slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI slave, internally clocked
SID212_2	tEN_HOLD_PR E	SPI slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI slave, internally clocked
SID213_2	tEN_SETUP_C O	SPI slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI slave, internally clocked
SID214_2	tEN_HOLD_CO	SPI slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI slave, internally clocked
SID215_2	tW_DIS_INT	SPI slave Select inactive time	40	–	–	ns	SPI slave, internally clocked
SID216_2	tW_SCLKH_IN T	SPI SCLK pulse width HIGH	36	–	–	ns	SPI slave, internally clocked
SID217_2	tW_SCLKL_INT	SPI SCLK pulse width LOW	36	–	–	ns	SPI slave, internally clocked
SID218_2	tSIH_INT	SPI MOSI hold from SCLK	20	–	–	ns	SPI slave, internally clocked
SID219_2	CSPI5_INT	SPI Capacitive Load	–	–	20	pF	SPI slave, internally clocked

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SPI interface slave (externally clocked, SMC I/O)							
SID220_2	fSPI_EXT	SPI operating frequency	–	–	12.5	MHz	SPI slave, externally clocked: 12.5 Mbps
SID221_2	tDMI_EXT	SPI slave: MOSI Valid before Sclock capturing edge	8	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID222_2	tDSO_EXT	SPI slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	34	ns	SPI slave, externally clocked: 12.5 Mbps
SID223_2	tHSO_EXT	SPI slave: Previous MISO data hold time	5	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID224_2	tEN_SETUP_EXT	SPI slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID225_2	tEN_HOLD_EXT	SPI slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID226_2	tW_DIS_EXT	SPI slave Select inactive time	20	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID227_2	tW_SCLKH_EXT	SPI SCLK pulse width HIGH	36	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID228_2	tW_SCLKL_EXT	SPI SCLK pulse width LOW	36	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID229_2	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI slave, externally clocked: 12.5 Mbps
SID230_2	CSPIIS_EXT	SPI Capacitive Load	–	–	20	pF	SPI slave, externally clocked: 12.5 Mbps
SID231_2	tVSS_EXT	SPI slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	37	ns	SPI slave, externally clocked: 12.5 Mbps
SPI interface slave (externally clocked, 20 MHz)							
SID220A	fSPI_EXT	SPI operating frequency	–	–	20	MHz	SPI slave, externally clocked: 20 Mbps
SID221A	tDMI_EXT	SPI slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI slave, externally clocked: 20 Mbps

(表格续下页.....)

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表 37 (续) 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID222A	tDSO_EXT	SPI slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	18	ns	SPI slave, externally clocked: 20 Mbps
SID223A	tHSO_EXT	SPI slave: Previous MISO data hold time	5	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID224A	tEN_SETUP_EXT	SPI slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID225A	tEN_HOLD_EXT	SPI slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID226A	tw_DIS_EXT	SPI slave Select inactive time	20	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID227A	tw_SCLKH_EXT	SPI SCLK pulse width HIGH	20	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID228A	tw_SCLKL_EXT	SPI SCLK pulse width LOW	20	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID229A	tSIH_EXT	SPI MOSI hold from SCLK	5	–	–	ns	SPI slave, externally clocked: 20 Mbps
SID230A	CSPI_EXT	SPI Capacitive Load	–	–	20	pF	SPI slave, externally clocked: 20 Mbps
SID231A	tVSS_EXT	SPI slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	23	ns	SPI slave, externally clocked: 20 Mbps

UART interface

建议 I/O 配置

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> = 0b000

SID240	fBPS	Signaling rate	–	–	10	Mbps	
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1) 为了以 400 kHz 的频率驱动满总线负载, 在 0.6 V_{VOL} 时需要 6 mA I_{OL0}

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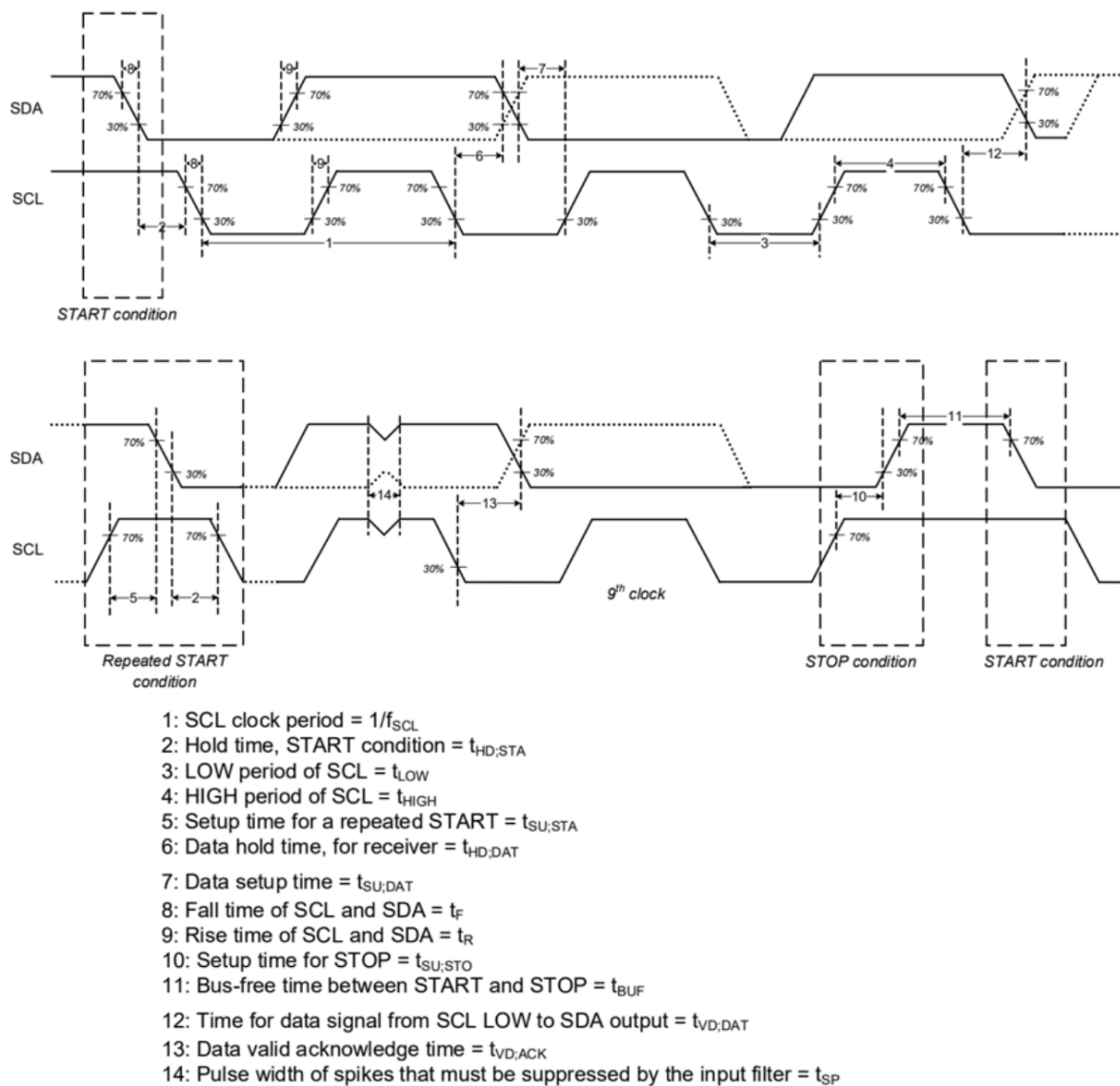


图 18 I2C 时序图

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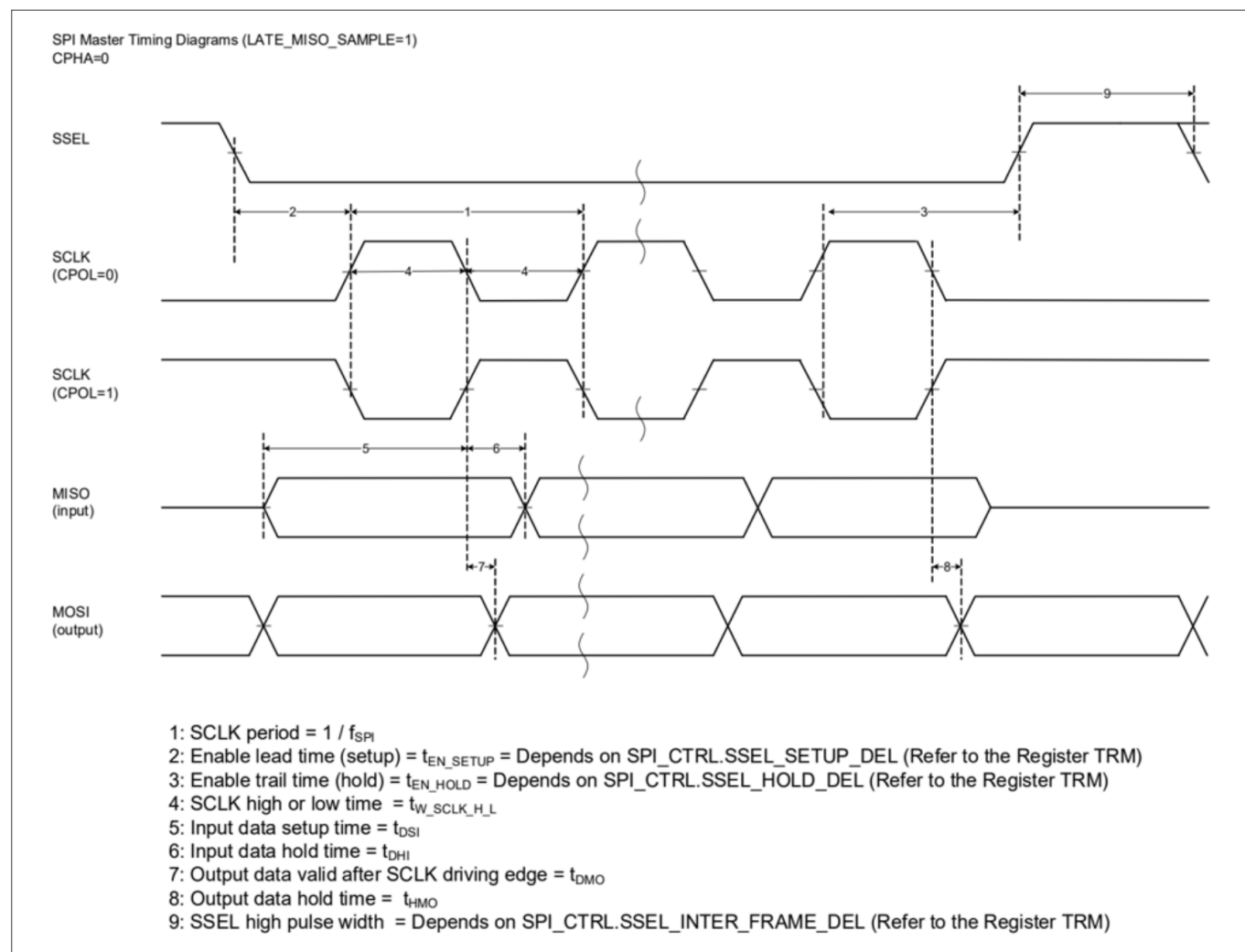


图 19 SPI 主机时序图（低时钟相位）

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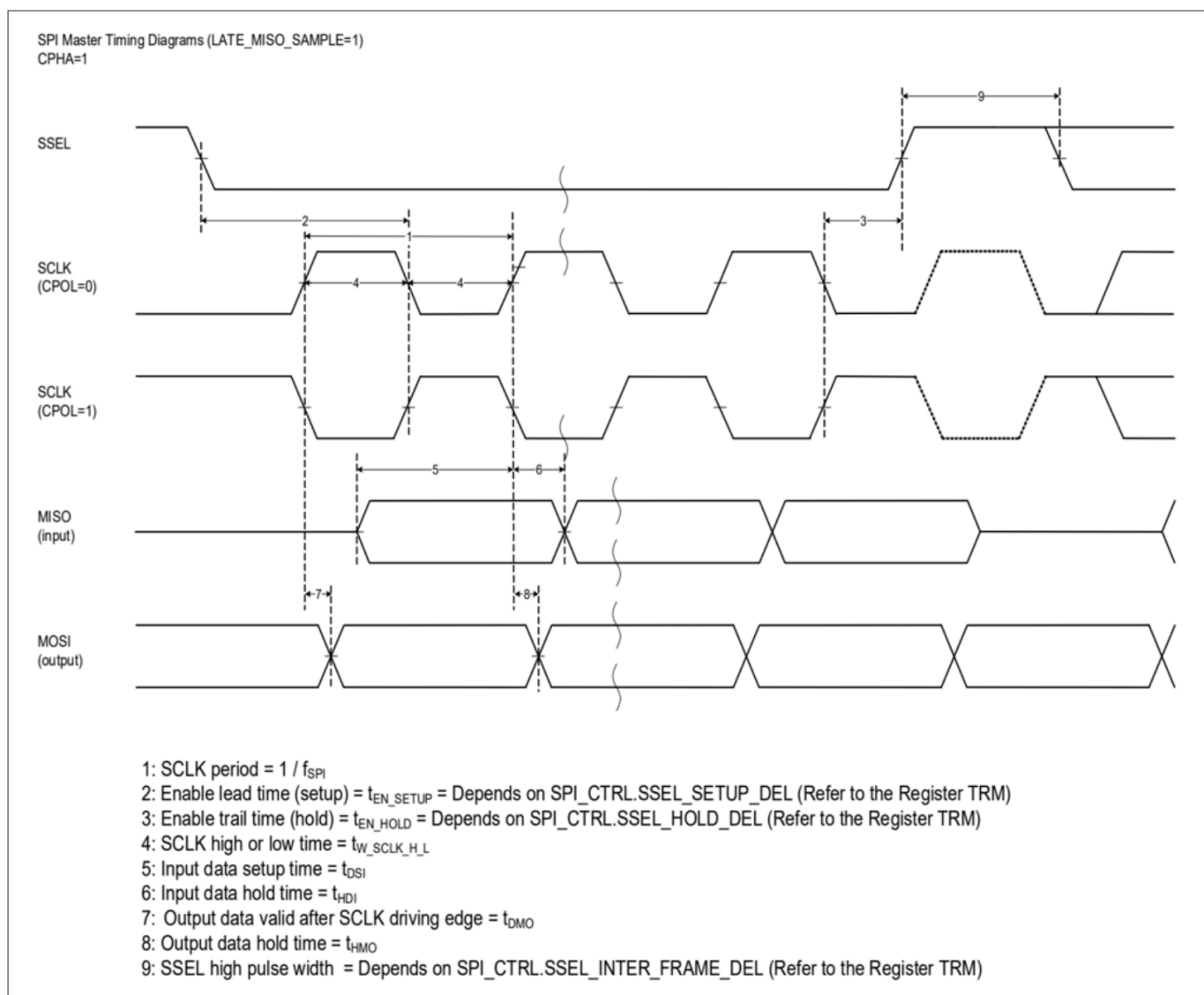


图 20 SPI 主机时序图（高时钟相位）

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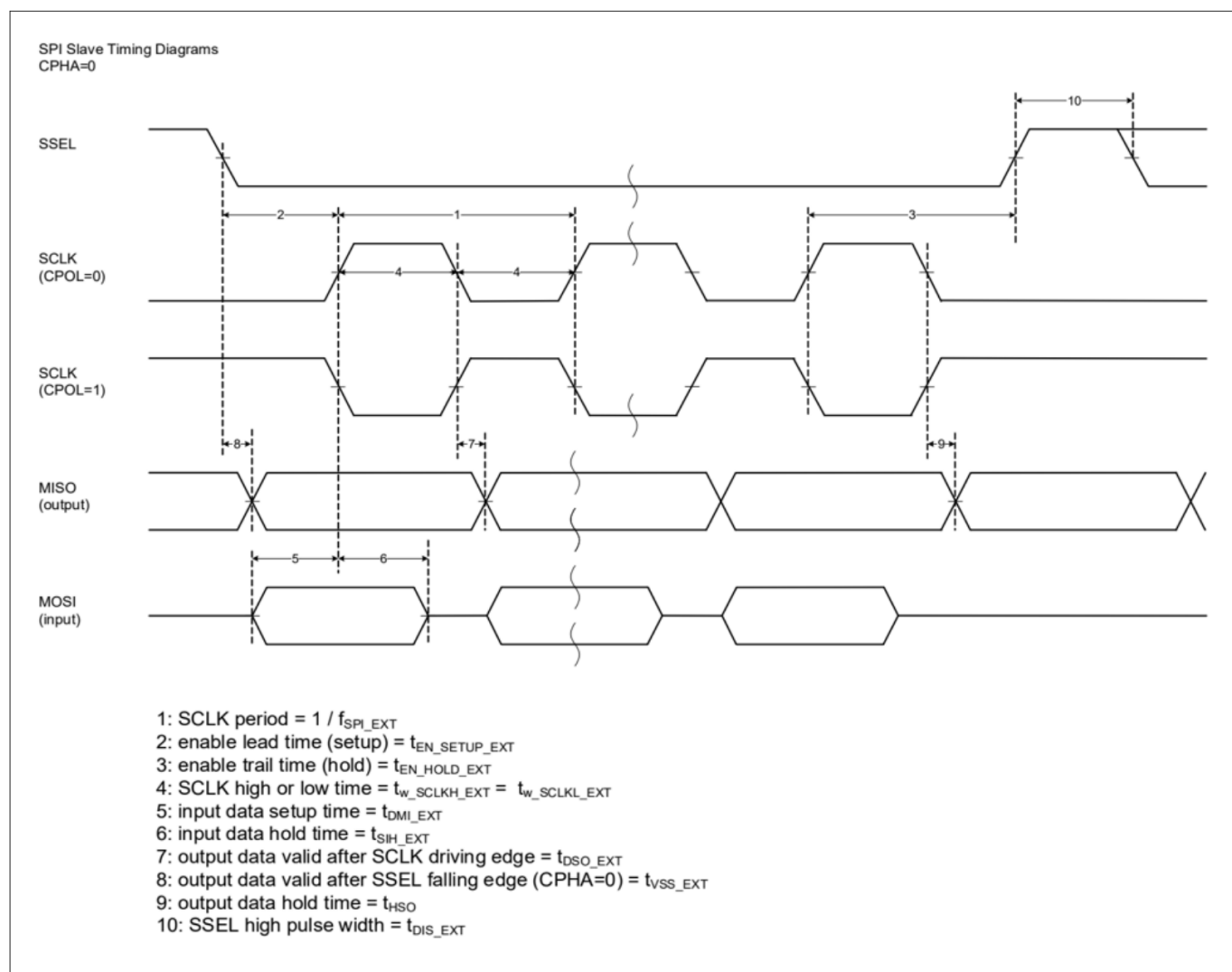


图 21 SPI 从机时序图（低时钟相位）

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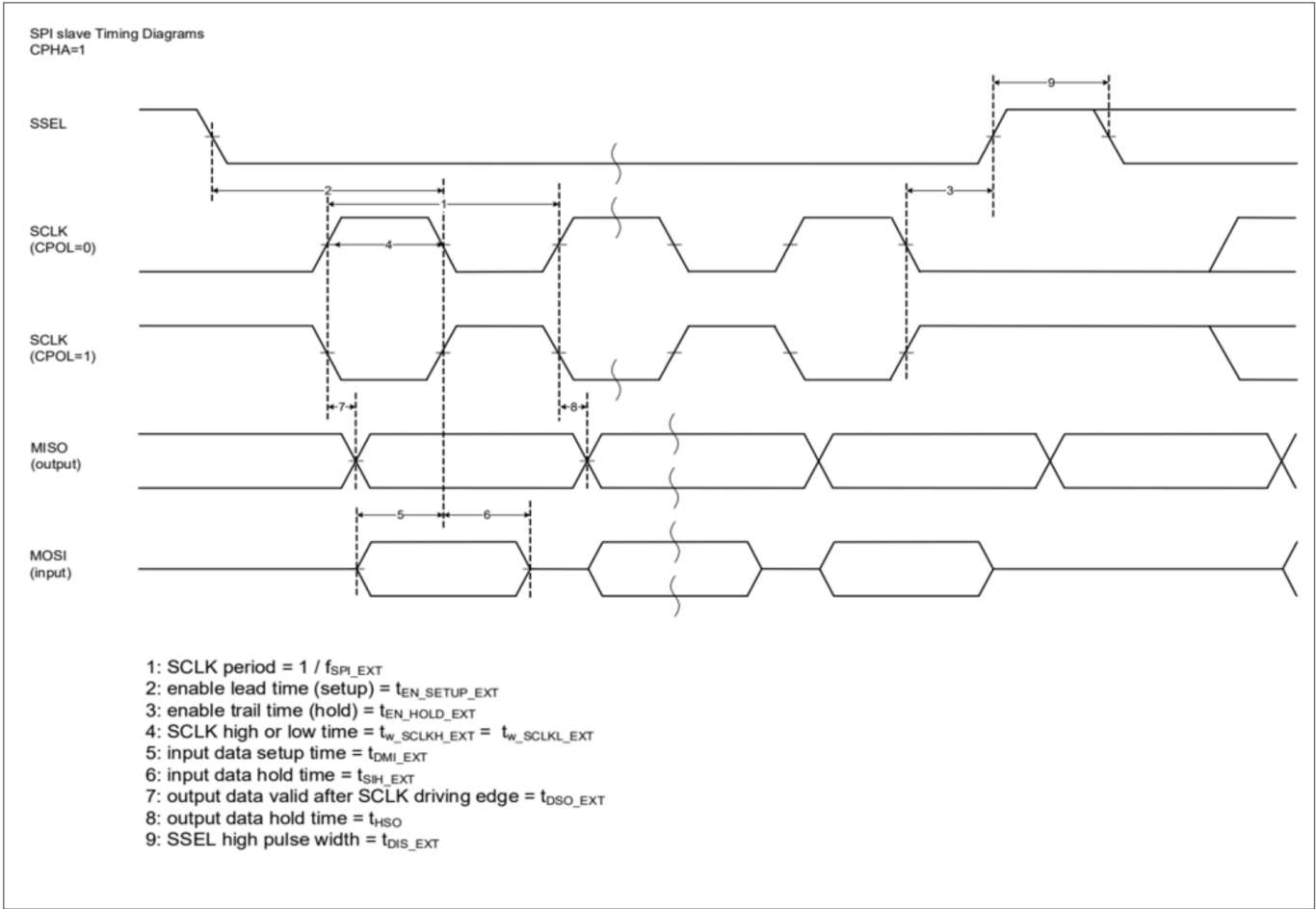


图 22 SPI 从机时序图（高时钟相位）

27.8.1 LIN 规格

表 38 LIN 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID249	f _{LIN}	Internal clock frequency to the LIN block	-	-	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	-	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	-	115.2	kbps	Guaranteed by design

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27.8.2 CAN FD 规格

表 39 CAN FD 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID630	f _{HCLK}	System clock (HCLK) frequency	-	-	100	MHz	f _{CCLK} ≤ f _{HCLK} , guaranteed by design
SID631	f _{CCLK}	CAN clock (CCLK) frequency	-	-	100	MHz	f _{CCLK} ≤ f _{HCLK} , guaranteed by design

27.9 存储器

表 40 Flash DC规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID257A	V _{PE}	Erase and program voltage	2.7	-	5.5	V	

表 41 Flash AC 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID257	f _{FO}	Maximum operation frequency	-	-	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 320 MHz
SID254	t _{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	-	-	37.5	μs	
SID255	t _{ERS_RES_SUS}	Minimum time allowed from erase resume to erase suspend	250	-	-	μs	Guaranteed by design
SID258	t _{BC_WF}	Blank Check time for Work Flash N-byte	-	-	10+0.3×N	μs	At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time
SID258A	t _{AA_BC_ENTRY}	Time to enter Blank Check mode	-	5	-	μs	
SID258B	t _{AA_BC_EXIT}	Time to exit Blank Check mode	-	5	-	μs	
SID259	t _{SECTOR- RASE1}	Sector erase time (code-flash: 32 KB)	-	45	90	ms	Includes internal preprogramming time
SID260	t _{SECTOR- RASE2}	Sector erase time (code-flash: 8 KB)	-	15	30	ms	Includes internal preprogramming time
SID261	t _{SECTOR- RASE3}	Sector erase time (work-flash, 2 KB)	-	80	160	ms	Includes internal preprogramming time

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表 41 (续) Flash AC 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID262	tSECTOR- RASE4	Sector erase time (work-flash, 128 B)	-	5	15	ms	Includes internal preprogramming time
SID263	tWRITE1	64-bit write time (code-flash)	-	30	60	μs	Excludes system overhead time
SID264	tWRITE2	256-bit write time (code-flash)	-	40	70	μs	Excludes system overhead time
SID265	tWRITE3	4096-bit write time (code-flash)	-	320	1200	μs	Excludes system overhead time
SID266	tWRITE4	32-bit write time (work-flash)	-	30	60	μs	Excludes system overhead time
SID267	tFRET1	Code-flash retention. 1000 program/erase cycles	20	-	-	years	Temperature at write/erase time. T _A ≤ +85°C average
SID182T1	tFRET2	Code-flash retention. 100 program/erase cycles	50	-	-	years	Temperature at write/erase time. T _A ≤ +30°C average
SID268	tFRET3	Work-flash retention. 125,000 program/erase cycles	20	-	-	years	Temperature at write/erase time. T _A ≤ +85°C average
SID269	tFRET4	Work-flash retention. 250,000 program/erase cycles	10	-	-	years	Temperature at write/erase time. T _A ≤ +85°C average
SID182T2	tFRET5	Work-flash retention. 1000 program/erase cycles	50	-	-	years	Temperature at write/erase time. T _A ≤ +30°C average
SID612	ICC_ACT2	Program operating current (code or work-flash)	-	15	62	mA	V _{DD} = 5 V, V _{CCD} = 1.1 V Guaranteed by design
SID613	ICC_ACT3	Erase operating current (code- or work-flash)	-	15	62	mA	V _{DD} = 5 V, V _{CCD} = 1.1 V Guaranteed by design

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27.10 系统资源

表 42 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
Power-on-reset specifications							
SID270	V _{POR_R}	POR rising trip voltage	1.5	–	2.35	V	Guaranteed by design
SID276	V _{POR_F}	POR falling trip voltage	1.45	–	2.1	V	
SID271	V _{POR_H}	Level detection hysteresis	20	–	300	mV	
SID272	t _{DLY_POR}	Delay between V _{DD} rising through 2.3 V and POR reset output rising through V _{DD} /2	–	–	3	μs	Guaranteed by design
SID273	t _{POFF}	Power off time	350	–	–	μs	V _{DD} < 1.45 V Does not apply to SID274A and SID274B
SID274A	POR_RR1	V _{DD} power ramp rate with robust BOD - XRES_L asserted (BOD operation is guaranteed)	–	–	100	mV/μs	Applies to ramp up and ramp down
SID274B	POR_RR1	V _{DD} power ramp rate with robust BOD - XRES_L de-asserted (BOD operation is guaranteed)	1	–	100	mV/μs	Applies to ramp up and ramp down
SID275	POR_RR2	V _{DD} power ramp rate without robust BOD	100	–	1000	mV/μs	This ramp does not support robust BOD t _{POFF} must be satisfied. Applies to ramp up and ramp down
High-voltage BOD (HV BOD) specifications							
SID500	V _{TR_2P7_R}	HV BOD 2.7 V trimmed rising trip point for V _{DD} and V _{DDA_ADC} (default)	2.474	2.55	2.627	V	
SID501	V _{TR_2P7_F}	HV BOD 2.7 V trimmed falling trip point for V _{DD} and V _{DDA_ADC} (default)	2.449	2.525	2.601	V	
SID502	V _{TR_3P0_R}	HV BOD 3.0 V trimmed rising trip point for V _{DD} and V _{DDA_ADC}	2.765	2.85	2.936	V	

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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID503	VTR_3P0_F	HV BOD 3.0 V trimmed falling trip point for V _{DD} and V _{DDA_ADC}	2.74	2.825	2.91	V	
SID505	HVBOD_R_R_A	Power ramp rate: V _{DD} and V _{DDA_ADC} (Active)	–	–	100	mV/μs	
SID506	HVBOD_R_R_DS	Power ramp rate: V _{DD} and V _{DDA_ADC} (DeepSleep)	–	–	10	mV/μs	
SID507	tdLY_ACT_HV_BOD	Active mode delay between V _{DD} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD output transitioning through V _{DD} / 2	–	–	0.5	μs	Guaranteed by design
SID507A	tdLY_ACT_HV_BOD_A	Active mode delay between V _{DDA_ADC} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and internal HV BOD output transitioning through V _{DD} / 2	–	–	1	μs	Guaranteed by design
SID507B	tdLY_DS_HVBOD	DeepSleep mode delay between V _{DD} /V _{DDA_ADC} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD output transitioning through V _{DD} / 2	–	–	4	μs	Guaranteed by design
SID508	tRES_HVBOD	Response time of HV BOD, V _{DD} /V _{DDA_ADC} supply. HV BOD guaranteed to generate pulse for V _{DD} /V _{DDA_ADC} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below V _{TR_2P7_F} or V _{TR_3P0_F})	100	–	–	ns	Guaranteed by design

Low-voltage BOD (LV BOD) specifications

SID510	VTR_R_LVBOD	LV BOD trimmed rising trip point for V _{CCD}	0.917	0.945	0.973	V	
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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID511	VTR_F_LVBOD	LV BOD trimmed falling trip point for V _{CCD}	0.892	0.92	0.948	V	
SID515	tdLY_ACT_LVBOD	Active delay between V _{CCD} falling/rising through VTR_R/F_LVBOD and an internal LV BOD output transitioning through V _{DDD} / 2	–	–	1	μs	Guaranteed by design
SID515A	tdLY_DS_LVBOD	DeepSleep mode delay between V _{CCD} falling/rising through VTR_R/F_LVBOD and an internal LV BOD output transitioning through V _{DDD} / 2	–	–	12	μs	Guaranteed by design
SID516	tRES_LVBOD	Response time of LV BOD. LV BOD guaranteed to generate pulse for V _{CCD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below VTR_F_LVBOD)	100	–	–	ns	Guaranteed by design

Low-voltage detector (LVD) DC specifications

SID520	VTR_2P8_F	LVD 2.8 V trimmed falling trip point for V _{DDD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	VTR_2P9_F	LVD 2.9 V trimmed falling trip point for V _{DDD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	VTR_3P0_F	LVD 3.0 V trimmed falling trip point for V _{DDD}	Typ – 4%	3000	Typ + 4%	mV	
SID523	VTR_3P1_F	LVD 3.1 V trimmed falling trip point for V _{DDD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	VTR_3P2_F	LVD 3.2 V trimmed falling trip point for V _{DDD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	VTR_3P3_F	LVD 3.3 V trimmed falling trip point for V _{DDD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	VTR_3P4_F	LVD 3.4 V trimmed falling trip point for V _{DDD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	VTR_3P5_F	LVD 3.5 V trimmed falling trip point for V _{DDD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	VTR_3P6_F	LVD 3.6 V trimmed falling trip point for V _{DDD}	Typ – 4%	3600	Typ + 4%	mV	

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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID529	VTR_3P7_F	LVD 3.7 V trimmed falling trip point for V _{DDD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	VTR_3P8_F	LVD 3.8 V trimmed falling trip point for V _{DDD}	Typ – 4%	3800	Typ + 4%	mV	
SID531	VTR_3P9_F	LVD 3.9 V trimmed falling trip point for V _{DDD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	VTR_4P0_F	LVD 4.0 V trimmed falling trip point for V _{DDD}	Typ – 4%	4000	Typ + 4%	mV	
SID533	VTR_4P1_F	LVD 4.1 V trimmed falling trip point for V _{DDD}	Typ – 4%	4100	Typ + 4%	mV	
SID534	VTR_4P2_F	LVD 4.2 V trimmed falling trip point for V _{DDD}	Typ – 4%	4200	Typ + 4%	mV	
SID535	VTR_4P3_F	LVD 4.3 V trimmed falling trip point for V _{DDD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	VTR_4P4_F	LVD 4.4 V trimmed falling trip point for V _{DDD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	VTR_4P5_F	LVD 4.5 V trimmed falling trip point for V _{DDD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	VTR_4P6_F	LVD 4.6 V trimmed falling trip point for V _{DDD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	VTR_4P7_F	LVD 4.7 V trimmed falling trip point for V _{DDD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	VTR_4P8_F	LVD 4.8 V trimmed falling trip point for V _{DDD}	Typ – 4%	4800	Typ + 4%	mV	
SID541	VTR_4P9_F	LVD 4.9 V trimmed falling trip point for V _{DDD}	Typ – 4%	4900	Typ + 4%	mV	
SID542	VTR_5P0_F	LVD 5.0 V trimmed falling trip point for V _{DDD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	VTR_5P1_F	LVD 5.1 V trimmed falling trip point for V _{DDD}	Typ – 4%	5100	Typ + 4%	mV	
SID544	VTR_5P2_F	LVD 5.2 V trimmed falling trip point for V _{DDD}	Typ – 4%	5200	Typ + 4%	mV	
SID545	VTR_5P3_F	LVD 5.3 V trimmed falling trip point for V _{DDD}	Typ – 4%	5300	Typ + 4%	mV	
SID546	VTR_2P8_R	LVD 2.8 V trimmed rising trip point for V _{DDD}	Typ – 4%	2825	Typ + 4%	mV	Same as V _{TR_2P8_F} + 25 mV
SID547	VTR_2P9_R	LVD 2.9 V trimmed rising trip point for V _{DDD}	Typ – 4%	2925	Typ + 4%	mV	Same as V _{TR_2P9_F} + 25 mV

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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID548	V _{TR_3P0_R}	LVD 3.0 V trimmed rising trip point for V _{DDD}	Typ – 4%	3025	Typ + 4%	mV	Same as V _{TR_3P0_F} + 25 mV
SID549	V _{TR_3P1_R}	LVD 3.1 V trimmed rising trip point for V _{DDD}	Typ – 4%	3125	Typ + 4%	mV	Same as V _{TR_3P1_F} + 25 mV
SID550	V _{TR_3P2_R}	LVD 3.2 V trimmed rising trip point for V _{DDD}	Typ – 4%	3225	Typ + 4%	mV	Same as V _{TR_3P2_F} + 25 mV
SID551	V _{TR_3P3_R}	LVD 3.3 V trimmed rising trip point for V _{DDD}	Typ – 4%	3325	Typ + 4%	mV	Same as V _{TR_3P3_F} + 25 mV
SID552	V _{TR_3P4_R}	LVD 3.4 V trimmed rising trip point for V _{DDD}	Typ – 4%	3425	Typ + 4%	mV	Same as V _{TR_3P4_F} + 25 mV
SID553	V _{TR_3P5_R}	LVD 3.5 V trimmed rising trip point for V _{DDD}	Typ – 4%	3525	Typ + 4%	mV	Same as V _{TR_3P5_F} + 25 mV
SID554	V _{TR_3P6_R}	LVD 3.6 V trimmed rising trip point for V _{DDD}	Typ – 4%	3625	Typ + 4%	mV	Same as V _{TR_3P6_F} + 25 mV
SID555	V _{TR_3P7_R}	LVD 3.7 V trimmed rising trip point for V _{DDD}	Typ – 4%	3725	Typ + 4%	mV	Same as V _{TR_3P7_F} + 25 mV
SID556	V _{TR_3P8_R}	LVD 3.8 V trimmed rising trip point for V _{DDD}	Typ – 4%	3825	Typ + 4%	mV	Same as V _{TR_3P8_F} + 25 mV
SID557	V _{TR_3P9_R}	LVD 3.9 V trimmed rising trip point for V _{DDD}	Typ – 4%	3925	Typ + 4%	mV	Same as V _{TR_3P9_F} + 25 mV
SID558	V _{TR_4P0_R}	LVD 4.0 V trimmed rising trip point for V _{DDD}	Typ – 4%	4025	Typ + 4%	mV	Same as V _{TR_4P0_F} + 25 mV
SID559	V _{TR_4P1_R}	LVD 4.1 V trimmed rising trip point for V _{DDD}	Typ – 4%	4125	Typ + 4%	mV	Same as V _{TR_4P1_F} + 25 mV
SID560	V _{TR_4P2_R}	LVD 4.2 V trimmed rising trip point for V _{DDD}	Typ – 4%	4225	Typ + 4%	mV	Same as V _{TR_4P2_F} + 25 mV
SID561	V _{TR_4P3_R}	LVD 4.3 V trimmed rising trip point for V _{DDD}	Typ – 4%	4325	Typ + 4%	mV	Same as V _{TR_4P3_F} + 25 mV
SID562	V _{TR_4P4_R}	LVD 4.4 V trimmed rising trip point for V _{DDD}	Typ – 4%	4425	Typ + 4%	mV	Same as V _{TR_4P4_F} + 25 mV
SID563	V _{TR_4P5_R}	LVD 4.5 V trimmed rising trip point for V _{DDD}	Typ – 4%	4525	Typ + 4%	mV	Same as V _{TR_4P5_F} + 25 mV
SID564	V _{TR_4P6_R}	LVD 4.6 V trimmed rising trip point for V _{DDD}	Typ – 4%	4625	Typ + 4%	mV	Same as V _{TR_4P6_F} + 25 mV
SID565	V _{TR_4P7_R}	LVD 4.7 V trimmed rising trip point for V _{DDD}	Typ – 4%	4725	Typ + 4%	mV	Same as V _{TR_4P7_F} + 25 mV
SID566	V _{TR_4P8_R}	LVD 4.8 V trimmed rising trip point for V _{DDD}	Typ – 4%	4825	Typ + 4%	mV	Same as V _{TR_4P8_F} + 25 mV

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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID567	V _{TR_4P9_R}	LVD 4.9 V trimmed rising trip point for V _{DDD}	Typ – 4%	4925	Typ + 4%	mV	Same as V _{TR_4P9_F} + 25 mV
SID568	V _{TR_5P0_R}	LVD 5.0 V trimmed rising trip point for V _{DDD}	Typ – 4%	5025	Typ + 4%	mV	Same as V _{TR_5P0_F} + 25 mV
SID569	V _{TR_5P1_R}	LVD 5.1 V trimmed rising trip point for V _{DDD}	Typ – 4%	5125	Typ + 4%	mV	Same as V _{TR_5P1_F} + 25 mV
SID570	V _{TR_5P2_R}	LVD 5.2 V trimmed rising trip point for V _{DDD}	Typ – 4%	5225	Typ + 4%	mV	Same as V _{TR_5P2_F} + 25 mV
SID571	V _{TR_5P3_R}	LVD 5.3 V trimmed rising trip point for V _{DDD}	Typ – 4%	5325	Typ + 4%	mV	Same as V _{TR_5P3_F} + 25 mV
SID573	LVD_RR_A	Power ramp rate: V _{DDD} (Active)	–	–	100	mV/μs	
SID574	LVD_RR_DS	Power ramp rate: V _{DDD} (DeepSleep)	–	–	10	mV/μs	
SID575	t _{DLY_ACT_LVD}	Active mode delay between V _{DDD} falling/ rising through LVD rising/ falling point and an internal LVD output transitioning through V _{DDD} / 2	–	–	1	μs	Guaranteed by design
SID575A	t _{DLY_DS_LVD}	DeepSleep mode delay between V _{DDD} falling/ rising through LVD rising/ falling point and an internal LVD output transitioning through V _{DDD} / 2	–	–	4	μs	Guaranteed by design
SID576	t _{RES_LVD}	Response time of LVD, V _{DDD} supply. LVD guaranteed to generate pulse for V _{DDD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling trip point.)	100	–	–	ns	Guaranteed by design

High-voltage OVD (HV OVD) specifications

SID580	V _{TR_5P0_R}	HV OVD 5.0-V trimmed rising trip point for V _{DDD} and V _{DDA_ADC}	5.049	5.205	5.361	V	
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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID581	VTR_5P0_F	HV OVD 5.0-V trimmed falling trip point for V _{DD} and V _{DDA_ADC}	5.025	5.18	5.335	V	
SID582	VTR_5P5_R	HV OVD 5.5-V trimmed rising trip point for V _{DD} and V _{DDA_ADC} (default)	5.548	5.72	5.892	V	
SID583	VTR_5P5_F	HV OVD 5.5-V trimmed falling trip point for V _{DD} and V _{DDA_ADC} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V _{DD} and V _{DDA_ADC} (Active)	–	–	100	mV/μs	
SID586	HVOVD_RR_DS	Power ramp rate: V _{DD} and V _{DDA_ADC} (DeepSleep)	–	–	10	mV/μs	
SID587	tDLY_ACT_HV_OVD	Active mode delay between V _{DD} falling/ rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD output transitioning through V _{DD} / 2	–	–	1	μs	Guaranteed by design
SID587A	tDLY_ACT_HV_OVD_A	Active mode delay between V _{DDA_ADC} falling/ rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD output transitioning through V _{DD} / 2	–	–	1.5	μs	Guaranteed by design
SID587B	tDLY_DS_HVOVD	DeepSleep mode delay between V _{DD} /V _{DDA_ADC} falling/ rising through V _{TR_5P0_F/R} or V _{TR_5P5_F/R} and an internal HV OVD output transitioning through V _{DD} / 2	–	–	4	μs	Guaranteed by design
SID588	tRES_HVOVD	Response time of HV OVD HV OVD guaranteed to generate pulse for V _{DD} / V _{DDA_ADC} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above V _{TR_5P0_R} or V _{TR_5P5_R})	100	–	–	ns	Guaranteed by design

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表 42 (续) 系统资源

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
Low-voltage OVD (LV OVD) specifications							
SID590	V _{TR_R_LVOVD}	LV OVD trimmed rising trip point for V _{CCD}	Typ – 3%	1300	Typ + 3%	mV	
SID591	V _{TR_F_LVOVD}	LV OVD trimmed falling trip point for V _{CCD}	Typ – 3%	1275	Typ + 3%	mV	Same as V _{TR_R_LVOVD} – 25 mV
SID595	t _{DLY_ACT_LVOVD}	Active mode delay between V _{CCD} falling/ rising through V _{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V _{DDD} / 2	–	–	1	μs	Guaranteed by design
SID595A	t _{DLY_DS_LVOVD}	DeepSleep mode delay between V _{CCD} falling/ rising through V _{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V _{DDD} / 2	–	–	12	μs	Guaranteed by design
SID596	t _{RES_LVOVD}	Response time of LV OVD. LV OVD guaranteed to generate pulse for V _{CCD} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above V _{TR_R_LVOVD})	100	–	–	ns	Guaranteed by design
Over current detection (OCD) specifications							
SID598_A	I _{OCD}	Over current detection range for internal Active regulator	156	–	315	mA	
SID599	I _{OCD_DPSLP}	Over current detection range for internal DeepSleep regulator	18	–	72	mA	

27 电气规范

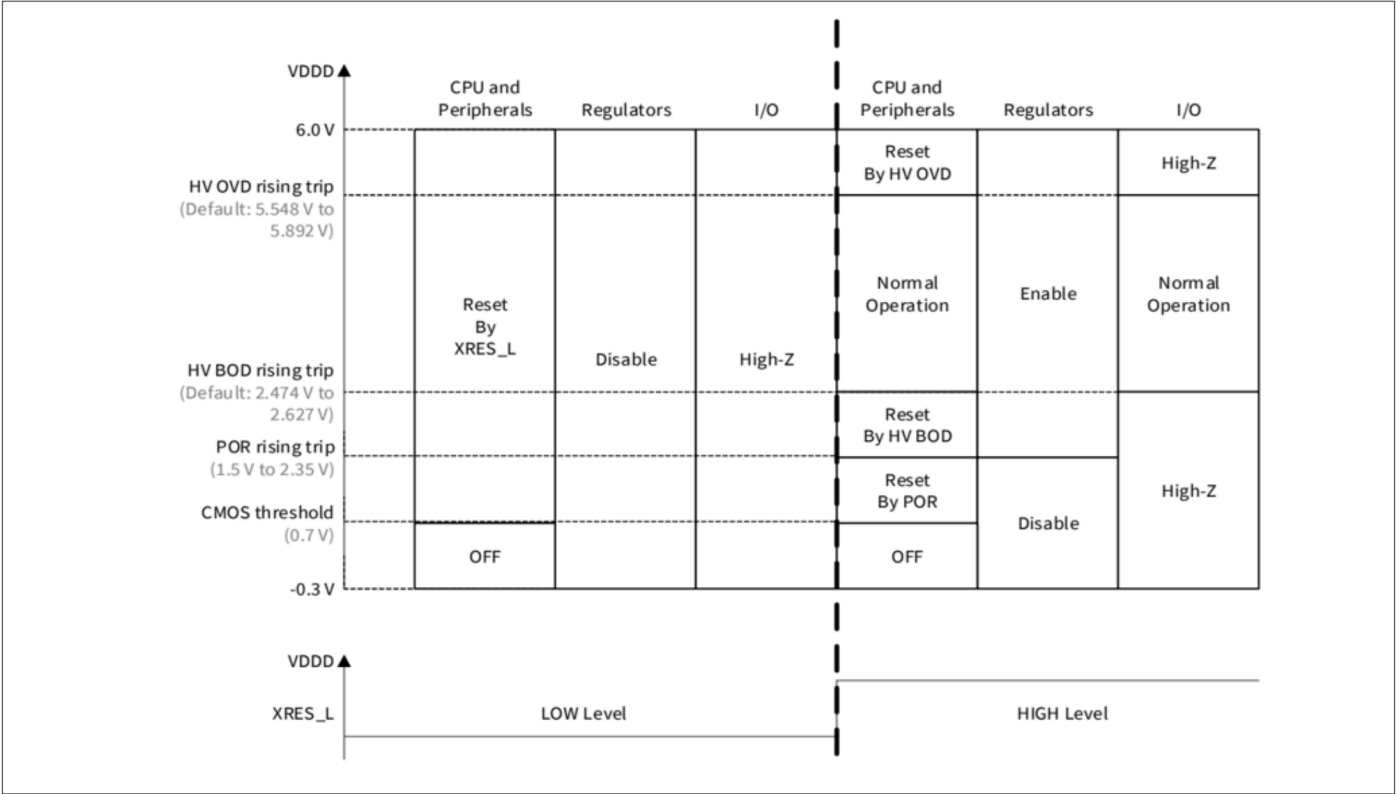


图 23 器件操作电源范围

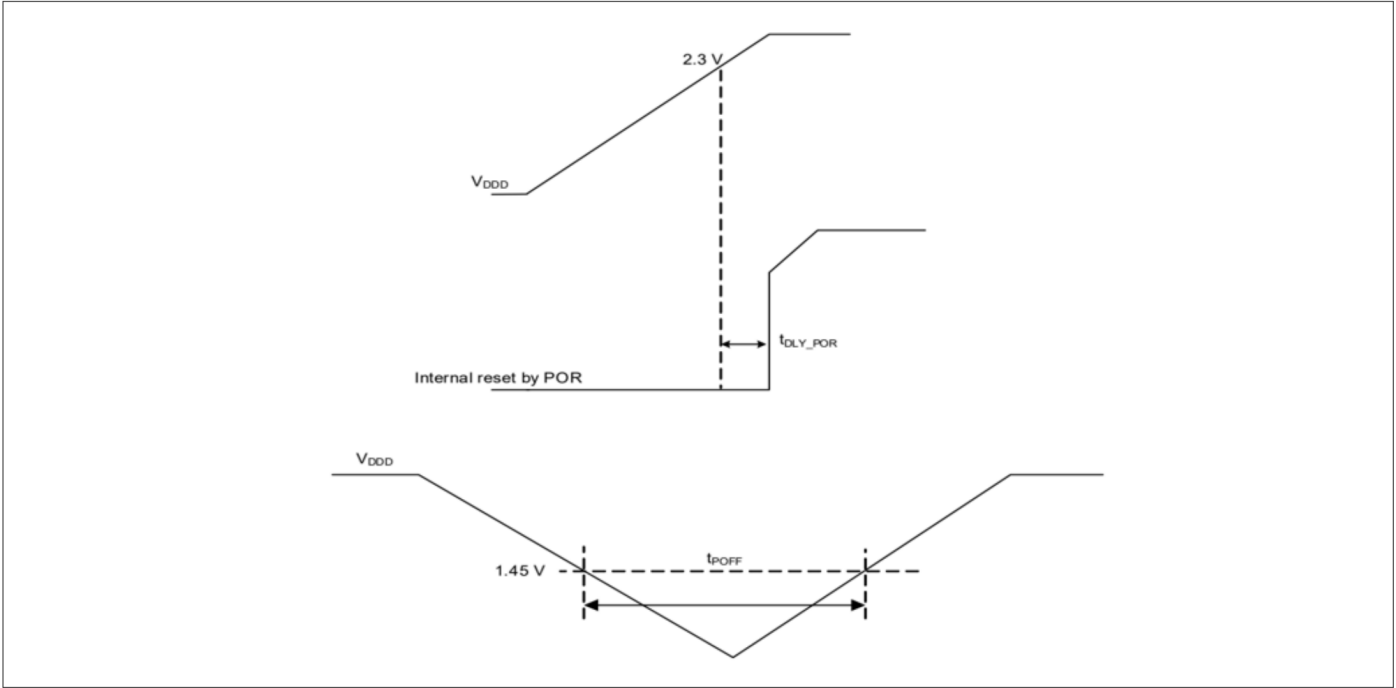


图 24 POR 规格

27 电气规范

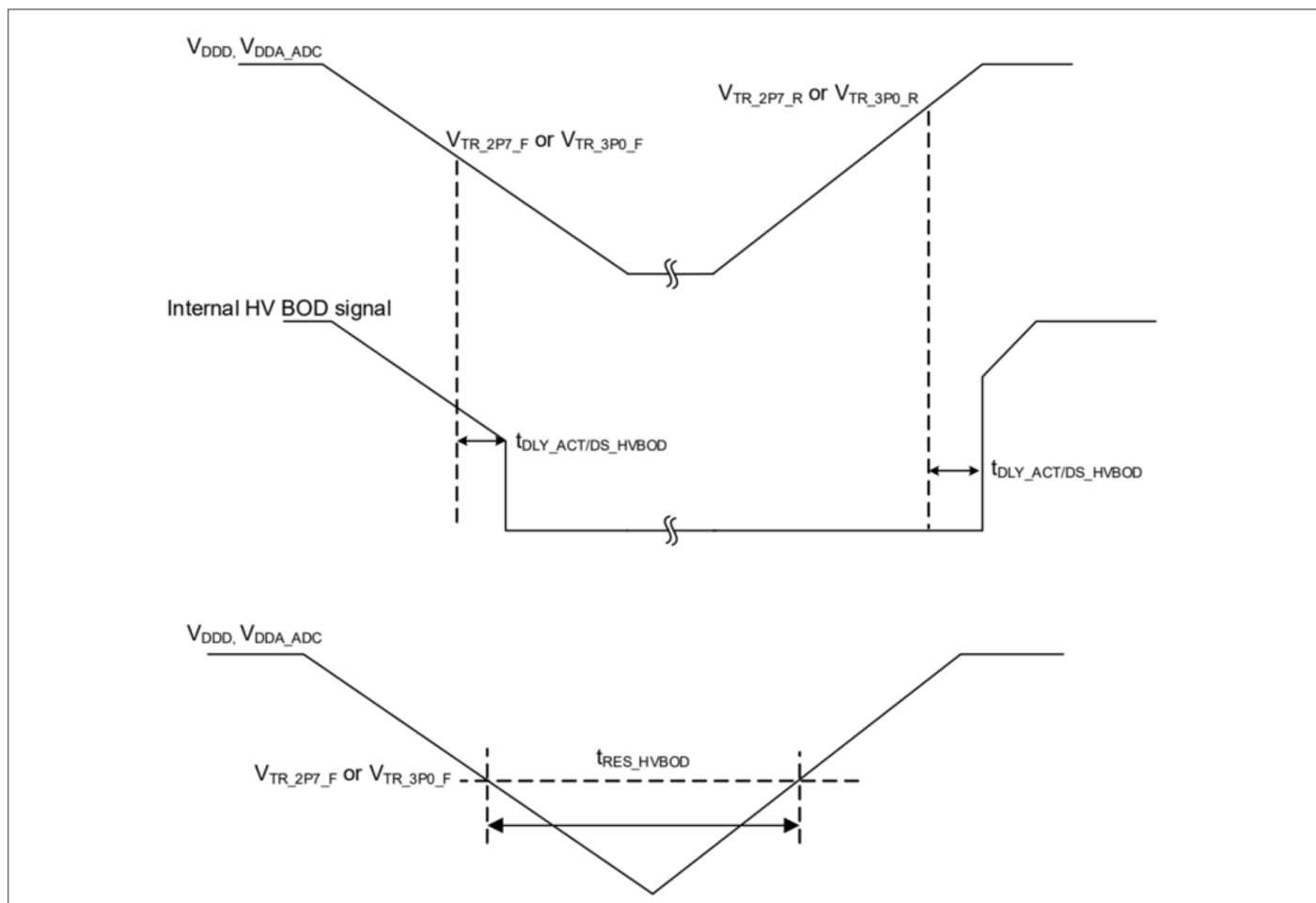


图 25 高压 BOD 规格

27 电气规范

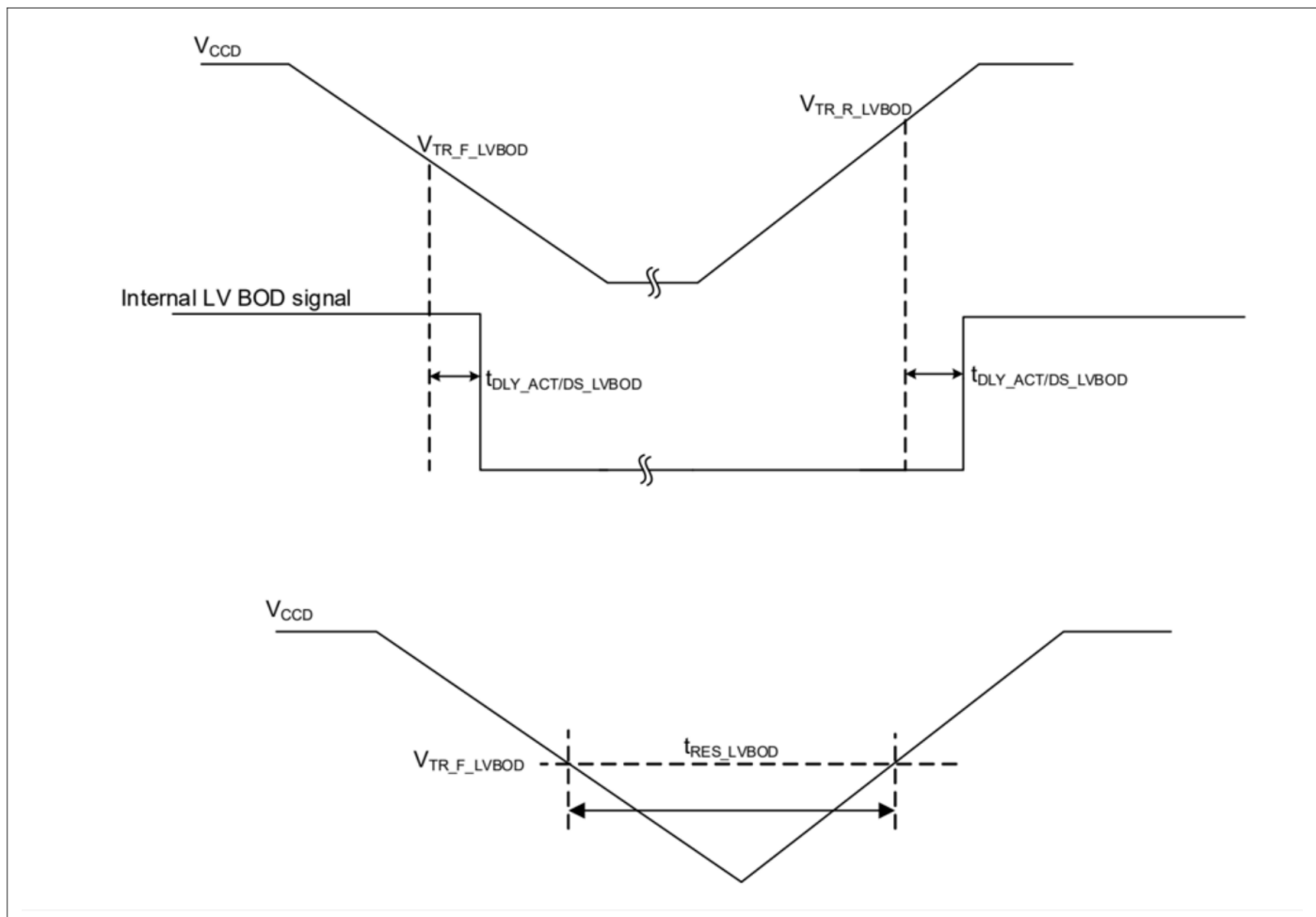


图 26 低压 BOD 规格

27 电气规范

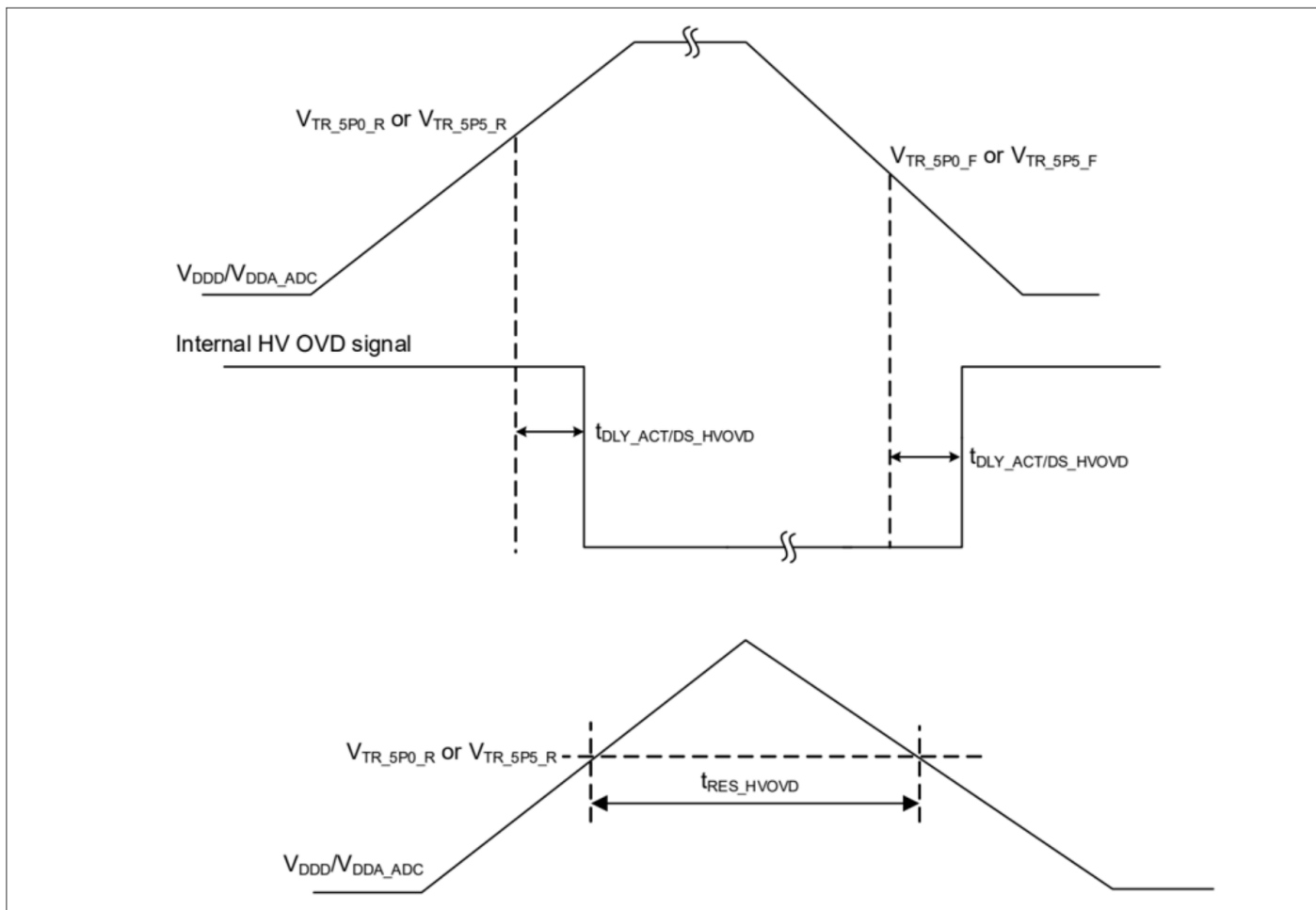


图 27 高压 OVD 规格

27 电气规范

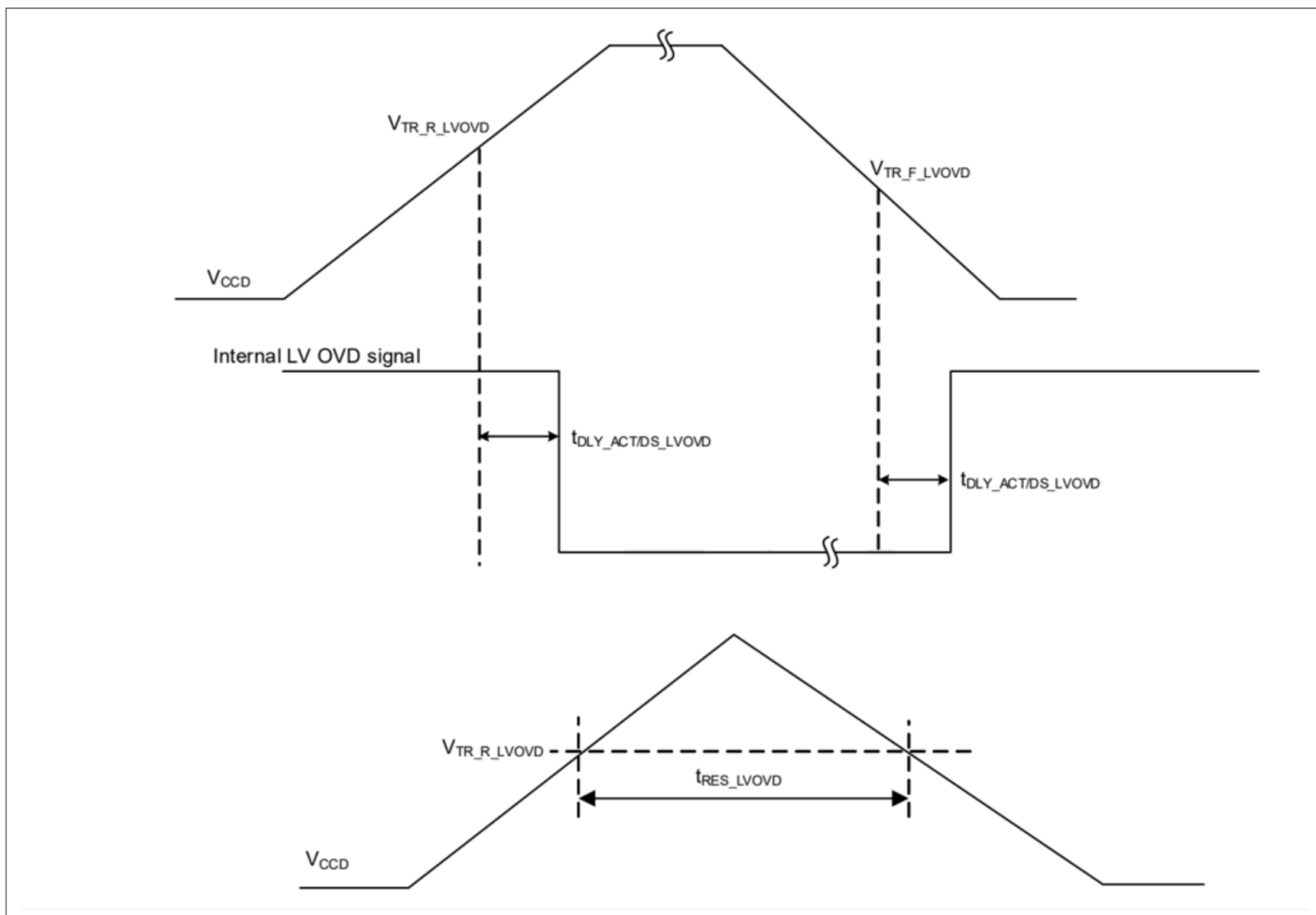


图 28 低压 OVD 规格

27 电气规范

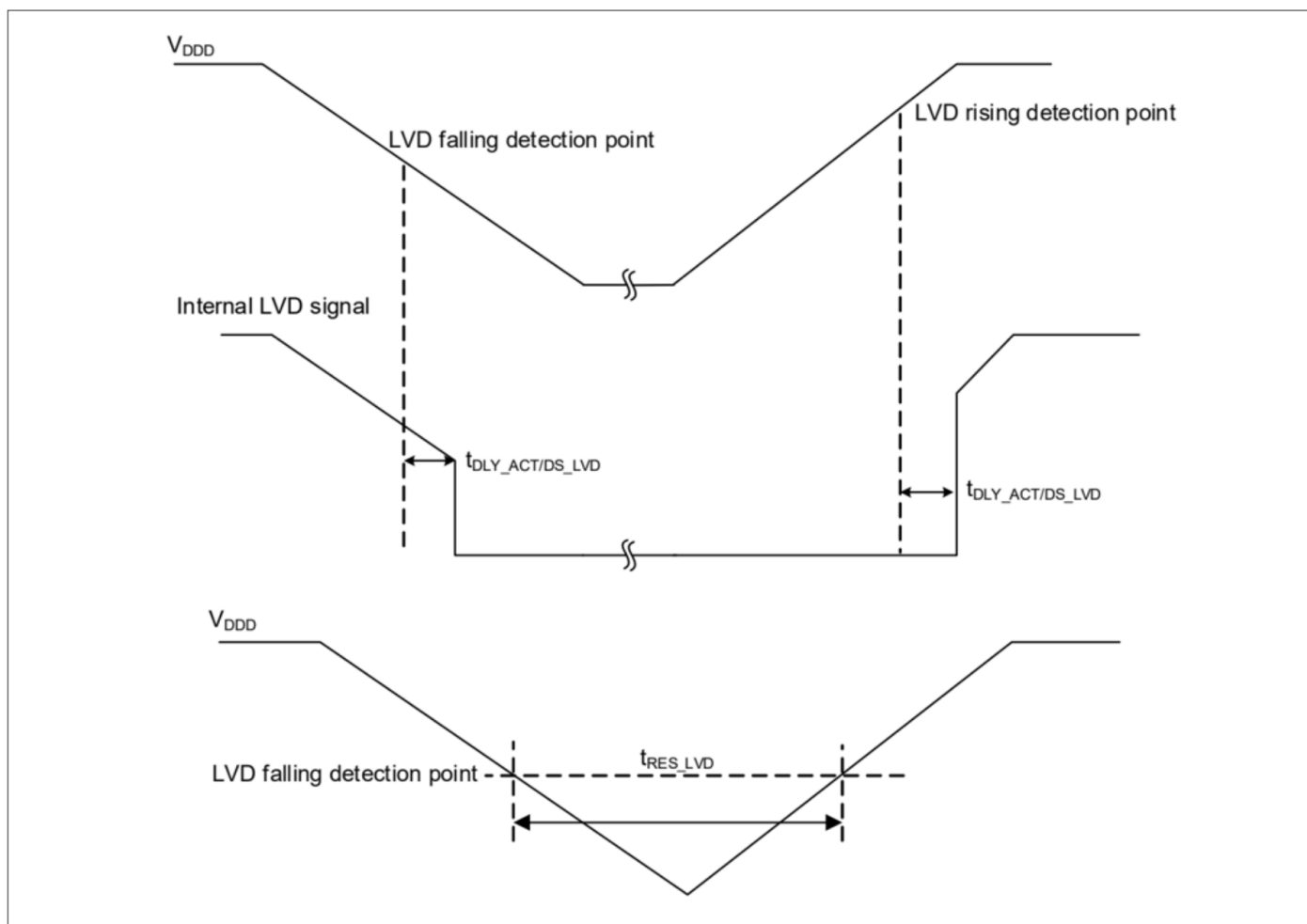


图 29 LVD 规格

表 43 SWD 接口规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置：							
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID300	fSWDCLK	SWD clock input frequency	–	–	10	MHz	$2.7\text{ V} \leq V_{\text{DDIO_GPIO}} \leq 5.5\text{ V}$
SID301	tSWDI_SETUP	SWDI setup time	$0.25 \times T$	–	–	ns	$T = 1/f_{\text{SWDCLK}}$
SID302	tSWDI_HOLD	SWDI hold time	$0.25 \times T$	–	–	ns	$T = 1/f_{\text{SWDCLK}}$
SID303	tSWDO_VALID	SWDO valid time	–	–	$0.5 \times T$	ns	$T = 1/f_{\text{SWDCLK}}$
SID304	tSWDO_HOLD	SWDO hold time	1	–	–	ns	$T = 1/f_{\text{SWDCLK}}$

27 电气规范

表 44 JTAG AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置：							
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID620	t _{JCKH}	TCK HIGH time	25	–	–	ns	30-pF load on TDO
SID621	t _{JCKL}	TCK LOW time	25	–	–	ns	30-pF load on TDO
SID622	t _{JCP}	TCK clock period	62.5	–	–	ns	30-pF load on TDO
SID623	t _{JSU}	TDI/TMS setup time	6.25	–	–	ns	30-pF load on TDO
SID624	t _{JH}	TDI/TMS hold time	6.25	–	–	ns	30-pF load on TDO
SID625	t _{JZX}	TDO High-Z to active	–	–	25	ns	30-pF load on TDO
SID626	t _{JXZ}	TDO active to High-Z	–	–	25	ns	30-pF load on TDO
SID627	t _{JCO}	TDO clock to output	–	–	25	ns	30-pF load on TDO

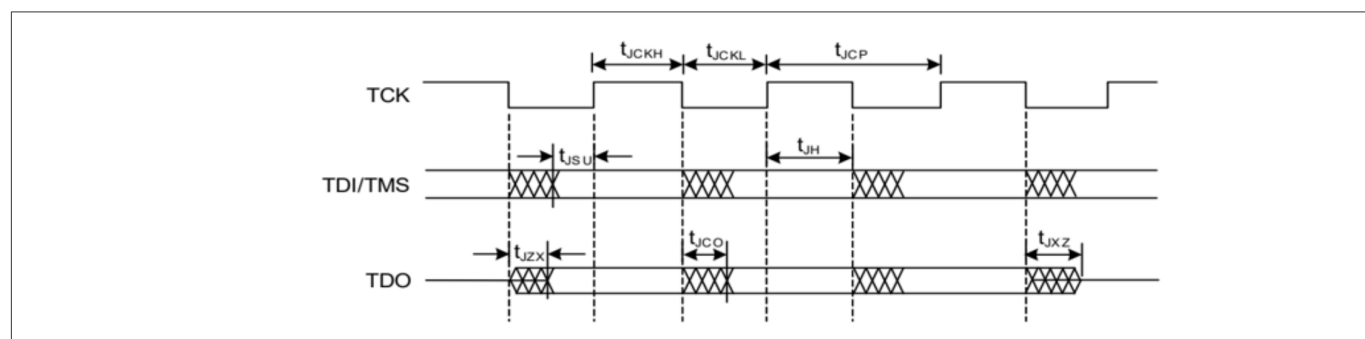


图 30 JTAG 规格

表 45 Trace 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
建议 I/O 配置：							
HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1412A	C _{TRACE}	Trace Capacitive Load	–	–	30	pF	
SID1412	t _{TRACE_CYC}	Trace clock period	20	–	–	ns	Trace clock cycle time for 50 MHz
SID1413	t _{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width

(表格续下页.....)

27 电气规范

表 45 (续) Trace 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1414	tTRACE_CLKH	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width
SID1415	tTRACE_SETUP	Trace data setup time	2	–	–	ns	Trace data setup time, CLK_PERI ≥ 75 MHz
SID1416	tTRACE_HOLD	Trace data hold time	1	–	–	ns	Trace data hold time, CLK_PERI ≥ 75 MHz
SID1415A	tTRACE_SETUP	Trace data setup time	3	–	–	ns	Trace data setup time, CLK_PERI < 75 MHz
SID1416A	tTRACE_HOLD	Trace data hold time	2	–	–	ns	Trace data hold time, CLK_PERI < 75 MHz

27.11 时钟规格

对内核时钟频率依赖性的基本要求是，Cortex®-M0+ 内核的运行频率应为 Cortex®-M4F 内核时钟频率的整数分频。示例组合列于表 27-19 中。

表 46 时钟要求

Core Cortex® -M4F Clock (MHz)	Core Cortex® -CM0+ Clock (MHz)
160	80
100	100
80	80

表 47 根时钟和中间时钟⁴⁾, ²⁾

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ³⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁴⁾			PLL/FLL Clock source: IMO ⁵⁾ , ⁶⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF0	160	PLL200#1	160	NA	NA	153	NA	NA	Root clock for CPUSS (CM0+, CM4), PERI (CLK_SLOW, CLK_PERI)
		FLL	100	NA	NA	100	NA	NA	
	100	PLL200#1	100	NA	NA	95	NA	NA	
		FLL	100	NA	NA	97	NA	NA	
CLK_HF1	100	PLL200#1	100	NA	NA	95	NA	NA	Event generator (CLK_REF), clock output on EXT_CLK pins (when

(表格续下页.....)

27 电气规范

表 47 (续) 根时钟和中间时钟^{1), 2)}

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ³⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁴⁾			PLL/FLL Clock source: IMO ⁵⁾ , ⁶⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
		FLL	100	NA	NA	97	NA	NA	used as output)
CLK_HF2	200	PLL400#0/ PLL200#2/ EXT_CLK	200	196	198	191	189	191	Sound Subsystem #0 root clock, (CLK_IF_SRSS0)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF3	200	PLL400#0/ PLL200#2/ EXT_CLK	200	196	198	191	189	191	Sound Subsystem #1 root clock (CLK_IF_SRSS1)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF4	200	PLL400#0/ PLL200#2/ EXT_CLK	200	196	198	191	189	191	Sound Subsystem #2 root clock (CLK_IF_SRSS2)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF5	200	PLL200#2	200	NA	NA	191	NA	NA	SMIF#0 root clock
		FLL	100	NA	NA	100	NA	NA	
CLK_HF6	ILO		NA						CSV Dedicated (< 1 MHz)
CLK_FAST	160	CLK_HF0	160	NA	NA	153	NA	NA	Generated by dividing CLK_HF0, intermediate clock for CM4
		FLL	100	NA	NA	100	NA	NA	
CLK_SLOW	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_PERI, intermediate clock for CM0+, Crypto, P-DMA, M-DMA
		FLL	100	NA	NA	97	NA	NA	
CLK_PERI	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_HF0, intermediate

(表格续下页.....)

27 电气规范

表 47 (续) 根时钟和中间时钟^{1), 2)}

Root Clock	Maximum permitted clock frequency (MHz) ³⁾	Source	Maximum permitted clock frequency (MHz) ³⁾						Description
			PLL/FLL Clock source: ECO/LPECO ⁴⁾			PLL/FLL Clock source: IMO ⁵⁾ , ⁶⁾			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
		FLL	100	NA	NA	97	NA	NA	clock for LIN, SCB, PASS, CAN, TCPWM,CXPI, IOSS, CPU trace

- 1) 未列出的中间时钟具有与其父时钟相同的限制。
2) 表格显示了根时钟 (CLK_HF_x) 与 PLL 之间的保证映射关系。
3) 相应时钟源 (PLL/FLL + 分频器) 之后的最大时钟频率。所有内部公差和影响都包含在这些频率内。
4) 对于 ECO, LPECO: 设计可容忍外部时钟源高达 ±150 ppm 的不确定度。
5) IMO 操作频率公差包括在内。
6) 通过设计保证了使用 IMO/FLL 以 100 MHz 的频率执行 ROM 和闪存启动。

表 48 PLL400 操作模式

PLL400 operation mode	Spread spectrum clock generation (SSCG)	Fractional
Integer	OFF	OFF
SSCG	ON	OFF
Fractional	OFF	ON

表 49 IMO AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID310	f _{IMO}	IMO operating frequency	7.632	8	8.368	MHz	Accuracy after factory trimming
SID311	t _{STARTIMO}	IMO startup time	-	-	7.5	μs	Startup time to 90% of final frequency
SID312	I _{IMO_ACT}	IMO current	-	13.5	22	μA	Guaranteed by design

表 50 ILO AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID320	f _{ILOTRIM}	ILO operating frequency	30.965	32.768	34.57	kHz	5.5% accuracy after factory trimming
SID321	t _{STARTILO}	ILO startup time	-	8	12	μs	Startup time to 90% of final frequency
SID323	I _{ILO}	ILO current	-	500	2800	nA	Guaranteed by design

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表 51 LPECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID325	fLPECO	LPECO operating frequency	3.99	–	8.01	MHz	Drive level protection DL ≥ 100 μW, ESR ≤ 200 Ω Crystal load capacitance (C _L) 5 pF to 25 pF
SID329	ILPECO_4M	LPECO current at 4 MHz	–	93	110	μA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID354	ILPECO_4M	LPECO current at 4 MHz	–	97	125	μA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID326	ILPECO_4M	LPECO current at 4 MHz	–	106	145	μA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID355	ILPECO_4M	LPECO current at 4 MHz	–	115	155	μA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID356	ILPECO_8M	LPECO current at 8 MHz	–	140	165	μA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID357	ILPECO_8M	LPECO current at 8 MHz	–	149	175	μA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID327	ILPECO_8M	LPECO current at 8 MHz	–	165	190	μA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0
SID358	ILPECO_8M	LPECO current at 8 MHz	–	183	220	μA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/ LPECO_AMPDET_EN<0:0>=0b0

(表格续下页.....)

表 51 (续) LPECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID328	tSTART_LPECO	LPECO startup time[62]	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (BACKUP_LPECO_CTL.LPECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_LPECO_STATUS.LPECO_READY<0:0>=0b1 and BACKUP_LPECO_STATUS.LPECO_AMPDET_OK<0:0>=0b1).

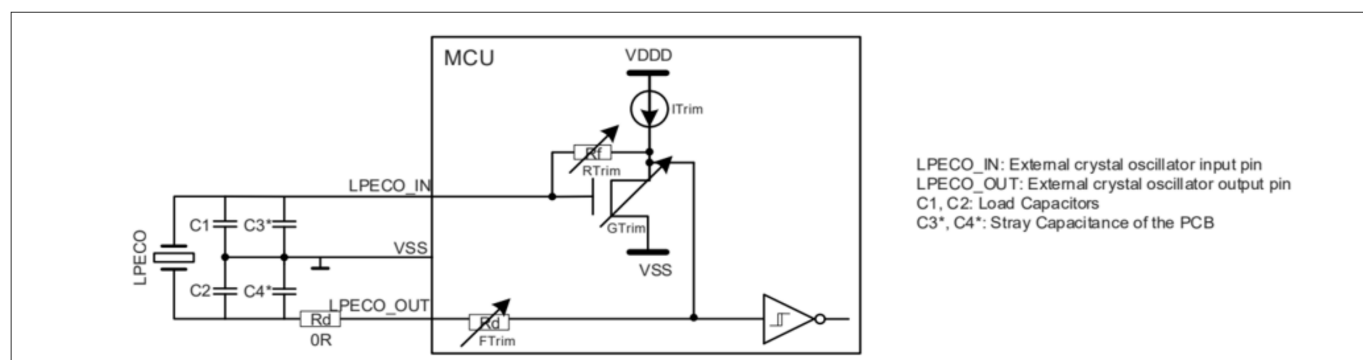


图 31 **LPECO 连接方案¹⁶⁾**

表 52 **ECO 规格**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID330	f _{ECO}	Crystal frequency range	7.2	–	33.34	MHz	
SID332	R _{FDBK}	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100 kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design
SID333	I _{ECO3}	ECO current at T _J = 150°C	–	1200	2000	μA	Maximum operation current at 33 MHz crystal, up to 18 pF load

(表格续下页.....)

¹⁶ 有关晶振要求的更多信息，可参阅特定于系列的架构 TRM（002-19314，TRAVEO™ T2G 汽车车身控制器项系列架构技术基准手册（TRM））。

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表 52 (续) ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID334	t _{START_7M}	7.2 MHz ECO startup time ¹⁾	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).
SID335	t _{START_33M}	33 MHz ECO startup time ¹⁾	–	–	1	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).

1) 振荡器启动时间是一个性能参数，主要取决于所选的外部晶振和负载电容。

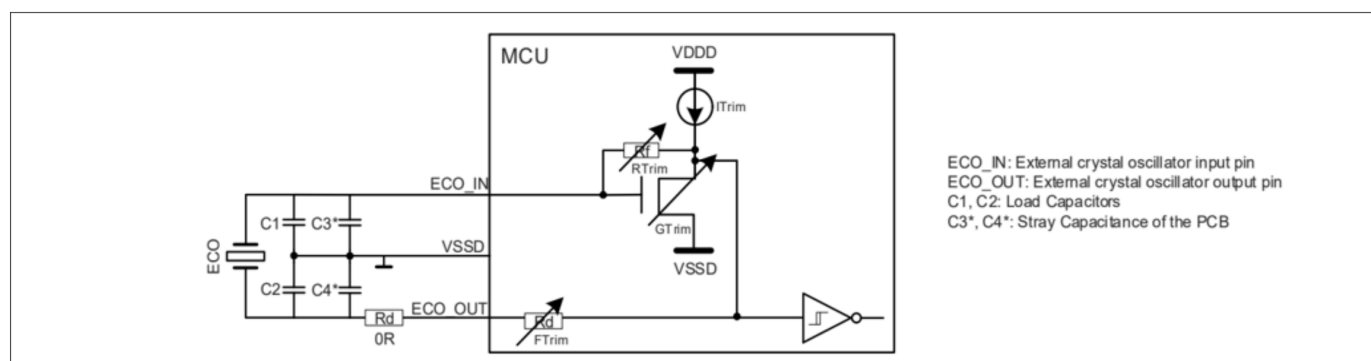


图 32 ECO 连接方案¹⁷⁾

表 53 PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
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PLL Specifications for “PLL without SSCG and Fractional Operation” (PLL200)

(表格续下页...)

¹⁷⁾ 有关晶体要求的更多信息，请参阅特定系列的架构技术参考手册（002-33175，TRAVEO™ T2G 车规级 MCU 入门级架构技术参考手册）。在启用 ECO 之前，应将 TRIM 寄存器配置为正确的设置（ATRIM、WDTRIM、FTRIM、GTRIM 和 RTRIM），配置依据《用户指南》中的“ECO 参数设置，TRAVEO™ T2G 系列”（文档编号 002-30194）以及晶体供应商提供的晶体匹配测试结果。

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表 53 (续) PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SI D3 40	t _{PLL200_LOCK}	Time to achieve PLL lock	–	–	35	μs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SI D3 41	f _{OUT}	Output frequency from PLL block (PLL_OUT)	10.998	–	200.03	MHz	
SI D3 46	f _{IN}	PLL input frequency (Reference Clock f _{REF})	3.988	–	33.34	MHz	
SI D3 47	I _{PLL_200M}	PLL operating current	–	0.87	1.85	mA	f _{OUT} = 200 MHz
SI D3 48 C	f _{PLL_VCO}	VCO frequency, clock output of 'Voltage Control Oscillator (VCO)'	169.9745	–	400.06	MHz	
SI D3 49 C	f _{PLL_PFD}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	8.0012	MHz	
SI D3 42	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by design f _{PLL_VCO} : 320 MHz or 400 MHz f _{PLL_OUT} : 40 MHz to 200 MHz f _{PLL_PFD} : 8 MHz f _{PLL_IN} : ECO

(表格续下页.....)

27 电气规范

表 53 (续) PLL 规格

Sp ec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SI D3 43	PLL_LJIT2	Long term jitter	-0.5	–	0.5	ns	For 500 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SI D3 44	PLL_LJIT3	Long term jitter	-0.5	–	0.5	ns	For 1000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO
SI D3 45 A1	PLL_LJIT5	Long term jitter	-0.75	–	0.75	ns	For 10000 ns Guaranteed by design $f_{\text{PLL_VCO}}$: 320 MHz or 400 MHz $f_{\text{PLL_OUT}}$: 40 MHz to 200 MHz $f_{\text{PLL_PFD}}$: 8 MHz $f_{\text{PLL_IN}}$: ECO

PLL Specifications for “PLL with SSCG and Fractional Operation” (PLL400)

SI D3 40 A	$t_{\text{PLL400_LOCK}}$	Time to achieve PLL lock	–	–	50	μs	
SI D3 41 A	f_{OUT}	Output frequency from PLL block (PLL_OUT)	24.996	–	400.06	MHz	
SI D3 43 A	SPREAD_D	Spread spectrum modulation depth	0.5	–	3	%	Down spread only, triangle modulation

(表格续下页.....)

27 电气规范

表 53 (续) PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SI D3 43 B	fSPREAD_MR	Spread spectrum modulation rate	–	–	32	kHz	Selected by modulation divider from f _{PDF}
SI D3 46 A	f _{IN}	PLL input frequency (Reference Clock f _{REF})	3.988	–	33.34	MHz	
SI D3 47 A	IPLL_400M	PLL operating current	–	1.4	2.2	mA	f _{OUT} = 400 MHz
SI D3 48 A	fPDF_S	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	20.003	MHz	Fractional operation OFF
SI D3 49 A	fPDF_F	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	7.9988	–	20.003	MHz	Fractional operation ON
SI D3 45 A	f _{VCO}	VCO frequency, Clock output of 'Voltage Control Oscillator (VCO)'	399.94	–	800.12	MHz	
SI D3 42 D1	PLL400_LJIT 1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by Design f _{VCO} : 800 MHz (Integer mode) f _{IN} : ECO f _{PDF} : 4 MHz f _{OUT} : 100 MHz to 400 MHz

(表格续下页.....)

27 电气规范

表 53 (续) PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SI D3 43 D1	PLL400_LJIT 2	Long term jitter	-0.5	-	0.5	ns	For 500 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz
SI D3 44 D1	PLL400_LJIT 3	Long term jitter	-1	-	1	ns	For 1000 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz
SI D3 45 E1	PLL400_LJIT 5	Long term jitter	-1.5	-	1.5	ns	For 10000 ns Guaranteed by Design f_{VCO} : 800 MHz (Integer mode) f_{IN} : ECO f_{PFD} : 4 MHz f_{OUT} : 100 MHz to 400 MHz

表 54 FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	-	-	5	μs	Wakeup with <10°C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value

(表格续下页.....)

27 电气规范

表 54 (续) FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID351	f _{FLL_OUT}	Output frequency from FLL block	24	-	100	MHz	Output range of FLL divided-by-2 output
SID352	FLL_CJIT	FLL frequency accuracy	-1	-	1	%	This is added to the error of the source
SID353	f _{FLL_IN}	Input frequency	0.25	-	100	MHz	

表 55 WCO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	f _{wco}	Watch crystal frequency	-	32.768	-	kHz	Tuning Fork Crystal with following parameters: DL (drive level) ≥ 0.5 μW, ESR ≤ 130 k Ω
SID361	WCO_DC	WCO duty cycle	10	-	90	%	
SID362	t _{START_WCO}	WCO start up time ¹⁾	-	-	1000	ms	Time from oscillator enable (BACKUP_CTL.WCO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_STATUS.WCO_OK<0:0>=0b1)
SID363	I _{wco}	WCO current	-	1.4	-	μA	AGC = OFF

1) 振荡器启动时间是一个性能参数，主要取决于所选的外部晶振和负载电容。

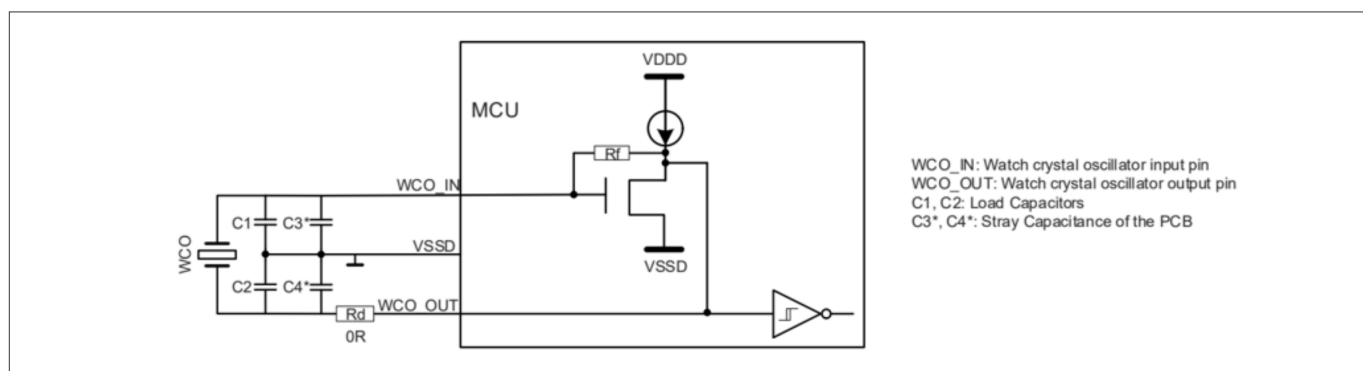


图 33 WCO 连接方案¹⁸⁾

表 56 外部时钟输入规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f _{EXT}	External clock input frequency	0.25	-	100	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	Duty cycle	45	-	55	%	

¹⁸⁾ 有关晶振要求的更多信息，可参阅特定系列的架构 TRM (002-33175, TRAVEO™ T2G 车规级 MCU 仪表簇入门架构技术参考手册)。

27 电气规范

27.12 时钟时序图

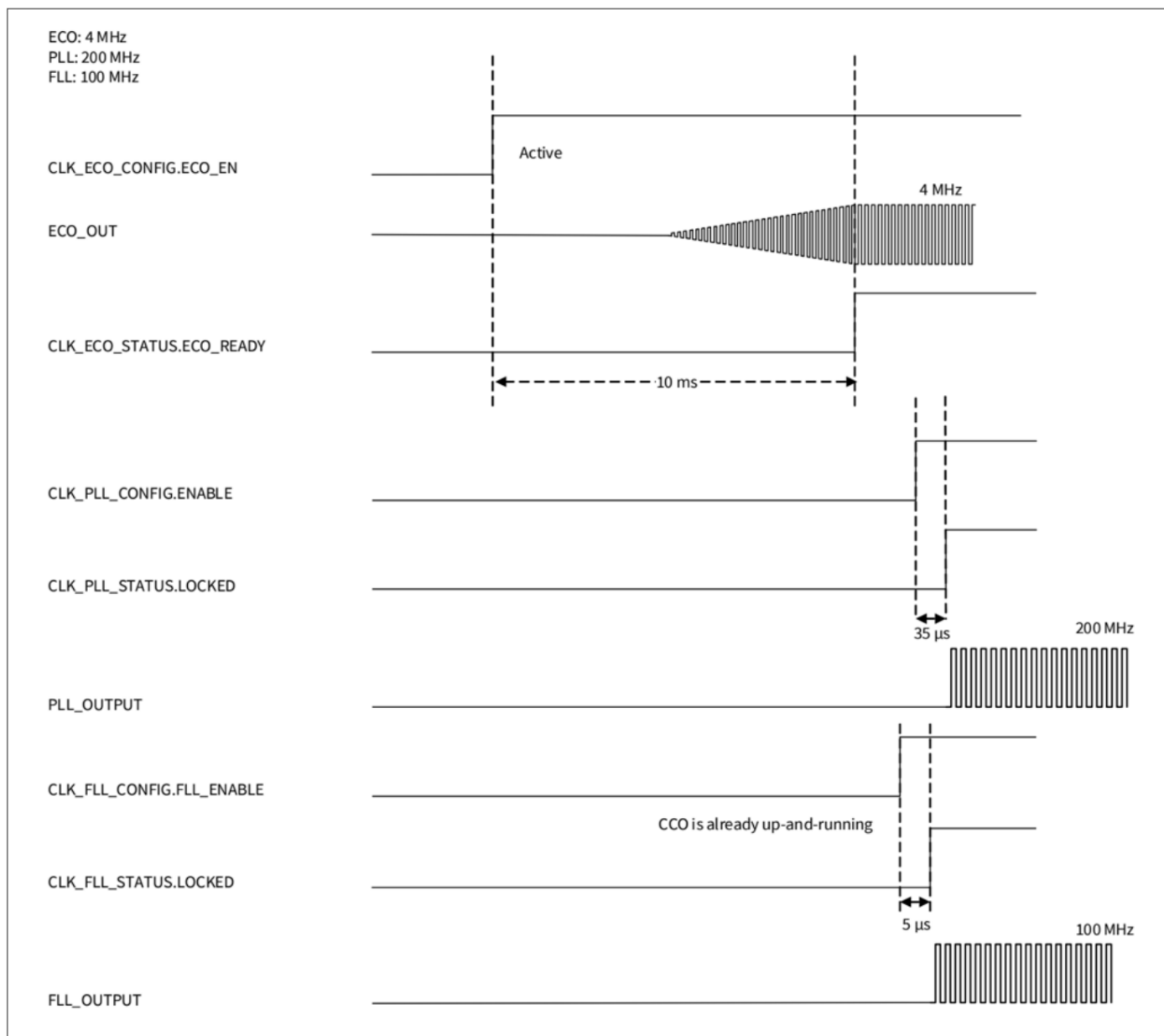


图 34 ECO 至 PLL 或 FLL 图

27 电气规范

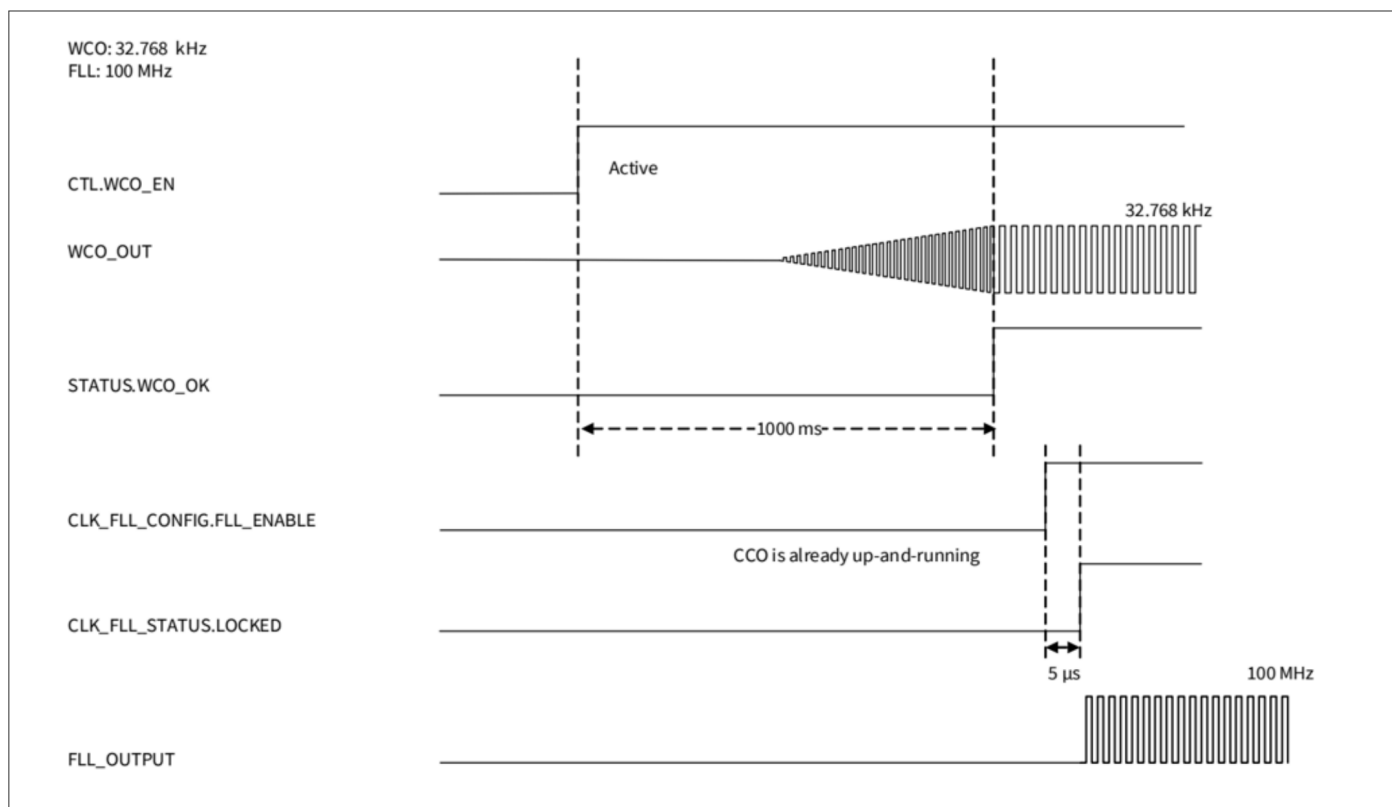


图 35 WCO 至 FLL 图

表 57 MCWDT 超时规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID410	tMCWDT1	Minimum MCWDT timeout	57.85	-	-	μs	When using the ILO (32 kHz + 5.5%) and 16-bit MCWDT counter Guaranteed by design
SID411	tMCWDT2	Maximum MCWDT timeout	-	-	2.12	s	When using the ILO (32 kHz - 5.5%) and 16-bit MCWDT counter Guaranteed by design

表 58 WDT 超时规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID412	tWDT1	Minimum WDT timeout	57.85	-	-	μs	When using the ILO (32 kHz+5.5%)and 32-bit WDT counter Guaranteed by design
SID413	tWDT2	Maximum WDT timeout	-	-	38.53	h	When using the ILO (32 kHz-5.5%)and 32-bit WDT counter Guaranteed by design
SID414	tWDT3	Default WDT timeout	-	1000	-	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design

27 电气规范

27.13 声音子系统规格

表 59 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
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I²S I/O 设置

建议 I/O 配置

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1

I²S 串行时钟频率

SID796	tsCLK	Serial clock period	162	–	–	ns	Guaranteed by design No feature is used for low frequency I ² S operation: DUT RX Master: * RX_IF_CTL.LATE_SAMPLE = 0 * RX_IF_CTL.LATE_CAPTURE = 0b00 DUT TX slave: No special configuration DUT RX slave: * RX_IF_CTL.LATE_SAMPLE = 0 I ² S can only be used at 2.7 V ≤ V _{DD} ≤ 3.6 V
SID797	thC	Serial clock high time	0.35 × tsCLK	–	–	ns	Guaranteed by design
SID798	tlC	Serial clock low time	0.35 × tsCLK	–	–	ns	Guaranteed by design
SID799	tmCLK	Master clock period	20	–	–	ns	Guaranteed by design I ² S can only be used at 2.7 V ≤ V _{DD} ≤ 3.6 V

I²S 发射器时序

SID740	tdTR	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	0.8 × tsCLK	ns	Guaranteed by design
SID741	thTR	Hold from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design

(表格续下页.....)

27 电气规范

表 59 (续) 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID743	t _{HR_WS_P} OL_0	TX slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	

I²S 接收器时序

SID751	t _{SR}	Setup on RX_SD/ RX_FSYNC (WS) before the rising edge to RX_CLK	0.2 × t _{SCLK}	–	–	ns	Guaranteed by design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE or SCK_POLARITY setting
SID752A	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the rising edge to RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 × t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-slave: SCK_POLARITY = 0
SID753	t _{SCLK_TRANS}	SCLK transition timing	1	–	8	ns	20% to 80%
SID754	t _{MCLK_TRANS}	MCLK transition timing	1	–	8	ns	20% to 80%
SID755	t _{DATA_TRANS}	DATA transition timing	1	–	8	ns	20% to 80%

TDM I/O 设置

建议 I/O 配置

对于高达 25 MHz 的串行时钟

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1

TDM Serial Clock

(表格续下页...)

27 电气规范

表 59 (续) 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1000 B	tsCLK	Serial clock period, TDM[x] (x=0 through 1)	40	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX slave: RX_IF_CTL.SCK_POLARITY= 0 TDM can only be used at $2.7\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$
SID1000 D	tsCLK	Serial clock period, TDM[x] (x=0 through 1)	80	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX slave: RX_IF_CTL.SCK_POLARITY = 0 TDM can only be used at $2.7\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$
SID1001	thC	Serial clock high time	$0.35 \times \text{tsCLK}$	–	–	ns	Guaranteed by design
SID1002	tlC	Serial clock low time	$0.35 \times \text{tsCLK}$	–	–	ns	Guaranteed by design
SID1010 A	tMCLK	Master clock input period	20	–	–	ns	MCLK must be SCLK*2; The maximum output frequency of the TDM depends on the used I/O type.
SID1002 B	tMCLK	Master clock output period	40	–	–	ns	

(表格续下页.....)

27 电气规范

表 59 (续) 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1002D	tMCLK_IH	Master clock input HIGH time	$0.45 \times t_{MCLK}$	–	–	ns	
SID1002E	tMCLK_IL	Master clock input LOW time	$0.45 \times t_{MCLK}$	–	–	ns	

TDM transmit timing

SID1003	tDTR	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	$0.8 \times t_{SCLK}$	ns	Guaranteed by design
SID1004	tHTR	Hold from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID1011	tHR_WS_P OL_0	TX slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	
SID1012	tHR_WS_P OL_1	TX slave: Hold on TX_FSYNC (WS) after the 2nd edge following the driving edge of TX_CLK (SCK_POLARITY = 1, zero-cycle hold)	1.8	–	–	ns	

TDM receive timing

SID1005	tSR	Setup on RX_SD/ RX_FSYNC (WS) before the 1st edge following the driving edge of RX_CLK	$0.2 \times t_{SCLK}$	–	–	ns	Guaranteed by design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE and SCK_POLARITY setting
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(表格续下页.....)

27 电气规范

表 59 (续) 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1006C	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 1st edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-slave: SCK_POLARITY = 0
SID1006D	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 2nd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by design Sampling edge w.r.t driving edge of RX_SCLK: 2nd edge (1 x t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 1, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-slave: SCK_POLARITY = 1
SID1006E	t _{HR}	Hold on RX_SD/ RX_FSYNC (WS) after the 3rd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by design Sampling edge w.r.t driving edge of RX_SCLK: 3rd edge (1.5 x t _{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b01 RX slave: not applicable

TDM transition timing

SID1007B	t _{SCLK_TRANS}	SCLK input transition timing	1	–	0.15 × t _{SCLK}	ns	Guaranteed by design
SID1008	t _{MCLK_TRANS}	MCLK input/output transition timing	–	–	0.15 × t _{SCLK}	ns	Guaranteed by design
SID1009B	t _{DATA_TRANS}	DATA input transition timing	1	–	0.15 × t _{SCLK}	ns	Guaranteed by design
SID1007C	t _{SCLK_TRANS}	SCLK output transition timing	0.1	–	0.15 x t _{SCLK}	ns	TTL Level
SID1009C	t _{DATA_TRANS}	DATA output transition timing	0.1	–	0.15 x t _{SCLK}	ns	TTL Level

(PCM) PWM

(表格续下页.....)

27 电气规范

表 59 (续) 声音子系统规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
建议 I/O 配置:							
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01							
GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01							
GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01							
SID1100_2	tpw_2	Pulse width on CH1_P, CH1_N, CH2_P, CH2_N for GPIO	20	–	–	ns	PWM clock ≤ 40 MHz, min pulse width nom. 25 ns – 20% max distortion (PCM) PWM can only be used at 2.7 V ≤ V _{DD} ≤ 3.6 V Guaranteed by design
SID1101	fPWM	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1110	tmCLK	Master clock input period	10	–	–	ns	Guaranteed by design
SID1111	tmCLKI_DUTY	Master clock input duty cycle	40	–	50	%	Guaranteed by design

Sound generator

建议 I/O 配置:

GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01

GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01

GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01

SID1102	fPWM	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1103	tmCLK	Master clock input period	10	–	–	ns	Guaranteed by design
SID1104	tmCLKI_DUTY	Master clock input duty cycle	40	–	50	%	Guaranteed by design

27.14 CXPI 规格

表 60 CXPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1400	fCLK_AHB	CLK_PERI clock frequency	–	–	100	MHz	Guaranteed by design, AHB Interface clock
SID1402	tBIT_CONT	Width of clock disparity against the bit width t _{BIT_REF} of nominal signaling rate	–0.5	–	+0.5	%	Guaranteed by design

(表格续下页.....)

27 电气规范

表 60 (续) CXPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1403	trx_0_HI_CONT	The time that should be detected the receiving node is HIGH level.	0.02	–	–	t _{BIT}	t _{BIT} = 1/f _{BRC} , Guaranteed by design
SID1404	ttX_DIF_CONT	Difference of width of LOW-level at the constant threshold that receiving node should discriminate logic '1' and logic '0'	0.05	–	–	t _{BIT}	t _{BIT} = 1/f _{BRC} , Guaranteed by design ttX_DIF_CONT = ttX_0_LO – ttX_1_LO
SID1405	ttX_0_PD_CONT [68]	At the time of logical value '0' outputs, time from the LOW level detection of the communication bus unit falling the voltage "TH_dom".	–	–	0.01	t _{BIT}	t _{BIT} = 1/f _{BRC} , CTL0.FILTER_EN bit = '0', Guaranteed by design
SID1406	ttX_0_PD_CONT 1)	At the time of logical value '0' outputs, time from the LOW-level detection of the communication bus unit falling the voltage "TH_dom".	–	–	0.0125	t _{BIT}	t _{BIT} = 1/f _{BRC} , CTL0.FILTER_EN bit = '1', Guaranteed by design
SID1407	trx_0_FF_CONST	Delay from external serial data input pin to a flop. This is a standard to satisfy AC.11.	–	–	20	ns	Guaranteed by design
SID1408	ttX_0_FF_CONST	Delay from a flop to external serial data output pin. This is a standard to satisfy AC.11.	–	–	80	ns	Guaranteed by design
SID1409	BR	Bit rate	–	–	20	kbps	
SID1411	OS	Oversampling factor	–	–	400		

1) 根据 CXPI 控制器规范, AC 规范最大为 0.01 t_{BIT}。根据 CXPI 系统规范, AC 规范 (包括收发器或驱动器/接收器) 最大为 0.1 t_{BIT}。

27 电气规范

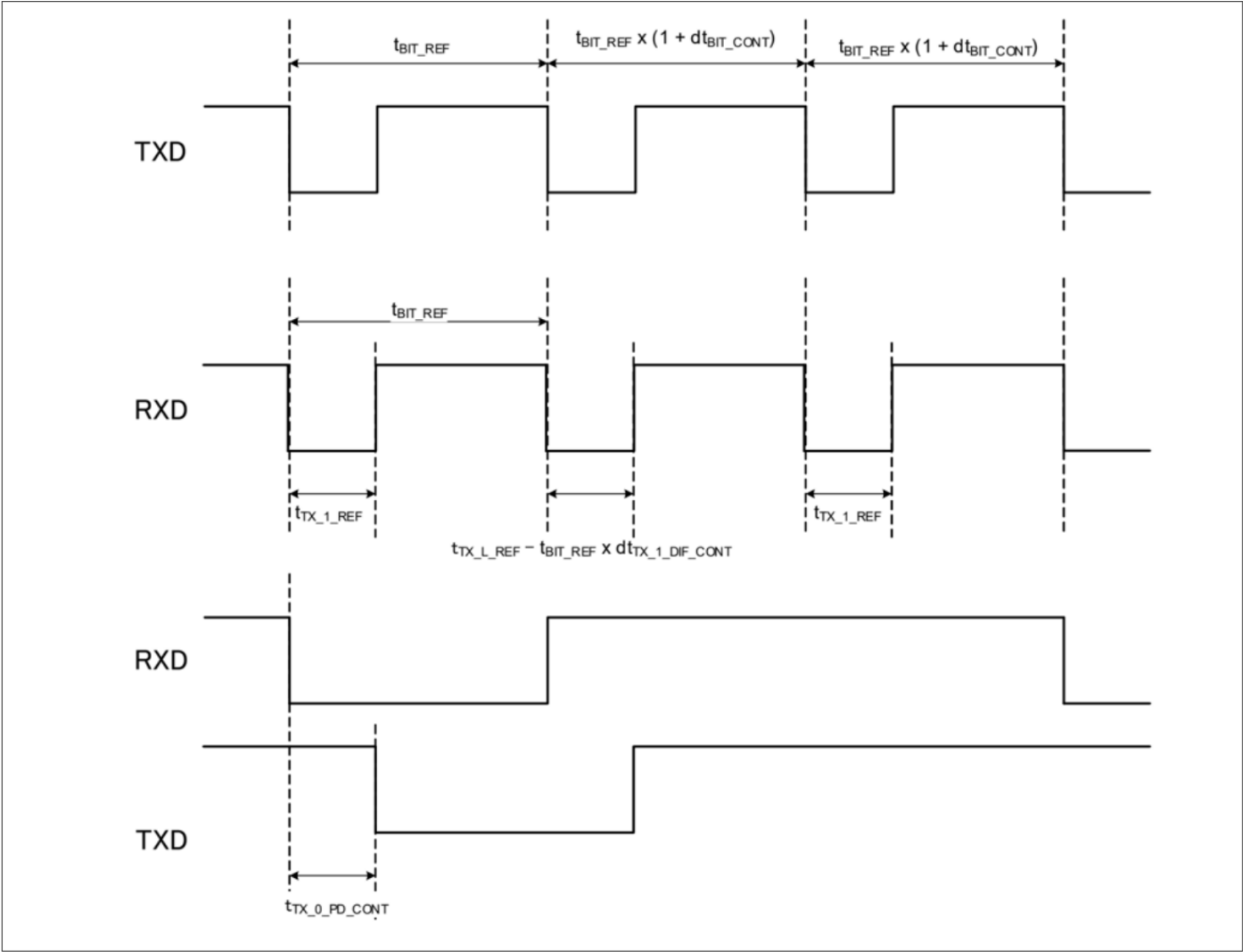


图 36 CXPI 规格

27.15 串行存储器接口规格

表 61 xSPI 规格

Spec ID	Parameter	Description	Min.	Max.	Units
xSPI (JEDEC JESD251 xSPI200)			xSPI200		
建议 I/O 配置					
xSPI200: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0>=0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b0, CFG_SLEW_EXT/SLEW<0:0>= 0b0 (single and dual slave [load ≤ 15 pF])					
SID1500_3	t _{CK}	Interface clock period (JEDEC)	10	-	ns
SID1500_3CM	t _{CK}	Interface clock period (CMOS)	10	-	ns
SID1501_3	t _{CKDCD}	Allowable clock distortion 1)	-	0.05×t _{CK}	ns
SID1502_3	t _{CKMPW}	Minimum clock pulse width (JEDEC)	4.5	-	ns

(表格续下页.....)

27 电气规范

表 61 (续) xSPI 规格

Spec ID	Parameter	Description	Min.	Max.	Units
xSPI (JEDEC JESD251 xSPI200)			xSPI200		
SID1502_3CM	t _{CKMPW}	Minimum clock pulse width (CMOS)	4.5	-	ns
SID1503_3HV	OUT_SR	Output slew rate with respect to V _{OH} /V _{OL}	1.03	-	V/ns
SID1504_3	t _{OSU}	Output setup time of DS and I/O[7:0] to CK	1.1	-	ns
SID1505_3	t _{OH}	Output hold time of DS and I/O[7:0] to CK	1.1	-	ns
SID1506_3HV	IN_SR	Input slew rate with respect to V _{IH} /V _{IL}	1.03	-	V/ns
SID1507_3	t _{DSPW}	Input min pulse width of DS (JEDEC)	4.1	-	ns
SID1507_3CM	t _{DSPW}	Input min pulse width of DS (CMOS)	4.1	-	ns
SID1508_3	t _{RQ}	Input DS to I/O[7:0] valid time (JEDEC)	-	0.9	ns
SID1508_3CM	t _{RQ}	Input DS to I/O[7:0] valid time (CMOS)	-	0.9	ns
SID1509_3	t _{RQH}	Input I/O[7:0] invalid to DS time (JEDEC)	-	0.9	ns
SID1509_3CM	t _{RQH}	Input I/O[7:0] invalid to DS time (CMOS)	-	0.9	ns
SID1511_3	t _{CKLCSL}	CK LOW to CS LOW	8	-	ns
SID1512_3	t _{CSLCKH}	CS LOW to CK HIGH	8	-	ns
SID1513_3	t _{CKLCSH}	CK LOW to CS HIGH	8	-	ns
SID1514_3	t _{CSHCKH}	CS HIGH to CK HIGH	8	-	ns
SID1515_3	t _{DSLCSH}	DS LOW to CS HIGH	8	-	ns
SID1516_3	t _{CSHDST}	CS HIGH to DS High-Z	-	10	ns
SID1517_3	t _{CSLDSL}	CS LOW to DS LOW	0	-	ns
SID1518_3	t _{DSTCSL}	DS High-Z to CS LOW	0	-	ns

1) PLL#400, SSCG = 0, 小数分频器关闭

27 电气规范

表 62 xSPI (JEDEC JESD251) 延迟抽头推荐配置

Feature	xSPI200
	Rx
Delay tap selection (SMIF_DEVICE_DELAY_TAP_SEL/ DELAY_TAPS_NR_LOG2<7:0>)	6
Delay line selection (SMIF_CTL/DELAY_LINE_SEL<2:0>)	0

表 63 支持的输入、输出基准电压参考电平

Signal	Supported modes for voltage reference levels	
	CMOS	JEDEC
Clock	$V_T = (50\% \times V_{DDIO_HSIO})$	
RWDS(output)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO_HSIO}$
DQ[7:0] (output)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO_HSIO}$
RWDS(input)	$V_T = (50\% \times V_{DDIO_HSIO})$	
DQ[7:0] (input)	$V_T = (50\% \times V_{DDIO_HSIO})$	$V_{IH}/V_{IL} = 70\% / 30\% \times V_{DDIO_HSIO}$

注： 根据实际存储器的要求， 需要选择其中一种模式 ("CMOS"、"JEDEC") 。

- 某些参数可能是可用的， 并单独列出了各个模式的参数。 参数描述中会提到相应的模式。
- 没有明确模式描述的参数（例如 t_{OSU} ） 适用于所有模式， 但基准电压参考电平按照表格仍然适用。

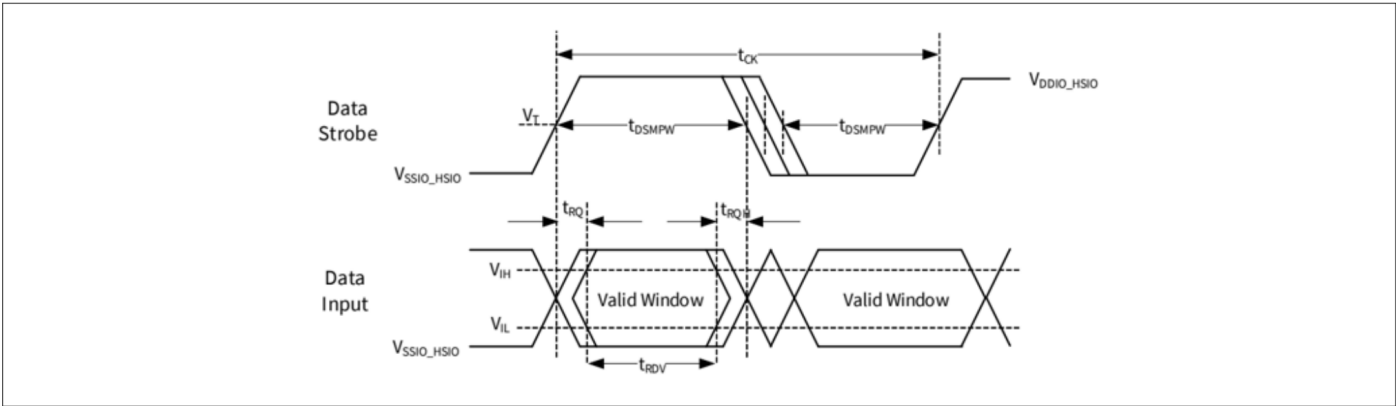


图 37 xSPI 主机数据输入时序基准电平（JEDEC）

27 电气规范

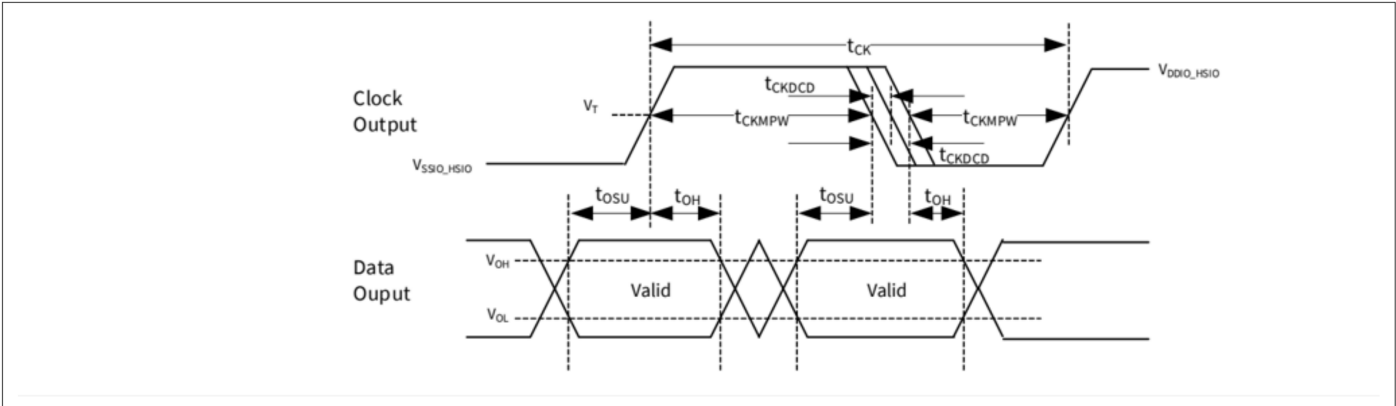


图 38 xSPI 主机数据输出时序基准电平（JEDEC）

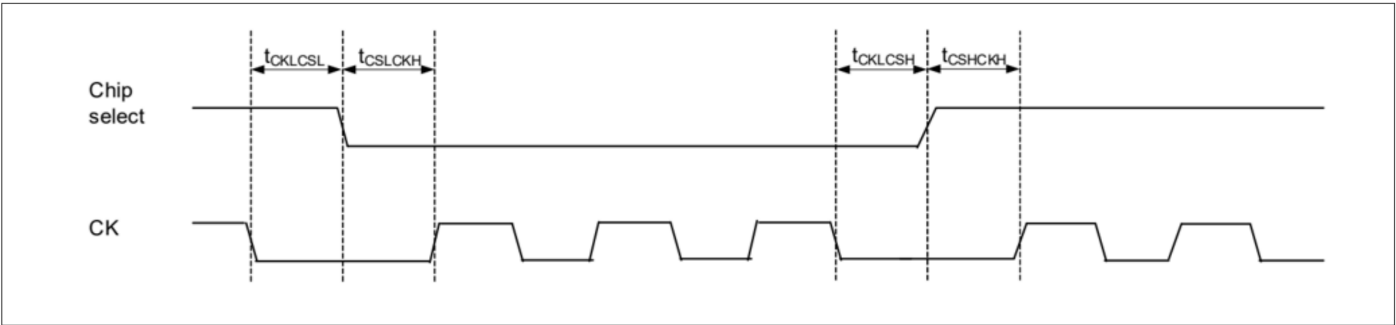


图 39 xSPI 时钟到片选时序图

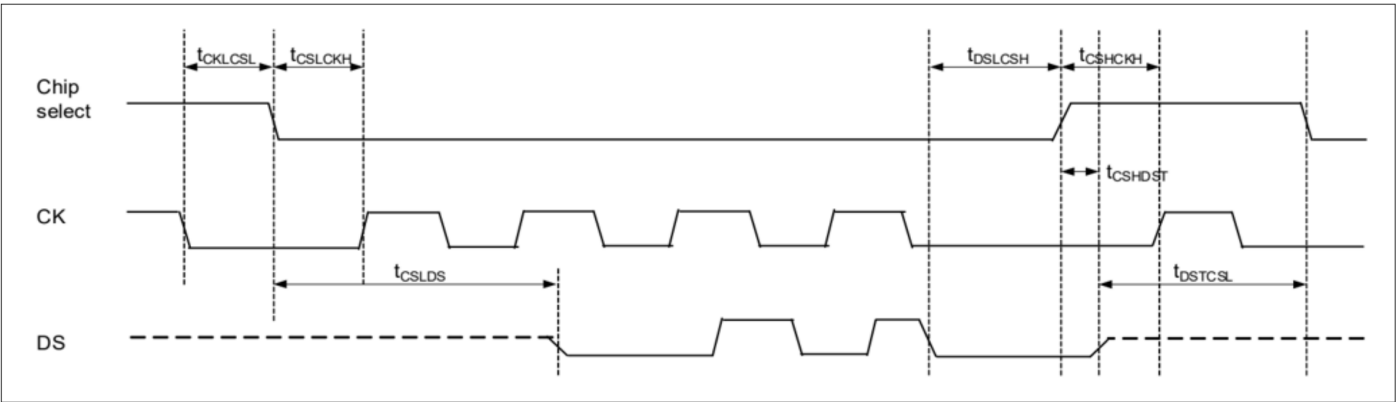


图 40 xSPI 数据选通与片选时序图

表 64 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
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Standard SPI SDR

建议 I/O 配置

HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0>= 0b0, CFG_SLEW_EXT/SLEW<2:0>= 0b000

接收器的 DLL Tap 设置:

SMIF_CTL/DELAY_LINE_SEL<2:0>= 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0>= 2

所有时序均与 $V_T = (50\% \times V_{DDIO_HSIO})$ 对齐。

(表格续下页.....)

27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1600_21)	t _{CK}	Interface clock period	10	–	–	ns	15-pF output loads, 3.3 V
SID1601	t _{CKPW}	Clock pulse width	$0.45 \times t_{CK}$	–	$0.55 \times t_{CK}$	ns	15-pF output loads
SID1602_HS	t _{CSS}	CS# active setup to CK (f _{CK} > 50 MHz)	4	–	–	ns	15-pF output loads, f _{CK} > 50 MHz Guaranteed by design
SID1602_LS	t _{CSS}	CS# active setup to CK (f _{CK} ≤ 50 MHz)	5	–	–	ns	15-pF output loads, f _{CK} ≤ 50 MHz Guaranteed by design
SID1603	t _{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1604	t _{CSH3}	CS# active hold to CK (mode 3)	6	–	–	ns	15-pF output loads Guaranteed by design
SID1605_2	t _{OSU}	Output setup time of DQ[7:0] to CK high (f _{CK} = 100 MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OSU} = t_{OSU_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t _{OSU_min} = value at MIN of SID1605_2 t _{CK_min} = value at MIN of SID1600_2 t _{CK} = actual clock period
SID1606_2	t _{OH}	Output hold time of DQ[7:0] to CK high (f _{CK} = 100 MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH_min} + 0.45 \times (t_{CK} - t_{CK_min})$ t _{OH_min} = value at MIN of SID1606_2 t _{CK_min} = value at MIN of SID1600_2 t _{CK} = actual clock period

(表格续下页.....)

27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1607	t _{IN_V}	CK low to DQ[7:0] input valid time	1	–	6.7	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b0 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0>=0b01 3) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b1 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0> needs to be adjusted based on INTR/DL_WARNING
SID1607A	t _{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/ bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1608	t _{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/ bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011

(表格续下页.....)

27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1609	t _{RDV}	Input data valid time of DQ[7:0]	3.8	–	–	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b0 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0>=0b01 3) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b1 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0> needs to be adjusted based on INTR/DL_WARNING
SID1610	t _{CS}	CS# HIGH time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1610A	t _{CS}	CS# HIGH time (Read when reset feature and quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1610B	t _{CS}	CS# High time (Program/Erase)	50	–	–	ns	15-pF output loads Guaranteed by design
SID1611	t _{DIS}	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1614	IN_SR	Input slew rate with respect to V _{IH} /V _{IL}	1.03	–	–	V/ns	–

Standard SPI DDR

(表格续下页...)

27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
建议 I/O 配置 HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> = 0b000 接收器的 DLL Tap 设置: SMIF_CTL/DELAY_LINE_SEL<2:0> = 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0> = 2 所有时序均与 $V_T = (50\% \times V_{DDIO_HSIO})$ 对齐。							
SID1700_2[70]	t _{CK}	Interface clock period	12.5	–	–	ns	15-pF output loads, 3.3 V
SID1701	t _{CKPW}	Clock pulse width	$0.45 \times t_{CK}$	–	$0.55 \times t_{CK}$	ns	15-pF output loads
SID1702_HS	t _{CSS}	CS# active setup to CK ($f_{CK} > 50$ MHz)	4	–	–	ns	15-pF output loads, $f_{CK} > 50$ MHz Guaranteed by design
SID1702_LS	t _{CSS}	CS# active setup to CK ($f_{CK} \leq 50$ MHz)	5	–	–	ns	15-pF output loads, $f_{CK} \leq 50$ MHz Guaranteed by design
SID1703	t _{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1705_2	t _{OSU}	Output setup time of DQ[7:0] to CK edge ($f_{CK} = 80$ MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OSU} = t_{OSU_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t_{OSU_min} = value at MIN of SID1705_2 t_{CK_min} = value at MIN of SID1700_2 t_{CK} = actual clock period
SID1706_2	t _{OH}	Output hold time of DQ[7:0] to CK edge ($f_{CK} = 80$ MHz)	1.6	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH_min} + 0.225 \times (t_{CK} - t_{CK_min})$ t_{OH_min} = value at MIN of SID1706_2 t_{CK_min} = value at MIN of SID1700_2 t_{CK} = actual clock period

(表格续下页.....)

27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1707	t _{IN_V}	CK edge to DQ[7:0] input valid time	1	–	6.7	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> >=0b0 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0>=0b01 3) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> >=0b1 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0> needs to be adjusted based on INTR/DL_WARNING
SID1707A	t _{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/ bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1708	t _{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/ bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011

(表格续下页.....)

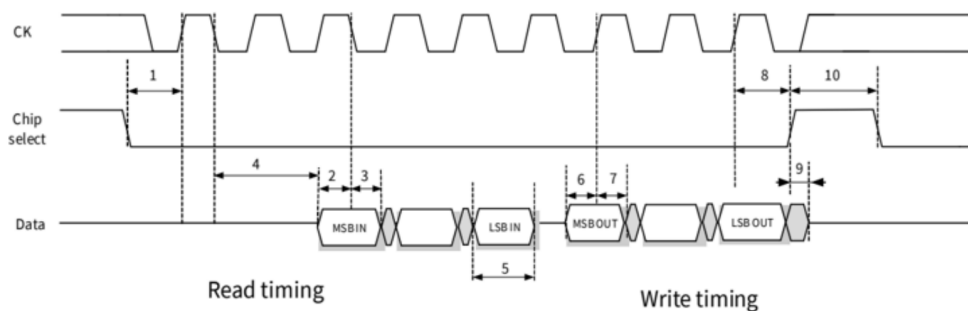
27 电气规范

表 64 (续) 标准 SPI 规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1709_2	trDV	Input data valid time of DQ[7:0] ($f_{CK} \leq 80$ MHz)	3.5	–	–	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b0 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0>=0b01 3) CTL/ CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/ INT_CLOCK_DL_ENABLED<0:0> = 0b1 CTL/ INT_CLOCK_CAPTURE_CYCLE <1:0> needs to be adjusted based on INTR/DL_WARNING
SID1710	tcs	CS# High time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1710A	tcs	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1710B	tcs	CS# High time (Program/Erase)	50	–	–	ns	15-pF output loads Guaranteed by design
SID1711	tdIS	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1714	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.03	–	–	V/ns	–

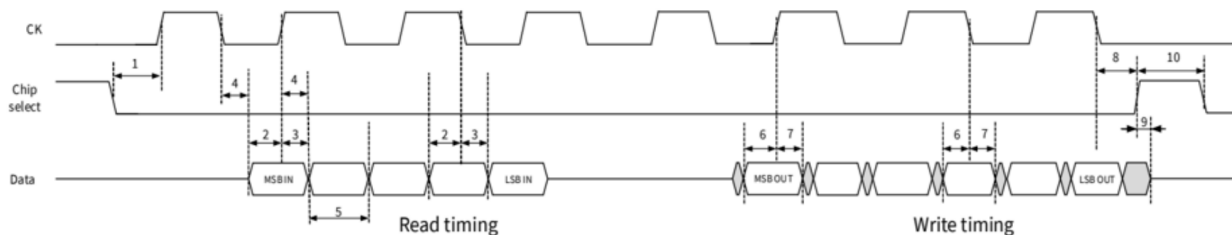
1) 确保将 PLL#400 明确配置为整数模式，设置 "SSCG = OFF"，"Fractional = OFF"。

27 电气规范



- 1: CS# active setup to CK = t_{CSS}
- 2: Data setup time = t_{ISU}
- 3: Data hold time = t_{IH}
- 4: CK low to DQ[7:0] input valid time = t_{IN_V}
- 5: Read data valid time of DQ[7:0] = t_{RDV}
- 6: Output setup of DQ[7:0] to CK rise = t_{OSU}
- 7: Output hold time of DQ[7:0] from CK rise = t_{OH}
- 8: CS# active hold to CK = t_{CSH}
- 9: CS# inactive to output disable = t_{DIS}
- 10: Chip select HIGH time = t_{CS}

图 41 SDR 写入和读取时序图



- 1: CS# active setup time to CK = t_{CSS}
- 2: Data setup time = t_{ISU}
- 3: Data hold time = t_{IH}
- 4: CK edge low to DQ[7:0] input valid time = t_{IN_V}
- 5: Read data valid time of DQ[7:0] = t_{RDV}
- 6: Output setup time of DQ[7:0] to CK edge = t_{OSU}
- 7: Output hold time of DQ[7:0] from CK edge = t_{OH}
- 8: CS# active hold time to CK = t_{CSH}
- 9: CS# inactive to output disable time = t_{DIS}
- 10: CS# HIGH time = t_{CS}

图 42 DDR 写入和读取时序图

27.16 LCD 控制器规格

表 65 LCD 控制器规格

Spec ID	Parameter	Description	Min.	Typ.	Max.	Units	Details/conditions
SID1243	f _{LCD_FR}	LCD frame rate	10	-	150	Hz	

28 订购信息

28 订购信息

CYT2CL 微控制器料号和特性列于表 66 中。Arm® TAP JTAG ID 为 0x6BA0 0477。

28 订购信息

表 66 CYT2CL 订购信息 ¹⁾

Product	Ordering code	Package	Code-flash (KB)	Work-flash (KB)	SRAM (KB)	ADC Channels	SCB Channels	LIN Channels	CANFD Channels	CXPI Channels	LCD	SMIF	Mixer	PCM-PWM	TDM	AUTOSAR package	Temperature Grade	JTAG IDCODE
CYT2CL7B AS	CYT2CL7BAAQ0AZ SGS	144-LQFP ₂ ²⁾	416 ₀₃₎	128 ₄₎	51 ₂	48	12	2	4	2	32 S x 4 C ₅₎	1x	1x	1x	2x	No	S ₆₎	0x1EC03069 ⁷⁾
CYT2CL8B XS	CYT2CL8BXAQ0AZ SGS	144-LQFP ₂ ²⁾	416 ₀₃₎	128 ₄₎	51 ₂	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	Yes	S	0x1EC03069
CYT2CLHB AS	CYT2CLHBAAQ0AZ SGS	144-LQFP ₈ ²⁾	416 ₀	128	51 ₂	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	No	S	0x1EC05069
CYT2CL7B XS	CYT2CL7BXAQ0AZ SGS	144-LQFP ₈ ²⁾	416 ₀	128	51 ₂	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	Yes	S	0x1EC05069
CYT2CL8B AS	CYT2CL8BAAQ0AZ SGS	176-LQFP	416 ₀	128	51 ₂	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	No	S	0x1EC01069
CYT2CLHB XS	CYT2CLHBXAQ0AZ SGS	176-LQFP	416 ₀	128	51 ₂	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	Yes	S	0x1EC01069

- 1) 支持的装运类型为“托盘”（默认）和“卷带包装”。在末尾添加字符‘T’，获取“卷带包装”装运类型的订购代码。
- 2) 封装引脚间距为 0.5 mm。
- 3) 代码闪存大小 4160 KB = 32 KB × 126 (大扇区) + 8 KB × 16 (小扇区)。
- 4) 工作闪存大小 128 KB = 2 KB × 48 (大扇区) + 128 B × 256 (小扇区)。
- 5) 32 个段和 4 个公共端。
- 6) S 级温度 (-40°C至105°C)。
- 7) JTAG ID CODE 位 12 至 27 代表器件的硅片 ID。
- 8) 封装引脚间距为 0.4 mm。

28 订购信息

28.1 器件型号命名规则

表 67 器件代码命名规则

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family	2	TRAVEO™ T2G (Core M4)
B	Application	C	Cluster Entry
D	Code-flash/Work-flash/ SRAM quantity	L	4160 KB/128 KB/512 KB
P	Packages	8	176-LQFP
		7	144-LQFP (0.5 mm Pitch)
		H	144-LQFP (0.4 mm Pitch)
H	Hardware option	B	Security on (HSM), RSA-3072
I	Marketing option	A	No options
		X	AUTOSAR package
C	Temperature grade	S	S-grade (-40°C to 105°C)

表 68 订购代码命名规则

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family name	2	TRAVEO™ T2G (Core M4)
B	Application	C	Cluster Entry
D	Code-flash/Work-flash/ SRAM quantity	L	4160 KB/128 KB/512 KB
P	Packages	8	176-LQFP
		7	144-LQFP (0.5 mm Pitch)
H	Hardware option	B	Security on (HSM), RSA-3072
I	Marketing option	A	No options
		X	AUTOSAR package
R	Revision	A	First revision
F	Fab location	Q	UMC(Fab 12i) Singapore
X	Reserved	0	Reserved
K	Package code	AZ	LQFP
C	Temperature grade	S	S-grade (-40°C to 105°C)
Q	Quality grade	ES	Engineering samples

(表格续下页.....)



28 订购信息

表 68 (续) 订购代码命名规则

Field	Description	Value	Meaning
		GS	Standard grade of automotive
S	Shipment type	Blank	Tray shipment
		T	Tape and reel shipment

29 封装

29 封装

CYT2CL 提供以下封装，详见表 69。

表 69 封装信息

Package	Dimensions ¹⁾	Contact/lead pitch	Coefficient of thermal expansion ²⁾	I/O pins
176-LQFP	24 × 24 × 1.7 mm(max)	0.5 mm	a1 ³⁾ = 8.5 ppm/°C, a2 ⁴⁾ = 33.8 ppm/°C	140
144-LQFP	20 × 20 × 1.7 mm(max)	0.5 mm	a1 ³⁾ = 8.5 ppm/°C, a2 ⁴⁾ = 33.7 ppm/°C	108
144-LQFP	16 × 16 × 1.7 mm(max)	0.4 mm	a1 ³⁾ = 8.5 ppm/°C, a2 ⁴⁾ = 33.65 ppm/°C	108

1) 尺寸（第 2 列）适用于室温。

2) 这些数字仅为基于仿真的估计值，并且基于每种封装类型的单个物料清单组合。

3) a1 = 低于 T_g 的 CTE（热膨胀系数）值（ppm/°C）（T_g 是玻璃化转变温度，为 131°C）。

4) a2 = 高于 T_g 的 CTE 值（ppm/°C）。

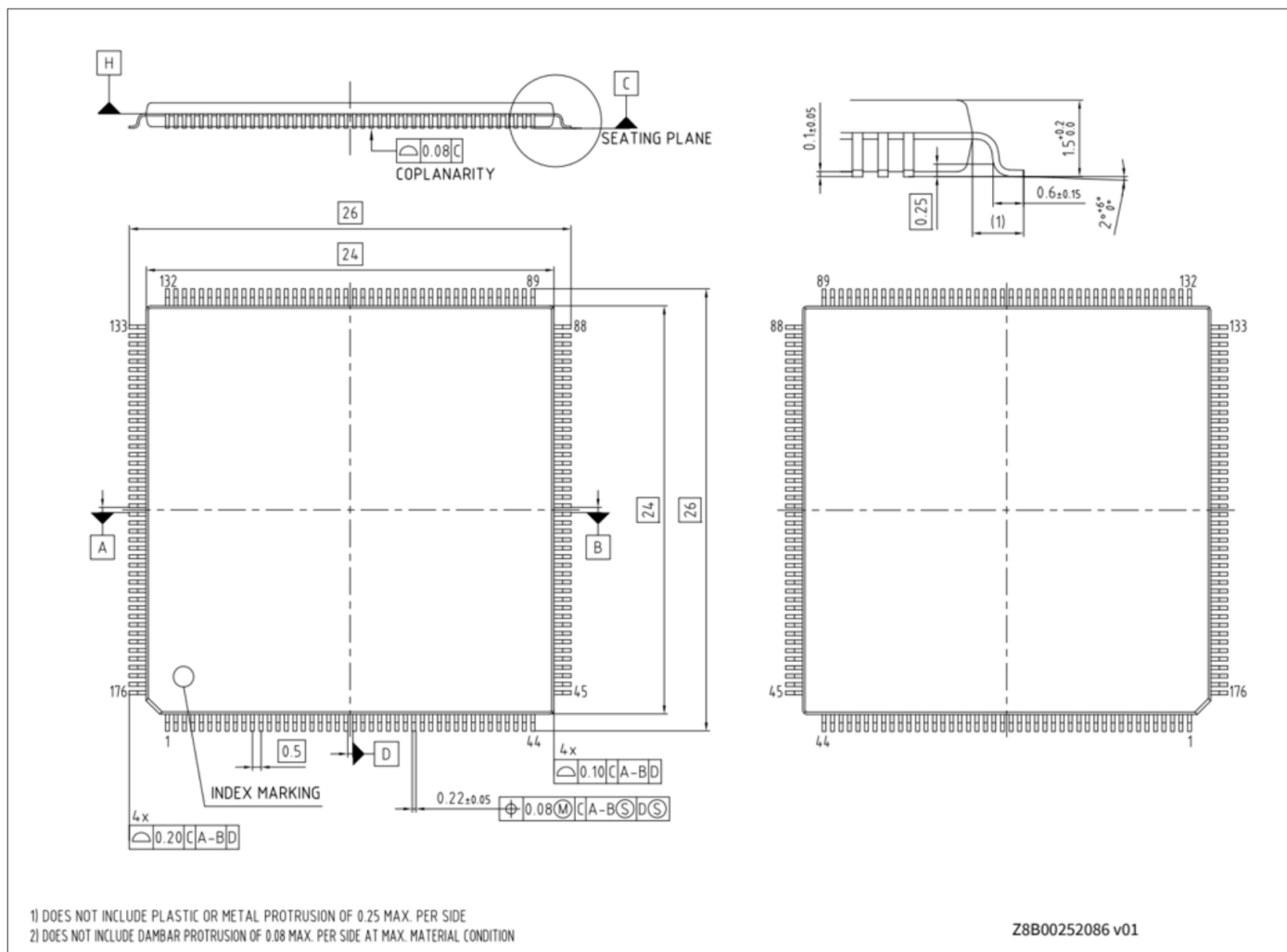
表 70 封装特性¹⁾

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T _A	Operating ambient temperature	S-grade	-40	-	105	°C
T _J	Operating junction temperature	-	-	-	150	°C
R _{θJA}	Package thermal resistance, junction to ambient θ _{JA} ²⁾	144 LQFP (0.4 mm)	-	-	23.0	°C/Watt
		144 LQFP (0.5 mm)	-	-	23.1	°C/Watt
		176 LQFP	-	-	21.8	°C/Watt
R _{θJB}	Package thermal resistance, junction to board θ _{JB}	144 LQFP (0.4 mm)	-	-	15.3	°C/Watt
		144 LQFP (0.5 mm)	-	-	15.0	°C/Watt
		176 LQFP	-	-	14.8	°C/Watt
R _{θJC}	Package thermal resistance, junction to case θ _{JC}	144 LQFP (0.4 mm)	-	-	5.2	°C/Watt
		144 LQFP (0.5 mm)	-	-	5.3	°C/Watt
		176 LQFP	-	-	4.5	°C/Watt

1) 电路板条件符合 JESD51-7（4 层）。

2) 尺寸（第 2 列）适用于室温。

Package	Maximum peak temperature (°C)	Maximum time at peak temperature (seconds)	MSL
144 LQFP (0.4 mm)	260	30	3
144 LQFP (0.5 mm)	260	30	3
176 LQFP	260	30	3



29 封装

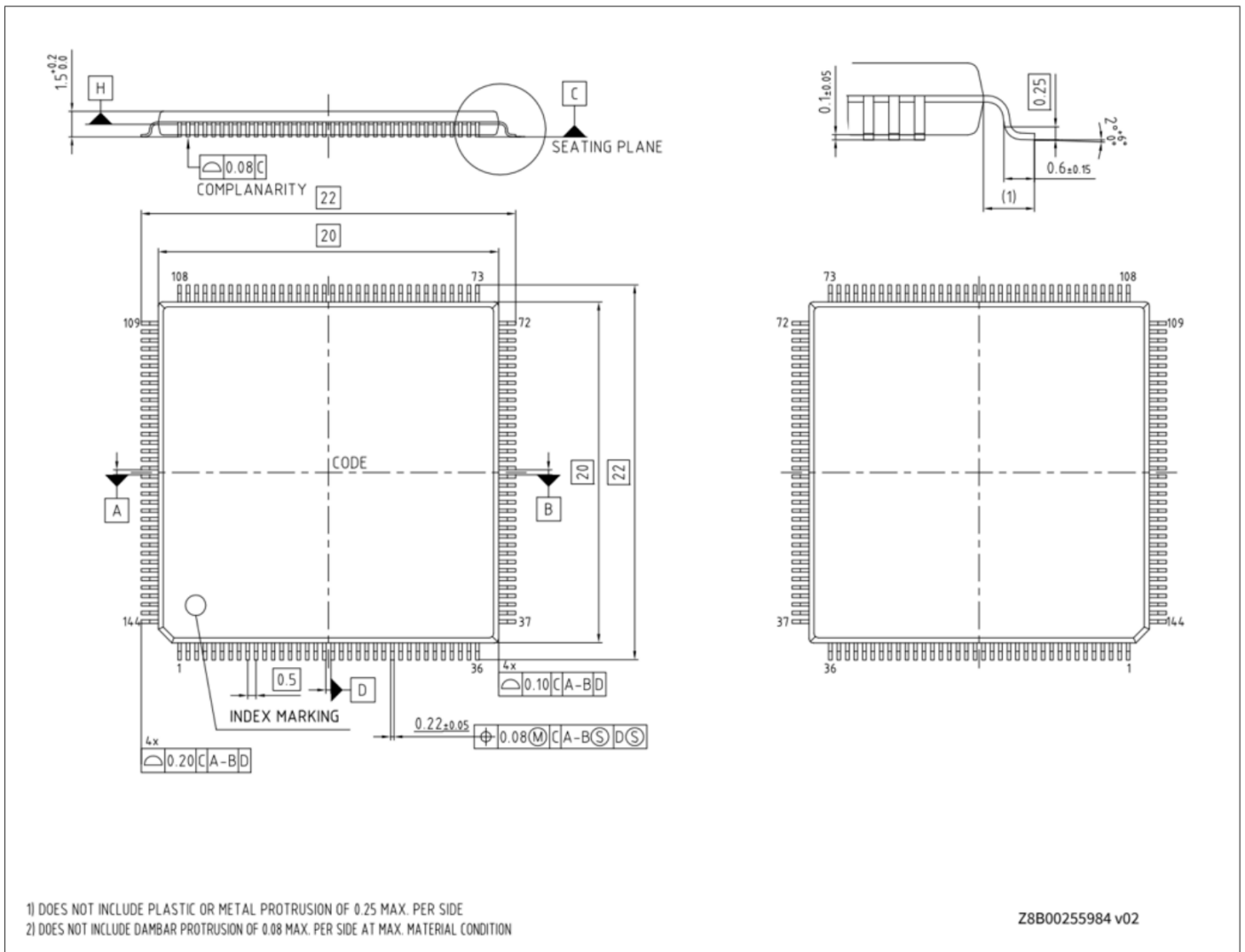
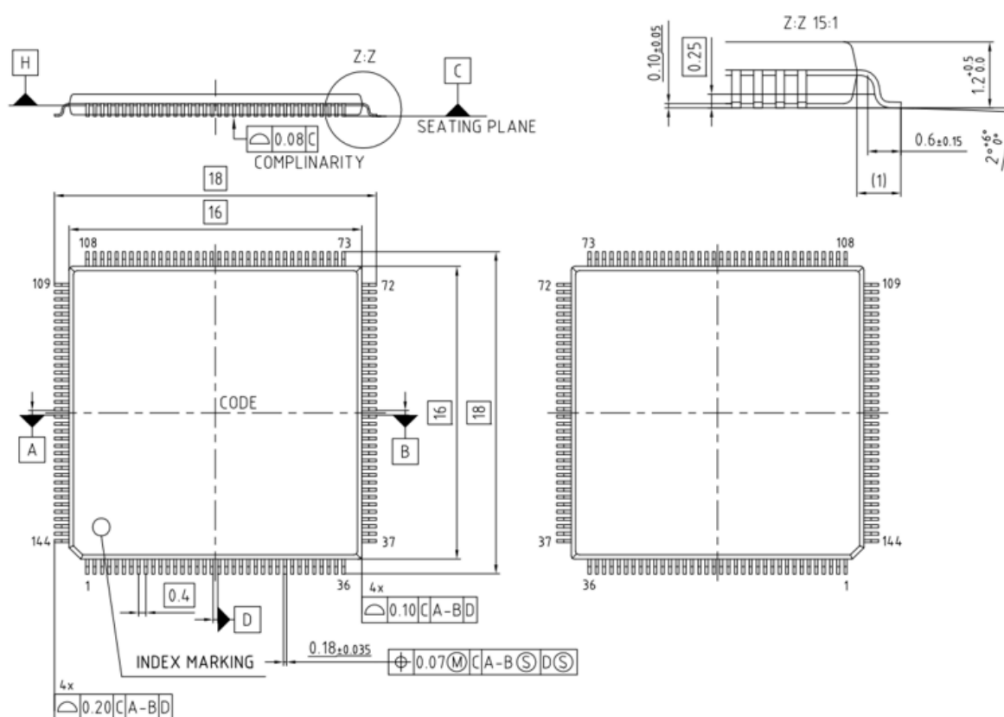


图 44 封装外形 - 144-LQFP (0.5 mm) (PG-LQFP-144)

29 封装



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.25 MAX. PER SIDE
2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.08 MAX. PER SIDE AT MAX. MATERIAL CONDITION

Z8B00255820 v01

图 45 封装外形 - 144-LQFP (0.4 mm) (PG-LQFP-144)

30 附录

30 附录

30.1 引导加载或生产线末端编程

- 如果满足触发条件，则在设备启动时触发
- 可以使用 CAN 或 LIN 通讯
- 引导加载程序在不同的时间帧上轮询 CAN 或 LIN 上的通讯，直到达到整体 300 秒超时
- 如果在任一通信接口上收到引导加载程序命令，则轮询停止，并且引导加载程序开始使用该接口

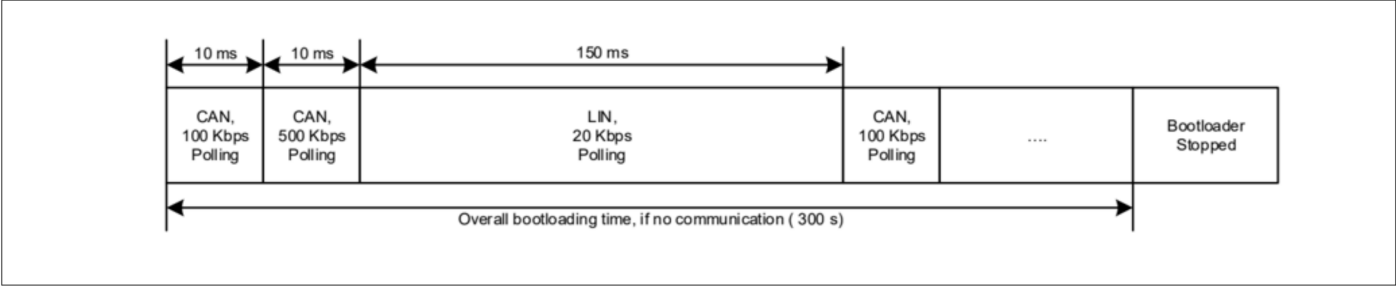


图 46 引导加载序列

表 72 CAN 接口详情

Sl. No.	CAN interface	Configuration
1	CAN Mode	Classic CAN
2	CAN Instance	CAN0, Channel#0
3	CAN TX	P18.2/CAN0_0_TX
4	CAN RX	P18.3/CAN0_0_RX
5	CAN Transceiver EN (High)	P19.2
6	CAN Transceiver EN (Low)	P19.3
7	CAN RX Message ID	0x1A1
8	CAN TX Message ID	0x1B1
9	Baud	100 or 500 kbps alternating

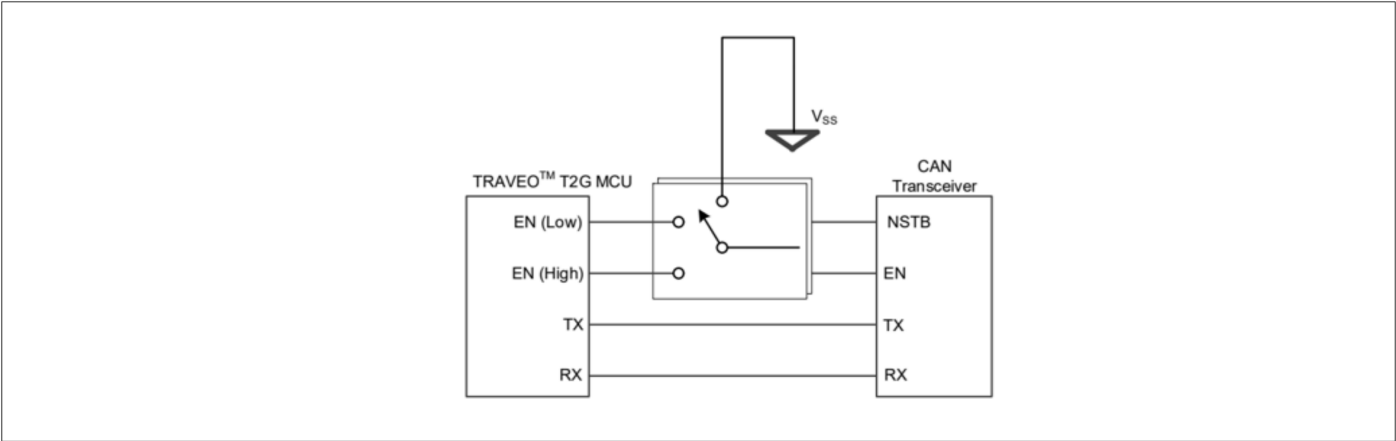


图 47 MCU 到 CAN 收发器的连接

表 73 LIN 接口详细信息

Sl. No.	LIN interface	Configuration
1	LIN type	LIN0, Channel#0
2	LIN mode	slave
3	LIN checksum type	Classic
4	LIN TX	P19.0/LIN0_0_TX
5	LIN RX	P19.1/LIN0_0_RX
6	LIN EN/EN (High)	P19.2
7	LIN EN (Low)	P19.3
8	LIN TX PID	0x46
9	LIN RX PID	0x45
10	Baud	20 or 115.2 kbps
11	Break field length	11
12	Break delimiter length	1 bit

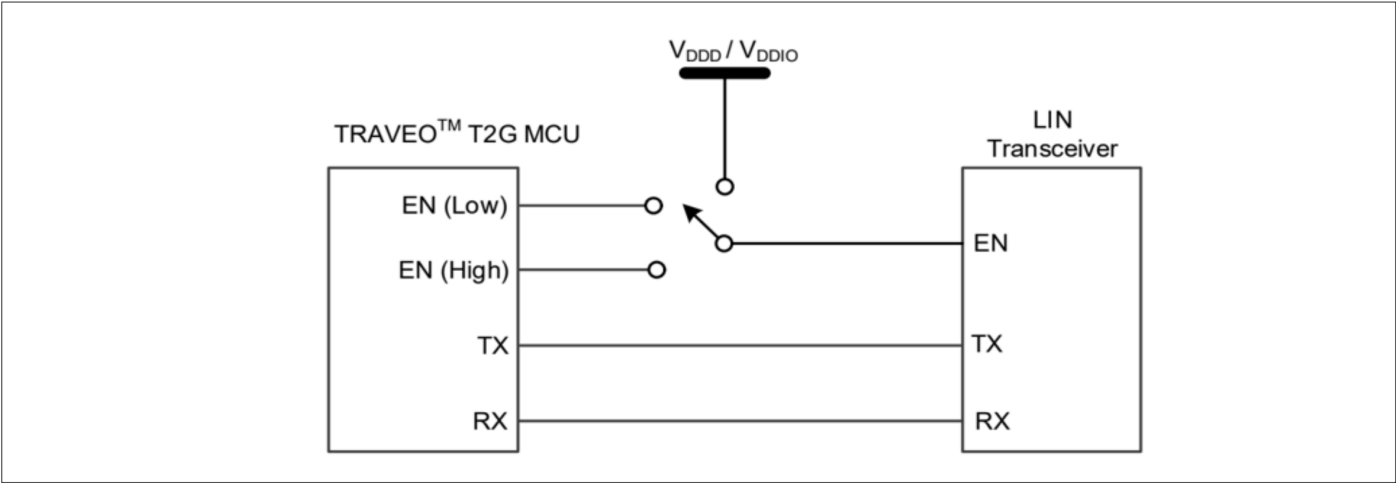


图 48 MCU 至 LIN 收发器连接

30.2 外部 IP 修订

表 74 外部 IP 修订

Module	IP	Revision	Vendor
CAN FD	mxttcanfd	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex®-M0+-r0p1	Arm®
Arm® Cortex®-M4F	armcm4	Cortex®-M4-r0p1	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100- r3p2	Arm®

30 附录

30.3 内部 IP 修订

表 75 表 30-4 内部 IP 修订

Module	Revision
SMIF	SMIF version 3.0 (Variant v3.1)

31 缩略语

31 缩略语

表 76 本文档中使用的缩略语

Acronym	Description	Acronym	Description
A/D	Analog to Digital	IRQ	Interrupt request
ABS	Absolute	JTAG	Joint test action group
ADC	Analog to Digital converter	LDO	Low drop out regulators
AES	Advanced encryption standard	LIN	Local Interconnect Network, a communications protocol
AHB	AMBA(advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus	LVD	Low voltage detection
Arm®	Advanced RISC machine, a CPU architecture	OTA	Over-the-air programming
ASIL	Automotive safety integrity level	OTP	One-time programmable
BOD	Brown-out detection	OVD	Overvoltage detection
CAN FD	Controller Area Network with Flexible Data rate	P-DMA	Peripheral-Direct Memory Access same as DW
CMOS	Complementary metal-oxide-semiconductor	PLL	Phase Locked Loop
CPU	Central Processing Unit	POR	Power-on reset
CRC	Cyclic redundancy check, an error-checking protocol	PPU	Peripheral protection unit
CSV	Clock supervisor	PRNG	Pseudorandom number generator
CTI	Cross trigger interface	PWM	Pulse-width modulation
CXPI	Clock Extension Peripheral Interface	MCU	Microcontroller Unit
DES	Data encryption standard	MCWDT	Multi-counter watchdog timer
DFT	Design-For-Test	M-DMA	Memory-Direct Memory Access
DW	Datwire same as P-DMA	MISO	SPI Master-in slave-out
ECC	Error correcting code/Elliptical curve cryptography	MMIO	Memory mapped I/O
ECO	External crystal oscillator	MOSI	SPI Master-out slave-in
ETM	Embedded Trace Macrocell	MPU	Memory protection unit
EVTGEN	Event Generator	MTB	Micro trace buffer
FLL	Frequency Locked Loop	MUL	Multiplier
FPU	Floating point unit	MUX	Multiplexer
GHS	Green Hills tool chain with Multi IDE	NVIC	Nested vectored interrupt controller
GPIO	General purpose input/output	RAM	Random access memory
HSM	Hardware security module	RISC	Reduced-instruction-set computing

(表格续下页.....)

31 缩略语

表 76 (续) 本文档中使用的缩略语

Acronym	Description	Acronym	Description
I/O	Input/output	ROM	Read only memory
I2C	Inter-Integrated Circuit, a communications protocol	RSA	Rivest-Shamir-Adleman Public Key Encryption Algorithm
ILO	Internal low-speed oscillator	RTC	Real-time clock
IMO	Internal main oscillator	SAR	Successive approximation register
IOSS	Input/output sub-system	SCB	Serial communication block
IPC	Inter-processor communication	SCL	I2C serial clock
IrDA	Infrared interface	SDA	I2C serial data
SECCED	Single error correction, double error detection	TCPWM	Timer/Counter Pulse-width modulator
SHA	Secure hash algorithm	TTL	Transistor-transistor logic
SHE	Secure hardware extension	TRNG	True random number generator
SMPU	Shared memory protection unit	UART	Universal Asynchronous Transmitter Receiver
SPI	Serial peripheral interface, a communications protocol	WCO	Watch crystal oscillator
SRAM	Static random access memory	WDT	Watchdog timer reset
SWD	Serial wire debug	XRES_L	External reset I/O pin
SWJ	Serial wire JTAG		

修订记录

修订记录

Document revision	Date of release	Description of changes
**	2018-03-05	New datasheet
*A	2018-07-20	Updated Features List and Functional Description. Updated Electrical Specifications. Updated Peripheral I/O Map and Pin Assignment. Added the following sections: trigger Multiplexer, triggers group Inputs, triggers group Outputs, triggers One To One. Updated Interrupts and Wake-up Assignments and Peripheral Clocks.
*B	2018-09-27	Updated Features. Minor corrections in Features List, Peripheral I/O Map. Updated Blocks and Functionality. Updated Functional Description. Updated trigger Multiplexer and Core Interrupt Types. Added General P-DMA descriptions, Clock Dividers, and GPIO power port source information. Updated Clock diagram Added HSIOM Connections Reference table and references to it in alternate pin assignment Updated Electrical Specifications. Added Errata.
*C	2019-05-15	Updated Features. Corrections and updates in Features List and Functional Description. Added group and slave details in Peripheral I/O Map. Corrected CAN MRAM size in Peripheral I/O Map. Added PPU Fixed Structure Pairs table with address and size details. Updated Miscellaneous Configuration with CM0+/CM4 MPU numbers supported. Updated Ordering Information and Packaging. Updated Clock Specifications (added Table 47). Added Appendix with Bootloading details.
**	2021-03-11	Minor corrections in Features List. Updated Peripheral I/O Map. Updated Electrical Specifications. Updated Errata.New datasheet

修订记录

Document revision	Date of release	Description of changes
*A	2021-05-13	Correction in the package dimensions for 144-LQFP (0.4 mm) Updated Features list. Corrected Power modes description. Updated Table 5. Added trigger MUX diagrams and subsequent tables in trigger multiplexer. Added Peripheral Protection Unit Fixed Structure Pairs Table in Peripheral protection unit fixed structure pairs. Updated Electrical specifications. Updated SCB/SPI Diagrams. Added “AC Specifications”. Added Table 44. Updated Table 69 and Figure 45 Added Table 75.
*B	2021-09-17	Renamed TRAVEO™ II to TRAVEO™ T2G. Updated Features list. Added Peripheral instance list. Updated Pin assignment diagrams. Updated Package pin list and alternate functions. Updated Alternate function pin assignments. Updated Pin function description. Updated Electrical specifications. Updated Packaging. Updated Package outline – 176-LQFP (PG-LQFP-176), Package outline – 144-LQFP (0.5 mm) (PG-LQFP-144), and Package outline – 144-LQFP (0.4 mm) (PG-LQFP-144) Updated CAN interface details, LIN interface details
*C	2022-07-15	Migrated to IFX template. Updated Features. Updated CPU subsystem, System resources, Peripherals, I/Os. Updated CYT2CL address map. Updated Alternate function pin assignments. Updated Interrupts and wake-up assignments. Updated Faults. Updated Electrical specifications. Updated Ordering information. Updated Errata.
*D	2022-09-15	Changed datasheet status to Final. Updated Electrical specifications.
*E	2022-10-07	Added note 84. Updated Errata.
*F	2022-10-20	Updated Ordering information.

修订记录

Document revision	Date of release	Description of changes
*G	2023-02-14	Updated Features list. Updated Peripheral I/O map. Updated Pin function description. Updated Electrical specifications. Updated Packaging.
*H	2023-05-19	Updated CYT2CL clock diagram. Updated Pin function description. Updated Electrical specifications. Updated Errata.
*I	2024-03-04	Updated Blocks and functionality. Updated Peripherals. Updated triggers one-to-one. Updated Electrical specifications. Updated Errata.
*J	2025-06-13	Updated PLL and FLL. Updated Table 28. Updated Table 31. Updated Table 64. Updated Table 34. Updated Table 56. Updated Packaging. Updated Figure 43. Updated Figure 44. Updated Figure 45. Removed Errata section.
*K	2026-06-18	Updated template. Updated footnote numbers. Updated General description Updated Features Updated Features list Updated Package pin list and alternate functions Updated Clock specifications Updated Ordering information Updated Part number nomenclature

修订记录变更日志

修订记录变更日志

表 77 Rev. *K 章节更新

Section	Change description	Current Spec (002-32508 Rev. *J)	New Spec (002-32508 Rev. *K)	Reason for change
General description	Added description	None	Infineon TRAVEO™ T2G 32-bit Automotive MCU is a high-performance, low-power controller designed for automotive applications, compliant to ISO 26262 for functional safety and ISO 21434 for cybersecurity.	Addition
Features	Updated description	Crypto engine	ISO 21434 compliant/EVITA Full	Updated
Features	Updated description	Functional safety for ASIL-B	ISO 26262 functional safety compliant for ASIL-B	Updated
Features list	Updated description	Functional safety ASIL-B	Functional safety ISO 26262 ASIL-B compliant	Updated
Features list	Updated description	Security	Security - ISO 21434 compliant	Updated
Package pin list and alternate functions	Table 14: Added +B input column	None	+B input column	Addition
Clock specifications	Updated description for Note for ECO connection scheme	65. See the family-specific Architecture TRM for more information on crystal requirements (002-33175, TRAVEO™ T2G Automotive MCU cluster entry architecture technical reference manual).	17. See the family-specific Architecture TRM for more information on crystal requirements (002-33175, TRAVEO™ T2G Automotive MCU cluster entry architecture technical reference manual). Before enable ECO the TRIM registers shall be configured with correct settings (ATRIM, WDTRIM, FTRIM, GTRIM and RTRIM) based on and User Guide "Setting ECO parameters, TRAVEO™ T2G family" (Doc No. 002-30194) and crystal matching test at crystal vendor.	Updated
Ordering information	Table 66: Added three new device codes, added AUTOSAR package column	None	Added three new device codes CYT2CL8BXS, CYT2CL7BXS, CYT2CLHBXS Added AUTOSAR package column	Addition
Part number nomenclature	Table 67: Updated Marketing option	None	X AUTOSAR package	Updated
Part number nomenclature	Table 68: Updated Marketing option	None	X AUTOSAR package	Updated

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