英飞凌TRAVEO™ T2G 32 位汽车类 MCU

基于Arm® Cortex®-M4F-single

概述

英飞凌 TRAVEO™ T2G 32 位汽车MCU是一款高性能、低功耗控制器，专为汽车应用而设计，符合 ISO 26262 功能安全标准和 ISO 21434 网络安全标准。CYT2BL 是 TRAVEO™ T2G 微控制器系列，针对车身控制单元等汽车系统。CYT2BL 采用 Arm® Cortex®-M4F CPU 用于主处理，并配备 Arm® Cortex®-M0+ CPU 用于外设和安全处理。这些器件包含支持具有灵活数据传输速率的控制器局域网（CAN FD）、本地互连网络（LIN）、时钟扩展外设接口（CXPI）、LCD 控制器的嵌入式外设。TRAVEO™ T2G 器件采用先进的 40 纳米工艺制造。CYT2BL 集成低功耗闪存、多种高性能模拟和数字外设，并支持创建安全的计算平台。

特性

- **双 CPU 子系统**
  - 160 MHz（最大）32 位 Arm® Cortex®-M4F CPU，带有
    - 单周期乘法
    - 单精度浮点单元（FPU）
    - 存储器保护单元（MPU）
  - 100 MHz（最大）32 位 Arm® Cortex®-M0+ CPU，带有
    - 单周期乘法
    - 存储器保护单元
  - 处理器之间硬件通信单元
  - 三个 DMA 控制器
    - 外设 DMA 控制器 #0 (P-DMA0) 带有 92个通道
    - 外设 DMA 控制器 #1 (P-DMA1) 带有 44 个通道
    - 内存 DMA 控制器 (M-DMA0) 带有 4 个通道
- **集成存储器**
  - 4160 KB 代码闪存，另加 128 KB 工作闪存
    - 边读边写（RWW）允许在执行代码时对代码闪存/工作闪存进行更新
    - 单组和双组模式（专门用于无线固件更新 [FOTA]）
    - 通过 SWD/JTAG 接口对闪存进行编程
  - 512 KB SRAM，具有可选保留粒度
- **符合 ISO 21434 标准/EVITA Full**[1)]
  - 支持增强型安全硬件扩展 (eSHE) 和硬件安全模块 (HSM)
  - 安全启动和身份验证
    - 使用数字签名验证
    - 使用快速安全启动

  -AES：128 位块，128/192/256 位密钥
  - 3DES[2)]: 64 位块，64 位密钥
  - 向量单元[2)] 支持非对称密钥加密算法（如 Rivest-Shamir-Adleman (RSA) 和 Elliptic Curve (ECC)）
  - SHA-1/2/3[2)]: SHA-512, SHA-256, SHA-160，可变长度输入数据
  - CRC[2)]：支持 CCITT CRC16 和 IEEE-802.3 CRC32

1 部分 MPN 具有加密引擎功能。
2 此功能不适用于 "仅限 eSHE "部件。更多信息，请参阅订购信息。

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

  - 真随机数生成器（TRNG）和伪随机数生成器（PRNG）
  - 伽罗瓦/计数器模式（GCM）
- **符合 ISO 26262 功能安全标准，达到 ASIL-B 等级**
  - 存储器保护单元（MPU）
  - 共享存储器保护单元（SMPU）
  - 外设保护单元（PPU）
  - 看门狗计时器（WDT）
  - 多计数器看门狗定时器（MCWDT）
  - 低电压检测器（LVD）
  - 欠压检测器（BOD）
  - 过压检测（OVD）
  - 时钟监视器（CSV）
  - 硬件纠错（SECDED ECC）在所有安全关键存储器（SRAM、闪存）
- **低功耗 2.7 V 至 5.5 V 操作**
  - 低功耗运行、睡眠、低功耗睡眠、深度睡眠和休眠模式，可实现精细的电源管理
  - 可配置选项以实现稳健的电压欠压检测（BOD）
    - 两个阈值电平（2.7 V 和 3.0 V）用于 BOD 在 V_{DDD} 和 V_{DDA}
    - 一个阈值电平（1.1 V）用于 BOD 在 V_{CCD}
- **唤醒支持**
  - 最多两个引脚可唤醒休眠模式
  - 最多 152 个 GPIO 引脚可唤醒睡眠模式
  - 事件发生器、SCB、看门狗计时器、RTC 警报可从深度睡眠模式中唤醒
- **时钟源**
  - 内部主振荡器（IMO）
  - 内部低速振荡器（ILO）
  - 外部晶体振荡器（ECO）
  - 时钟晶体振荡器（WCO）
  - 锁相环（PLL）
  - 锁频环（FLL）
- **通信接口**
  - 最多八个 CAN FD 通道
    - 与传统 CAN 相比，数据速率有所提高（高达 8 Mbps），但受物理层拓扑和收发器的限制
    - 符合 ISO 11898-1:2015 标准
    - 支持 Bosch CAN FD 规范 V1.0 对非 ISO CAN FD 的所有要求
    - ISO 16845:2015 证书可用
  - 多达 8 个运行时可配置的串行通讯功能块（SCB）通道，每个功能块可配置为 I^2C、SPI、或 UART
  - 最多 12 个独立 LIN 通道
    - LIN 协议符合 ISO 17987 标准
  - 多达 4 个 CXPI 通道，数据传输速率高达 20 kbps
- **定时器**
  - 最多 75 个 16 位和 8 个 32 位定时器/计数器脉宽调制器 (TCPWM) 模块
    - 最多 12 个 16 位计数器用于电机控制

Features

  - 最多 63 个 16 位计数器和8个 32 位计数器用于常规操作
  - 支持定时器、捕获、正交解码、脉冲宽度调制 (PWM)、带死区时间的 PWM (PWM_DT)、伪随机 PWM (PWM_PR) 和移位寄存器 (SR) 模式
- 最多 11 个事件生成（EVTGEN）定时器，支持从深度睡眠模式循环唤醒
  - 事件触发特定的设备操作（例如执行中断处理程序、SAR ADC 转换等）

- **实时时钟（RTC）**
  - 年/月/日、星期、小时：分钟：秒字段
  - 支持 12 小时和 24 小时制
  - 自动闰年校正
- **I/O**
  - 最多 152 个可编程 I/O
  - 两种 I/O 类型
    - GPIO 标准（GPIO_STD）
    - GPIO 增强（GPIO_ENH）
- **稳压器**
  - 支持 2.7 V 至 5.5 V 输入电压生成 1.1 V 内核电压
  - 稳压器的两种类型
    - 深度睡眠
    - 核心内部
- 可编程的模拟资源
  - 三个 SAR A/D 转换器，最多具有 67 个外部通道（64 个 I/O + 3 个用于电机控制的 I/O）
    - ADC0 支持 24 个逻辑通道，有 24 + 1 个物理连接
    - ADC1 支持 32 个逻辑通道，有 32 + 1 个物理连接
    - ADC2 支持 8 个逻辑通道，有 8 + 1 个物理连接
    - 任何外部通道都可以连接到相应 SAR 中的任何逻辑通道
  - 每个 ADC 支持 12 位分辨率和高达 1 Msps 的采样率
  - 每个 ADC 还支持最多 6 个内部模拟输入，如
    - 带隙基准电压源用于提供绝对电压值
    - 用于结温计算的校准二极管
    - 两个 AMUXBUS 输入和两个用于监测电源电平的直接连接
  - 每个 ADC 支持外部多路复用器的寻址
  - 每个 ADC 都有一个序列器，支持对已配置通道进行自主扫描
  - 针对电机感应应用的所有 ADC 的同步采样
- **智能 I/O**
  - 最多5个智能 I/O 模块，可对进出 I/O 的信号执行布尔运算
  - 支持最多 36 个 I/O (GPIO_STD)
- **调试接口**
  - 符合 IEEE-1149.1-2001 的 JTAG 控制器和接口
  - Arm®串行线调试（ SWD ）端口
  - 支持 Arm® 嵌入式跟踪宏单元（ETM）
    - 使用 SWD 进行数据跟踪
    - 使用 JTAG 进行指令和数据跟踪
- **与行业标准工具兼容**
  - GHS/MULTI 或 IAR EWARM 用于代码开发和调试
- **封装**
  - 64-LQFP，10 × 10 × 1.7 毫米（最大），0.5 毫米引脚间距

- 80-LQFP，12×12×1.7 毫米（最大），0.5 毫米引脚间距
- 100-LQFP，14×14×1.7 毫米（最大），0.5 毫米引脚间距
- 144-LQFP，20×20×1.7 毫米（最大），0.5 毫米引脚间距
- 176-LQFP，24×24×1.7 毫米（最大），0.5 毫米引脚间距

• **认证**

- 符合 AEC-Q100 的汽车应用要求

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1 特性列表

表 1 CYT2BL 所有封装特性列表

Features	Package				
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP
CPU					
Core	32-bit Arm® Cortex®-M4F CPU and 32-bit Arm® Cortex®-M0+ CPU				
Functional safety	ISO 26262 ASIL-B compliant				
Operating voltage	2.7 V to 5.5 V				
Core voltage	1.05 V to 1.15 V				
Operating frequency	Arm® Cortex®-M4F 160 MHz (max) and Arm® Cortex®-M0+ 100 MHz (max), related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on)				
MPU, PPU	Supported				
FPU	Single precision (32-bit)				
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M4F CPU				
存储器					
Code flash	4160 KB (4032 KB + 128 KB)				
Work flash	128 KB (96 KB + 32 KB)				
SRAM (configurable for retention)	512KB				
ROM	32 KB				
通信接口					
CAN0 (CAN FD: Up to 8 Mbps)	3 ch		4 ch		
CAN1 (CAN FD: Up to 8 Mbps)	2 ch	4 ch			
CAN RAM	32 KB per instance (4 ch), 64 KB in total				
Serial communication block (SCB/UART)	7 ch	8 ch			
Serial communication block (SCB/I^2C)	6 ch		8 ch		
Serial communication block (SCB/SPI)	3 ch	6 ch	8 ch		
LIN0	7 ch	9 ch		12 ch	
CXPI Controller	2 ch	3 ch	4 ch		
定时器					
RTC	1 ch				
TCPWM (16-bit) (Motor control)	12 ch				
TCPWM (16-bit)	63 ch				
TCPWM (32-bit)	8 ch				

（表格续下页……）

1 Feature list

表 1 （续） CYT2BL 所有封装特性列表

Features	Package				
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP
External Interrupts	49	63	78	122	152
模拟模块					
12-bit, 1 Msps SAR ADC	3 Units (SAR0/24, SAR1/32, SAR2/8 logical channels)				
	27 external channels (SAR0 11 ch, SAR1 9 ch, SAR2 7 ch)	34 external channels (SAR0 12 ch, SAR1 14 ch, SAR2 8 ch)	39 external channels (SAR0 14 ch, SAR1 17 ch, SAR2 8 ch)	54 external channels (SAR0 21 ch, SAR1 25 ch, SAR2 8 ch)	64 external channels (SAR0 24 ch, SAR1 32 ch, SAR2 8 ch)
	18 ch (6 per ADC) Internal sampling				
Motor control input	3 ch (synchronous sampling of one channel on each of the 3 ADCs)				
安全 – 符合 ISO 21434 标准					
Flash security (program/work read protection)	Supported				
Flash Chip erase enable	Configurable				
eSHE/HSM	By separate firmware[1)]				
系统					
DMA controller	P-DMA0 with 92 channels (16 general purpose), P-DMA1 with 44 channels (8 general purpose), and M-DMA0 with 4 channels				
Internal main oscillator	8 MHz				
Internal low-speed oscillator	32.768 kHz (nominal)				
PLL	Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 160 MHz				
FLL	Input frequency: 0.25 to 80 MHz, FLL output frequency: up to 100 MHz				
Watchdog timer and multi-counter Watchdog timer	Supported (WDT + 2× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM4				
Clock supervisor	Supported				
Cyclic wakeup	Supported				
GPIO_STD	45	59	74	118	148
GPIO_ENH	4				
Smart I/O (Blocks)	3 blocks, 9 I/Os	3 blocks, 14 I/Os	4 blocks, 20 I/Os	5 blocks, 29 I/Os	5 blocks, 36 I/Os
Low-voltage detect	Two, 26 selectable levels				
Maximum ambient temperature	105°C for S-grade and 125°C for E-grade				
Debug interface	SWD/JTAG				
Debug trace	Arm® Cortex®-M4F ETB size of 8 KB, Arm® Cortex® M0+ MTB size of 4 KB				

1) 增强安全硬件扩展（eSHE）和硬件安全模块（HSM）支持由第三方固件实现。

1.1 通信外设实例列表

下表列出了通讯外设在每个封装下支持的实例，根据实现功能所需的最少引脚数。

表 2 外设实例列表

Module	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP	Minimum pin functions
CXPI	0/1	0/1/2	0/1/2/3	0/1/2/3	0/1/2/3	TX, RX
CAN0	0/1/2	0/1/2	0/1/2/3	0/1/2/3	0/1/2/3	TX, RX
CAN1	0/2	0/1/2/3	0/1/2/3	0/1/2/3	0/1/2/3	TX, RX
LIN0	0/1/2/3/4/7/9	0/1/2/3/4/6/7/8/9	0/1/2/3/4/6/7/8/9	0/1/2/3/4/5/6/7/8/9/10/11	0/1/2/3/4/5/6/7/8/9/10/11	TX, RX
SCB/UART	0/1/2/3/4/5/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	TX, RX
SCB/I^2C	0/2/3/4/5/7	0/1/3/4/5/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	SCL, SDA
SCB/SPI	0/3/4	0/1/3/4/5/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	0/1/2/3/4/5/6/7	MISO, MOSI, SCK, SELECT0

2 模块和功能

2.1 框图

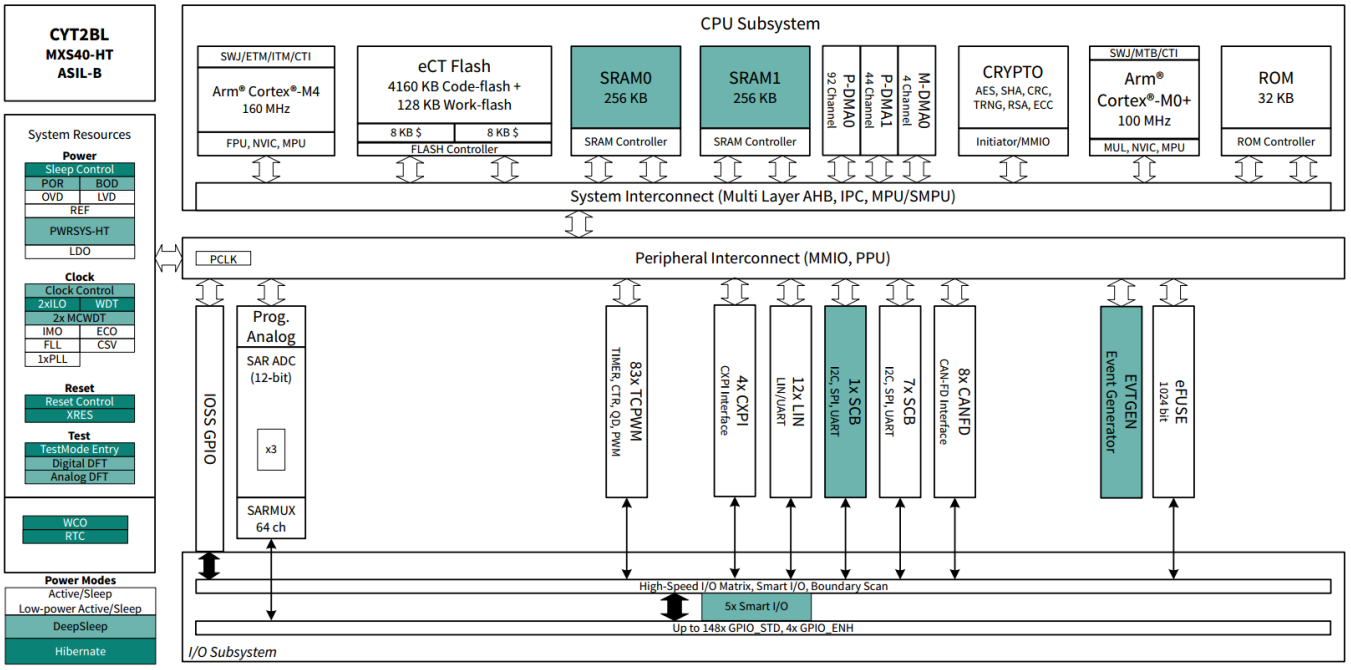

图 1 框图

图1显示了 CYT2BL 架构，其中给出了子系统和模块之间互连的简化视图。CYT2BL 有四个主要子系统：CPU、系统资源、外设和 I/O[3], [4]。颜色编码显示最低功率模式，其中特定功能块仍然起作用。

CYT2BL 广泛支持硬件和固件的编程、测试、调试和跟踪。

片上调试功能支持使用生产器件进行系统调试。它不需要特殊的接口、调试转接板、模拟器或仿真器。

JTAG 接口与 I-jet、J-Link 和 GHS 等行业标准的第三方探测器完全兼容。调试电路默认启用。

CYT2BL 提供高级的安全性，具有强大的闪存保护以及调试等禁用功能。

此外，如果某些应用担心网络钓鱼攻击会通过对器件恶意重新编程或试图启动和中断闪存编程序列来击败安全设定，所有器件接口都可以被永久禁用。当器件的最大安全级别被使能时，将禁用所有编程、调试和测试接口。

3 GPIO_STD 支持 2.7 V 至 5.5 V V_{DDIO} 范围。
4 GPIO_ENH 支持 2.7 V 至 5.5 V V_{DDIO} 范围，在较低电压下具有较高的电流。

3 功能描述

3.1 CPU 子系统

3.1.1 CPU

CYT2BL CPU 子系统包含一个 32 位 Arm® Cortex®-M0+ CPU（带 MPU）、一个 32 位 Arm® Cortex®-M4F CPU（带MPU）和单精度 FPU。该子系统还包括 P-/M-DMA 控制器、加密加速器、4160 KB 的代码闪存、128 KB 的工作闪存、512 KB 的 SRAM 和 32 KB 的 ROM。

Cortex®-M0+ CPU 提供了安全、不可中断的启动功能。这保证了启动功能完成后，系统完整性有效且权限得到强制执行。共享资源（闪存、SRAM、外设等）可以通过总线仲裁进行访问，并且使用硬件信号量的处理器间通讯（IPC）机制来支持独占访问。

3.1.2 DMA 控制器

CYT2BL 有三个 DMA 控制器：具有 16 个通用通道和 76 个专用通道的 P-DMA0、具有 8 个通用通道和 36 个专用通道的 P-DMA1 以及具有 4 个通道的 M-DMA0。P-DMA 用于外设到存储器和存储器到外设的数据传输，并为大量通道提供低延迟。

每个 P-DMA 控制器使用单个数据传输引擎并由相关通道共享。通用通道具有丰富的互连矩阵，包括 P-DMA 交叉触发，可满足苛刻的数据传输场景的要求。专用通道具有单个触发输入（例如 ADC 通道）来处理常见的传输需求。M-DMA 用于存储器到存储器的数据传输，并为少量通道提供高内存带宽。M-DMA 为每个通道使用专用的数据传输引擎。它们支持使用 AHB 多层总线去独立访问外设。

3.1.3 闪存

CYT2BL 具有 4160 KB（4032 KB 扇区大小为 32 KB，128 KB 扇区大小为 8 KB）的代码闪存，以及额外的工作闪存高达 128 KB（96 KB 扇区大小为 2 KB，32 KB 扇区大小为 128 B）。工作闪存经过了优化，可以比代码闪存进行更多次重新编程。代码闪存支持边写边读（RWW）操作，允许在 CPU 运行模式时更新闪存。代码闪存和工作闪存区域均支持远程升级（OTA）编程的双区操作。

3.1.4 SRAM

CYT2BL 具有 512 KB 的 SRAM 和两个独立的控制器。第一个控制器SRAM0 以 32 KB 的增量提供在深度睡眠模式保留，而 SRAM1 可在完全保留或不保留之间选择。

3.1.5 ROM

CYT2BL 具有 32 KB 的 ROM，其中包含启动和配置例程。该 ROM 可实现安全启动和用户的闪存验证，以保证系统的安全。

3.1.6 安全加密加速器

密码加速器实现（3）DES 功能块密码、AES 功能块密码、SHA 散列、循环冗余校验、伪随机数生成、真随机数生成、伽罗瓦/计数器模式和矢量单元以支持 RSA 和 ECC 等非对称密钥密码。

根据料号的不同，此功能块可能完全可用、部分可用或完全不可用。详情参见订购信息。

3.2 系统资源

3.2.1 电源系统

电源系统确保电源电压水平满足每种电源模式的要求，并在这些水平无效时提供全系统复位。内部上电复位（POR）保证初始电源上升期间的全芯片复位。

三个欠压检测（BOD）电路用于监测外部电源电压（V_{DDD}、V_{DDA}、V_{CCD}）。V_{DDD} 和 V_{CCD} 上的初始状态为启用且无法禁用 BOD。V_{DDA} 上的 BOD 初始状态为禁用，可由用户启用。对于外部电源 V_{DDD} 和 V_{DDA}，BOD 电路可通过软件配置，提供两种设置：一种是适用于所有内部信号的 2.7 V 最小电压，另一种是适用于所有 I/O 规范的 3.0 V 最小电压（2.7 V 时 I/O 规范得到保证）。V_{CCD} 上的 BOD 仅作为安全措施提供，并非可靠的检测器。

提供三个过压检测（OVD）电路用于监控外部电源（V_{DDD}、V_{DDA}、V_{CCD}），以及过流检测（OCD）电路用于监控内部和外部稳压器。V_{DDD} 和 V_{DDA} 上的 OVD 阈值可配置为两种设置：5.0 V 和 5.5 V 最大电压。

提供了两个电压检测电路来监控外部电源电压（V_{DDD}）的下降和上升电平，每个电路均可配置为 26 个可选电平之一。

V_{DDD} 和 V_{CCD} 上的所有 BOD、OVD 和 OCD 电路都会产生复位，因为它们用于保护 CPU 和故障逻辑。V_{DDA} 上的 BOD 和 OVD 电路可以配置为产生复位或故障。

3.2.2 稳压器

CYT2BL 包含两个稳压器，为低压核晶体管提供电源：深度睡眠和核内稳压器。这些稳压器接受 2.7 V 至 5.5 V V_{DDD} 供电，并为器件的各个部分提供低噪声的 1.1 V 供电。这些稳压器在切换电源模式时由硬件和固件自动启用和禁用。核内稳压器在激活模式下工作，为 CPU 子系统及相关外设供电。

3.2.2.1 深度睡眠

深度睡眠稳压器用于在深度睡眠模式下维持供电给少数模块。这些模块包括 ILO 和 WDT 定时器、BOD 检测器、SCB0、SRAM 存储器、智能 I/O 和其他配置存储器。深度睡眠稳压器在深度睡眠模式下启用，此时核内稳压器被禁用。 当 XRES_L 有效（低电平）并且核内稳压器被禁用时，深度睡眠稳压器也被禁用。

3.2.2.2 核心内部

核内稳压器支持高达 150 mA 的负载电流，并且在器件启动（启动过程）期间以及在运行/睡眠模式下运行。

3.2.3 时钟系统

CYT2BL 时钟系统为所有需要时钟的子系统提供时钟，并在不同时钟源之间实现无缝切换。此外，它还确保不发生亚稳态。

CYT2BL 的时钟系统由 8 MHz IMO、两个 ILO、三个看门狗定时器、一个 PLL、一个 FLL、五个时钟监视器 (CSV)、一个 3.988 至 33.34 MHz ECO 和一个 32.768 kHz WCO 组成。

时钟系统支持两个主时钟域：CLK_HF 和 CLK_LF。

- CLK_HFx 是运行域时钟。每个都可以使用任何高频时钟源，包括 IMO、EXT_CLK、ECO、FLL 或 PLL。
- CLK_LF 是深度睡眠域时钟，为 MCWDT 或 RTC 模块提供源。CLK_LF 域的基准时钟可以从 ILO0、ILO1、WCO 中选择或禁用。

表 3　　CLK_HF 目标

Name	Description
CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure
CLK_HF1	Event Generator, also available in HSIOM as an output

3.2.3.1　IMO 时钟源

IMO 是 CYT2BL 的频率基准，当没有外部基准可用或被使能时。IMO 的运行频率约为 8 MHz。

3.2.3.2　ILO 时钟源

ILO 是一种低功耗振荡器，标称频率为 32.768 kHz，在深度睡眠模式下为看门狗定时器产生时钟。有两个 ILO 可确保深度睡眠模式下的时钟监控器 (CSV) 功能。可以根据 IMO、WCO 或 ECO 来校准 ILO 驱动的计数器，以提高其精度。ILO1 也用于时钟监控。

3.2.3.3　PLL 和 FLL

可以使用 PLL或 FLL 从 IMO、ECO 或 EXT_CLK 生成高速时钟。FLL 的锁定速度比 PLL 快得多（5 µs，而PLL 为 35 µs），但会引入少量频率误差 [5]。

3.2.3.4　时钟监测器

每个时钟监控器 (CSV) 允许一个时钟 (基准) 监控另一个时钟 (被监控) 的行为。每个 CSV 都有用于监控和参考时钟的计数器。每个计数器的参数决定基准时钟的频率以及受监控时钟的频率上限和下限。如果频率范围比较器检测到停止的时钟或指定频率范围之外的时钟，则会发出异常状态信号并产生复位或中断。

3.2.3.5　EXT_CLK

两个 GPIO_STD I/O 中的一个可用于提供高达 80 MHz 的外部时钟输入。该时钟可以用作 PLL 或 FLL 的源时钟，也可以直接由 CLK_HF 域使用。

3.2.3.6　ECO

ECO 使用连接到 ECO_IN 和 ECO_OUT 引脚的外部晶体提供高频时钟。它支持基模（非泛音）石英晶体，范围为 3.988 至 33.34 MHz。与 PLL 结合使用时，它能生成 CPU 和外设所需的器件最大时钟。ECO 精度取决于所选的晶体。如果 ECO 被禁用，则相关引脚可用于任何可用的 I/O 功能。

5　由于频率误差，不建议使用基于 FLL 的参考源来操作参考定时外设（例如 UART）。

3.2.3.7 WCO

WCO 是一款低功耗时钟晶振振荡器，适用于实时时钟应用。它需要一个外部 32.768-kHz 晶振连接到 WCO_IN 和 WCO_OUT 引脚。WCO 还可以配置为 CLK_LF 的时钟基准，CLK_LF 是MCWDT 和 RTC 的时钟源。

3.2.4 复位

CYT2BL 可以从多种来源复位，包括软件。复位事件是异步的，并能够确保器件恢复到一个已知状态。复位原因（POR、BOD、OVD、过流、XRES_L、WDT、MCWDT、软件复位、故障、CSV、休眠唤醒、调试）记录在一个寄存器中，该寄存器在复位后保留，并允许软件确定复位的原因。XRES_L 引脚可用于外部复位。

3.2.5 看门狗定时器

CYT2BL 具有一个看门狗定时器（WDT）和两个多计数器看门狗定时器（MCWDT）。

WDT 是一个自由运行的计数器，仅由 ILO0 提供时钟，因此可以将其用作休眠模式的唤醒源。这允许在所有电源模式下进行看门狗操作，并且需要在配置的窗口期间进行维护，否则如果在超时发生之前未进行维护，则会生成看门狗复位。看门狗复位被记录在复位原因寄存器中。

每个 CPU 核都有一个 MCWDT。这些定时器提供比 WDT 更多的功能，并且仅在运行、睡眠和深度睡眠模式下可用。这些计时器有多个计数器，可以单独使用或级联使用来触发中断和/或复位。它们由 ILO0 或 WCO 提供时钟。

3.2.6 功耗模式

CYT2BL 有六种功耗模式。

- 运行 – 所有外设均可用
- 低功耗运行（LPACTIVE） – 运行模式低功耗配置，其中所有外设和 CPU 均可用，但功能有限
- 睡眠 – 除 CPU 外的所有外设均可用
- 低功耗睡眠（LPSLEEP） – 睡眠模式低功耗配置，其中除 CPU 之外的所有外设均可用，但功能有限
- 深度睡眠 – 仅可使用与 CLK_LF 配合使用的外设
- 休眠 – 器件和 I/O 状态被冻结，器件在唤醒时会复位

3.3 外设

3.3.1 外设时钟分频器

提供整数和小数时钟分频器用于外设和定时目的。

表 4 时钟分频器

Divider	Count	Description
div_8	32	Integer divider, 8 bits
div_16	16	Integer divider, 16 bits
div_24_5	8	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 外设保护单元

外设保护单元（PPU）控制和监视从所有主设备（CPU、P-/M-DMA、加密和任何启用的调试接口）到外设的未经授权的访问。它允许或限制总线基础设施上的数据传输。访问规则是根据传输的特定属性来强制执行的，例如传输的地址范围和访问属性（例如读/写、用户/特殊权限和安全/非安全）。

3.3.3 12 位 SAR ADC

CYT2BL 包含三个 1-Msps SAR ADC。这类 ADC 的时钟频率高达 26.67 MHz，可在 26 个时钟周期内提供 12 位结果。

所有三个SAR ADC 的参考信号来自一对专用输入：VREFH 和 VREFL[6]。

CYT2BL 支持多达 85 个逻辑 ADC 通道，以及多达 67 个 I/O 的外部输入。每个 ADC 还支持六个内部连接，用于诊断和监控。表 1 列出了 ADC 通道数量（每个 ADC 和封装类型）。

每个 ADC 都有一个序列器，能够自主循环配置的通道（序列扫描），并且没有切换开销（也就是说，当时钟频率为26.67 MHz时，无论用于单个通道还是分布在多个通道上，总采样率都等于 1 Msps）。序列器切换通过状态机或固件控制。序列器对触发请求进行优先级排序，启用适当的模拟通道，控制 ADC 采样，启动 ADC 数据转换，管理结果，并启动后续的重复转换或组转换，而无需 CPU 干预。

每个 SAR ADC 都有一个模拟多路复用器，用于将要测量的信号连接到 ADC。它有 32 个 GPIO_STD 输入、一个用于电机感应的特殊 GPIO_STD 输入，以及6个附加输入，用于测量内部信号，如带隙基准、温度传感器和电源。该器件支持三个 ADC 上一个电机检测通道的同步采样。

CYT2BL 有一个温度传感器，由3个 ADC 共享。温度传感器每次只能由一个 ADC 进行采样。需要软件后处理将温度传感器读数转换为开尔文或摄氏度值。

为了适应各种源阻抗和频率的信号，每个通道可以编程不同的采样时间。ADC 还支持范围比较功能，无需等待定序器扫描完成，也无需等待 CPU 固件评估测量值是否超出量程，即可快速检测出超出范围的数值。

ADC 不能用于深度睡眠和休眠模式，因为它们需要高速时钟。ADC 输入基准电压 VREFH 范围为 2.7 V 至V_{DDA}，VREFL 为V_{SSA}。

3.3.4 定时器/计数器/PWM (TCPWM) 模块

TCPWM 功能块由 16 位（75 个通道）和 32 位（8 个通道）计数器组成，具有用户可编程周期。其中 12 个 16 位计数器具有支持电机控制操作的额外功能。每个 TCPWM 计数器包含一个捕获寄存器，用于记录发生事件时的计数值，一个周期寄存器 (用于停止或自动重新加载计数值，当计数值等于周期寄存器的值) 和比较寄存器，用于控制 PWM 占空比。

TCPWM 模块内的每个计数器都支持多种功能模式，例如定时器、捕获、正交、PWM、带死区插入的 PWM（PWM_DT，8 位）、伪随机 PWM（PWM_PR）和移位寄存器。

在电机控制应用中，TCPWM功能块内的计数器支持增强型正交模式，具有非对称 PWM 产生、死区插入（16 位）以及 PWM 输出信号的不同死区关联等功能。

6 VREF_L 可防止 VSSIO 和 VSSA 路径中的 IR 压降影响测量。当 VREF_L 正确连接时，可以降低或消除 VSSIO 和 VSSA 路径中的 IR 压降对测量的影响。

TCPWM 模块还提供了正向输出和反向输出，它们之间偏移可编程控制，以允许它们用作死区互补 PWM 输出。TCPWM 模块还具有 kill 输入（仅适用于 PWM 模式）用于强制输出进入预定状态；例如，在马达驱动系统中，当出现过流状态时，需要立即使用它来关闭驱动 FET 的PWM（没有时间用于软件干预）。

3.3.5 串行通信模块 (SCB)

CYT2BL 包含 8 个串行通信模块，每个模块可配置为 I²C、UART 或 SPI。

- I2C接口

  SCB可配置为实现完整的 I²C主设备（能够进行多主设备仲裁）或从设备接口。每个由 SCB 配置的 I²C 都可以以高达 1 Mbps 的速度运行（增强型快速模式 [7]），并具有灵活的缓冲选项，以减少中断开销和 CPU 的延迟。此外，每个SCB都支持接收和发送数据的 FIFO 缓冲，这通过增加 CPU 读取数据的时间，减少了时钟延长的需要。I²C接口与标准、快速模式和增强型快速模式设备兼容，如 NXP I²C 总线规范和用户手册 (UM10204) 中所规定。I²C 总线 I/O 采用 GPIO 开漏模式 [8]，[9] 实现。

- UART 接口

  当配置为 UART，每个 SCB 提供全功能 UART，其最大速率由配置的外设时钟频率和过采样率确定。它支持红外接口（IrDA）和智能卡（ISO 7816）协议，这些协议是 UART 协议的小变种。此外，它还支持 9 位多处理器模式，此模式允许寻址连接到通用 RX 和 TX 线的外设。支持通用 UART 功能，如奇偶校验、停止位的数量、中断检测和帧错误。发送和接收数据的 FIFO 缓冲允许容忍更大的 CPU 服务延迟。 LIN 协议由 UART 支持。LIN 基于单主多从拓扑结构。LIN 总线上有一个主节点和多个从机节点。SCB UART 仅支持 LIN 从机功能。 与专用 LIN 模块相比，以 SCB/UART 用作 LIN 需要更高水平的软件交互和增加 CPU 负载。

- SPI 接口

  SPI 配置支持完整的 Motorola SPI、TI 同步串行协议 (SSP，本质上是添加启动脉冲用于同步基于 SPI 的编解码) 和 National Microwire (SPI 的半双工形式)。SPI 接口可以使用 FIFO。SPI 接口以高达 12.5 MHz 的 SPI 时钟运行。SCB 还支持 EZSPI [10] 模式。

SCB0 支持以下附加特性：

- 在深度睡眠模式下可作为从机操作
- I ²C 从机 EZ (EZI2C [11]) 模式，最多可容纳 256-B 数据缓冲，无需 CPU 干预即可实现多字节通讯
- I²C 从机外部时钟操作
- 具有 512 B 数据缓冲区的命令/响应模式，可进行多字节通信，无需 CPU 干预

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7 I/O 驱动电平不支持增强型快速模式速度下的完整电流电容。

8 这并非 100% 符合 I2C-总线规范；I/O 不符合高压标准，不支持增强型快速模式的 20 mA 灌电流要求，并且在不供电的情况下违反泄漏规范。

9 只有 Port 0 启用斜率控制下满足最小下降时间要求。

10 Easy SPI (EZSPI) 协议基于摩托罗拉 SPI 协议可在任何模式（0、1、2 或 3）下运行。它允许主机和从机之间进行通信，同时减少 CPU 干预的需要。

11 Easy I²C (EZI2C) 协议是英飞凌在 I²C 协议基础上构建的独特通信方案。它使用标准 I²C 协议周围的元协议，使用索引内存传输与 I²C 从机进行通信。这减少了对 CPU 干预的需要。

3.3.6 CAN FD

CYT2BL 包含两个 CAN FD 控制器模块，每个模块支持四个 CAN FD 通道。所有 CAN FD 控制器均符合 ISO 11898-1:2015 标准；可提供 ISO 16845:2015 证书。它还在硬件中完全实现了 ISO 11898-4（TTCAN 协议级别 1 和 2）中指定的时间触发 CAN（TTCAN）协议。所有与信息处理有关的功能均由 Rx 和 Tx 处理程序实现。Rx 处理器管理信息接受过滤、将接收到的消息从 CAN 核心传输到消息 RAM，并提供接收消息状态。Tx 处理器负责将发送信息从信息 RAM 传输到 CAN 核心，并提供发送消息状态。

3.3.7 本地互连网络（LIN）

CYT2BL 含有多达 12 个 LIN 通道。每个功能块都支持按照 ISO 标准 17987 的 LIN 协议传输/接收数据。每个 LIN 功能块通过3引脚接口（包括使能函数）连接到外部收发器，并支持主机和从机功能。每个通道还支持经典和增强的检验和，以及消息接收和唤醒信令期间的中断检测。断点检测、同步场、校验和计算以及错误中断均由硬件处理。

3.3.8 时钟扩展外设接口（CXPI）

CYT2BL 包含多达4个符合 JASO D015 和 ISO 标准 20794（包括控制器规范）的 CXPI 通道。

每个通道支持：

- 主机和从机功能
- 针对正常帧和长帧的轮询和事件触发方法
- 非归零编码（NRZ）和PWM信号模式
- 碰撞解析以及载波监听多路访问机制
- 唤醒脉冲的生成和检测
- 正常帧和长帧的 CRC8 和 CRC16
- 错误检测
- 用于发送和接收的专用 FIFO (16 B)

3.3.9 一次性可编程（OTP）eFuse

CYT2BL 包含一个 1024 位 OTP eFuse 存储器，可用于存储和访问每个器件的唯一且不可更改的标识符或序列号。eFuse 还用于控制设备生命周期（制造、编程、正常运行、寿命终止等）和安全状态。在 1024 位中，有 192 位可供用户使用。

3.3.10 事件发生器

事件发生器支持在运行模式下产生中断和触发，以及在深度睡眠模式下产生中断。事件发生器用于触发特定的器件操作（执行中断处理程序、SAR ADC 转换等）并提供从深度睡眠模式的循环唤醒机制。它们为器件功能提供无需 CPU 的触发器，减少 CPU 在触发器件功能时的参与，从而降低总体功率消耗和处理开销。

3.3.11 触发器多路复用器

CYT2BL 支持使用触发信号连接各种外设。触发器用于通知外部设备事件的发生或状态的改变。这些触发器用于影响或启动其他外设的某些操作。

触发器多路复用器用于将触发器从来源设备路由到目的地。触发器提供主动的逻辑功能，并且通常在运行模式下支持。

3.4 I/O

CYT2BL 具有多达 152 个可编程 I/O。

I/O 被组织为称为端口的逻辑实体，其最大宽度为 8 位。在上电和复位期间，I/O 被强制进入高阻状态。在休眠模式期间，I/O 被冻结。

每个 I/O 引脚都能生成一个中断（如果被启用），并且每个 I/O 端口都有一个与其相关的中断请求（IRQ）和中断服务程序（ISR）。

I/O 端口功率源映射列于表 5 中。相关电源决定了配置为 CMOS 和汽车阈值时的 V_{OH}、V_{OL}、V_{IH} 和 V_{IL} 电平。

表 5 I/O 端口电源

Supply	Ports
V_{DDD}	P0, P1, P2, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23
V_{DDIO_1}	P6, P7, P8, P9[1)]
V_{DDIO_2}	P10, P11, P12, P13, P14, P15

1) VDDIO_1 域中的 I/O 是指 64-LQFP 封装中的 VDDD 域。

3.4.1 端口命名规则

Px.y 描述 I/O 端口 “x” 内可用的特定位 “y”。

例如，P4.2 读取“端口 4，位 2”。
每个 I/O 实施以下内容：

- 可编程驱动模式
  - 高阻态
  - 电阻上拉
  - 电阻下拉
  - 开漏和强下拉
  - 开漏和强上拉
  - 强上拉或下拉
  - 弱上拉或下拉

CYT2BL 有两种可编程 I/O：GPIO 标准和 GPIO 增强。

3.4.2 GPIO 标准 (GPIO_STD)

支持 2.7 V 至 5.5 V V_{DDIO} 范围内的标准汽车信号。GPIO 标准 I/O 具有多个可配置的驱动级别、驱动模式和可选的输入级别。

3.4.3 GPIO 增强 (GPIO_ENH)

支持 2.7 V 至 5.5 V V_{DDIO} 范围内的扩展功能汽车信号，可在较低电压下提供更高的电流（完全 I^2C 时序支持、斜率控制）。

GPIO_STD 和 GPIO_ENH 都实现了以下内容：

- 可配置输入阈值（CMOS、TTL 或汽车）

- 保持模式，用于锁存先前状态（即保持 I/O 状态处于深度睡眠模式）
- 模拟输入模式（输入和输出缓冲器禁用）

3.4.4 智能 I/O

智能 I/O 允许对从芯片子系统发送到 I/O 的信号或进入芯片的信号进行布尔运算。CYT2BL 有5个智能 I/O 块。操作可以是同步或异步，并且块可以在除休眠之外的所有器件功率模式下操作。

4 CYT2BL 地址映射

CYT2BL 微控制器支持所示的存储空间如图 2：

- 4160 KB（4032 KB + 128 KB）代码闪存，用于单组或双组模式基于相关的位元在闪存控制寄存器
  - 单组模式 - 4160 KB
  - 双组模式 - 每组 2080 KB
- 128 KB（96 KB + 32 KB）工作闪存，用于单组或双组模式基于相关的位元在闪存控制寄存器
  - 单组模式 - 128 KB
  - 双组模式 - 每组 64 KB
- 32 KB 安全 ROM
- 512 KB SRAM（前 2 KB 保留供内部使用）

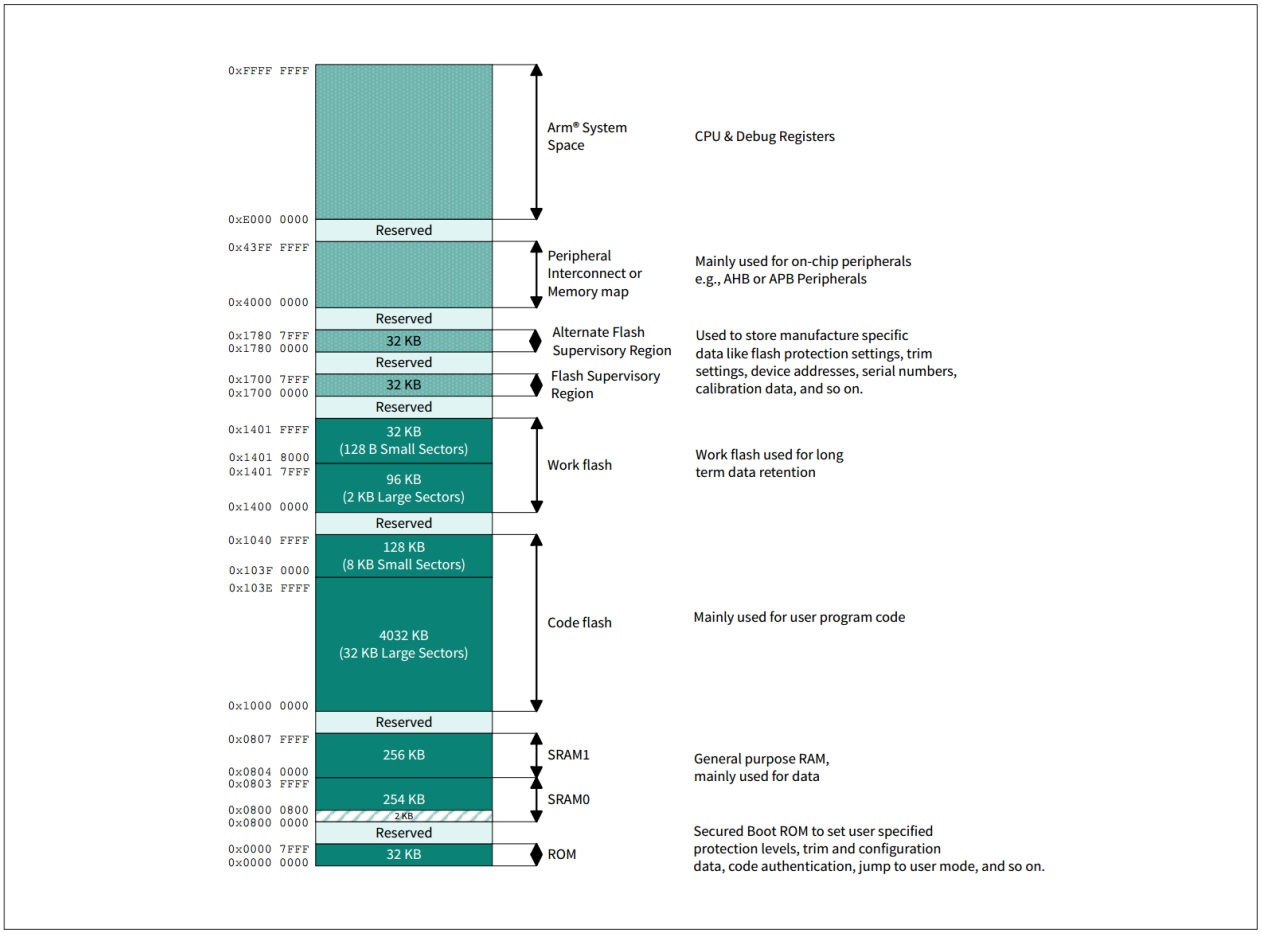

图 2 CYT2BL 地址映射[12)] , [13)]

12 尺寸不是等比例缩放。

13 第一个 2KB SRAM 被保留，不供用户使用。用户必须在所有工作、低功耗工作、睡眠、低功耗睡眠和深度睡眠模式下，保 持 SRAM0 前 32 KB 功能块的供电处于使能或保留状态。

5 闪存基地址映射

表 6 至表11 提供有关代码和工作闪存区域的扇区映射及其各自基地址的信息。

表 6 单组模式下代码闪存地址映射

Code-flash size (KB)	Large sectors (LS)	Small sectors (SS)	Large sector base address	Small sector base address
4160	32 KB × 126	8 KB × 16	0x1000 0000	0x103F 0000

表 7 单组模式下工作闪存地址映射

Work-flash size (KB)	Large sectors (LS)	Small sectors (SS)	Large sector base address	Small sector base address
128	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000

表 8 双组模式下代码闪存地址映射（映射 A）

Code-flash Size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
4160	32 KB × 63	8KB × 8	32 KB × 63	8 KB × 8	0x1000 0000	0x101F 8000	0x1200 0000	0x121F 8000

表 9 双组模式下代码闪存地址映射（映射 B）

Code-flash size (KB)	First half LS	First half SS	Second Half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1200 0000	0x121F 8000	0x1000 0000	0x101F 8000

表 10 双组模式下工作闪存地址映射（映射 A）

Work-flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1400 0000	0x1400 0000	0x1500 0000	0x1500 C000

表 11 双组模式下工作闪存地址映射（映射 B）

Work-flash size (KB)	First half LS	First half SS	Second half LS	Second half SS	First half LS base address	First half SS base address	Second half LS base address	Second half SS base address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1500 0000	0x1500 C000	0x1400 0000	0x1400 0000

6 外设 I/O 映射

表 12 CYT2BL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	Group	Slave
PERI	Peripheral interconnect	0x4000 0000			0	0
	Peripheral group (0, 1, 2, 3, 5, 6, 9)	0x4000 0000	7	0x20		
	Peripheral trigger group	0x4000 0000	11	0x400		
	Peripheral 1:1 trigger group	0x4000 0000	11	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4001 0000			0	1
	PERI Programmable PPU	0x4001 0000	6[1)]	0x40		
	PERI Fixed PPU	0x4001 0800	487	0x40		
Crypto	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000			2	2
	IPC structures	0x4022 0000	8	0x20		
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000			2	3
	Shared memory protection unit structures	0x4023 2000	16	0x40		
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	FLASH controller	0x4024 0000			2	4
SRSS	System Resources Sub-System Core Registers	0x4026 0000			2	5
	Clock Supervision High Frequency	0x4026 1400	3	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Multi Counter WDT	0x4026 8000	2	0x100		
	Free Running WDT	0x4026 0000	1			
Backup	SRSS Backup Domain/RTC	0x4027 0000			2	6
	Backup Register	0x4027 1000	4	0x04		
P-DMA	P-DMA0 Controller	0x4028 0000			2	7
	P-DMA0 channel structures	0x4028 8000	92	0x40		
	P-DMA1 Controller	0x4029 0000			2	8
	P-DMA1 channel structures	0x4029 8000	44	0x40		

（表格续下页……）

表 12 (续) CYT2BL 外设 I/O 映射

Section	Description	Base address	Instances	Instance size	Group	Slave
M-DMA	M-DMA0 Controller	0x402A 0000			2	9
	M-DMA0 channels	0x402A 1000	4	0x100		
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	10
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	24	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	24	0x80	3	1
Smart IO	Programmable I/O configuration	0x4032 0000			3	2
	SMART I/O port configuration	0x4032 0C00	5	0x100		
TCPWM	Timer/Counter/PWM 0 (TCPWM0)	0x4038 0000			3	3
	TCPWM0 Group #0 (16-bit)	0x4038 0000	63	0x80		
	TCPWM0 Group #1 (16-bit, Motor control)	0x4038 8000	12	0x80		
	TCPWM0 Group #2 (32-bit)	0x4039 0000	8	0x80		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	4
	Event generator 0 comparator structures	0x403F 0800	11	0x20		
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	12	0x100		
CXPI	Clock Extension Peripheral Interface 0 (CXPI0)	0x4051 0000			5	1
	CXPI0 Channels	0x4051 8000	4	0x100		
TTCANFD	CAN0 controller	0x4052 0000	4	0x200	5	2
	Message RAM CAN0	0x4053 0000		0x8000		
	CAN1 controller	0x4054 0000	4	0x200	5	3
	Message RAM CAN1	0x4055 0000		0x8000		
SCB	Serial Communications Block (SPI/UART/ I^2C)	0x4060 0000	8	0x10000	6	0-7
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR1 channel controller	0x4090 1000				
	SAR2 channel controller	0x4090 2000				
	SAR0 channel structures	0x4090 0800	24	0x40		
	SAR1 channel structures	0x4090 1800	32	0x40		
	SAR2 channel structures	0x4090 2800	8	0x40		

1) 这6个可编程 PPU 由 Boot ROM 配置，并根据访问权限供用户使用。请参阅特定于设备的 TRM 以了解有关这些可编程 PPU 的配置的更多信息。

7 CYT2BL 时钟图

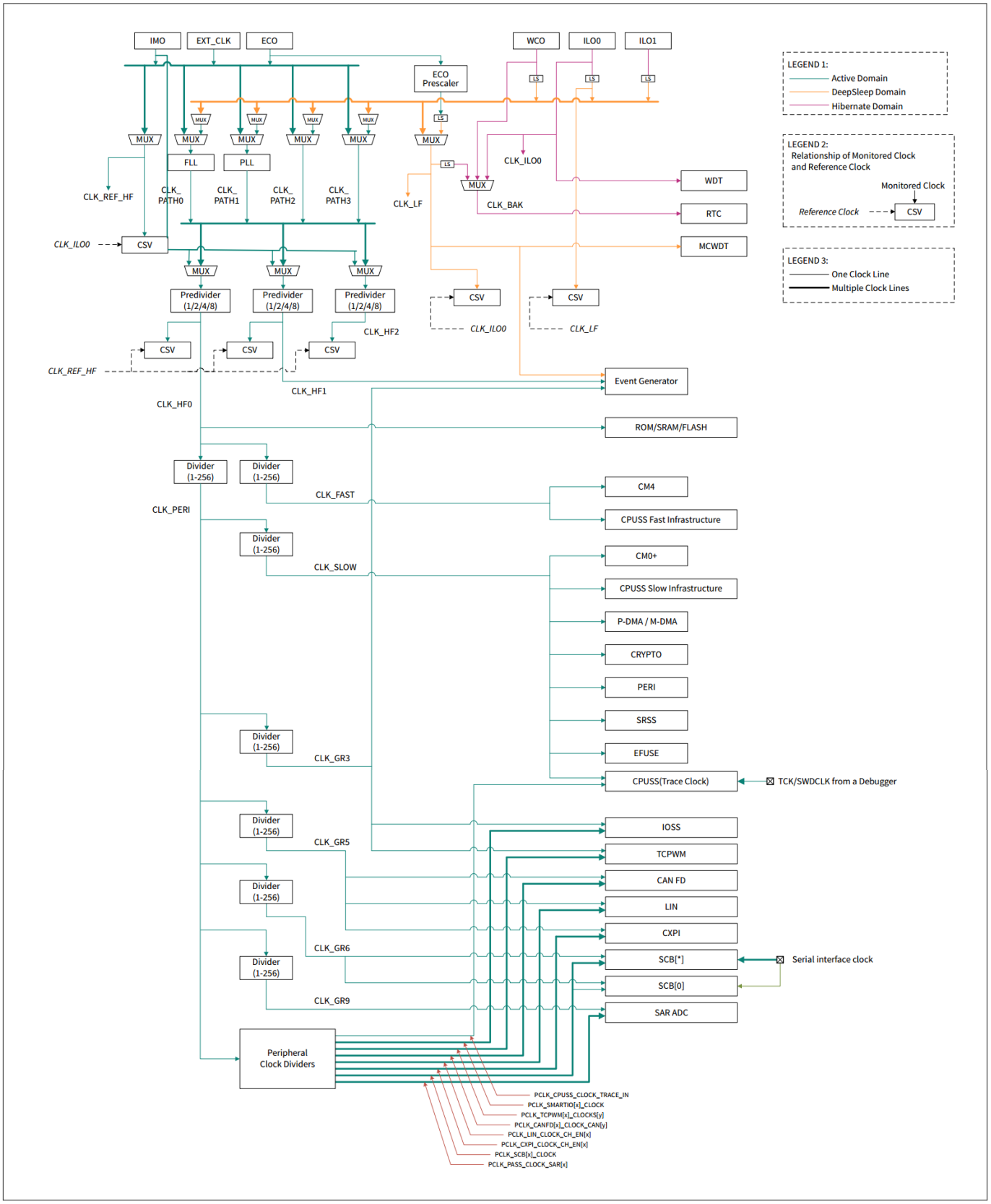

图 3 CYT2BL 时钟图

8 CYT2BL CPU 启动序列

以下步骤描述了启动序列：

1. 系统复位（@0x0000 0000）
2. CM0+ 执行 ROM 启动（@0x0000 0004）
   a. 应用调整
   b. 使能调试访问端口（DAP）访问限制以及根据来自电子保险丝和监控闪存的内容来开启系统保护
   c. 验证闪存启动（仅在安全生命周期阶段）并将控制权转移给闪存启动
3. CM0+ 执行闪存启动（来自监控闪存@0x1700 2000）
   a. 调试引脚根据 SWD/JTAG 规范配置 [14]
   b. 将 CM0+ 矢量表基址寄存器（CPUSS_CM0_VECTOR_TABLE_BASE - CPU 子系统的一部分）设置为闪存起始位置（@0x1000 0000))
   c. CM0+ 分支到其复位处理程序
4. CM0+开始执行
   a. 将 CM0+ 向量表移至 SRAM（更新 CM0+ 向量表基址）
   b. 将 CM4_VECTOR_TABLE_BASE (@0x0000 0200) 设置为闪存中提到的 CM4 向量表的位置（在 CM4 linker definition 文件中指定）。
   c. 从复位释放 CM4
   d. 继续执行 CM0+ 用户应用程序
5. CM4 直接从代码闪存或 SRAM 执行
   a. CM4 分支到其复位处理程序
   b. 继续执行 CM4 用户应用程序

[14] 在启动完成后 SWD/JTAG 引脚的端口配置将从默认的 GPIO 模式更改为支持调试，请参见表 14 了解引脚分配。

9 引脚分配

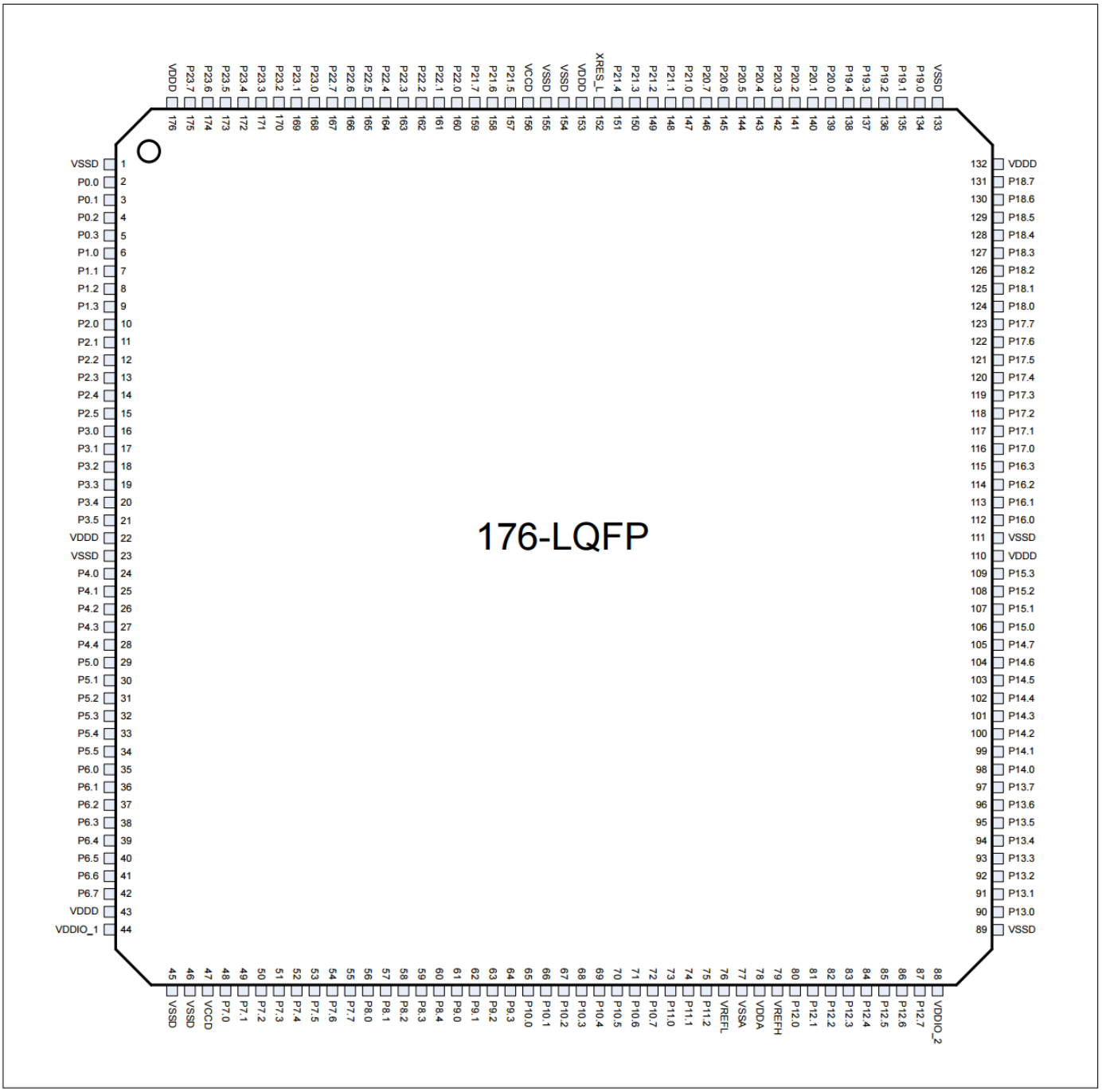

图 4 176-LQFP 引脚分配

9 Pin assignment

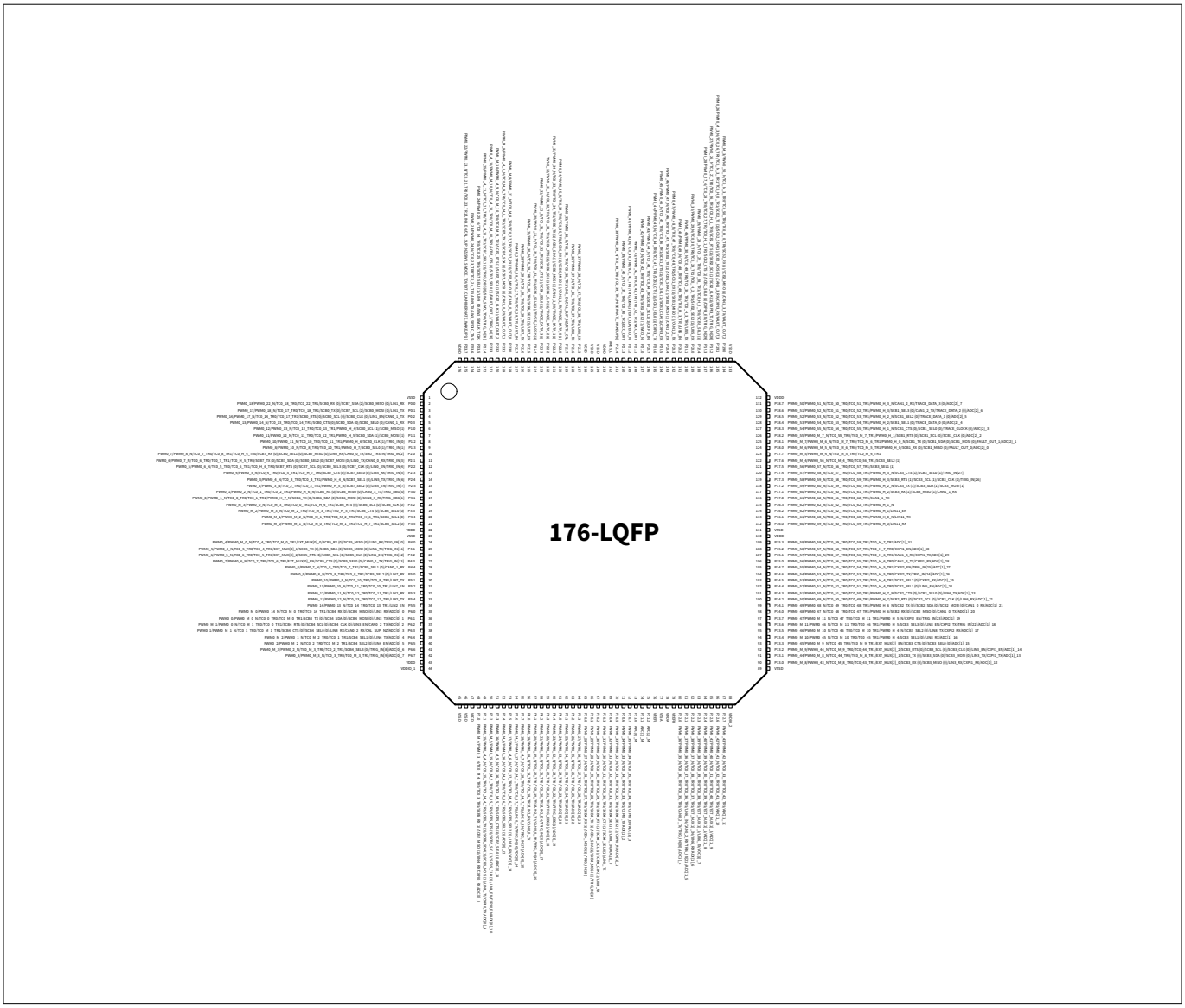

Figure 5 176-LQFP pin assignment with alternate functions

9 Pin assignment

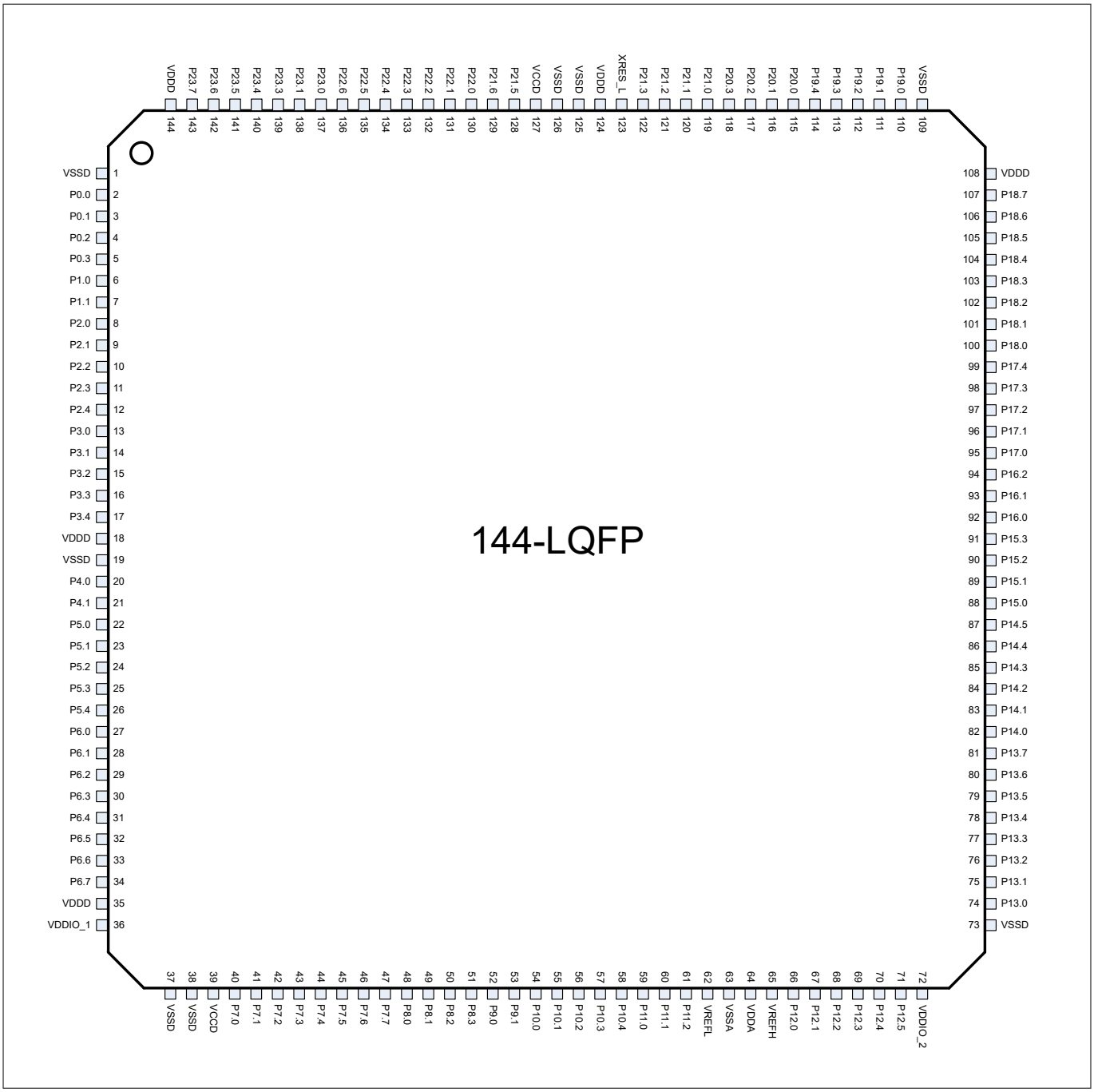

Figure 6 144-LQFP pin assignment

9 Pin assignment

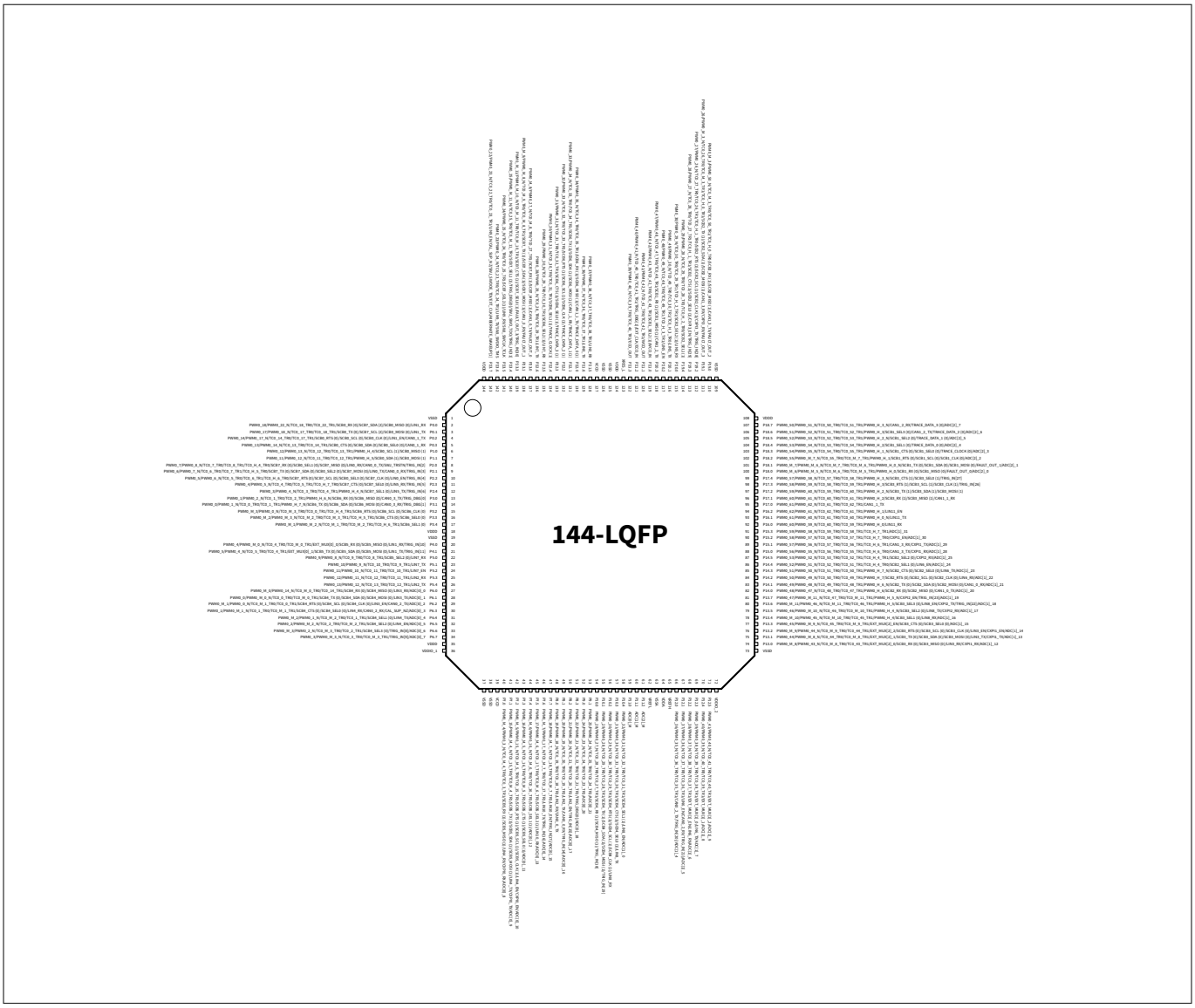

Figure 7 144-LQFP pin assignment with alternate functions

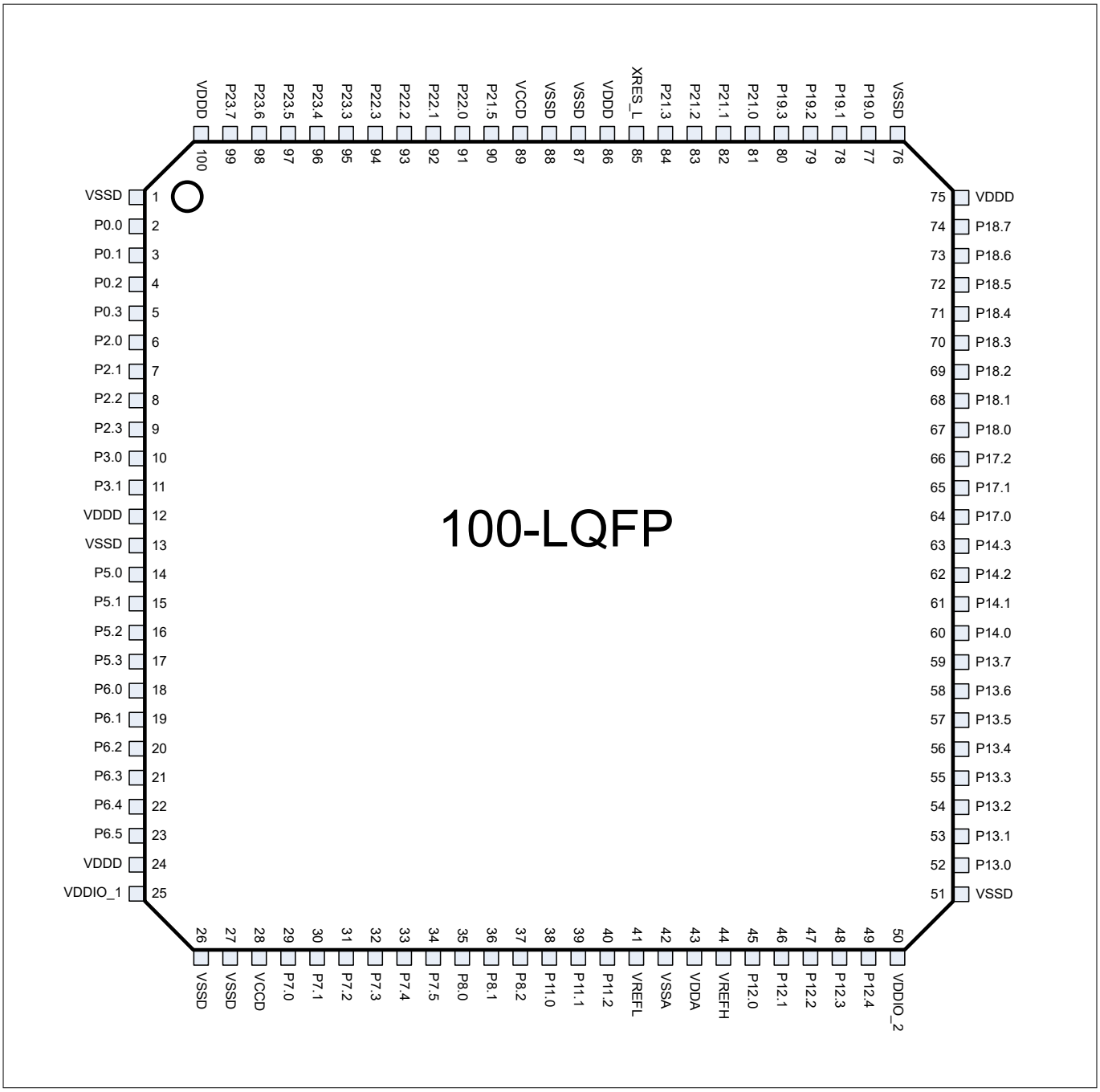

Figure 8 100-LQFP pin assignment

9 Pin assignment

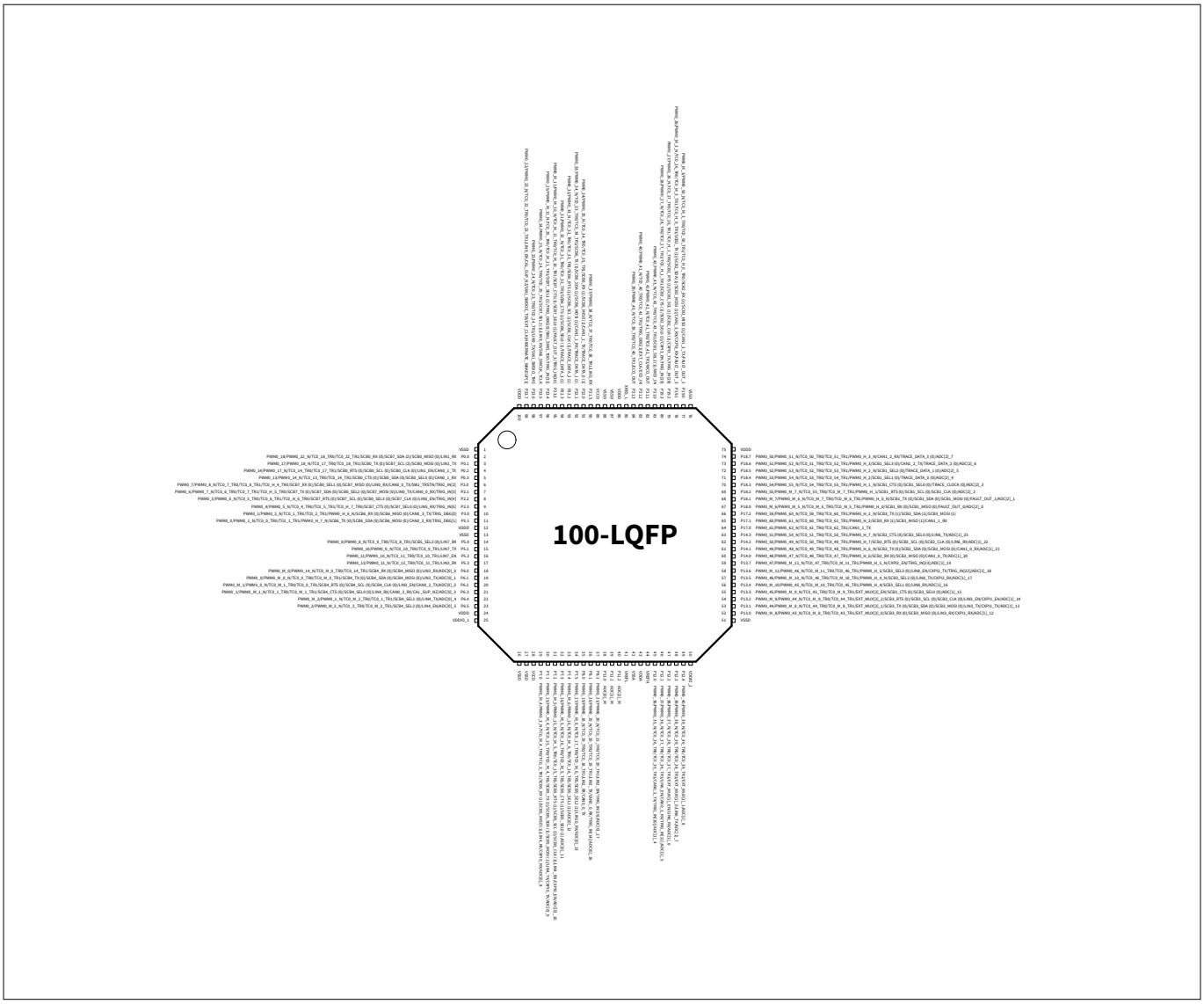

Figure 9 100-LQFP pin assignment with alternate functions

9 Pin assignment

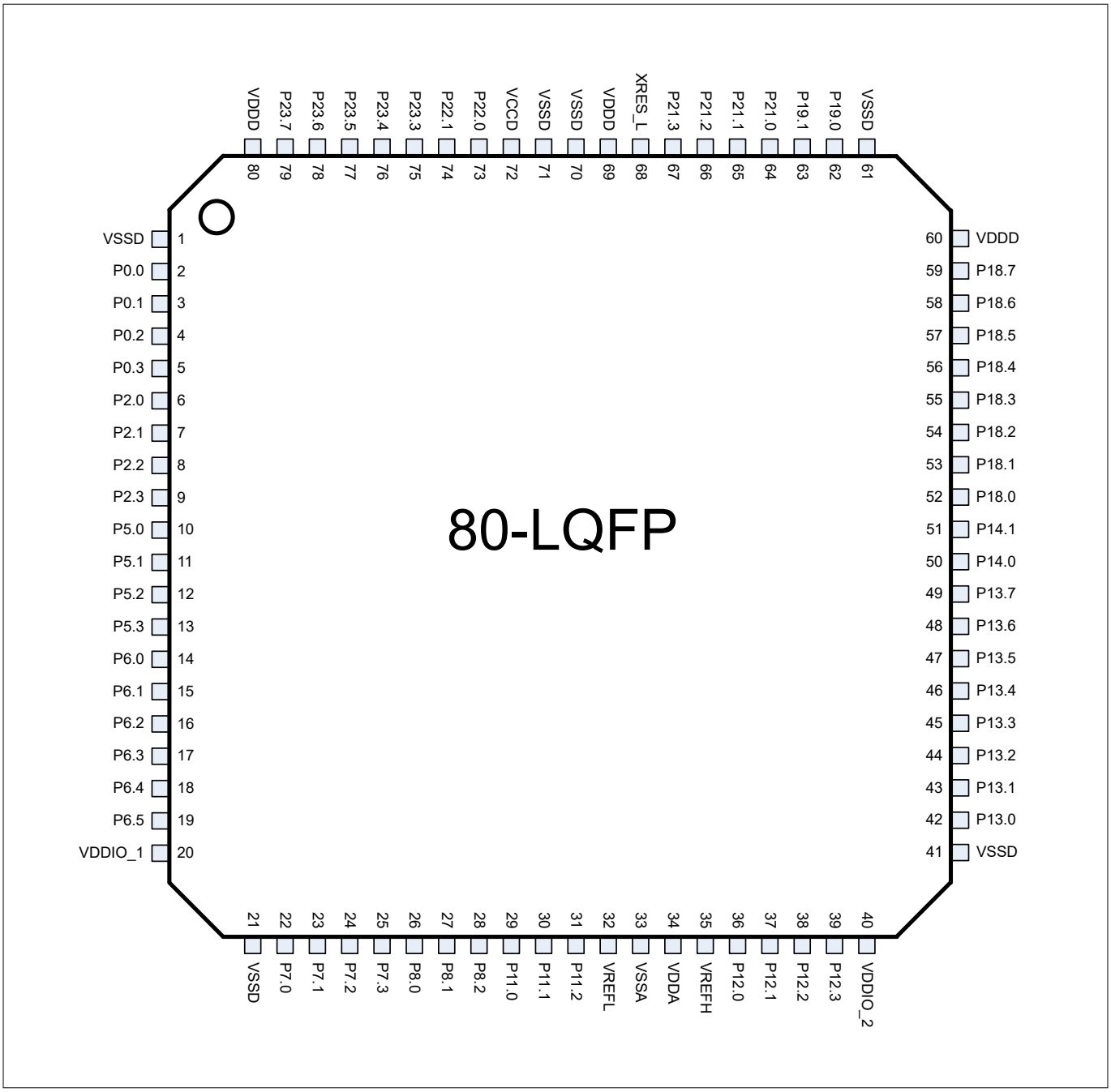

Figure 10 80-LQFP pin assignment

9 Pin assignment

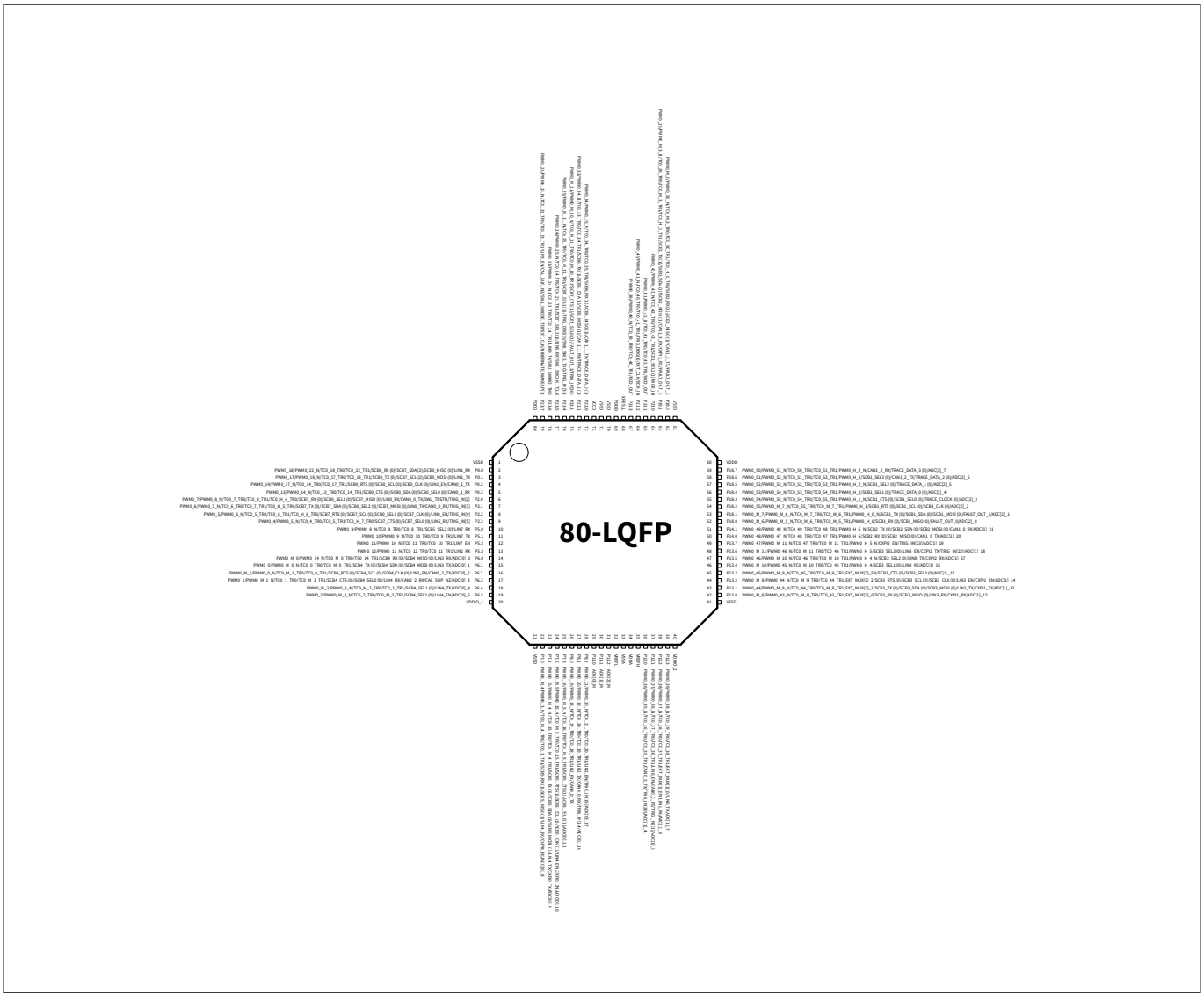

Figure 11 80-LQFP pin assignment with alternate functions

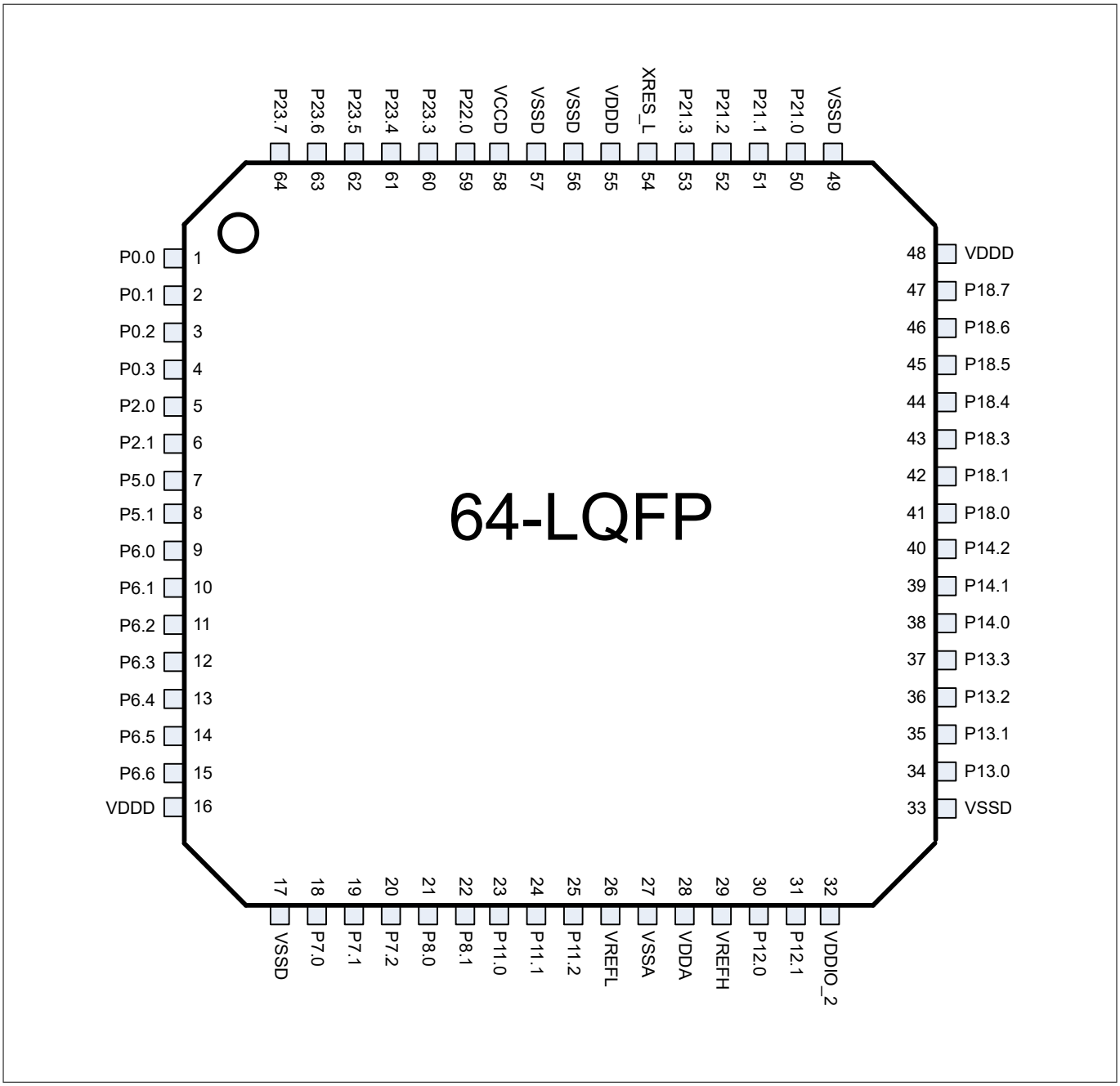

Figure 12 64-LQFP pin assignment

9 Pin assignment

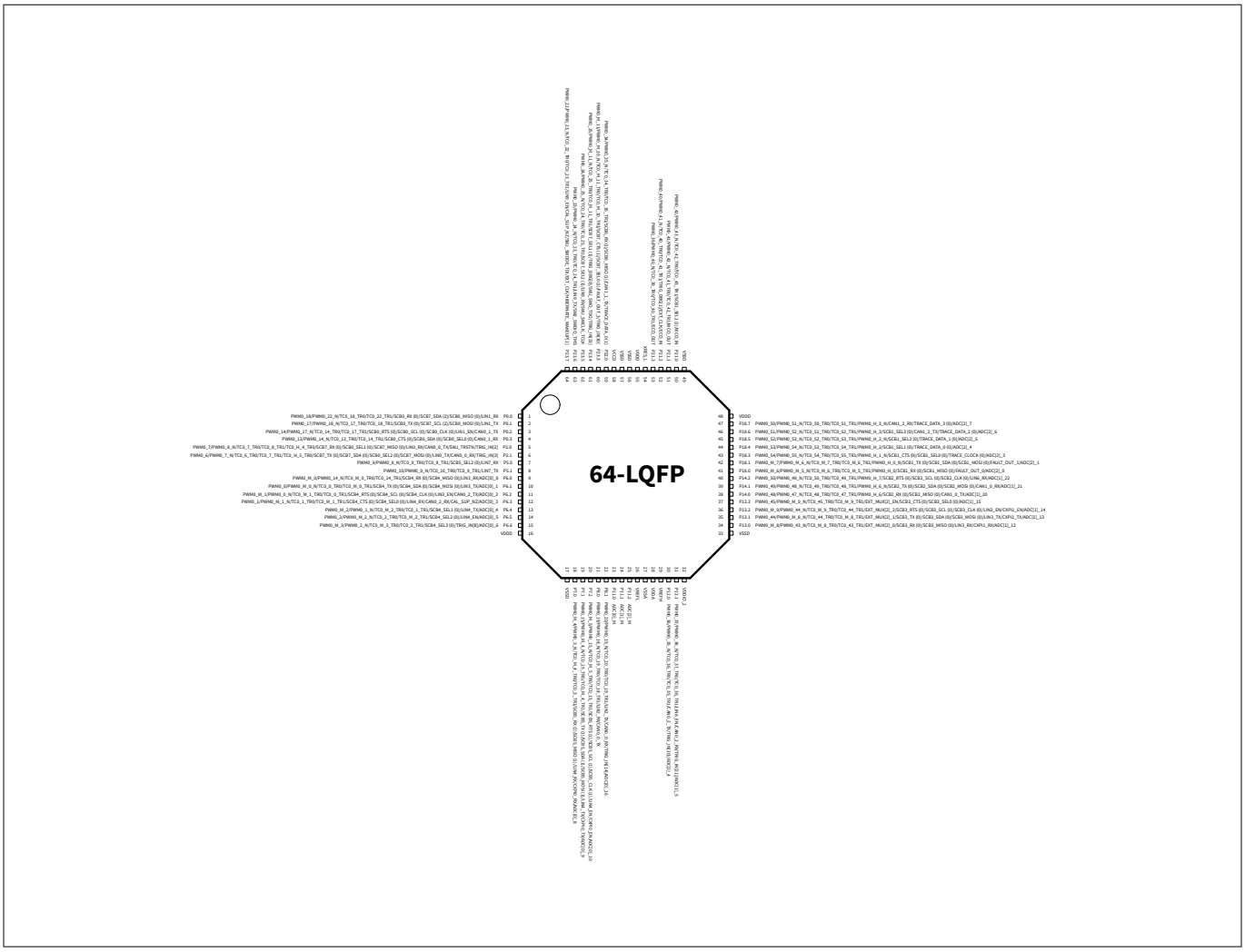

Figure 13 64-LQFP pin assignment with alternate functions

10 高速 I/O 矩阵 (HSIOM) 连接

表 13 HSIOM 连接参考

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7

11 封装引脚列表和备用功能

大多数引脚具有备用功能，如表 14 所示。

端口 11 具有以下附加功能：

- 当 $V_{DDD} < V_{DDA}$ 时，能够将全电平模拟信号传送至 SAR，而不会削波至 V_{DDD}
- 能够同时捕获三个具有最高优先级的 ADC 信号 (ADC[0:2]_M)
- 噪音更低，适用于采样灵敏的传感器

表 14 深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P0.0	GPIO_ENH	2	2	2	2	1			SCB0_MISO (0)		
P0.1	GPIO_ENH	3	3	3	3	2			SCB0_MOSI (0)		
P0.2	GPIO_ENH	4	4	4	4	3	SCB0_SCL (0)		SCB0_CLK (0)		
P0.3	GPIO_ENH	5	5	5	5	4	SCB0_SDA (0)		SCB0_SEL0 (0)		
P1.0	GPIO_STD	6	6	nA	nA	nA	SCB0_SCL (1)		SCB0_MISO (1)		
P1.1	GPIO_STD	7	7	nA	nA	nA	SCB0_SDA (1)		SCB0_MOSI (1)		
P1.2	GPIO_STD	8	nA	nA	nA	nA			SCB0_CLK (1)		
P1.3	GPIO_STD	9	nA	nA	nA	nA			SCB0_SEL0 (1)		
P2.0	GPIO_STD	10	8	6	6	5		SWJ_TRSTN	SCB0_SEL1 (0)		
P2.1	GPIO_STD	11	9	7	7	6			SCB0_SEL2 (0)		
P2.2	GPIO_STD	12	10	8	8	nA			SCB0_SEL3 (0)		
P2.3	GPIO_STD	13	11	9	9	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O 1) , [2)]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3)]			Analog	Smart IO
	HCon#0[4)]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5)]	DS #1	DS#2		
P2.4	GPIO_STD	14	12	nA	nA	nA					
P2.5	GPIO_STD	15	nA	nA	nA	nA					
P3.0	GPIO_STD	16	13	10	nA	nA					
P3.1	GPIO_STD	17	14	11	nA	nA					
P3.2	GPIO_STD	18	15	nA	nA	nA					
P3.3	GPIO_STD	19	16	nA	nA	nA					
P3.4	GPIO_STD	20	17	nA	nA	nA					
P3.5	GPIO_STD	21	nA	nA	nA	nA					
P4.0	GPIO_STD	24	20	nA	nA	nA					
P4.1	GPIO_STD	25	21	nA	nA	nA					
P4.2	GPIO_STD	26	nA	nA	nA	nA					
P4.3	GPIO_STD	27	nA	nA	nA	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P4.4	GPIO_STD	28	nA	nA	nA	nA					
P5.0	GPIO_STD	29	22	14	10	7					
P5.1	GPIO_STD	30	23	15	11	8					
P5.2	GPIO_STD	31	24	16	12	nA					
P5.3	GPIO_STD	32	25	17	13	nA					
P5.4	GPIO_STD	33	26	nA	nA	nA					
P5.5	GPIO_STD	34	nA	nA	nA	nA					
P6.0	GPIO_STD	35	27	18	14	9				ADC[0]_0	
P6.1	GPIO_STD	36	28	19	15	10				ADC[0]_1	
P6.2	GPIO_STD	37	29	20	16	11				ADC[0]_2	
P6.3	GPIO_STD	38	30	21	17	12				ADC[0]_3	
P6.4	GPIO_STD	39	31	22	18	13				ADC[0]_4	

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P6.5	GPIO_STD	40	32	23	19	14				ADC[0]_5	
P6.6	GPIO_STD	41	33	nA	nA	15				ADC[0]_6	
P6.7	GPIO_STD	42	34	nA	nA	nA				ADC[0]_7	
P7.0	GPIO_STD	48	40	29	22	18				ADC[0]_8	
P7.1	GPIO_STD	49	41	30	23	19				ADC[0]_9	
P7.2	GPIO_STD	50	42	31	24	20				ADC[0]_10	
P7.3	GPIO_STD	51	43	32	25	nA				ADC[0]_11	
P7.4	GPIO_STD	52	44	33	nA	nA				ADC[0]_12	
P7.5	GPIO_STD	53	45	34	nA	nA				ADC[0]_13	
P7.6	GPIO_STD	54	46	nA	nA	nA				ADC[0]_14	
P7.7	GPIO_STD	55	47	nA	nA	nA				ADC[0]_15	
P8.0	GPIO_STD	56	48	35	26	21					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P8.1	GPIO_STD	57	49	36	27	22				ADC[0]_16	
P8.2	GPIO_STD	58	50	37	28	nA				ADC[0]_17	
P8.3	GPIO_STD	59	51	nA	nA	nA				ADC[0]_18	
P8.4	GPIO_STD	60	nA	nA	nA	nA				ADC[0]_19	
P9.0	GPIO_STD	61	52	nA	nA	nA				ADC[0]_20	
P9.1	GPIO_STD	62	53	nA	nA	nA				ADC[0]_21	
P9.2	GPIO_STD	63	nA	nA	nA	nA				ADC[0]_22	
P9.3	GPIO_STD	64	nA	nA	nA	nA				ADC[0]_23	
P10.0	GPIO_STD	65	54	nA	nA	nA					
P10.1	GPIO_STD	66	55	nA	nA	nA					
P10.2	GPIO_STD	67	56	nA	nA	nA					
P10.3	GPIO_STD	68	57	nA	nA	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P10.4	GPIO_STD	69	58	nA	nA	nA				ADC[1]_0	
P10.5	GPIO_STD	70	nA	nA	nA	nA				ADC[1]_1	
P10.6	GPIO_STD	71	nA	nA	nA	nA				ADC[1]_2	
P10.7	GPIO_STD	72	nA	nA	nA	nA				ADC[1]_3	
P11.0	GPIO_STD	73	59	38	29	23				ADC[0]_M	
P11.1	GPIO_STD	74	60	39	30	24				ADC[1]_M	
P11.2	GPIO_STD	75	61	40	31	25				ADC[2]_M	
P12.0	GPIO_STD	80	66	45	36	30				ADC[1]_4	SMARTIO12_0
P12.1	GPIO_STD	81	67	46	37	31				ADC[1]_5	SMARTIO12_1
P12.2	GPIO_STD	82	68	47	38	nA				ADC[1]_6	SMARTIO12_2
P12.3	GPIO_STD	83	69	48	39	nA				ADC[1]_7	SMARTIO12_3
P12.4	GPIO_STD	84	70	49	nA	nA				ADC[1]_8	SMARTIO12_4

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P12.5	GPIO_STD	85	71	nA	nA	nA				ADC[1]_9	SMARTIO12_5
P12.6	GPIO_STD	86	nA	nA	nA	nA				ADC[1]_10	SMARTIO12_6
P12 .7	GPIO_STD	87	nA	nA	nA	nA				ADC[1]_11	SMARTIO12_7
P13 .0	GPIO_STD	90	74	52	42	34				ADC[1]_12	SMARTIO13_0
P13.1	GPIO_STD	91	75	53	43	35				ADC[1]_13	SMARTIO13_1
P13.2	GPIO_STD	92	76	54	44	36				ADC[1]_14	SMARTIO13_2
P13.3	GPIO_STD	93	77	55	45	37				ADC[1]_15	SMARTIO13_3
P13.4	GPIO_STD	94	78	56	46	nA				ADC[1]_16	SMARTIO13_4
P13.5	GPIO_STD	95	79	57	47	nA				ADC[1]_17	SMARTIO13_5
P13.6	GPIO_STD	96	80	58	48	nA				ADC[1]_18	SMARTIO13_6
P13.7	GPIO_STD	97	81	59	49	nA				ADC[1]_19	SMARTIO13_7
P14.0	GPIO_STD	98	82	60	50	38				ADC[1]_20	SMARTIO14_0

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P14.1	GPIO_STD	99	83	61	51	39				ADC[1]_21	SMARTIO14_1
P14 .2	GPIO_STD	100	84	62	nA	40				ADC[1]_22	SMARTIO14_2
P14 .3	GPIO_STD	101	85	63	nA	nA				ADC[1]_23	SMARTIO14_3
P14.4	GPIO_STD	102	86	nA	nA	nA				ADC[1]_24	SMARTIO14_4
P14.5	GPIO_STD	103	87	nA	nA	nA				ADC[1]_25	SMARTIO14_5
P14 .6	GPIO_STD	104	nA	nA	nA	nA				ADC[1]_26	SMARTIO14_6
P14 .7	GPIO_STD	105	nA	nA	nA	nA				ADC[1]_27	SMARTIO14_7
P15.0	GPIO_STD	106	88	nA	nA	nA				ADC[1]_28	SMARTIO15_0
P15.1	GPIO_STD	107	89	nA	nA	nA				ADC[1]_29	SMARTIO15_1
P15.2	GPIO_STD	108	90	nA	nA	nA				ADC[1]_30	SMARTIO15_2
P15.3	GPIO_STD	109	91	nA	nA	nA				ADC[1]_31	SMARTIO15_3
P16 .0	GPIO_STD	112	92	nA	nA	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P16 .1	GPIO_STD	113	93	nA	nA	nA					
P16 .2	GPIO_STD	114	94	nA	nA	nA					
P16 .3	GPIO_STD	115	nA	nA	nA	nA					
P17 .0	GPIO_STD	116	95	64	nA	nA					SMARTIO17_0
P17.1	GPIO_STD	117	96	65	nA	nA					SMARTIO17_1
P17.2	GPIO_STD	118	97	66	nA	nA					SMARTIO17_2
P17.3	GPIO_STD	119	98	nA	nA	nA					SMARTIO17_3
P17.4	GPIO_STD	120	99	nA	nA	nA					SMARTIO17_4
P17 .5	GPIO_STD	121	nA	nA	nA	nA					SMARTIO17_5
P17 .6	GPIO_STD	122	nA	nA	nA	nA					SMARTIO17_6
P17 .7	GPIO_STD	123	nA	nA	nA	nA					SMARTIO17_7
P18.0	GPIO_STD	124	100	67	52	41				ADC[2]_0	

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P18.1	GPIO_STD	125	101	68	53	42				ADC[2]_1	
P18.2	GPIO_STD	126	102	69	54	nA				ADC[2]_2	
P18.3	GPIO_STD	127	103	70	55	43				ADC[2]_3	
P18.4	GPIO_STD	128	104	71	56	44				ADC[2]_4	
P18.5	GPIO_STD	129	105	72	57	45				ADC[2]_5	
P18.6	GPIO_STD	130	106	73	58	46				ADC[2]_6	
P18 .7	GPIO_STD	131	107	74	59	47				ADC[2]_7	
P19.0	GPIO_STD	134	110	77	62	nA					
P19.1	GPIO_STD	135	111	78	63	nA					
P19.2	GPIO_STD	136	112	79	nA	nA					
P19.3	GPIO_STD	137	113	80	nA	nA					
P19.4	GPIO_STD	138	114	nA	nA	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P20.0	GPIO_STD	139	115	nA	nA	nA					
P20 .1	GPIO_STD	140	116	nA	nA	nA					
P20 .2	GPIO_STD	141	117	nA	nA	nA					
P20.3	GPIO_STD	142	118	nA	nA	nA					
P20 .4	GPIO_STD	143	nA	nA	nA	nA					
P20 .5	GPIO_STD	144	nA	nA	nA	nA					
P20 .6	GPIO_STD	145	nA	nA	nA	nA					
P20 .7	GPIO_STD	146	nA	nA	nA	nA					
P21.0	GPIO_STD	147	119	81	64	50				WCO_IN[6]	
P21.1	GPIO_STD	148	120	82	65	51				WCO_OUT[6]	
P21.2	GPIO_STD	149	121	83	66	52				ECO_IN[6]	
P21.3	GPIO_STD	150	122	84	67	53				ECO_OUT[6]	

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P21.4[7]	GPIO_STD	151	nA	nA	nA	nA				HIBERNATE_WAKEUP[0]	
P21.5	GPIO_STD	157	128	90	nA	nA					
P21 .6	GPIO_STD	158	129	nA	nA	nA					
P21 .7	GPIO_STD	159	nA	nA	nA	nA		RTC_CAL			
P22.0	GPIO_STD	160	130	91	73	59					
P22.1	GPIO_STD	161	131	92	74	nA					
P22.2	GPIO_STD	162	132	93	nA	nA					
P22.3	GPIO_STD	163	133	94	nA	nA					
P22.4	GPIO_STD	164	134	nA	nA	nA					
P22 .5	GPIO_STD	165	135	nA	nA	nA					
P22 .6	GPIO_STD	166	136	nA	nA	nA					
P22 .7	GPIO_STD	167	nA	nA	nA	nA					

（表格续下页……）

表 14 （续）深度睡眠（DS）模式、模拟、智能 I/O [1], [2]下的引脚选择器和备用引脚功能

Name		Package pins					DeepSleep mapping[3]			Analog	Smart IO
	HCon#0[4]	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	GPIO						DS #0[5]	DS #1	DS#2		
P23.0	GPIO_STD	168	137	nA	nA	nA					
P23.1	GPIO_STD	169	138	nA	nA	nA					
P23 .2	GPIO_STD	170	nA	nA	nA	nA					
P23.3	GPIO_STD	171	139	95	75	60					
P23.4	GPIO_STD	172	140	96	76	61		SWJ_SWO_TDO			
P23.5	GPIO_STD	173	141	97	77	62		SWJ_SWCLK_TCLK			
P23.6	GPIO_STD	174	142	98	78	63		SWJ_SWDIO_TMS			
P23.7	GPIO_STD	175	143	99	79	64		SWJ_SWDOE_TDI		HIBERNATE_WAKEUP[1]	
XRES_L		152	123	85	68	54					

1) 有关使用的引脚多路复用器缩写的更多信息，请参见表17。
2) 对于任何标有标识符 (n) 的函数，交流时序仅在相应的组“n”内得到保证。
3) 所有在深度睡眠模式下可用的端口引脚功能在运行模式下也可用。
4) 高速 I/O 矩阵连接 (HCon) 基准请参见 表 13。
5) 深度睡眠排序（DS#0、DS#1、DS#2）对选择任何备用功能没有任何影响；HSIOM 模块处理单独的替换功能属性。
6) 如果振荡器是启用的，则支持振荡器功能（WCO 或 ECO）的 GPIO 引脚必须配置为高阻。
7) 当 VDDD 低于 POR 阈值时，此 I/O 将增加漏电至电压。

12 电源引脚分配

表 15 电源引脚分配

Name	Package					Remarks
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP	
VDDD	55, 48, 16	80, 69, 60	100, 86, 75, 24, 12	144, 124, 108, 35, 18	176, 153, 132, 110, 43, 22	Main digital supply
VSSD	57, 56, 49, 33, 17	71, 70, 61, 41, 21, 1	88, 87, 76, 51, 27, 26, 13, 1	126, 125, 109, 73, 38, 37, 19, 1	155, 154, 133, 111, 89, 46, 45, 23, 1	Main digital ground
VDDIO_1	nA	20	25	36	44	I/O supply for group 1
VDDIO_2	32	40	50	72	88	I/O supply for group 2
VCCD[1)]	58	72	89, 28	127, 39	156, 47	Main regulated supply, driven by internal LDO regulator
VREFH	29	35	44	65	79	High reference voltage for SAR
VREFL	26	32	41	62	76	Low reference voltage for SAR
VDDA	28	34	43	64	78	Main analog supply (for PASS SAR)
VSSA	27	33	42	63	77	Main analog ground

1) V_{CCD} 引脚必须连接在一起，以确保低阻抗连接（参见图 16）。

13 备用功能引脚分配

表 16 激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P0.0	PWM0_18	PWM0_22_N	TC0_18_TR0	TC0_22_TR1		SCB0_RX (0)	SCB7_SDA (2)		LIN1_RX				
P0.1	PWM0_17	PWM0_18_N	TC0_17_TR0	TC0_18_TR1		SCB0_TX (0)	SCB7_SCL (2)		LIN1_TX				
P0.2	PWM0_14	PWM0_17_N	TC0_14_TR0	TC0_17_TR1		SCB0_RTS (0)			LIN1_EN	CAN0_1_TX			
P0.3	PWM0_13	PWM0_14_N	TC0_13_TR0	TC0_14_TR1		SCB0_CTS (0)				CAN0_1_RX			
P1.0	PWM0_12	PWM0_13_N	TC0_12_TR0	TC0_13_TR1	PWM0_H_4								
P1.1	PWM0_11	PWM0_12_N	TC0_11_TR0	TC0_12_TR1	PWM0_H_5								
P1.2	PWM0_10	PWM0_11_N	TC0_10_TR0	TC0_11_TR1	PWM0_H_6							TRIG_IN[0]	
P1.3	PWM0_8	PWM0_10_N	TC0_8_TR0	TC0_10_TR1	PWM0_H_7							TRIG_IN[1]	
P2.0	PWM0_7	PWM0_8_N	TC0_7_TR0	TC0_8_TR1	TC0_H_4_TR0	SCB7_RX (0)		SCB7_MISO (0)	LIN0_RX	CAN0_0_TX		TRIG_IN[2]	
P2.1	PWM0_6	PWM0_7_N	TC0_6_TR0	TC0_7_TR1	TC0_H_5_TR0	SCB7_TX (0)	SCB7_SDA (0)	SCB7_MOSI (0)	LIN0_TX	CAN0_0_RX		TRIG_IN[3]	
P2.2	PWM0_5	PWM0_6_N	TC0_5_TR0	TC0_6_TR1	TC0_H_6_TR0	SCB7_RTS (0)	SCB7_SCL (0)	SCB7_CLK (0)	LIN0_EN			TRIG_IN[4]	

（表格续下页……）

表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P2.3	PWM0_4	PWM0_5_N	TC0_4_TR0	TC0_5_TR1	TC0_H_7_TR0	SCB7_CTS (0)		SCB7_SEL0 (0)	LIN5_RX			TRIG_IN[5]	
P2.4	PWM0_3	PWM0_4_N	TC0_3_TR0	TC0_4_TR1	PWM0_H_4_N			SCB7_SEL1 (0)	LIN5_TX			TRIG_IN[6]	
P2.5	PWM0_2	PWM0_3_N	TC0_2_TR0	TC0_3_TR1	PWM0_H_5_N			SCB7_SEL2 (0)	LIN5_EN			TRIG_IN[7]	
P3.0	PWM0_1	PWM0_2_N	TC0_1_TR0	TC0_2_TR1	PWM0_H_6_N	SCB6_RX (0)		SCB6_MISO (0)		CAN0_3_TX			TRIG_DBG[0]
P3.1	PWM0_0	PWM0_1_N	TC0_0_TR0	TC0_1_TR1	PWM0_H_7_N	SCB6_TX (0)	SCB6_SDA (0)	SCB6_MOSI (0)		CAN0_3_RX			TRIG_DBG[1]
P3.2	PWM0_M_3	PWM0_0_N	TC0_M_3_TR0	TC0_0_TR1	TC0_H_4_TR1	SCB6_RTS (0)	SCB6_SCL (0)	SCB6_CLK (0)					
P3.3	PWM0_M_2	PWM0_M_3_N	TC0_M_2_TR0	TC0_M_3_TR1	TC0_H_5_TR1	SCB6_CTS (0)		SCB6_SEL0 (0)					
P3.4	PWM0_M_1	PWM0_M_2_N	TC0_M_1_TR0	TC0_M_2_TR1	TC0_H_6_TR1			SCB6_SEL1 (0)					
P3.5	PWM0_M_0	PWM0_M_1_N	TC0_M_0_TR0	TC0_M_1_TR1	TC0_H_7_TR1			SCB6_SEL2 (0)					
P4.0	PWM0_4	PWM0_M_0_N	TC0_4_TR0	TC0_M_0_TR1	EXT_MUX[0]_0	SCB5_RX (0)		SCB5_MISO (0)	LIN1_RX			TRIG_IN[10]	
P4.1	PWM0_5	PWM0_4_N	TC0_5_TR0	TC0_4_TR1	EXT_MUX[0]_1	SCB5_TX (0)	SCB5_SDA (0)	SCB5_MOSI (0)	LIN1_TX			TRIG_IN[11]	

（表格续下页……）

表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P4.2	PWM0_6	PWM0_5_N	TC0_6_TR0	TC0_5_TR1	EXT_MUX[0]_2	SCB5_RTS (0)	SCB5_SCL (0)	SCB5_CLK (0)	LIN1_EN			TRIG_IN[12]	
P4.3	PWM0_7	PWM0_6_N	TC0_7_TR0	TC0_6_TR1	EXT_MUX[0]_EN	SCB5_CTS (0)		SCB5_SEL0 (0)		CAN0_1_TX		TRIG_IN[13]	
P4.4	PWM0_8	PWM0_7_N	TC0_8_TR0	TC0_7_TR1				SCB5_SEL1 (0)		CAN0_1_RX			
P5.0	PWM0_9	PWM0_8_N	TC0_9_TR0	TC0_8_TR1				SCB5_SEL2 (0)	LIN7_RX				
P5.1	PWM0_10	PWM0_9_N	TC0_10_TR0	TC0_9_TR1					LIN7_TX				
P5.2	PWM0_11	PWM0_10_N	TC0_11_TR0	TC0_10_TR1					LIN7_EN				
P5.3	PWM0_12	PWM0_11_N	TC0_12_TR0	TC0_11_TR1					LIN2_RX				
P5.4	PWM0_13	PWM0_12_N	TC0_13_TR0	TC0_12_TR1					LIN2_TX				
P5.5	PWM0_14	PWM0_13_N	TC0_14_TR0	TC0_13_TR1					LIN2_EN				
P6.0	PWM0_M_0	PWM0_14_N	TC0_M_0_TR0	TC0_14_TR1		SCB4_RX (0)		SCB4_MISO (0)	LIN3_RX				
P6.1	PWM0_0	PWM0_M_0_N	TC0_0_TR0	TC0_M_0_TR1		SCB4_TX (0)	SCB4_SDA (0)	SCB4_MOSI (0)	LIN3_TX				

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P6.2	PWM0_M_1	PWM0_0_N	TC0_M_1_TR0	TC0_0_TR1		SCB4_RTS (0)	SCB4_SCL (0)	SCB4_CLK (0)	LIN3_EN	CAN0_2_TX			
P6.3	PWM0_1	PWM0_M_1_N	TC0_1_TR0	TC0_M_1_TR1		SCB4_CTS (0)		SCB4_SEL0 (0)	LIN4_RX	CAN0_2_RX			CAL_SUP_NZ
P6.4	PWM0_M_2	PWM0_1_N	TC0_M_2_TR0	TC0_1_TR1				SCB4_SEL1 (0)	LIN4_TX				
P6.5	PWM0_2	PWM0_M_2_N	TC0_2_TR0	TC0_M_2_TR1				SCB4_SEL2 (0)	LIN4_EN				
P6.6	PWM0_M_3	PWM0_2_N	TC0_M_3_TR0	TC0_2_TR1				SCB4_SEL3 (0)				TRIG_IN[8]	
P6.7	PWM0_3	PWM0_M_3_N	TC0_3_TR0	TC0_M_3_TR1								TRIG_IN[9]	
P7.0	PWM0_M_4	PWM0_3_N	TC0_M_4_TR0	TC0_3_TR1		SCB5_RX (1)		SCB5_MISO (1)	LIN4_RX		CXPI0_RX		
P7.1	PWM0_15	PWM0_M_4_N	TC0_15_TR0	TC0_M_4_TR1		SCB5_TX (1)	SCB5_SDA (1)	SCB5_MOSI (1)	LIN4_TX		CXPI0_TX		
P7.2	PWM0_M_5	PWM0_15_N	TC0_M_5_TR0	TC0_15_TR1		SCB5_RTS (1)	SCB5_SCL (1)	SCB5_CLK (1)	LIN4_EN		CXPI0_EN		
P7.3	PWM0_16	PWM0_M_5_N	TC0_16_TR0	TC0_M_5_TR1		SCB5_CTS (1)		SCB5_SEL0 (1)					
P7.4	PWM0_M_6	PWM0_16_N	TC0_M_6_TR0	TC0_16_TR1				SCB5_SEL1 (1)					

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P7.5	PWM0_17	PWM0_M_6_N	TC0_17_TR0	TC0_M_6_TR1				SCB5_SEL2 (1)	LIN10_RX				
P7.6	PWM0_M_7	PWM0_17_N	TC0_M_7_TR0	TC0_17_TR1					LIN10_TX			TRIG_IN[16]	
P7.7	PWM0_18	PWM0_M_7_N	TC0_18_TR0	TC0_M_7_TR1					LIN10_EN			TRIG_IN[17]	
P8.0	PWM0_19	PWM0_18_N	TC0_19_TR0	TC0_18_TR1					LIN2_RX	CAN0_0_TX			
P8.1	PWM0_20	PWM0_19_N	TC0_20_TR0	TC0_19_TR1					LIN2_TX	CAN0_0_RX		TRIG_IN[14]	
P8.2	PWM0_21	PWM0_20_N	TC0_21_TR0	TC0_20_TR1					LIN2_EN			TRIG_IN[15]	
P8.3	PWM0_22	PWM0_21_N	TC0_22_TR0	TC0_21_TR1									TRIG_DBG[0]
P8.4	PWM0_23	PWM0_22_N	TC0_23_TR0	TC0_22_TR1									TRIG_DBG[1]
P9.0	PWM0_24	PWM0_23_N	TC0_24_TR0	TC0_23_TR1									
P9.1	PWM0_25	PWM0_24_N	TC0_25_TR0	TC0_24_TR1									
P9.2	PWM0_26	PWM0_25_N	TC0_26_TR0	TC0_25_TR1									

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P9.3	PWM0_27	PWM0_26_N	TC0_27_TR0	TC0_26_TR1									
P10.0	PWM0_28	PWM0_27_N	TC0_28_TR0	TC0_27_TR1		SCB4_RX (1)		SCB4_MISO (1)				TRIG_IN[18]	
P10.1	PWM0_29	PWM0_28_N	TC0_29_TR0	TC0_28_TR1		SCB4_TX (1)	SCB4_SDA (1)	SCB4_MOSI (1)				TRIG_IN[19]	
P10.2	PWM0_30	PWM0_29_N	TC0_30_TR0	TC0_29_TR1		SCB4_RTS (1)	SCB4_SCL (1)	SCB4_CLK (1)	LIN8_RX				
P10.3	PWM0_31	PWM0_30_N	TC0_31_TR0	TC0_30_TR1		SCB4_CTS (1)		SCB4_SEL0 (1)	LIN8_TX				
P10.4	PWM0_32	PWM0_31_N	TC0_32_TR0	TC0_31_TR1				SCB4_SEL1 (1)	LIN8_EN				
P10.5	PWM0_33	PWM0_32_N	TC0_33_TR0	TC0_32_TR1				SCB4_SEL2 (1)			CXPI0_RX		
P10.6	PWM0_34	PWM0_33_N	TC0_34_TR0	TC0_33_TR1							CXPI0_TX		
P10.7	PWM0_35	PWM0_34_N	TC0_35_TR0	TC0_34_TR1							CXPI0_EN		
P11.0													
P11.1													

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P11.2													
P12.0	PWM0_36	PWM0_35_N	TC0_36_TR0	TC0_35_TR1						CAN0_2_TX		TRIG_IN[20]	
P12.1	PWM0_37	PWM0_36_N	TC0_37_TR0	TC0_36_TR0					LIN6_EN	CAN0_2_RX		TRIG_IN[11]	
P12.2	PWM0_38	PWM0_37_N	TC0_38_TR0	TC0_37_TR1	EXT_MUX[0]_EN				LIN6_RX				
P12.3	PWM0_39	PWM0_38_N	TC0_39_TR0	TC0_38_TR1	EXT_MUX[0]_0				LIN6_TX				
P12.4	PWM0_40	PWM0_39_N	TC0_40_TR0	TC0_39_TR1	EXT_MUX[1]_1								
P12.5	PWM0_41	PWM0_40_N	TC0_41_TR0	TC0_40_TR1	EXT_MUX[1]_2								
P12.6	PWM0_42	PWM0_41_N	TC0_42_TR0	TC0_41_TR1									
P12.7	PWM0_43	PWM0_42_N	TC0_43_TR0	TC0_42_TR1									
P13.0	PWM0_M_8	PWM0_43_N	TC0_M_8_TR0	TC0_43_TR1	EXT_MUX[2]_0	SCB3_RX (0)		SCB3_MISO (0)	LIN3_RX		CXPI1_RX		
P13.1	PWM0_44	PWM0_M_8_N	TC0_44_TR0	TC0_M_8_TR1	EXT_MUX[2]_1	SCB3_TX (0)	SCB3_SDA (0)	SCB3_MOSI (0)	LIN3_TX		CXPI1_TX		

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P13.2	PWM0_M_9	PWM0_44_N	TC0_M_9_TR0	TC0_44_TR1	EXT_MUX[2]_2	SCB3_RTS (0)	SCB3_SCL (0)	SCB3_CLK (0)	LIN3_EN		CXPI1_EN		
P13.3	PWM0_45	PWM0_M_9_N	TC0_45_TR0	TC0_M_9_TR1	EXT_MUX[2]_EN	SCB3_CTS (0)		SCB3_SEL0 (0)					
P13.4	PWM0_M_10	PWM0_45_N	TC0_M_10_TR0	TC0_45_TR1	PWM0_H_4			SCB3_SEL1 (0)	LIN8_RX				
P13.5	PWM0_46	PWM0_M_10_N	TC0_46_TR0	TC0_M_10_TR1	PWM0_H_4_N			SCB3_SEL2 (0)	LIN8_TX		CXPI2_RX		
P13.6	PWM0_M_11	PWM0_46_N	TC0_M_11_TR0	TC0_46_TR1	PWM0_H_5			SCB3_SEL3 (0)	LIN8_EN		CXPI2_TX	TRIG_IN[22]	
P13.7	PWM0_47	PWM0_M_11_N	TC0_47_TR0	TC0_M_11_TR1	PWM0_H_5_N						CXPI2_EN	TRIG_IN[23]	
P14.0	PWM0_48	PWM0_47_N	TC0_48_TR0	TC0_47_TR1	PWM0_H_6	SCB2_RX (0)		SCB2_MISO (0)		CAN1_0_TX			
P14.1	PWM0_49	PWM0_48_N	TC0_49_TR0	TC0_48_TR1	PWM0_H_6_N	SCB2_TX (0)	SCB2_SDA (0)	SCB2_MOSI (0)		CAN1_0_RX			
P14.2	PWM0_50	PWM0_49_N	TC0_50_TR0	TC0_49_TR1	PWM0_H_7	SCB2_RTS (0)	SCB2_SCL (0)	SCB2_CLK (0)	LIN6_RX				
P14.3	PWM0_51	PWM0_50_N	TC0_51_TR0	TC0_50_TR1	PWM0_H_7_N	SCB2_CTS (0)		SCB2_SEL0 (0)	LIN6_TX				
P14.4	PWM0_52	PWM0_51_N	TC0_52_TR0	TC0_51_TR1	TC0_H_4_TR0			SCB2_SEL1 (0)	LIN6_EN				

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P14.5	PWM0_53	PWM0_52_N	TC0_53_TR0	TC0_52_TR1	TC0_H_4_TR1			SCB2_SEL2 (0)			CXPI2_RX		
P14.6	PWM0_54	PWM0_53_N	TC0_54_TR0	TC0_53_TR1	TC0_H_5_TR0						CXPI2_TX	TRIG_IN[24]	
P14.7	PWM0_55	PWM0_54_N	TC0_55_TR0	TC0_54_TR1	TC0_H_5_TR1						CXPI2_EN	TRIG_IN[25]	
P15.0	PWM0_56	PWM0_55_N	TC0_56_TR0	TC0_55_TR1	TC0_H_6_TR0					CAN1_3_TX	CXPI1_RX		
P15.1	PWM0_57	PWM0_56_N	TC0_57_TR0	TC0_56_TR1	TC0_H_6_TR1					CAN1_3_RX	CXPI1_TX		
P15.2	PWM0_58	PWM0_57_N	TC0_58_TR0	TC0_57_TR1	TC0_H_7_TR0						CXPI1_EN		
P15.3	PWM0_59	PWM0_58_N	TC0_59_TR0	TC0_58_TR1	TC0_H_7_TR1								
P16.0	PWM0_60	PWM0_59_N	TC0_60_TR0	TC0_59_TR1	PWM0_H_0				LIN11_RX				
P16.1	PWM0_61	PWM0_60_N	TC0_61_TR0	TC0_60_TR1	PWM0_H_0_N				LIN11_TX				
P16.2	PWM0_62	PWM0_61_N	TC0_62_TR0	TC0_61_TR1	PWM0_H_1				LIN11_EN				
P16.3	PWM0_62	PWM0_62_N	TC0_62_TR0	TC0_62_TR1	PWM0_H_1_N								

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P17.0	PWM0_61	PWM0_62_N	TC0_61_TR0	TC0_62_TR1						CAN1_1_TX			
P17.1	PWM0_60	PWM0_61_N	TC0_60_TR0	TC0_61_TR1	PWM0_H_2	SCB3_RX (1)		SCB3_MISO (1)		CAN1_1_RX			
P17.2	PWM0_59	PWM0_60_N	TC0_59_TR0	TC0_60_TR1	PWM0_H_2_N	SCB3_TX (1)	SCB3_SDA (1)	SCB3_MOSI (1)					
P17.3	PWM0_58	PWM0_59_N	TC0_58_TR0	TC0_59_TR1	PWM0_H_3	SCB3_RTS (1)	SCB3_SCL (1)	SCB3_CLK (1)				TRIG_IN[26]	
P17.4	PWM0_57	PWM0_58_N	TC0_57_TR0	TC0_58_TR1	PWM0_H_3_N	SCB3_CTS (1)		SCB3_SEL0 (1)				TRIG_IN[27]	
P17.5	PWM0_56	PWM0_57_N	TC0_56_TR0	TC0_57_TR1				SCB3_SEL1 (1)					
P17.6	PWM0_M_4	PWM0_56_N	TC0_M_4_TR0	TC0_56_TR1				SCB3_SEL2 (1)					
P17.7	PWM0_M_5	PWM0_M_4_N	TC0_M_5_TR0	TC0_M_4_TR1									
P18.0	PWM0_M_6	PWM0_M_5_N	TC0_M_6_TR0	TC0_M_5_TR1	PWM0_H_0	SCB1_RX (0)		SCB1_MISO (0)					FAULT_OUT_0
P18.1	PWM0_M_7	PWM0_M_6_N	TC0_M_7_TR0	TC0_M_6_TR1	PWM0_H_0_N	SCB1_TX (0)	SCB1_SDA (0)	SCB1_MOSI (0)					FAULT_OUT_1
P18.2	PWM0_55	PWM0_M_7_N	TC0_55_TR0	TC0_M_7_TR1	PWM0_H_1	SCB1_RTS (0)	SCB1_SCL (0)	SCB1_CLK (0)					

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P18.3	PWM0_54	PWM0_55_N	TC0_54_TR0	TC0_55_TR1	PWM0_H_1_N	SCB1_CTS (0)		SCB1_SEL0 (0)					TRACE_CLOCK (0)
P18.4	PWM0_53	PWM0_54_N	TC0_53_TR0	TC0_54_TR1	PWM0_H_2			SCB1_SEL1 (0)					TRACE_DATA_0 (0)
P18.5	PWM0_52	PWM0_53_N	TC0_52_TR0	TC0_53_TR1	PWM0_H_2_N			SCB1_SEL2 (0)					TRACE_DATA_1 (0)
P18.6	PWM0_51	PWM0_52_N	TC0_51_TR0	TC0_52_TR1	PWM0_H_3			SCB1_SEL3 (0)		CAN1_2_TX			TRACE_DATA_2 (0)
P18.7	PWM0_50	PWM0_51_N	TC0_50_TR0	TC0_51_TR1	PWM0_H_3_N					CAN1_2_RX			TRACE_DATA_3 (0)
P19.0	PWM0_M_3	PWM0_50_N	TC0_M_3_TR0	TC0_50_TR1	TC0_H_0_TR0	SCB2_RX (1)		SCB2_MISO (1)		CAN1_3_TX			FAULT_OUT_2
P19.1	PWM0_26	PWM0_M_3_N	TC0_26_TR0	TC0_M_3_TR1	TC0_H_0_TR1	SCB2_TX (1)	SCB2_SDA (1)	SCB2_MOSI (1)		CAN1_3_RX	CXPI3_RX		FAULT_OUT_3
P19.2	PWM0_27	PWM0_26_N	TC0_27_TR0	TC0_26_TR1	TC0_H_1_TR0	SCB2_RTS (1)	SCB2_SCL (1)	SCB2_CLK (1)			CXPI3_TX	TRIG_IN[28]	
P19.3	PWM0_28	PWM0_27_N	TC0_28_TR0	TC0_27_TR1	TC0_H_1_TR1	SCB2_CTS (1)		SCB2_SEL0 (1)			CXPI3_EN	TRIG_IN[29]	
P19.4	PWM0_29	PWM0_28_N	TC0_29_TR0	TC0_28_TR1	TC0_H_2_TR0			SCB2_SEL1 (1)					
P20.0	PWM0_30	PWM0_29_N	TC0_30_TR0	TC0_29_TR1	TC0_H_2_TR1			SCB2_SEL2 (1)	LIN5_RX				

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P20.1	PWM0_49	PWM0_30_N	TC0_49_TR0	TC0_30_TR1	TC0_H_0_TR0				LIN5_TX				
P20.2	PWM0_48	PWM0_49_N	TC0_48_TR0	TC0_49_TR1	TC0_H_3_TR1				LIN5_EN				
P20.3	PWM0_47	PWM0_48_N	TC0_47_TR0	TC0_48_TR1		SCB1_RX (1)		SCB1_MISO (1)		CAN1_2_TX			
P20.4	PWM0_46	PWM0_47_N	TC0_46_TR0	TC0_47_TR1		SCB1_TX (1)	SCB1_SDA (1)	SCB1_MOSI (1)		CAN1_2_RX			
P20.5	PWM0_45	PWM0_46_N	TC0_45_TR0	TC0_46_TR1		SCB1_RTS (1)	SCB1_SCL (1)	SCB1_CLK (1)			CXPI3_RX		
P20.6	PWM0_44	PWM0_45_N	TC0_44_TR0	TC0_45_TR1		SCB1_CTS (1)		SCB1_SEL0 (1)			CXPI3_TX		
P20.7	PWM0_43	PWM0_44_N	TC0_43_TR0	TC0_44_TR1				SCB1_SEL1 (1)			CXPI3_EN		
P21.0	PWM0_42	PWM0_43_N	TC0_42_TR0	TC0_43_TR1				SCB1_SEL2 (1)					
P21.1	PWM0_41	PWM0_42_N	TC0_41_TR0	TC0_42_TR1									
P21.2	PWM0_40	PWM0_41_N	TC0_40_TR0	TC0_41_TR1								EXT_CLK	TRIG_DBG[1]
P21.3	PWM0_39	PWM0_40_N	TC0_39_TR0	TC0_40_TR1									

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表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P21.4	PWM0_38	PWM0_39_N	TC0_38_TR0	TC0_39_TR1									
P21.5	PWM0_37	PWM0_38_N	TC0_37_TR0	TC0_38_TR1					LIN0_RX				
P21.6	PWM0_36	PWM0_37_N	TC0_36_TR0	TC0_37_TR1					LIN0_TX				
P21.7	PWM0_35	PWM0_36_N	TC0_35_TR0	TC0_36_TR0					LIN0_EN				CAL_SUP_NZ
P22.0	PWM0_34	PWM0_35_N	TC0_34_TR0	TC0_35_TR1		SCB6_RX (1)		SCB6_MISO (1)		CAN1_1_TX			TRACE_DATA_0 (1)
P22.1	PWM0_33	PWM0_34_N	TC0_33_TR0	TC0_34_TR1		SCB6_TX (1)	SCB6_SDA (1)	SCB6_MOSI (1)		CAN1_1_RX			TRACE_DATA_1 (1)
P22.2	PWM0_32	PWM0_33_N	TC0_32_TR0	TC0_33_TR1		SCB6_RTS (1)	SCB6_SCL (1)	SCB6_CLK (1)					TRACE_DATA_2 (1)
P22.3	PWM0_31	PWM0_32_N	TC0_31_TR0	TC0_32_TR1		SCB6_CTS (1)		SCB6_SEL0 (1)					TRACE_DATA_3 (1)
P22.4	PWM0_30	PWM0_31_N	TC0_30_TR0	TC0_31_TR1				SCB6_SEL1 (1)					TRACE_CLOCK (1)
P22.5	PWM0_29	PWM0_30_N	TC0_29_TR0	TC0_30_TR1				SCB6_SEL2 (1)	LIN7_RX				
P22.6	PWM0_28	PWM0_29_N	TC0_28_TR0	TC0_29_TR1					LIN7_TX				

（表格续下页……）

表 16 （续）激活模式下的备用引脚功能 [1], [2]

Name	Active mapping												
	HCon#8 [3]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#26	HCon#27
	ACT#0 [4]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#14	ACT#15
P22.7	PWM0_27	PWM0_28_N	TC0_27_TR0	TC0_28_TR1					LIN7_EN				
P23.0	PWM0_M_8	PWM0_27_N	TC0_M_8_TR0	TC0_27_TR1		SCB7_RX (1)		SCB7_MISO (1)		CAN1_0_TX			FAULT_OUT_0
P23.1	PWM0_M_9	PWM0_M_8_N	TC0_M_9_TR0	TC0_M_8_TR1		SCB7_TX (1)	SCB7_SDA (1)	SCB7_MOSI (1)		CAN1_0_RX			FAULT_OUT_1
P23.2	PWM0_M_10	PWM0_M_9_N	TC0_M_10_TR0	TC0_M_9_TR1		SCB7_RTS (1)	SCB7_SCL (1)	SCB7_CLK (1)					FAULT_OUT_2
P23.3	PWM0_M_11	PWM0_M_10_N	TC0_M_11_TR0	TC0_M_10_TR1		SCB7_CTS (1)		SCB7_SEL0 (1)				TRIG_IN[30]	FAULT_OUT_3
P23.4	PWM0_25	PWM0_M_11_N	TC0_25_TR0	TC0_M_11_TR1				SCB7_SEL1 (1)				TRIG_IN[31]	TRIG_DBG[0]
P23.5	PWM0_24	PWM0_25_N	TC0_24_TR0	TC0_25_TR1				SCB7_SEL2 (1)	LIN9_RX				
P23.6	PWM0_23	PWM0_24_N	TC0_23_TR0	TC0_24_TR1					LIN9_TX				
P23.7	PWM0_22	PWM0_23_N	TC0_22_TR0	TC0_23_TR1					LIN9_EN			EXT_CLK	CAL_SUP_NZ

1) 有关使用的引脚多路复用器缩写的更多信息，请参见表 17。
2) 对于任何标有标识符 (n) 的函数，交流时序仅在相应的组“n”内得到保证。
3) High Speed I/O 矩阵连接 (HCon) 基准请参见表 13。
4) 运行模式顺序（ACT#0、ACT#1 等）对选择任何备用功能没有任何影响；HSIOM 模块将处理单独的替换功能分配。

14 引脚多路复用器描述

表 17 引脚多路复用器描述

Sl. No.	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_M_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number
9	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
10	SCBx_RX	SCB	UART Receive, x-SCB block
11	SCBx_TX	SCB	UART Transmit, x-SCB block
12	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
13	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
14	SCBx_SDA	SCB	I2C Data line, x-SCB block
15	SCBx_SCL	SCB	I2C Clock line, x-SCB block
16	SCBx_MISO	SCB	SPI Master Input Slave Output, x-SCB block
17	SCBx_MOSI	SCB	SPI Master Output Slave Input, x-SCB block
18	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
19	SCBx_SELy	SCB	SPI Slave Select, x-SCB block, y-select line
20	LINx_RX	LIN	LIN Receive line, x-LIN block
21	LINx_TX	LIN	LIN Transmit line, x-LIN block
22	LINx_EN	LIN	LIN Enable line, x-LIN block
23	CXPI0_RX	CXPI	CXPI Receive line, x-CXPI block
24	CXPI0_TX	CXPI	CXPI Transmit line, x-CXPI block
25	CXPI0_EN	CXPI	CXPI Enable line, x-CXPI block

（表格续下页……）

表 17 （续）引脚多路复用器描述

Sl. No.	Pin	Module	Description
26	CANx_y_TX	CAN FD	CAN Transmit line, x-CAN block, y-channel number
27	CANx_y_RX	CAN FD	CAN Receive line, x-CAN block, y-channel number
28	CAL_SUP_NZ	CPUSS	ETAS Calibration support line
29	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
30	TRACE_DATA_x	SRSS	Trace data out line x-0 to 3
31	TRACE_CLOCK	SRSS	Trace clock line
32	RTC_CAL	SRSS RTC	RTC calibration clock input
33	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
34	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
35	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
36	SWJ_SWDIO_TM S	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/ Output)
37	SWJ_SWDOE_TDI	SRSS	JTAG Test data input
38	HIBERNATE_WAKEUP[x]	SRSS	Hibernate wakeup line x-0 to 1
39	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
40	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
41	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
42	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
43	EXT_CLK	SRSS	External clock input or output
44	TRIG_IN[x]	HSIOM	HSIOM_IO_INPUT[x] of trigger inputs, x-0 to 47
45	TRIG_DBG[x]	HSIOM	HSIOM_IO_OUTPUT[x] of trigger outputs, x-0 to 1
46	WCO_IN	SRSS	Watch crystal oscillator input
47	WCO_OUT	SRSS	Watch crystal oscillator output
48	ECO_IN	SRSS	External crystal oscillator input
49	ECO_OUT	SRSS	External crystal oscillator output

15 中断和唤醒分配

表 18 外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS inter process communication interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS inter process communication interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS inter process communication interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS inter process communication interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS inter process communication interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS inter process communication interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS inter process communication interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS inter process communication interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS fault structure #0 interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS fault structure #1 interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS fault structure #2 interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS fault structure #3 interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain Interrupt
13	srss_interrupt_mcwdt_0_IRQn	DeepSleep	Multi-counter watchdog timer #0 interrupt
14	srss_interrupt_mcwdt_1_IRQn	DeepSleep	Multi-counter watchdog timer #1 interrupt
15	srss_interrupt_wdt_IRQn	DeepSleep	Hardware watchdog timer interrupt
16	srss_interrupt_IRQn	DeepSleep	Other combined interrupts for SRSS (LVD, CLK_CAL)
17	scb_0_interrupt_IRQn	DeepSleep	Serial communication block #0 (DeepSleep capable)
18	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event gen DeepSleep domain interrupt
19	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Supply (V_{DDIO}, V_{DDA}, V_{DDD}) state change Interrupt
20	ioss_interrupt_gpio_IRQn	DeepSleep	Consolidated interrupt for GPIO_STD and GPIO_ENH, All ports
21	ioss_interrupts_gpio_0_IRQn	DeepSleep	GPIO_ENH Port #0 interrupt
22	ioss_interrupts_gpio_1_IRQn	DeepSleep	GPIO_STD Port #1 interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
23	ioss_interrupts_gpio_2_IRQn	DeepSleep	GPIO_STD Port #2 interrupt
24	ioss_interrupts_gpio_3_IRQn	DeepSleep	GPIO_STD Port #3 interrupt
25	ioss_interrupts_gpio_4_IRQn	DeepSleep	GPIO_STD Port #4 interrupt
26	ioss_interrupts_gpio_5_IRQn	DeepSleep	GPIO_STD Port #5 interrupt
27	ioss_interrupts_gpio_6_IRQn	DeepSleep	GPIO_STD Port #6 interrupt
28	ioss_interrupts_gpio_7_IRQn	DeepSleep	GPIO_STD Port #7 interrupt
29	ioss_interrupts_gpio_8_IRQn	DeepSleep	GPIO_STD Port #8 interrupt
30	ioss_interrupts_gpio_9_IRQn	DeepSleep	GPIO_STD Port #9 interrupt
31	ioss_interrupts_gpio_10_IRQn	DeepSleep	GPIO_STD Port #10 interrupt
32	ioss_interrupts_gpio_11_IRQn	DeepSleep	GPIO_STD Port #11 interrupt
33	ioss_interrupts_gpio_12_IRQn	DeepSleep	GPIO_STD Port #12 interrupt
34	ioss_interrupts_gpio_13_IRQn	DeepSleep	GPIO_STD Port #13 interrupt
35	ioss_interrupts_gpio_14_IRQn	DeepSleep	GPIO_STD Port #14 interrupt
36	ioss_interrupts_gpio_15_IRQn	DeepSleep	GPIO_STD Port #15 interrupt
37	ioss_interrupts_gpio_16_IRQn	DeepSleep	GPIO_STD Port #16 interrupt
38	ioss_interrupts_gpio_17_IRQn	DeepSleep	GPIO_STD Port #17 interrupt
39	ioss_interrupts_gpio_18_IRQn	DeepSleep	GPIO_STD Port #18 interrupt
40	ioss_interrupts_gpio_19_IRQn	DeepSleep	GPIO_STD Port #19 interrupt
41	ioss_interrupts_gpio_20_IRQn	DeepSleep	GPIO_STD Port #20 interrupt
42	ioss_interrupts_gpio_21_IRQn	DeepSleep	GPIO_STD Port #21 interrupt
43	ioss_interrupts_gpio_22_IRQn	DeepSleep	GPIO_STD Port #22 interrupt
44	ioss_interrupts_gpio_23_IRQn	DeepSleep	GPIO_STD Port #23 interrupt
45	cpuss_interrupt_crypto_IRQn	Active	Crypto accelerator interrupt
46	cpuss_interrupt_fm_IRQn	Active	Flash macro Interrupt
47	cpuss_interrupts_cm4_fp_IRQn	Active	CM4 floating point operation fault
48	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross trigger interface) #0
49	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI #1
50	cpuss_interrupts_cm4_cti_0_IRQn	Active	CM4 CTI #0
51	cpuss_interrupts_cm4_cti_1_IRQn	Active	CM4 CTI #1
52	evtgen_0_interrupt_IRQn	Active	Event Generator Active domain interrupt

（表格续下页……）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
53	canfd_0_interrupt0_IRQn	Active	CAN0, Consolidated interrupt #0 for all three channels
54	canfd_0_interrupt1_IRQn	Active	CAN0, Consolidated interrupt #1 for all three channels
55	canfd_1_interrupt0_IRQn	Active	CAN1, Consolidated interrupt #0 for all three channels
56	canfd_1_interrupt1_IRQn	Active	CAN1, Consolidated interrupt #1 for all three channels
57	canfd_0_interrupts0_0_IRQn	Active	CAN0, Interrupt #0, Channel #0
58	canfd_0_interrupts0_1_IRQn	Active	CAN0, Interrupt #0, Channel #1
59	canfd_0_interrupts0_2_IRQn	Active	CAN0, Interrupt #0, Channel #2
60	canfd_0_interrupts0_3_IRQn	Active	CAN0, Interrupt #0, Channel #3
61	canfd_0_interrupts1_0_IRQn	Active	CAN0, Interrupt #1, Channel #0
62	canfd_0_interrupts1_1_IRQn	Active	CAN0, Interrupt #1, Channel #1
63	canfd_0_interrupts1_2_IRQn	Active	CAN0, Interrupt #1, Channel #2
64	canfd_0_interrupts1_3_IRQn	Active	CAN0, Interrupt #1, Channel #3
65	canfd_1_interrupts0_0_IRQn	Active	CAN1, Interrupt #0, Channel #0
66	canfd_1_interrupts0_1_IRQn	Active	CAN1, Interrupt #0, Channel #1
67	canfd_1_interrupts0_2_IRQn	Active	CAN1, Interrupt #0, Channel #2
68	canfd_1_interrupts0_3_IRQn	Active	CAN1, Interrupt #0, Channel #3
69	canfd_1_interrupts1_0_IRQn	Active	CAN1, Interrupt #1, Channel #0
70	canfd_1_interrupts1_1_IRQn	Active	CAN1, Interrupt #1, Channel #1
71	canfd_1_interrupts1_2_IRQn	Active	CAN1, Interrupt #1, Channel #2
72	canfd_1_interrupts1_3_IRQn	Active	CAN1, Interrupt #1, Channel #1
73	lin_0_interrupts_0_IRQn	Active	LIN0, Channel #0 Interrupt
74	lin_0_interrupts_1_IRQn	Active	LIN0, Channel #1 Interrupt
75	lin_0_interrupts_2_IRQn	Active	LIN0, Channel #2 Interrupt
76	lin_0_interrupts_3_IRQn	Active	LIN0, Channel #3 Interrupt
77	lin_0_interrupts_4_IRQn	Active	LIN0, Channel #4 Interrupt
78	lin_0_interrupts_5_IRQn	Active	LIN0, Channel #5 Interrupt
79	lin_0_interrupts_6_IRQn	Active	LIN0, Channel #6 Interrupt
80	lin_0_interrupts_7_IRQn	Active	LIN0, Channel #7 Interrupt
81	lin_0_interrupts_8_IRQn	Active	LIN0, Channel #8 Interrupt
82	lin_0_interrupts_9_IRQn	Active	LIN0, Channel #9 Interrupt

（表格续下页……）

15 Interrupts and wake-up assignments

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
83	lin_0_interrupts_10_IRQn	Active	LIN0, Channel #10 Interrupt
84	lin_0_interrupts_11_IRQn	Active	LIN0, Channel #11 Interrupt
85	cxpi_0_interrupts_0_IRQn	Active	CXPI0 Channel #0 Interrupt
86	cxpi_0_interrupts_1_IRQn	Active	CXPI0 Channel #1 Interrupt
87	cxpi_0_interrupts_2_IRQn	Active	CXPI0 Channel #2 Interrupt
88	cxpi_0_interrupts_3_IRQn	Active	CXPI0 Channel #3 Interrupt
89	scb_1_interrupt_IRQn	Active	SCB1 Interrupt
90	scb_2_interrupt_IRQn	Active	SCB2 Interrupt
91	scb_3_interrupt_IRQn	Active	SCB3 Interrupt
92	scb_4_interrupt_IRQn	Active	SCB4 Interrupt
93	scb_5_interrupt_IRQn	Active	SCB5 Interrupt
94	scb_6_interrupt_IRQn	Active	SCB6 Interrupt
95	scb_7_interrupt_IRQn	Active	SCB7 Interrupt
96	pass_0_interrupts_sar_0_IRQn	Active	SAR0, Logical channel #0 interrupt
97	pass_0_interrupts_sar_1_IRQn	Active	SAR0, Logical channel #1 interrupt
98	pass_0_interrupts_sar_2_IRQn	Active	SAR0, Logical channel #2 interrupt
99	pass_0_interrupts_sar_3_IRQn	Active	SAR0, Logical channel #3 interrupt
100	pass_0_interrupts_sar_4_IRQn	Active	SAR0, Logical channel #4 interrupt
101	pass_0_interrupts_sar_5_IRQn	Active	SAR0, Logical channel #5 interrupt
102	pass_0_interrupts_sar_6_IRQn	Active	SAR0, Logical channel #6 interrupt
103	pass_0_interrupts_sar_7_IRQn	Active	SAR0, Logical channel #7 interrupt
104	pass_0_interrupts_sar_8_IRQn	Active	SAR0, Logical channel #8 interrupt
105	pass_0_interrupts_sar_9_IRQn	Active	SAR0, Logical channel #9 interrupt
106	pass_0_interrupts_sar_10_IRQn	Active	SAR0, Logical channel #10 interrupt
107	pass_0_interrupts_sar_11_IRQn	Active	SAR0, Logical channel #11 interrupt
108	pass_0_interrupts_sar_12_IRQn	Active	SAR0, Logical channel #12 interrupt
109	pass_0_interrupts_sar_13_IRQn	Active	SAR0, Logical channel #13 interrupt
110	pass_0_interrupts_sar_14_IRQn	Active	SAR0, Logical channel #14 interrupt
111	pass_0_interrupts_sar_15_IRQn	Active	SAR0, Logical channel #15 interrupt
112	pass_0_interrupts_sar_16_IRQn	Active	SAR0, Logical channel #16 interrupt
113	pass_0_interrupts_sar_17_IRQn	Active	SAR0, Logical channel #17 interrupt
114	pass_0_interrupts_sar_18_IRQn	Active	SAR0, Logical channel #18 interrupt
115	pass_0_interrupts_sar_19_IRQn	Active	SAR0, Logical channel #19 interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
116	pass_0_interrupts_sar_20_IRQn	Active	SAR0, Logical channel #20 interrupt
117	pass_0_interrupts_sar_21_IRQn	Active	SAR0, Logical channel #21 interrupt
118	pass_0_interrupts_sar_22_IRQn	Active	SAR0, Logical channel #22 interrupt
119	pass_0_interrupts_sar_23_IRQn	Active	SAR0, Logical channel #23 interrupt
120	pass_0_interrupts_sar_32_IRQn	Active	SAR1, Logical channel #0 interrupt
121	pass_0_interrupts_sar_33_IRQn	Active	SAR1, Logical channel #1 interrupt
122	pass_0_interrupts_sar_34_IRQn	Active	SAR1, Logical channel #2 interrupt
123	pass_0_interrupts_sar_35_IRQn	Active	SAR1, Logical channel #3 interrupt
124	pass_0_interrupts_sar_36_IRQn	Active	SAR1, Logical channel #4 interrupt
125	pass_0_interrupts_sar_37_IRQn	Active	SAR1, Logical channel #5 interrupt
126	pass_0_interrupts_sar_38_IRQn	Active	SAR1, Logical channel #6 interrupt
127	pass_0_interrupts_sar_39_IRQn	Active	SAR1, Logical channel #7 interrupt
128	pass_0_interrupts_sar_40_IRQn	Active	SAR1, Logical channel #8 interrupt
129	pass_0_interrupts_sar_41_IRQn	Active	SAR1, Logical channel #9 interrupt
130	pass_0_interrupts_sar_42_IRQn	Active	SAR1, Logical channel #10 interrupt
131	pass_0_interrupts_sar_43_IRQn	Active	SAR1, Logical channel #11 interrupt
132	pass_0_interrupts_sar_44_IRQn	Active	SAR1, Logical channel #12 interrupt
133	pass_0_interrupts_sar_45_IRQn	Active	SAR1, Logical channel #13 interrupt
134	pass_0_interrupts_sar_46_IRQn	Active	SAR1, Logical channel #14 interrupt
135	pass_0_interrupts_sar_47_IRQn	Active	SAR1, Logical channel #15 interrupt
136	pass_0_interrupts_sar_48_IRQn	Active	SAR1, Logical channel #16 interrupt
137	pass_0_interrupts_sar_49_IRQn	Active	SAR1, Logical channel #17 interrupt
138	pass_0_interrupts_sar_50_IRQn	Active	SAR1, Logical channel #18 interrupt
139	pass_0_interrupts_sar_51_IRQn	Active	SAR1, Logical channel #19 interrupt
140	pass_0_interrupts_sar_52_IRQn	Active	SAR1, Logical channel #20 interrupt
141	pass_0_interrupts_sar_53_IRQn	Active	SAR1, Logical channel #21 interrupt
142	pass_0_interrupts_sar_54_IRQn	Active	SAR1, Logical channel #22 interrupt
143	pass_0_interrupts_sar_55_IRQn	Active	SAR1, Logical channel #23 interrupt
144	pass_0_interrupts_sar_56_IRQn	Active	SAR1, Logical channel #24 interrupt
145	pass_0_interrupts_sar_57_IRQn	Active	SAR1, Logical channel #25 interrupt
146	pass_0_interrupts_sar_58_IRQn	Active	SAR1, Logical channel #26 interrupt
147	pass_0_interrupts_sar_59_IRQn	Active	SAR1, Logical channel #27 interrupt
148	pass_0_interrupts_sar_60_IRQn	Active	SAR1, Logical channel #28 interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
149	pass_0_interrupts_sar_61_IRQn	Active	SAR1, Logical channel #29 interrupt
150	pass_0_interrupts_sar_62_IRQn	Active	SAR1, Logical channel #30 interrupt
151	pass_0_interrupts_sar_63_IRQn	Active	SAR1, Logical channel #31 interrupt
152	pass_0_interrupts_sar_64_IRQn	Active	SAR2, Logical channel #0 interrupt
153	pass_0_interrupts_sar_65_IRQn	Active	SAR2, Logical channel #1 interrupt
154	pass_0_interrupts_sar_66_IRQn	Active	SAR2, Logical channel #2 interrupt
155	pass_0_interrupts_sar_67_IRQn	Active	SAR2, Logical channel #3 interrupt
156	pass_0_interrupts_sar_68_IRQn	Active	SAR2, Logical channel #4 interrupt
157	pass_0_interrupts_sar_69_IRQn	Active	SAR2, Logical channel #5 interrupt
158	pass_0_interrupts_sar_70_IRQn	Active	SAR2, Logical channel #6 interrupt
159	pass_0_interrupts_sar_71_IRQn	Active	SAR2, Logical channel #7 interrupt
160	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA0, Channel #0 Interrupt
161	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA0, Channel #1 Interrupt
162	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA0, Channel #2 Interrupt
163	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA0, Channel #3 Interrupt
164	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA0, Channel #0 Interrupt
165	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA0, Channel #1 Interrupt
166	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA0, Channel #2 Interrupt
167	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA0, Channel #3 Interrupt
168	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA0, Channel #4 Interrupt
169	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA0, Channel #5 Interrupt
170	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA0, Channel #6 Interrupt
171	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA0, Channel #7 Interrupt
172	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA0, Channel #8 Interrupt
173	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA0, Channel #9 Interrupt
174	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA0, Channel #10 Interrupt
175	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA0, Channel #11 Interrupt
176	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA0, Channel #12 Interrupt
177	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA0, Channel #13 Interrupt
178	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA0, Channel #14 Interrupt
179	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA0, Channel #15 Interrupt
180	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA0, Channel #16 Interrupt
181	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA0, Channel #17 Interrupt

（表格续下页.....）

15 Interrupts and wake-up assignments

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
182	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA0, Channel #18 Interrupt
183	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA0, Channel #19 Interrupt
184	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA0, Channel #20 Interrupt
185	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA0, Channel #21 Interrupt
186	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA0, Channel #22 Interrupt
187	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA0, Channel #23 Interrupt
188	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA0, Channel #24 Interrupt
189	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA0, Channel #25 Interrupt
190	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA0, Channel #26 Interrupt
191	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA0, Channel #27 Interrupt
192	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA0, Channel #28 Interrupt
193	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA0, Channel #29 Interrupt
194	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA0, Channel #30 Interrupt
195	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA0, Channel #31 Interrupt
196	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA0, Channel #32 Interrupt
197	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA0, Channel #33 Interrupt
198	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA0, Channel #34 Interrupt
199	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA0, Channel #35 Interrupt
200	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA0, Channel #36 Interrupt
201	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA0, Channel #37 Interrupt
202	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA0, Channel #38 Interrupt
203	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA0, Channel #39 Interrupt
20 4	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA0, Channel #40 Interrupt
205	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA0, Channel #41 Interrupt
206	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA0, Channel #42 Interrupt
207	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA0, Channel #43 Interrupt
208	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA0, Channel #44 Interrupt
209	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA0, Channel #45 Interrupt
210	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA0, Channel #46 Interrupt
211	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA0, Channel #47 Interrupt
212	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA0, Channel #48 Interrupt
213	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA0, Channel #49 Interrupt
214	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA0, Channel #50 Interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
215	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA0, Channel #51 Interrupt
216	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA0, Channel #52 Interrupt
217	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA0, Channel #53 Interrupt
218	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA0, Channel #54 Interrupt
219	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA0, Channel #55 Interrupt
220	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA0, Channel #56 Interrupt
221	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA0, Channel #57 Interrupt
222	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA0, Channel #58 Interrupt
223	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA0, Channel #59 Interrupt
224	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA0, Channel #60 Interrupt
225	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA0, Channel #61 Interrupt
226	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA0, Channel #62 Interrupt
227	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA0, Channel #63 Interrupt
228	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA0, Channel #64 Interrupt
229	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA0, Channel #65 Interrupt
230	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA0, Channel #66 Interrupt
231	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA0, Channel #67 Interrupt
232	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA0, Channel #68 Interrupt
233	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA0, Channel #69 Interrupt
234	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA0, Channel #70 Interrupt
235	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA0, Channel #71 Interrupt
236	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA0, Channel #72 Interrupt
237	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA0, Channel #73 Interrupt
238	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA0, Channel #74 Interrupt
239	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA0, Channel #75 Interrupt
240	cpuss_interrupts_dw0_76_IRQn	Active	CPUSS P-DMA0, Channel #76 Interrupt
241	cpuss_interrupts_dw0_77_IRQn	Active	CPUSS P-DMA0, Channel #17 Interrupt
242	cpuss_interrupts_dw0_78_IRQn	Active	CPUSS P-DMA0, Channel #78 Interrupt
243	cpuss_interrupts_dw0_79_IRQn	Active	CPUSS P-DMA0, Channel #79 Interrupt
244	cpuss_interrupts_dw0_80_IRQn	Active	CPUSS P-DMA0, Channel #80 Interrupt
245	cpuss_interrupts_dw0_81_IRQn	Active	CPUSS P-DMA0, Channel #81 Interrupt
246	cpuss_interrupts_dw0_82_IRQn	Active	CPUSS P-DMA0, Channel #82 Interrupt
247	cpuss_interrupts_dw0_83_IRQn	Active	CPUSS P-DMA0, Channel #83 Interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
248	cpuss_interrupts_dw0_84_IRQn	Active	CPUSS P-DMA0, Channel #84 Interrupt
249	cpuss_interrupts_dw0_85_IRQn	Active	CPUSS P-DMA0, Channel #85 Interrupt
250	cpuss_interrupts_dw0_86_IRQn	Active	CPUSS P-DMA0, Channel #86 Interrupt
251	cpuss_interrupts_dw0_87_IRQn	Active	CPUSS P-DMA0, Channel #87 Interrupt
252	cpuss_interrupts_dw0_88_IRQn	Active	CPUSS P-DMA0, Channel #88 Interrupt
253	cpuss_interrupts_dw0_89_IRQn	Active	CPUSS P-DMA0, Channel #89 Interrupt
254	cpuss_interrupts_dw0_90_IRQn	Active	CPUSS P-DMA0, Channel #90 Interrupt
255	cpuss_interrupts_dw0_91_IRQn	Active	CPUSS P-DMA0, Channel #91 Interrupt
256	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA1, Channel #0 Interrupt
2 5 7	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA1, Channel #1 Interrupt
258	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA1, Channel #2 Interrupt
259	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA1, Channel #3 Interrupt
260	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA1, Channel #4 Interrupt
261	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA1, Channel #5 Interrupt
262	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA1, Channel #6 Interrupt
263	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA1, Channel #7 Interrupt
264	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA1, Channel #8 Interrupt
265	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA1, Channel #9 Interrupt
266	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA1, Channel #10 Interrupt
267	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA1, Channel #11 Interrupt
268	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA1, Channel #12 Interrupt
269	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA1, Channel #13 Interrupt
270	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA1, Channel #14 Interrupt
271	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA1, Channel #15 Interrupt
272	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA1, Channel #16 Interrupt
273	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA1, Channel #17 Interrupt
274	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA1, Channel #18 Interrupt
275	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA1, Channel #19 Interrupt
276	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA1, Channel #20 Interrupt
277	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA1, Channel #21 Interrupt
278	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA1, Channel #22 Interrupt
279	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA1, Channel #23 Interrupt
280	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA1, Channel #24 Interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
281	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA1, Channel #25 Interrupt
282	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA1, Channel #26 Interrupt
283	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA1, Channel #27 Interrupt
284	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA1, Channel #28 Interrupt
285	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA1, Channel #29 Interrupt
286	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA1, Channel #30 Interrupt
287	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA1, Channel #31 Interrupt
288	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA1, Channel #32 Interrupt
289	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA1, Channel #33 Interrupt
290	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA1, Channel #34 Interrupt
291	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA1, Channel #35 Interrupt
292	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA1, Channel #36 Interrupt
293	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA1, Channel #37 Interrupt
294	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA1, Channel #38 Interrupt
295	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA1, Channel #39 Interrupt
296	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA1, Channel #40 Interrupt
297	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA1, Channel #41 Interrupt
298	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA1, Channel #42 Interrupt
299	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA1, Channel #43 Interrupt
300	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 Group #0, Counter #0 Interrupt
301	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 Group #0, Counter #1 Interrupt
302	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 Group #0, Counter #2 Interrupt
303	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 Group #0, Counter #3 Interrupt
30 4	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 Group #0, Counter #4 Interrupt
305	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 Group #0, Counter #5 Interrupt
306	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 Group #0, Counter #6 Interrupt
307	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 Group #0, Counter #7 Interrupt
308	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 Group #0, Counter #8 Interrupt
309	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 Group #0, Counter #9 Interrupt
310	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 Group #0, Counter #10 Interrupt
311	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 Group #0, Counter #11 Interrupt
312	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 Group #0, Counter #12 Interrupt
313	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 Group #0, Counter #13 Interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
314	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 Group #0, Counter #14 Interrupt
315	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 Group #0, Counter #15 Interrupt
316	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 Group #0, Counter #16 Interrupt
317	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 Group #0, Counter #17 Interrupt
318	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 Group #0, Counter #18 Interrupt
319	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 Group #0, Counter #19 Interrupt
320	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 Group #0, Counter #20 Interrupt
321	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 Group #0, Counter #21 Interrupt
322	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 Group #0, Counter #22 Interrupt
323	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 Group #0, Counter #23 Interrupt
324	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 Group #0, Counter #2 Interrupt
325	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 Group #0, Counter #25 Interrupt
326	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 Group #0, Counter #26 Interrupt
327	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 Group #0, Counter #27 Interrupt
328	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 Group #0, Counter #28 Interrupt
329	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 Group #0, Counter #29 Interrupt
330	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 Group #0, Counter #30 Interrupt
331	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 Group #0, Counter #31 Interrupt
332	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 Group #0, Counter #32 Interrupt
333	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 Group #0, Counter #33 Interrupt
334	tcpwm_0_interrupts_34_IRQn	Active	TCPWM0 Group #0, Counter #34 Interrupt
335	tcpwm_0_interrupts_35_IRQn	Active	TCPWM0 Group #0, Counter #35 Interrupt
336	tcpwm_0_interrupts_36_IRQn	Active	TCPWM0 Group #0, Counter #36 Interrupt
337	tcpwm_0_interrupts_37_IRQn	Active	TCPWM0 Group #0, Counter #37 Interrupt
338	tcpwm_0_interrupts_38_IRQn	Active	TCPWM0 Group #0, Counter #38 Interrupt
339	tcpwm_0_interrupts_39_IRQn	Active	TCPWM0 Group #0, Counter #39 Interrupt
340	tcpwm_0_interrupts_40_IRQn	Active	TCPWM0 Group #0, Counter #40 Interrupt
341	tcpwm_0_interrupts_41_IRQn	Active	TCPWM0 Group #0, Counter #41 Interrupt
342	tcpwm_0_interrupts_42_IRQn	Active	TCPWM0 Group #0, Counter #42 Interrupt
343	tcpwm_0_interrupts_43_IRQn	Active	TCPWM0 Group #0, Counter #43 Interrupt
344	tcpwm_0_interrupts_44_IRQn	Active	TCPWM0 Group #0, Counter #44 Interrupt
345	tcpwm_0_interrupts_45_IRQn	Active	TCPWM0 Group #0, Counter #45 Interrupt
346	tcpwm_0_interrupts_46_IRQn	Active	TCPWM0 Group #0, Counter #46 Interrupt

（表格续下页.....）

15 Interrupts and wake-up assignments

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
347	tcpwm_0_interrupts_47_IRQn	Active	TCPWM0 Group #0, Counter #47 Interrupt
348	tcpwm_0_interrupts_48_IRQn	Active	TCPWM0 Group #0, Counter #48 Interrupt
349	tcpwm_0_interrupts_49_IRQn	Active	TCPWM0 Group #0, Counter #49 Interrupt
350	tcpwm_0_interrupts_50_IRQn	Active	TCPWM0 Group #0, Counter #50 Interrupt
351	tcpwm_0_interrupts_51_IRQn	Active	TCPWM0 Group #0, Counter #51 Interrupt
352	tcpwm_0_interrupts_52_IRQn	Active	TCPWM0 Group #0, Counter #52 Interrupt
353	tcpwm_0_interrupts_53_IRQn	Active	TCPWM0 Group #0, Counter #53 Interrupt
354	tcpwm_0_interrupts_54_IRQn	Active	TCPWM0 Group #0, Counter #54 Interrupt
355	tcpwm_0_interrupts_55_IRQn	Active	TCPWM0 Group #0, Counter #55 Interrupt
356	tcpwm_0_interrupts_56_IRQn	Active	TCPWM0 Group #0, Counter #56 Interrupt
357	tcpwm_0_interrupts_57_IRQn	Active	TCPWM0 Group #0, Counter #57 Interrupt
358	tcpwm_0_interrupts_58_IRQn	Active	TCPWM0 Group #0, Counter #58 Interrupt
359	tcpwm_0_interrupts_59_IRQn	Active	TCPWM0 Group #0, Counter #59 Interrupt
360	tcpwm_0_interrupts_60_IRQn	Active	TCPWM0 Group #0, Counter #60 Interrupt
361	tcpwm_0_interrupts_61_IRQn	Active	TCPWM0 Group #0, Counter #61 Interrupt
362	tcpwm_0_interrupts_62_IRQn	Active	TCPWM0 Group #0, Counter #62 Interrupt
363	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 Group #1, Counter #0 Interrupt
364	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 Group #1, Counter #1 Interrupt
365	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 Group #1, Counter #2 Interrupt
366	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 Group #1, Counter #3 Interrupt
367	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 Group #1, Counter #4 Interrupt
368	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 Group #1, Counter #5 Interrupt
369	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 Group #1, Counter #6 Interrupt
370	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 Group #1, Counter #7 Interrupt
371	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 Group #1, Counter #8 Interrupt
372	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 Group #1, Counter #9 Interrupt
372	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 Group #1, Counter #10 Interrupt
374	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 Group #1, Counter #11 Interrupt
375	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 Group #2, Counter #0 Interrupt
376	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 Group #2, Counter #1 Interrupt
377	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 Group #2, Counter #2 Interrupt
378	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 Group #2, Counter #3 Interrupt
379	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 Group #2, Counter #4 Interrupt

（表格续下页.....）

表 18 （续）外设中断分配和唤醒源

Interrupt	Source	Power mode	Description
380	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 Group #2, Counter #5 Interrupt
381	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 Group #2, Counter #6 Interrupt
382	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 Group #2, Counter #7 Interrupt

16 核心中断类型

表 19 核心中断类型

Interrupt	Source	Power mode	Description
0	CPUIntIdx0_IRQn[1)]	DeepSleep	CPU user interrupt #0
1	CPUIntIdx1_IRQn[1)]	DeepSleep	CPU user interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU user interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU user interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU user interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU user interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU user interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU user interrupt #7
8	Internal0_IRQn	Active	Internal software interrupt #0
9	Internal1_IRQn	Active	Internal software interrupt #1
10	Internal2_IRQn	Active	Internal software interrupt #2
11	Internal3_IRQn	Active	Internal software interrupt #3
12	Internal4_IRQn	Active	Internal software interrupt #4
13	Internal5_IRQn	Active	Internal software interrupt #5
14	Internal6_IRQn	Active	Internal software interrupt #6
15	Internal7_IRQn	Active	Internal software interrupt #7

1) 用户中断不能用于 CM0+ 应用程序，因为它由系统调用内部使用。请注意，这不会影响 CM4 应用程序。

17 触发器多路复用器

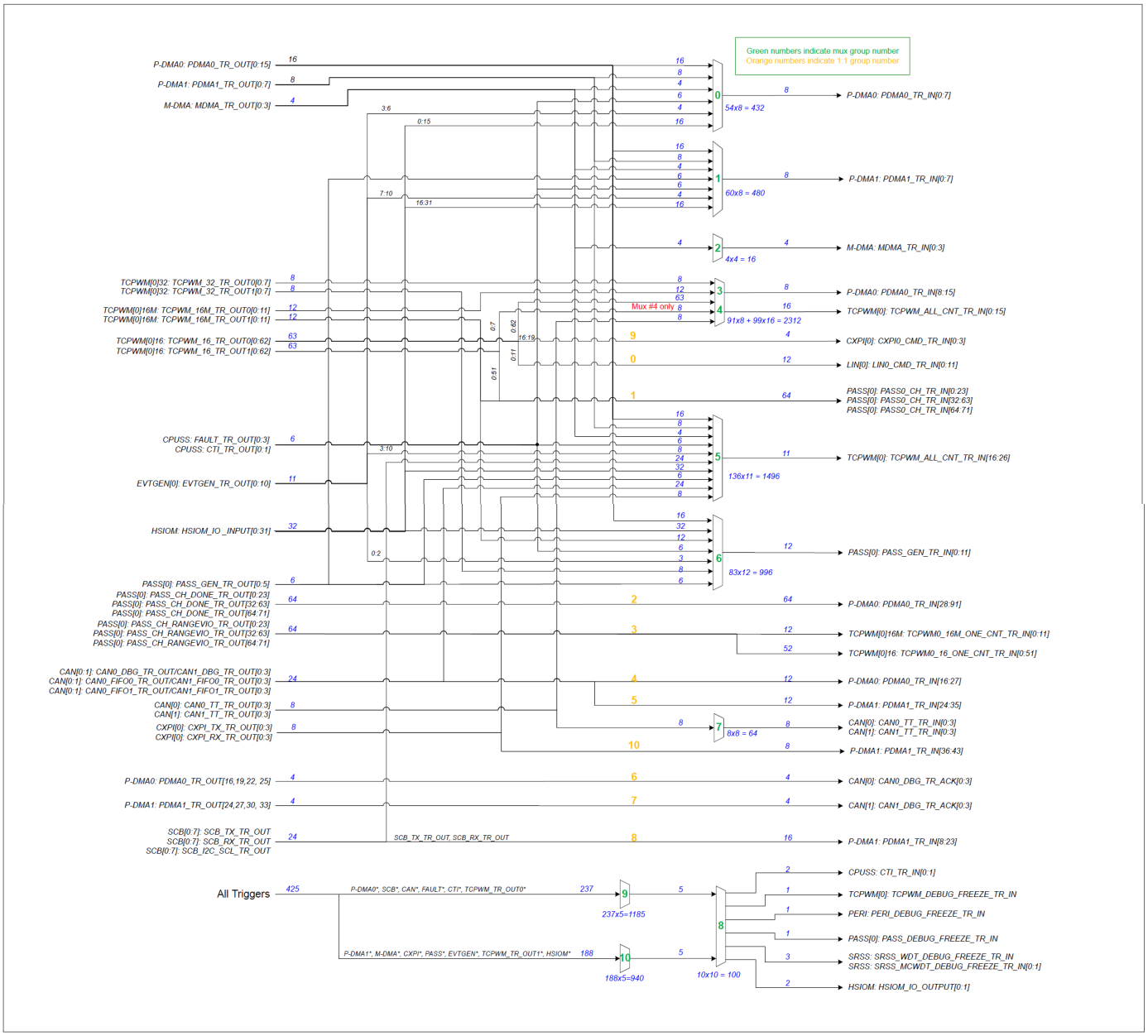

图 14 触发器多路复用器[15)]

15 该图仅显示 TRIG_LABEL；最终触发形成基于公式TRIG_{PREFIX(IN/ OUT)}_{MUX_x}_{TRIG_LABEL} / TRIG_{PREFIX(IN_1TO1/OUT_1TO1)}_{x}_{TRIG_LABEL}（参见表 20，表 21，和表 22 。）

18 触发组输入

表 20 触发输入

Input	Trigger	Description
MUX Group 0: PDMA0_TR (P-DMA0 trigger multiplexer)		
1:16[1)]	PDMA0_TR_OUT[0:15]	Allow P-DMA0 to chain to itself, useful for triggering once per row for 2D transfer
17:24	PDMA1_TR_OUT[0:7]	Cross connections from P-DMA1 to P-DMA0, Channels 0-7 are used
25:28	MDMA_TR_OUT[0:3]	Cross connections from M-DMA0 to P-DMA0
29:32	FAULT_TR _OUT[0:3]	Allow faults to initiate data transfer for debug purposes
33:34	CTI_TR_OUT[0:1]	Trace events
35:38	EVTGEN_TR_OUT[3:6]	EVTGEN triggers
39:54	HSIOM_IO_INPUT[0:15]	I/O inputs
MUX Group 1: PDMA1_TR (P-DMA1 trigger multiplexer)		
1:16	PDMA0_TR_OUT[0:15]	Allow P-DMA0 to trigger P-DMA1
17:24	PDMA1_TR_OUT[0:7]	Allow P-DMA1 to chain to itself, useful for triggering once per row for 2D transfer
25:28	MDMA_TR_OUT[0:3]	Allow M-DMA0 to trigger P-DMA0
29:32	FAULT_TR _OUT[0:3]	Allow faults to initiate data transfer for debug purposes
33:34	CTI_TR_OUT[0:1]	Trace events
35:38	EVTGEN_TR_OUT[7:10]	EVTGEN triggers
39:54	HSIOM_IO_INPUT[16:31]	I/O inputs
55:60	PASS_GEN_TR_OUT[0:5]	PASS SAR events
MUX Group 2: MDMA (M-DMA0 trigger multiplexer)		
1:4	MDMA_TR_OUT[0:3]	Allow M-DMA0 to trigger itself
MUX Group 3: TCPWM_TO_PDMA0 (TCPWM0 to P-DMA0 trigger multiplexer)		
1:8	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
9:20	TCPWM_16M_TR_OUT0[0:11]	16-bit motor enhanced TCPWM0 counters
21:83	TCPWM_16_TR_OUT0[0:62]	16-bit TCPWM0 counters
84:87	CAN0_TT_TR_OUT[0:3]	CAN0 TT sync outputs
88:91	CAN1_TT_TR_OUT[0:3]	CAN1 TT sync outputs
MUX Group 4: TCPWM_OUT (TCPWM0 loop back multiplexer)		
1:8	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
9:20	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
21:83	TCPWM_16_TR_OUT0[0:62]	16-bit TCPWM0 counters

（表格续下页……）

18 Triggers group inputs

表 20 （续）触发输入

Input	Trigger	Description
84:91	TCPWM_16_TR_OUT1[0:7]	Allows feedback of two signals from same counters
92:95	CAN0_TT_TR_OUT[0:3]	CAN0 TT sync outputs
96:99	CAN1_TT_TR_OUT[0:3]	CAN1 TT sync outputs
MUX Group 5: TCPWM_IN (TCPWM0 Trigger Multiplexer)		
1:16	PDMA0_TR_OUT[0:15]	General-purpose P-DMA0 triggers
17:24	PDMA1_TR_OUT[0:7]	General-purpose P-DMA1 triggers
25:28	MDMA_TR_OUT[0:3]	M-DMA0 triggers
29:30	CTI_TR_OUT[0:1]	Trace events
31:34	FAULT_TR _OUT[0:3]	Fault events
35:40	PASS_GEN_TR_OUT[0:5]	PASS SAR events
41:72	HSIOM_IO_INPUT[0:31]	I/O inputs
73	SCB_TX_TR_OUT[0]	SCB0 TX trigger
74	SCB_RX_TR_OUT[0]	SCB0 RX trigger
75	SCB_I2C_SCL_TR_OUT[0]	SCB0 I^2C trigger
76	SCB_TX_TR_OUT[1]	SCB1 TX trigger
77	SCB_RX_TR_OUT[1]	SCB1 RX trigger
78	SCB_I2C_SCL_TR_OUT[1]	SCB1 I^2C trigger
79	SCB_TX_TR_OUT[2]	SCB2 TX trigger
80	SCB_RX_TR_OUT[2]	SCB2 RX trigger
81	SCB_I2C_SCL_TR_OUT[2]	SCB2 I^2C trigger
82	SCB_TX_TR_OUT[3]	SCB3 TX trigger
83	SCB_RX_TR_OUT[3]	SCB3 RX trigger
84	SCB_I2C_SCL_TR_OUT[3]	SCB3 I^2C trigger
85	SCB_TX_TR_OUT[4]	SCB4 TX trigger
86	SCB_RX_TR_OUT[4]	SCB4 RX trigger
87	SCB_I2C_SCL_TR_OUT[4]	SCB4 I^2C trigger
88	SCB_TX_TR_OUT[5]	SCB5 TX trigger
89	SCB_RX_TR_OUT[5]	SCB5 RX trigger
90	SCB_I2C_SCL_TR_OUT[5]	SCB5 I^2C trigger
91	SCB_TX_TR_OUT[6]	SCB6 TX trigger
92	SCB_RX_TR_OUT[6]	SCB6 RX trigger
93	SCB_I2C_SCL_TR_OUT[6]	SCB6 I^2C trigger
94	SCB_TX_TR_OUT[7]	SCB7 TX trigger

（表格续下页……）

18 Triggers group inputs

表 20 （续）触发输入

Input	Trigger	Description
95	SCB_RX_TR_OUT[7]	SCB7 RX trigger
96	SCB_I2C_SCL_TR_OUT[7]	SCB7 I^2C trigger
97:100	CAN0_DBG_T R_OUT[0:3]	CAN0 M-DMA0 events
101:104	CAN0_FIFO0_TR_OUT[0:3]	CAN0 FIFO0 events
105:108	CAN0_FIFO1_TR_OUT[0:3]	CAN0 FIFO1 events
109:112	CAN1_DBG_T R_OUT[0:3]	CAN1 M-DMA0 events
113:116	CAN1_FIFO0_TR_OUT[0:3]	CAN1 FIFO0 events
117:120	CAN1_FIFO1_TR_OUT[0:3]	CAN1 FIFO1 events
121:124	CXPI_TX_TR_OUT[0:3]	CXPI transmit events
125:128	CXPI_RX_TR_OUT[0:3]	CXPI receive events
129:136	EVTGEN_TR_OUT[3:10]	EVTGEN triggers
MUX Group 6: PASS (PASS SAR trigger multiplexer)		
1:16	PDMA0_TR_OUT[0:15]	General purpose P-DMA0 triggers
17:18	CTI_TR_OUT[0:1]	Trace events
19:22	FAULT_TR _OUT[0:3]	Fault events
23:25	EVTGEN_TR_OUT[0:2]	EVTGEN triggers
26:31	PASS_GEN_TR_OUT[0:5]	PASS SAR done signals
32:63	HSIOM_IO_INPUT[0:31]	I/O inputs
64:71	TCPWM_32_TR_OUT1[0:7]	32-bit TCPWM0 counters
72:83	TCPWM_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM0 counters
MUX Group 7: CAN TT sync triggers		
1:4	CAN0_TT_TR_OUT[0:3]	CAN0 TT sync outputs
5:8	CAN1_TT_TR_OUT[0:3]	CAN1 TT sync outputs
MUX Group 8: DebugMain (Debug Multiplexer)		
1:5	TR_GROUP9_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #2
MUX Group 9: DebugReduction1 (Debug Reduction #1)		
1:92	PDMA0_TR_OUT[0:91]	P-DMA0 triggers
93:100	SCB_TX_TR_OUT[0:7]	SCB TTCAN tx triggers
101:108	SCB_RX_TR_OUT[0:7]	SCB TTCAN rx triggers
109:116	SCB_I2C_SCL_TR_OUT[0:7]	SCB I^2C triggers
117:120	CAN0_DBG_T R_OUT[0:3]	CAN0 P-DMA
121:124	CAN0_FIFO0_TR_OUT[0:3]	CAN0 FIFO0

（表格续下页……）

表 20 （续）触发输入

Input	Trigger	Description
125:128	CAN0_FIFO1_TR_OUT[0:3]	CAN0 FIFO1
129:132	CAN0_TT_TR_OUT[0:3]	CAN TT sync outputs
133:136	CAN1_DBG_T R_OUT[0:3]	CAN1 P-DMA
137:140	CAN1_FIFO0_TR_OUT[0:3]	CAN1 FIFO0
141:144	CAN1_FIFO1_TR_OUT[0:3]	CAN1 FIFO1
145:148	CAN1_TT_TR_OUT[0:3]	CAN TT sync outputs
149:150	CTI_TR_OUT[0:1]	Trace events
151:154	FAULT_TR _OUT[0:3]	Fault events
155:162	TCPWM_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
163:174	TCPWM_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
175:237	TCPWM_16_TR_OUT0[0:62]	16-bit TCPWM0 counters
MUX Group 10: DebugReduction2 (Debug Reduction #2)		
1:44	PDMA1_TR_OUT[0:43]	16-bit Motor enhanced TCPWM0 counters
45:48	MDMA_TR_OUT[0:3]	16-bit TCPWM0 counters
49:56	TCPWM_32_TR_OUT1[0:7]	32-bit TCPWM0 counters
57:68	TCPWM_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM0 counters
69:131	TCPWM_16_TR_OUT1[0:62]	16-bit TCPWM0 counters
132:137	PASS_GEN_TR_OUT[0:5]	PASS SAR conversion complete events
138:148	EVTGEN_TR_OUT[0:10]	EVTGEN Triggers
149:152	CXPI_TX_TR_OUT[0:3]	CXPI transmit events
153:156	CXPI_RX_TR_OUT[0:3]	CXPI receive events
157:188	HSIOM_IO_INPUT[0:31]	I/O inputs

1) “x:y” 表示从 ‘x’ 到 ‘y’ 的范围。

19 触发组输出

表 21 触发输出

Output	Trigger	Description
MUX Group 0: PDMA0_TR (P-DMA0 trigger multiplexer)		
0:7	PDMA0_TR_IN[0:7]	Triggers to P-DMA0[0:7]
MUX Group 1: PDMA1_TR (P-DMA1 trigger multiplexer)		
0:7	PDMA1_TR_IN[0:7]	Triggers to P-DMA1[0:7]
MUX Group 2: MDMA (M-DMA0 trigger multiplexer)		
0:3	MDMA_TR_IN[0:3]	Triggers to M-DMA0
MUX Group 3: TCPWM_TO_PDMA0 (TCPWM0 to P-DMA0 trigger multiplexer)		
0:7	PDMA0_TR_IN[8:15]	Triggers to P-DMA0[8:15]
MUX Group 4: TCPWM_OUT (TCPWM0 loop back multiplexer)		
0:15	TCPWM_ALL_CNT_TR_IN[0:15]	All counters trigger input
MUX Group 5: TCPWM_IN (TCPWM0 Trigger Multiplexer)		
0:10	TCPWM_ALL_CNT_TR_IN[16:26]	Triggers to TCPWM0
MUX Group 6: PASS (PASS SAR trigger multiplexer)		
0:11	PASS_GEN_TR_IN[0:11]	Triggers to SAR ADCs
MUX Group 7: CAN TT sync triggers		
0:3	CAN0_TT_TR_IN[0:3]	CAN0 TT Sync Inputs
4:7	CAN1_TT_TR_IN[0:3]	CAN1 TT Sync Inputs
MUX Group 8: DebugMain (Debug Multiplexer)		
0:1	HSIOM_IO_OUTPUT[0:1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To CPU Cross Trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze SAR ADC operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
7:8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0:1]	Signal to Freeze MCWDT operation
9	TCPWM_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM0 operation
MUX Group 9: DebugReduction1 (Debug Reduction #1)		
0:4	TR_GROUP8_INPUT[1:5]	To main debug multiplexer
MUX Group 10: DebugReduction2 (Debug Reduction #2)		
0:4	TR_GROUP8_INPUT[6:10]	To main debug multiplexer

20 一对一触发器

表 22 触发器 1:1

Input	Trigger in	Trigger out	Description
MUX Group 0: TCPWM0 to LIN0 Triggers			
0:11	TCPWM0_16_TR_OUT0[0:11]	LIN0_CMD_TR_IN[0:11]	TCPWM0 (Group #0 Counter #00 to #07) to LIN0
MUX Group 1: TCPWM0 to PASS SARx direct connect			
0	TCPWM0_16M_TR_OUT1[0]	PASS0_CH_TR_IN[0]	TCPWM0 Group #1 Counter #00 (PWM0_M_0) to SAR0 ch#0
1	TCPWM0_16M_TR_OUT1[1]	PASS0_CH_TR_IN[1]	TCPWM0 Group #1 Counter #03 (PWM0_M_3) to SAR0 ch#1
2	TCPWM0_16M_TR_OUT1[2]	PASS0_CH_TR_IN[2]	TCPWM0 Group #1 Counter #06 (PWM0_M_6) to SAR0 ch#2
3	TCPWM0_16M_TR_OUT1[3]	PASS0_CH_TR_IN[3]	TCPWM0 Group #1 Counter #09 (PWM0_M_9) to SAR0 ch#3
4:23	TCPWM0_16_TR_OUT1[0:19]	PASS0_CH_TR_IN[4:23]	TCPWM0 Group #0 Counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#4 through SAR0 ch#23
24	TCPWM0_16M_TR_OUT1[4]	PASS0_CH_TR_IN[32]	TCPWM0 Group #1 Counter #01 (PWM0_M_1) to SAR1 ch#0
25	TCPWM0_16M_TR_OUT1[5]	PASS0_CH_TR_IN[33]	TCPWM0 Group #1 Counter #04 (PWM0_M_4) to SAR1 ch#1
26	TCPWM0_16M_TR_OUT1[6]	PASS0_CH_TR_IN[34]	TCPWM0 Group #1 Counter #07 (PWM0_M_7) to SAR1 ch#2
27	TCPWM0_16M_TR_OUT1[7]	PASS0_CH_TR_IN[35]	TCPWM0 Group #1 Counter #10 (PWM0_M_10) to SAR1 ch#3
28:55	TCPWM0_16_TR_OUT1[20:47]	PASS0_CH_TR_IN[36:63]	TCPWM0 Group #0 Counter #20 through 47 (PWM0_20 to PWM0_47) to SAR1 ch#4 through SAR1 ch#31
56	TCPWM0_16M_TR_OUT1[8]	PASS0_CH_TR_IN[64]	TCPWM0 Group #1 Counter #02 (PWM0_M_2) to SAR2 ch#0
57	TCPWM0_16M_TR_OUT1[9]	PASS0_CH_TR_IN[65]	TCPWM0 Group #1 Counter #05 (PWM0_M_5) to SAR2 ch#1
58	TCPWM0_16M_TR_OUT1[10]	PASS0_CH_TR_IN[66]	TCPWM0 Group #1 Counter #08 (PWM0_M_8) to SAR2 ch#2
59	TCPWM0_16M_TR_OUT1[11]	PASS0_CH_TR_IN[67]	TCPWM0 Group #1 Counter #11 (PWM0_M_11) to SAR2 ch#3
60:63	TCPWM0_16_TR_OUT1[48:51]	PASS0_CH_TR_IN[68:71]	TCPWM0 Group #0 Counter #48 through 51 (PWM0_48 to PWM0_51) to SAR2 ch#4 through SAR2 ch#7
MUX Group 2: PASS SARx to P-DMA0 direct connect			

(表格续下页.....)

20 Triggers one-to-one

表 22　　（续） 触发器 1:1

Input	Trigger in	Trigger out	Description
0:23	PASS0_CH_DONE_TR_OUT[0:23]	PDMA0_TR_IN[28:51]	PASS SAR0 [0:23] to P-DMA0 direct connect
24:55	PASS0_CH_DONE_TR_OUT[32:63]	PDMA0_TR_IN[52:83]	PASS SAR1 [0:31] to P-DMA0 direct connect
56:63	PASS0_CH_DONE_TR_OUT[64:71]	PDMA0_TR_IN[84:91]	PASS SAR2 [0:8] to P-DMA0 direct connect
MUX Group 3: PASS SARx to TCPWM0 direct connect			
0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#0[1)], range violation to TCPWM0 Group #1 Counter #00 trig=4
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#1, range violation to TCPWM0 Group #1 Counter #03 trig=4
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#2, range violation to TCPWM0 Group #1 Counter #06 trig=4
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#3, range violation to TCPWM0 Group #1 Counter #09 trig=4
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16_ONE_CNT_TR_IN[0]	SAR0 ch#4, range violation to TCPWM0 Group #0 Counter #00 trig=4
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16_ONE_CNT_TR_IN[1]	SAR0 ch#5, range violation to TCPWM0 Group #0 Counter #01 trig=4
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16_ONE_CNT_TR_IN[2]	SAR0 ch#6, range violation to TCPWM0 Group #0 Counter #02 trig=4
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16_ONE_CNT_TR_IN[3]	SAR0 ch#7, range violation to TCPWM0 Group #0 Counter #03 trig=4
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16_ONE_CNT_TR_IN[4]	SAR0 ch#8, range violation to TCPWM0 Group #0 Counter #04 trig=4
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16_ONE_CNT_TR_IN[5]	SAR0 ch#9, range violation to TCPWM0 Group #0 Counter #05 trig=4
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16_ONE_CNT_TR_IN[6]	SAR0 ch#10, range violation to TCPWM0 Group #0 Counter #06 trig=4
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16_ONE_CNT_TR_IN[7]	SAR0 ch#11, range violation to TCPWM0 Group #0 Counter #07 trig=4
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16_ONE_CNT_TR_IN[8]	SAR0 ch#12, range violation to TCPWM0 Group #0 Counter #08 trig=4
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16_ONE_CNT_TR_IN[9]	SAR0 ch#13, range violation to TCPWM0 Group #0 Counter #09 trig=4
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16_ONE_CNT_TR_IN[10]	SAR0 ch#14, range violation to TCPWM0 Group #0 Counter #10 trig=4
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16_ONE_CNT_TR_IN[11]	SAR0 ch#15, range violation to TCPWM0 Group #0 Counter #11 trig=4

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20 Triggers one-to-one

表 22 （续）触发器 1:1

Input	Trigger in	Trigger out	Description
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16_ONE_CNT_TR_IN[12]	SAR0 ch#16, range violation to TCPWM0 Group #0 Counter #12 trig=4
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16_ONE_CNT_TR_IN[13]	SAR0 ch#17, range violation to TCPWM0 Group #0 Counter #13 trig=4
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16_ONE_CNT_TR_IN[14]	SAR0 ch#18, range violation to TCPWM0 Group #0 Counter #14 trig=4
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16_ONE_CNT_TR_IN[15]	SAR0 ch#19, range violation to TCPWM0 Group #0 Counter #15 trig=4
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16_ONE_CNT_TR_IN[16]	SAR0 ch#20, range violation to TCPWM0 Group #0 Counter #16 trig=4
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16_ONE_CNT_TR_IN[17]	SAR0 ch#21, range violation to TCPWM0 Group #0 Counter #17 trig=4
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#22, range violation to TCPWM0 Group #0 Counter #18 trig=4
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#23, range violation to TCPWM0 Group #0 Counter #19 trig=4
24	PASS0_CH_RANGEVIO_TR_OUT[32]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR1 ch#0, range violation to TCPWM0 Group #1 Counter #01 trig=4
25	PASS0_CH_RANGEVIO_TR_OUT[33]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR1 ch#1, range violation to TCPWM0 Group #1 Counter #04 trig=4
26	PASS0_CH_RANGEVIO_TR_OUT[34]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR1 ch#2, range violation to TCPWM0 Group #1 Counter #07 trig=4
27	PASS0_CH_RANGEVIO_TR_OUT[35]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR1 ch#3, range violation to TCPWM0 Group #1 Counter #10 trig=4
28	PASS0_CH_RANGEVIO_TR_OUT[36]	TCPWM0_16_ONE_CNT_TR_IN[20]	SAR1 ch#4, range violation to TCPWM0 Group #0 Counter #20 trig=4
29	PASS0_CH_RANGEVIO_TR_OUT[37]	TCPWM0_16_ONE_CNT_TR_IN[21]	SAR1 ch#5, range violation to TCPWM0 Group #0 Counter #21 trig=4
30	PASS0_CH_RANGEVIO_TR_OUT[38]	TCPWM0_16_ONE_CNT_TR_IN[22]	SAR1 ch#6, range violation to TCPWM0 Group #0 Counter #22 trig=4
31	PASS0_CH_RANGEVIO_TR_OUT[39]	TCPWM0_16_ONE_CNT_TR_IN[23]	SAR1 ch#7, range violation to TCPWM0 Group #0 Counter #23 trig=4
32	PASS0_CH_RANGEVIO_TR_OUT[40]	TCPWM0_16_ONE_CNT_TR_IN[24]	SAR1 ch#8, range violation to TCPWM0 Group #0 Counter #24 trig=4
33	PASS0_CH_RANGEVIO_TR_OUT[41]	TCPWM0_16_ONE_CNT_TR_IN[25]	SAR1 ch#9, range violation to TCPWM0 Group #0 Counter #25 trig=4
34	PASS0_CH_RANGEVIO_TR_OUT[42]	TCPWM0_16_ONE_CNT_TR_IN[26]	SAR1 ch#10, range violation to TCPWM0 Group #0 Counter #26 trig=4

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20 Triggers one-to-one

表 22 （续）触发器 1:1

Input	Trigger in	Trigger out	Description
35	PASS0_CH_RANGEVIO_TR_OUT[43]	TCPWM0_16_ONE_CNT_TR_IN[27]	SAR1 ch#11, range violation to TCPWM0 Group #0 Counter #27 trig=4
36	PASS0_CH_RANGEVIO_TR_OUT[44]	TCPWM0_16_ONE_CNT_TR_IN[28]	SAR1 ch#12, range violation to TCPWM0 Group #0 Counter #28 trig=4
37	PASS0_CH_RANGEVIO_TR_OUT[45]	TCPWM0_16_ONE_CNT_TR_IN[29]	SAR1 ch#13, range violation to TCPWM0 Group #0 Counter #29 trig=4
38	PASS0_CH_RANGEVIO_TR_OUT[46]	TCPWM0_16_ONE_CNT_TR_IN[30]	SAR1 ch#14, range violation to TCPWM0 Group #0 Counter #30 trig=4
39	PASS0_CH_RANGEVIO_TR_OUT[47]	TCPWM0_16_ONE_CNT_TR_IN[31]	SAR1 ch#15, range violation to TCPWM0 Group #0 Counter #31 trig=4
40	PASS0_CH_RANGEVIO_TR_OUT[48]	TCPWM0_16_ONE_CNT_TR_IN[32]	SAR1 ch#16, range violation to TCPWM0 Group #0 Counter #32 trig=4
41	PASS0_CH_RANGEVIO_TR_OUT[49]	TCPWM0_16_ONE_CNT_TR_IN[33]	SAR1 ch#17, range violation to TCPWM0 Group #0 Counter #33 trig=4
42	PASS0_CH_RANGEVIO_TR_OUT[50]	TCPWM0_16_ONE_CNT_TR_IN[34]	SAR1 ch#18, range violation to TCPWM0 Group #0 Counter #34 trig=4
43	PASS0_CH_RANGEVIO_TR_OUT[51]	TCPWM0_16_ONE_CNT_TR_IN[35]	SAR1 ch#19, range violation to TCPWM0 Group #0 Counter #35 trig=4
44	PASS0_CH_RANGEVIO_TR_OUT[52]	TCPWM0_16_ONE_CNT_TR_IN[36]	SAR1 ch#20, range violation to TCPWM0 Group #0 Counter #36 trig=4
45	PASS0_CH_RANGEVIO_TR_OUT[53]	TCPWM0_16_ONE_CNT_TR_IN[37]	SAR1 ch#21, range violation to TCPWM0 Group #0 Counter #37 trig=4
46	PASS0_CH_RANGEVIO_TR_OUT[54]	TCPWM0_16_ONE_CNT_TR_IN[38]	SAR1 ch#22, range violation to TCPWM0 Group #0 Counter #38 trig=4
47	PASS0_CH_RANGEVIO_TR_OUT[55]	TCPWM0_16_ONE_CNT_TR_IN[39]	SAR1 ch#23, range violation to TCPWM0 Group #0 Counter #39 trig=4
48	PASS0_CH_RANGEVIO_TR_OUT[56]	TCPWM0_16_ONE_CNT_TR_IN[40]	SAR1 ch#24, range violation to TCPWM0 Group #0 Counter #40 trig=4
49	PASS0_CH_RANGEVIO_TR_OUT[57]	TCPWM0_16_ONE_CNT_TR_IN[41]	SAR1 ch#25, range violation to TCPWM0 Group #0 Counter #41 trig=4
50	PASS0_CH_RANGEVIO_TR_OUT[58]	TCPWM0_16_ONE_CNT_TR_IN[42]	SAR1 ch#26, range violation to TCPWM0 Group #0 Counter #42 trig=4
51	PASS0_CH_RANGEVIO_TR_OUT[59]	TCPWM0_16_ONE_CNT_TR_IN[43]	SAR1 ch#27, range violation to TCPWM0 Group #0 Counter #43 trig=4
52	PASS0_CH_RANGEVIO_TR_OUT[60]	TCPWM0_16_ONE_CNT_TR_IN[44]	SAR1 ch#28, range violation to TCPWM0 Group #0 Counter #44 trig=4
53	PASS0_CH_RANGEVIO_TR_OUT[61]	TCPWM0_16_ONE_CNT_TR_IN[45]	SAR1 ch#29, range violation to TCPWM0 Group #0 Counter #45 trig=4

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表 22 （续）触发器 1:1

Input	Trigger in	Trigger out	Description
54	PASS0_CH_RANGEVIO_TR_OUT[62]	TCPWM0_16_ONE_CNT_TR_IN[46]	SAR1 ch#30, range violation to TCPWM0 Group #0 Counter #46 trig=4
55	PASS0_CH_RANGEVIO_TR_OUT[63]	TCPWM0_16_ONE_CNT_TR_IN[47]	SAR1 ch#31, range violation to TCPWM0 Group #0 Counter #47 trig=4
56	PASS0_CH_RANGEVIO_TR_OUT[64]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR2 ch#0, range violation to TCPWM0 Group #1 Counter #02 trig=4
57	PASS0_CH_RANGEVIO_TR_OUT[65]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR2 ch#1, range violation to TCPWM0 Group #1 Counter #05 trig=4
58	PASS0_CH_RANGEVIO_TR_OUT[66]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR2 ch#2, range violation to TCPWM0 Group #1 Counter #08 trig=4
59	PASS0_CH_RANGEVIO_TR_OUT[67]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR2 ch#3, range violation to TCPWM0 Group #1 Counter #11 trig=4
60	PASS0_CH_RANGEVIO_TR_OUT[68]	TCPWM0_16_ONE_CNT_TR_IN[48]	SAR2 ch#4, range violation to TCPWM0 Group #0 Counter #48 trig=4
61	PASS0_CH_RANGEVIO_TR_OUT[69]	TCPWM0_16_ONE_CNT_TR_IN[49]	SAR2 ch#5, range violation to TCPWM0 Group #0 Counter #49 trig=4
62	PASS0_CH_RANGEVIO_TR_OUT[70]	TCPWM0_16_ONE_CNT_TR_IN[50]	SAR2 ch#6, range violation to TCPWM0 Group #0 Counter #50 trig=4
63	PASS0_CH_RANGEVIO_TR_OUT[71]	TCPWM0_16_ONE_CNT_TR_IN[51]	SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #51 trig=4
MUX Group 4: CAN0 to P-DMA0 Triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[16]	CAN0, Channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[17]	CAN0, Channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[18]	CAN0, Channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[19]	CAN0, Channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[20]	CAN0, Channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[21]	CAN0, Channel #1 FIFO1 trigger
6	CAN0_DBG_TR_OUT[2]	PDMA0_TR_IN[22]	CAN0, Channel #2 P-DMA0 trigger
7	CAN0_FIFO0_TR_OUT[2]	PDMA0_TR_IN[23]	CAN0, Channel #2 FIFO0 trigger
8	CAN0_FIFO1_TR_OUT[2]	PDMA0_TR_IN[24]	CAN0, Channel #2 FIFO1 trigger
9	CAN0_DBG_TR_OUT[3]	PDMA0_TR_IN[25]	CAN0, Channel #3 P-DMA0 trigger
10	CAN0_FIFO0_TR_OUT[3]	PDMA0_TR_IN[26]	CAN0, Channel #3 FIFO0 trigger
11	CAN0_FIFO1_TR_OUT[3]	PDMA0_TR_IN[27]	CAN0, Channel #3 FIFO1 trigger
MUX Group 5: CAN1 to P-DMA1 triggers			
0	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[24]	CAN1, Channel #0 P-DMA01 trigger
1	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[25]	CAN1, Channel #0 FIFO0 trigger

（表格续下页.....）

20 Triggers one-to-one

表 22 （续） 触发器 1:1

Input	Trigger in	Trigger out	Description
2	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[26]	CAN1, Channel #0 FIFO1 trigger
3	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[27]	CAN1, Channel #1 P-DMA1 trigger
4	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[28]	CAN1, Channel #1 FIFO0 trigger
5	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[29]	CAN1, Channel #1 FIFO1 trigger
6	CAN1_DBG_TR_OUT[2]	PDMA1_TR_IN[30]	CAN1, Channel #2 P-DMA1 trigger
7	CAN1_FIFO0_TR_OUT[2]	PDMA1_TR_IN[31]	CAN1, Channel #2 FIFO0 trigger
8	CAN1_FIFO1_TR_OUT[2]	PDMA1_TR_IN[32]	CAN1, Channel #2 FIFO1 trigger
9	CAN1_DBG_TR_OUT[3]	PDMA1_TR_IN[33]	CAN1, Channel #3 P-DMA1 trigger
10	CAN1_FIFO0_TR_OUT[3]	PDMA1_TR_IN[34]	CAN1, Channel #3 FIFO0 trigger
11	CAN1_FIFO1_TR_OUT[3]	PDMA1_TR_IN[35]	CAN1, Channel #3 FIFO1 trigger
MUX Group 6:Acknowledge triggers from P-DMA0 to CAN0			
0	PDMA0_TR_OUT[16]	CAN0_DBG_TR_ACK[0]	CAN0, Channel #0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[19]	CAN0_DBG_TR_ACK[1]	CAN0, Channel #1 P-DMA0 acknowledge
2	PDMA0_TR_OUT[22]	CAN0_DBG_TR_ACK[2]	CAN0, Channel #2 P-DMA0 acknowledge
3	PDMA0_TR_OUT[25]	CAN0_DBG_TR_ACK[3]	CAN0, Channel #3 P-DMA0 acknowledge
MUX Group 7: Acknowledge triggers from P-DMA1 to CAN1			
0	PDMA1_TR_OUT[24]	CAN1_DBG_TR_ACK[0]	CAN1, Channel #0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[27]	CAN1_DBG_TR_ACK[1]	CAN1, Channel #1 P-DMA1 acknowledge
2	PDMA1_TR_OUT[30]	CAN1_DBG_TR_ACK[2]	CAN1, Channel #2 P-DMA1 acknowledge
3	PDMA1_TR_OUT[33]	CAN1_DBG_TR_ACK[3]	CAN1, Channel #3 P-DMA1 acknowledge
MUX Group 8: SCBx to P-DMA1 Triggers			
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[8]	SCB0 TX to P-DMA1 Trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[9]	SCB0 RX to P-DMA1 Trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[10]	SCB1 TX to P-DMA1 Trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[11]	SCB1 RX to P-DMA1 Trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[12]	SCB2 TX to P-DMA1 Trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[13]	SCB2 RX to P-DMA1 Trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[14]	SCB3 TX to P-DMA1 Trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[15]	SCB3 RX to P-DMA1 Trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[16]	SCB4 TX to P-DMA1 Trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[17]	SCB4 RX to P-DMA1 Trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[18]	SCB5 TX to P-DMA1 Trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[19]	SCB5 RX to P-DMA1 Trigger

（表格续下页……）

表 22 （续）触发器 1:1

Input	Trigger in	Trigger out	Description
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[20]	SCB6 TX to P-DMA1 Trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[21]	SCB6 RX to P-DMA1 Trigger
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[22]	SCB7 TX to P-DMA1 Trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[23]	SCB7 RX to P-DMA1 Trigger
MUX Group 9: TCPWM0 to CXPI Triggers			
0:3	TCPWM0_16_TR_OUT0[16:19]	CXPI0_CMD_TR_IN[0:3]	TCPWM0 Group #0 (Counter #16 to #19) to CXPI0 Trigger
MUX Group 10: CXPI to P-DMA1 Triggers			
0:3	CXPI_TX_TR_OUT[0:3]	PDMA1_TR_IN[36:39]	CXPI0 TX to P-DMA1 Triggers
4:7	CXPI_RX_TR_OUT[0:3]	PDMA1_TR_IN[40:43]	CXPI0 RX to P-DMA1 Triggers

1) SAR ADC[x] 的每个逻辑通道都可以连接到任意 SAR ADC[x]_y 外部引脚。(x = 0, or 1, or, 2 and y=0 to max 31)

21 外设时钟

表 23 外设时钟分配

Output	Destination	Description
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO12_CLOCK	SMART I/O #12
2	PCLK_SMARTIO13_CLOCK	SMART I/O #13
3	PCLK_SMARTIO14_CLOCK	SMART I/O #14
4	PCLK_SMARTIO15_CLOCK	SMART I/O #15
5	PCLK_SMARTIO17_CLOCK	SMART I/O #17
6	PCLK_CANFD0_CLOCK_CAN0	CAN0, Channel #0
7	PCLK_CANFD0_CLOCK_CAN1	CAN0, Channel #1
8	PCLK_CANFD0_CLOCK_CAN2	CAN0, Channel #2
9	PCLK_CANFD0_CLOCK_CAN3	CAN0, Channel #3
10	PCLK_CANFD1_CLOCK_CAN0	CAN1, Channel #0
11	PCLK_CANFD1_CLOCK_CAN1	CAN1, Channel #1
12	PCLK_CANFD1_CLOCK_CAN2	CAN1, Channel #2
13	PCLK_CANFD1_CLOCK_CAN3	CAN1, Channel #3
14	PCLK_LIN0_CLOCK_CH_EN0	LIN0, Channel #0
15	PCLK_LIN0_CLOCK_CH_EN1	LIN0, Channel #1
16	PCLK_LIN0_CLOCK_CH_EN2	LIN0, Channel #2
17	PCLK_LIN0_CLOCK_CH_EN3	LIN0, Channel #3
18	PCLK_LIN0_CLOCK_CH_EN4	LIN0, Channel #4
19	PCLK_LIN0_CLOCK_CH_EN5	LIN0, Channel #5
20	PCLK_LIN0_CLOCK_CH_EN6	LIN0, Channel #6
21	PCLK_LIN0_CLOCK_CH_EN7	LIN0, Channel #7
22	PCLK_LIN0_CLOCK_CH_EN8	LIN0, Channel #8
23	PCLK_LIN0_CLOCK_CH_EN9	LIN0, Channel #9
24	PCLK_LIN0_CLOCK_CH_EN10	LIN0, Channel #10
25	PCLK_LIN0_CLOCK_CH_EN11	LIN0, Channel #11
26	PCLK_CXPI0_CLOCK_CH_EN0	CXPI0 Channel #0
27	PCLK_CXPI0_CLOCK_CH_EN1	CXPI0 Channel #1
28	PCLK_CXPI0_CLOCK_CH_EN2	CXPI0 Channel #2
29	PCLK_CXPI0_CLOCK_CH_EN3	CXPI0 Channel #3
30	PCLK_SCB0_CLOCK	SCB0
31	PCLK_SCB1_CLOCK	SCB1

（表格续下页.....）

表 23 （续） 外设时钟分配

Output	Destination	Description
32	PCLK_SCB2_CLOCK	SCB2
33	PCLK_SCB3_CLOCK	SCB3
34	PCLK_SCB4_CLOCK	SCB4
35	PCLK_SCB5_CLOCK	SCB5
36	PCLK_SCB6_CLOCK	SCB6
37	PCLK_SCB7_CLOCK	SCB7
38	PCLK_PASS0_CLOCK_SAR0	SAR0
39	PCLK_PASS0_CLOCK_SAR1	SAR1
40	PCLK_PASS0_CLOCK_SAR2	SAR2
41	PCLK_TCPWM0_CLOCKS0	TCPWM0 Group #0, Counter #0
42	PCLK_TCPWM0_CLOCKS1	TCPWM0 Group #0, Counter #1
43	PCLK_TCPWM0_CLOCKS2	TCPWM0 Group #0, Counter #2
44	PCLK_TCPWM0_CLOCKS3	TCPWM0 Group #0, Counter #3
45	PCLK_TCPWM0_CLOCKS4	TCPWM0 Group #0, Counter #4
46	PCLK_TCPWM0_CLOCKS5	TCPWM0 Group #0, Counter #5
47	PCLK_TCPWM0_CLOCKS6	TCPWM0 Group #0, Counter #6
48	PCLK_TCPWM0_CLOCKS7	TCPWM0 Group #0, Counter #7
49	PCLK_TCPWM0_CLOCKS8	TCPWM0 Group #0, Counter #8
50	PCLK_TCPWM0_CLOCKS9	TCPWM0 Group #0, Counter #9
51	PCLK_TCPWM0_CLOCKS10	TCPWM0 Group #0, Counter #10
52	PCLK_TCPWM0_CLOCKS11	TCPWM0 Group #0, Counter #11
53	PCLK_TCPWM0_CLOCKS12	TCPWM0 Group #0, Counter #12
54	PCLK_TCPWM0_CLOCKS13	TCPWM0 Group #0, Counter #13
55	PCLK_TCPWM0_CLOCKS14	TCPWM0 Group #0, Counter #14
56	PCLK_TCPWM0_CLOCKS15	TCPWM0 Group #0, Counter #15
57	PCLK_TCPWM0_CLOCKS16	TCPWM0 Group #0, Counter #16
58	PCLK_TCPWM0_CLOCKS17	TCPWM0 Group #0, Counter #17
59	PCLK_TCPWM0_CLOCKS18	TCPWM0 Group #0, Counter #18
60	PCLK_TCPWM0_CLOCKS19	TCPWM0 Group #0, Counter #19
61	PCLK_TCPWM0_CLOCKS20	TCPWM0 Group #0, Counter #20
62	PCLK_TCPWM0_CLOCKS21	TCPWM0 Group #0, Counter #21
63	PCLK_TCPWM0_CLOCKS22	TCPWM0 Group #0, Counter #22
64	PCLK_TCPWM0_CLOCKS23	TCPWM0 Group #0, Counter #23

（表格续下页.....）

表 23 （续）外设时钟分配

Output	Destination	Description
65	PCLK_TCPWM0_CLOCKS24	TCPWM0 Group #0, Counter #24
66	PCLK_TCPWM0_CLOCKS25	TCPWM0 Group #0, Counter #25
67	PCLK_TCPWM0_CLOCKS26	TCPWM0 Group #0, Counter #26
68	PCLK_TCPWM0_CLOCKS27	TCPWM0 Group #0, Counter #27
69	PCLK_TCPWM0_CLOCKS28	TCPWM0 Group #0, Counter #28
70	PCLK_TCPWM0_CLOCKS29	TCPWM0 Group #0, Counter #29
71	PCLK_TCPWM0_CLOCKS30	TCPWM0 Group #0, Counter #30
72	PCLK_TCPWM0_CLOCKS31	TCPWM0 Group #0, Counter #31
73	PCLK_TCPWM0_CLOCKS32	TCPWM0 Group #0, Counter #32
74	PCLK_TCPWM0_CLOCKS33	TCPWM0 Group #0, Counter #33
75	PCLK_TCPWM0_CLOCKS34	TCPWM0 Group #0, Counter #34
76	PCLK_TCPWM0_CLOCKS35	TCPWM0 Group #0, Counter #35
77	PCLK_TCPWM0_CLOCKS36	TCPWM0 Group #0, Counter #36
78	PCLK_TCPWM0_CLOCKS37	TCPWM0 Group #0, Counter #37
79	PCLK_TCPWM0_CLOCKS38	TCPWM0 Group #0, Counter #38
80	PCLK_TCPWM0_CLOCKS39	TCPWM0 Group #0, Counter #39
81	PCLK_TCPWM0_CLOCKS40	TCPWM0 Group #0, Counter #40
82	PCLK_TCPWM0_CLOCKS41	TCPWM0 Group #0, Counter #41
83	PCLK_TCPWM0_CLOCKS42	TCPWM0 Group #0, Counter #42
84	PCLK_TCPWM0_CLOCKS43	TCPWM0 Group #0, Counter #43
85	PCLK_TCPWM0_CLOCKS44	TCPWM0 Group #0, Counter #44
86	PCLK_TCPWM0_CLOCKS45	TCPWM0 Group #0, Counter #45
87	PCLK_TCPWM0_CLOCKS46	TCPWM0 Group #0, Counter #46
88	PCLK_TCPWM0_CLOCKS47	TCPWM0 Group #0, Counter #47
89	PCLK_TCPWM0_CLOCKS48	TCPWM0 Group #0, Counter #48
90	PCLK_TCPWM0_CLOCKS49	TCPWM0 Group #0, Counter #49
91	PCLK_TCPWM0_CLOCKS50	TCPWM0 Group #0, Counter #50
92	PCLK_TCPWM0_CLOCKS51	TCPWM0 Group #0, Counter #51
93	PCLK_TCPWM0_CLOCKS52	TCPWM0 Group #0, Counter #52
94	PCLK_TCPWM0_CLOCKS53	TCPWM0 Group #0, Counter #53
95	PCLK_TCPWM0_CLOCKS54	TCPWM0 Group #0, Counter #54
96	PCLK_TCPWM0_CLOCKS55	TCPWM0 Group #0, Counter #55
97	PCLK_TCPWM0_CLOCKS56	TCPWM0 Group #0, Counter #56

（表格续下页……）

表 23 （续） 外设时钟分配

Output	Destination	Description
98	PCLK_TCPWM0_CLOCKS57	TCPWM0 Group #0, Counter #57
99	PCLK_TCPWM0_CLOCKS58	TCPWM0 Group #0, Counter #58
100	PCLK_TCPWM0_CLOCKS59	TCPWM0 Group #0, Counter #59
101	PCLK_TCPWM0_CLOCKS60	TCPWM0 Group #0, Counter #60
102	PCLK_TCPWM0_CLOCKS61	TCPWM0 Group #0, Counter #61
103	PCLK_TCPWM0_CLOCKS62	TCPWM0 Group #0, Counter #62
104	PCLK_TCPWM0_CLOCKS256	TCPWM0 Group #1, Counter #0
105	PCLK_TCPWM0_CLOCKS257	TCPWM0 Group #1, Counter #1
106	PCLK_TCPWM0_CLOCKS258	TCPWM0 Group #1, Counter #2
107	PCLK_TCPWM0_CLOCKS259	TCPWM0 Group #1, Counter #3
108	PCLK_TCPWM0_CLOCKS260	TCPWM0 Group #1, Counter #4
109	PCLK_TCPWM0_CLOCKS261	TCPWM0 Group #1, Counter #5
110	PCLK_TCPWM0_CLOCKS262	TCPWM0 Group #1, Counter #6
111	PCLK_TCPWM0_CLOCKS263	TCPWM0 Group #1, Counter #7
112	PCLK_TCPWM0_CLOCKS264	TCPWM0 Group #1, Counter #8
113	PCLK_TCPWM0_CLOCKS265	TCPWM0 Group #1, Counter #9
114	PCLK_TCPWM0_CLOCKS266	TCPWM0 Group #1, Counter #10
115	PCLK_TCPWM0_CLOCKS267	TCPWM0 Group #1, Counter #11
116	PCLK_TCPWM0_CLOCKS512	TCPWM0 Group #2, Counter #0
117	PCLK_TCPWM0_CLOCKS513	TCPWM0 Group #2, Counter #1
118	PCLK_TCPWM0_CLOCKS514	TCPWM0 Group #2, Counter #2
119	PCLK_TCPWM0_CLOCKS515	TCPWM0 Group #2, Counter #3
120	PCLK_TCPWM0_CLOCKS516	TCPWM0 Group #2, Counter #4
121	PCLK_TCPWM0_CLOCKS517	TCPWM0 Group #2, Counter #5
122	PCLK_TCPWM0_CLOCKS518	TCPWM0 Group #2, Counter #6
123	PCLK_TCPWM0_CLOCKS519	TCPWM0 Group #2, Counter #7

22 故障

表 24 故障分配

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ SMPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation.
1	CPUSS_MPU_VIO_1	CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_MPU_VIO_16	CM4 system bus AHB-Lite interface MPU violation. See CPUSS_MPU_VIO_0 description
17	CPUSS_MPU_VIO_17	CM4 code bus AHB-Lite interface MPU violation for non flash controller accesses. See CPUSS_MPU_VIO_0 description.
18	CPUSS_MPU_VIO_18	CM4 code bus AHB-Lite interface MPU violation for flash controller accesses. See CPUSS_MPU_VIO_0 description.
26	PERI_PERI_C_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
27	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation

（表格续下页……）

表 24 （续） 故障分配

Fault	Source	Description
28	PERI_MS_VIO_0	CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": master interface, PPU violation, "1": timeout detected, "2": bus error, other: undefined.
29	PERI_MS_VIO_1	CM4 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_2	P-DMA0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
31	PERI_MS_VIO_3	P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
32	PERI_GROUP_VIO_0	Peripheral Group #0 violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.

（表格续下页……）

表 24 （续） 故障分配

Fault	Source	Description
37	PERI_GROUP_VIO_5	Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERROR	Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERROR	Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.

（表格续下页……）

表 24 （续）故障分配

Fault	Source	Description
56	CPUSS_FLASHC_CM4_CA_C_ECC	Flash controller CM4 cache correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
57	CPUSS_FLASHC_CM4_CA_NC_ECC	Flash controller CM4 cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
64	CPUSS_CRYPTO_C_ECC	Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.
65	CPUSS_CRYPTO_NC_ECC	CRYPTO memory non-correctable ECC violation. See CPUSS_CRYPTO_C_ECC description.
70	CPUSS_DW0_C_ECC	P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
71	CPUSS_DW0_NC_ECC	P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
72	CPUSS_DW1_C_ECC	P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
73	CPUSS_DW1_NC_ECC	P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
74	CPUSS_FM_SRAM_C_ECC	Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
75	CPUSS_FM_SRAM_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.

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表 24 （续）故障分配

Fault	Source	Description
80	CANFD_0_CAN_C_ECC	CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.
81	CANFD_0_CAN_NC_ECC	CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
82	CANFD_1_CAN_C_ECC	CAN1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description.
83	CANFD_1_CAN_NC_ECC	CAN1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDDA DATA[1]: OVD on VDDA DATA[16]: LVD/HVD #1 DATA0[17]: LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT

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表 24 （续） 故障分配

Fault	Source	Description
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description.

23 外设保护单元固定结构对

保护对由一对 PPU 结构、一个主机和一个从机结构组成。主结构保护从机结构，从机结构保护外设寄存器等资源，或外设本身。

表 25 PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
0	PERI_MS_PPU_FX_PERI_MAIN	0x40000000	0x00002000	Peripheral interconnect main
1	PERI_MS_PPU_FX_PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_MS_PPU_FX_PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral group #0 main
3	PERI_MS_PPU_FX_PERI_GR1_GROUP	0x40004030	0x00000004	Peripheral group #1 main
4	PERI_MS_PPU_FX_PERI_GR2_GROUP	0x40004050	0x00000004	Peripheral group #2 main
5	PERI_MS_PPU_FX_PERI_GR3_GROUP	0x40004060	0x00000020	Peripheral group #3 main
6	PERI_MS_PPU_FX_PERI_GR5_GROUP	0x400040A0	0x00000020	Peripheral group #5 main
7	PERI_MS_PPU_FX_PERI_GR6_GROUP	0x400040C0	0x00000020	Peripheral group #6 main
8	PERI_MS_PPU_FX_PERI_GR9_GROUP	0x40004120	0x00000020	Peripheral group #9 main
9	PERI_MS_PPU_FX_PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
10	PERI_MS_PPU_FX_CRYPTO_MAIN	0x40100000	0x00000400	Crypto main
11	PERI_MS_PPU_FX_CRYPTO_CRYPTO	0x40101000	0x00000800	Crypto MMIO (memory mapped I/O)
12	PERI_MS_PPU_FX_CRYPTO_BOOT	0x40102000	0x00000100	Crypto boot
13	PERI_MS_PPU_FX_CRYPTO_KEY0	0x40102100	0x00000004	Crypto Key #0
14	PERI_MS_PPU_FX_CRYPTO_KEY1	0x40102120	0x00000004	Crypto Key #1
15	PERI_MS_PPU_FX_CRYPTO_BUF	0x40108000	0x00002000	Crypto buffer
16	PERI_MS_PPU_FX_CPUSS_CM4	0x40200000	0x00000400	CM4 CPU core
17	PERI_MS_PPU_FX_CPUSS_CM0	0x40201000	0x00001000	CM0+ CPU core

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
18	PERI_MS_PPU_FX_CPUSS_BOOT[1)]	0x40202000	0x00000200	CPUSS boot
19	PERI_MS_PPU_FX_CPUSS_CM0_INT	0x40208000	0x00000800	CPUSS CM0+ interrupts
20	PERI_MS_PPU_FX_CPUSS_CM4_INT	0x4020A000	0x00000800	CPUSS CM4 interrupts
21	PERI_MS_PPU_FX_FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUSS fault structure #0 main
22	PERI_MS_PPU_FX_FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUSS fault structure #1 main
23	PERI_MS_PPU_FX_FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS fault structure #2 main
24	PERI_MS_PPU_FX_FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS fault structure #3 main
25	PERI_MS_PPU_FX_IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC structure #0
26	PERI_MS_PPU_FX_IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC structure #1
27	PERI_MS_PPU_FX_IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC structure #2
28	PERI_MS_PPU_FX_IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC structure #3
29	PERI_MS_PPU_FX_IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC structure #4
30	PERI_MS_PPU_FX_IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC structure #5
31	PERI_MS_PPU_FX_IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC structure #6
32	PERI_MS_PPU_FX_IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC structure #7
33	PERI_MS_PPU_FX_IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC interrupt structure #0
34	PERI_MS_PPU_FX_IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC interrupt structure #1
35	PERI_MS_PPU_FX_IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC interrupt structure #2
36	PERI_MS_PPU_FX_IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC interrupt structure #3

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
37	PERI_MS_PPU_FX_IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC interrupt structure #4
38	PERI_MS_PPU_FX_IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC interrupt structure #5
39	PERI_MS_PPU_FX_IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC Interrupt Structure #6
40	PERI_MS_PPU_FX_IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC Interrupt Structure #7
41	PERI_MS_PPU_FX_PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection SMPU main
42	PERI_MS_PPU_FX_PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
43	PERI_MS_PPU_FX_PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
44	PERI_MS_PPU_FX_PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
45	PERI_MS_PPU_FX_FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
46	PERI_MS_PPU_FX_FLASHC_CMD	0x40240008	0x00000004	Flash controller command
47	PERI_MS_PPU_FX_FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
48	PERI_MS_PPU_FX_FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
49	PERI_MS_PPU_FX_FLASHC_CM4	0x40240480	0x00000080	Flash controller CM4
50	PERI_MS_PPU_FX_FLASHC_CRYPTO	0x40240500	0x00000004	Flash controller Crypto
51	PERI_MS_PPU_FX_FLASHC_DW0	0x40240580	0x00000004	Flash controller P-DMA0
52	PERI_MS_PPU_FX_FLASHC_DW1	0x40240600	0x00000004	Flash controller P-DMA1
53	PERI_MS_PPU_FX_FLASHC_DMAC	0x40240680	0x00000004	Flash controller M-DMA0
54	PERI_MS_PPU_FX_FLASHC_FlashMgmt[1)]	0x4024F000	0x00000080	Flash management
55	PERI_MS_PPU_FX_FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller code-flash safety

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
56	PERI_MS_PPU_FX_FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work-flash safety
57	PERI_MS_PPU_FX_SRSS_GENERAL	0x40260000	0x00000400	SRSS general
58	PERI_MS_PPU_FX_SRSS_MAIN	0x40261000	0x00001000	SRSS main
59	PERI_MS_PPU_FX_SRSS_SECURE	0x40262000	0x00002000	SRSS secure
60	PERI_MS_PPU_FX_MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
61	PERI_MS_PPU_FX_MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
62	PERI_MS_PPU_FX_MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
63	PERI_MS_PPU_FX_MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
64	PERI_MS_PPU_FX_WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
65	PERI_MS_PPU_FX_WDT_MAIN	0x4026C040	0x00000020	System WDT main
66	PERI_MS_PPU_FX_BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
67	PERI_MS_PPU_FX_DW0_DW	0x40280000	0x00000100	P-DMA0 main
68	PERI_MS_PPU_FX_DW1_DW	0x40290000	0x00000100	P-DMA1 main
69	PERI_MS_PPU_FX_DW0_DW_CRC	0x40280100	0x00000080	P-DMA0 CRC
70	PERI_MS_PPU_FX_DW1_DW_CRC	0x40290100	0x00000080	P-DMA1 CRC
71	PERI_MS_PPU_FX_DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA0 Channel #0
72	PERI_MS_PPU_FX_DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA0 Channel #1
73	PERI_MS_PPU_FX_DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA0 Channel #2
74	PERI_MS_PPU_FX_DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA0 Channel #3

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
75	PERI_MS_PPU_FX_DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA0 Channel #4
76	PERI_MS_PPU_FX_DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA0 Channel #5
77	PERI_MS_PPU_FX_DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA0 Channel #6
78	PERI_MS_PPU_FX_DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA0 Channel #7
79	PERI_MS_PPU_FX_DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA0 Channel #8
80	PERI_MS_PPU_FX_DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA0 Channel #9
81	PERI_MS_PPU_FX_DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA0 Channel #10
82	PERI_MS_PPU_FX_DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA0 Channel #11
83	PERI_MS_PPU_FX_DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA0 Channel #12
84	PERI_MS_PPU_FX_DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA0 Channel #13
85	PERI_MS_PPU_FX_DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA0 Channel #14
86	PERI_MS_PPU_FX_DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA0 Channel #15
87	PERI_MS_PPU_FX_DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA0 Channel #16
88	PERI_MS_PPU_FX_DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA0 Channel #17
89	PERI_MS_PPU_FX_DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA0 Channel #18
90	PERI_MS_PPU_FX_DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA0 Channel #19
91	PERI_MS_PPU_FX_DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA0 Channel #20
92	PERI_MS_PPU_FX_DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA0 Channel #21
93	PERI_MS_PPU_FX_DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA0 Channel #22

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表 25 （续）PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
94	PERI_MS_PPU_FX_DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA0 Channel #23
95	PERI_MS_PPU_FX_DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA0 Channel #24
96	PERI_MS_PPU_FX_DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA0 Channel #25
97	PERI_MS_PPU_FX_DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA0 Channel #26
98	PERI_MS_PPU_FX_DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA0 Channel #27
99	PERI_MS_PPU_FX_DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA0 Channel #28
100	PERI_MS_PPU_FX_DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA0 Channel #29
101	PERI_MS_PPU_FX_DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA0 Channel #30
102	PERI_MS_PPU_FX_DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA0 Channel #31
103	PERI_MS_PPU_FX_DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA0 Channel #32
104	PERI_MS_PPU_FX_DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA0 Channel #33
105	PERI_MS_PPU_FX_DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA0 Channel #34
106	PERI_MS_PPU_FX_DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA0 Channel #35
107	PERI_MS_PPU_FX_DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA0 Channel #36
108	PERI_MS_PPU_FX_DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA0 Channel #37
109	PERI_MS_PPU_FX_DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA0 Channel #38
110	PERI_MS_PPU_FX_DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA0 Channel #39
111	PERI_MS_PPU_FX_DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA0 Channel #40
112	PERI_MS_PPU_FX_DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA0 Channel #41

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
113	PERI_MS_PPU_FX_DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA0 Channel #42
114	PERI_MS_PPU_FX_DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA0 Channel #43
115	PERI_MS_PPU_FX_DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA0 Channel #44
116	PERI_MS_PPU_FX_DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA0 Channel #45
117	PERI_MS_PPU_FX_DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA0 Channel #46
118	PERI_MS_PPU_FX_DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA0 Channel #47
119	PERI_MS_PPU_FX_DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA0 Channel #48
120	PERI_MS_PPU_FX_DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA0 Channel #49
121	PERI_MS_PPU_FX_DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA0 Channel #50
122	PERI_MS_PPU_FX_DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA0 Channel #51
123	PERI_MS_PPU_FX_DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA0 Channel #52
124	PERI_MS_PPU_FX_DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA0 Channel #53
125	PERI_MS_PPU_FX_DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA0 Channel #54
126	PERI_MS_PPU_FX_DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA0 Channel #55
127	PERI_MS_PPU_FX_DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA0 Channel #56
128	PERI_MS_PPU_FX_DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA0 Channel #57
129	PERI_MS_PPU_FX_DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA0 Channel #58
130	PERI_MS_PPU_FX_DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA0 Channel #59
131	PERI_MS_PPU_FX_DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA0 Channel #60

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	地址	Size	Description
132	PERI_MS_PPU_FX_DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA0 Channel #61
133	PERI_MS_PPU_FX_DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA0 Channel #62
134	PERI_MS_PPU_FX_DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA0 Channel #63
135	PERI_MS_PPU_FX_DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA0 Channel #64
136	PERI_MS_PPU_FX_DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA0 Channel #65
137	PERI_MS_PPU_FX_DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA0 Channel #66
138	PERI_MS_PPU_FX_DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA0 Channel #67
139	PERI_MS_PPU_FX_DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA0 Channel #68
140	PERI_MS_PPU_FX_DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA0 Channel #69
141	PERI_MS_PPU_FX_DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA0 Channel #70
142	PERI_MS_PPU_FX_DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA0 Channel #71
143	PERI_MS_PPU_FX_DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA0 Channel #72
144	PERI_MS_PPU_FX_DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA0 Channel #73
145	PERI_MS_PPU_FX_DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA0 Channel #74
146	PERI_MS_PPU_FX_DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA0 Channel #75
147	PERI_MS_PPU_FX_DW0_CH_STRUCT76_CH	0x40289300	0x00000040	P-DMA0 Channel #76
148	PERI_MS_PPU_FX_DW0_CH_STRUCT77_CH	0x40289340	0x00000040	P-DMA0 Channel #77
149	PERI_MS_PPU_FX_DW0_CH_STRUCT78_CH	0x40289380	0x00000040	P-DMA0 Channel #78
150	PERI_MS_PPU_FX_DW0_CH_STRUCT79_CH	0x402893C0	0x00000040	P-DMA0 Channel #79

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
151	PERI_MS_PPU_FX_DW0_CH_STRUCT80_CH	0x40289400	0x00000040	P-DMA0 Channel #80
152	PERI_MS_PPU_FX_DW0_CH_STRUCT81_CH	0x40289440	0x00000040	P-DMA0 Channel #81
153	PERI_MS_PPU_FX_DW0_CH_STRUCT82_CH	0x40289480	0x00000040	P-DMA0 Channel #82
154	PERI_MS_PPU_FX_DW0_CH_STRUCT83_CH	0x402894C0	0x00000040	P-DMA0 Channel #83
155	PERI_MS_PPU_FX_DW0_CH_STRUCT84_CH	0x40289500	0x00000040	P-DMA0 Channel #84
156	PERI_MS_PPU_FX_DW0_CH_STRUCT85_CH	0x40289540	0x00000040	P-DMA0 Channel #85
157	PERI_MS_PPU_FX_DW0_CH_STRUCT86_CH	0x40289580	0x00000040	P-DMA0 Channel #86
158	PERI_MS_PPU_FX_DW0_CH_STRUCT87_CH	0x402895C0	0x00000040	P-DMA0 Channel #87
159	PERI_MS_PPU_FX_DW0_CH_STRUCT88_CH	0x40289600	0x00000040	P-DMA0 Channel #88
160	PERI_MS_PPU_FX_DW0_CH_STRUCT89_CH	0x40289640	0x00000040	P-DMA0 Channel #89
161	PERI_MS_PPU_FX_DW0_CH_STRUCT90_CH	0x40289680	0x00000040	P-DMA0 Channel #90
162	PERI_MS_PPU_FX_DW0_CH_STRUCT91_CH	0x402896C0	0x00000040	P-DMA0 Channel #91
163	PERI_MS_PPU_FX_DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA1 Channel #0
164	PERI_MS_PPU_FX_DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA1 Channel #1
165	PERI_MS_PPU_FX_DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA1 Channel #2
166	PERI_MS_PPU_FX_DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA1 Channel #3
167	PERI_MS_PPU_FX_DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA1 Channel #4
168	PERI_MS_PPU_FX_DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA1 Channel #5
169	PERI_MS_PPU_FX_DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA1 Channel #6

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
170	PERI_MS_PPU_FX_DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA1 Channel #7
171	PERI_MS_PPU_FX_DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA1 Channel #8
172	PERI_MS_PPU_FX_DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA1 Channel #9
173	PERI_MS_PPU_FX_DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA1 Channel #10
174	PERI_MS_PPU_FX_DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA1 Channel #11
175	PERI_MS_PPU_FX_DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA1 Channel #12
176	PERI_MS_PPU_FX_DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA1 Channel #13
177	PERI_MS_PPU_FX_DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA1 Channel #14
178	PERI_MS_PPU_FX_DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA1 Channel #15
179	PERI_MS_PPU_FX_DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA1 Channel #16
180	PERI_MS_PPU_FX_DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA1 Channel #17
181	PERI_MS_PPU_FX_DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA1 Channel #18
182	PERI_MS_PPU_FX_DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA1 Channel #19
183	PERI_MS_PPU_FX_DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA1 Channel #20
184	PERI_MS_PPU_FX_DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA1 Channel #21
185	PERI_MS_PPU_FX_DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA1 Channel #22
186	PERI_MS_PPU_FX_DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA1 Channel #23
187	PERI_MS_PPU_FX_DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA1 Channel #24
188	PERI_MS_PPU_FX_DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA1 Channel #25

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
189	PERI_MS_PPU_FX_DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA1 Channel #26
190	PERI_MS_PPU_FX_DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA1 Channel #27
191	PERI_MS_PPU_FX_DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA1 Channel #28
192	PERI_MS_PPU_FX_DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA1 Channel #29
193	PERI_MS_PPU_FX_DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA1 Channel #30
194	PERI_MS_PPU_FX_DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA1 Channel #31
195	PERI_MS_PPU_FX_DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA1 Channel #32
196	PERI_MS_PPU_FX_DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA1 Channel #33
197	PERI_MS_PPU_FX_DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA1 Channel #34
198	PERI_MS_PPU_FX_DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA1 Channel #35
199	PERI_MS_PPU_FX_DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA1 Channel #36
200	PERI_MS_PPU_FX_DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA1 Channel #37
201	PERI_MS_PPU_FX_DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA1 Channel #38
202	PERI_MS_PPU_FX_DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA1 Channel #39
203	PERI_MS_PPU_FX_DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA1 Channel #40
204	PERI_MS_PPU_FX_DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA1 Channel #41
205	PERI_MS_PPU_FX_DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA1 Channel #42
206	PERI_MS_PPU_FX_DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA1 Channel #43
207	PERI_MS_PPU_FX_DMAC_TOP	0x402A0000	0x00000010	M-DMA0 main

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
208	PERI_MS_PPU_FX_DMAC_CH0_CH	0x402A1000	0x00000100	M-DMA0 Channel #0
209	PERI_MS_PPU_FX_DMAC_CH1_CH	0x402A1100	0x00000100	M-DMA0 Channel #1
210	PERI_MS_PPU_FX_DMAC_CH2_CH	0x402A1200	0x00000100	M-DMA0 Channel #2
211	PERI_MS_PPU_FX_DMAC_CH3_CH	0x402A1300	0x00000100	M-DMA0 Channel #3
212	PERI_MS_PPU_FX_EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
213	PERI_MS_PPU_FX_EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
214	PERI_MS_PPU_FX_BIST	0x402F0000	0x00001000	Built-in self test
215	PERI_MS_PPU_FX_HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOm Port #0
216	PERI_MS_PPU_FX_HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOm Port #1
217	PERI_MS_PPU_FX_HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOm Port #2
218	PERI_MS_PPU_FX_HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOm Port #3
219	PERI_MS_PPU_FX_HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOm Port #4
220	PERI_MS_PPU_FX_HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOm Port #1
221	PERI_MS_PPU_FX_HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOm Port #1
222	PERI_MS_PPU_FX_HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOm Port #1
223	PERI_MS_PPU_FX_HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOm Port #8
224	PERI_MS_PPU_FX_HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOm Port #9
225	PERI_MS_PPU_FX_HSIOM_PRT10_PRT	0x403000A0	0x00000008	HSIOm Port #10
226	PERI_MS_PPU_FX_HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOm Port #11

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
227	PERI_MS_PPU_FX_HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOm Port #12
228	PERI_MS_PPU_FX_HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOm Port #13
229	PERI_MS_PPU_FX_HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOm Port #14
230	PERI_MS_PPU_FX_HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOm Port #15
231	PERI_MS_PPU_FX_HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOm Port #16
232	PERI_MS_PPU_FX_HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOm Port #17
233	PERI_MS_PPU_FX_HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOm Port #18
234	PERI_MS_PPU_FX_HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOm Port #19
235	PERI_MS_PPU_FX_HSIOM_PRT20_PRT	0x40300140	0x00000008	HSIOm Port #20
236	PERI_MS_PPU_FX_HSIOM_PRT21_PRT	0x40300150	0x00000008	HSIOm Port #21
237	PERI_MS_PPU_FX_HSIOM_PRT22_PRT	0x40300160	0x00000008	HSIOm Port #22
238	PERI_MS_PPU_FX_HSIOM_PRT23_PRT	0x40300170	0x00000008	HSIOm Port #23
239	PERI_MS_PPU_FX_HSIOM_AMUX	0x40302000	0x00000010	HSIOm Analog multiplexer
240	PERI_MS_PPU_FX_HSIOM_MON	0x40302200	0x00000010	HSIOm monitor
241	PERI_MS_PPU_FX_HSIOM_ALTJTAG	0x40302240	0x00000004	HSIOm Alternate JTAG
242	PERI_MS_PPU_FX_GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_ENH Port #0
243	PERI_MS_PPU_FX_GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD Port #1
244	PERI_MS_PPU_FX_GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD Port #2
245	PERI_MS_PPU_FX_GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_STD Port #3

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
246	PERI_MS_PPU_FX_GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD Port #4
247	PERI_MS_PPU_FX_GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_STD Port #5
248	PERI_MS_PPU_FX_GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_STD Port #6
249	PERI_MS_PPU_FX_GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_STD Port #7
250	PERI_MS_PPU_FX_GPIO_PRT8_PRT	0x40310400	0x00000040	GPIO_STD Port #8
251	PERI_MS_PPU_FX_GPIO_PRT9_PRT	0x40310480	0x00000040	GPIO_STD Port #9
252	PERI_MS_PPU_FX_GPIO_PRT10_PRT	0x40310500	0x00000040	GPIO_STD Port #10
253	PERI_MS_PPU_FX_GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_STD Port #11
254	PERI_MS_PPU_FX_GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_STD Port #12
255	PERI_MS_PPU_FX_GPIO_PRT13_PRT	0x40310680	0x00000040	GPIO_STD Port #13
256	PERI_MS_PPU_FX_GPIO_PRT14_PRT	0x40310700	0x00000040	GPIO_STD Port #14
257	PERI_MS_PPU_FX_GPIO_PRT15_PRT	0x40310780	0x00000040	GPIO_STD Port #15
258	PERI_MS_PPU_FX_GPIO_PRT16_PRT	0x40310800	0x00000040	GPIO_STD Port #16
259	PERI_MS_PPU_FX_GPIO_PRT17_PRT	0x40310880	0x00000040	GPIO_STD Port #17
260	PERI_MS_PPU_FX_GPIO_PRT18_PRT	0x40310900	0x00000040	GPIO_STD Port #18
261	PERI_MS_PPU_FX_GPIO_PRT19_PRT	0x40310980	0x00000040	GPIO_STD Port #19
262	PERI_MS_PPU_FX_GPIO_PRT20_PRT	0x40310A00	0x00000040	GPIO_STD Port #20
263	PERI_MS_PPU_FX_GPIO_PRT21_PRT	0x40310A80	0x00000040	GPIO_STD Port #21
264	PERI_MS_PPU_FX_GPIO_PRT22_PRT	0x40310B00	0x00000040	GPIO_STD Port #22

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
265	PERI_MS_PPU_FX_GPIO_PRT23_PRT	0x40310B80	0x00000040	GPIO_STD Port #23
266	PERI_MS_PPU_FX_GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_ENH Port #0 configuration
267	PERI_MS_PPU_FX_GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD Port #1 configuration
268	PERI_MS_PPU_FX_GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD Port #2 configuration
269	PERI_MS_PPU_FX_GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_STD Port #3 configuration
270	PERI_MS_PPU_FX_GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD Port #4 configuration
271	PERI_MS_PPU_FX_GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_STD Port #5 configuration
272	PERI_MS_PPU_FX_GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_STD Port #6 configuration
273	PERI_MS_PPU_FX_GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_STD Port #7 configuration
274	PERI_MS_PPU_FX_GPIO_PRT8_CFG	0x40310440	0x00000020	GPIO_STD Port #8 configuration
275	PERI_MS_PPU_FX_GPIO_PRT9_CFG	0x403104C0	0x00000020	GPIO_STD Port #9 configuration
276	PERI_MS_PPU_FX_GPIO_PRT10_CFG	0x40310540	0x00000020	GPIO_STD Port #10 configuration
277	PERI_MS_PPU_FX_GPIO_PRT11_CFG	0x403105C0	0x00000020	GPIO_STD Port #11 configuration
278	PERI_MS_PPU_FX_GPIO_PRT12_CFG	0x40310640	0x00000020	GPIO_STD Port #12 configuration
279	PERI_MS_PPU_FX_GPIO_PRT13_CFG	0x403106C0	0x00000020	GPIO_STD Port #13 configuration
280	PERI_MS_PPU_FX_GPIO_PRT14_CFG	0x40310740	0x00000020	GPIO_STD Port #14 configuration
281	PERI_MS_PPU_FX_GPIO_PRT15_CFG	0x403107C0	0x00000020	GPIO_STD Port #15 configuration
282	PERI_MS_PPU_FX_GPIO_PRT16_CFG	0x40310840	0x00000020	GPIO_STD Port #16 configuration
283	PERI_MS_PPU_FX_GPIO_PRT17_CFG	0x403108C0	0x00000020	GPIO_STD Port #17 configuration

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
284	PERI_MS_PPU_FX_GPIO_PRT18_CFG	0x40310940	0x00000020	GPIO_STD Port #18 configuration
285	PERI_MS_PPU_FX_GPIO_PRT19_CFG	0x403109C0	0x00000020	GPIO_STD Port #19 configuration
286	PERI_MS_PPU_FX_GPIO_PRT20_CFG	0x40310A40	0x00000020	GPIO_STD Port #20 configuration
287	PERI_MS_PPU_FX_GPIO_PRT21_CFG	0x40310AC0	0x00000020	GPIO_STD Port #21 configuration
288	PERI_MS_PPU_FX_GPIO_PRT22_CFG	0x40310B40	0x00000020	GPIO_STD Port #22 configuration
289	PERI_MS_PPU_FX_GPIO_PRT23_CFG	0x40310BC0	0x00000020	GPIO_STD Port #23 configuration
290	PERI_MS_PPU_FX_GPIO_GPIO	0x40314000	0x00000040	GPIO main
291	PERI_MS_PPU_FX_GPIO_TEST	0x40315000	0x00000008	GPIO test
292	PERI_MS_PPU_FX_SMARTIO_PRT12_PRT	0x40320C00	0x00000100	SMART I/O #12
293	PERI_MS_PPU_FX_SMARTIO_PRT13_PRT	0x40320D00	0x00000100	SMART I/O #13
294	PERI_MS_PPU_FX_SMARTIO_PRT14_PRT	0x40320E00	0x00000100	SMART I/O #14
295	PERI_MS_PPU_FX_SMARTIO_PRT15_PRT	0x40320F00	0x00000100	SMART I/O #15
296	PERI_MS_PPU_FX_SMARTIO_PRT17_PRT	0x40321100	0x00000100	SMART I/O #17
297	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT0_CNT	0x40380000	0x00000080	TCPWM0 Group #0, Counter #0
298	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT1_CNT	0x40380080	0x00000080	TCPWM0 Group #0, Counter #1
299	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT2_CNT	0x40380100	0x00000080	TCPWM0 Group #0, Counter #2
300	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT3_CNT	0x40380180	0x00000080	TCPWM0 Group #0, Counter #3
301	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT4_CNT	0x40380200	0x00000080	TCPWM0 Group #0, Counter #4
302	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT5_CNT	0x40380280	0x00000080	TCPWM0 Group #0, Counter #5

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
303	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT6_CNT	0x40380300	0x00000080	TCPWM0 Group #0, Counter #6
304	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT7_CNT	0x40380380	0x00000080	TCPWM0 Group #0, Counter #7
305	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT8_CNT	0x40384000	0x00000080	TCPWM0 Group #0, Counter #8
306	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT9_CNT	0x40384080	0x00000080	TCPWM0 Group #0, Counter #9
307	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT10_CNT	0x40385000	0x00000080	TCPWM0 Group #0, Counter #10
308	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT11_CNT	0x40385080	0x00000080	TCPWM0 Group #0, Counter #11
309	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT12_CNT	0x40386000	0x00000080	TCPWM0 Group #0, Counter #12
310	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT13_CNT	0x40386080	0x00000080	TCPWM0 Group #0, Counter #13
311	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT14_CNT	0x40387000	0x00000080	TCPWM0 Group #0, Counter #14
312	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT15_CNT	0x40387080	0x00000080	TCPWM0 Group #0, Counter #15
313	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT16_CNT	0x40388000	0x00000080	TCPWM0 Group #0, Counter #16
314	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT17_CNT	0x40388080	0x00000080	TCPWM0 Group #0, Counter #17
315	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT18_CNT	0x40389000	0x00000080	TCPWM0 Group #0, Counter #18
316	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT19_CNT	0x40389080	0x00000080	TCPWM0 Group #0, Counter #19
317	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT20_CNT	0x40380A00	0x00000080	TCPWM0 Group #0, Counter #20
318	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT21_CNT	0x40380A80	0x00000080	TCPWM0 Group #0, Counter #21
319	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT22_CNT	0x40380B00	0x00000080	TCPWM0 Group #0, Counter #22
320	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT23_CNT	0x40380B80	0x00000080	TCPWM0 Group #0, Counter #23
321	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT24_CNT	0x40380C00	0x00000080	TCPWM0 Group #0, Counter #24

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
322	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT25_CNT	0x40380C80	0x00000080	TCPWM0 Group #0, Counter #25
323	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT26_CNT	0x40380D00	0x00000080	TCPWM0 Group #0, Counter #26
324	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT27_CNT	0x40380D80	0x00000080	TCPWM0 Group #0, Counter #27
325	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT28_CNT	0x40380E00	0x00000080	TCPWM0 Group #0, Counter #28
326	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT29_CNT	0x40380E80	0x00000080	TCPWM0 Group #0, Counter #29
327	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT30_CNT	0x40380F00	0x00000080	TCPWM0 Group #0, Counter #30
328	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT31_CNT	0x40380F80	0x00000080	TCPWM0 Group #0, Counter #31
329	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT32_CNT	0x40381000	0x00000080	TCPWM0 Group #0, Counter #32
330	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT33_CNT	0x40381080	0x00000080	TCPWM0 Group #0, Counter #33
331	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT34_CNT	0x40381100	0x00000080	TCPWM0 Group #0, Counter #34
332	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT35_CNT	0x40381180	0x00000080	TCPWM0 Group #0, Counter #35
333	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT36_CNT	0x40381200	0x00000080	TCPWM0 Group #0, Counter #36
334	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT37_CNT	0x40381280	0x00000080	TCPWM0 Group #0, Counter #37
335	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT38_CNT	0x40381300	0x00000080	TCPWM0 Group #0, Counter #38
336	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT39_CNT	0x40381380	0x00000080	TCPWM0 Group #0, Counter #39
337	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT40_CNT	0x40381400	0x00000080	TCPWM0 Group #0, Counter #40
338	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT41_CNT	0x40381480	0x00000080	TCPWM0 Group #0, Counter #41
339	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT42_CNT	0x40381500	0x00000080	TCPWM0 Group #0, Counter #42
340	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT43_CNT	0x40381580	0x00000080	TCPWM0 Group #0, Counter #43

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
341	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT44_CNT	0x40381600	0x00000080	TCPWM0 Group #0, Counter #44
342	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT45_CNT	0x40381680	0x00000080	TCPWM0 Group #0, Counter #45
343	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT46_CNT	0x40381700	0x00000080	TCPWM0 Group #0, Counter #46
344	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT47_CNT	0x40381780	0x00000080	TCPWM0 Group #0, Counter #47
345	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT48_CNT	0x40381800	0x00000080	TCPWM0 Group #0, Counter #48
346	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT49_CNT	0x40381880	0x00000080	TCPWM0 Group #0, Counter #49
347	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT50_CNT	0x40381900	0x00000080	TCPWM0 Group #0, Counter #50
348	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT51_CNT	0x40381980	0x00000080	TCPWM0 Group #0, Counter #51
349	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT52_CNT	0x40381A00	0x00000080	TCPWM0 Group #0, Counter #52
350	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT53_CNT	0x40381A80	0x00000080	TCPWM0 Group #0, Counter #53
351	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT54_CNT	0x40381B00	0x00000080	TCPWM0 Group #0, Counter #54
352	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT55_CNT	0x40381B80	0x00000080	TCPWM0 Group #0, Counter #55
353	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT56_CNT	0x40381C00	0x00000080	TCPWM0 Group #0, Counter #56
354	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT57_CNT	0x40381C80	0x00000080	TCPWM0 Group #0, Counter #57
355	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT58_CNT	0x40381D00	0x00000080	TCPWM0 Group #0, Counter #58
356	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT59_CNT	0x40381D80	0x00000080	TCPWM0 Group #0, Counter #59
357	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT60_CNT	0x40381E00	0x00000080	TCPWM0 Group #0, Counter #60
358	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT61_CNT	0x40381E80	0x00000080	TCPWM0 Group #0, Counter #61
359	PERI_MS_PPU_FX_TCPWM0_GRP0_CNT62_CNT	0x40381F00	0x00000080	TCPWM0 Group #0, Counter #62

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
360	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT0_CNT	0x40388000	0x00000080	TCPWM0 Group #1, Counter #0
361	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT1_CNT	0x40388080	0x00000080	TCPWM0 Group #1, Counter #1
362	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT2_CNT	0x40388100	0x00000080	TCPWM0 Group #1, Counter #2
363	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT3_CNT	0x40388180	0x00000080	TCPWM0 Group #1, Counter #3
364	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT4_CNT	0x40388200	0x00000080	TCPWM0 Group #1, Counter #4
365	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT5_CNT	0x40388280	0x00000080	TCPWM0 Group #1, Counter #5
366	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT6_CNT	0x40388300	0x00000080	TCPWM0 Group #1, Counter #6
367	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT7_CNT	0x40388380	0x00000080	TCPWM0 Group #1, Counter #7
368	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT8_CNT	0x40388400	0x00000080	TCPWM0 Group #1, Counter #8
369	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT9_CNT	0x40388480	0x00000080	TCPWM0 Group #1, Counter #9
370	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT10_CNT	0x40388500	0x00000080	TCPWM0 Group #1, Counter #10
371	PERI_MS_PPU_FX_TCPWM0_GRP1_CNT11_CNT	0x40388580	0x00000080	TCPWM0 Group #1, Counter #11
372	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT0_CNT	0x40390000	0x00000080	TCPWM0 Group #2, Counter #0
373	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT1_CNT	0x40390080	0x00000080	TCPWM0 Group #2, Counter #1
374	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT2_CNT	0x40390100	0x00000080	TCPWM0 Group #2, Counter #2
375	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT3_CNT	0x40390180	0x00000080	TCPWM0 Group #2, Counter #3
376	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT4_CNT	0x40390200	0x00000080	TCPWM0 Group #2, Counter #4
377	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT5_CNT	0x40390280	0x00000080	TCPWM0 Group #2, Counter #5
378	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT6_CNT	0x40390300	0x00000080	TCPWM0 Group #2, Counter #6

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
379	PERI_MS_PPU_FX_TCPWM0_GRP2_CNT7_CNT	0x40390380	0x00000080	TCPWM0 Group #2, Counter #7
380	PERI_MS_PPU_FX_EVTGEN0	0x403F0000	0x00001000	Event generator #0
381	PERI_MS_PPU_FX_LIN0_MAIN	0x40500000	0x00000008	LIN0, main
382	PERI_MS_PPU_FX_LIN0_CH0_CH	0x40508000	0x00000100	LIN0, Channel #0
383	PERI_MS_PPU_FX_LIN0_CH1_CH	0x40508100	0x00000100	LIN0, Channel #1
384	PERI_MS_PPU_FX_LIN0_CH2_CH	0x40508200	0x00000100	LIN0, Channel #2
385	PERI_MS_PPU_FX_LIN0_CH3_CH	0x40508300	0x00000100	LIN0, Channel #3
386	PERI_MS_PPU_FX_LIN0_CH4_CH	0x40508400	0x00000100	LIN0, Channel #4
387	PERI_MS_PPU_FX_LIN0_CH5_CH	0x40508500	0x00000100	LIN0, Channel #5
388	PERI_MS_PPU_FX_LIN0_CH6_CH	0x40508600	0x00000100	LIN0, Channel #6
389	PERI_MS_PPU_FX_LIN0_CH7_CH	0x40508700	0x00000100	LIN0, Channel #7
390	PERI_MS_PPU_FX_LIN0_CH8_CH	0x40508800	0x00000100	LIN0, Channel #8
391	PERI_MS_PPU_FX_LIN0_CH9_CH	0x40508900	0x00000100	LIN0, Channel #9
392	PERI_MS_PPU_FX_LIN0_CH10_CH	0x40508A00	0x00000100	LIN0, Channel #10
393	PERI_MS_PPU_FX_LIN0_CH11_CH	0x40508B00	0x00000100	LIN0, Channel #11
394	PERI_MS_PPU_FX_CXPI0_MAIN	0x40510000	0x00000008	CXPI0, main
395	PERI_MS_PPU_FX_CXPI0_CH0_CH	0x40518000	0x00000100	CXPI0, Channel #0
396	PERI_MS_PPU_FX_CXPI0_CH1_CH	0x40518100	0x00000100	CXPI0, Channel #1
397	PERI_MS_PPU_FX_CXPI0_CH2_CH	0x40518200	0x00000100	CXPI0, Channel #2

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
398	PERI_MS_PPU_FX_CXPI0_CH3_CH	0x40518300	0x00000100	CXPI0, Channel #3
399	PERI_MS_PPU_FX_CANFD0_CH0_CH	0x40520000	0x00000200	CANFD0, Channel #0
400	PERI_MS_PPU_FX_CANFD0_CH1_CH	0x40520200	0x00000200	CANFD0, Channel #1
401	PERI_MS_PPU_FX_CANFD0_CH2_CH	0x40520400	0x00000200	CANFD0, Channel #2
402	PERI_MS_PPU_FX_CANFD0_CH3_CH	0x40520600	0x00000200	CANFD0, Channel #3
403	PERI_MS_PPU_FX_CANFD1_CH0_CH	0x40540000	0x00000200	CANFD1, Channel #0
404	PERI_MS_PPU_FX_CANFD1_CH1_CH	0x40540200	0x00000200	CANFD1, Channel #1
405	PERI_MS_PPU_FX_CANFD1_CH2_CH	0x40540400	0x00000200	CANFD1, Channel #2
406	PERI_MS_PPU_FX_CANFD1_CH3_CH	0x40540600	0x00000200	CANFD1, Channel #3
407	PERI_MS_PPU_FX_CANFD0_MAIN	0x40521000	0x00000100	CANFD0, main
408	PERI_MS_PPU_FX_CANFD1_MAIN	0x40541000	0x00000100	CANFD1, main
409	PERI_MS_PPU_FX_CANFD0_BUF	0x40530000	0x00010000	CANFD0, buffer
410	PERI_MS_PPU_FX_CANFD1_BUF	0x40550000	0x00010000	CANFD1, buffer
411	PERI_MS_PPU_FX_SCB0	0x40600000	0x00010000	SCB0
412	PERI_MS_PPU_FX_SCB1	0x40610000	0x00010000	SCB1
413	PERI_MS_PPU_FX_SCB2	0x40620000	0x00010000	SCB2
414	PERI_MS_PPU_FX_SCB3	0x40630000	0x00010000	SCB3
415	PERI_MS_PPU_FX_SCB4	0x40640000	0x00010000	SCB4
416	PERI_MS_PPU_FX_SCB5	0x40650000	0x00010000	SCB5

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23 Peripheral protection unit fixed structure pairs

表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
417	PERI_MS_PPU_FX_SCB6	0x40660000	0x00010000	SCB6
418	PERI_MS_PPU_FX_SCB7	0x40670000	0x00010000	SCB7
419	PERI_MS_PPU_FX_PASS0_SAR0_SAR	0x40900000	0x00000400	PASS0, SAR Channel #0
420	PERI_MS_PPU_FX_PASS0_SAR1_SAR	0x40901000	0x00000400	PASS0, SAR Channel #1
421	PERI_MS_PPU_FX_PASS0_SAR2_SAR	0x40902000	0x00000400	PASS0, SAR Channel #2
422	PERI_MS_PPU_FX_PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR0, Channel #0
423	PERI_MS_PPU_FX_PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR0, Channel #1
424	PERI_MS_PPU_FX_PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR0, Channel #2
425	PERI_MS_PPU_FX_PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR0, Channel #3
426	PERI_MS_PPU_FX_PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR0, Channel #4
427	PERI_MS_PPU_FX_PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR0, Channel #5
428	PERI_MS_PPU_FX_PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR0, Channel #6
429	PERI_MS_PPU_FX_PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR0, Channel #7
430	PERI_MS_PPU_FX_PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR0, Channel #8
431	PERI_MS_PPU_FX_PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR0, Channel #9
432	PERI_MS_PPU_FX_PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR0, Channel #10
433	PERI_MS_PPU_FX_PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR0, Channel #11
434	PERI_MS_PPU_FX_PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR0, Channel #12
435	PERI_MS_PPU_FX_PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR0, Channel #13

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
436	PERI_MS_PPU_FX_PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR0, Channel #14
437	PERI_MS_PPU_FX_PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR0, Channel #15
438	PERI_MS_PPU_FX_PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR0, Channel #16
439	PERI_MS_PPU_FX_PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR0, Channel #17
440	PERI_MS_PPU_FX_PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR0, Channel #18
441	PERI_MS_PPU_FX_PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR0, Channel #19
442	PERI_MS_PPU_FX_PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR0, Channel #20
443	PERI_MS_PPU_FX_PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR0, Channel #21
444	PERI_MS_PPU_FX_PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR0, Channel #22
445	PERI_MS_PPU_FX_PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR0, Channel #23
446	PERI_MS_PPU_FX_PASS0_SAR1_CH0_CH	0x40901800	0x00000040	SAR1, Channel #0
447	PERI_MS_PPU_FX_PASS0_SAR1_CH1_CH	0x40901840	0x00000040	SAR1, Channel #1
448	PERI_MS_PPU_FX_PASS0_SAR1_CH2_CH	0x40901880	0x00000040	SAR1, Channel #2
449	PERI_MS_PPU_FX_PASS0_SAR1_CH3_CH	0x409018C0	0x00000040	SAR1, Channel #3
450	PERI_MS_PPU_FX_PASS0_SAR1_CH4_CH	0x40901900	0x00000040	SAR1, Channel #4
451	PERI_MS_PPU_FX_PASS0_SAR1_CH5_CH	0x40901940	0x00000040	SAR1, Channel #5
452	PERI_MS_PPU_FX_PASS0_SAR1_CH6_CH	0x40901980	0x00000040	SAR1, Channel #6
453	PERI_MS_PPU_FX_PASS0_SAR1_CH7_CH	0x409019C0	0x00000040	SAR1, Channel #7
454	PERI_MS_PPU_FX_PASS0_SAR1_CH8_CH	0x40901A00	0x00000040	SAR1, Channel #8

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
455	PERI_MS_PPU_FX_PASS0_SAR1_CH9_CH	0x40901A40	0x00000040	SAR1, Channel #9
456	PERI_MS_PPU_FX_PASS0_SAR1_CH10_CH	0x40901A80	0x00000040	SAR1, Channel #10
457	PERI_MS_PPU_FX_PASS0_SAR1_CH11_CH	0x40901AC0	0x00000040	SAR1, Channel #11
458	PERI_MS_PPU_FX_PASS0_SAR1_CH12_CH	0x40901B00	0x00000040	SAR1, Channel #12
459	PERI_MS_PPU_FX_PASS0_SAR1_CH13_CH	0x40901B40	0x00000040	SAR1, Channel #13
460	PERI_MS_PPU_FX_PASS0_SAR1_CH14_CH	0x40901B80	0x00000040	SAR1, Channel #14
461	PERI_MS_PPU_FX_PASS0_SAR1_CH15_CH	0x40901BC0	0x00000040	SAR1, Channel #15
462	PERI_MS_PPU_FX_PASS0_SAR1_CH16_CH	0x40901C00	0x00000040	SAR1, Channel #16
463	PERI_MS_PPU_FX_PASS0_SAR1_CH17_CH	0x40901C40	0x00000040	SAR1, Channel #17
464	PERI_MS_PPU_FX_PASS0_SAR1_CH18_CH	0x40901C80	0x00000040	SAR1, Channel #18
465	PERI_MS_PPU_FX_PASS0_SAR1_CH19_CH	0x40901CC0	0x00000040	SAR1, Channel #19
466	PERI_MS_PPU_FX_PASS0_SAR1_CH20_CH	0x40901D00	0x00000040	SAR1, Channel #20
467	PERI_MS_PPU_FX_PASS0_SAR1_CH21_CH	0x40901D40	0x00000040	SAR1, Channel #21
468	PERI_MS_PPU_FX_PASS0_SAR1_CH22_CH	0x40901D80	0x00000040	SAR1, Channel #22
469	PERI_MS_PPU_FX_PASS0_SAR1_CH23_CH	0x40901DC0	0x00000040	SAR1, Channel #23
470	PERI_MS_PPU_FX_PASS0_SAR1_CH24_CH	0x40901E00	0x00000040	SAR1, Channel #24
471	PERI_MS_PPU_FX_PASS0_SAR1_CH25_CH	0x40901E40	0x00000040	SAR1, Channel #25
472	PERI_MS_PPU_FX_PASS0_SAR1_CH26_CH	0x40901E80	0x00000040	SAR1, Channel #26
473	PERI_MS_PPU_FX_PASS0_SAR1_CH27_CH	0x40901EC0	0x00000040	SAR1, Channel #27

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表 25 （续） PPU 固定结构对

Pair no.	PPU fixed structure pair	Address	Size	Description
474	PERI_MS_PPU_FX_PASS0_SAR1_CH28_CH	0x40901F00	0x00000040	SAR1, Channel #28
475	PERI_MS_PPU_FX_PASS0_SAR1_CH29_CH	0x40901F40	0x00000040	SAR1, Channel #29
476	PERI_MS_PPU_FX_PASS0_SAR1_CH30_CH	0x40901F80	0x00000040	SAR1, Channel #30
477	PERI_MS_PPU_FX_PASS0_SAR1_CH31_CH	0x40901FC0	0x00000040	SAR1, Channel #31
478	PERI_MS_PPU_FX_PASS0_SAR2_CH0_CH	0x40902800	0x00000040	SAR2, Channel #0
479	PERI_MS_PPU_FX_PASS0_SAR2_CH1_CH	0x40902840	0x00000040	SAR2, Channel #1
480	PERI_MS_PPU_FX_PASS0_SAR2_CH2_CH	0x40902880	0x00000040	SAR2, Channel #2
481	PERI_MS_PPU_FX_PASS0_SAR2_CH3_CH	0x409028C0	0x00000040	SAR2, Channel #3
482	PERI_MS_PPU_FX_PASS0_SAR2_CH4_CH	0x40902900	0x00000040	SAR2, Channel #4
483	PERI_MS_PPU_FX_PASS0_SAR2_CH5_CH	0x40902940	0x00000040	SAR2, Channel #5
484	PERI_MS_PPU_FX_PASS0_SAR2_CH6_CH	0x40902980	0x00000040	SAR2, Channel #6
485	PERI_MS_PPU_FX_PASS0_SAR2_CH7_CH	0x409029C0	0x00000040	SAR2, Channel #7
486	PERI_MS_PPU_FX_PASS0_TOP	0x409F0000	0x00001000	PASS0, top

1) PPU 配置固定在启用内部，用户不得更改此 PPU 的属性。

24 总线主控器

仲裁器（闪存控制器的一部分）根据主控标识符执行基于优先级的仲裁。每个总线主控都有一个专用的 4 位主控标识符。该主控标识符用于总线仲裁和 IPC 功能。

表 26 用于访问和保护控制的总线主控器

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for Cortex®-M0+ CPU
1	CPUSS_MS_ID_CRYPTO	Master ID for Crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA 0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA 1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA0
14	CPUSS_MS_ID_CM4	Master ID for Cortex®-M4F CPU
15	CPUSS_MS_ID_TC	Master ID for DAP Tap controller

25 杂项配置

表 27 CYT2BL 器件的杂项配置

Sl. no.	Configuration	Number/ instances	Description
0	SRSS_NUM_CLKPATH	4	Number of clock paths. One for each of FLL, PLL, Direct and CSV
1	SRSS_NUM_HFROOT	3	Number of CLK_HFs roots present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_CLOCK_NR	124	Number of programmable clocks (outputs)
4	PERI_DIV_8_NR	32	Number of divide-by-8 clock dividers
5	PERI_DIV_16_NR	16	Number of divide-by-16 clock dividers
6	PERI_DIV_24_5_NR	8	Number of divide-by-24.5 clock dividers
7	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
8	CPUSS_CM4_MPU_NR	8	Number of MPU regions in CM4
9	CPUSS_CRYPTO_BUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
10	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
11	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM4 access 2 - Reserved for DAP access Remaining for user purposes
12	SCBx_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. ***Note***: *Only SCB0 supports CMD_RESP mode*
13	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of SMPU protection structures
14	TCPWM_TR_ONE_CNT_NR	3	Number of input triggers per counter, routed to one counter
15	TCPWM_TR_ALL_CNT_NR	27	Number of input triggers routed to all counters, based on the pin package
16	TCPWM_GRP_NR	3	Number of TCPWM0 counter groups
17	TCPWM_GRP_NR0_GRP_GRP_CNT_NR	63	Number of counters per TCPWM0 Group #0
18	TCPWM_GRP_NR0_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #0
19	TCPWM_GRP_NR1_GRP_GRP_CNT_NR	12	Number of counters per TCPWM0 Group #1

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表 27 （续）CYT2BL 器件的杂项配置

Sl. no.	Configuration	Number/ instances	Description
20	TCPWM_GRP_NR1_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #1
21	TCPWM_GRP_NR2_GRP_GRP_CNT_NR	8	Number of counters per TCPWM0 Group #2
22	TCPWM_GRP_NR2_CNT_GRP_CNT_WIDTH	32	Counter width in number of bits per TCPWM0 Group #2
23	CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE	32	Message RAM size in KB shared by all the channels
24	EVTGEN_COMP_STRUCT_NR	11	Number of event generator comparator structures

26 开发支持

CYT2BL 拥有丰富的文档、编程工具和在线资源，协助开发过程。请访问 www.infineon.cn 了解更多信息。

26.1 文档

一系列文档支持 CYT2BL，确保您能够快速找到问题的答案。本节列出了一些关键文档。

26.1.1 软件用户指南

使用示例驱动程序库以及第三方 IDE（例如 IAR EWARM 和 GHS Multi）的分步指南。

26.1.2 技术参考手册

技术参考手册（TRM）包含使用 CYT2BL 器件所需的所有技术细节，包括所有寄存器的完整描述。TRM 可在 www.infineon.cn 的文档部分找到。

26.2 工具

CYT2BL 受第三方开发工具生态系统（如 IAR 和 GHS）支持。英飞凌的编程工具也支持 CYT2BL，可使用英飞凌的 MiniProg4 或 Segger J-link 进行编程、擦除或读取。更多详细信息请参阅 www.infineon.cn 中的文档部分。

27 电气规格

27.1 绝对最大额定值

在 表 28 所列最小和最大限制之外的条件下使用本设备，可能会对设备造成永久性损坏。长时间 暴露在 表 28 限制范围内但超出正常操作限制的条件下，可能会影响器件的可靠性。最高存储温度为 150°C，符合 JEDEC 标准 JESD22-A103 "高温存储寿命"。如果在表 28 的限制条件下运行，但超出正常运行的限制条件，器件可能无法按规格运行。

功率考虑因素

平均芯片结温 T_J 以 °C 为单位，可采用以下公式计算：

$T_J = T_A + (P_D \times \theta_{JA})$

其中：

T_A 是环境温度，单位为 °C。

θ_{JA} 是封装结点至环境的热阻，单位为 °C/W。

P_D 是 P_{INT} 与 P_{IO} 之和（$P_D = P_{INT} + P_{IO}$）。
P_{INT}为芯片内部电源。（$P_{INT} = V_{DDD} \times I_{DD} + V_{DDA} \times I_A$）

P_{IO} 表示输入和输出引脚上的功耗；由用户确定。

对于大多数应用，$P_{IO} < P_{INT}$ 可以被忽略。
另一方面，如果器件配置为连续驱动外部模块和/或存储器，则 P_{IO} 可能很重要。

表 28 绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID10	V_{DDD_ABS}	V_{DDD} power supply voltage[1]	V_{SSD} – 0.3	–	V_{SSD} + 6.0	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23
SID10B	$V_{DDIO\_1\_ABS}$	V_{DDIO_1} power supply voltage[1]	V_{SSD} – 0.3	–	V_{SSD} + 6.0	V	For ports 6, 7, 8, 9[2]
SID10C1	$V_{DDIO\_2\_ABS}$	V_{DDIO_2} power supply voltage[1]	V_{SSD} – 0.3	–	V_{SSD} + 6.0	V	For ports 10, 11, 12, 13, 14, 15
SID11	V_{DDA_ABS}	V_{DDA} analog power supply voltage[1]	V_{SSA} – 0.3	–	V_{SSA} + 6.0	V	$V_{DDIO\_2} = V_{DDA}$
SID12	V_{REFH_ABS}	Analog reference voltage, HIGH[1]	V_{SSA} – 0.3	–	V_{SSA} + 6.0	V	$V_{REFH} \le V_{DDA}$ + 0.3 V
SID12A	V_{REFL_ABS}	Analog reference voltage, LOW[1]	V_{SSA} – 0.3	–	V_{SSA} + 0.3	V	
SID15A	V_{I0_ABS0}	Input voltage[1]	V_{SSD} – 0.5	–	V_{DDD} + 0.5	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23
SID15B	V_{I1_ABS1}	Input voltage[1]	V_{SSD} – 0.5	–	V_{DDIO_1} + 0.5	V	For ports 6, 7, 8, 9[2]

（表格续下页.....）

表 28 （续）绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID15C	V_{I2_ABS2}	Input voltage[1]	V_{SSD} – 0.5	–	V_{DDIO_2} + 0.5	V	For ports 10, 11, 12, 13, 14, 15
SID16	V_{IA_ABS}	Analog input voltage[1]	V_{SSA} – 0.3	–	V_{DDA} + 0.3	V	
SID17A	V_{O0_ABS0}	Output voltage[1]	V_{SSD} – 0.3	–	V_{DDD} + 0.3	V	For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23
SID17B	V_{O1_ABS1}	Output voltage[1]	V_{SSD} – 0.3	–	V_{DDIO_1} + 0.3	V	For ports 6, 7, 8, 9[2]
SID17C	V_{O2_ABS2}	Output voltage[1]	V_{SSD} – 0.3	–	V_{DDIO_2} + 0.3	V	For ports 10, 11, 12, 13, 14, 15
SID18	I_{CLAMP_ABS}	Maximum clamp current[3], [4], [5]	–5	–	5	mA	
SID18A	$I_{CLAMP\_SUPPLY\_POS\_ABS}$	Maximum positive clamp current per I/O supply pin. Limit applies to I/O supply pin closest to the B+ injected current[6]	–	–	10	mA	+B injected DC currents are not allowed for Ports 11 and 21 .
SID18B	$I_{CLAMP\_SUPPLY\_NEG\_ABS}$	Maximum negative clamp current per I/O ground pin. Limit applies to I/O supply pin closest to the B+ injected current[6]	–	–	10	mA	+B injected DC currents are not allowed for Ports 11 and 21 .
SID18C	$I_{CLAMP\_TOTAL\_POS\_ABS}$	Maximum positive clamp current per I/O supply, if not limited by the per supply pin (based on SID18A).	–	–	50	mA	
SID18D	$I_{CLAMP\_TOTAL\_NEG\_ABS}$	Maximum negative clamp current per I/O ground, if not limited by the per supply pin (based on SID18B).	–	–	50	mA	
SID20A	I_{OL1A_ABS}	LOW-level maximum output current[7]	–	–	6	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b0X
SID20B	I_{OL1B_ABS}	LOW-level maximum output current[7]	–	–	2	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b10

（表格续下页……）

表 28 （续）绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID20C	I_{OL1C_ABS}	LOW-level maximum output current[7]	–	–	1	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b11
SID21A	I_{OL2A_ABS}	LOW-level maximum output current[7]	–	–	6	mA	For GPIO_ENH, configured for drive_sel<1:0>= 0b0X
SID21B	I_{OL2B_ABS}	LOW-level maximum output current[7]	–	–	2	mA	For GPIO_ENH, configured for drive_sel<1:0>= 0b10
SID21C	I_{OL2C_ABS}	LOW-level maximum output current[7]	–	–	1	mA	For GPIO_ENH, configured for drive_sel<1:0>= 0b11
SID26A	$\sum I_{OL\_ABS\_GPIO}$	LOW-level total output current[8]	–	–	50	mA	
SID27A	I_{OH1A_ABS}	HIGH-level maximum output current[7]	–	–	–5	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b0X
SID27B	I_{OH1B_ABS}	HIGH-level maximum output current[7]	–	–	–2	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b10
SID27C	I_{OH1C_ABS}	HIGH-level maximum output current[7]	–	–	–1	mA	For GPIO_STD, configured for drive_sel<1:0>= 0b11
SID28A	I_{OH2A_ABS}	HIGH-level maximum output current[7]	–	–	–5	mA	For GPIO_ENH, configured for drive_sel<1:0>= 0b0X
SID28B	I_{OH2B_ABS}	HIGH-level maximum output current[7]	–	–	–2	mA	For GPIO_ENH, configured for drive_sel<1:0>= 0b10
SID28C	I_{OH2C_ABS}	HIGH-level maximum output current[7]	–	–	–1	mA	For GPIO_ENH, configured for drive_sel<1:0> = 0b11

（表格续下页……）

表 28 （续）绝对最大额定值

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID33A	$\Sigma I_{OH\_ABS\_GPIO}$	HIGH-level total output current[8]	–	–	–50	mA	
SID34	P_D	Power dissipation	–	–	1000	mW	T_J should not exceed 150 °C
SID35	T_A	Ambient temperature	–40	–	105	°C	For S-grade devices
SID36	T_A	Ambient temperature	–40	–	125	°C	For E-grade devices
SID37	T_{stg}	Storage temperature	–55	–	150	°C	
SID38	T_J	Operating junction temperature	–40	–	150	°C	
SID39A	V_{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	
SID39B1	V_{ESD_CDM1}	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B2	V_{ESD_CDM2}	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	I_{LU}	The maximum pin current the device can tolerate before triggering a latch-up	– 100	–	100	mA	

1) 这些参数基于 $V_{SSD} = V_{SSA} = 0.0$ V 的条件。
2) VDDIO_1 域中的 I/O 是指 64-LQFP 封装中的 V_{DDD} 域。
3) 必须配备限流电阻，使得 I/O 引脚的电流在任何时候都不超过额定值，包括功率瞬变期间。请参阅图 15了解有关推荐电路的更多信息。
4) V_{DDD} 和 V_{DDIO} 必须有足够的负载或受到保护，以防止它们被钳位电流拉出建议的工作范围。
5) 当满足 3), 4) 和 SID18A/B/C/D 条件时，$|I_{CLAMP\_ABS}|$ 取代 V_{IA_ABS} 和 V_{I_ABS}。
6) “更近” 的定义取决于封装。在 LQFP 封装中，“最接近”是通过计算引脚数来确定的。例如，在 176-LQFP 封装中，P17.4（引脚 120）距离引脚 110 上的 VDDD 比距离引脚 132 上的 VDDD 更近。端口 11 和 21 不应用于注入电流。注入电流的影响仅针对 GPIO_STD/GPIO_ENH 类型 I/O 进行定义。
7) 最大输出电流是流过任何一个 GPIO 的峰值电流。
8) 总输出电流是流过所有 I/O (GPIO_STD 和 GPIO_ENH) 的最大电流。

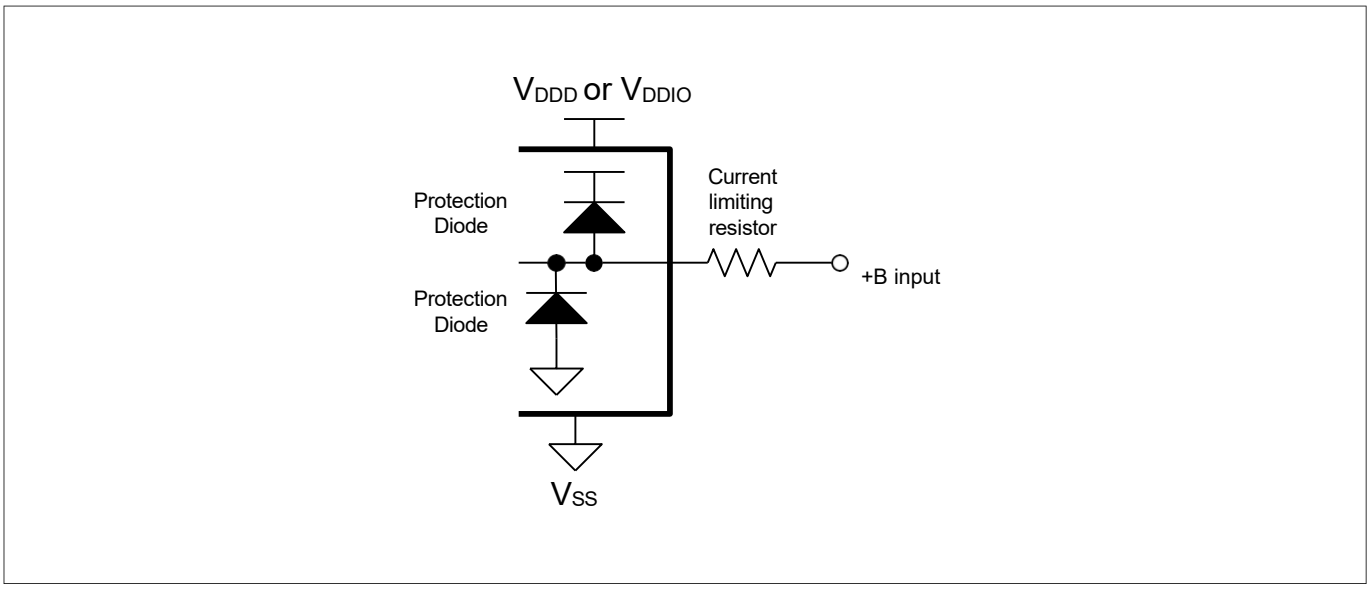


图 15　　推荐电路示例

注释: *+B 是电池正极电压，约为 45 V。*

警告: 半导体器件可能因施加超过绝对最大额定值的压力（包括但不限于电压、电流或温度）而导致永久损坏。不要超过任何这些额定值。

27.2　推荐工作条件

表 29　　器件级规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended operating conditions							
SID40	V_{DDD}, V_{DDA}, V_{DDIO_1}, V_{DDIO_2},	Power supply voltage[1)]	2.7[2)]	–	5.5[3)]	V	
SID40A	$V_{DDIO\_1\_EFP}$	Power supply voltage for eFuse programming[4)]	3	–	5.5	V	
SID41	C_{S1}	Smoothing capacitor[5), 6)]	3.76	–	11	µF	

1) V_{DDD}、V_{DDIO_1}、V_{DDIO_2} 和 V_{DDA} 没有任何顺序限制，可以按任意顺序建立。这些电源（V_{DDA} 和 V_{DDIO_2} 除外）的电压电平相互独立。使用 ADC 单元时，请参阅 12 位 SAR ADC DC 规格。

2) 支持 3.0 V ±10% 的电压范围，V_{DDD} 和 V_{DDA} 提供较低的 BOD 设置选项。此设置可为内部时序提供强大的保护，但当电压低于规定的工作条件时，BOD 复位会发生。此外，还提供更高的 BOD 设置选项（与低至 3.0 V 的电压一致），以确保满足所有工作条件。

3) 5.0 V ±10% 的过电压保护可通过更高的OVD V_{DDD} 和 V_{DDA} 保护设置选项实现。此设置可为内部和接口时序提供强大的保护，但 OVD 复位发生在电压高于指定运行条件时。较低的 OVD 设置选项可用（最高可达 5.0 V），并保证满足所有运行条件。允许电压过充至 VDDD 和 VDDA 的更高 OVD 设置范围，前提是累计持续时间小于 2 小时。请注意，在过冲电压条件下，电气参数无法得到保证。

4) eFuse 编程必须在部件处于“安静”状态时进行，尽量减少活动（最好只有 JTAG 或单个 LIN/CAN 通道在 VDDD 域，V_{DDIO_1} 上无活动）。

5) 每个芯片都需要一个平滑电容 C_{S1}（而不是每个 V_{CCD} 引脚）。V_{CCD} 引脚必须连接在一起，以确保低阻抗连接（参见图 16）。

6) 用于电源去耦或滤波的电容器在连续直流偏置下运行。许多使用直流电源的电容器提供的电容小于其目标电容，并且其电容在其工作电压范围内不是恒定的。选择用于此设备的电容器时，请确保所选组件在设计中使用的特定温度和电压工作条件下提供所需的电容。虽然温度系数通常可以在零件目录中找到（例如 X7R、C0G、Y5V），但匹配的电压系数可能仅在组件数据表上提供或直接从制造商处获得。在实际运行条件下使用不能提供所需电容的组件可能会导致器件运行不符合数据表规格。

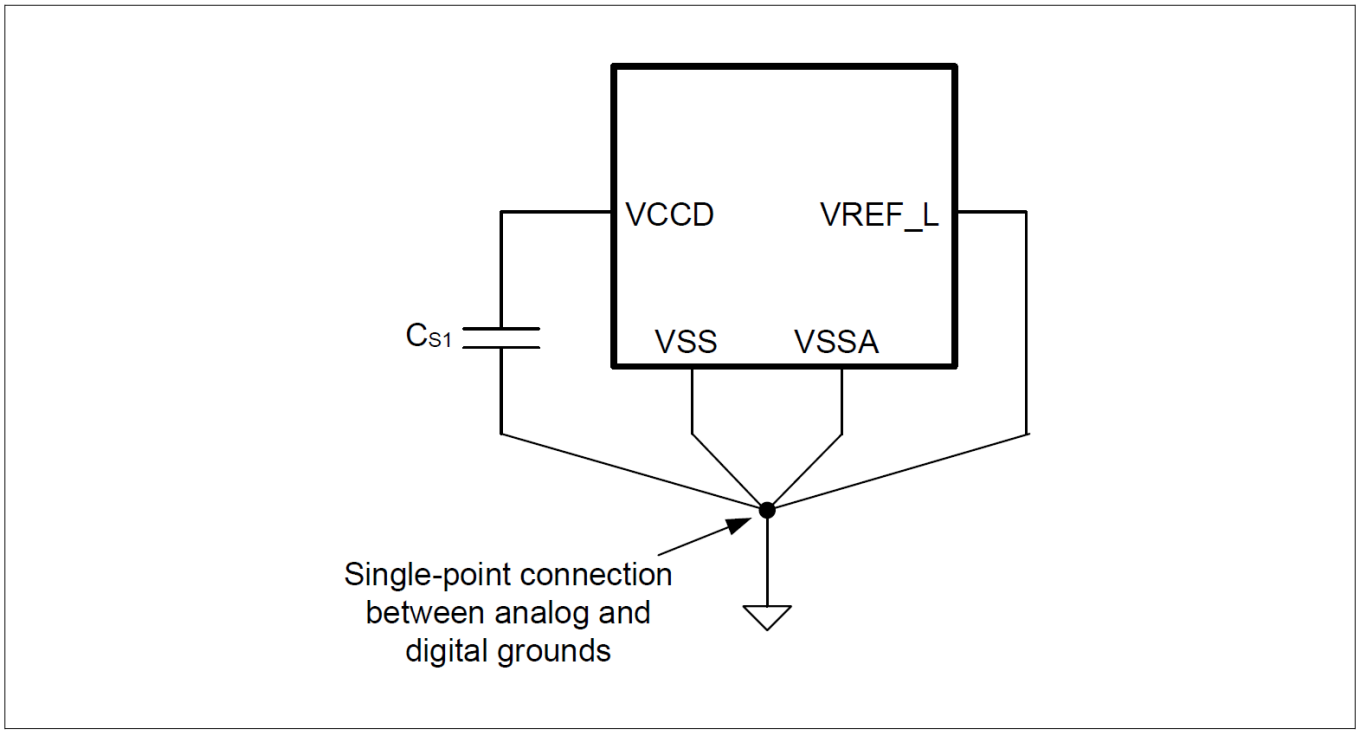


图 16 平滑电容器

平滑电容器应尽可能靠近 V_{CCD} 引脚放置。

27.3 DC 规格

表 30 DC 规格、CPU电流和转换时间规格

除非另有说明，所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID49C1	$I_{DD1\_CM04\_8\_1}$	LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are disabled)	–	5	10	mA	CM0+ and CM4 clocked at 8 MHz with IMO. All peripherals are disabled. No I/O toggling. TYP: T_A = 25 °C, V_{DDD} = 5.0 V, process typ (TT), CM0+ and CM4 executing Dhrystone from flash with cache enabled MAX: T_A = 25 °C, V_{DDD} = 5.5 V, process worst (FF), CM0+ and CM4 executing Dhrystone from flash with cache enabled.

（表格续下页……）

表 30　　（续）DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID49C4	$I_{DD1\_CM04\_8\_4M}$	LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are enabled)	–	6	73	mA	CM0+ and CM4 clocked at 8 MHz with IMO. All peripherals are enabled. No I/O toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. TYP: T_A = 25 °C, V_{DDD} = 5.0 V, process typ (TT), CM0+ and CM4 executing Dhrystone from flash with cache enabled MAX: T_A = 125 °C, V_{DDD} = 5.5 V, process worst (FF), CM0+ and CM4 executing max_power.c from flash with cache enabled.
SID49E4	$I_{DD1\_F160\_4M}$	Active mode (CM4 at 160 MHz, CM0+ at 80 MHz, all peripherals are enabled)	–	52	127	mA	PLL enabled at 160 MHz with ECO reference. All peripherals are enabled. No I/O toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. TYP: T_A = 25 °C, V_{DDD} = 5.0 V, process typ (TT), CM4 and CM0+ executing Dhrystone from flash with cache enabled. MAX: T_A = 125 °C, V_{DDD} = 5.5 V, process worst (FF), CM4 and CM0+ executing max_power.c from flash with cache enabled
SID53A4	$I_{DD2\_8\_4M}$	All CPUs in Sleep mode	–	4	68	mA	PLL disabled, CM4 and CM0+ are sleeping at 8 MHz with IMO. All peripherals, peripheral clocks, interrupts, CSV, DMA, FLL, ECO are disabled. No I/O toggling. Typ: T_A = 25 °C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 125 °C, V_{DDD} = 5.5 V, process worst (FF)

（表格续下页……）

表 30　　（续）DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID56A	I_{DD_CWU2}	Average current for cyclic wake-up operation This is the average current for the specified LP Active mode and DeepSleep mode (RTC, WDT and Event generator operating).	–	46	136	µA	V_{DDD} = 5.5 V, T_A = 25 °C, 64-KB SRAM retention, ILO0 operation in DeepSleep, Smart I/O operations with ILO0, CM0+, CM4: Retain Typ: process typ (TT) Max: process worst (FF) This average current is achieved under the following conditions. MCU repetitively goes from DeepSleep to LP Active with a period of 32 ms. One of the I/Os is toggled using Smart I/O to activate an external sensor connected to an analog input of A/D in DeepSleep. After 200 µs delay, the CM4 wakes up by event generator trigger to LP Active mode with IMO and A/D conversion is triggered by software. Group A/D conversion is performed on 5 channels with the sampling time of 1 µs each. Once the group A/D conversion is finished, and the results fit in the window of the range comparator, the I/O is toggled back by software to de-activate the sensor and the CM4 goes back to DeepSleep.
SID59A	I_{DD_DS64B}	64-KB SRAM retention, ILO0 operation in DeepSleep mode	–	35	130	µA	DeepSleep Mode (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), T_A = 25 °C, CM0+, CM4: Retained Typ: V_{DDD} = 5.0 V, process typ (TT) Max: V_{DDD} = 5.5 V, process worst (FF)

（表格续下页……）

表 30　　（续） DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID61A	I_{DD_DS64D}	64-KB SRAM retention, ILO0 operation in DeepSleep mode	–	0.9	3.5	mA	DeepSleep Mode steady state at T_A = 125 °C (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers),CM0+, CM4: Retained Typ: V_{DDD} = 5.0 V, process typ (TT) Max: V_{DDD} = 5.5 V, process worst (FF)
Hibernate mode							
SID62	I_{DD_HIB1}	Hibernate Mode	–	5	–	µA	ILO0/WDT operating. All other peripherals, and all CPUs are off. T_A = 25 °C, V_{DDD} = 5.5 V, process typ (TT)
SID62A	I_{DD_HIB2}	Hibernate Mode	–	–	130	µA	ILO0/WDT operating. All other peripherals, and all CPUs are off. T_A = 125 °C, V_{DDD} = 5.5 V, process worst (FF)
Power mode transition times							
SID65	t_{ACT_DS}	Power down time from Active to DeepSleep	–	–	2.5	µs	When the IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID63	t_{DS_ACT}	DeepSleep to Active transition time (IMO clock, SRAM execution)	–	–	10[1)]	µs	When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until wakeup.
SID63C	t_{DS_ACT}	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	20 [1)]	µs	When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.
SID63A	$t_{DS\_ACT\_FLL}$	DeepSleep to Active transition time (FLL clock, SRAM execution)	–	–	15[1)]	µs	When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the FLL locks.

（表格续下页……）

表 30　　（续） DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID63D	$t_{DS\_ACT\_FLL1}$	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	21.5[1)]	µs	When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.
SID63B	$t_{DS\_ACT\_PLL}$	DeepSleep to Active transition time (PLL clock, SRAM or flash execution)	–	–	60[1)]	µs	When using the PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the PLL locks.
SID68	t_{HVR_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) release until CM0+ begins executing ROM boot	–	–	265	µs	Without boot runtime. Guaranteed by design
SID68A	t_{LVR_ACT}	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/ Sleep until CM0+ begins executing ROM boot	–	–	10	µs	Without boot runtime. Guaranteed by design
SID68B	t_{LVR_DS}	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	µs	Without boot runtime. Guaranteed by design
SID80A	t_{RB_N}	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	1800	µs	Guaranteed by design CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later)
SID80B	t_{RB_S}	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	2740	µs	Guaranteed by design CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later)

（表格续下页……）

表 30　　（续）DC 规格、CPU 电流和转换时间规格

除非另有说明，所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID81A	t_{FB}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	80	µs	Guaranteed by Design, TOC2_FLAGS = 0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms (Flash boot version 3.1.0.556 and later)
SID81B	t_{FB_A}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	5000	µs	Guaranteed by Design, TOC2_FLAGS = 0x24F, CM0+ clocked at 100 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, APP size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5. Valid for RSA-2048. (Flash boot version 3.1.0.556 and later)
Regulator specifications							
SID600	V_{CCD}	Core supply voltage	1.05	1.1	1.15	V	
SID601	I_{DD_ACT}	Regulator operating current in Active/Sleep mode	–	80	150	µA	Guaranteed by Design
SID602	I_{DD_DPSLP}	Regulator operating current in DeepSleep mode	–	1.5	20	µA	Guaranteed by Design
SID604	I_{OUT}	Available regulator output current for operation	–	–	150	mA	Without triggering OVD
SID603	I_{RUSH}	In-rush current	–	–	375	mA	Average V_{DDD} current until C_{s1} (connected to V_{CCD} pin) is charged after Active regulator is turned on

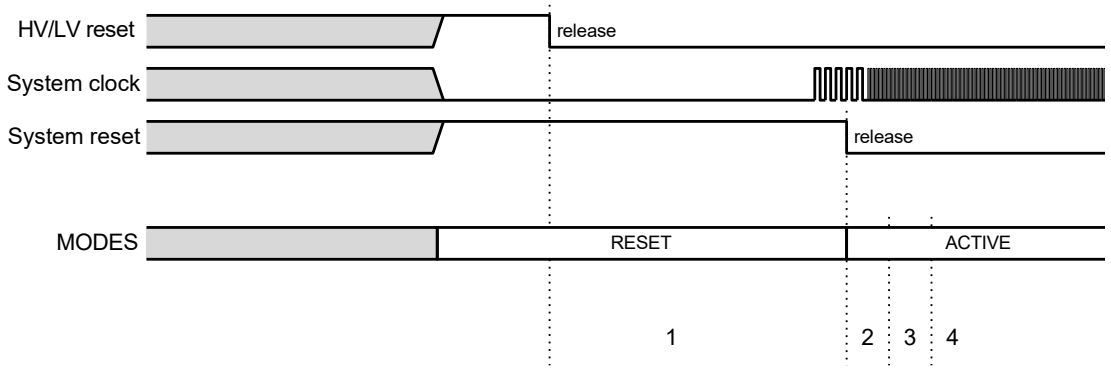
1)　在低温 - 5 °C 至 - 40 °C 下，深度睡眠到运行模式的转换时间可能比指示的最大时间高出 20 µs。

27.4　　复位规格

除非另有说明，所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 31 XRES_L 复位

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
XRES_L DC specifications							
SID73	I_{DD_XRES}	I_{DD} when XRES_L asserted	–	–	0.9	mA	TA = 125 °C, V_{DDD} = 5.5 V, process worst (FF)
SID74	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID75	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID76	RPULLUP	Pull-up resistor	7	–	20	KΩ	
SID77	C_{IN}	Input capacitance	–	–	5	pF	
SID78	VHYSXRES	Input voltage hysteresis	0.05 × V_{DDD}	–	–	V	
XRES_L AC specifications							
SID70	t_{XRES_ACT}	XRES_L release to Active transition time	–	–	265	µs	Without boot runtime. Guaranteed by design
SID71	t_{XRES_PW}	XRES_L pulse width	5	–	–	µs	
SID72	t_{XRES_FT}	Pulse suppression width	100	–	–	ns	



1 : **SID68/68A/68B**: Time from HV/LV reset release until CM0+ begins executing ROM boot
SID80A/80B: ROM boot code operation
2 : **SID81A/81B**: Flash boot code operation
User code operation

图 17 复位序列

27.5 I/O

除非另有说明， 所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 32 I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
GPIO_STD specifications for ports P1 through P23							
SID650	$V_{OL1\_GPIO\_STD}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID650C	$V_{OL1C\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID651	$V_{OL2\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID652	$V_{OL3\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID652C	$V_{OL3C\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID653	$V_{OL4\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID653C	$V_{OL4C\_GPIO\_STD}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID654	$V_{OH1\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID655	$V_{OH2\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID656	$V_{OH3\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID656C	$V_{OH3C\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID657	$V_{OH4\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID657C	$V_{OH4C\_GPIO\_STD}$	Output voltage HIGH level	(V_{DDD} or V_{DDIO_1} or V_{DDIO_2}) – 0.5	–	–	V	I_{OH} = –1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID658	$R_{PD\_GPIO\_STD}$	Pull-down resistance	25	50	100	kΩ	
SID659	$R_{PU\_GPIO\_STD}$	Pull-up resistance	25	50	100	kΩ	
SID660	$V_{IH\_CMOS\_GPIO\_STD}$	Input voltage HIGH threshold in CMOS mode	0.7 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	–	–	V	
SID661	$V_{IH\_TTL\_GPIO\_STD}$	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	
SID662	$V_{IH\_AUTO\_GPIO\_STD}$	Input voltage HIGH threshold in AUTO mode	0.8 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	–	–	V	
SID663	$V_{IL\_CMOS\_GPIO\_STD}$	Input voltage LOW threshold in CMOS mode	–	–	0.3 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	V	
SID664	$V_{IL\_TTL\_GPIO\_STD}$	Input voltage LOW threshold in TTL mode	–	–	0.8	V	
SID665	$V_{IL\_AUTO\_GPIO\_STD}$	Input voltage LOW threshold in AUTO mode	–	–	0.5 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	V	

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID666	$V_{HYST\_CMOS\_GPIO\_STD}$	Hysteresis in CMOS mode	0.05 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	–	–	V	
SID668	$V_{HYST\_AUTO\_GPIO\_STD}$	Hysteresis in AUTO mode	0.05 × (V_{DDD} or V_{DDIO_1} or V_{DDIO_2})	–	–	V	
SID669	$C_{in\_GPIO\_STD}$	Input pin capacitance	–	–	5	pF	For 10 MHz and 100 MHz
SID670	$I_{IL\_GPIO\_STD}$	Input leakage current	–250	0.02	250	nA	For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P23.3, P23.4. $V_{DDIO\_1} = V_{DDIO\_2} = V_{DDD} = V_{DDA} = 5.5$ V, $V_{SSD} < V_I < V_{DDD}$, V_{DDIO_1}, V_{DDIO_2} –40 °C ≤ TA ≤ 125 °C TYP: T_A = 25 °C, $V_{DDIO\_1} = V_{DDIO\_2} = V_{DDD} = V_{DDA} = 5.0$ V
SID670C	$I_{IL\_GPIO\_STD\_B}$	Input leakage current	–700	0.02	700	nA	Only for P21.0, P21.1, P21.2, P21.3, P21.4, P23.3, P23.4. $V_{DDIO\_1} = V_{DDIO\_2} = V_{DDD} = V_{DDA} = 5.5$ V, $V_{SSD} < V_I < V_{DDD}$, V_{DDIO_1}, V_{DDIO_2} –40 °C ≤ TA ≤ 125 °C TYP: T_A = 25 °C, $V_{DDIO\_1} = V_{DDIO\_2} = V_{DDD} = V_{DDA} = 5.0$ V
SID671	t_R or t_F (fast)$_{20\_0\_GPIO\_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	10	ns	20-pF load, drive_sel<1:0> = 0b00
SID672	t_R or t_F (fast)$_{50\_0\_GPIO\_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	50-pF load, drive_sel<1:0> = 0b00
SID673	t_R or t_F (fast)$_{20\_1\_GPIO\_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	20-pF load, drive_sel<1:0> = 0b01, guaranteed by design

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID674	t_R or t_F (fast)$_{\_10\_2\_GPIO\_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	10-pF load, drive_sel<1:0> = 0b10, guaranteed by design
SID675	t_R or t_F (fast)$_{\_6\_3\_GPIO\_STD}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	6-pF load, drive_sel<1:0> = 0b11, guaranteed by design
SID676	t_F (fast)$_{\_100\_GPIO\_STD}$	Fall time (30% to 70% of V_{DDIO})	0.35	–	250	ns	10-pF to 400-pF load, RPU = 767 Ω, drive_sel<1:0>= 0b00, Freq = 100 kHz
SID677	t_F (fast)$_{\_400\_GPIO\_STD}$	Fall time (30% to 70% of V_{DDIO})	0.35	–	250	ns	10-pF to 400-pF load, RPU = 350 Ω, drive_sel<1:0>= 0b00, Freq = 400 kHz
SID678	$f_{IN\_GPIO\_STD}$	Input frequency	–	–	100	MHz	
SID679	$f_{OUT\_GPIO\_STD0H}$	Output frequency	–	–	50	MHz	20-pF load, drive_sel<1:0>= 00, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID680	$f_{OUT\_GPIO\_STD0L}$	Output frequency	–	–	32	MHz	20-pF load, drive_sel<1:0>= 00, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID681	$f_{OUT\_GPIO\_STD1H}$	Output frequency	–	–	25	MHz	20-pF load, drive_sel<1:0>= 01, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID682	$f_{OUT\_GPIO\_STD1L}$	Output frequency	–	–	15	MHz	20-pF load, drive_sel<1:0>= 01, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
SID683	$f_{OUT\_GPIO\_STD2H}$	Output frequency	–	–	25	MHz	10-pF load, drive_sel<1:0>= 10, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID684	$f_{OUT\_GPIO\_STD2L}$	Output frequency	–	–	15	MHz	10-pF load, drive_sel<1:0>= 10, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID685	$f_{OUT\_GPIO\_STD3H}$	Output frequency	–	–	15	MHz	6-pF load, drive_sel<1:0>= 11, 4.5 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} ≤ 5.5 V
SID686	$f_{OUT\_GPIO\_STD3L}$	Output frequency	–	–	10	MHz	6-pF load, drive_sel<1:0>= 11, 2.7 V ≤ V_{DDD} or V_{DDIO_1} or V_{DDIO_2} < 4.5 V
GPIO_ENH specifications only for P0							
SID650A	$V_{OL1\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA drive_sel<1:0> = 0b00/01, 2.7 V ≤ V_{DDD} ≤ 5.5 V
SID650D	$V_{OL1D\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA drive_sel<1:0> = 0b00/01, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID651A	$V_{OL2\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA drive_sel<1:0> = 0b00/01, 2.7 V ≤ V_{DDD} < 4.5 V
SID652A	$V_{OL3\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V_{DDD} < 4.5 V
SID652D	$V_{OL3D\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID653A	$V_{OL4\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V_{DDD} < 4.5 V
SID653D	$V_{OL4D\_GPIO\_ENH}$	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID654A	$V_{OH1\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –2 mA drive_sel<1:0> = 0b00/01, 2.7 V ≤ V_{DDD} < 4.5 V

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID655A	$V_{OH2\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –5 mA drive_sel<1:0> = 0b00/01, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID656A	$V_{OH3\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V_{DDD} < 4.5 V
SID656D	$V_{OH3D\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID657A	$V_{OH4\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V_{DDD} < 4.5 V
SID657D	$V_{OH4D\_GPIO\_ENH}$	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OL} = –1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID658A	$R_{PD\_GPIO\_ENH}$	Pull-down resistance	25	50	100	kΩ	
SID659A	$R_{PU\_GPIO\_ENH}$	Pull-up resistance	25	50	100	kΩ	
SID660A	$V_{IH\_CMOS\_GPIO\_ENH}$	Input voltage HIGH threshold in CMOS mode	0.70 × V_{DDD}	–	–	V	
SID661A	$V_{IH\_TTL\_GPIO\_ENH}$	Input voltage HIGH threshold in TTL mode	2	–	–	V	
SID662A	$V_{IH\_AUTO\_GPIO\_ENH}$	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDD}	–	–	V	
SID663A	$V_{IL\_CMOS\_GPIO\_ENH}$	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDD}	V	
SID664A	$V_{IL\_TTL\_GPIO\_ENH}$	Input voltage LOW threshold in TTL mode	–	–	0.8	V	
SID665A	$V_{IL\_AUTO\_GPIO\_ENH}$	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDD}	V	
SID666A	$V_{HYST\_CMOS\_GPIO\_ENH}$	Hysteresis in CMOS mode	0.05 × V_{DDD}	–	–	V	

（表格续下页……）

表 32 （续）I/O 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID668A	$V_{HYST\_AUTO\_GPIO\_ENH}$	Hysteresis in AUTO mode	0.05 × V_{DDD}	–	–	V	
SID669A	$C_{in\_GPIO\_ENH}$	Input pin capacitance	–	–	5	pF	For 10 MHz and 100 MHz
SID670A	$I_{IL\_GPIO\_ENH}$	Input leakage current	–350	0.055	350	nA	$V_{DDD} = V_{DDA} = 5.5$ V, $V_{SSD} < V_I < V_{DDD}$, –40 °C ≤ T_A ≤ 125 °C TYP: T_A = 25 °C, $V_{DDD} = V_{DDA} = 5.0$ V
SID671A	t_R or t_F (fast)$_{\_20\_0\_GPIO\_ENH}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	10	ns	20-pF load, drive_sel<1:0> = 0b00, slow = 0
SID672A	t_R or t_F (fast)$_{\_50\_0\_GPIO\_ENH}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	50-pF load, drive_sel<1:0> = 0b00, slow = 0
SID673A	t_R or t_F (fast)$_{\_20\_1\_GPIO\_ENH}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	20-pF load, drive_sel<1:0> = 0b01, slow = 0, guaranteed by design
SID674A	t_R or t_F (fast)$_{\_10\_2\_GPIO\_ENH}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	10-pF load, drive_sel<1:0> = 0b10, slow = 0, guaranteed by design
SID675A	t_R or t_F (fast)$_{\_6\_3\_GPIO\_EnH}$	Rise time or fall time (10% to 90% of V_{DDIO})	1	–	20	ns	6-pF load, drive_sel<1:0> = 0b11, slow = 0, guaranteed by design
SID676A	t_{F_I2C} (slow)$_{\_GPIO\_ENH}$	Fall time (30% to 70% of V_{DDIO})	20 × (V_{DDD} / 5.5)	–	250	ns	10-pF to 400-pF load, drive_sel<1:0> = 0b00, slow = 1, minimum R_{PU} = 400 Ω
SID677A	t_R or t_F (slow)$_{\_20\_GPIO\_EnH}$	Rise time or fall time (10% to 90% of V_{DDIO})	20 × (V_{DDD} / 5.5)	–	160	ns	20-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 1 MHz

（表格续下页……）

表 32 （续）I/O 规格

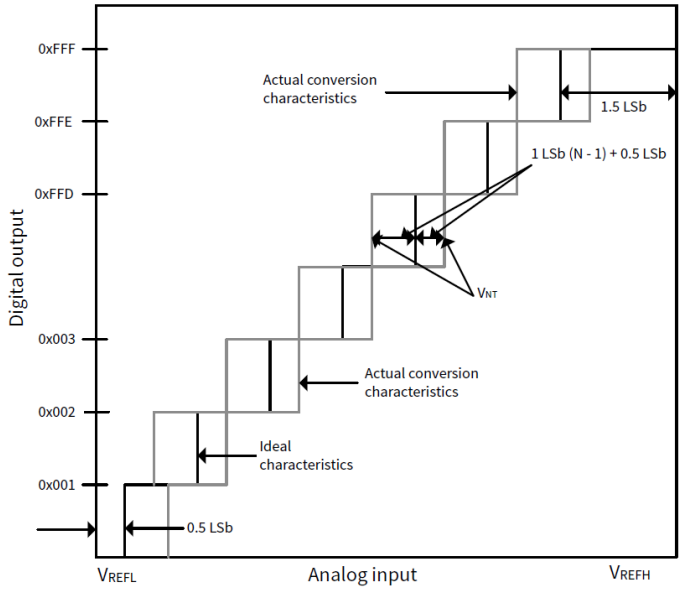
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID678A	t_R or t_F (slow)_400_GPIO_ENH	Rise time or fall time (10% to 90% of V_{DDIO})	20 × (V_{DDD} / 5.5)	–	250	ns	400-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 400 kHz
SID679A	$f_{IN\_GPIO\_ENH}$	Input frequency	–	–	100	MHz	
SID680A	$f_{OUT\_GPIO\_ENH0H}$	Output frequency	–	–	50	MHz	20-pF load, drive_sel<1:0>= 0b00, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID681A	$f_{OUT\_GPIO\_ENH0L}$	Output frequency	–	–	32	MHz	20-pF load, drive_sel<1:0>= 0b00, 2.7 V ≤ V_{DDD} < 4.5 V
SID682A	$f_{OUT\_GPIO\_ENH1H}$	Output frequency	–	–	25	MHz	20-pF load, drive_sel<1:0>= 0b01, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID683A	$f_{OUT\_GPIO\_ENH1L}$	Output frequency	–	–	15	MHz	20-pF load, drive_sel<1:0>= 0b01, 2.7 V ≤ V_{DDD} < 4.5 V
SID684A	$f_{OUT\_GPIO\_ENH2H}$	Output frequency	–	–	25	MHz	10-pF load, drive_sel<1:0>= 0b10, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID685A	$f_{OUT\_GPIO\_ENH2L}$	Output frequency	–	–	15	MHz	10-pF load, drive_sel<1:0>= 0b10, 2.7 V ≤ V_{DDD} < 4.5 V
SID686A	$f_{OUT\_GPIO\_ENH3H}$	Output frequency	–	–	15	MHz	6-pF load, drive_sel<1:0>= 0b11, 4.5 V ≤ V_{DDD} ≤ 5.5 V
SID687A	$f_{OUT\_GPIO\_ENH3L}$	Output frequency	–	–	10	MHz	6-pF load, drive_sel<1:0>= 0b11, 2.7 V ≤ V_{DDD} < 4.5 V
GPIO input specifications							
SID98	t_{FT}	Analog glitch filter (pulse suppression width)	–	–	50[1)]	ns	One filter per port group
SID99	t_{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

1) 如果需要更长的脉冲宽度抑制，请使用智能 I/O。

27.6 模拟外设

除非另有说明， 所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

27.6.1 SAR ADC



Total error of digital output N = (V_{NT} {1 LSb × (N – 1) + 0.5 LSb})/ 1 LSb [LSb]

1 LSb (Ideal value) = (V_{REFH} – V_{REFL}) / 4096 [V]

N: A/D converter digital output value
V_{ZT} (Ideal value): V_{REFL} + 0.5 LSb [V]
V_{FST} (Ideal value): V_{REFH} – 1.5 LSb [V]
V_{NT}: Voltage at which the digital output changes from N – 1 to N

图 18 ADC 特性和误差定义

表 33 12 位 SAR ADC DC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	–	–	12	bits	
SID101	A_V_{INS}	Input Voltage Range	V_{REFL}	–	V_{REFH}	V	
SID102	A_V_{REFH}	V_{REFH} voltage range	2.7	–	V_{DDA}	V	ADC performance degrades when high reference is higher than supply
SID102A	A_V_{DDA} *1)*	V_{DDA} voltage range	2.7	–	5.5	V	

（表格续下页.....）

表 33 （续）12 位 SAR ADC DC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID103	A_V_{REFL}	V_{REFL} voltage range	V_{SSA}	–	V_{SSA}	V	ADC performance degrades when low reference is lower than ground
SID103A	V_{band_gap}	Internal band gap reference voltage	0.882	0.9	0.918	V	
SID19A	CLAMP_COUPLING_RATIO_POS	Ratio of current collected on a pin to the positive current injected into a neighboring pin	–	–	0.25	%	
SID19B	CLAMP_COUPLING_RATIO_NEG	Ratio of current collected on a pin to the negative current injected into a neighboring pin	–	–	1.2	%	
SID19C	$R_{CLAMP\_INTERNAL}$	Internal pin resistance to current collection point	–	–	50	Ω	

1) 当 ADC[2] 启用时， VDDD 必须大于 $0.8 \times V_{DDA}$。当 ADC[0] 启用时， VDDIO_1 必须大于 $0.8 \times V_{DDA}$。

27.6.2 计算相邻引脚的影响

基于SID19A、SID19B和SID19C的三个ADC规格可用于计算引脚泄漏以及注入电流引起的ADC偏移，公式如下：

$I_{LEAK} = I_{INJECTED} \times CLAMP\_COUPLING\_RATIO$

$V_{ERROR} = I_{LEAK} \times (R_{CLAMP\_INTERNAL} + R_{SOURCE})$

$Code\ Error = V_{ERROR} \times 2^{12} / V_{REF}$

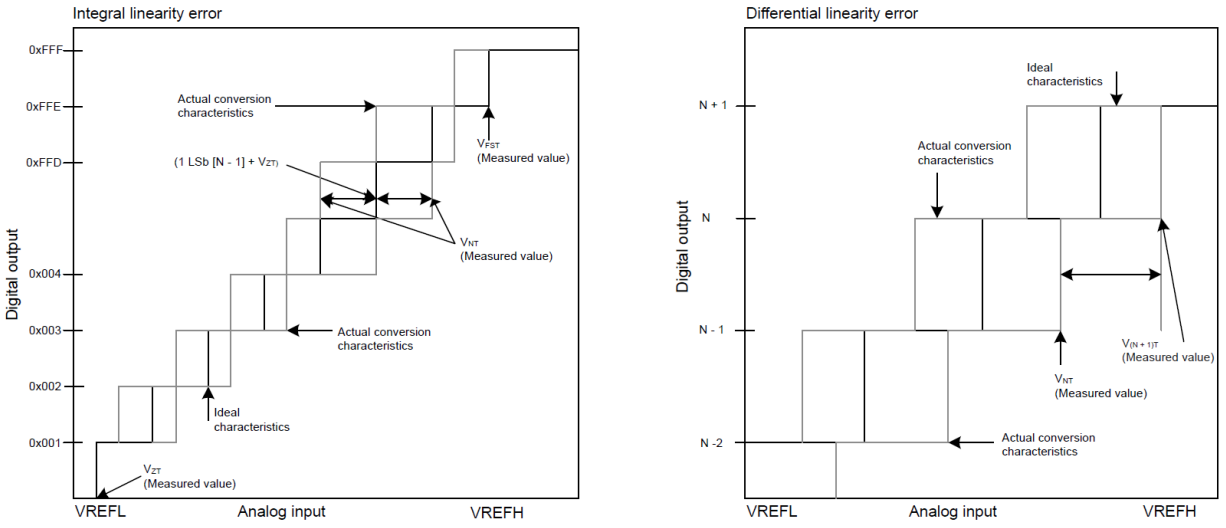
其中：

$I_{INJECTED}$ 是注入电流（以 mA 为单位）。

I_{LEAK} 是计算出的漏电流（以 mA 为单位）。

V_{ERROR} 是由于 V 中的漏电流而计算出的电压误差。

V_{REF} 是 ADC 参考电压，单位为 V。

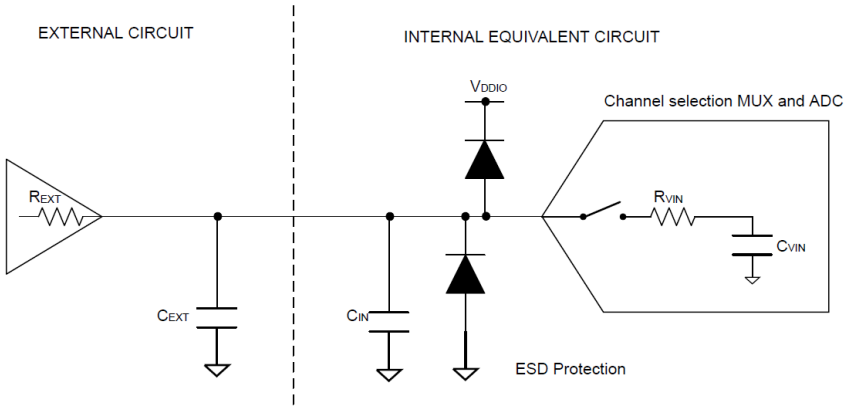


Integral linearity error of digital output N = (V_{NT} – {1 LSb × (N – 1) + V_{ZT}}) / 1 LSb [LSb]

Differential linearity error of digital output N = ($V_{(N+1)T}$ – V_{NT} – 1 LSb) / 1 LSb [LSb]

1 LSb = (V_{FST} – V_{ZT}) / 4094 [V]

图 19 积分和微分线性误差



REXT: Source impedance
CEXT: On-PCB capacitance
CIN: I/O pad or Input capacitance
RVIN: ADC equivalent input resistance
CVIN: ADC equivalent input capacitance
K: Constant for sampling accuracy, K = ln(abs(4096/LSbSAMPLE))

Sampling Time (tSAMPLE) requirement is shown in the following equation
tSAMPLE > K x { CVIN x (RVIN + REXT) + (CIN + CEXT) x (REXT) } [seconds]

K = value of 9.0 is recommended to get ±0.5 LSb sampling accuracy at 12-bit (LSbSAMPLE = ±0.5)

图 20 ADC模拟输入等效电路

表 34 SAR ADC AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V_{ZT}	Zero transition voltage	–20	–	20	mV	V_{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 125 °C before offset adjustment
SID105	V_{FST}	Full-scale transition voltage	–20	–	20	mV	V_{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 125 °C before offset adjustment
SID114	f_{ADC_4P5}	ADC operating frequency	2	–	26.67	MHz	4.5 V ≤ V_{DDA} ≤ 5.5 V
SID114A	f_{ADC_2P7}	ADC operating frequency	2	–	13.34	MHz	2.7 V ≤ V_{DDA} < 4.5 V
SID113	t_{S_4P5}	Analog input sample time for channels of own SARMUX	412	–	–	ns	4.5 V ≤ V_{DDA} ≤ 5.5 V guaranteed by design
SID113A	t_{S_2P7}	Analog input sample time for channels of own SARMUX	600	–	–	ns	2.7 V ≤ V_{DDA} < 4.5 V guaranteed by design
SID113B	$t_{S\_DR\_4P5}$	Analog input sample time when input is from diagnostic reference	2	–	–	µs	4.5 V ≤ V_{DDA} ≤ 5.5 V guaranteed by design
SID113C	$t_{S\_DR\_2P7}$	Analog input sample time when input is from diagnostic reference	2.5	–	–	µs	2.7 V ≤ V_{DDA} < 4.5 V Guaranteed by design
SID113D	t_{S_TS}	Analog input sample time for temperature sensor	3	–	–	µs	2.7 V ≤ V_{DDA} ≤ 5.5 V guaranteed by design
SID113E	$t_{S\_4P5\_A}$	Analog input sample time for channels of another SARMUXn (n=1,2)	824	–	–	ns	4.5 V ≤ V_{DDA} ≤ 5.5 V When ADC0 borrows the SARMUX of another ADC, guaranteed by design
SID113F	$t_{S\_2P7\_A}$	Analog input sample time for channels of another SARMUXn (n=1,2)	1648	–	–	ns	2.7V ≤ V_{DDA} ≤ 4.5 V When ADC0 borrows the SARMUX of another ADC, guaranteed by design
SID106	t_{ST_4P5}	ADC max throughput (samples per second) when using the SARMUX of own ADC	–	–	1	Msps	4.5 V ≤ V_{DDA} ≤ 5.5 V, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles

（表格续下页……）

表 34 （续） SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID106A	t_{ST_2P7}	ADC max throughput (samples per second) when using the SARMUX of own ADC	–	–	0.5	Msps	2.7 V ≤ V_{DDA} < 4.5 V 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID106B	$t_{ST\_4P5\_A}$	ADC0 max throughput (samples per second) when borrowing the SARMUXn of another ADC (n=1,2)	–	–	0.5	Msps	4.5 V ≤ V_{DDA} ≤ 5.5 V, 80 MHz/6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID106C	$t_{ST\_2P7\_A}$	ADC0 max throughput (samples per second) when borrowing the SARMUXn of another ADC (n=1,2)	–	–	0.25	Msps	2.7V ≤ VDDA < 4.5 V, 80 MHz / 12 = 6.67 MHz, 11 sampling cycles, 15 conversion cycles
SID107	C_{VIN}	ADC input sampling capacitance	–	–	4.8	pF	Guaranteed by design
SID108	R_{VIN1}	Input path ON resistance (4.5 V to 5.5 V)	–	–	9.4	kΩ	Guaranteed by design
SID108A	R_{VIN2}	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	R_{DREF1}	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	R_{DREF2}	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	
SID109	A_TE	Total error	–5	–	5	LSb	V_{DDA} = V_{REFH} = 2.7 V to 5.5 V, V_{REFL} = V_{SSA} –40 °C ≤ T_A ≤ 125 °C Total error after offset and gain adjustment at 12 bit resolution mode
SID109A	A_TEB	Total error	–12	–	12	LSb	V_{DDA} = V_{REFH} = 2.7 V to 5.5 V, V_{REFL} = V_{SSA} –40 °C ≤ T_A ≤ 125 °C Total error before offset and gain adjustment at 12 bit resolution mode
SID110	A_INL	Integral nonlinearity	–2.5	–	2.5	LSb	V_{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 125 °C

（表格续下页……）

表 34 （续） SAR ADC AC规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID111	A_DNL	Differential nonlinearity	–0.99	–	1.9	LSb	V_{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 125 °C
SID112	A_CE	Channel-to-channel variation (for channels connected to same ADC)	–1	–	1	LSb	V_{DDA} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 125 °C
SID115	I_{AIC}	Analog input leakage current	–350	70	350	nA	When input pad is selected for conversion
SID116	$I_{DIAGREF}$	Diagnostic reference current	–	–	70	µA	
SID117	I_{VDDA}	Analog power supply current while ADC is operating	–	360	550	µA	Per enabled ADC
SID117A	I_{VDDA_DS}	Analog power supply current while ADC is not operating	–	–	21	µA	Per enabled ADC
SID118	I_{VREF}	Analog reference voltage current while ADC is operating	–	360	550	µA	Per enabled ADC
SID118A	I_{VREF_LEAK}	Analog reference voltage current while ADC is not operating	–	1.8	5	µA	Per enabled ADC

27.6.3 温度传感器

表 35 温度传感器规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201	$T_{SENSACC2}$	Temperature sensor accuracy 2	–5	–	5	°C	–40 °C ≤ T_J ≤ 150 °C This spec is valid when using ADC[0] (V_{DDIO_1}), ADC[1] (V_{DDIO_2}) or ADC[2] (V_{DDD}) with the following conditions: a. 3.0 V ≤ V_{DDD}, V_{DDIO_1} or V_{DDIO_2} = V_{DDA} = V_{REFH} ≤ 3.6 V or b. 4.5 V ≤ V_{DDD}, V_{DDIO_1} or V_{DDIO_2} = V_{DDA} = V_{REFH} ≤ 5.5 V

（表格续下页……）

表 35 （续）温度传感器规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201A	$T_{SENSACC3}$	Temperature sensor accuracy 3	–10	–	10	°C	–40 °C ≤ T_J ≤ 150 °C This spec is valid when using ADC[0] (V_{DDIO_1}) or ADC[2] (V_{DDD}) with the following condition: 2.7 V ≤ V_{DDD} or V_{DDIO_1} ≤ 5.5 V and 2.7 V ≤ V_{DDA} = V_{REFH} ≤ 5.5 V and 0.8 × V_{DDA} < V_{DDD} or V_{DDIO_1}

27.6.4 分压器准确度

表 36 分压器准确度

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID202	V_{MONDIV}	Uncorrected monitor voltage divider accuracy (measured by ADC), compared to ideal supply/2	–20	2	20	%	Any HV supply pad within 2.7 V - 5.5 V operating range

27.7 AC 规格

除非另有说明，时序均按照图 21 中提到的指导原则定义。

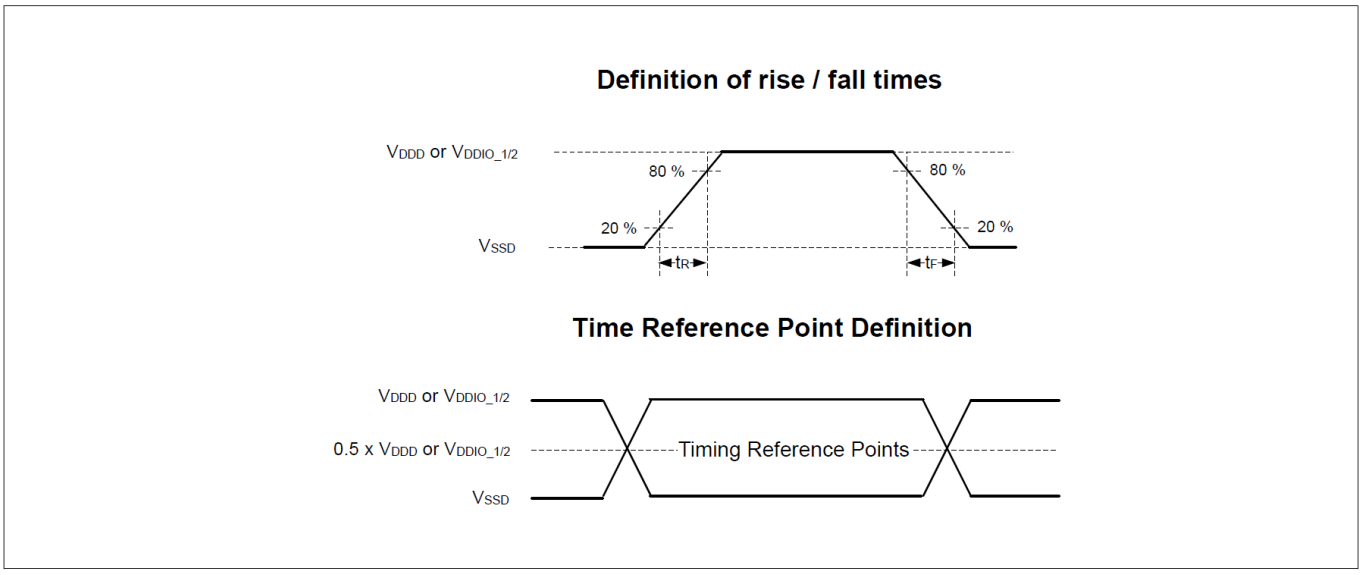


图 21 AC 时序规范

27.8 数字外设

除非另有说明， 所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 37 定时器/计数器/PWM（TCPWM）规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID120	f_C	TCPWM operating frequency	–	–	100	MHz	f_C = peripheral clock
SID121	$t_{PWMENEXT}$	Input trigger pulse width for all trigger events	2 / f_C	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMEXT}	Output trigger pulse widths	2 / f_C	–	–	ns	Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs
SID123	t_{CRES}	Resolution of counter	1 / f_C	–	–	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	1 / f_C	–	–	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	2 / f_C	–	–	ns	Minimum pulse width between Quadrature phase inputs.

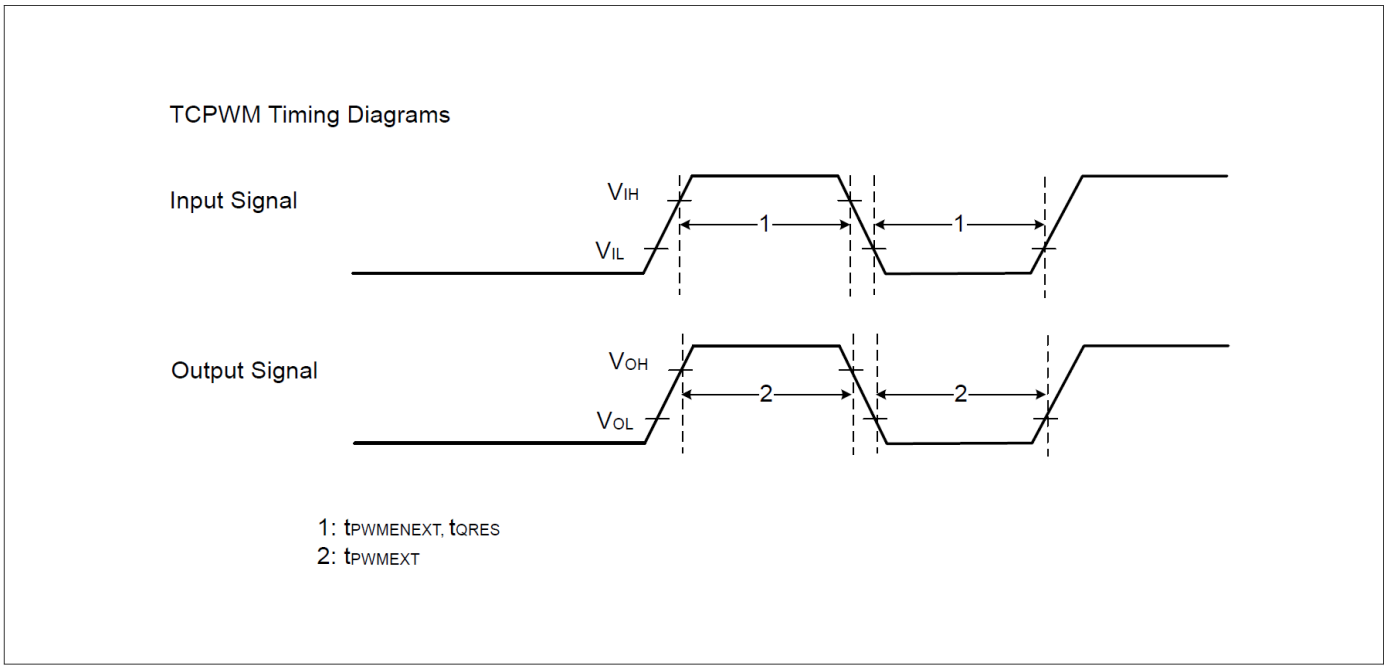


图 22 TCPWM 时序图

表 38 串行通信模块 (SCB) 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID129	f_{SCB}	SCB operating frequency	–	–	100	MHz	
I2C interface - standard mode							
SID130	f_{SCL}	SCL clock frequency	–	–	100	KHz	
SID131	$t_{HD;STA}$	Hold time, START condition	4000	–	–	ns	
SID132	t_{low}	Low period of SCL	4700	–	–	ns	
SID133	t_{HIGH}	High period of SCL	4000	–	–	ns	
SID134	$t_{SU;STA}$	Setup time for a repeated START	4700	–	–	ns	
SID135	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID136	$t_{SU;DAT}$	Data setup time	250	–	–	ns	
SID138	t_F	Fall time of SCL and SDA	–	–	300	ns	Input and output
SID139	$t_{SU;STO}$	Setup time for STOP	4000	–	–	ns	
SID140	t_{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C_b	Capacitive load for each bus line	–	–	400	pF	
SID142	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	$t_{VD;ACK}$	Data valid acknowledge time	–	–	3450	ns	
SID144	V_{OL}	LOW level output voltage	0	–	0.4	V	Open-drain at 3 mA sink current
SID145	I_{OL}	LOW level output current	3	–	–	mA	V_{OL} = 0.4 V
I2C interface-fast-mode							
SID150	f_{SCL_F}	SCL clock frequency	–	–	400	KHz	
SID151	$t_{HD;STA\_F}$	Hold time, START condition	600	–	–	ns	
SID152	t_{LOW_F}	Low period of SCL	1300	–	–	ns	
SID153	t_{HIGH_F}	High period of SCL	600	–	–	ns	
SID154	$t_{SU;STA\_F}$	Setup time for a repeated START	600	–	–	ns	
SID155	$t_{HD;DAT\_F}$	Data hold time, for receiver	0	–	–	ns	
SID156	$t_{SU;DAT\_F}$	Data setup time	100	–	–	ns	

（表格续下页……）

表 38 （续）串行通信模块（SCB）规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID158	t_{F_F}	Fall time of SCL and SDA	20× (V_{DDD} / 5.5)	–	300	ns	Input and output, GPIO_ENH: slow mode, 400 pF load
SID158A	t_{FA_F}	Fall time of SCL and SDA	0.35	–	300	ns	Input and output GPIO_STD: drive_sel<1:0>= 0b00 MIN: 10 pF load, RPU = 35.41 kΩ MAX: 400 pF load, RPU = 350 Ω
SID159	$t_{SU;STO\_F}$	Setup time for STOP	600	–	–	ns	Input and output
SID160	t_{BUF_F}	Bus free time between START and STOP	1300	–	–	ns	
SID161	C_{B_F}	Capacitive load for each bus line	–	–	400	pF	
SID162	$t_{VD;DAT\_F}$	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	$t_{VD;ACK\_F}$	Data valid acknowledge time	–	–	900	ns	
SID164	t_{SP_F}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
SID165	V_{OL_F}	LOW level output voltage	0	–	0.4	V	Open-drain at 3 mA sink current
SID165	I_{OL_F}	LOW level output current	3	–	–	mA	V_{OL} = 0.4 V
SID167	I_{OL2_F}	LOW level output current	6	–	–	mA	V_{OL} = 0.6 V[1)]
I2C interface-fast-plus mode							
SID170	f_{SCL_FP}	SCL clock frequency	–	–	1	MHz	
SID171	$t_{HD;STA\_FP}$	Hold time, START condition	260	–	–	ns	
SID172	t_{LOW_FP}	Low period of SCL	500	–	–	ns	
SID173	t_{HIGH_FP}	High period of SCL	260	–	–	ns	
SID174	$t_{SU;STA\_FP}$	Setup time for a repeated START	260	–	–	ns	
SID175	$t_{HD;DAT\_FP}$	Data hold time, for receiver	0	–	–	ns	
SID176	$t_{SU;DAT\_FP}$	Data setup time	50	–	–	ns	

（表格续下页……）

表 38 （续）串行通信模块（SCB）规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID178	t_{F_FP}	Fall time of SCL and SDA	20 × (V_{DDD} / 5.5)	–	160	ns	Input and output 20-pF load GPIO_ENH: slow mode
SID179	$t_{SU;STO\_FP}$	Setup time for STOP	260	–	–	ns	Input and output
SID180	t_{BUF_FP}	Bus free time between START and STOP	500	–	–	ns	
SID181	C_{B_FP}	Capacitive load for each bus line	–	–	20	pF	
SID182	$t_{VD;DAT\_FP}$	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	$t_{VD;ACK\_FP}$	Data valid acknowledge time	–	–	450	ns	
SID184	t_{SP_FP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
SID186	V_{OL_FP}	LOW level output voltage	0	–	0.4	V	Open-drain at 3 mA sink current
SID187	I_{OL_FP}	LOW level output current	3	–	–	mA	V_{OL} = 0.4 V[2)]
SPI interface master (Full-clock mode: LATE_MISO_SAMPLE = 1) [Conditions: drive_sel<1:0>= 0x]							
SID190	F_{SPI}	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0
SID191	T_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns	
SID192	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	40	–	–	ns	
SID193	T_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	
SID194	$t_{W\_SCLK\_H\_L}$	SPI SCLK pulse width HIGH or LOW	–	0.4 × (1 / f_{SPI})	–	ns	
SID196	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	
SID198	t_{EN_SETUP}	SSEL valid, before the first SCK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period
SID199	t_{EN_SHOLD}	SSEL hold, after the last SCK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period

（表格续下页……）

表 38 （续）串行通信模块（SCB）规格

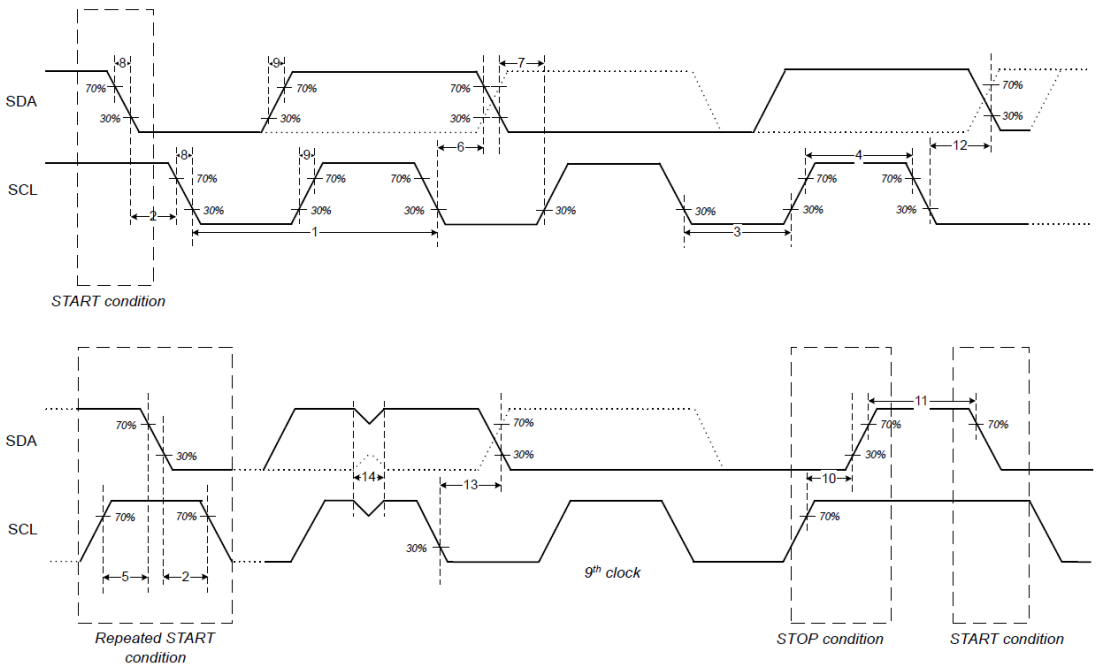
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID195	C_{SPIM_MS}	SPI capacitive load	–	–	10	pF	
SPI interface slave (internally clocked) [Conditions: drive_sel<1:0>= 0x]							
SID205	f_{SPI_INT}	SPI operating frequency	–	–	10	MHz	
SID206	t_{DMI_INT}	SPI Slave: MOSI valid before Sclock capturing edge	5	–	–	ns	
SID207	t_{DSO_INT}	SPI Slave: MISO valid after Sclock driving edge, in the internal-clocked mode	–	–	62	ns	
SID208	t_{HSP}	SPI Slave: Previous MISO data hold time	3	–	–	ns	
SID209	$t_{EN\_SETUP\_INT}$	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	
SID210	$t_{EN\_HOLD\_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	
SID211	$t_{EN\_SETUP\_PRE}$	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	
SID212	$t_{EN\_HOLD\_PRE}$	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	
SID213	$t_{EN\_SETUP\_CO}$	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	
SID214	$t_{EN\_HOLD\_CO}$	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	
SID215	$t_{W\_DIS\_INT}$	SPI Slave Select inactive time	40	–	–	ns	
SID216	$t_{W\_SCLKH\_INT}$	SPI SCLK pulse width HIGH	20	–	–	ns	
SID217	$t_{W\_SCLKL\_INT}$	SPI SCLK pulse width LOW	20	–	–	ns	
SID218	t_{SIH_INT}	SPI MOSI hold from SCLK	12	–	–	ns	
SID219	C_{SPIS_INT}	SPI Capacitive Load	–	–	10	pF	
SPI interface slave (externally clocked) [Conditions: drive_sel<1:0>= 0x]							
SID220	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	
SID221	t_{DMI_EXT}	SPI Slave: MOSI valid before Sclock capturing edge	5	–	–	ns	

（表格续下页……）

表 38 （续）串行通信模块（SCB）规格

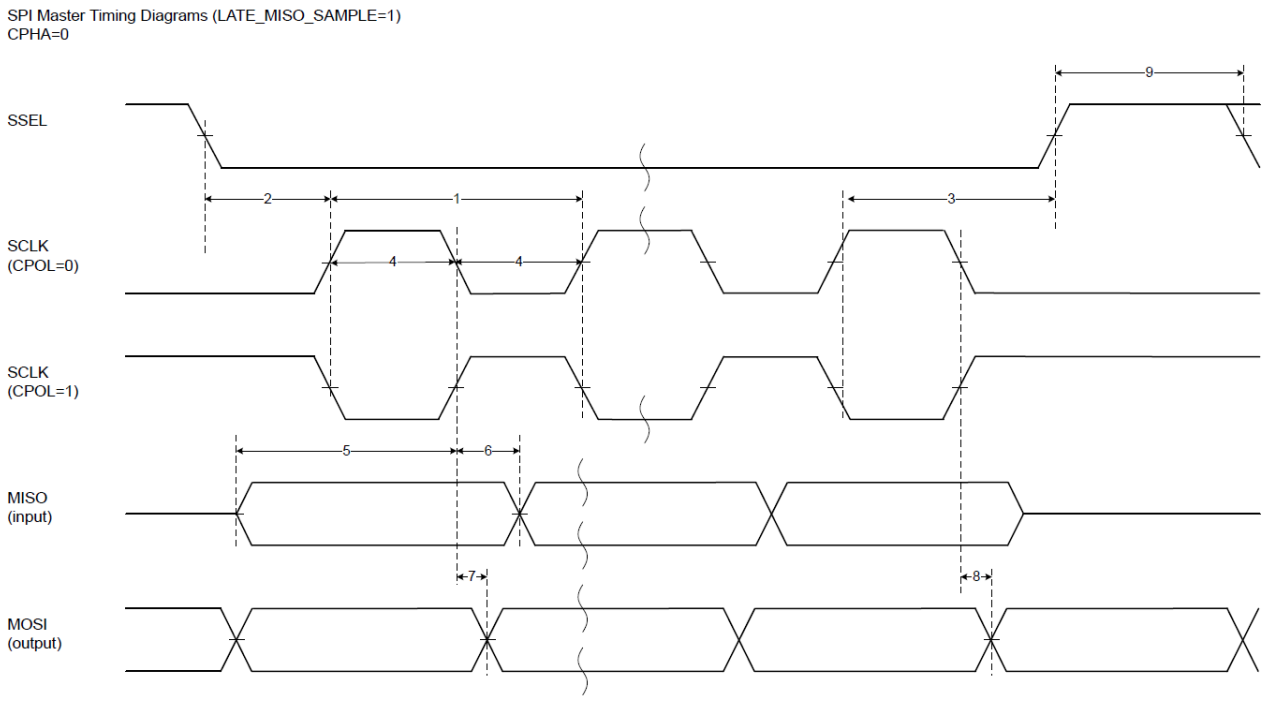
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID222	t_{DSO_EXT}	SPI Slave: MISO valid after Sclock driving edge, in the external-clocked mode	–	–	32	ns	
SID223	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	
SID224	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCK valid edge	40	–	–	ns	
SID225	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	40	–	–	ns	
SID226	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	80	–	–	ns	
SID227	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	34	–	–	ns	
SID228	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	34	–	–	ns	
SID229	t_{SIH_EXT}	SPI MOSI hold from SCLK	20	–	–	ns	
SID230	C_{SPIS_EXT}	SPI capacitive load	–	–	10	pF	
SID231	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	
UART interface							
SID240	f_{BPS}	Data rate	–	–	10	MBps	

1) 为了以 400 kHz 的频率驱动满总线负载， 在 0.6 V V_{OL} 时需要 6 mA I_{OL}。
2) 为了以 1 MHz 的频率驱动满总线负载， 在 0.4 V V_{OL} 时需要 20 mA I_{OL}。但是，该器件不支持此模式。



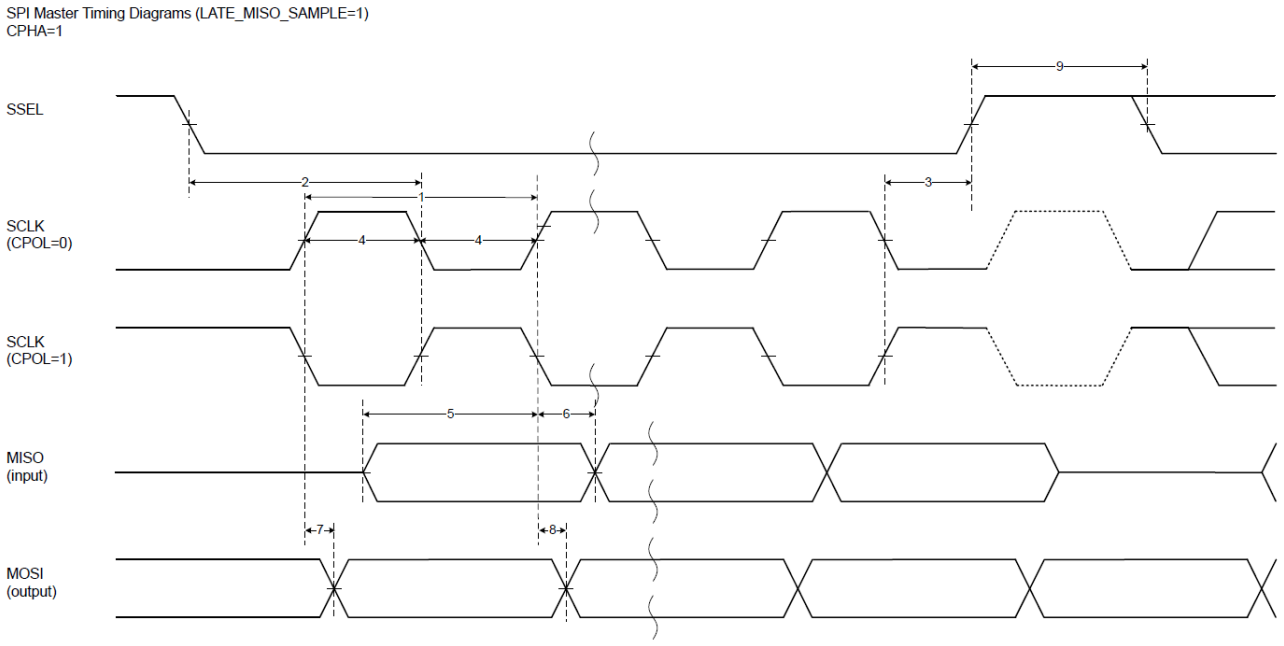
1: SCL clock period = $1/f_{SCL}$
2: Hold time, START condition = $t_{HD;STA}$
3: LOW period of SCL = t_{LOW}
4: HIGH period of SCL = t_{HIGH}
5: Setup time for a repeated START = $t_{SU;STA}$
6: Data hold time, for receiver = $t_{HD;DAT}$
7: Data setup time = $t_{SU;DAT}$
8: Fall time of SCL and SDA = t_F
9: Rise time of SCL and SDA = t_R
10: Setup time for STOP = $t_{SU;STO}$
11: Bus-free time between START and STOP = t_{BUF}
12: Time for data signal from SCL LOW to SDA output = $t_{VD;DAT}$
13: Data valid acknowledge time = $t_{VD;ACK}$
14: Pulse width of spikes that must be suppressed by the input filter = t_{SP}

图 23 I²C 时序图



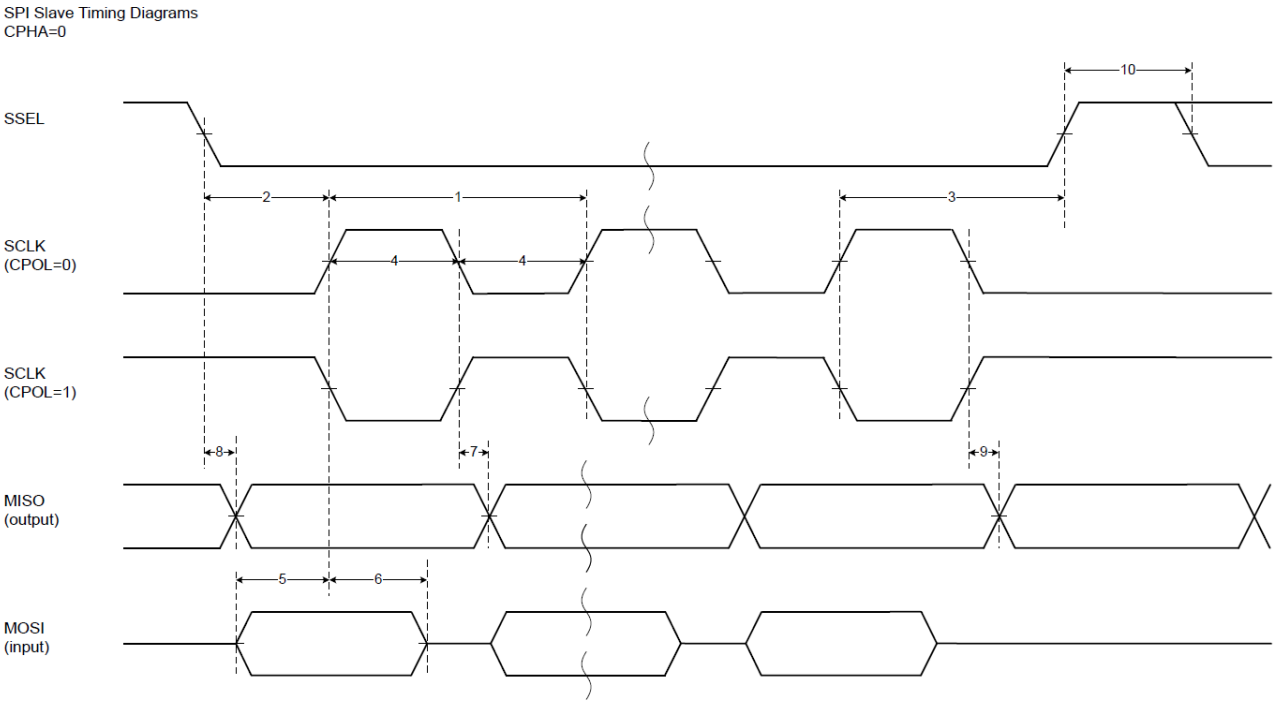
1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{DHI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

图 24　　SPI 主机时序图（低时钟相位）



1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{HDI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

图 25　　SPI 主机时序图（高时钟相位）



1: SCLK period = 1 / f_{SPI_EXT}
2: enable lead time (setup) = $t_{EN\_SETUP\_EXT}$
3: enable trail time (hold) = $t_{EN\_HOLD\_EXT}$
4: SCLK high or low time = $t_{w\_SCLKH\_EXT}$ = $t_{w\_SCLKL\_EXT}$
5: input data setup time = t_{DMI_EXT}
6: input data hold time = t_{SIH_EXT}
7: output data valid after SCLK driving edge = t_{DSO_EXT}
8: output data valid after SSEL falling edge (CPHA=0) = t_{VSS_EXT}
9: output data hold time = t_{HSO}
10: SSEL high pulse width = t_{DIS_EXT}

图 26　　SPI 从机时序图（低时钟相位）

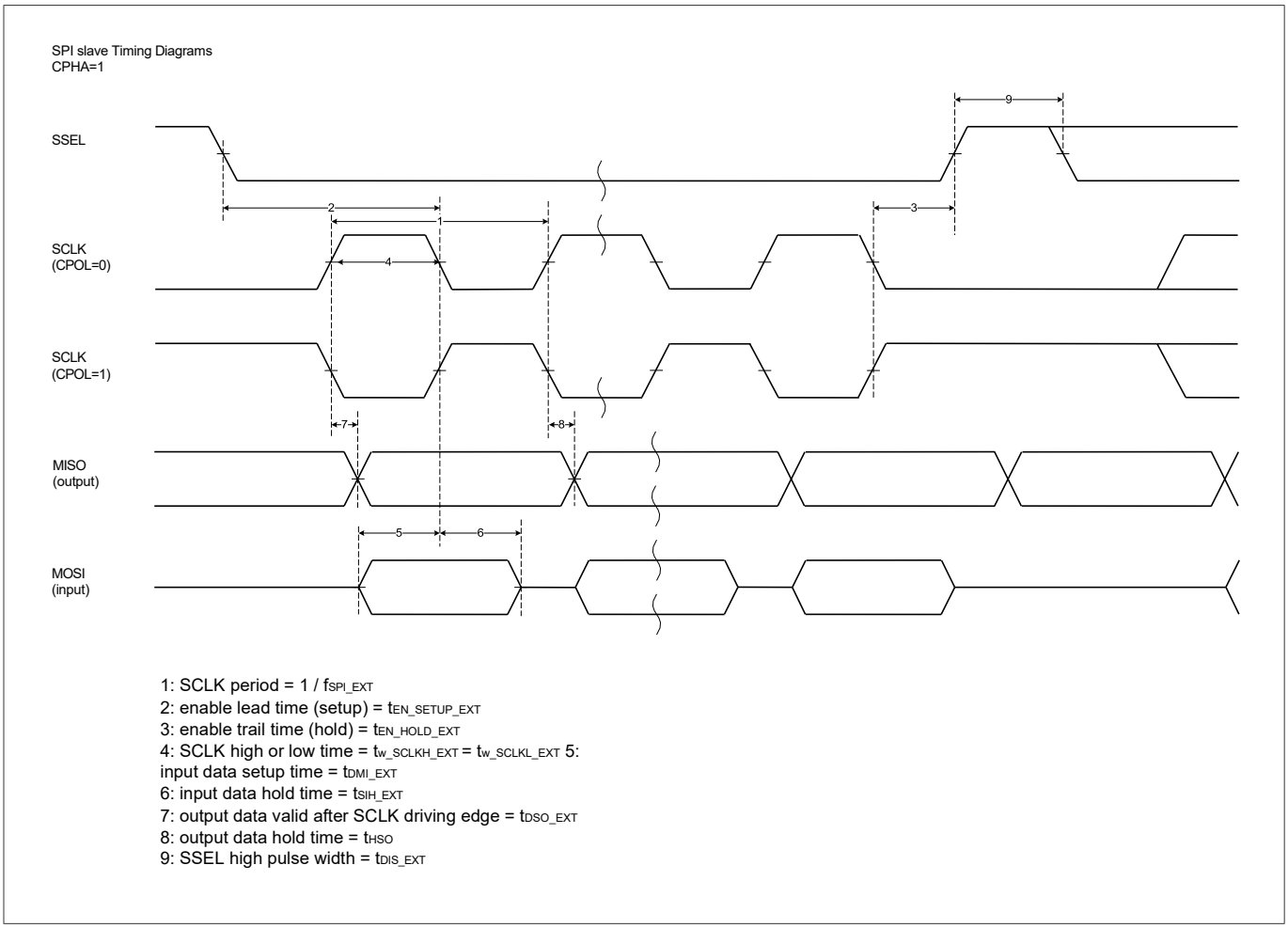


图 27　　SPI 从机时序图（高时钟相位）

27.8.1　LIN 规格

表 39　　LIN 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID249	f_{LIN}	Internal clock frequency to the LIN block	–	–	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	Guaranteed by design

27.8.2 CAN FD 规格

表 40 CAN FD 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID630	f_{HCLK}	System clock frequency	–	–	100	MHz	$f_{cclk} \leq f_{hclk}$, Guaranteed by design
SID631	f_{CCLK}	CAN clock frequency	–	–	100	MHz	$f_{cclk} \leq f_{hclk}$, Guaranteed by design

27.8.3 CXPI 规格

表 41 PWM 模式的 CXPI 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID400	f_{CXPI}	CXPI operating frequency	–	–	100	MHz	Guaranteed by design
SID401	f_{BRC}	Bit rate of CXPI bus	–	–	20	kbps	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design
SID402	dt_{BIT_CONT}	Difference between the signal output on TXD and the bit width (t_{BIT_REF}) of the reference communication speed	–0.5	–	0.5	%	Guaranteed by design
SID403	$t_{TX\_0\_HI\_CONT}$	Time to detect the signal input on RXD as HIGH	0.02	–	–	t_{Bit}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design
SID404	$t_{TX\_DIF\_CONT}$	Difference between the LOW width of a certain threshold value to be correctly discriminated as the logic value 1 and the logic value 0 for the signal input on RXD $t_{TX\_DIF\_CONT} = (t_{TX\_0\_LO} - t_{TX\_1\_LO})$	0.05	–	–	t_{Bit}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design
SID406	$t_{TX\_0\_PD\_CONT}$	Time from the falling edge input of RXD to the falling edge output of TXD when the logic value 0 outputs at the slave node	–	–	0.01	t_{Bit}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '0', Guaranteed by design
SID406A	$t_{TX\_0\_PD\_CONT}$	Time from the falling edge input of RXD to the falling edge output of TXD when the logic value 0 outputs at the slave node	–	–	0.0125	t_{Bit}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '1', Guaranteed by design

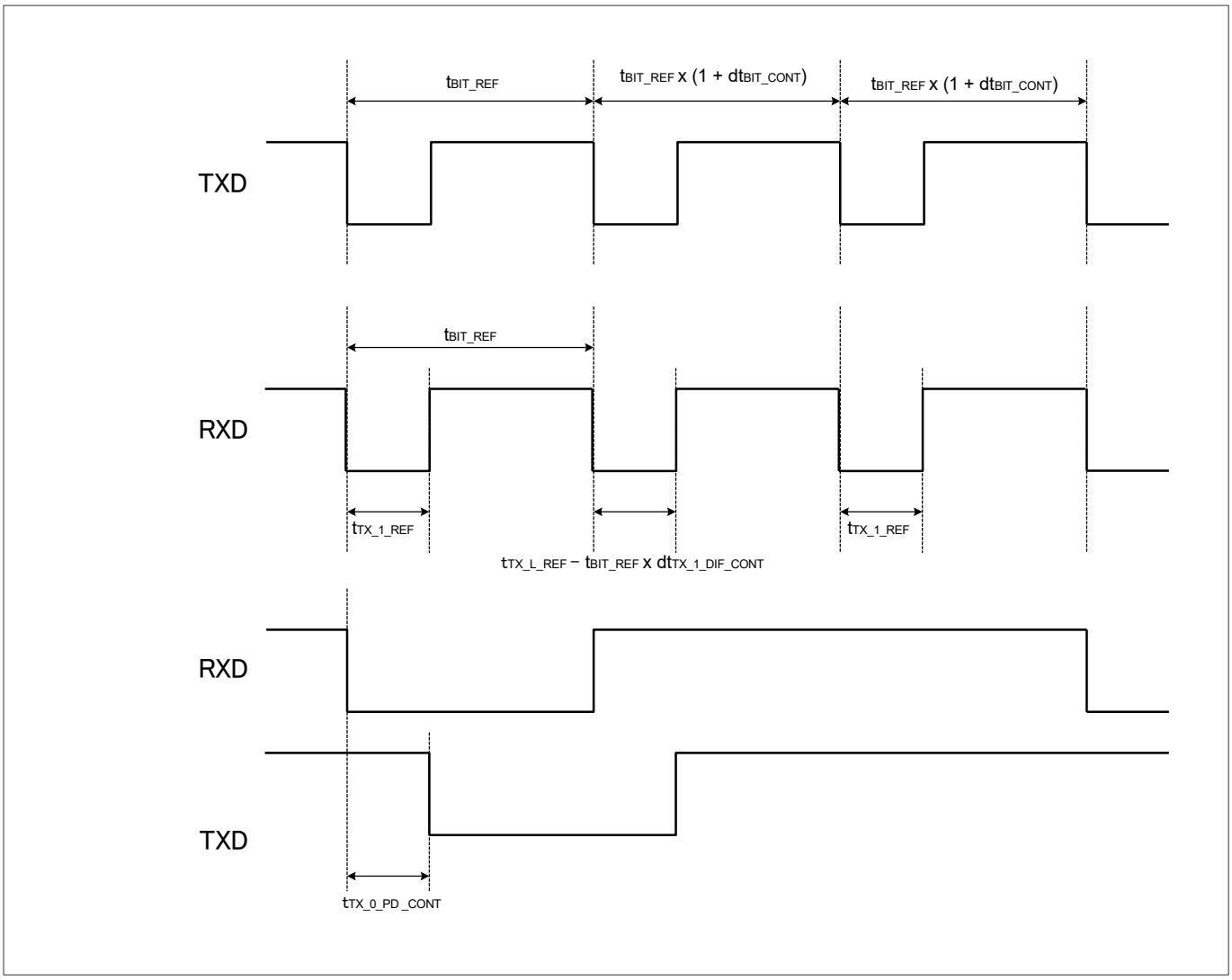


图 28 CXPI 规格

27.9 存储器

除非另有说明，所有规格均适用于 –40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 42 Flash DC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID260	V_{PE}	Erase and program voltage	2.7	–	5.5	V	

表 43 Flash AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257	f_{FO}	Maximum flash memory operation frequency	–	–	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 160 MHz

（表格续下页……）

27 Electrical specifications

表 43 （续） Flash AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID254	t_{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	–	–	37.5	µs	
SID255	$t_{ERS\_RES\_SUS}$	Minimum time allowed from erase resume to erase suspend	250	–	–	µs	Guaranteed by design
SID258	t_{BC_WF}	Blank check time for N-bytes of work-flash	–	–	10 + 0.3 × N	µs	At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time
SID259	$t_{SECTORERASE1}$	Sector erase time (Code-flash: 32 KB)	–	45	90	ms	Includes internal preprogramming time
SID259A	$t_{SECTORERASE2}$	Sector erase time (Code-flash: 8 KB)	–	15	30	ms	Includes internal preprogramming time
SID261	$t_{SECTORERASE3}$	Sector erase time (Work-flash, 2 KB)	–	80	160	ms	Includes internal preprogramming time
SID262	$t_{SECTORERASE4}$	Sector erase time (Work-flash, 128 bytes)	–	5	15	ms	Includes internal preprogramming time
SID263	t_{WRITE1}	64-bit write time (Code-flash)	–	30	60	µs	Excludes system overhead time
SID264	t_{WRITE2}	256-bit write time (Code-flash)	–	40	70	µs	Excludes system overhead time
SID265	t_{WRITE3}	4096-bit write time (Code-flash)[1)]	–	320	1200	µs	Excludes system overhead time
SID266	t_{WRITE4}	32-bit write time (Work-flash)	–	30	60	µs	Excludes system overhead time
SID267	t_{FRET1}	Code-flash retention. 1000 program/erase cycles	20	–	–	years	T_A (power on and off) ≤ 85 °C average
SID268	t_{FRET3}	Work-flash retention. 125,000 program/erase cycles	20	–	–	years	T_A (power on and off) ≤ 85 °C average
SID269	t_{FRET4}	Work-flash retention. 250,000 program/erase cycles	10	–	–	years	T_A (power on and off) ≤ 85 °C average
SID612A	I_{CC_ACT2}	Program operating current (Code or Work-flash)	–	15	53	mA	V_{DDD} = 5 V Guaranteed by design
SID613A	I_{CC_ACT3}	Erase operating current (Code or Work-flash)	–	15	53	mA	V_{DDD} = 5 V Guaranteed by design

1) 代码闪存包括一个 4096 位的“写入缓冲区”。如果应用软件多次写入该缓冲器，要获得总写入时间，请将一个扇区写入时间乘以相应的因子（假设因子为 64，例如 64 x 512 B = 32 KB [一个扇区]

27.10 系统资源

除非另有说明，所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

表 44 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
Power-on-reset specifications							
SID270	V_{POR_R}	V_{DDD} rising voltage to de assert POR	1.5	–	2.35	V	Guaranteed by design
SID276	V_{POR_F}	V_{DDD} falling voltage to assert POR	1.45	–	2.1	V	
SID271	V_{POR_H}	Level detection hysteresis	20	–	300	mV	Guaranteed by design
SID272	t_{DLY_POR}	Delay between V_{DDD} rising through 2.3 V and an internal deassertion of POR	–	–	3	µs	Guaranteed by design
SID273	t_{POFF}	V_{DDD} Power off time	100	–	–	µs	V_{DDD} < 1.45 V
SID274	POR_RR1	V_{DDD} power ramp rate with robust BOD (BOD operation is guaranteed)	–	–	100	mV/µs	This ramp supports robust BOD
SID275	POR_RR2	V_{DDD} power ramp rate without robust BOD	–	–	1000	mV/µs	This ramp does not support robust BOD t_{POFF} must be satisfied
High-voltage BOD (HV BOD) specifications							
SID500	$V_{TR\_2P7\_R}$	HV BOD 2.7 V rising detection point for V_{DDD} and V_{DDA} (default)	2.474	2.55	2.627	V	
SID501	$V_{TR\_2P7\_F}$	HV BOD 2.7 V falling detection point for V_{DDD} and V_{DDA} (default)	2.449	2.525	2.601	V	
SID502	$V_{TR\_3P0\_R}$	HV BOD 3.0 V rising detection point for V_{DDD} and V_{DDA}	2.765	2.85	2.936	V	
SID503	$V_{TR\_3P0\_F}$	HV BOD 3.0 V falling detection point for V_{DDD} and V_{DDA}	2.74	2.825	2.91	V	
SID505	HVBOD_RR_A	Power ramp rate: V_{DDD} and V_{DDA} (Active)	–	–	100	mV/µs	
SID506	HVBOD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA} (DeepSleep)	–	–	10	mV/µs	
SID507	$t_{DLY\_ACT\_HVBOD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD signal transitioning	–	–	0.5	µs	Guaranteed by design

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表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID507A	$t_{DLY\_ACT\_HVBOD}$	Active mode delay between V_{DDA} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and internal HV BOD signal transitioning	–	–	1	µs	Guaranteed by design
SID507B	$t_{DLY\_DS\_HVBOD}$	DeepSleep mode delay between V_{DDD}/V_{DDA} falling/ rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD signal transitioning	–	–	4	µs	Guaranteed by design
SID508	t_{RES_HVBOD}	Response time of HV BOD, V_{DDD}/V_{DDA} supply. (For falling-then-rising supply at max ramp rate; threshold is $V_{TR\_2P7\_F}$ or $V_{TR\_3P0\_F}$.)	100	–	–	ns	Guaranteed by design
Low-voltage BOD (LV BOD) specifications							
SID510	$V_{TR\_R\_LVBOD}$	LV BOD rising detection point for V_{CCD}	0.917	0.945	0.973	V	
SID511	$V_{TR\_F\_LVBOD}$	LV BOD falling detection point for V_{CCD}	0.892	0.92	0.948	V	
SID515	$t_{DLY\_ACT\_LVBOD}$	Active delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD signal transitioning	–	–	1	µs	Guaranteed by design
SID515A	$t_{DLY\_DS\_LVBOD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD signal transitioning	–	–	12	µs	Guaranteed by design
SID516	t_{RES_LVBOD}	Response time of LV BOD. (For falling-then-rising supply at max ramp rate; threshold is $V_{TR\_F\_LVBOD}$.)	100	–	–	ns	Guaranteed by design
Low-voltage detector (LVD) DC specifications							
SID520	$V_{TR\_2P8\_F}$	LVD 2.8 V falling detection point for V_{DDD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	$V_{TR\_2P9\_F}$	LVD 2.9 V falling detection point for V_{DDD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	$V_{TR\_3P0\_F}$	LVD 3.0 V falling detection point for V_{DDD}	Typ – 4%	3000	Typ + 4%	mV	

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表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID523	$V_{TR\_3P1\_F}$	LVD 3.1 V falling detection point for V_{DDD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	$V_{TR\_3P2\_F}$	LVD 3.2 V falling detection point for V_{DDD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	$V_{TR\_3P3\_F}$	LVD 3.3 V falling detection point for V_{DDD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	$V_{TR\_3P4\_F}$	LVD 3.4 V falling detection point for V_{DDD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	$V_{TR\_3P5\_F}$	LVD 3.5 V falling detection point for V_{DDD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	$V_{TR\_3P6\_F}$	LVD 3.6 V falling detection point for V_{DDD}	Typ – 4%	3600	Typ + 4%	mV	
SID529	$V_{TR\_3P7\_F}$	LVD 3.7 V falling detection point for V_{DDD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	$V_{TR\_3P8\_F}$	LVD 3.8 V falling detection point for V_{DDD}	Typ – 4%	3800	Typ + 4%	mV	
SID531	$V_{TR\_3P9\_F}$	LVD 3.9 V falling detection point for V_{DDD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	$V_{TR\_4P0\_F}$	LVD 4.0 V falling detection point for V_{DDD}	Typ – 4%	4000	Typ + 4%	mV	
SID533	$V_{TR\_4P1\_F}$	LVD 4.1 V falling detection point for V_{DDD}	Typ – 4%	4 100	Typ + 4%	mV	
SID534	$V_{TR\_4P2\_F}$	LVD 4.2 V falling detection point for V_{DDD}	Typ – 4%	4 200	Typ + 4%	mV	
SID535	$V_{TR\_4P3\_F}$	LVD 4.3 V falling detection point for V_{DDD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	$V_{TR\_4P4\_F}$	LVD 4.4 V falling detection point for V_{DDD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	$V_{TR\_4P5\_F}$	LVD 4.5 V falling detection point for V_{DDD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	$V_{TR\_4P6\_F}$	LVD 4.6 V falling detection point for V_{DDD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	$V_{TR\_4P7\_F}$	LVD 4.7 V falling detection point for V_{DDD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	$V_{TR\_4P8\_F}$	LVD 4.8 V falling detection point for V_{DDD}	Typ – 4%	4 800	Typ + 4%	mV	
SID541	$V_{TR\_4P9\_F}$	LVD 4.9 V falling detection point for V_{DDD}	Typ – 4%	4900	Typ + 4%	mV	

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表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID542	$V_{TR\_5P0\_F}$	LVD 5.0 V falling detection point for V_{DDD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	$V_{TR\_5P1\_F}$	LVD 5.1 V falling detection point for V_{DDD}	Typ – 4%	5 100	Typ + 4%	mV	
SID544	$V_{TR\_5P2\_F}$	LVD 5.2 V falling detection point for V_{DDD}	Typ – 4%	5 200	Typ + 4%	mV	
SID545	$V_{TR\_5P3\_F}$	LVD 5.3 V falling detection point for V_{DDD}	Typ – 4%	5300	Typ + 4%	mV	
SID546	$V_{TR\_2P8\_R}$	LVD 2.8 V rising detection point for V_{DDD}	Typ – 4%	2825	Typ + 4%	mV	Same as $V_{TR\_2P8\_F}$ + 25 mV
SID547	$V_{TR\_2P9\_R}$	LVD 2.9 V rising detection point for V_{DDD}	Typ – 4%	2925	Typ + 4%	mV	Same as $V_{TR\_2P9\_F}$ + 25 mV
SID548	$V_{TR\_3P0\_R}$	LVD 3.0 V rising detection point for V_{DDD}	Typ – 4%	30 25	Typ + 4%	mV	Same as $V_{TR\_3P0\_F}$ + 25 mV
SID549	$V_{TR\_3P1\_R}$	LVD 3.1 V rising detection point for V_{DDD}	Typ – 4%	3125	Typ + 4%	mV	Same as $V_{TR\_3P1\_F}$ + 25 mV
SID550	$V_{TR\_3P2\_R}$	LVD 3.2 V rising detection point for V_{DDD}	Typ – 4%	3225	Typ + 4%	mV	Same as $V_{TR\_3P2\_F}$ + 25 mV
SID551	$V_{TR\_3P3\_R}$	LVD 3.3 V rising detection point for V_{DDD}	Typ – 4%	3325	Typ + 4%	mV	Same as $V_{TR\_3P3\_F}$ + 25 mV
SID552	$V_{TR\_3P4\_R}$	LVD 3.4 V rising detection point for V_{DDD}	Typ – 4%	3425	Typ + 4%	mV	Same as $V_{TR\_3P4\_F}$ + 25 mV
SID553	$V_{TR\_3P5\_R}$	LVD 3.5 V rising detection point for V_{DDD}	Typ – 4%	3525	Typ + 4%	mV	Same as $V_{TR\_3P5\_F}$ + 25 mV
SID554	$V_{TR\_3P6\_R}$	LVD 3.6 V rising detection point for V_{DDD}	Typ – 4%	3625	Typ + 4%	mV	Same as $V_{TR\_3P6\_F}$ + 25 mV
SID555	$V_{TR\_3P7\_R}$	LVD 3.7 V rising detection point for V_{DDD}	Typ – 4%	3725	Typ + 4%	mV	Same as $V_{TR\_3P7\_F}$ + 25 mV
SID556	$V_{TR\_3P8\_R}$	LVD 3.8 V rising detection point for V_{DDD}	Typ – 4%	3825	Typ + 4%	mV	Same as $V_{TR\_3P8\_F}$ + 25 mV

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表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID557	$V_{TR\_3P9\_R}$	LVD 3.9 V rising detection point for V_{DDD}	Typ – 4%	3925	Typ + 4%	mV	Same as $V_{TR\_3P9\_F}$ + 25 mV
SID558	$V_{TR\_4P0\_R}$	LVD 4.0 V rising detection point for V_{DDD}	Typ – 4%	40 25	Typ + 4%	mV	Same as $V_{TR\_4P0\_F}$ + 25 mV
SID559	$V_{TR\_4P1\_R}$	LVD 4.1 V rising detection point for V_{DDD}	Typ – 4%	4125	Typ + 4%	mV	Same as $V_{TR\_4P1\_F}$ + 25 mV
SID560	$V_{TR\_4P2\_R}$	LVD 4.2 V rising detection point for V_{DDD}	Typ – 4%	4225	Typ + 4%	mV	Same as $V_{TR\_4P2\_F}$ + 25 mV
SID561	$V_{TR\_4P3\_R}$	LVD 4.3 V rising detection point for V_{DDD}	Typ – 4%	4325	Typ + 4%	mV	Same as $V_{TR\_4P3\_F}$ + 25 mV
SID562	$V_{TR\_4P4\_R}$	LVD 4.4 V rising detection point for V_{DDD}	Typ – 4%	4425	Typ + 4%	mV	Same as $V_{TR\_4P4\_F}$ + 25 mV
SID563	$V_{TR\_4P5\_R}$	LVD 4.5 V rising detection point for V_{DDD}	Typ – 4%	45 25	Typ + 4%	mV	Same as $V_{TR\_4P5\_F}$ + 25 mV
SID564	$V_{TR\_4P6\_R}$	LVD 4.6 V rising detection point for V_{DDD}	Typ – 4%	4625	Typ + 4%	mV	Same as $V_{TR\_4P6\_F}$ + 25 mV
SID565	$V_{TR\_4P7\_R}$	LVD 4.7 V rising detection point for V_{DDD}	Typ – 4%	4725	Typ + 4%	mV	Same as $V_{TR\_4P7\_F}$ + 25 mV
SID566	$V_{TR\_4P8\_R}$	LVD 4.8 V rising detection point for V_{DDD}	Typ – 4%	4825	Typ + 4%	mV	Same as $V_{TR\_4P8\_F}$ + 25 mV
SID567	$V_{TR\_4P9\_R}$	LVD 4.9 V rising detection point for V_{DDD}	Typ – 4%	4925	Typ + 4%	mV	Same as $V_{TR\_4P9\_F}$ + 25 mV
SID568	$V_{TR\_5P0\_R}$	LVD 5.0 V rising detection point for V_{DDD}	Typ – 4%	50 25	Typ + 4%	mV	Same as $V_{TR\_5P0\_F}$ + 25 mV
SID569	$V_{TR\_5P1\_R}$	LVD 5.1 V rising detection point for V_{DDD}	Typ – 4%	5125	Typ + 4%	mV	Same as $V_{TR\_5P1\_F}$ + 25 mV

（表格续下页.....）

表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID570	$V_{TR\_5P2\_R}$	LVD 5.2 V rising detection point for V_{DDD}	Typ – 4%	5225	Typ + 4%	mV	Same as $V_{TR\_5P2\_F}$ + 25 mV
SID571	$V_{TR\_5P3\_R}$	LVD 5.3 V rising detection point for V_{DDD}	Typ – 4%	5325	Typ + 4%	mV	Same as $V_{TR\_5P3\_F}$ + 25 mV
SID573	LVD_RR_A	Power ramp rate: V_{DDD} (Active)	–	–	100	mV/µs	
SID574	LVD_RR_DS	Power ramp rate: V_{DDD} (DeepSleep)	–	–	10	mV/µs	
SID575	$t_{DLY\_ACT\_LVD}$	Active mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning	–	–	1	µs	Guaranteed by design
SID575A	$t_{DLY\_DS\_LVD}$	DeepSleep mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD signal rising	–	–	4	µs	Guaranteed by design
SID576	t_{RES_LVD}	Response time of LVD, V_{DDD} supply. LVD guaranteed to generate pulse for V_{DDD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling point)	100	–	–	ns	Guaranteed by design
High-voltage OVD (HV OVD) specifications							
SID580	$V_{TR\_5P0\_R}$	HV OVD 5.0-V rising detection point for V_{DDD} and V_{DDA}	5.049	5.205	5.361	V	
SID581	$V_{TR\_5P0\_F}$	HV OVD 5.0-V falling detection point for V_{DDD} and V_{DDA}	5.025	5.18	5.335	V	
SID582	$V_{TR\_5P5\_R}$	HV OVD 5.5-V rising detection point for V_{DDD} and V_{DDA} (default)	5.548	5.72	5.892	V	
SID583	$V_{TR\_5P5\_F}$	HV OVD 5.5-V falling detection point for V_{DDD} and V_{DDA} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V_{DDD} and V_{DDA} (Active)	–	–	100	mV/µs	
SID586	HVOVD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA} (DeepSleep)	–	–	10	mV/µs	

（表格续下页……）

表 44 （续） 系统资源

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID587	$t_{DLY\_ACT\_HVOVD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning	–	–	1	µs	Guaranteed by design
SID587A	$t_{DLY\_ACT\_HVOVD\_A}$	Active mode delay between V_{DDA} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning	–	–	1.5	µs	Guaranteed by design
SID587B	$t_{DLY\_DS\_HVOVD}$	DeepSleep mode delay between V_{DDD}/V_{DDA} falling/ rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning	–	–	4	µs	Guaranteed by design
SID588	t_{RES_HVOVD}	Response time of HV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR\_5P0\_R}$ or $V_{TR\_5P5\_R}$.)	100	–	–	ns	Guaranteed by design
Low-voltage OVD (LV OVD) specifications							
SID590	$V_{TR\_R\_LVOVD}$	LV OVD rising detection point for V_{CCD}	1.261	1.3	1.339	V	
SID591	$V_{TR\_F\_LVOVD}$	LV OVD falling detection point for V_{CCD}	1.237	1.275	1.313	V	
SID595	$t_{DLY\_ACT\_LVOVD}$	Active mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD signal transitioning	–	–	1	µs	Guaranteed by design
SID595A	$t_{DLY\_DS\_LVOVD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD signal transitioning	–	–	12	µs	Guaranteed by design
SID596	t_{RES_LVOVD}	Response time of LV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR\_R\_LVOVD}$.)	100	–	–	ns	Guaranteed by design
Over current detection (OCD) specifications							
SID598	I_{OCD}	OCD detection range for V_{CCD}	156	–	315	mA	Guaranteed by design
SID599	I_{OCD_DPSLP}	Over current detection range in DeepSleep mode	18	–	72	mA	Guaranteed by design

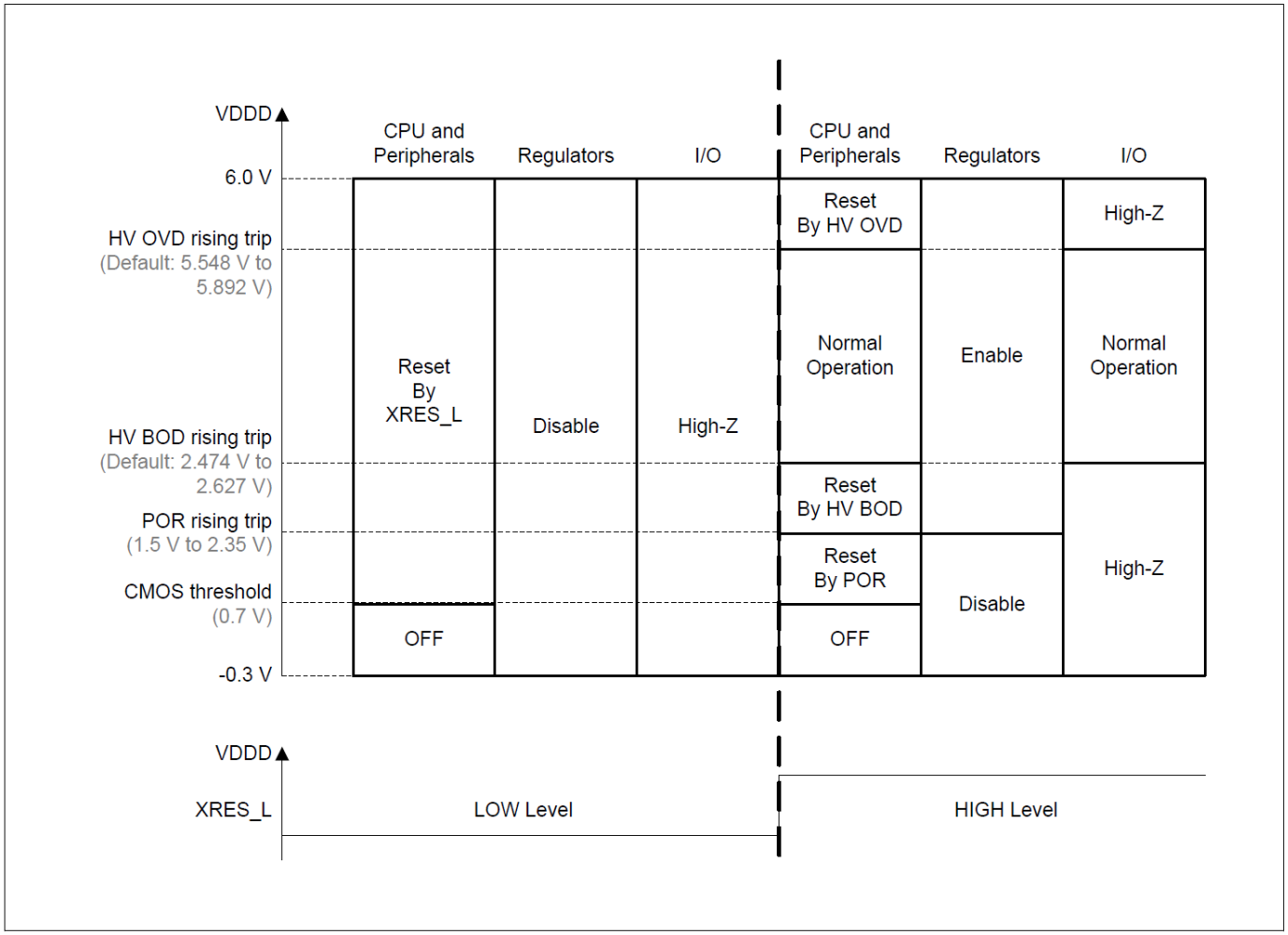

图 29　　器件操作电源范围

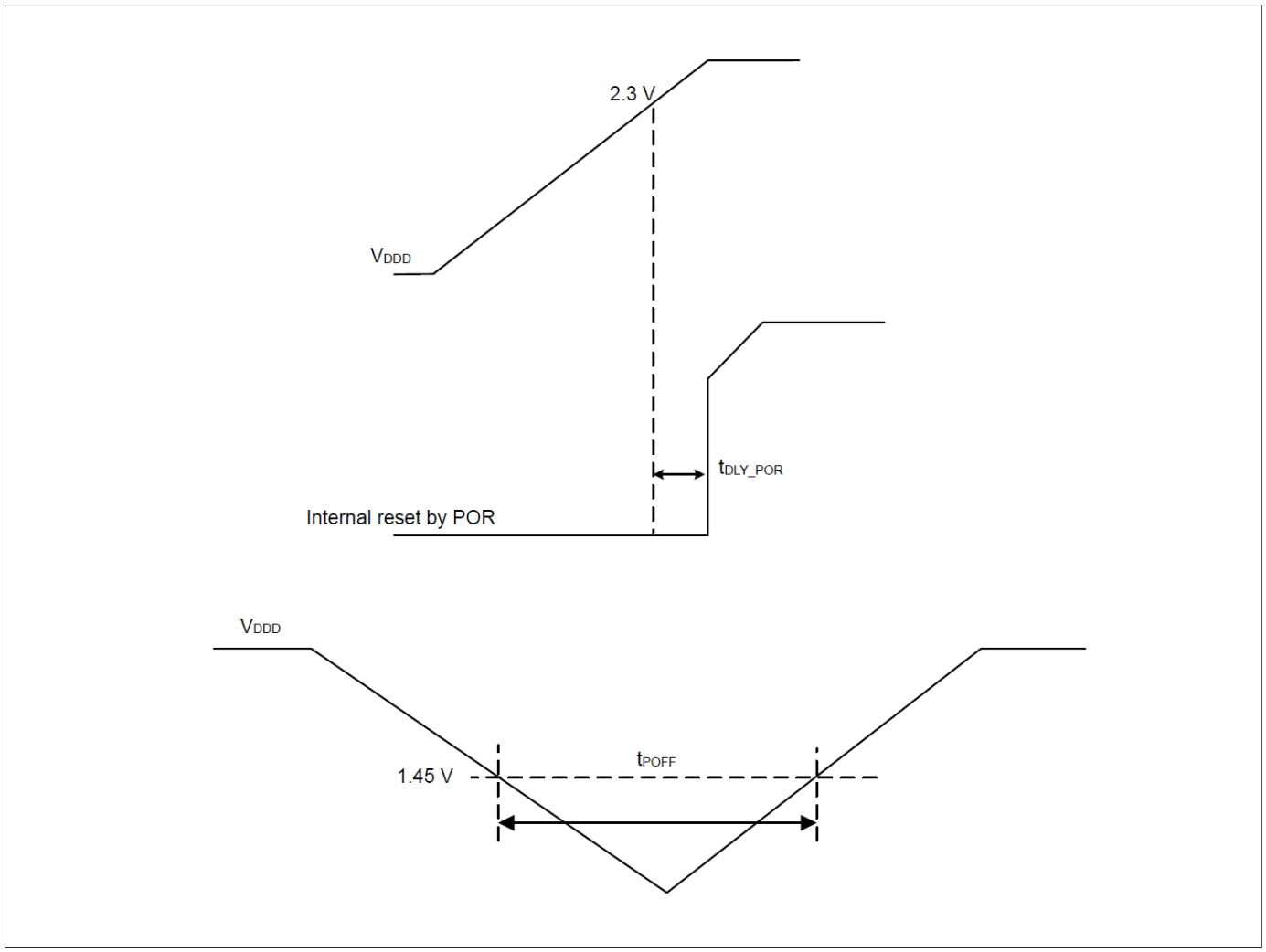

图 30 POR 规格

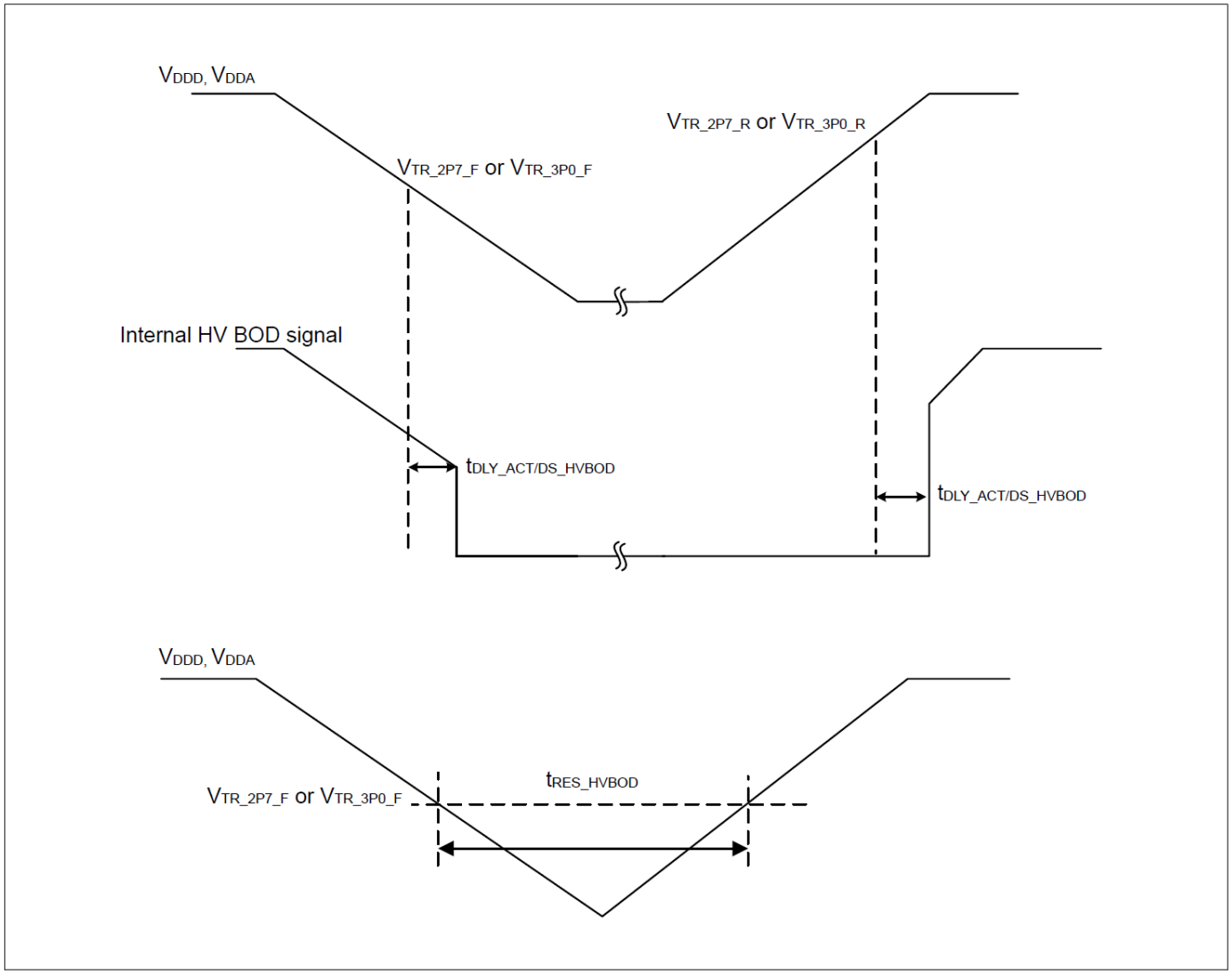
VDDD, VDDA
VTR_2P7_R or VTR_3P0_R
VTR_2P7_F or VTR_3P0_F
Internal HV BOD signal
tDLY_ACT/DS_HVBOD
tDLY_ACT/DS_HVBOD
VDDD, VDDA
tRES_HVBOD
VTR_2P7_F or VTR_3P0_F

图 31　　高压 BOD 规格

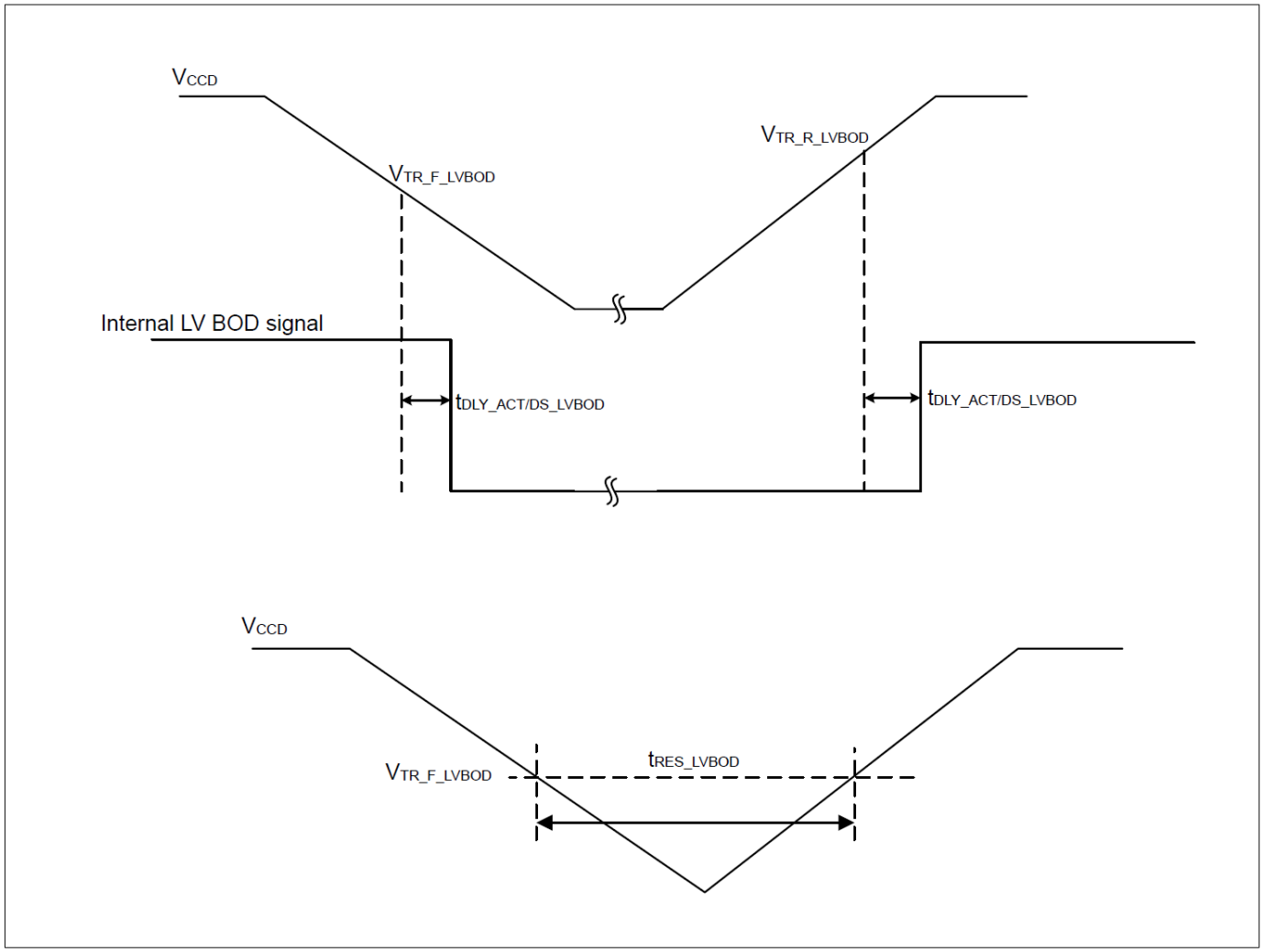
VCCD
VTR_F_LVBOD
VTR_R_LVBOD
Internal LV BOD signal
tDLY_ACT/DS_LVBOD
tDLY_ACT/DS_LVBOD
VCCD
VTR_F_LVBOD
tRES_LVBOD

图 32　　低压 BOD 规格

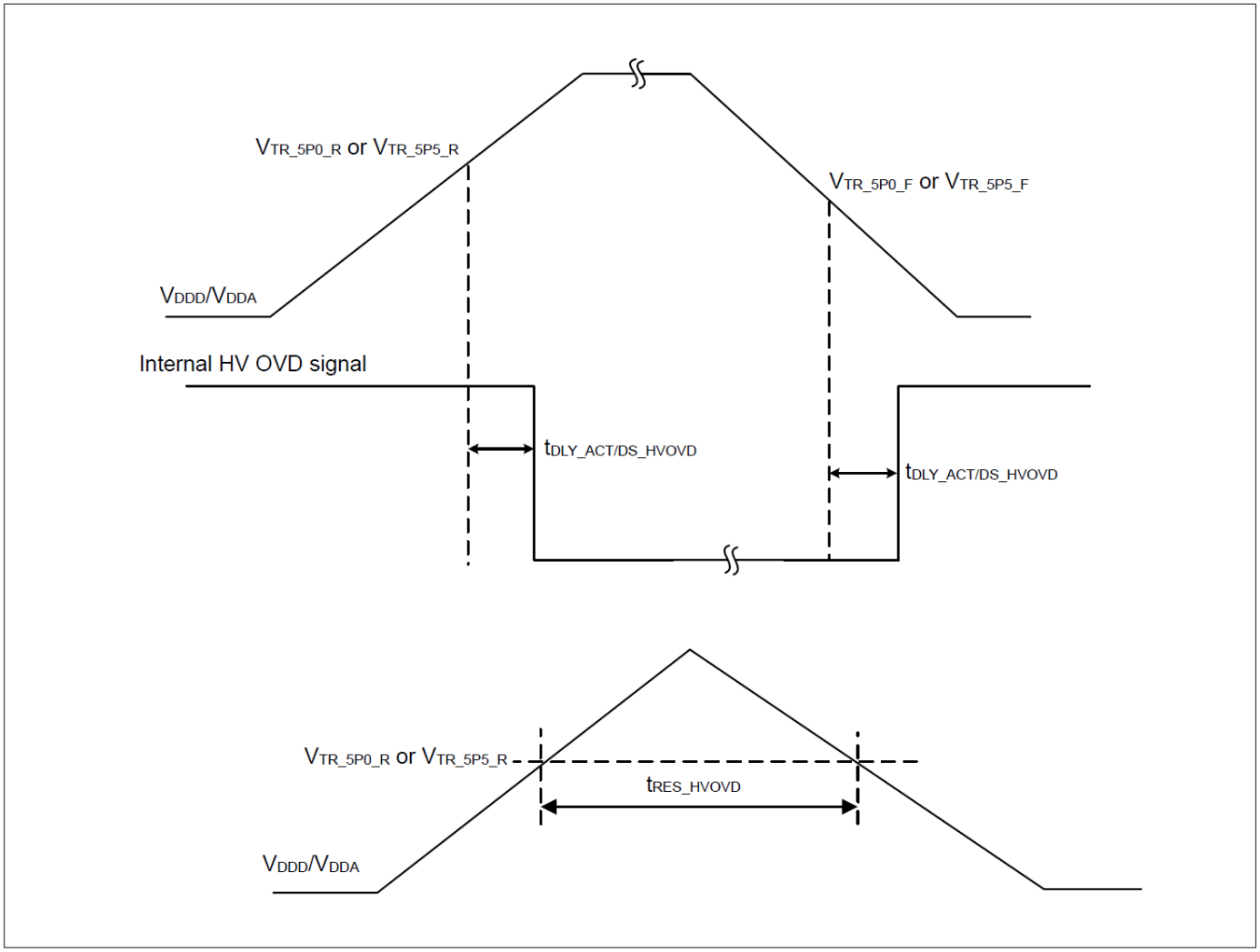
VTR_5P0_R or VTR_5P5_R
VTR_5P0_F or VTR_5P5_F
VDDD/VDDA
Internal HV OVD signal
tDLY_ACT/DS_HVOVD
tDLY_ACT/DS_HVOVD
VTR_5P0_R or VTR_5P5_R
tRES_HVOVD
VDDD/VDDA

图 33　　高压 OVD 规格

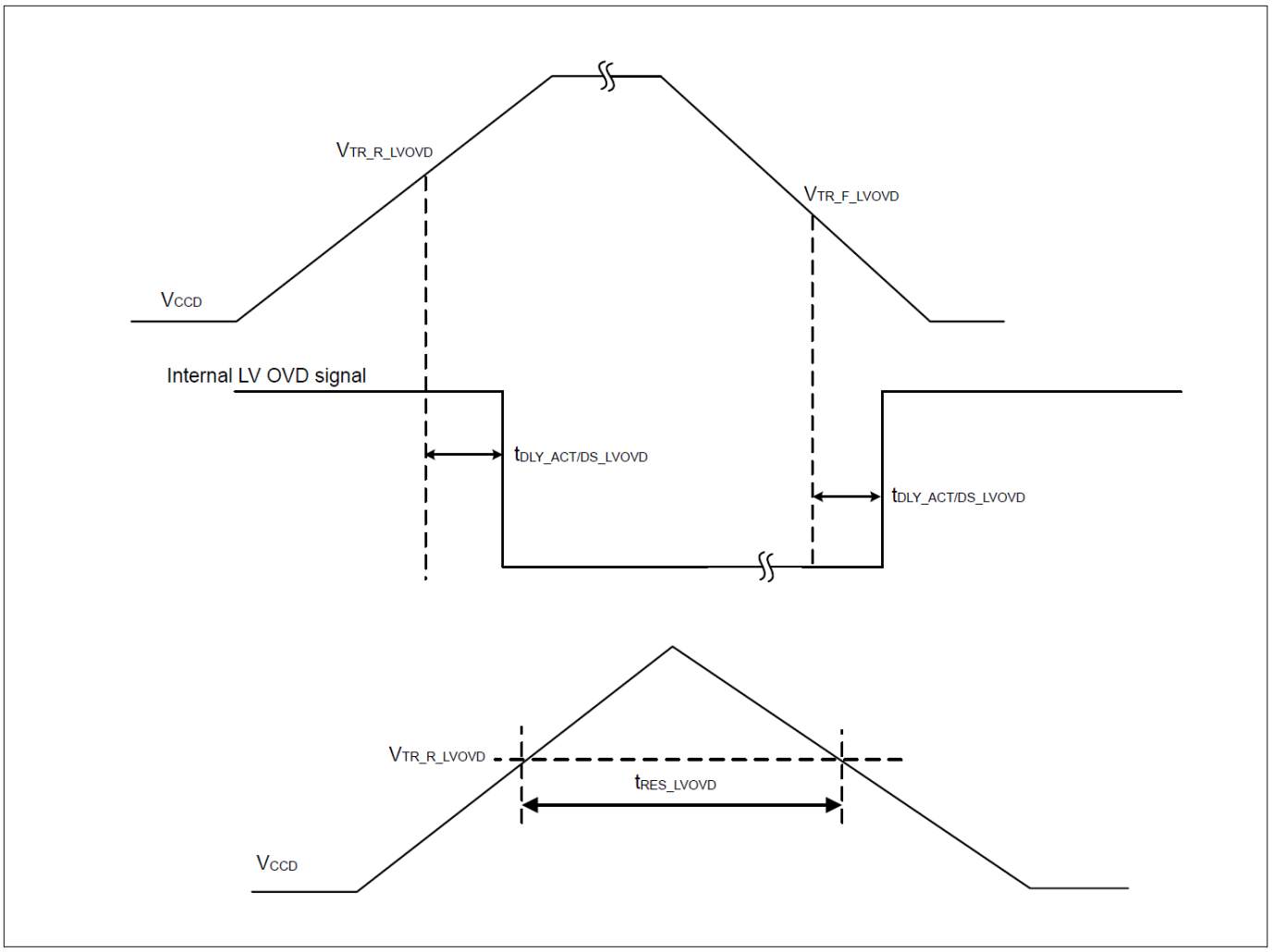
VTR_R_LVOVD
VTR_F_LVOVD
VCCD
Internal LV OVD signal
tDLY_ACT/DS_LVOVD
tDLY_ACT/DS_LVOVD
VTR_R_LVOVD
tRES_LVOVD
VCCD

图 34　　低压 OVD 规格

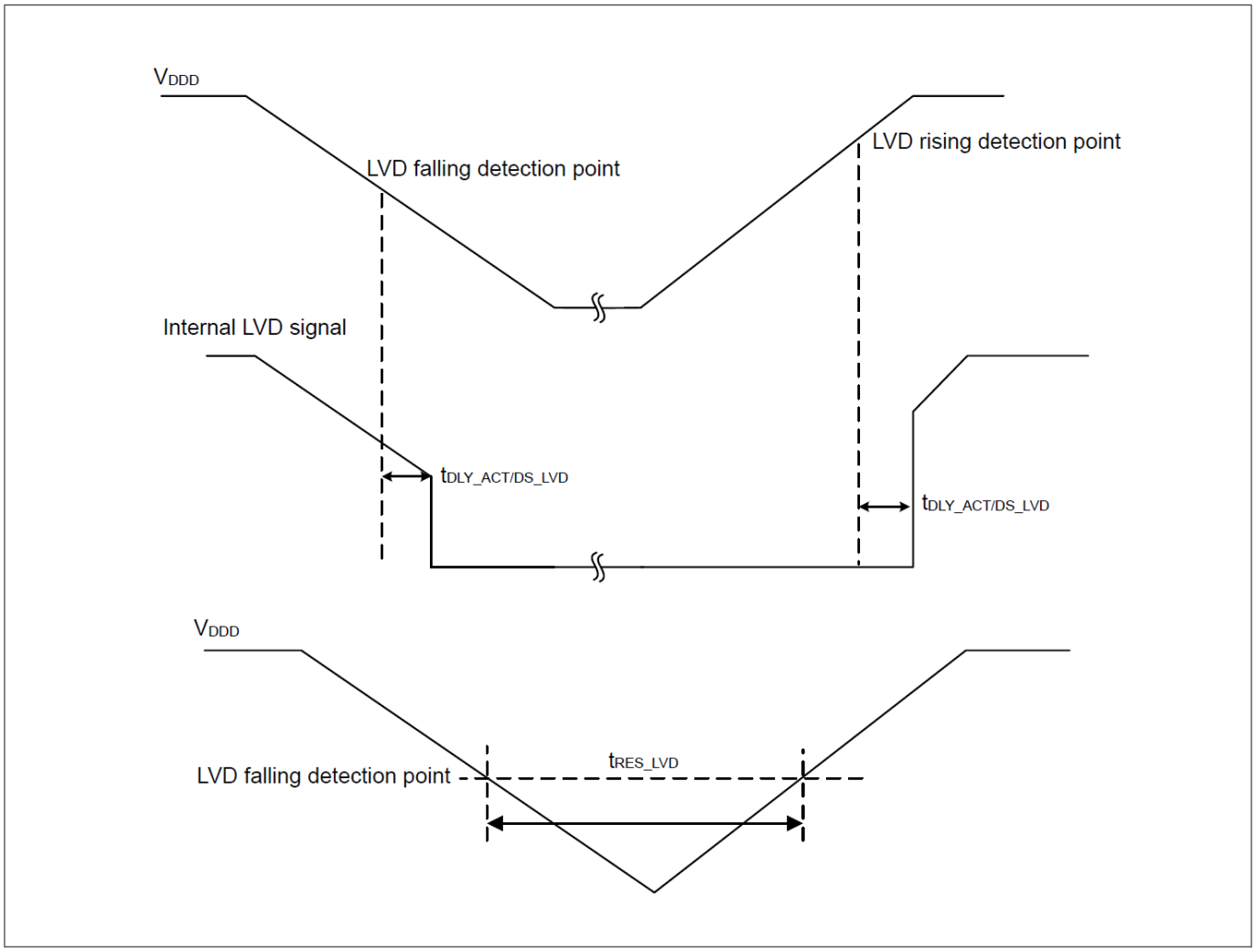

图 35 LVD规格

27.10.1 SWD、JTAG 和跟踪规格

表 45 SWD 接口规范 [条件：drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID300	f_{SWDCLK}	SWD clock input frequency	–	–	10	MHz	2.7 V ≤ V_{DDD} ≤ 5.5 V
SID301	t_{SWDI_SETUP}	SWDI setup time	0.25 × T	–	–	ns	T = 1 / f_{SWDCLK}
SID302	t_{SWDI_HOLD}	SWDI hold time	0.25 × T	–	–	ns	T = 1 / f_{SWDCLK}
SID303	t_{SWDO_VALID}	SWDO valid time	–	–	0.5 × T	ns	T = 1 / f_{SWDCLK}
SID304	t_{SWDO_HOLD}	SWDO hold time	1	–	–	ns	T = 1 / f_{SWDCLK}

表 46　　JTAG AC 规范 [条件： drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID620	t_{JCKH}	TCK HIGH time	30	–	–	ns	30-pF load
SID621	t_{JCKL}	TCK LOW time	30	–	–	ns	30-pF load
SID622	t_{JCP}	TCK clock period	66.7	–	–	ns	30-pF load
SID623	t_{JSU}	TDI/TMS setup time	12	–	–	ns	30-pF load
SID624	t_{JH}	TDI/TMS hold time	12	–	–	ns	30-pF load
SID625	t_{JZX}	TDO High-Z to active	–	–	30	ns	30-pF load
SID626	t_{JXZ}	TDO active to High-Z	–	–	30	ns	30-pF load
SID627	t_{JCO}	TDO clock to output	–	–	30	ns	30-pF load

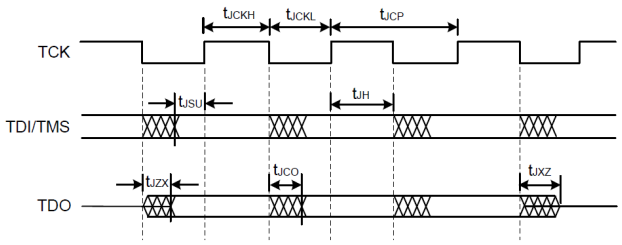

图 36　　JTAG 规格

图 47　　跟踪规格 [条件： drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1412A	C_{TRACE}	Trace capacitive load	–	–	30	pF	
SID1412	t_{TRACE_CYC}	Trace clock period	40	–	–	ns	Trace clock cycle time for 25 MHz
SID1413	t_{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width
SID1414	t_{TRACE_CLKH}	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width
SID1415A	t_{TRACE_SETUP}	Trace data setup time	3	–	–	ns	Trace data setup time
SID1416A	t_{TRACE_HOLD}	Trace data hold time	2	–	–	ns	Trace data hold time

27.11　　时钟规格

除非另有说明， 所有规格均适用于–40 °C ≤ T_A ≤ 125 °C 和 2.7 V 至 5.5 V。

对内核时钟频率依赖性的基本要求是，Cortex®-M0+ 磁芯的运行频率应与 Cortex®-M4F 磁芯的时钟频率相差一个整数分频器。示例组合列于表 48 中。

表 48　　时钟要求

Core Cortex®-M4F clock (MHz)	Core Cortex®-CM0+ clock (MHz)
160	80
120	60
100	100
80	80

表 49　　根时钟和中间时钟[1)]

Clock	Max permitted clock frequency (MHz)[2)]	Source	Maximum permitted clock frequency setting (MHz)[2)]		Description
			PLL/FLL Clock source: ECO[3)]	PLL/FLL Clock source: IMO[4)]	
CLK_HF0	160	PLL200#0	160	155	Root clock for CPUSS, PERI
		FLL	100	96	
	100	PLL200#0	100	98	
		FLL	100	96	
CLK_HF1	100	PLL200#0	100	98	Event generator (CLK_REF), Clock output on EXT_CLK pins (when used as output)
		FLL	100	96	
CLK_HF2	2	ILO	nA	nA	CSV
clk_fast	160	PLL200#0	160	155	Generated by dividing CLK_HF0, intermediate clock for CM4
		FLL	100	96	
	160	PLL200#0	100	98	
		FLL	100	96	
CLK_SLOW	100	PLL200#0	100	98	Generated by clock gating CLK_PERI, intermediate clock for CM0+, Crypto, P-DMA, M-DMA
		FLL	100	96	
CLK_PERI	100	PLL200#0	100	98	Generated by clock gating CLK_HF0, intermediate clock for LIN, SCB, PASS, CAN, TCPWM, CXPI, IOSS, CPU trace
		FLL	100	96	

1) 未列出的中间时钟具有与其父时钟相同的限制。
2) 相应时钟源（PLL/FLL + 分频器）之后的最大时钟频率。所有内部公差和影响都包含在这些频率内。
3) 对于 ECO：设计可容忍外部时钟源高达 ±150 ppm 的不确定度。

4) IMO操作频率公差包括在内。当不使用深度睡眠模式时，时钟源 IMO 情况下的最大允许时钟频率设置等于时钟源 ECO 情况下的最大允许时钟频率设置。

表 50 IMO AC 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID310A	$f_{IMOTOLA}$	IMO operating frequency	7.68	8	8.32	MHz	
SID311	$t_{STARTIMO}$	IMO startup time	–	–	7.5	µs	Startup time to 90% of final frequency
SID312	I_{IMO_ACT}	IMO current	–	13.5	22	µA	Guaranteed by design

表 51 ILO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID320	$f_{ILOTRIM}$	ILO operating frequency	31.1296	32.768	34.4064	KHz	
SID321	$t_{STARTILO}$	ILO startup time	–	8	12	µs	Startup time to 90% of final frequency
SID323	I_{ILO}	ILO Current	–	500	2800	nA	Guaranteed by design

表 52 ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID330	f_{ECO}	Crystal frequency range	3.988	–	33.34	MHz	
SID332	R_{FDBK}	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100 kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design
SID333	I_{ECO3}	ECO current at T_J = 150 °C	–	–	2000	µA	Maximum operation current with a 33-MHz crystal, max 18-pF load
SID334	t_{START_4M}	4-MHz ECO startup time[1)]	–	–	10	ms	Time from set CLK_ECO_CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams)

（表格续下页……）

27 Electrical specifications

表 52 (续) ECO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID335	t_{START_33M}	33-MHz ECO startup time[2)]	–	–	1	ms	Time from set CLK_ECO_CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams)

1) 主要看外部晶振。

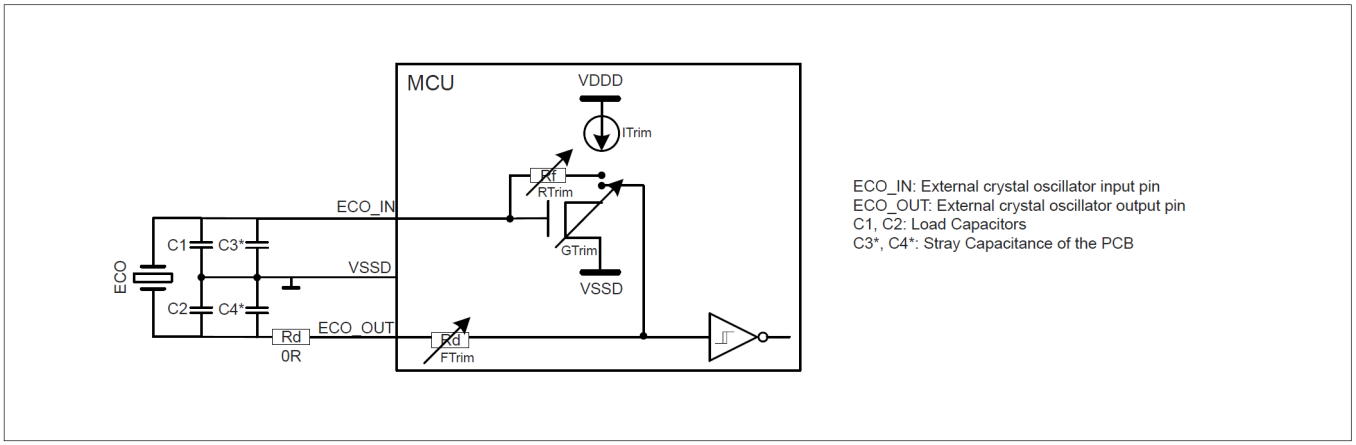

图 37 ECOO 连接方案 16)

表 53 PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID340	PLL_LOCK	Time to achieve PLL lock	–	–	35	µs	
SID341	f_{PLL_OUT}	Output frequency from PLL block	11	–	160	MHz	
SID342	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns f_{PLL_VCO}: 320 MHz f_{PLL_OUT}: 40 MHz to 160 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID343	PLL_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns f_{PLL_VCO}: 320 MHz f_{PLL_OUT}: 40 MHz to 160 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO

（表格续下页.....）

16 有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-19314，TRAVEO™ T2G Automotive MCU body controller entry architecture technical reference manual）。在启用 ECO 之前，应根据用户指南 "Setting ECO parameters, TRAVEO™ T2G family" (文档编号 002-30194）以及晶振供应商的晶振匹配测试，使用正确的设置来配置 TRIM 寄存器（ATRIM、WDTRIM、FTRIM、GTRIM 和 RTRIM）。

表 53 （续） PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID344	PLL_LJIT3	Long term jitter	–0.5	–	0.5	ns	For 1000 ns f_{PLL_VCO}: 320 MHz f_{PLL_OUT}: 40 MHz to 160 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID345A	PLL_LJIT5	Long term jitter	–0.75	–	0.75	ns	For 10000 ns f_{PLL_VCO}: 320 MHz f_{PLL_OUT}: 40 MHz to 160 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID346	f_{PLL_IN}	PLL input frequency	3.988	–	33.34	MHz	
SID347	I_{PLL_160M1}	PLL operating current (f_{OUT} = 160 MHz)	–	740	1110	µA	f_{IN} = 4 MHz, f_{PFD} = 4 MHz, f_{VCO} = 320 MHz, f_{OUT} = 160 MHz
SID347A	I_{PLL_160M2}	PLL operating current (f_{OUT} = 160 MHz)	–	750	1125	µA	f_{IN} = 8 MHz, f_{PFD} = 8 MHz, f_{VCO} = 320 MHz, f_{OUT} = 160 MHz
SID347B	I_{PLL_160M3}	PLL operating current (f_{OUT} = 160 MHz)	–	750	1125	µA	f_{IN} = 16 MHz, f_{PFD} = 8 MHz, f_{VCO} = 320 MHz, f_{OUT} = 160 MHz
SID339	I_{PLL_100M1}	PLL operating current (f_{OUT} = 100 MHz)	–	520	780	µA	f_{IN} = 4 MHz, f_{PFD} = 4 MHz, f_{VCO} = 200 MHz, f_{OUT} = 100 MHz
SID339A	I_{PLL_100M2}	PLL operating current (f_{OUT} = 100 MHz)	–	530	795	µA	f_{IN} = 8 MHz, f_{PFD} = 8 MHz, f_{VCO} = 200 MHz, f_{OUT} = 100 MHz
SID339B	I_{PLL_100M3}	PLL operating current (f_{OUT} = 100 MHz)	–	530	795	µA	f_{IN} = 16 MHz, f_{PFD} = 8 MHz, f_{VCO} = 200 MHz, f_{OUT} = 100 MHz

（表格续下页……）

表 53 （续） PLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID348	I_{PLL_80M1}	PLL operating current (f_{OUT} = 80 MHz)	–	520	780	µA	f_{IN} = 4 MHz, f_{PFD} = 4 MHz, f_{VCO} = 240 MHz, f_{OUT} = 80 MHz
SID348A	I_{PLL_80M2}	PLL operating current (f_{OUT} = 80 MHz)	–	530	795	µA	f_{IN} = 8 MHz, f_{PFD} = 8 MHz, f_{VCO} = 240 MHz, f_{OUT} = 80 MHz
SID348B	I_{PLL_80M3}	PLL operating current (f_{OUT} = 80 MHz)	–	530	795	µA	f_{IN} = 16 MHz, f_{PFD} = 8 MHz, f_{VCO} = 240 MHz, f_{OUT} = 80 MHz
SID348C	f_{PLL_VCO}	VCO frequency	170	–	400	MHz	
SID349C	f_{PLL_PFD}	PFD frequency	3.988	–	8	MHz	

表 54 FLL 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	–	–	5	µs	Wakeup with < 10 °C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value
SID351	f_{FLL_OUT}	Output frequency from FLL block	24	–	100	MHz	Output range of FLL divided-by-2 output
SID352	FLL_CJIT	FLL frequency accuracy	–1	–	1	%	This is added to the error of the source
SID353	f_{FLL_IN}	Input frequency	0.25	–	80	MHz	
SID354	I_{FLL}	FLL operating current	–	250	360	µA	Reference clock: IMO, CCO frequency: 200 MHz, FLL frequency: 100 MHz, guaranteed by design

表 55　　WCO 规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	f_{WCO}	Watch Crystal frequency	–	32.768	–	KHz	Maximum drive level: 0.5 µW
SID361	WCO_DC	WCO duty cycle	10	–	90	%	
SID362	t_{START_WCO}	WCO start-up time[1)]	–	–	1000	ms	For Grade-S devices Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams)
SID362E	t_{START_WCOE}	WCO start-up time[1)]	–	–	1400	ms	For Grade-E devices Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams)
SID363	I_{WCO}	WCO current	–	1.4	–	µA	

1)　主要看外部晶振。

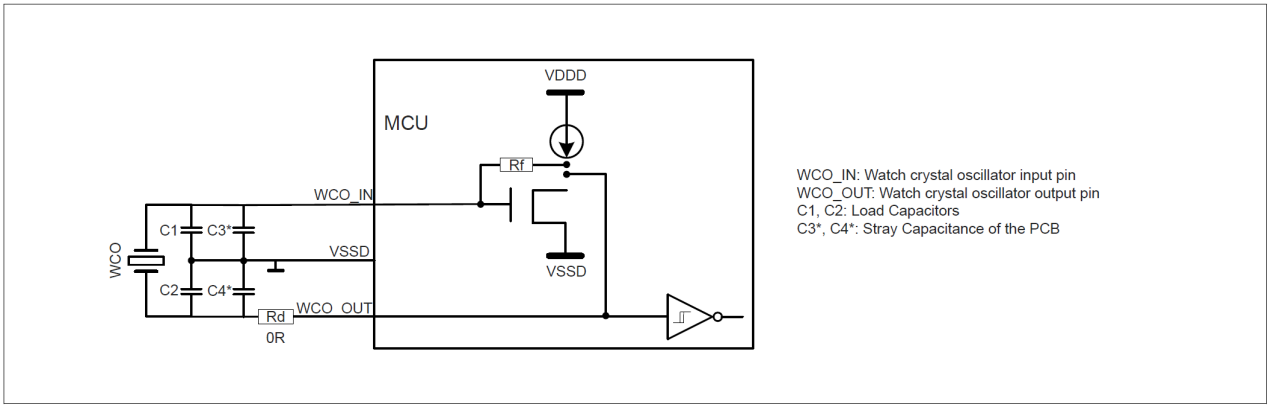

图 38　　WCO 连接方案

注意:　有关晶振要求的更多信息，请参阅特定系列的架构 TRM（002-19314，TRAVEO™ T2G Automotive MCU body controller entry architecture technical reference manual）。

表 56　　外部时钟输入规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f_{EXT}	External clock input frequency	0.25	–	80	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	External clock duty cycle	45	–	55	%	

28 时钟时序图

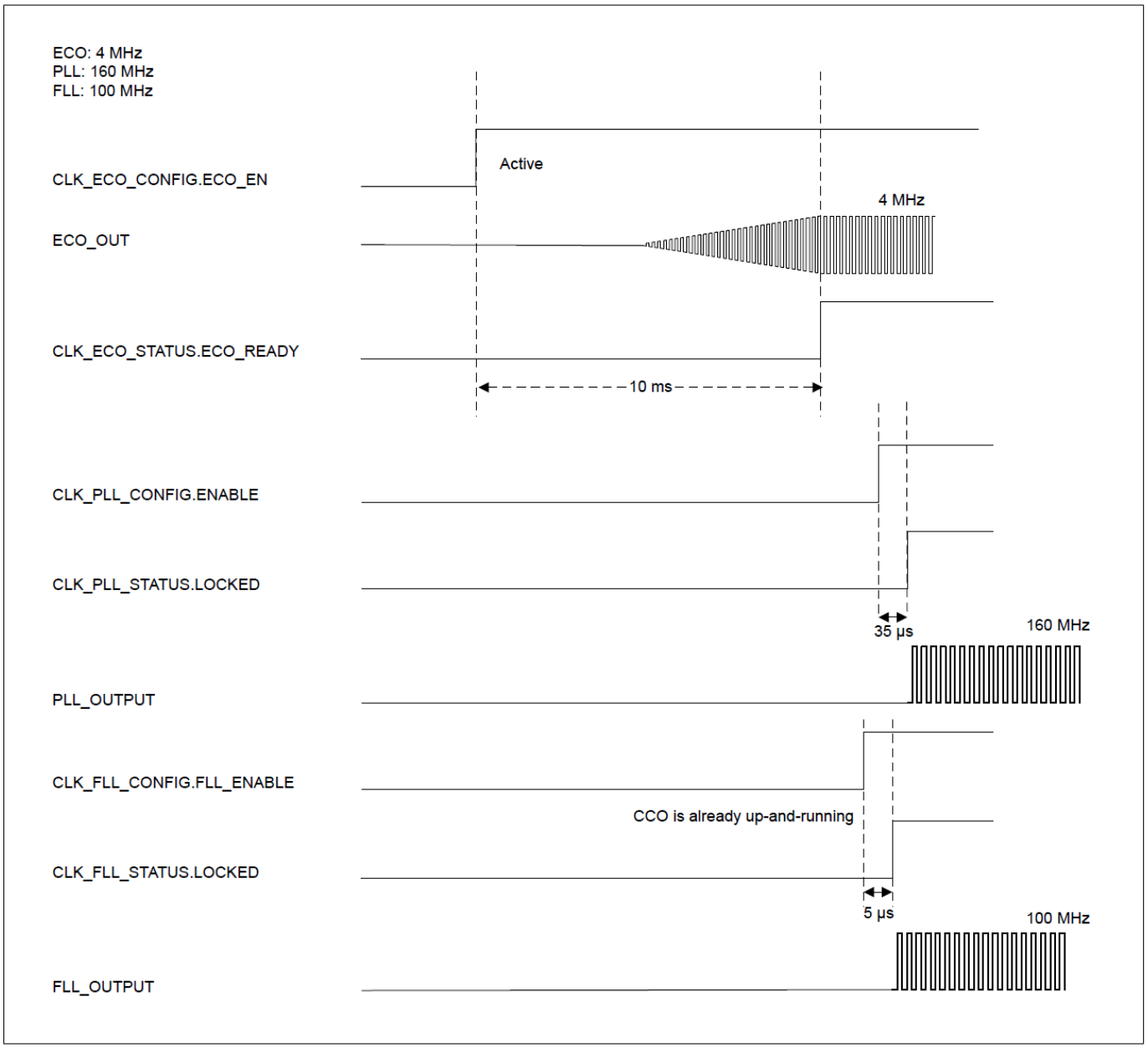

图 39 ECO 至 PLL 或 FLL 图

28 Clock timing diagrams

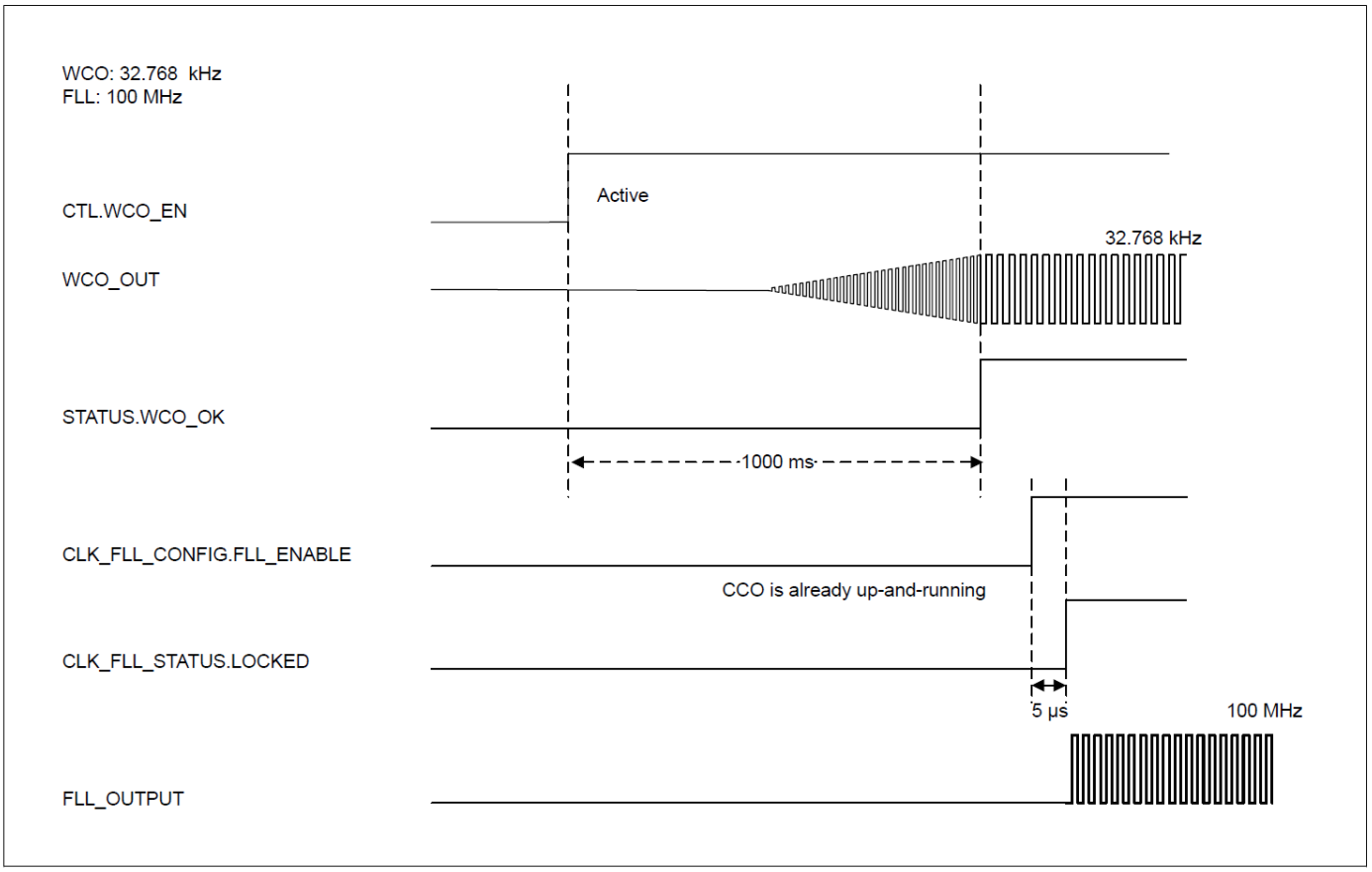

图 40 WCO 至 FLL 图

表 57 MCWDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID410	t_{MCWDT1}	Minimum MCWDT timeout	58.12	–	–	µs	When using the ILO (32.768 kHz + 5%) and 16-bit MCWDT counter Guaranteed by design
SID411	t_{MCWDT2}	Maximum MCWDT timeout	–	–	2.11	s	When using the ILO (32.768 kHz – 5%) and 16-bit MCWDT counter Guaranteed by design

表 58 WDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID412	t_{WDT1}	Minimum WDT timeout	58.12	–	–	µs	When using the ILO (32.768 kHz + 5%) and 32-bit WDT counter Guaranteed by design

（表格续下页……）

表 58 （续）WDT 超时规格

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID413	t_{WDT2}	Maximum WDT timeout	–	–	38.33	h	When using the ILO (32.768 kHz – 5%) and 32-bit WDT counter Guaranteed by design
SID414	t_{WDT3}	Default WDT timeout	–	1000	–	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design

29 订购信息

CYT2BL 微控制器料号和功能列于表 59 中。Arm® TAP JTAG ID 为 0x6BA0 0477。

表 59 CYT2BL 订购信息

Device code	Ordering code[1]	Package	Code-flash(KB)	Work-flash(KB)	RAM (KB)	ADC channels	SCB channels	LIN channels	CAN FD channels	CXPI channels	eSHE/ HSM	AUTO SAR package	Temperature grade	JTAG ID CODE
CYT2BL3BAS[2]	CYT2BL3BAAQ0AZSGS	64-LQFP	4160[3]	128[4]	512	27	7	7	5	2	eSHE	No	S[5]	0x1EA01069[6]
CYT2BL3BAE[2]	CYT2BL3BAAQ0AZEGS	64-LQFP	4160	128	512	27	7	7	5	2	eSHE	No	E[7]	0x1EA01069
CYT2BL3CAS	CYT2BL3CAAQ0AZSGS	64-LQFP	4160	128	512	27	7	7	5	2	HSM	No	S	0x1EA02069
CYT2BL3CAE	CYT2BL3CAAQ0AZEGS	64-LQFP	4160	128	512	27	7	7	5	2	HSM	No	E	0x1EA02069
CYT2BL3CXE	CYT2BL3CXAQ0AZEGS	64-LQFP	4160	128	512	27	7	7	5	2	HSM	Yes	E	0x1EA02069
CYT2BL4BAS[2]	CYT2BL4BAAQ0AZSGS	80-LQFP	4160	128	512	34	8	9	7	3	eSHE	No	S	0x1EA03069
CYT2BL4BAE[2]	CYT2BL4BAAQ0AZEGS	80-LQFP	4160	128	512	34	8	9	7	3	eSHE	No	E	0x1EA03069
CYT2BL4CAS	CYT2BL4CAAQ0AZSGS	80-LQFP	4160	128	512	34	8	9	7	3	HSM	No	S	0x1EA04069
CYT2BL4CAE	CYT2BL4CAAQ0AZEGS	80-LQFP	4160	128	512	34	8	9	7	3	HSM	No	E	0x1EA04069
CYT2BL4CXE	CYT2BL4CXAQ0AZEGS	80-LQFP	4160	128	512	34	8	9	7	3	HSM	Yes	E	0x1EA04069
CYT2BL5BAS[2]	CYT2BL5BAAQ0AZSGS	100-LQFP	4160	128	512	39	8	9	8	4	eSHE	No	S	0x1EA05069
CYT2BL5BAE[2]	CYT2BL5BAAQ0AZEGS	100-LQFP	4160	128	512	39	8	9	8	4	eSHE	No	E	0x1EA05069

（表格续下页……）

表 59 （续）CYT2BL 订购信息

Device code	Ordering code[1)]	Package	Code-flash(KB)	Work-flash(KB)	RAM (KB)	ADC channels	SCB channels	LIN channels	CAN FD channels	CXPI channels	eSHE/ HSM	AUTO SAR package	Temperature grade	JTAG ID CODE
CYT2BL5CAS	CYT2BL5CAAQ0AZSGS	100-LQFP	4160	128	512	39	8	9	8	4	HSM	No	S	0x1EA06069
CYT2BL5CAE	CYT2BL5CAAQ0AZEGS	100-LQFP	4160	128	512	39	8	9	8	4	HSM	No	E	0x1EA06069
CYT2BL5CXE	CYT2BL5CXAQ0AZEGS	100-LQFP	4160	128	512	39	8	9	8	4	HSM	Yes	E	0x1EA06069
CYT2BL7BAS[2)]	CYT2BL7BAAQ0AZSGS	144-LQFP	4160	128	512	54	8	12	8	4	eSHE	No	S	0x1EA07069
CYT2BL7BAE[2)]	CYT2BL7BAAQ0AZEGS	144-LQFP	4160	128	512	54	8	12	8	4	eSHE	No	E	0x1EA07069
CYT2BL7CAS	CYT2BL7CAAQ0AZSGS	144-LQFP	4160	128	512	54	8	12	8	4	HSM	No	S	0x1EA08069
CYT2BL7CAE	CYT2BL7CAAQ0AZEGS	144-LQFP	4160	128	512	54	8	12	8	4	HSM	No	E	0x1EA08069
CYT2BL7CXE	CYT2BL7CXAQ0AZEGS	144-LQFP	4160	128	512	54	8	12	8	4	HSM	Yes	E	0x1EA08069
CYT2BL8BAS[2)]	CYT2BL8BAAQ1AZSGS	176-LQFP	4160	128	512	64	8	12	8	4	eSHE	No	S	0x1EA09069
CYT2BL8BAE[2)]	CYT2BL8BAAQ1AZEGS	176-LQFP	4160	128	512	64	8	12	8	4	eSHE	No	E	0x1EA09069
CYT2BL8CAS	CYT2BL8CAAQ1AZSGS	176-LQFP	4160	128	512	64	8	12	8	4	HSM	No	S	0x1EA0A069
CYT2BL8CAE	CYT2BL8CAAQ1AZEGS	176-LQFP	4160	128	512	64	8	12	8	4	HSM	No	E	0x1EA0A069
CYT2BL8CXE	CYT2BL8CXAQ1AZEGS	176-LQFP	4160	128	512	64	8	12	8	4	HSM	Yes	E	0x1EA0A069

1) 支持的装运类型为“托盘”（默认）和“卷带包装”。 在末尾添加字符'T'，获取“卷带包装”装运类型的订购代码。

2) 不支持 3DES/SHA-1/SHA-2/SHA-3/CRC/矢量单元的不对称加密特性。

3) 代码闪存大小 4160 KB = 32 KB × 126 (大扇区) + 8 KB × 16 (小扇区)。

4) 工作闪存大小 128 KB = 2 KB × 48 (大扇区) + 128 B × 256 (小扇区)。

5) S 级温度（-40°C至105°C）。

6) JTAG ID CODE 位 12 至 27 代表器件的硅片 ID。

7) E 级温度（-40°C 至 125°C）。

29 Ordering information

29.1 料号命名规则

表 60 器件代码命名规则

Field	Description	Value	Meaning
CY	Cypress prefix, an Infineon company	CY	
T	Category	T	TRAVEO™
2	Family	2	TRAVEO™ T2G (Core M4)
B	Application	B	Body
D	Code-flash/Work-flash/SRAM quantity	L	4160 KB / 128 KB / 512 KB
P	Packages	3	64-LQFP
		4	80-LQFP
		5	100-LQFP
		7	144-LQFP
		8	176-LQFP
H	Hardware Option	B	eSHE – on, HSM – off, RSA-2048
		C	eSHE – on, HSM – on, RSA-2048
I	Marketing Option	A	No options
		X	AUTOSAR package
C	Temperature grade	S	S-grade (–40 °C to 105 °C)
		E	E-grade (–40°C to 125°C)

表 61 订购代码命名规则

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family Name	2	TRAVEO™ T2G (Core M4)
B	Application	B	Body
D	Code-flash/Work-flash/ SRAM quantity	L	4160 KB / 128 KB / 512 KB
P	Packages	3	64-LQFP
		4	80-LQFP
		5	100-LQFP
		7	144-LQFP
		8	176-LQFP
H	Hardware Option	B	eSHE – on, HSM – off, RSA-2048

（表格续下页……）

表 61 （续）订购代码命名规则

Field	Description	Value	Meaning
		C	eSHE – on, HSM – on, RSA-2048
I	Marketing Option	A	No options
		X	AUTOSAR package
R	Revision	A	First revision
F	Fab Location	Q	UMC (Fab 12i) Singapore
X	Reserved	0/1	Reserved
K	Package Code	AZ	LQFP
C	Temperature grade	S	S-grade (–40 °C to 105 °C)
		E	E-grade (–40°C to 125°C)
Q	Quality grade	ES	Engineering samples
		GS	Standard grade of automotive
S	Shipment type	Blank	Tray shipment
		T	Tape and reel shipment

30 封装

CYT2BL 包含在表 62 中列出的封装。

表 62 封装信息

Package	Dimensions	Contact/lead pitch	Coefficient of Thermal Expansion[1]	I/O Pins
176-LQFP	24 × 24 × 1.7 mm (max)	0.5 mm	a1[2] = 8.5 ppm/°C, a2[3] = 33.8 ppm/°C	152
144-LQFP	20 × 20 × 1.7 mm (max)	0.5 mm	a1[2] = 8.5 ppm/°C, a2[3] = 33.7 ppm/°C	122
100-LQFP	14 × 14 × 1.7 mm (max)	0.5 mm	a1[2] h = 8.5 ppm/°C, a2[3] = 33.6 ppm/°C	78
80-LQFP	12 × 12 × 1.7 mm (max)	0.5 mm	a1[2] = 8.5 ppm/°C, a2[3] = 33.5 ppm/°C	63
64-LQFP	10 × 10 × 1.7 mm (max)	0.5 mm	a1[2] = 8.5 ppm/°C, a2[3] = 33.2 ppm/°C	49

1) 这些数值仅为基于仿真的估计值，且每种封装类型仅基于单一物料清单组合得出。
2) a1 = 低于 T_g 的 CTE（热膨胀系数）值 （ppm/°C） （T_g 是玻璃化转变温度，为 131°C）。
3) a2 = 高于 T_g 的 CTE 值(ppm/°C).

表 63 封装特性

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	S-grade	–40	–	105	°C
T_A	Operating ambient temperature	E-grade	–40	–	125	°C
T_J	Operating junction temperature	–	–	–	150	°C
$R_{\theta JA}$	Package thermal resistance, junction to ambient θ_{JA} [1], [2]	64 LQFP	–	–	30.2	°C/Watt
		80 LQFP	–	–	29.2	°C/Watt
		100 LQFP	–	–	28.5	°C/Watt
		1444 LQFP	–	–	24.7	°C/Watt
		176 LQFP	–	–	25.8	°C/Watt
$R_{\theta JB}$	Package thermal resistance, junction to board θ_{JB}	64 LQFP	–	–	24.6	°C/Watt
		80 LQFP	–	–	23.4	°C/Watt
		100 LQFP	–	–	20.8	°C/Watt
		1444 LQFP	–	–	19.7	°C/Watt
		176 LQFP	–	–	21.2	°C/Watt
$R_{\theta JC}$	Package thermal resistance, junction to case θ_{JC}	64 LQFP	–	–	7.3	°C/Watt
		80 LQFP	–	–	6.4	°C/Watt
		100 LQFP	–	–	5.2	°C/Watt
		1444 LQFP	–	–	3.9	°C/Watt
		176 LQFP	–	–	3.8	°C/Watt

1) 电路板条件符合 JESD51-7（4层）。
2) 所示的最大值°C/Watt 适用于 T_A = 125 °C。

表 64 回流焊峰值温度、封装湿度敏感度等级 (MSL)、IPC/JEDEC J-STD-2

Package	Maximum peak temperature (°C)	Maximum time at peak temperature (seconds)	MSL
176-LQFP	260	30	3
144-LQFP	260	30	3
100-LQFP	260	30	3
80-LQFP	260	30	3
64-LQFP	260	30	3

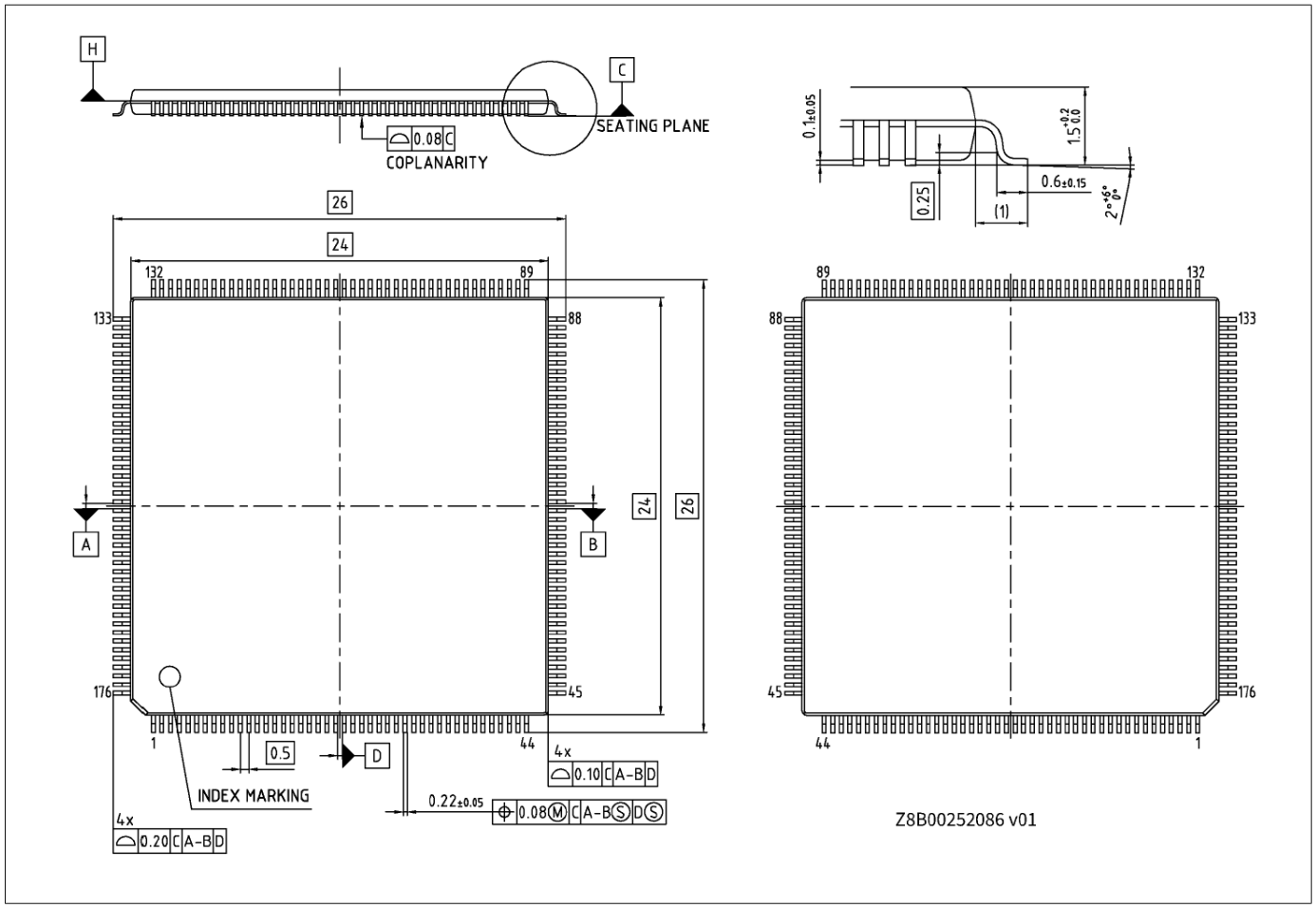

图 41 176-LQFP 封装外形 (PG-LQFP-176)

30 Packaging

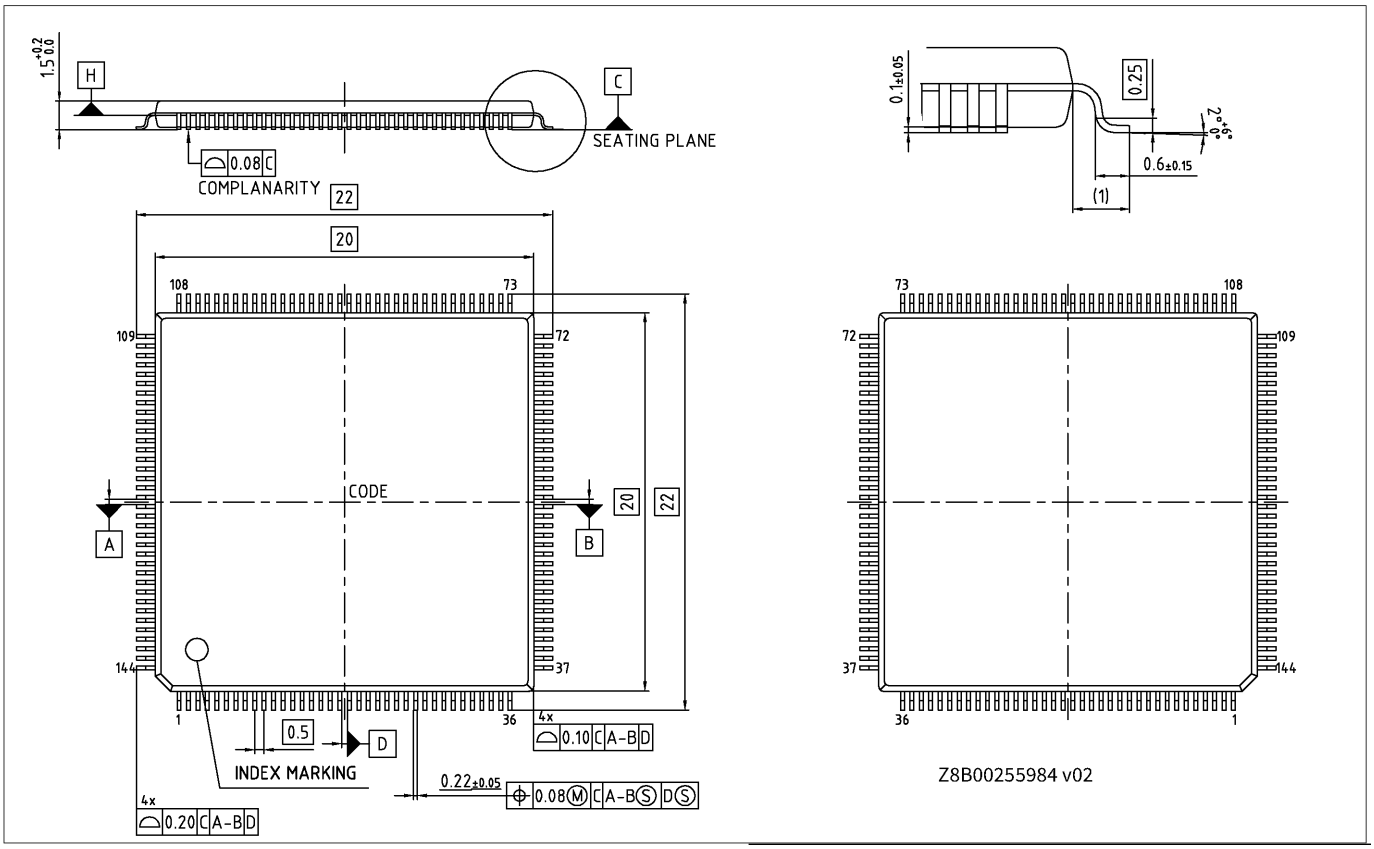

图 42 144-LQFP 封装外形 (PG-LQFP-144)

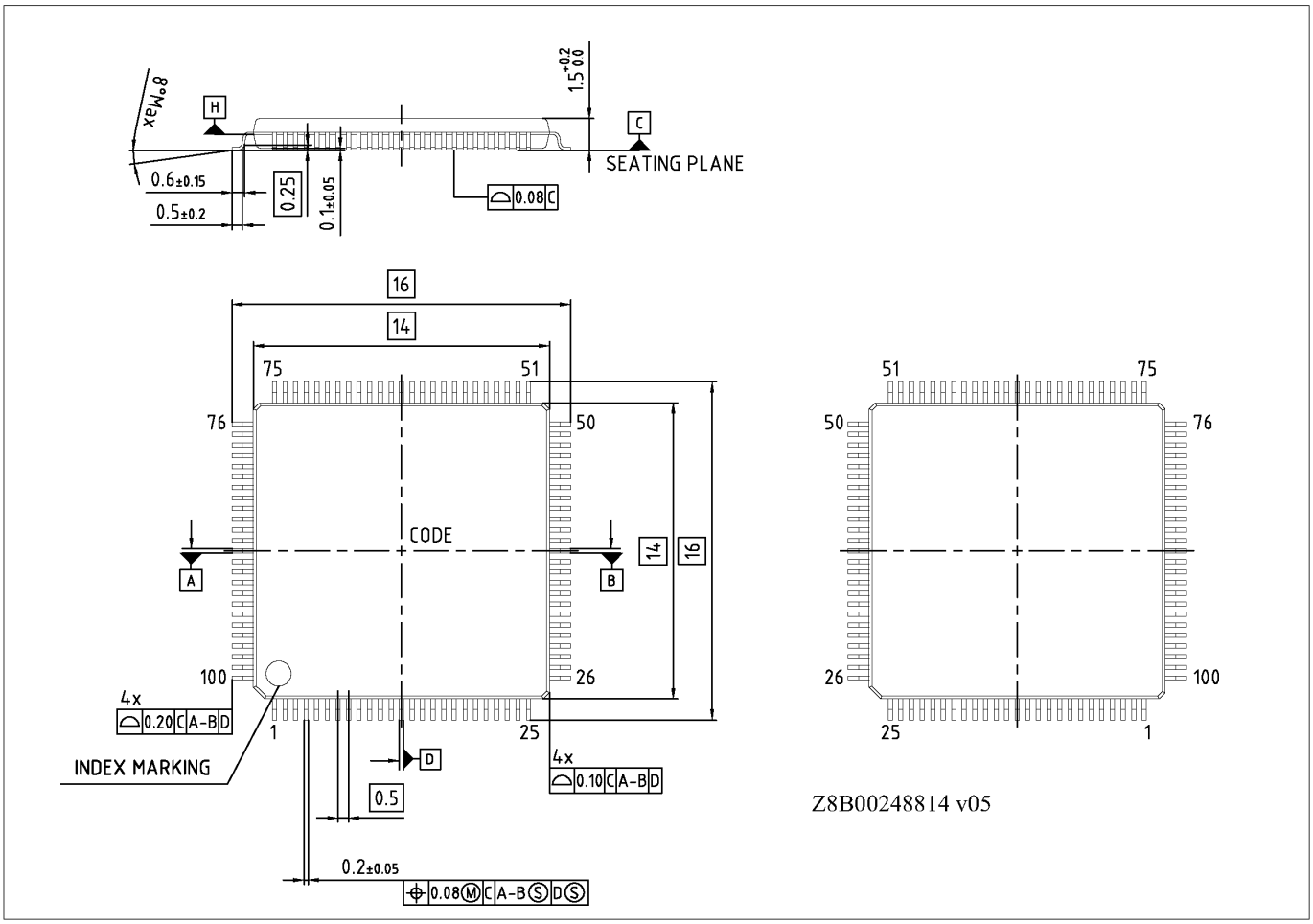

图 43 100-LQFP 封装外形 (PG-LQFP-100)

30 Packaging

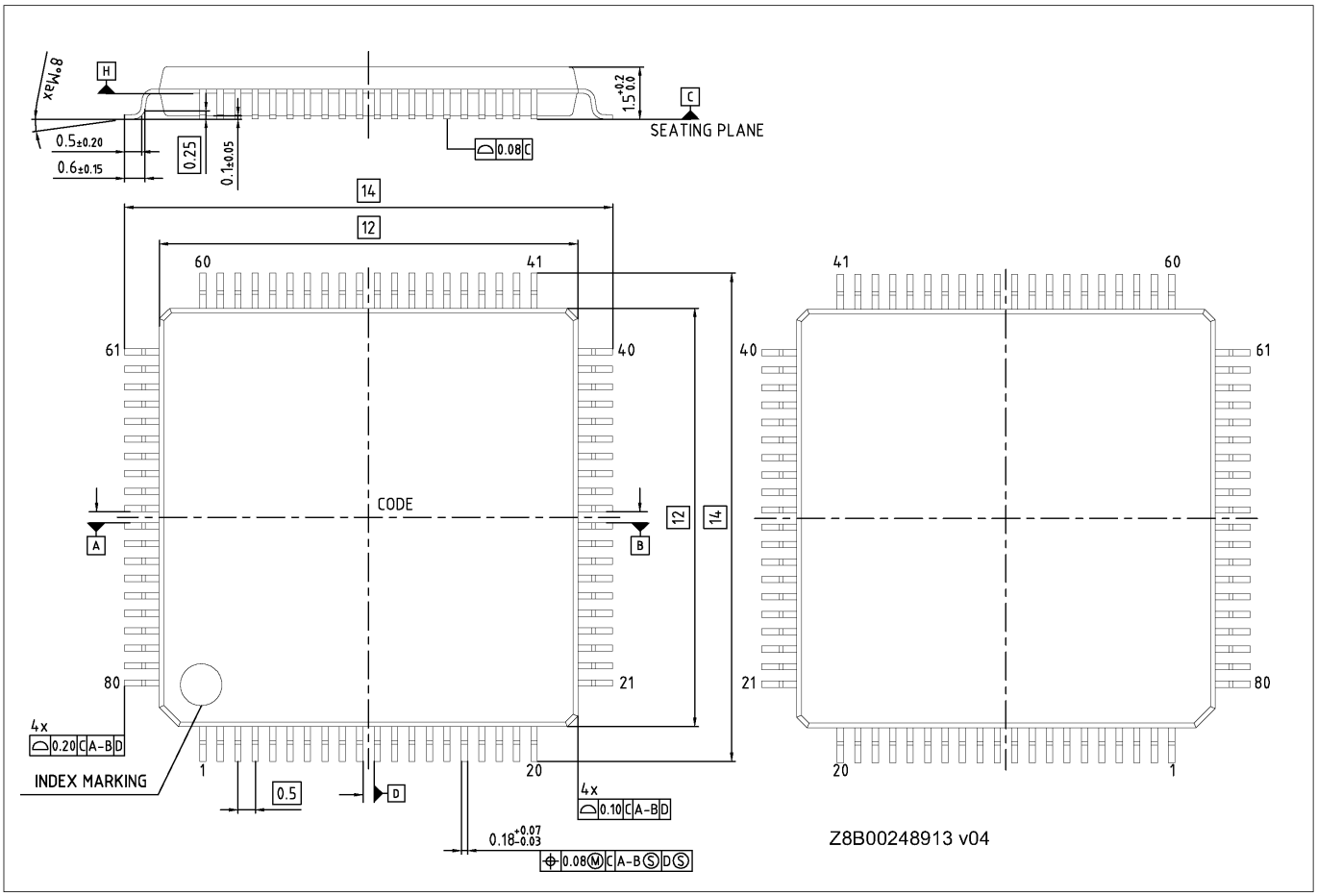

图 44　　80-LQFP 封装外形 (PG-LQFP-80)

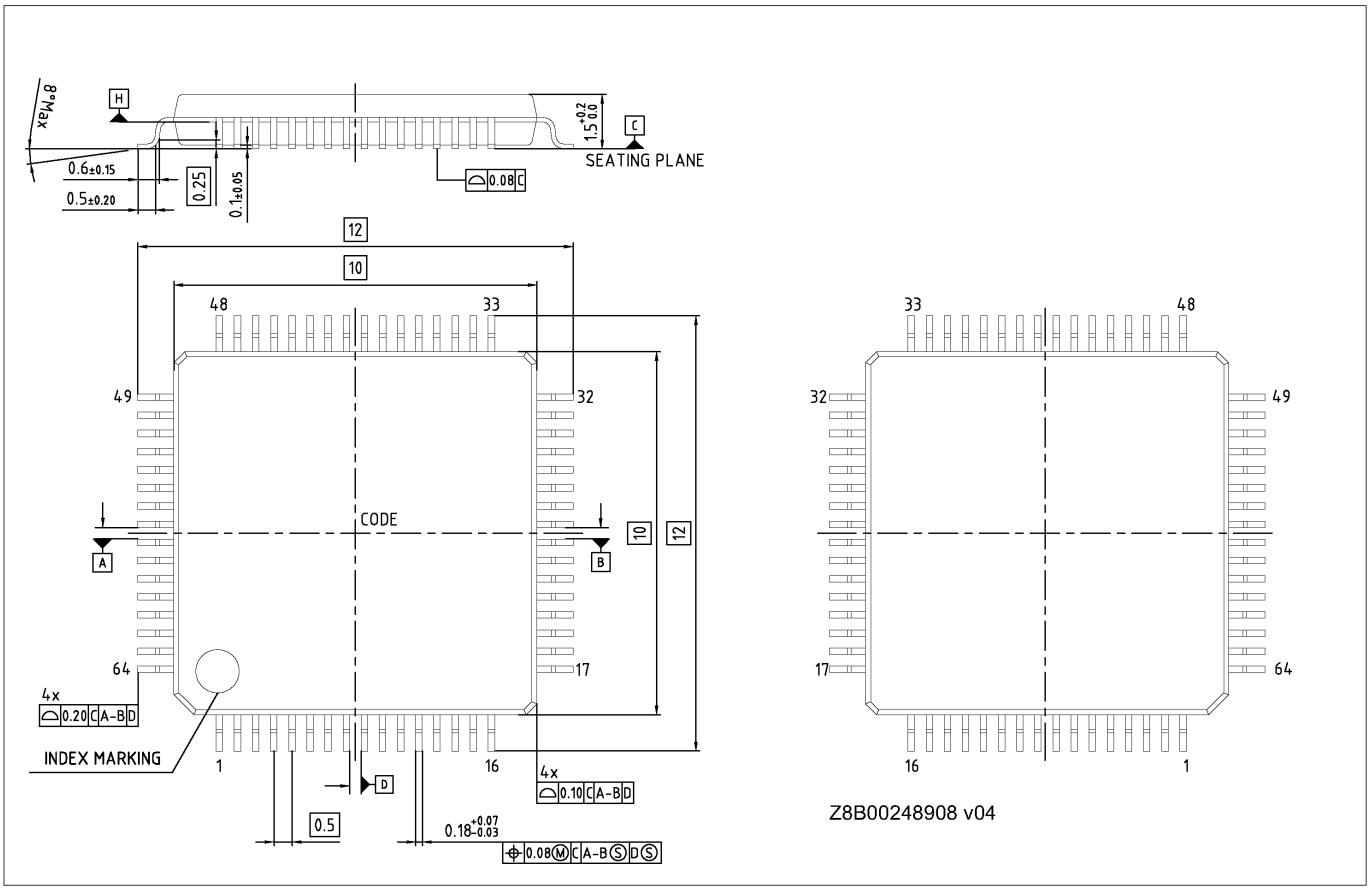

图 45　　64-LQFP 封装外形 (PG-LQFP-64)

31 附录

31.1 引导加载或生产线末端编程

- 如果满足触发条件，则在设备启动时触发
- 可以使用 CAN 或 LIN 通讯
- 引导加载程序在不同的时间帧上轮询 CAN 或 LIN 上的通讯，直到达到整体 300 秒超时
- 如果在任一通信接口上收到引导加载程序命令，则轮询停止，并且引导加载程序开始使用该接口

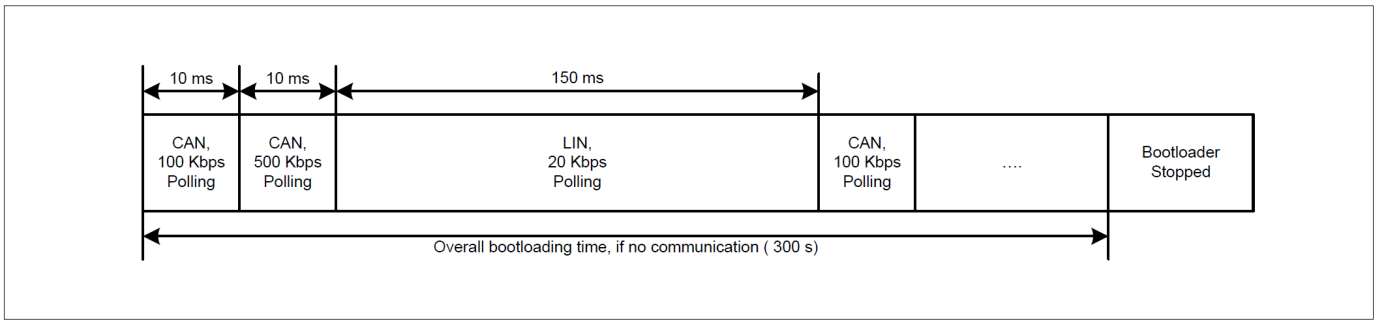

图 46 引导加载序列

表 65 CAN 接口详情

Sl. No.	CAN interface	Configuration
1	CAN Mode	Classic CAN
2	CAN Instance	CAN0, Channel#1
3	CAN Tx	P0.2 / CAN0_1_TX
4	CAN Rx	P0.3 / CAN0_1_RX
5	CAN Transceiver NSTB / EN (Low)	P23.3 (optional)
6	CAN Transceiver EN / EN (High)	P2.1 (optional)
7	CAN RX Message ID	0x1A1
8	CAN TX Message ID	0x1B1
9	Baud	100 or 500 kbps alternating

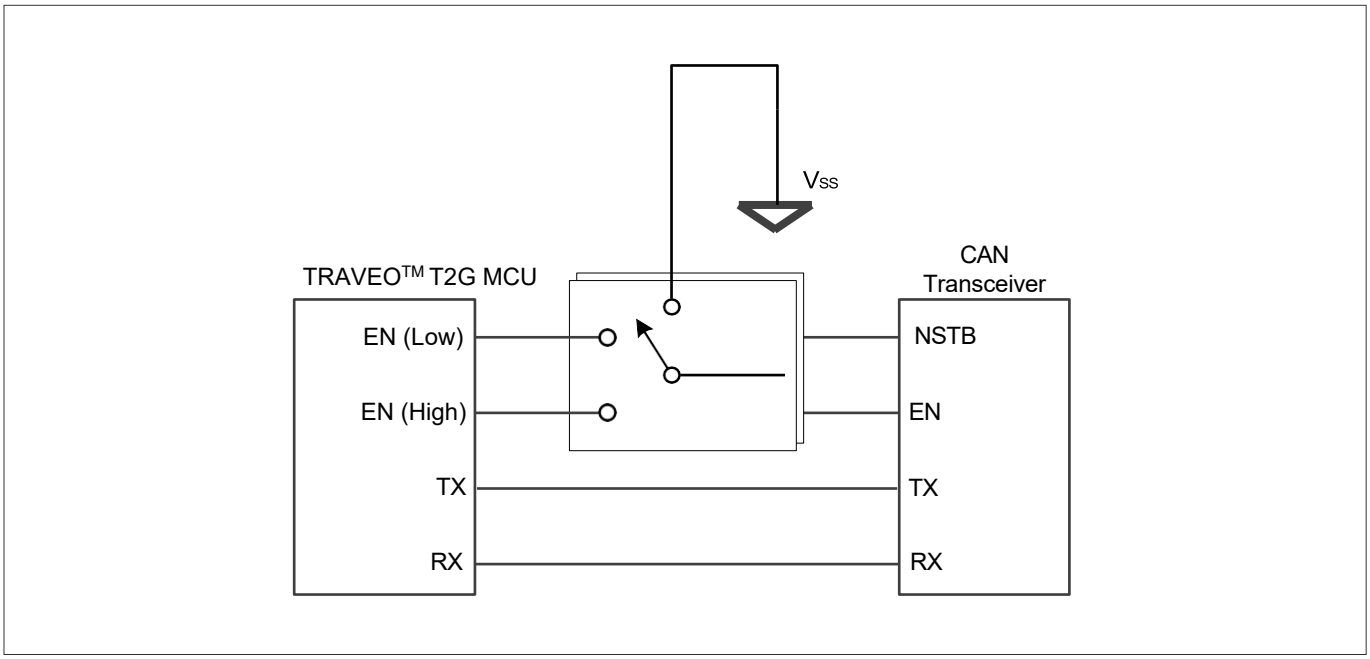

图 47 MCU 至 CAN 收发器连接

表 66 LIN 接口详情

Sl. No.	LIN interface	Configuration
1	LIN Type	LIN0, Channel#1
2	LIN Mode	Slave
3	LIN Checksum Type	Classic
4	LIN TX	P0.1 / LIN1_TX
5	LIN RX	P0.0 / LIN1_RX
6	LIN EN / EN (High)	P2.1 (optional)
7	LIN EN (Low)	P23.3 (optional)
8	LIN TX PID	0x46
9	LIN RX PID	0x45
10	Baud	20 or 115.2 kbps
11	Break Field Length	11
12	Break Delimiter Length	1 bit

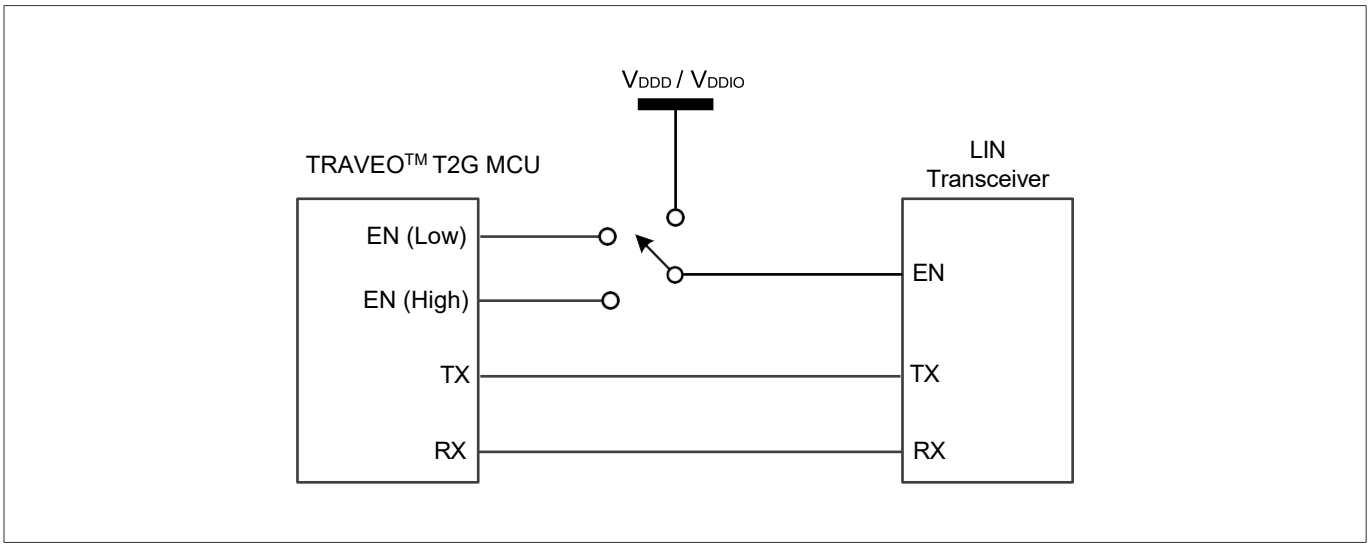

图 48 MCU 至 LIN 收发器连接

31.2 外部 IP 修订

表 67 IP 修订

Module	IP	Revision	Vendor
CAN FD	mxttcanfd	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex®-M0+-r0p1	Arm®
Arm® Cortex®-M4F	armcm4	Cortex®-M4-r0p1	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100-r3p2	Arm®

32 缩略语

表 68 本文档中使用的缩略语

Acronym	Description
A/D	Analog to Digital
ABS	Absolute
ADC	Analog to Digital converter
AES	Advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus
Arm®	Advanced RISC machine, a CPU architecture
ASIL	Automotive safety integrity level
BOD	Brown-out detection
CAN FD	Controller Area Network with Flexible Data rate
CMOS	Complementary metal-oxide-semiconductor
CPU	Central Processing Unit
CRC	Cyclic redundancy check, an error-checking protocol
CSV	Clock supervisor
CTI	Cross trigger interface
CXPI	Clock Extension Peripheral Interface
DES	Data encryption standard
DFT	Design-For-Test
DW	Datawire same as P-DMA
ECC	Error correcting code/Elliptical curve cryptography
ECO	External crystal oscillator
ETM	Embedded Trace Macrocell
EVTGEN	Event Generator
FLL	Frequency Locked Loop
FPU	Floating point unit
GHS	Green Hills tool chain with Multi IDE
GPIO	General purpose input/output
HSM	Hardware security module
I/O	Input/output
I^2C	Inter-Integrated Circuit, a communications protocol
ILO	Internal low-speed oscillator
IMO	Internal main oscillator
IOSS	Input/output sub-system

（表格续下页……）

表 68 （续）本文档中使用的缩略语

Acronym	Description
IPC	Inter-processor communication
IrDA	Infrared interface
IRQ	Interrupt request
JTAG	Joint test action group
LDO	Low drop out regulators
LIN	Local Interconnect Network, a communications protocol
LVD	Low voltage detection
OTA	Over-the-air programming
OTP	One-time programmable
OVD	Overvoltage detection
P-DMA	Peripheral-Direct Memory Access same as DW
PLL	Phase Locked Loop
POR	Power-on reset
PPU	Peripheral protection unit
PRNG	Pseudorandom number generator
PWM	Pulse-width modulation
MCU	Microcontroller Unit
MCWDT	Multi-counter watchdog timer
M-DMA	Memory-Direct Memory Access
MISO	SPI Master-in slave-out
MMIO	Memory mapped I/O
MOSI	SPI Master-out slave-in
MPU	Memory protection unit
MTB	Micro trace buffer
MUL	Multiplier
MUX	Multiplexer
NVIC	Nested vectored interrupt controller
RAM	Random access memory
RISC	Reduced-instruction-set computing
ROM	Read only memory
RSA	Rivest-Shamir-Adleman Public Key Encryption Algorithm
RTC	Real-time clock
SAR	Successive approximation register

（表格续下页……）

表 68 （续）本文档中使用的缩略语

Acronym	Description
SCB	Serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
TCPWM	Timer/Counter Pulse-width modulator
TTL	Transistor-transistor logic
TRNG	True random number generator
UART	Universal Asynchronous Transmitter Receiver
WCO	Watch crystal oscillator
WDT	Watchdog timer reset
XRES_L	External reset I/O pin

修订记录

Document revision	Date	Description of changes
**	2019-11-26	New datasheet for new device family.
*A	2019-12-12	Updated Electrical specifications.
*B	2020-04-01	Changed datasheet status to Preliminary. Updated Electrical specifications. Updated Ordering information and Packaging.
*C	2021-07-08	Updated Features list. Updated Clock system. Updated Power modes. Updated I/Os. Updated High-speed I/O matrix (HSIOM) connections and Alternate function pin assignments. Updated Triggers group inputs. Updated Faults. Updated Electrical specifications. Updated Ordering information and Packaging. Updated Appendix.
*D	2021-10-13	Updated Clock system Updated Pin assignment Updated Package pin list and alternate functions Updated Alternate function pin assignments Updated Electrical specifications Updated Errata.
*E	2022-02-16	Updated Features. Updated System resources. Updated Ordering information. Updated Errata.
*F	2022-10-07	Updated Electrical specifications. Added note in Packaging. Updated Errata.
*G	2023-07-12	Updated General description. Updated Features list. Updated Blocks and functionality. Updated Peripheral I/O map. Updated Package pin list and alternate functions. Updated Power pin assignments. Updated Pin mux descriptions. Updated Ordering information. Updated Packaging Updated Errata.
*H	2024-03-04	Updated Triggers one-to-one Updated Errata.

Revision history

Document revision	Date	Description of changes
*I	2025-06-10	Updated PLL and FLL Updated Table 38 Removed Errata Updated Figure 5, Figure 7, Figure 9, Figure 11, and Figure 13 Updated Table 63
*J	2026-03-10	Updated General description. Updated Features. Updated Features list. Updated Table 59 Updated Table 60. Updated Table 61. Updated template. Updated footnote numbers.

修订记录变更日志

Rev. *J 章节更新

Section	Change description	Current spec	New spec	Reason for change
General description	Added description	None	Infineon's TRAVEO™ T2G 32-bit Automotive MCU is a high-performance, low-power controller designed for automotive applications, compliant to ISO 26262 for functional safety and ISO 21434 for cybersecurity.	Addition
Features	Updated description	Crypto engine	ISO 21434 compliant / EVITA Full	Updated
Features	Updated description	Functional safety for ASIL-B	ISO 26262 functional safety compliant for ASIL-B	Updated
Features list	Updated description	Functional safety | ASIL-B	Functional safety | ISO 26262 ASIL-B compliant	Updated
Features list	Updated description	Security	Security - ISO 21434 compliant	Updated
26.11 Clock specifications	Updated description for Note for ECO connection scheme	16: See the family-specific Architecture TRM for more information on crystal requirements (002-19314, TRAVEO™ T2G Automotive MCU body controller entry architecture technical reference manual).	16: See the family-specific Architecture TRM for more information on crystal requirements (002-19314, TRAVEO™ T2G Automotive MCU body controller entry architecture technical reference manual). Before enabling ECO, the TRIM registers (ATRIM, WDTRIM, FTRIM, GTRIM and RTRIM) shall be configured with correct settings based on and User Guide "Setting ECO parameters, TRAVEO™ T2G family" (Doc No. 002-30194) and the crystal matching test from the crystal vendor.	Updated
27 Ordering information	Table 59 Added five new device codes, added AUTOSAR package column	None	Added five new device codes CYT2BL3CXE, CYT2BL4CXE, CYT2BL5CXE, CYT2BL7CXE, CYT2BL8CXE. Added AUTOSAR package column	Updated
27.1 Part number nomenclature	Table 60 Updated Marketing option	A | No options	A | No options X | AUTOSAR package	Updated
27.1 Part number nomenclature	Table 61 Updated Marketing option	A | No options	A | No options X | AUTOSAR package	Updated

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