CYRS1643KV18
CYRS1645KV18

144-Mbit QDR II+ SRAM Four-Word Burst Architecture with RadStop Technology

Radiation Performance

Radiation Data

- Total Dose = 200k
- Soft error rate (both Heavy Ion and proton)
  Heavy ions $\leq 1 \times 10^{-10}$ upsets/bit-day with an external SECDED EDAC Controller
- Dose rate = > 1.0 x 10^{9} rad(Si)/sec
- Dose rate survivability (rad(Si)/sec) = > 1.4 × 10^{10} rad(Si)/sec
- Dose rate latchup (rad(Si)/sec) > 3.0 × 10^{9} (125 °C)
- Latch up immunity = >120 MeV.cm2/mg (125 °C)

Prototyping Options

- Non qualified CYPT1642KV18 and CYPT1644KV18 devices with same functional and timing characteristics in a 165-ball Ceramic Column Grid Array (CCGA) package

Features

- Separate independent read and write data ports
  - Supports concurrent transactions
- 250-MHz clock for high bandwidth
- Four-word burst for reducing address bus frequency
- Double Data Rate (DDR) interfaces on both read and write ports (data transferred at 500 MHz) at 250 MHz
- Available in 2.0 clock cycle latency
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Single multiplexed address input bus latches address inputs for read and write ports
- Separate port selects for depth expansion
- Synchronous internally self-timed writes
- Quad data rate (QDR®) II+ operates with 2.0 cycle read latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to QDR I device with 1 cycle read latency when $\overline{DOFF}$ is asserted LOW
- Core V_{DD} = 1.8 V± 0.1 V; I/O V_{DDQ} = 1.4 V to V_{DD} [1]
  - Supports both 1.5 V and 1.8 V I/O supply
- HSTL inputs and variable drive HSTL output buffers
- Available in 165-ball CCGA (21 × 25 × 2.83 mm)
- JTAG 1149.1 compatible test access port
- Phase Locked Loop (PLL) for accurate data placement

Configurations

With Read Cycle Latency of 2.0 cycles:

CYRS1643KV18 – 8M × 18
CYRS1645KV18 – 4M × 36

Functional Description

The CYRS1643KV18 and CYRS1645KV18 are 1.8 V synchronous pipelined SRAMs, equipped with QDR II+ architecture. Similar to QDR II architecture, QDR II+ architecture consists of two separate ports: the read port and the write port to access the memory array. The read port has dedicated data outputs to support read operations and the write port has dedicated data inputs to support write operations. The QDR II+ architecture has separate data inputs and data outputs to completely eliminate the need to “turnaround” the data bus that exists with common I/O devices. Each port is accessed through a common address bus. Addresses for read and write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the QDR II+ read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with DDR interfaces. Each address location is associated with four 18-bit words (CYRS1643KV18) or 36-bit words (CYRS1645KV18) that burst sequentially into or out of the device. Because data is transferred into and out of the device on every rising edge of both input clocks (K and $\overline{K}$), memory bandwidth is maximized while simplifying system design by eliminating bus “turnarounds”.

Depth expansion is accomplished with port selects, which enables each port to operate independently.

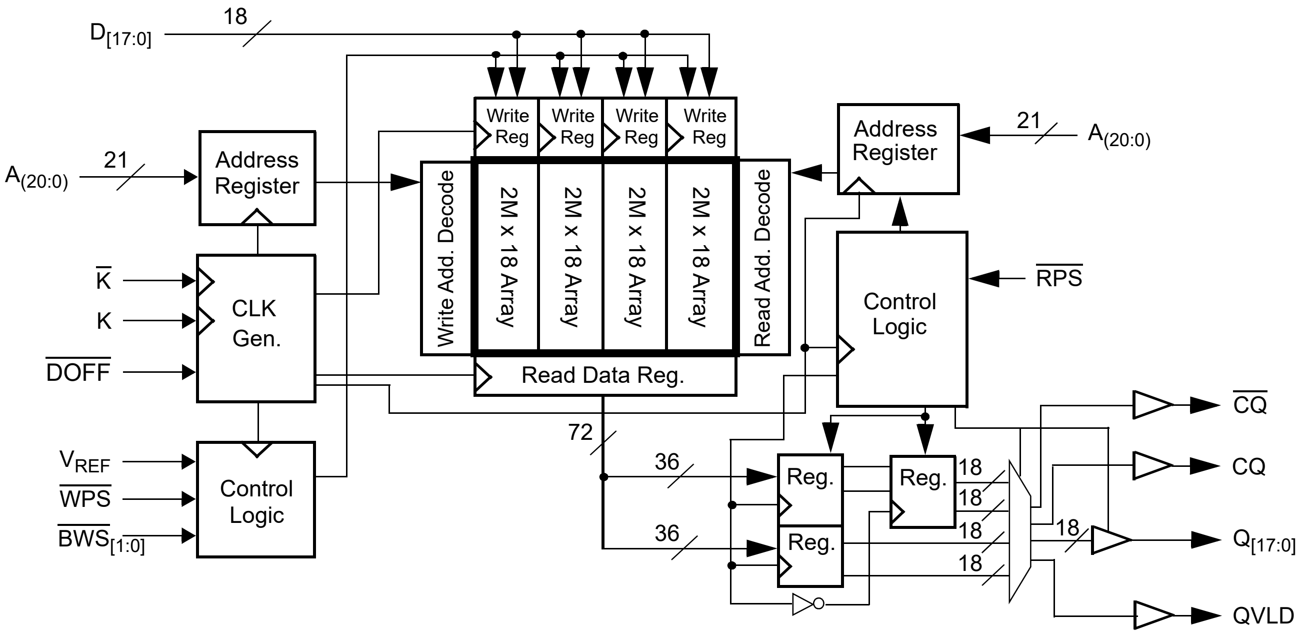
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Note
1. The Cypress QDR II+ devices surpass the QDR consortium specification and can support V_{DDQ} = 1.4 V to V_{DD}.

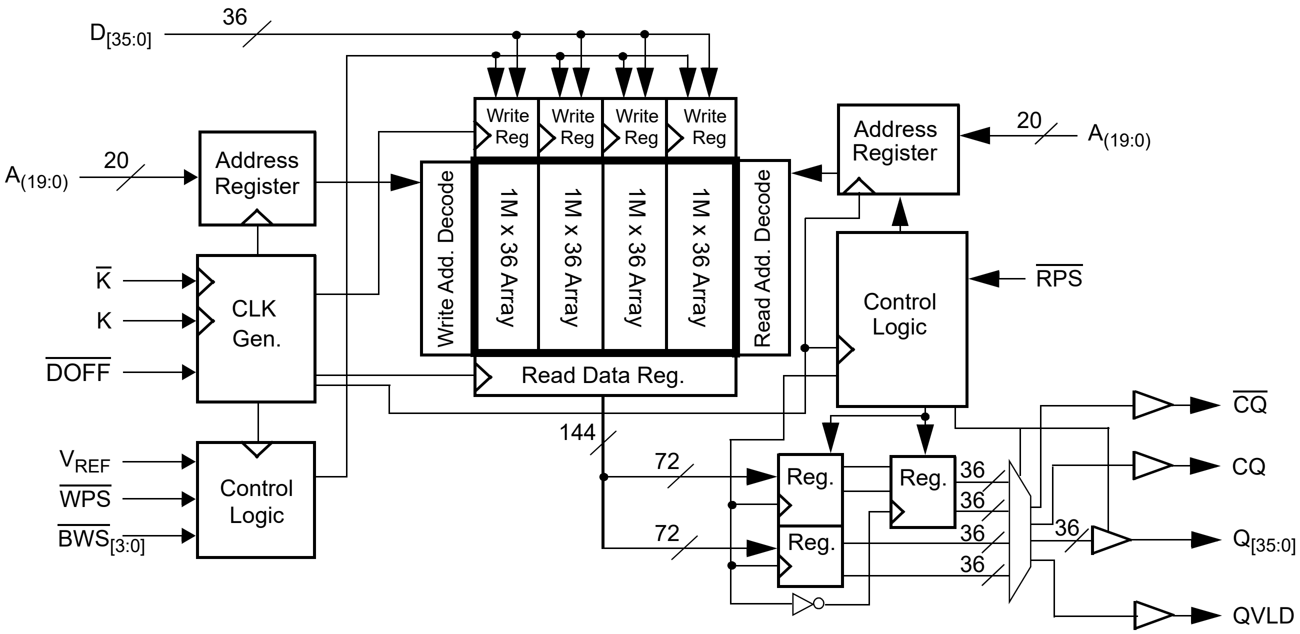
Selection Guide

Description		300 MHz	250 MHz	Unit
Maximum operating frequency		300	250	MHz
Maximum operating current	× 18	840	780	mA
	× 36	1070	1040	

Logic Block Diagram – CYRS1643KV18



Logic Block Diagram – CYRS1645KV18



Contents

Pinouts

The pin configurations for CYRS1643KV18 and CYRS1645KV18 follow. [2]

Figure 1. 165-ball CCGA (21 × 25 × 2.83 mm) pinout

CYRS1643KV18 (8M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	A	A	$\overline{\text{WPS}}$	$\overline{\text{BWS}_1}$	$\overline{\text{K}}$	NC/288M	$\overline{\text{RPS}}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{\text{BWS}_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{\text{DOFF}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CYRS1645KV18 (4M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	NC/288M	A	$\overline{\text{WPS}}$	$\overline{\text{BWS}_2}$	$\overline{\text{K}}$	$\overline{\text{BWS}_1}$	$\overline{\text{RPS}}$	A	A	CQ
B	Q27	Q18	D18	A	$\overline{\text{BWS}_3}$	K	$\overline{\text{BWS}_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	NC	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{\text{DOFF}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Note

2. NC/288M is not connected to the die and can be tied to any voltage level.

Pin Definitions

Pin Name	I/O	Pin Description
$D_{[x:0]}$	Input-Synchronous	**Data Input Signals**. Sampled on the rising edge of K and $\overline{K}$ clocks when valid write operations are active. CYRS1643KV18 – $D_{[17:0]}$ CYRS1645KV18 – $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	**Write Port Select** – **Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$.
$\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$	Input-Synchronous	**Byte Write Select 0, 1, 2 and 3** – **Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks when write operations are active. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CYRS1643KV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9]}$. CYRS1645KV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$, $\overline{BWS}_1$ controls $D_{[17:9]}$, $\overline{BWS}_2$ controls $D_{[26:18]}$ and $\overline{BWS}_3$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address Inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 8M × 18 (4 arrays each of 2M × 18) for CYRS1643KV18 and 4M × 36 (4 arrays each of 1M × 36) for CYRS1645KV18. Therefore, only 21 address inputs for CYRS1643KV18 and 20 address inputs for CYRS1645KV18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-Synchronous	**Data Output Signals**. These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of the K and $\overline{K}$ clocks during read operations. On deselecting the read port, $Q_{[x:0]}$ are automatically tri-stated. CYRS1643KV18 – $Q_{[17:0]}$ CYRS1645KV18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	**Read Port Select** – **Active LOW**. Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the K clock. Each read access consists of a burst of four sequential transfers.
QVLD	Valid output indicator	**Valid Output Indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$.
CQ	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics on page 25.
$\overline{CQ}$	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the QDR II+.The timings for the echo clocks are shown in the Switching Characteristics on page 25.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**PLL Turn Off** – **Active LOW**. Connecting this pin to ground turns off the PLL inside the device. The timings in the PLL turned off operation differs from those listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in QDR I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR I timing.
TDO	Output	**Test data-out (TDO) pin for JTAG**.
TCK	Input	**Test clock (TCK) pin for JTAG**.
TDI	Input	**Test data-in (TDI) pin for JTAG**.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
TMS	Input	**Test mode select (TMS) pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

Functional Overview

CYRS1643KV18 and CYRS1645KV18 are synchronous pipelined Burst SRAMs equipped with a read port and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and flows out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR II+ completely eliminates the need to “turnaround” the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of four 18-bit data transfers in the case of CYRS1643KV18 and four 36-bit data transfers in the case of CYRS1645KV18, in two clock cycles.

These devices operate with a read latency of two cycles when the $\overline{DOFF}$ pin is tied HIGH. When the $\overline{DOFF}$ pin is set LOW or connected to V_{SS}, then the device behaves in QDR I mode with a read latency of one clock cycle.

Accesses for both ports are initiated on the positive input clock (K). All synchronous input and output timing are referenced from the rising edge of the input clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) outputs pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$) as well.

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{NWS}_{[x:0]}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

CYRS1643KV18 is described in the following sections. The same basic descriptions apply to CYRS1645KV18.

Read Operations

CYRS1643KV18 is organized internally as four arrays of 2M × 18. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next two K clock rises, the corresponding lowest order 18-bit word of data is driven on to the $Q_{[17:0]}$ using K as the output timing reference. On the subsequent rising edge of $\overline{K}$, the next 18-bit data word is driven on to the $Q_{[17:0]}$. This process continues until all four 18-bit data words have been driven out onto $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K or $\overline{K}$). To maintain the internal logic, each read access must be allowed to complete. Each read access consists of four 18-bit data words and takes two clock cycles to complete. Therefore, read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second read request. Read accesses can be initiated on every other K clock rise. Doing so pipelines the data flow such that data is transferred out of the device on every rising edge of the input clocks (K and $\overline{K}$).

When the read port is deselected, CYRS1643KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tristates the outputs following the next rising edge of the positive input clock (K). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, write accesses to the device can not be initiated on two consecutive K clock rises. The internal logic of the device ignores the second write request. Write accesses can be initiated on every other rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When deselected, the write port ignores all inputs after the pending write operations have been completed.

Byte Write Operations

Byte write operations are supported by the CYRS1643KV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

Concurrent Transactions

The read and write ports on CYRS1643KV18 operate independently of one another. As each port latches the address inputs on different clock edges, the user can read or write to any location, regardless of the transaction on the other port. If the ports access the same location when a read follows a write in successive clock cycles, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Read access and write access must be scheduled such that one transaction is initiated on any clock cycle. If both ports are selected on the same K clock rise, the arbitration depends on the previous state of the SRAM. If both ports are deselected, the read port takes priority. If a read was initiated on the previous cycle, the write port takes priority (as read operations can not be initiated on consecutive cycles). If a write was initiated on the previous cycle, the read port takes priority (as write operations can not be initiated on consecutive cycles). Therefore, asserting both port selects active from a deselected state results in alternating read or write operations being initiated, with the first access being a read.

Depth Expansion

CYRS1643KV18 has a port select input for each port. This enables for easy depth expansion. Both port selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting a port does not affect the other port. All pending transactions (read and write) are completed before the device is deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM, the allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with $V_{DDQ} = 1.5$ V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the QDR II+ to simplify data capture on high-speed systems. Two echo clocks are generated by the QDR II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free-running clocks and are synchronized to the input clock of the QDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 25.

Valid Data Indicator (QVLD)

QVLD is provided on the QDR II+ to simplify data capture on high-speed systems. The QVLD is generated by the QDR II+ device along with data output. This signal is also edge-aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power-up, when the $\overline{DOFF}$ is tied HIGH, the PLL is locked after 20 µs of stable clock. The PLL can also be reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20 µs after a stable clock is presented. The PLL may be disabled by applying ground to the $\overline{DOFF}$ pin. When the PLL is turned off, the device behaves in QDR I mode (with one cycle latency and a longer access time). For information, refer to the application note AN46982 - *PLL Considerations in QDR® II/II+/DDR-II/II+ SRAMs*.

Qualification and Screening

The 65-nm RadStop™ technology was qualified by Cypress after meeting the criteria of the General Manufacturing Standards. The test flow includes screening units with the defined flow (Class Q, Class V) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the 90-nm process and the SRAM products are subject to period or lot-based technology conformance inspection (TCI) and quality conformance inspection (QCI) tests, respectively. Cypress offers both prototyping models and flight units of these product configurations.

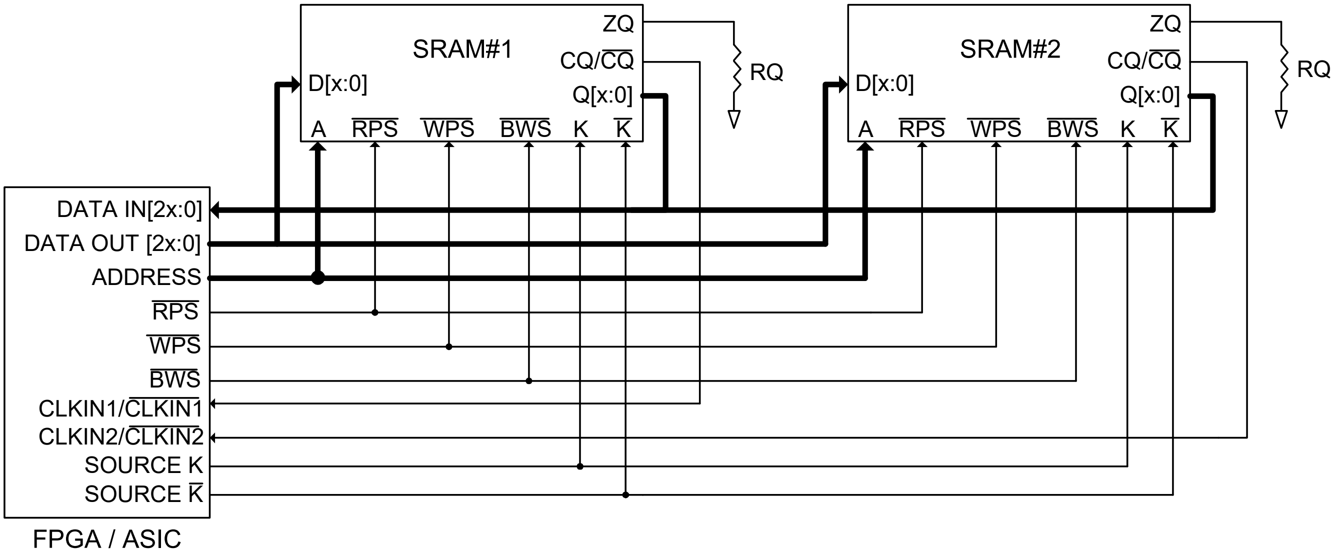
Table 1. Qualification Tests

Group Test	Feature
Group A	General electrical tests
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, lead Integrity, seal, and acceleration
Group C	Life tests - 1000 hours at 125 °C or equivalent
Group D	Package related mechanical tests - shock, vibration, accel, salt, seal, lead finish adhesion, lid torque, thermal shock, and moisture resistance
Group E	Radiation tests

Application Example

Figure 2 shows two QDR II+ devices used in an application.

Figure 2. Application Example



Truth Table

The truth table for CYRS1643KV18 and CYRS1645KV18 follows. [3, 4, 5, 6, 7, 8]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ	DQ	DQ
Write Cycle: Load address on the rising edge of K; input write data on two consecutive K and $\overline{K}$ rising edges.	L–H	H [9]	L [10]	D(A) at K(t + 1)↑	D(A + 1) at $\overline{K}$(t + 1)↑	D(A + 2) at K(t + 2)↑	D(A + 3) at $\overline{K}$(t + 2)↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K; wait two cycles; read data on two consecutive K and $\overline{K}$ rising edges.	L–H	L [10]	X	Q(A) at K(t + 2)↑	Q(A + 1) at $\overline{K}$(t + 2)↑	Q(A + 2) at K(t + 3)↑	Q(A + 3) at $\overline{K}$(t + 3)↑
NOP: No Operation	L–H	H	H	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Write Cycle Descriptions

The write cycle description table for CYRS1643KV18 follows. [3, 11]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: CYRS1643KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L–H	During the data portion of a write sequence: CYRS1643KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: CYRS1643KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: CYRS1643KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: CYRS1643KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: CYRS1643KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes

[3] X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.

[4] Device powers up deselected with the outputs in a tri-state condition.

[5] "A" represents address location latched by the devices when transaction was initiated. A + 1, A + 2, and A + 3 represents the address sequence in the burst.

[6] "t" represents the cycle at which a read/write operation is started. t + 1, t + 2, and t + 3 are the first, second and third clock cycles respectively succeeding the "t" clock cycle.

[7] Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges as well.

[8] It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

[9] If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation.

[10] This signal was HIGH on previous K clock rise. Initiating consecutive read or write operations on consecutive K clock rises is not permitted. The device ignores the second read or write request.

[11] Is based on a write cycle that was initiated in accordance with the Truth Table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$ and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

Write Cycle Descriptions

The write cycle description table for CYRS1645KV18 follows. [12, 13]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the Data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the Data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the Data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the Data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the Data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the Data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the Data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the Data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the Data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the Data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes

[12] X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.

[13] Is based on a write cycle that was initiated in accordance with the Truth Table on page 11. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$ and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the CCGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8 V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull-up resistor. TDO must be left unconnected. Upon power-up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port

Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 19). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 16. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 20 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 19.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 19. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the "extest output bus tri-state," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

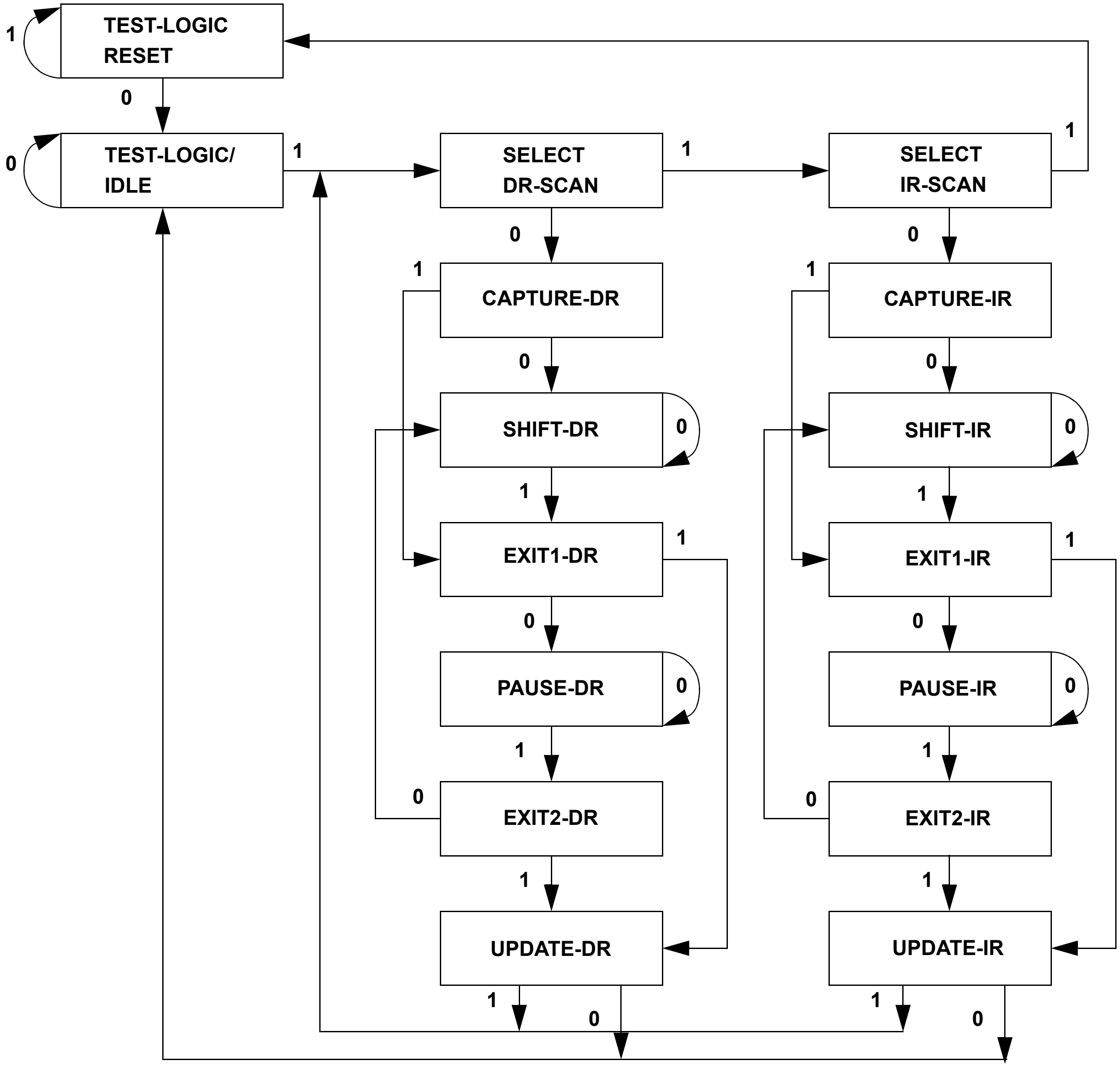
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

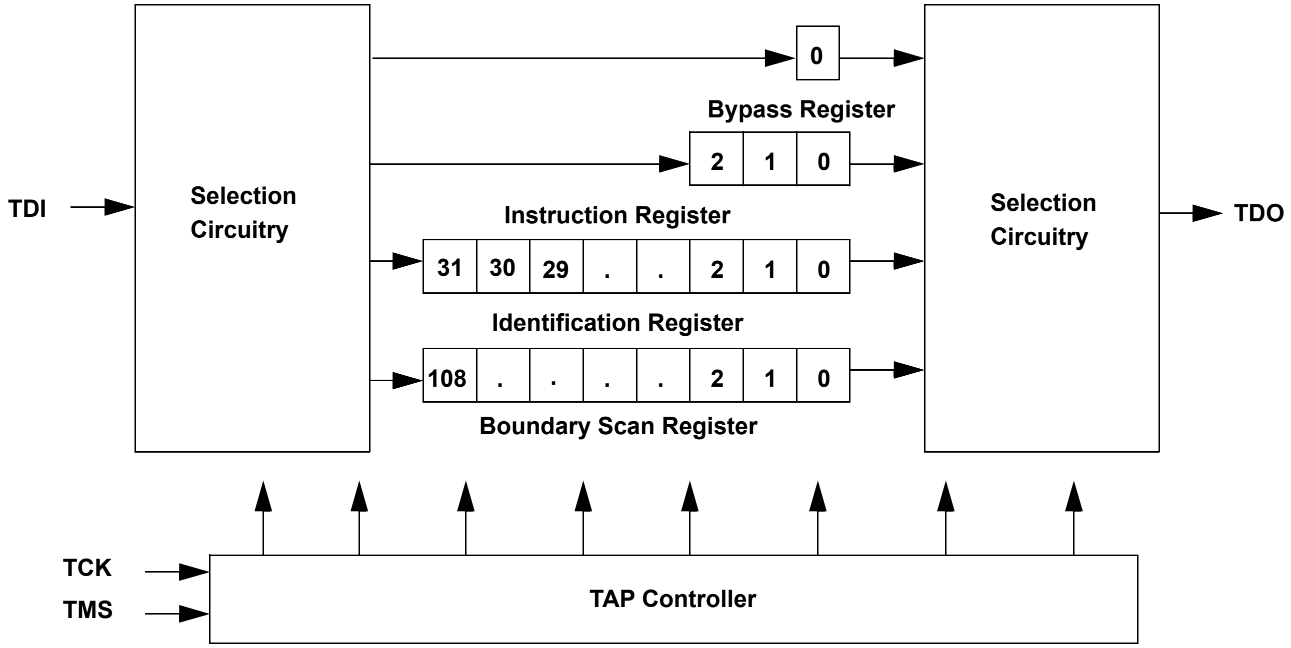
The state diagram for the TAP controller follows. [14]



Note

[14] The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range

Parameter [15, 16, 17]	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = -2.0$ mA	1.4	–	V
V_{OH2}	Output HIGH Voltage	$I_{OH} = -100$ µA	1.6	–	V
V_{OL1}	Output LOW Voltage	$I_{OL} = 2.0$ mA	–	0.4	V
V_{OL2}	Output LOW Voltage	$I_{OL} = 100$ µA	–	0.2	V
V_{IH}	Input HIGH Voltage	–	$0.65 \times V_{DD}$	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage	–	–0.3	$0.35 \times V_{DD}$	V
I_X	Input and Output Load Current	$GND \le V_I \le V_{DD}$	–5	5	µA

Notes

[15] These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics on page 22.

[16] Overshoot: $V_{IH}(AC) \le V_{DDQ} + 0.35V$ (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) \ge -0.3V$ (Pulse width less than $t_{CYC}/2$).

[17] All Voltage referenced to Ground.

TAP AC Switching Characteristics

Over the Operating Range

Parameter [18, 19]	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH	20	–	ns
t_{TL}	TCK Clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns

Notes

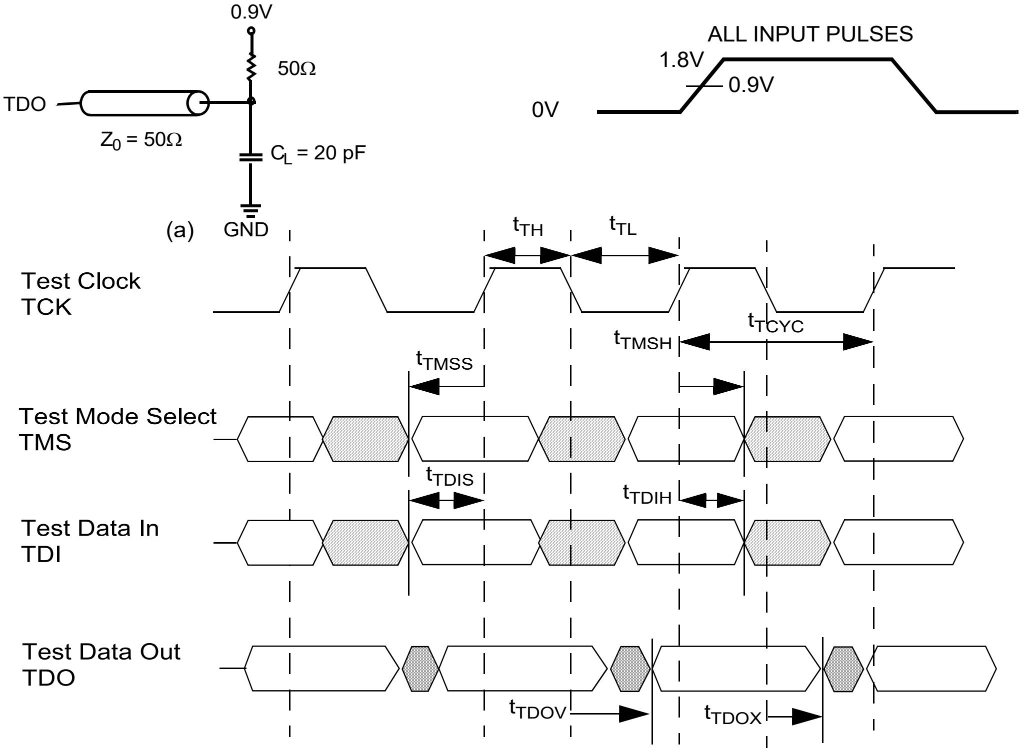
[18] t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.

[19] Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [20]

Figure 3. TAP Timing and Test Conditions



Note

20. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value		Description
	CYRS1643KV18	CYRS1645KV18	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	11010010101010011	11010010101100011	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power Up Sequence in QDR II+ SRAM

QDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

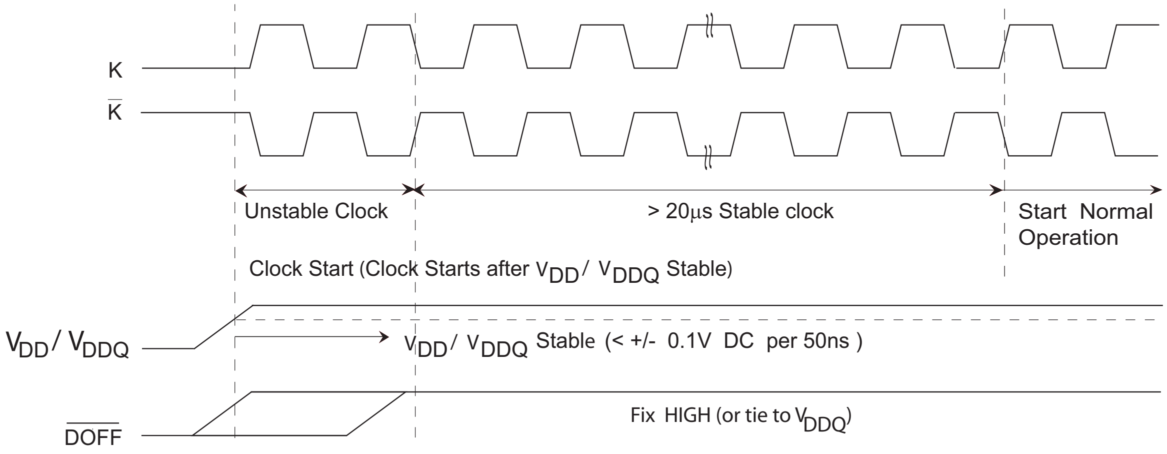
Power Up Sequence

- Apply power and drive $\overline{\text{DOFF}}$ either HIGH or LOW (all other inputs can be HIGH or LOW).
    - ❐ Apply V_{DD} before V_{DDQ}.
    - ❐ Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
    - ❐ Drive $\overline{\text{DOFF}}$ HIGH.
- Provide stable $\overline{\text{DOFF}}$ (HIGH), power, and clock (K, $\overline{\text{K}}$) for 20 µs to lock the PLL

PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low-phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock on to an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 µs of stable clock to relock to the desired clock frequency.

Figure 4. Power-Up Waveforms



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Case temperature
with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +2.9 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC Applied to Outputs in High-Z ......–0.5 V to V_{DDQ} + 0.3 V

DC Input Voltage [21] ....–0.5 V to V_{DD} + 0.3 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(MIL-STD-883, M. 3015) .... > 2001 V

Latch-up Current .... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD} [22]	V_{DDQ} [22]
Military	–55 °C to +125 °C	1.8 ± 0.1 V	1.4 V to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	197	216	FIT/ Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to the application note, AN54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”

Electrical Characteristics

Over the Operating Range

DC Electrical Characteristics

Over the Operating Range

Parameter [23]	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Power supply voltage			1.7	1.8	1.9	V
V_{DDQ}	I/O supply voltage			1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH voltage	Note 24		$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW voltage	Note 25		$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH voltage	I_{OH} = –0.1 mA, Nominal Impedance		V_{DDQ} – 0.2	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW voltage	I_{OL} = 0.1 mA, Nominal Impedance		V_{SS}	–	0.2	V
V_{IH}	Input HIGH voltage			V_{REF} + 0.1	–	V_{DDQ} + 0.3	V
V_{IL}	Input LOW voltage			–0.3	–	V_{REF} – 0.1	V
I_X	Input leakage current	GND ≤ V_I ≤ V_{DDQ}		–20	–	20	μA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–20	–	20	μA
V_{REF}	Input reference voltage [26]	Typical Value = 0.75 V		0.68	0.75	0.95	V
I_{DD} [27]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	(× 18)	–	–	720	mA
			(× 36)	–	–	980	mA

Notes

21. Overshoot: $V_{IH}(AC) \leq V_{DDQ}$ + 0.35V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) \geq$ –0.3V (Pulse width less than $t_{CYC}/2$).
22. Power up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
23. All Voltage referenced to Ground.
24. Output are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
25. Output are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
26. V_{REF} (min) = 0.68V or 0.46V_{DDQ}, whichever is larger, V_{REF} (max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.
27. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics (continued)

Over the Operating Range

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter [23]	Description	Test Conditions		Min	Typ	Max	Unit
I_{SB1}	Automatic Power down Current	Max V_{DD}, Both Ports Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX} = 1/t_{CYC}$, Inputs Static	(× 18)	–	–	390	mA
			(× 36)	–	–	390	mA

AC Electrical Characteristics

Over the Operating Range

Parameter [28]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		V_{REF} + 0.2	–	V_{DDQ} + 0.24	V
V_{IL}	Input LOW Voltage		–0.24	–	V_{REF} – 0.2	V

Note

[28] Overshoot: $V_{IH(AC)} < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width less than $t_{CYC}/2$).

Capacitance

Parameter [31]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	10	pF
C_O	Output capacitance		10	pF

Thermal Resistance

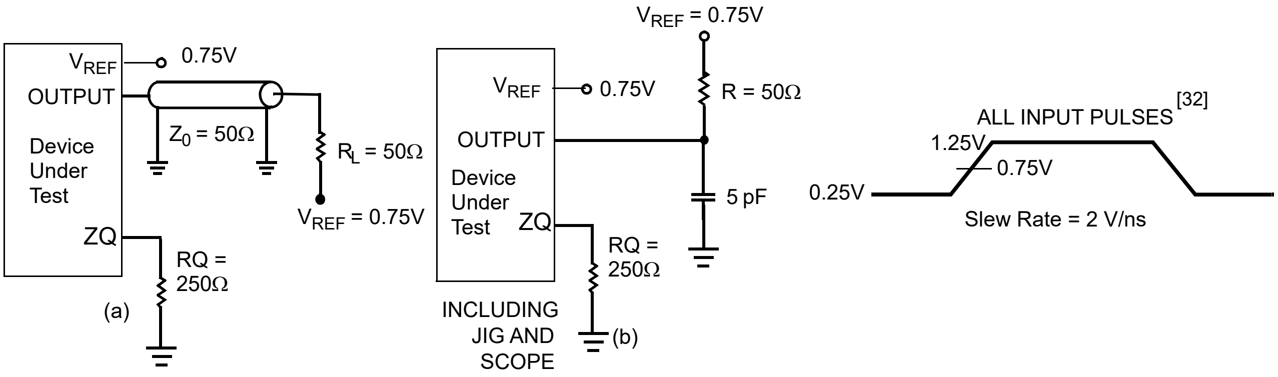
Parameter [31]	Description	Test Conditions	165-ball CCGA Package	Unit
Θ_{JC}	Thermal resistance (junction to case)	According to MIL-STD-883	8.6	°C/W

Radiation Performance

Parameter	Test Conditions	Limits	Unit
Total dose	T_A = 25 °C, V_{DD} = V_{DDQ} = 1.8 V	200k	Rads(Si) Co60
Soft error rate	T_A = 25 °C to 125 °C, V_{DD} = V_{DDQ} = 1.8 V with EDAC	1.0×10^{-10}	Upsets/bit-day
Transient dose rate upset	Pulse width (FWHM) = 50 ns, X-Ray, T_C = 25 °C, V_{DD} = V_{DDQ} = 1.8 V	8.6×10^{8}	Rads(Si)/s
Neutron fluence	1 MeV equivalent energy, Unbiased T_A = 25 °C	2e14	N/cm^2
Latch up immunity	T_A = 125 °C, V_{DD} = V_{DDQ} = 1.9 V	120	MeVcm^2/mg

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



Notes

29. Overshoot: $V_{IH(AC)} < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width less than $t_{CYC}/2$).
30. Power up: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
31. Tested initially and after any design or process change that may affect these parameters.
32. Unless otherwise noted, test conditions are based on signal transition time of 2V/ns, timing reference levels of 0.75V, Vref = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of Figure 5.

Switching Characteristics

Over the Operating Range

Parameters [32, 33]		Description	250 MHz		Unit
Cypress Parameter	Consortium Parameter		Min	Max	
t_{POWER}		V_{DD}(typical) to the First Access [34]	1	–	ms
t_{CYC}	t_{KHKH}	K Clock Cycle Time	4.0	8.4	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$) HIGH	1.6	–	ns
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$) LOW	1.6	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	1.8	–	ns
Setup Times					
t_{SA}	t_{AVKH}	Address Setup to K Clock Rise	0.5	–	ns
t_{SC}	t_{IVKH}	Control Setup to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.5	–	ns
t_{SCDDR}	t_{IVKH}	DDR Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.5	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise	0.5	–	ns
Hold Times					
t_{HA}	t_{KHAX}	Address Hold after K Clock Rise	0.5	–	ns
t_{HC}	t_{KHIX}	Control Hold after K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.5	–	ns
t_{HCDDR}	t_{KHIX}	DDR Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.5	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	0.5	–	ns
Output Times					
t_{CO}	t_{CHQV}	K/$\overline{K}$ Clock Rise to Data Valid	–	0.85	ns
t_{DOH}	t_{CHQX}	Data Output Hold after Output K/$\overline{K}$ Clock Rise (Active to Active)	–0.85	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ Clock Rise to Echo Clock Valid	–	0.85	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after K/$\overline{K}$ Clock Rise	–0.5	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid		0.50	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.30	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH [35]	1.55	–	ns
$t_{CQHC\overline{Q}H}$	$t_{CQHC\overline{Q}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise (rising edge to rising edge) [35]	1.55	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) Rise to High Z (Active to High Z) [36, 37]	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) Rise to Low Z [36, 37]	–0.45	–	ns
t_{QVLD}	$t_{CQHQVLD}$	Echo Clock High to QVLD Valid [38]	–0.50	0.50	ns
PLL Timing					
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	PLL Lock Time (K)	20	–	μs
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to PLL Reset [39]	30	–	ns

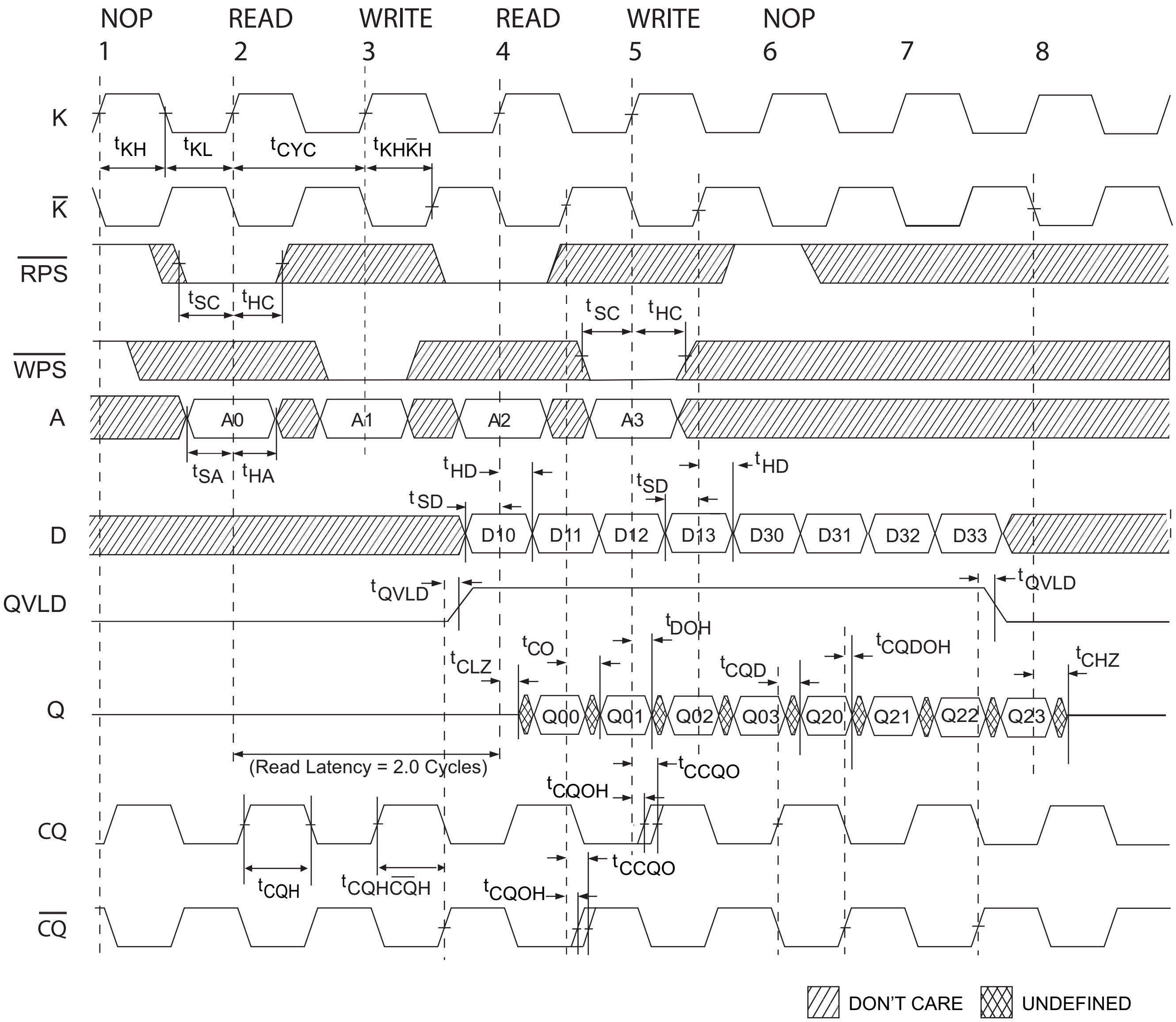
Notes

33. When a part with a maximum frequency above 333 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
34. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
35. These parameters are extrapolated from the input timing parameters (t_{CYC}/2 - 250 ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.
36. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms on page 24. Transition is measured ± 100 mV from steady-state voltage.
37. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
38. t_{QVLD} spec is applicable for both rising and falling edges of QVLD signal.
39. Hold to $>V_{IH}$ or $<V_{IL}$.

Switching Waveforms

Read/Write/Deselect Sequence

Figure 6. Waveform for 2.0 Cycle Read Latency [40, 41, 42]



Notes

40. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
41. Outputs are disabled (High-Z) one clock cycle after a NOP.
42. In this example, if address A2 = A1, then data Q20 = D10, Q21 = D11, Q22 = D12, and Q23 = D13. Write data is forwarded immediately as read results. This note applies to the whole diagram.

Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for (× 18 option), contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at www.cypress.com/products

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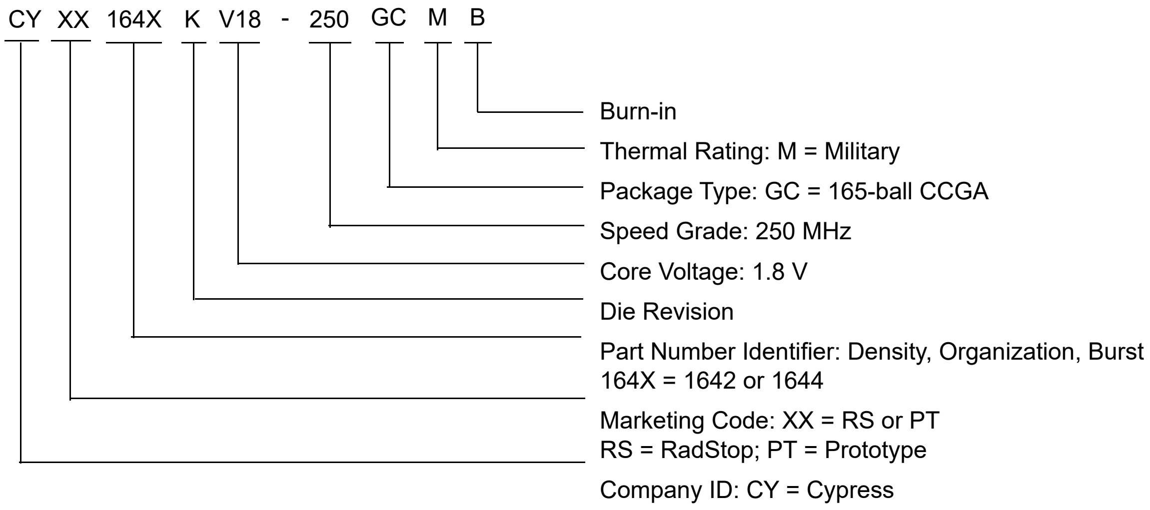
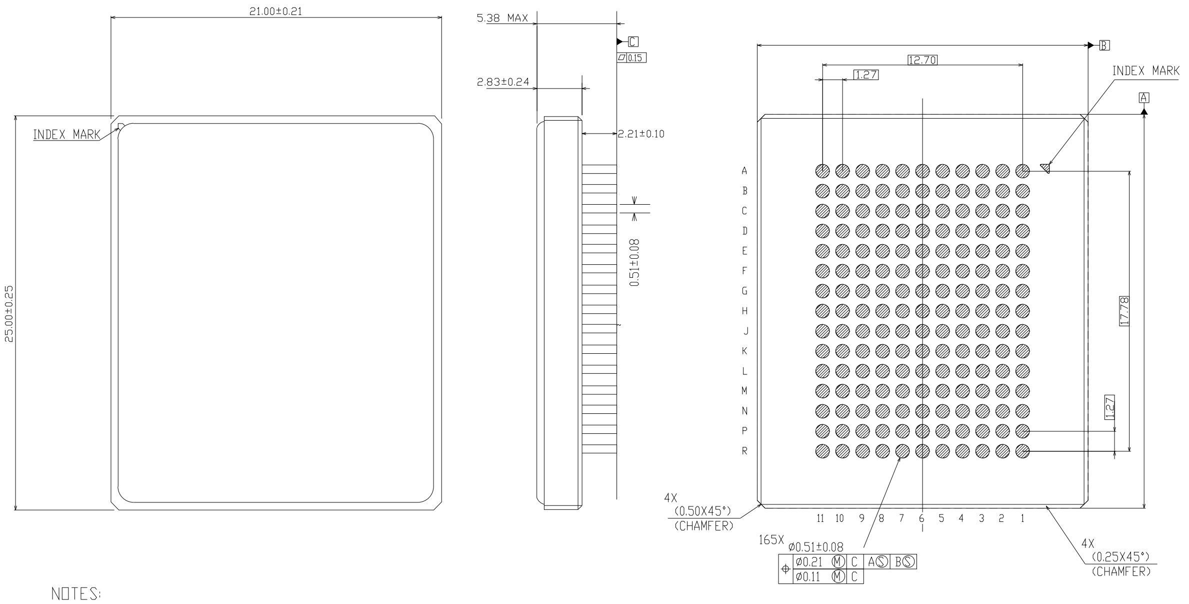
Speed (MHz)	Ordering Code	Description	Package Diagram	Package Type	Operating Range
250	CYRS1643KV18-250GCMB	144M QDR II+, × 18, Burst of 4	001-58969	165-ball CCGA (21 × 25 × 2.83 mm)	Military
	CYRS1645KV18-250GCMB	144M QDR II+, × 36, Burst of 4			
	CYPT1643KV18-250GCMB	144M QDR II+, × 18, Burst of 4, Prototype			
	CYPT1645KV18-250GCMB	144M QDR II+, × 36, Burst of 4, Prototype			
	5962R1821404VXF	144M QDR II+, × 18, Burst of 4, DLAM Part			
	5962R1821504VXF	144M QDR II+, × 36, Burst of 4, DLAM Part			

Ordering Code Definitions



Package Diagram

Figure 7. 165-ball CCGA (21 × 25 × 2.83 mm) Package Outline, 001-58969



NOTES:

1. JEDEC REFERENCE : MO-158 VAR BE-1
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-58969 *E

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BWS}}$	byte write select
CCGA	ceramic column grid array
DED	double error detection
DLL	delay lock loop
DDR	double data rate
DSCC	defense supply center columbus
EDAC	error detection and correction
HSTL	high speed transceiver logic
I/O	input/output
JTAG	Joint Test Action Group
LSB	least significant bit
LSBU	logical single-bit upsets
LMBU	logical multi-bit upsets
MSB	most significant bit
PDA	percent defect allowable
PIND	particle impact noise detection
PDA	percent defective allowable
QDR	quad data rate
$\overline{\text{RPS}}$	read port select
SEC	single error correction
SEL	single event latch up
SRAM	static random access memory
TAP	test access port
TCK	test clock
TDI	test data in
TDO	test data out
TMS	test mode select
$\overline{\text{WPS}}$	write port select

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Krad	kiloradian
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
N/cm^2	Neutron particles fluence per cm^2 area
ns	nanosecond
nm	nanometer
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
Rads(Si)	unit of absorbed radiation energy from ionizing radiation per kg of material. (1 rad(Si)) = 10 mGy = 10 – 2 J/kg
V	volt
W	watt

Document History Page

Document Title: CYRS1643KV18/CYRS1645KV18, 144-Mbit QDR II+ SRAM Four-Word Burst Architecture with RadStop Technology Document Number: 002-21798			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*C	6718425	10/30/2019	Changed the datasheet to Final.
*D	7144042	05/25/2021	Updated Radiation Performance table. Updated Sales, Solutions, and Legal Information and Copyright information.

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