16-Mb hardened static RAM with ECC and RADSTOP™ technology

(1M × 16)

Radiation performance

- Radiation data
  - Total dose = 200 krad
  - Embedded ECC for single-bit error correction[1, 2]
  - Soft error rate (both heavy ion and proton) heavy ions ≤ 1×10^{-10} upsets/bit-day
  - Neutron = 1.5×10^{11} N/cm^2
  - Dose rates:
    - ≥ 3.0×10^8 (rad(Si)/s) (R/W)
    - ≥ 2.0×10^9 (rad(Si)/s) (static)
  - Dose rate latch-up survivability ≥ 5.0×10^{10} (rad(Si)/s) (125°C)
  - Latch-up immunity >60 MeV.cm^2/mg (95°C)
- Processing flows
  - V Grade - Class V flow in compliance with MIL-PRF 38535
- Prototyping options
  - CYPT1061G prototype units with the same functional and timing as flight units using non-radiation hardened die in a 54-lead ceramic TSOP package

Features

- Temperature ranges
  - Military/Space: –55°C to 125°C
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 90 mA at 10 ns (typical)
- Low CMOS standby power
  - I_{SB2} = 20 mA (typical)
- 1.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$[3] and $\overline{OE}$ features
- Available in gold-plated 54-lead ceramic TSOP package

Notes
1. This device does not support automatic write-back on error detection.
2. SER FIT Rate < 0.1 FIT/Mb. See **AN88889** for details.
3. $\overline{CE}$ is the logical combination of $\overline{CE1}$ and CE2.

Logic block diagram

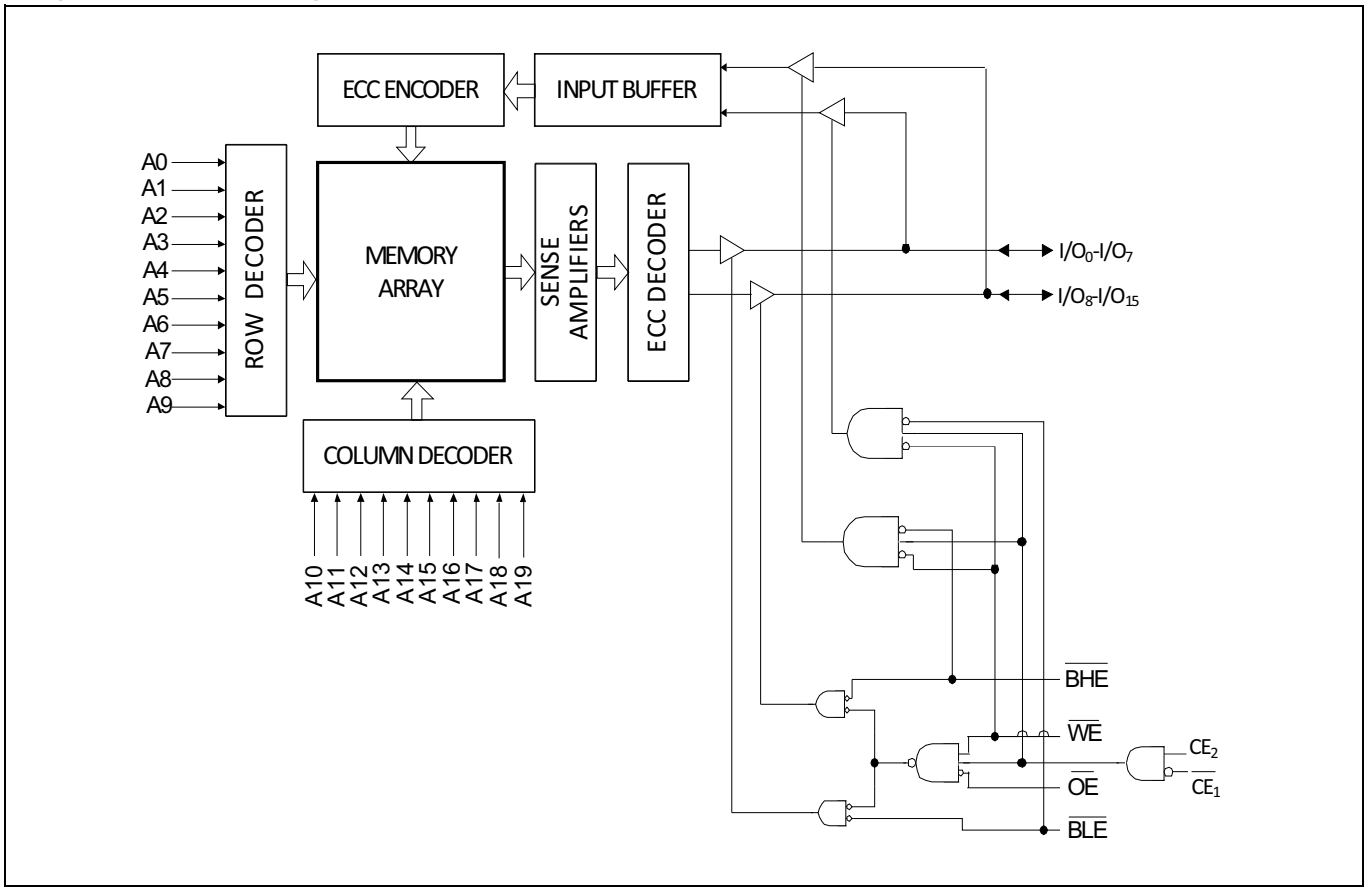


Table of contents

1 Functional description

CYRS1061G is a high-performance CMOS static RAM organized as 1M words by 16 bits with RADSTOP™ technology and embedded ECC. Infineon' state-of-the-art RADSTOP™ technology is radiation-hardened through proprietary design and process-hardening techniques. The 16-Mb fast asynchronous SRAM with the RADSTOP™ technology is also QML V certified with Defense Logistics Agency Land and Maritime (DLAM).

ECC logic can detect and correct single-bit error in read data word during read cycles.

This device is dual Chip Enable input and is accessed by asserting both Chip Enable inputs - $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a High-Z state when the device is deselected ($\overline{CE}$[4] HIGH), or control signals are de-asserted ($\overline{OE}$, BLE, BHE). See **Logic block diagram**.

The CYRS1061G military device is available in 54-lead ceramic TSOP package with center power and ground (revolutionary) pinout.

For best practice recommendations, see white paper, **SRAM Board Design Guidelines**.

Notes
4. $\overline{CE}$ is the logical combination of $\overline{CE}$1 and CE2.

2 Selection guide

Table 1 Selection guide

Description	3.3 V / 5.0 V	Unit
Maximum access time	10	ns
Maximum operating current	160	mA
Maximum CMOS standby current	50	

3 Pin configuration

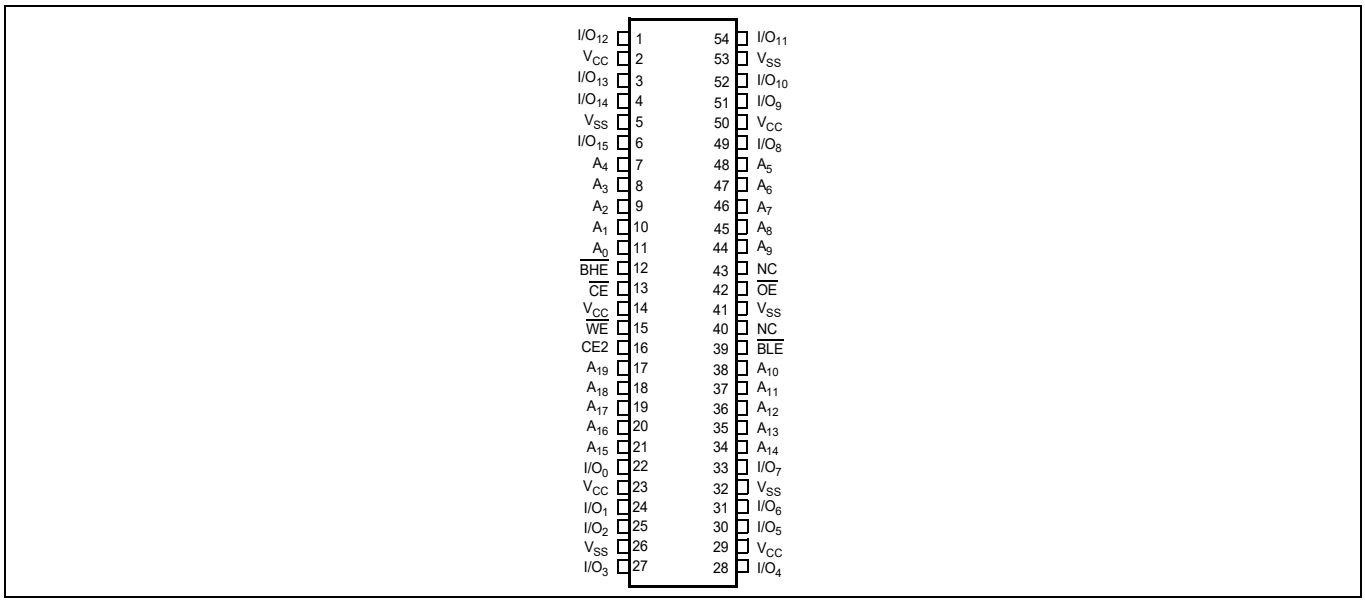


Figure 1 54-lead ceramic TSOP II (22.4 x 11.84 x 3.038 mm) package pinout (Top view)[5, 6]

Notes
5. NC leads are not connected on the die.
6. CE is the logical combination of CE1 and CE2.

4 Maximum ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Table 2 Maximum ratings

Parameter	Ratings
Storage temperature	–65°C to +150°C
Ambient temperature with power applied	–55°C to +125°C
Supply voltage on V_{CC} relative to GND[7]	–0.5 V to +6.0 V
DC voltage applied to outputs in High Z state[7]	–0.5 V to V_{CC} + 0.5 V
DC input voltage[7]	–0.5 V to V_{CC} + 0.5 V
Package power dissipation capability (T_A = 25°C)	1.0 W
Current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 140 mA

Notes

7. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC}(min) and 100-µs wait time after V_{CC} stabilization.

5 Operating range

Table 3 Operating range

Range	Ambient temperature	V_{CC}	Speed
Military/Space	–55°C to +125°C	2.2 V to 3.6 V	10 ns
		4.5 V to 5.5 V	10 ns

6 DC electrical characteristics

Table 4 DC electrical characteristics

Over the operating range

Parameter	Description	Test conditions		Military/Space		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –1.0 mA	2.2 V to 2.7 V	2.0	–	V
		V_{CC} = Min, I_{OH} = –4.0 mA	2.7 V to 3.0 V	2.2	–	
		V_{CC} = Min, I_{OH} = –4.0 mA	3.0 V to 3.6 V	2.4	–	
		V_{CC} = Min, I_{OH} = –4.0 mA	4.5 V to 5.5 V	2.4	–	
		V_{CC} = Min, I_{OH} = –0.1 mA	4.5 V to 5.5 V	V_{CC} – 0.4	–	
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 2 mA	2.2 V to 2.7 V	–	0.4	V
		V_{CC} = Min, I_{OL} = 8 mA	2.7 V to 3.6 V	–	0.4	
		V_{CC} = Min, I_{OL} = 8 mA	4.5 V to 5.5 V	–	0.4	
V_{IH}	Input HIGH voltage		2.2 V to 2.7 V	2.0	V_{CC} + 0.3	V
			2.7 V to 3.6 V	2.0	V_{CC} + 0.3	
			4.5 V to 5.5 V	2.0	V_{CC} + 0.5	
V_{IL}	Input LOW voltage		2.2 V to 2.7 V	–0.3	0.6	V
			2.7 V to 3.6 V	–0.3	0.8	
			4.5 V to 5.5 V	–0.5	0.8	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, output disabled		–5	+5	
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	100 MHz	–	160	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$[8] ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	60	
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$[8] ≥ V_{CC} – 0.2 V V_{IN} ≥ V_{CC} – 0.2 V, or V_{IN} ≤ 0.2 V, f = 0		–	50	

Notes

8. $\overline{CE}$ is the logical combination of $\overline{CE}$1 and CE2.

7 Capacitance

Table 5 Capacitance

Parameter[9]	Description	Test conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25°C, f = 1\,MHz, V_{CC} = 3.3\,V$	10	pF
C_{OUT}	I/O capacitance		10	

Notes
9. Tested initially and after any design or process changes that may affect these parameters.

8 Thermal resistance

Table 6 Thermal resistance

Parameter[10]	Description	Test Conditions	Ceramic flat package	Unit
Θ_{JC}	Thermal resistance (junction to case)	Test according to MIL-PRF 38538	3.38	°C/W

Notes
10.Tested initially and after any design or process changes that may affect these parameters.

9 AC test loads and waveforms

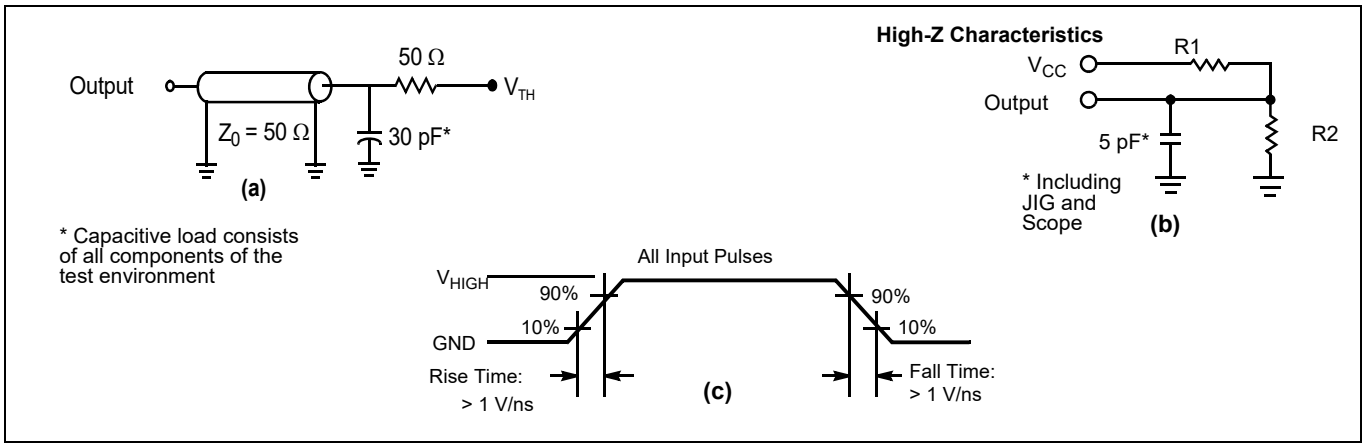


Figure 2 AC test loads and waveforms[11]

Table 7 AC test conditions

Parameters	3.0 V	5.0 V	Unit
R1	317	317	Ω
R2	351	351	
V_{TH}	1.5	1.5	V
V_{HIGH}	3	3	

Notes
11. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC}(min) and 100-µs wait time after V_{CC} stabilization.

10 Data retention characteristics and waveforms

Table 8 Data retention characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC}=V_{DR}$, $\overline{CE}$ [14] $\geq V_{CC}-0.2$ V, $V_{IN} \geq V_{CC}-0.2$ V or $V_{IN} \leq 0.2$ V	–	50.0	mA
t_{CDR} [12]	Chip deselect to data retention time	–	0	–	ns
t_R [12, 13]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	
		$V_{CC} < 2.2$ V	12.0	–	

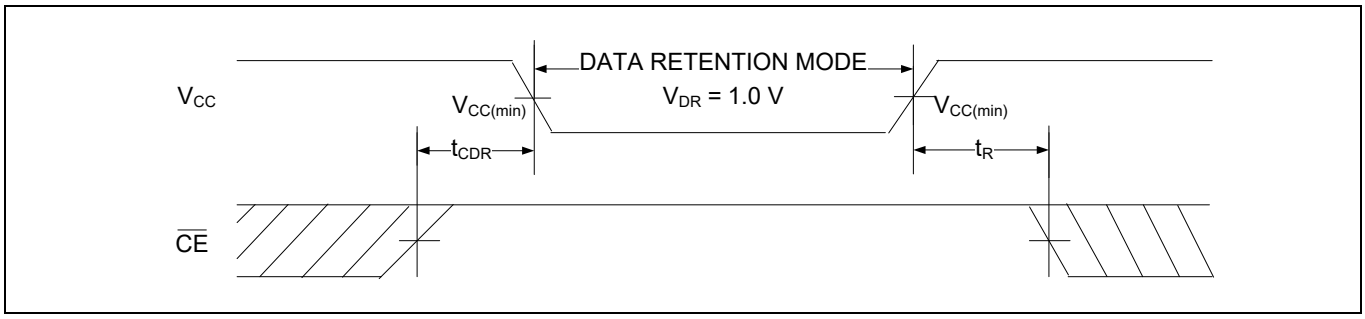


Figure 3 Data retention waveform [14]

Notes

12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
14. $\overline{CE}$ is the logical combination of $\overline{CE1}$ and CE2.

11 AC switching characteristics and waveforms

Table 9 AC switching characteristics

Over the operating range

Parameter[15]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC} (typical) to the first access[16, 17]	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	
t_{OHA}	Data hold from address change	3	–	
t_{ACE}	$\overline{CE}$ LOW to data valid[21]	–	10	
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	
t_{LZOE}	$\overline{OE}$ LOW to low Z[18, 19, 20]	0	–	
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[18, 19, 20]	–	5	
t_{LZCE}	$\overline{CE}$ LOW to low Z[18, 19, 20, 21]	3	–	
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[18, 19, 20, 21]	–	5	
t_{PU}	$\overline{CE}$ LOW to Power-up[17, 21]	0	–	
t_{PD}	$\overline{CE}$ HIGH to Power-down[17, 21]	–	10	
Write Cycle[19, 20]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [17, 21]	7	–	
t_{AW}	Address setup to write end	7	–	
t_{HA}	Address hold from write end	0	–	
t_{SA}	Address setup to write start	0	–	
t_{PWE}	$\overline{WE}$ pulse width	7	–	
t_{SD}	Data setup to write end	5	–	
t_{HD}	Data hold from write end	0	–	
t_{LZWE}	$\overline{WE}$ HIGH to low Z[18, 19, 20]	3	–	
t_{HZWE}	$\overline{WE}$ LOW to High-Z[18, 19, 20]	–	5	

Notes

15. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of **Figure 2**, unless specified otherwise.
16. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
17. These parameters are guaranteed by design and are not tested.
18. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as shown in (b) of **Figure 2**. Transition is measured ±200 mV from steady state voltage.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21. $\overline{CE}$ is the logical combination of $\overline{CE1}$ and CE2.

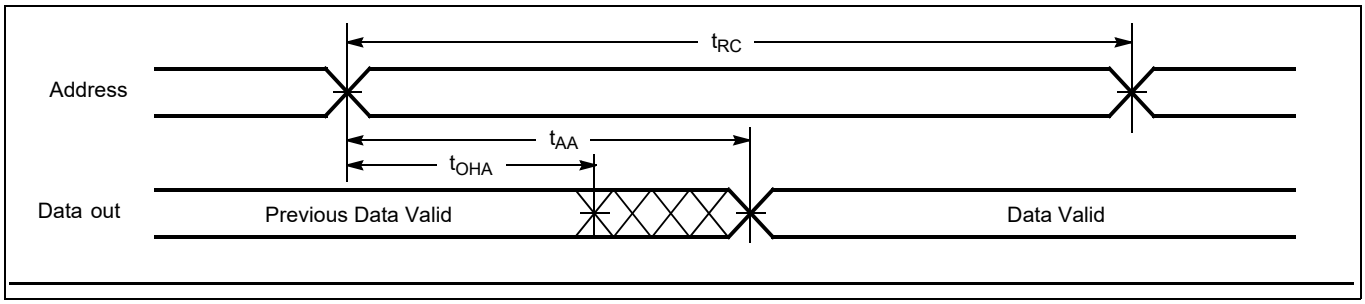


Figure 4 Read Cycle No. 1 [22, 23]

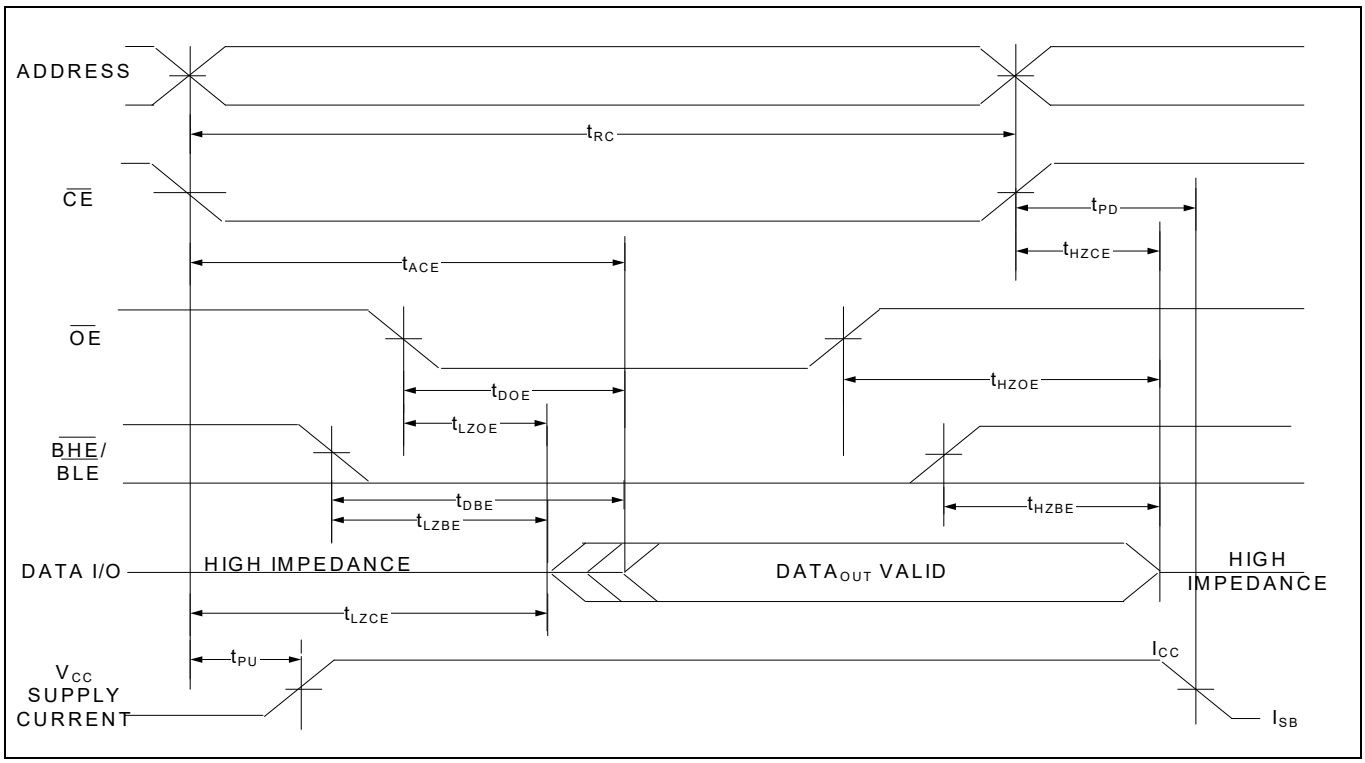


Figure 5 Read Cycle No. 2 ($\overline{OE}$ Controlled, $\overline{WE}$ HIGH) [23, 24, 25]

Notes
22. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
25. $\overline{CE}$ is the logical combination of $\overline{CE1}$ and CE2.

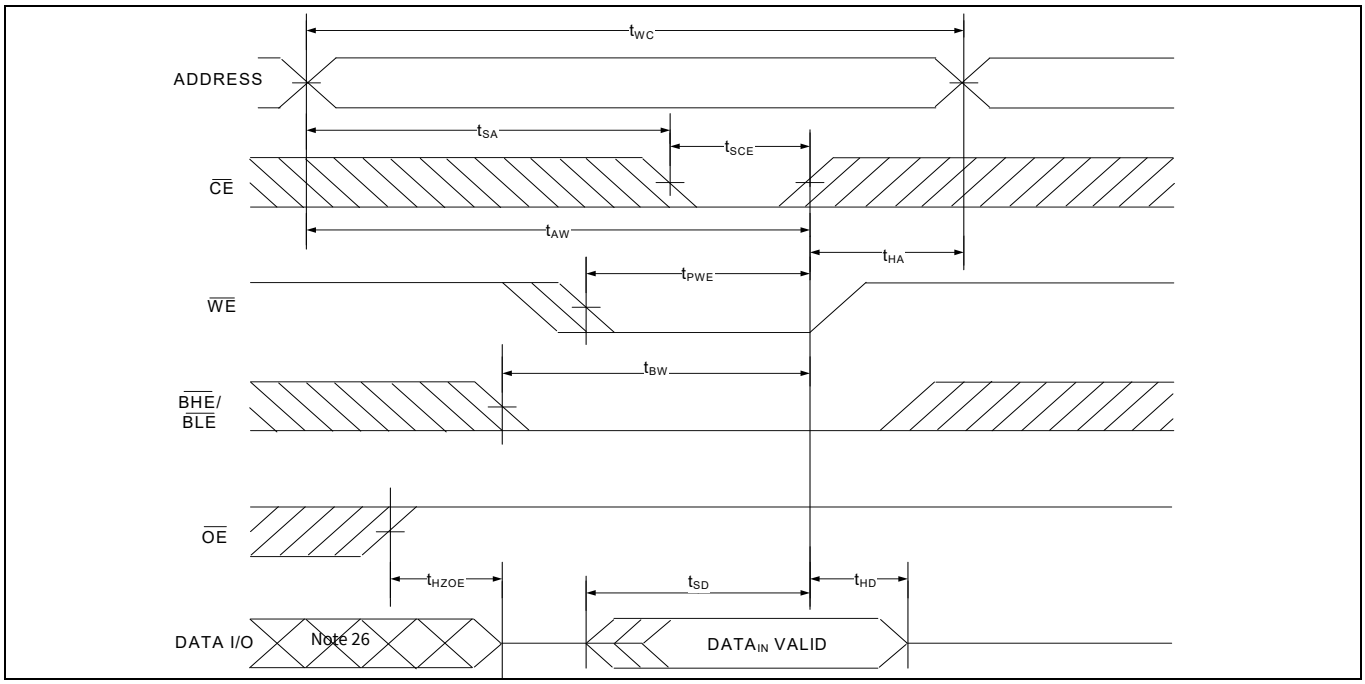


Figure 6 Write Cycle No. 1 (CE Controlled)[27, 28, 31]

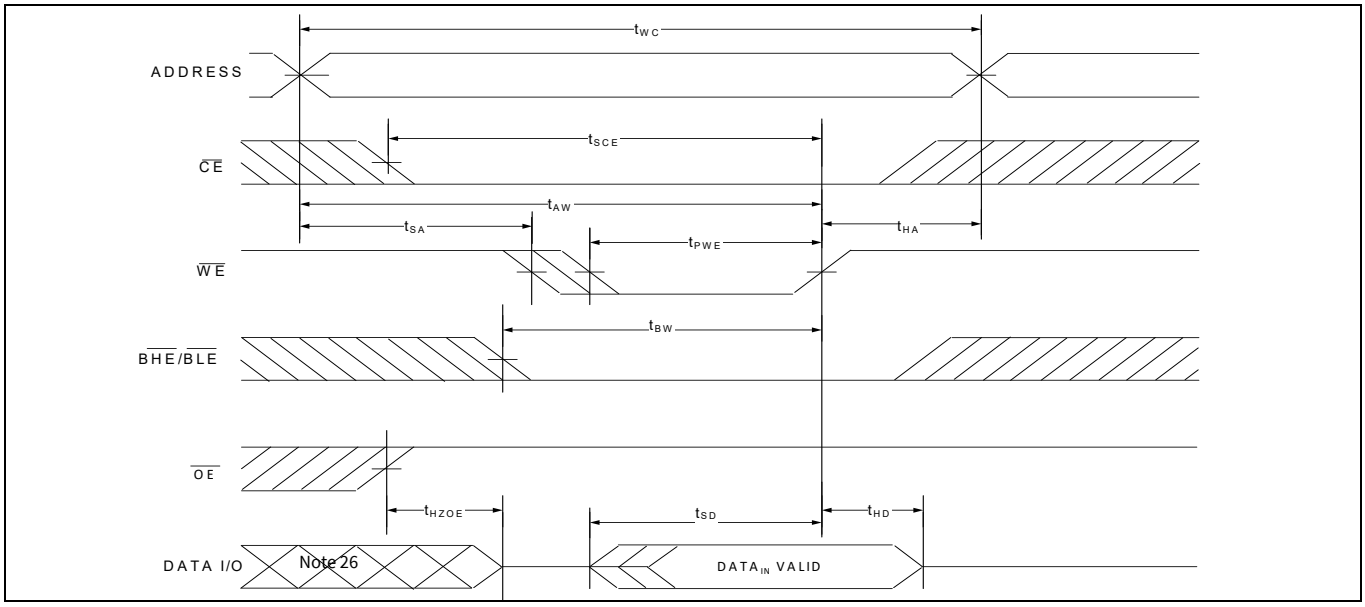


Figure 7 Write Cycle No. 2 (WE Controlled, OE HIGH during Write)[27, 28, 31]

Notes

26. During this period the I/Os are in the output state and input signals should not be applied.
27. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
28. Data I/O is in High-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
29. The minimum write cycle width should be sum of t_{HZWE} and t_{SD}.
30. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
31. $\overline{CE}$ is the logical combination of $\overline{CE1}$ and CE2.

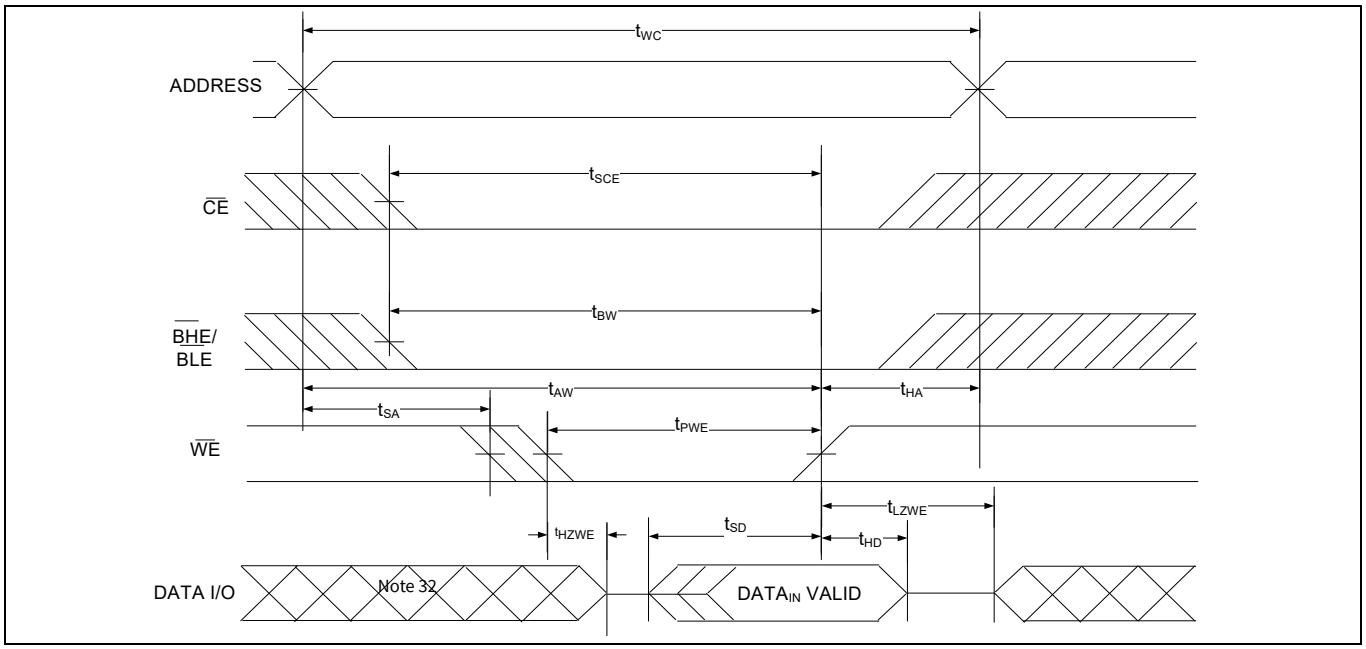


Figure 8 Write Cycle No. 3 (WE Controlled, OE LOW)[33, 34, 35, 36]

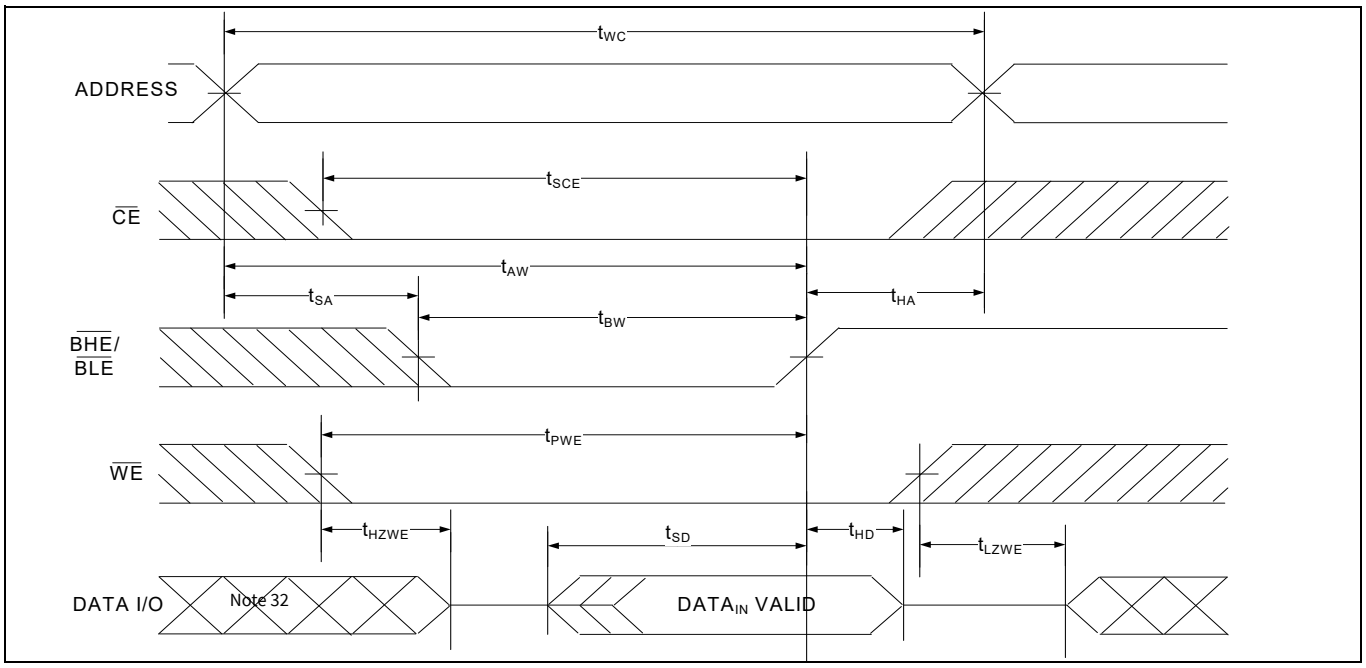


Figure 9 Write Cycle No. 4 (BLE or BHE Controlled)[33, 34, 36]

Notes
32. During this period the I/Os are in the output state and input signals should not be applied.
33. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in High-Z state if CE = V_{IH}, or OE = V_{IH} or BHE, and/or BLE = V_{IH}.
35. The minimum write cycle width should be sum of t_{HZWE} and t_{SD}.
36. CE is the logical combination of CE1 and CE2.

12 Truth table

Table 10 Truth table

CE[38]	$\overline{OE}$	$\overline{WE}$	BLE	BHE	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X[37]	X[37]	X[37]	X[37]	High-Z	High-Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High-Z	Read lower bits only	
L	L	H	H	L	High-Z	Data out	Read upper bits only	
L	X	L	L	L	Data in	Data in	Write all bits	
L	X	L	L	H	Data in	High-Z	Write lower bits only	
L	X	L	H	L	High-Z	Data in	Write upper bits only	
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	

Note
37. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
38. CE is the logical combination of $\overline{CE1}$ and CE2.

13 Ordering information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Infineon website at **www.infineon.com** and see product summary page at **www.infineon.com/products**.

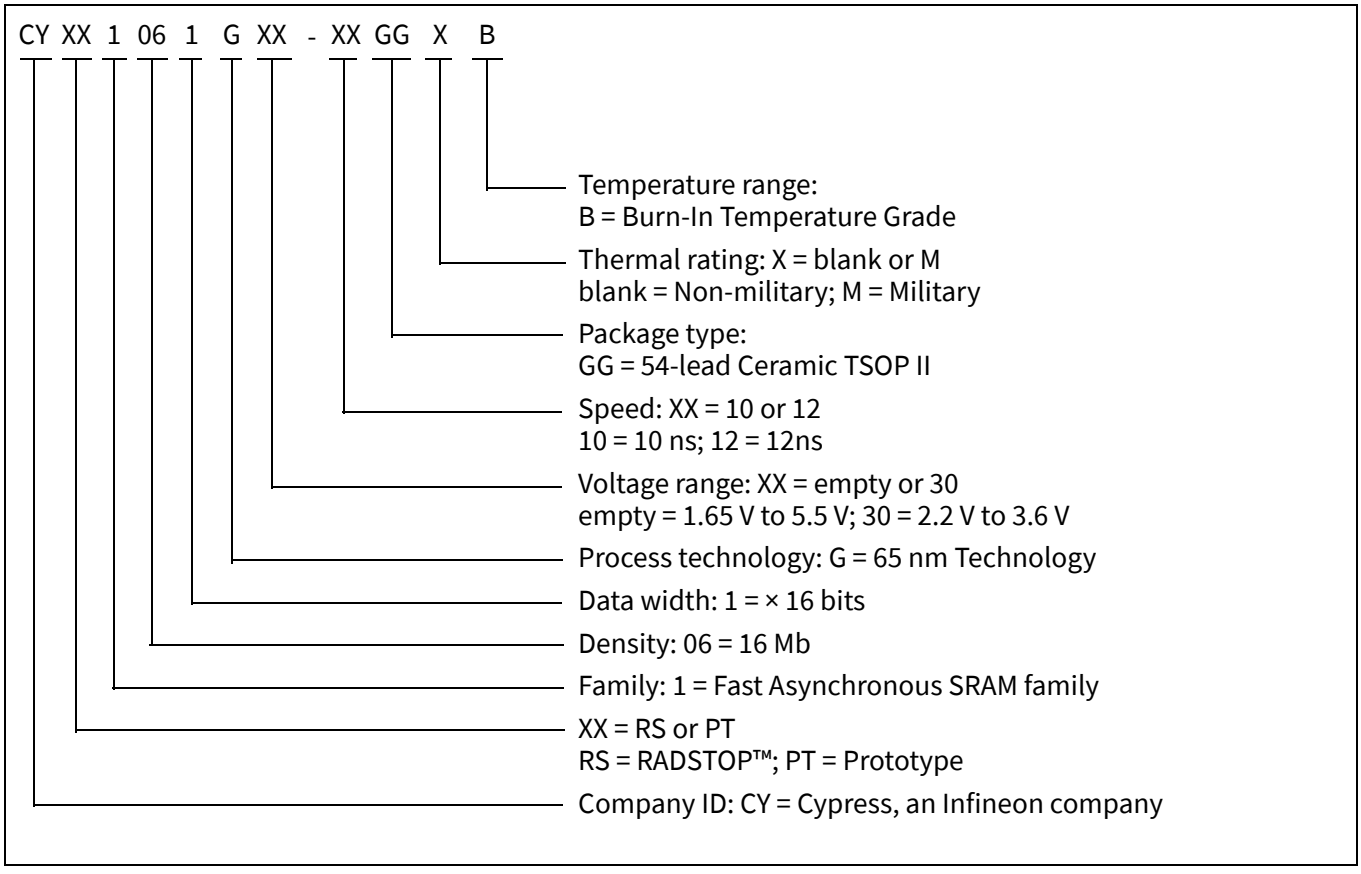
Infineon maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at **www.infineon.com/datasheet/offices**.

Table 11 Ordering information

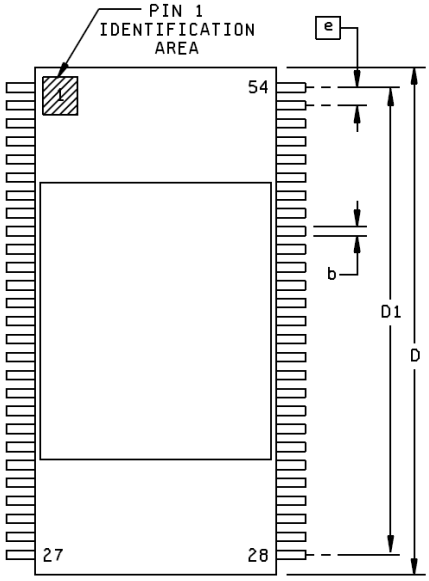
Speed (ns)	Ordering code	Package diagram	Package type	Operating range
10	CYRS1061G30-10GGMB	002-18372	54-lead ceramic TSOP II package	Military
10	CYPT1061G30-10GGMB		54-lead ceramic TSOP II package, Prototype part	
10	5962R2020201VXC		54-lead ceramic TSOP II package, DLAM QML-V part	

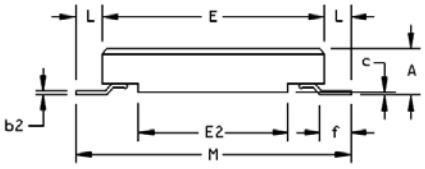
Contact your local Infineon sales representative for availability of these parts.

13.1 Ordering code definitions



14 Package diagram





Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.416	3.038	E2	7.00	7.40
b	.300	.400	e	.80 BSC	
b2	.150	.250	f	1.588	2.096
c	.073	---	L	1.233 NOM (ref)	
D	22.173	22.633	M	14.173	14.427
D1	20.60	21.00	N	54	
E	11.636	12.036			

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

002-18372 Rev. **

Figure 10 54-lead ceramic TSOP II (22.4 × 11.84 × 3.038 mm) GG54, (CG-TSOP-54)

15 Acronyms

Table 12 Acronyms used in this document

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
DLAM	Defense Logistics Agency Land and Maritime
DNU	do not use
ECC	error correcting code
EDAC	error detection and correction
I/O	input/output
LET	linear energy transfer
$\overline{OE}$	output enable
QML	qualified manufacturers list
SEC-DED	single error correction – double error detection
SEL	single-event latch-up
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

16 Document conventions

16.1 Units of measure

Table 13 Units of measure

Symbol	Unit of measure
°C	degree celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

17 Glossary

Table 14 Glossary

Total dose	Permanent device damage due to ions over device life
Heavy ion	Instantaneous device latch up due to single ion
LET	Linear energy transfer (measured in MeVcm^2)
krad	Unit of measurement to determine device life in radiation environments.
Neutron	Permanent device damage due to energetic neutrons or protons.
Prompt dose	Data loss of permanent device damage due to X-rays and gamma rays < 20 ns
RADSTOP™ technology	Infineon's patented Rad Hard design methodology
QML V	Space level certification from DSCC
DLAM	Defense Logistics Agency Land and Maritime
LSBU	Logical Single Bit Upset; Single bits in a single correction word are in error
LMBU	Logical Multi Bit Upset; Multiple bits in a single correction word are in error

Revision history

Document revision	Date	Description of changes
*C	2025-03-05	Publish to web. Updated package outline title in **Figure 10**. Updated cross-references for note lists in the document. Updated broken hyperlinks.

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