

Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

4-Mbit (512K × 8) Static RAM with RadStop™ Technology

Radiation Performance

Radiation Data

- Total dose = 300 Krad
- Soft error rate (both heavy ion and proton)
Heavy ions $\leq 1 \times 10^{-10}$ upsets/bit-day with single-error correction, double error detection and correction (SEC-DED EDAC)
- Neutron = 2.0×10^{14} N/cm²
- Dose rate $\geq 2.0 \times 10^9$ (rad(Si)/s)
- Latch up immunity LET = 120 MeV.cm²/mg (125 °C)

Processing Flows

- V Grade - Class V flow in compliance with MIL-PRF 38535

Prototyping Options

- CYPT1049DV33 prototype units with same functional and timing as flight units using non-radiation hardened die in a 36-pin ceramic flat package

Features

- Temperature ranges
 - Military/Space: -55 °C to 125 °C
- High speed
 - $t_{AA} = 12$ ns
- Low active power
 - $I_{CC} = 95$ mA at 12 ns ($P_{MAX} = 315$ mW)
- Low CMOS standby power
 - $I_{SB2} = 15$ mA
- 2.0 V data retention
- Automatic power-down when deselected

- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Gold plated leads 36-pin ceramic flat package

Functional Description

The CYRS1049DV33 is a high-performance complementary metal oxide semiconductor (CMOS) static RAM organized as 512K words by 8 bits with RadStop™ technology. Cypress' state-of-the-art RadStop technology is radiation hardened through proprietary design and process hardening techniques. The 4-Mbit fast asynchronous SRAM with RadStop technology is also QML V certified with Defense Logistics Agency Land and Maritime (DLAM).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See the [Truth Table on page 12](#) for a complete description of read and write modes.

The eight input or output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CYRS1049DV33 is available in a ceramic 36-pin Flat package with center power and ground (revolutionary) pinout.

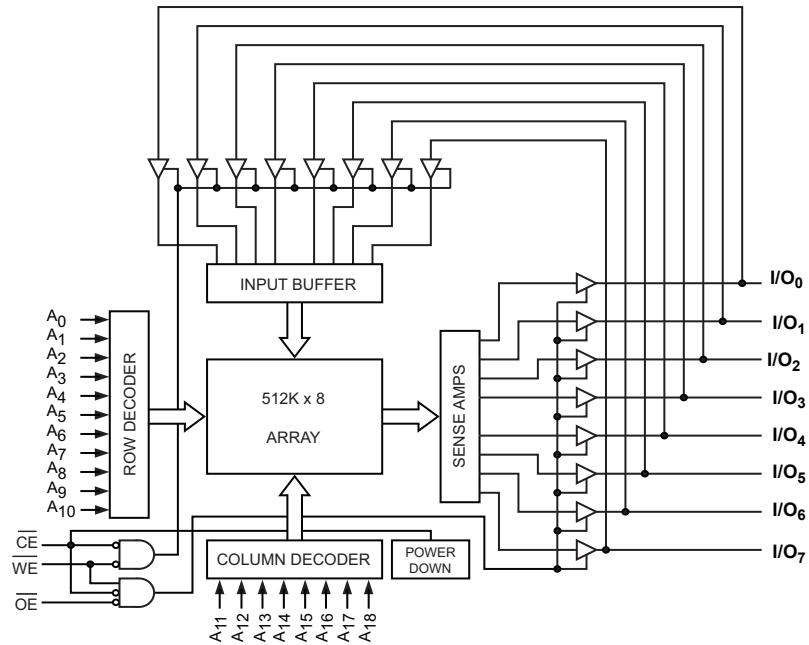
Easy memory expansion is provided by utilizing \overline{OE} , \overline{CE} , and tri-state drivers.

For a complete list of related documentation, [click here](#).

Selection Guide

Description	Military/Space	Unit
Maximum access time	12	ns
Maximum operating current	95	mA
Maximum CMOS standby current	15	mA

Logic Block Diagram



Contents

Pin Configuration	4	Package Diagram	14
Maximum Ratings	5	Acronyms	15
Operating Range	5	Document Conventions	15
DC Electrical Characteristics	5	Units of Measure	15
Capacitance	6	Glossary	15
Thermal Resistance	6	Document History Page	16
AC Test Loads and Waveforms	6	Sales, Solutions, and Legal Information	18
Data Retention Characteristics	7	Worldwide Sales and Design Support	18
Data Retention Waveform	7	Products	18
AC Switching Characteristics	8	PSoC® Solutions	18
Switching Waveforms	9	Cypress Developer Community	18
Truth Table	12	Technical Support	18
Ordering Information	13		
Ordering Code Definitions	13		

Pin Configuration

Figure 1. 36-pin Ceramic Flat Package pinout (Top View) ^[1]

A ₀	1	36	NC
A ₁	2	35	A ₁₈
A ₂	3	34	A ₁₇
A ₃	4	33	A ₁₆
A ₄	5	32	A ₁₅
CE	6	31	OE
IO ₀	7	30	IO ₇
IO ₁	8	29	IO ₆
V _{CC}	9	28	GND
GND	10	27	V _{CC}
IO ₂	11	26	IO ₅
IO ₃	12	25	IO ₄
WE	13	24	A ₁₄
A ₅	14	23	A ₁₃
A ₆	15	22	A ₁₂
A ₇	16	21	A ₁₁
A ₈	17	20	A ₁₀
A ₉	18	19	DNU

Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND ^[2] -0.3 V to +4.6 V

DC voltage applied to outputs in High Z state ^[2] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Military/Space	-55 °C to +125 °C	3.3 V ± 0.3 V	12 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Military/Space		Unit
			Min	Max	
V_{OH}	Output high voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	–	V
V_{OL}	Output low voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	–	0.4	V
V_{IH} ^[2]	Input high voltage		2.0	$V_{CC} + 0.3$	V
V_{IL} ^[2]	Input low voltage		-0.3	0.8	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, output disabled	-1	+1	μA
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$			
		83 MHz	–	95	mA
		66 MHz	–	85	mA
		40 MHz	–	75	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	–	15	mA

Note

2. $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

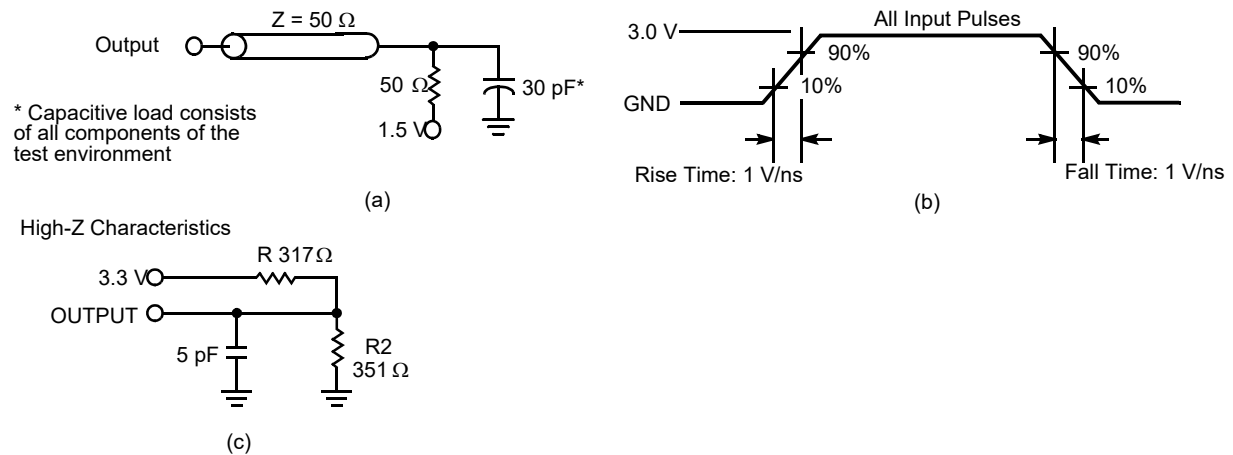
Parameter ^[3]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	I/O capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	Ceramic Flat Package	Unit
Θ _{JC}	Thermal resistance (junction to case)	Test according to MIL-PRF 38538	3.6	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

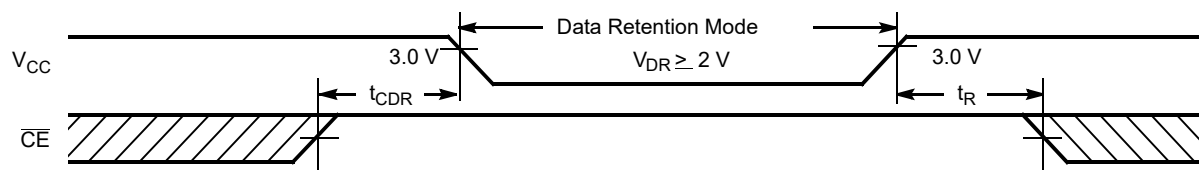
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions ^[5]	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	15	mA
$t_{CDR}^{[6]}$	Chip deselect to data retention time	–	0	–	ns
$t_R^{[7]}$	Operation recovery time	–	12	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

5. No input may exceed $V_{CC} + 0.3\text{ V}$.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 50\text{ }\mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	Military/Space		Unit
		Min	Max	
Read Cycle				
t _{power} ^[9]	V _{CC} (typical) to the first access	100	–	μs
t _{RC}	Read cycle time	12	–	ns
t _{AA}	Address to data valid	–	12	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[10]	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[10, 11]	–	6	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[10]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[10, 11]	–	6	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-up	0	–	ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-down	–	12	ns
Write Cycle ^[12, 13]				
t _{WC}	Write cycle time	12	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	8	–	ns
t _{AW}	Address setup to write end	8	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	WE pulse width	8	–	ns
t _{SD}	Data setup to write end	6	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[10]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[10, 11]	–	6	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of [Figure 2 on page 6](#). Transition is measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write and the transition of either of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 4 (WE Controlled, OE LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 [14, 15]

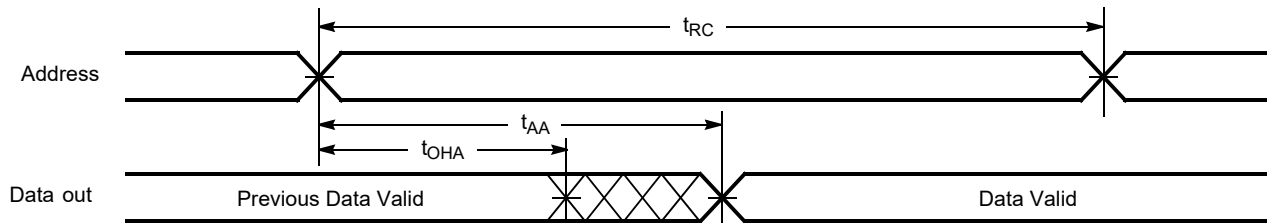
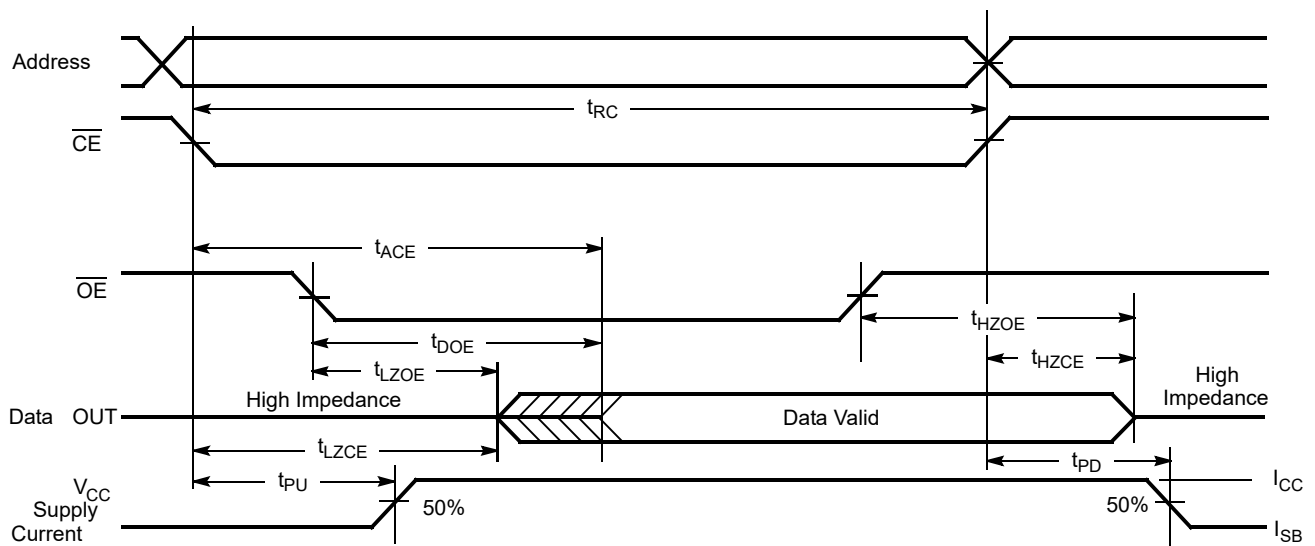


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]



Notes

14. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.

15. \overline{WE} is HIGH for read cycle.

16. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [17, 18]

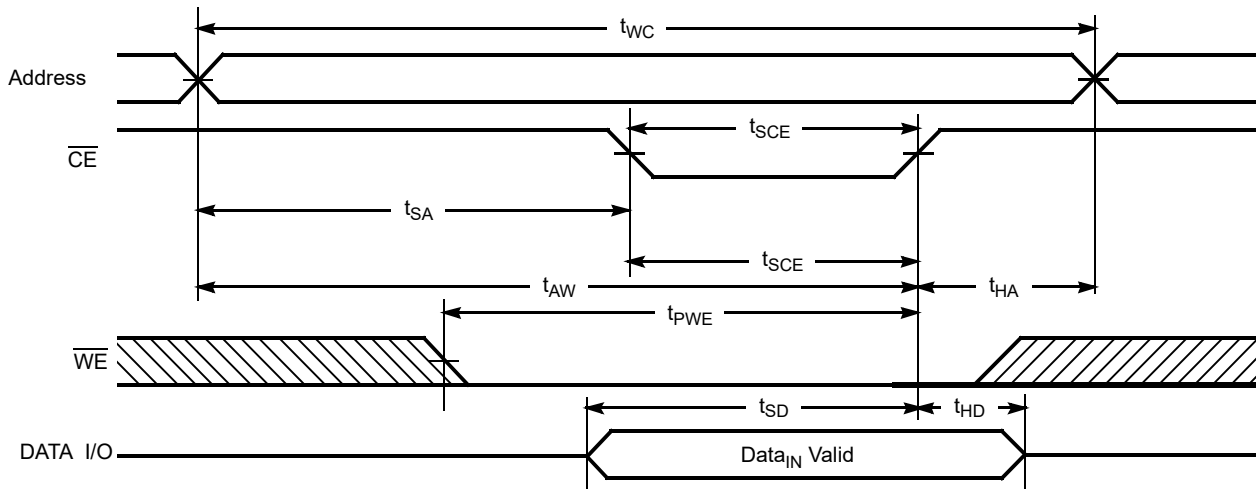
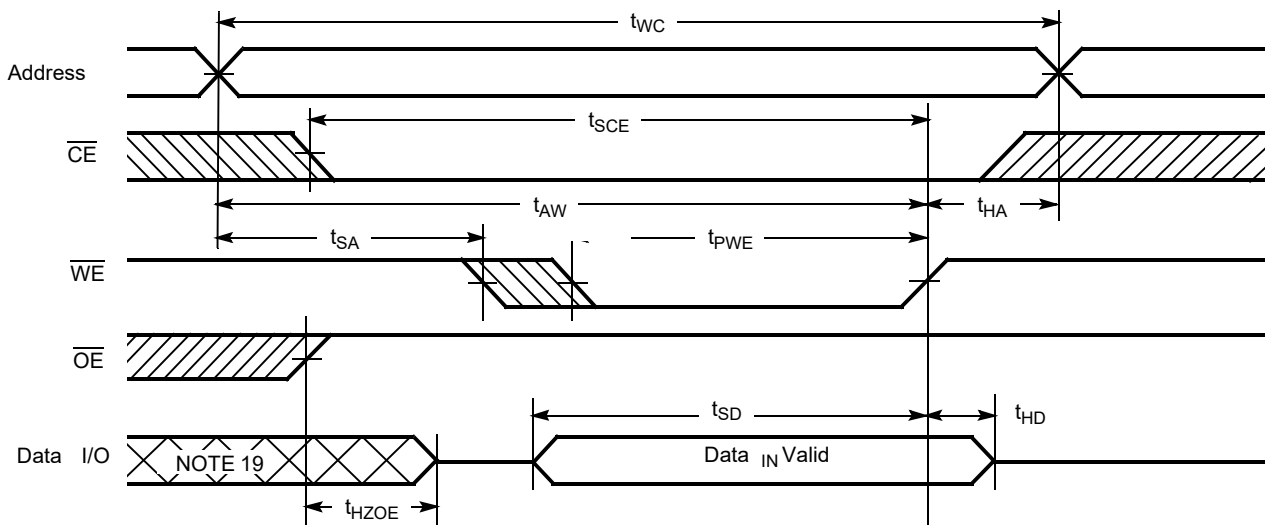


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write) [17, 18]



Notes

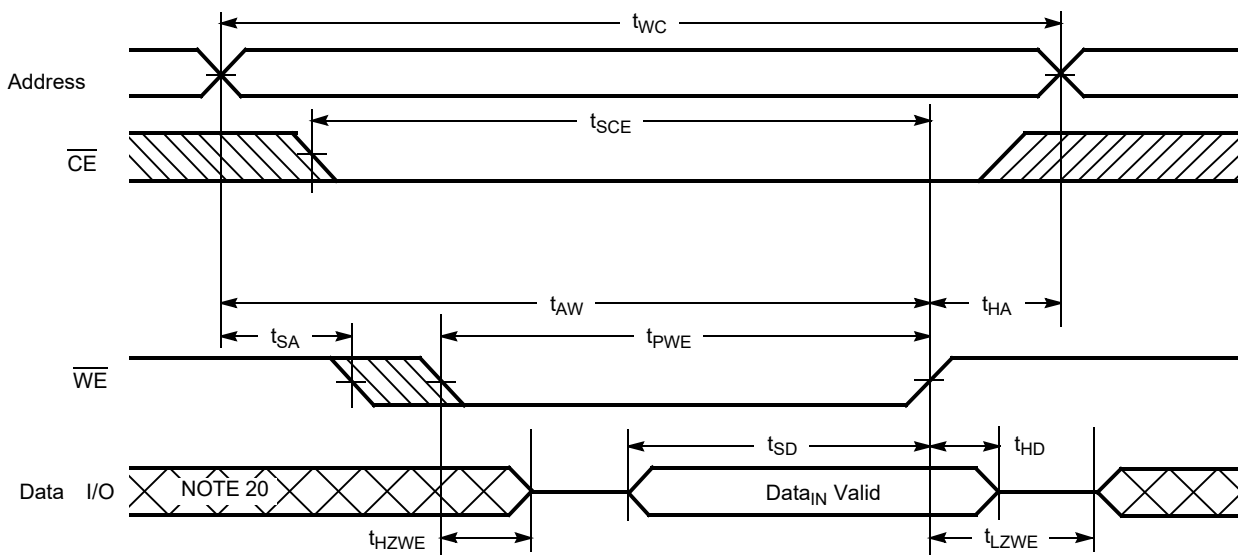
17. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$

18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



Note

20. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O ₀ –I/O ₇	Mode	Power
H	X	X	High Z	Power-down	Standby (I _{SB1} or I _{SB2})
L	L	H	Data out	Read	Active (I _{CC})
L	X	L	Data in	Write	Active (I _{CC})
L	H	H	High Z	Selected, Outputs disabled	Active (I _{CC})

Ordering Information

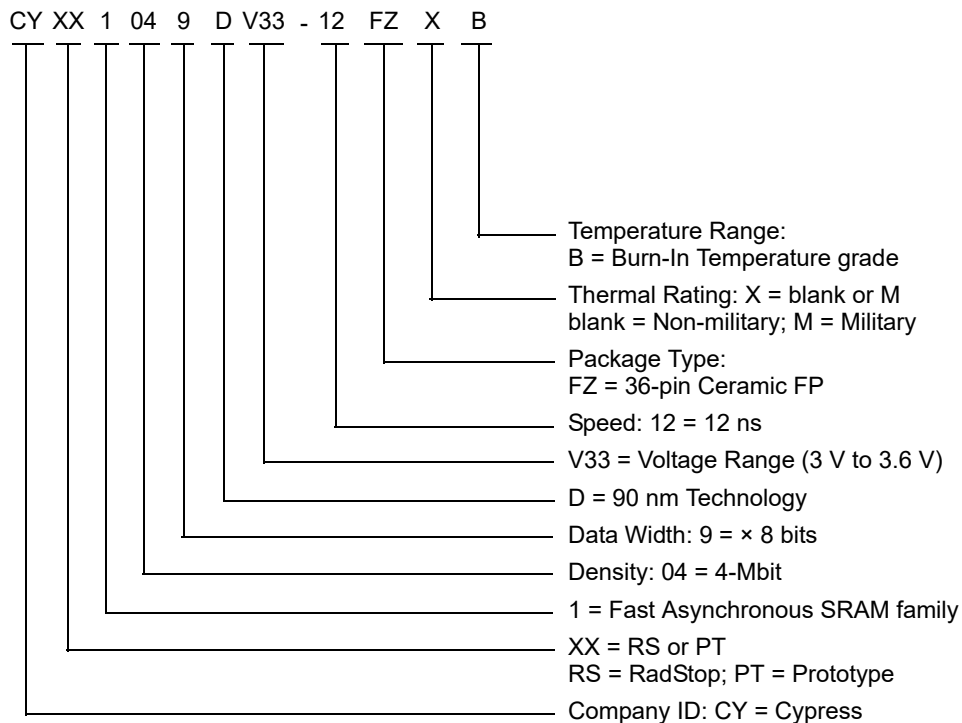
The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CYRS1049DV33-12FZMB	001-67583	36-pin ceramic flat package	Burn-In
12	CYPT1049DV33-12FZMB	001-67583	36-pin ceramic flat package, Prototype part	Burn-In
12	5962F1123501VXC	001-67583	36-pin ceramic flat package, DLAM part	Burn-In

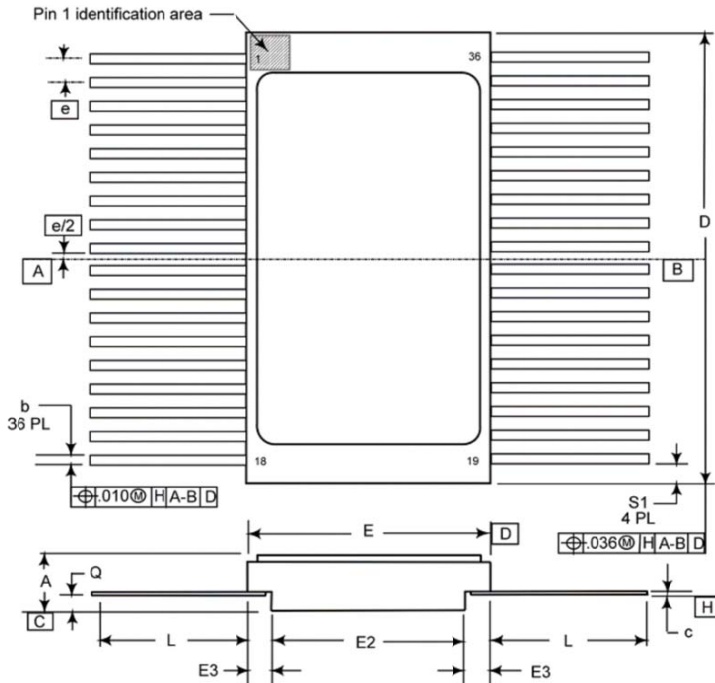
Contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



Package Diagram

Figure 9. 36-pin Ceramic Flat Pack (Solder Seal Lid) Package Outline, 001-67583



Case outline X

SYMBOL	Millimeters		Inches	
	Min	Max	Min	Max
A	2.40	2.99	0.094	0.118
b	0.38	0.48	0.015	0.019
c	0.102	0.152	0.004	0.006
D	23.12	23.62	0.910	0.930
E	11.99	12.39	0.472	0.488
E2	9.96	10.36	0.392	0.408
E3	0.082	1.22	0.003	0.048
e	1.19	1.35	0.047	0.053
L	10.19	10.64	0.401	0.419
Q	0.64	---	0.025	---
S1	0.13	---	0.51	---

NOTES:

1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The sealing and lid are not electrically connected to V_{SS} (isolated).
4. Lead finish is in accordance with MIL-PRF-38535.
5. Package material: opaque 90% minimum Alumina ceramic.

001-67583 *C

Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
DLAM	Defense Logistics Agency Land and Maritime
DNU	Do Not Use
EDAC	Error Detection and Correction
I/O	Input/Output
LET	Linear Energy Transfer
\overline{OE}	Output Enable
QML	Qualified Manufacturers List
SEC-DED	Single Error Correction – Double Error Detection
SEL	Single-Event Latch-up
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Glossary

Total Dose	Permanent device damage due to ions over device life
Heavy Ion	Instantaneous device latch up due to single ion
LET	Linear energy transfer (measured in MeVcm ²)
Krad	Unit of measurement to determine device life in radiation environments.
Neutron	Permanent device damage due to energetic neutrons or protons
Prompt Dose	Data loss of permanent device damage due to X-rays and gamma rays < 20 ns
RadStop Technology	Cypress's patented Rad Hard design methodology
QML V	Space level certification from DSCC.
DLAM	Defense Logistics Agency Land and Maritime
LSBU	Logical Single Bit Upset. Single bits in a single correction word are in error.
LMBU	Logical Multi Bit Upset. Multiple bits in a single correction word are in error

Document History Page

Document Title: CYRS1049DV33, 4-Mbit (512K × 8) Static RAM with RadStop™ Technology Document Number: 001-64292				
Rev.	ECN No.	Origin of Change	Submission Date	Description of Change
**	3098986	HRP	12/01/2010	New data sheet.
*A	3181475	PRAS	02/24/2011	Updated Package Diagram : Removed spec 001-64294 **. Added spec 001-67583 **.
*B	3438781	HRP	11/14/2011	Updated Package Diagram : spec 001-67583 – Changed revision from ** to *A.
*C	3554946	HRP	03/19/2012	Changed status from Preliminary to Final. Updated Radiation Performance : Updated Radiation Data : Updated description. Updated Prototyping Options : Updated description. Updated Features : Added "(P _{MAX} = 315 mW)" under "Low active power". Updated Functional Description : Added "Easy memory expansion is provided by utilizing \overline{OE} , \overline{CE} , and tri-state drivers." as a new paragraph. Updated Maximum Ratings : Updated details corresponding to "DC voltage applied to outputs in High Z state" and "DC input voltage". Updated AC Switching Characteristics : Changed the maximum value of t _{DOE} parameter from 7 ns to 6 ns. Updated Ordering Information : Updated part numbers.
*D	3887928	HRP	02/07/2013	Updated Radiation Performance : Updated Processing Flows : Replaced "V grade - Class V flow" with "Q grade - Class Q flow". Updated Prototyping Options : Added "Non-radiation hard" in the starting, replaced "V grade" with "Q grade". Updated Ordering Information : Updated part numbers.
*E	4208547	VINI	12/03/2013	Updated Radiation Performance : Updated Processing Flows : Added "V Grade - Class V flow in compliance with MIL-PRF 38535". Updated Prototyping Options : Updated first bullet as "CYPT1049DV33 protos with same functional and timing as flight units using non-radiation hardened die". Updated Ordering Information : Updated part numbers. Updated Package Diagram : spec 001-67583 – Changed revision from *A to *B. Updated to new template. Completing Sunset Review.
*F	4571914	VINI	11/17/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagram : spec 001-67583 – Changed revision from *B to *C. Completing Sunset Review.
*G	5966687	AESATMP8	11/14/2017	Updated Cypress Logo and Copyright.

Document History Page(continued)

Document Title: CYRS1049DV33, 4-Mbit (512K × 8) Static RAM with RadStop™ Technology Document Number: 001-64292				
Rev.	ECN No.	Origin of Change	Submission Date	Description of Change
*H	6103500	HRP	03/20/2018	Updated Ordering Information : Updated part numbers. Updated Functional Description : Updated hyperlink corresponding to "SRAM Board Design Guidelines". Updated to new template.
*I	6171033	HRP	05/16/2018	Updated Radiation Performance : Updated Processing Flows : Removed "Q Grade - Class Q flow in compliance with MIL-PRF 38535". Updated Features : Replaced "Pb-free 36-pin ceramic flat package" with "Gold plated leads 36-pin ceramic flat package".
*J	6594630	HRP	06/13/2019	Updated Functional Description : Removed "For best practice recommendations, refer to the Cypress application note AN1064 , SRAM System Guidelines ." (as AN1064 is obsolete). Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2010–2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.