

# 256 Mb pseudoSRAM (pSRAM) self-refresh dynamic RAM (DRAM) with Octal xSPI interface

**1.8 V**

## Features

- Encapsulated plastic component for low-Earth orbit satellite applications
- Interface
  - xSPI (Octal) interface
  - 1.8 V interface support
    - Single ended clock (CK) - 11 bus signals
    - Optional differential clock (CK, CK#) - 12 bus signals
  - Chip select (CS#)
  - 8-bit data bus (DQ[7:0])
  - Hardware reset (RESET#)
  - Bidirectional read-write data strobe (RWDS)
    - Output at the start of all transactions to indicate refresh latency
    - Output during read transactions as read data strobe
    - Input during write transactions as write data mask
- Performance, power, and packages
  - 200 MHz maximum clock rate
  - DDR - transfers data on both edges of the clock
  - Data throughput up to 400 MBps (3,200 Mbps)
  - Configurable burst characteristics
    - Linear burst
    - Wrapped burst lengths:
      - 16 bytes (8 clocks)
      - 32 bytes (16 clocks)
      - 64 bytes (32 clocks)
      - 128 bytes (64 clocks)
    - Hybrid option - one wrapped burst followed by linear burst
  - Configurable output drive strength
  - Power modes
    - Hybrid sleep mode
    - Deep power down
  - Array refresh
    - Partial memory array (1/8, 1/4, 1/2, and so on)
    - Full
  - Package
    - 24-ball FBGA
  - Operating temperature range
    - Extended: -40°C to +125°C
- Guaranteed TID radiation performance of 100 krad
- Single event latchup immunity >58LET (125°C)
- Single lot date code and 100% guaranteed electrical testing

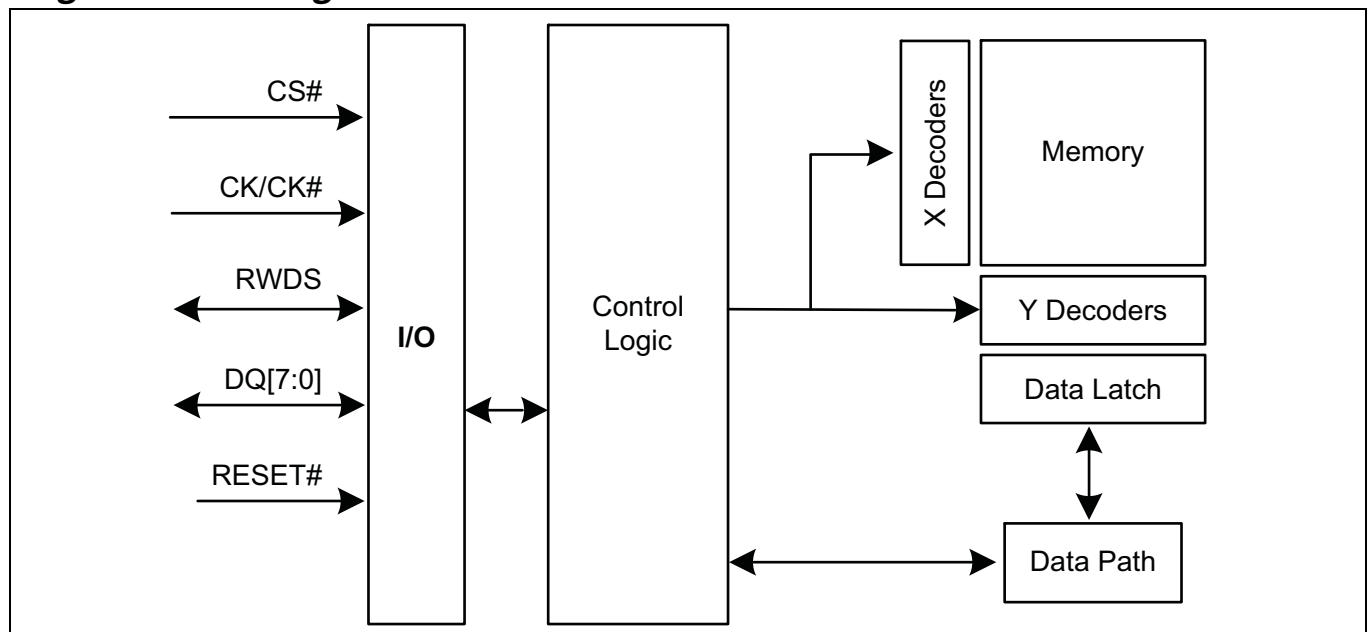
## Performance summary

- Technology
  - 25-nm DRAM

## Performance summary

Read transaction timings	Unit
Maximum clock rate at 1.8 V $V_{CC}/V_{CCQ}$	200 MHz
Maximum access time ( $t_{ACC}$ )	35 ns
Maximum current consumption	Unit
Burst read/write (linear burst at 200 MHz)	22 mA/25 mA
Standby	2 mA
Deep power down	20 $\mu$ A

## Logic block diagram



## Table of contents

<b>Features .....</b>	<b>1</b>
<b>Performance summary .....</b>	<b>2</b>
<b>Logic block diagram .....</b>	<b>2</b>
<b>Table of contents .....</b>	<b>3</b>
<b>1 Introduction .....</b>	<b>5</b>
1.1 xSPI (Octal) interface .....	5
<b>2 Product overview .....</b>	<b>8</b>
2.1 xSPI (Octal) interface .....	8
<b>3 Signal description .....</b>	<b>9</b>
3.1 Input/output summary .....	9
<b>4 xSPI (Octal) transaction details .....</b>	<b>10</b>
4.1 Command/address/data bit assignments .....	11
4.2 RESET ENABLE transaction .....	12
4.3 RESET transaction .....	12
4.4 READ ID transaction .....	13
4.5 DEEP POWER DOWN transaction .....	14
4.6 READ transaction .....	15
4.7 WRITE transaction .....	16
4.8 WRITE ENABLE transaction .....	17
4.9 WRITE DISABLE transaction .....	17
4.10 READ ANY REGISTER transaction .....	17
4.11 WRITE ANY REGISTER transaction .....	18
4.12 Data placement during memory READ/WRITE transactions .....	19
4.13 Data placement during register READ/WRITE transactions .....	20
<b>5 Memory space .....</b>	<b>21</b>
5.1 xSPI (Octal) interface .....	21
5.2 Density and row boundaries .....	21
<b>6 Register space access .....</b>	<b>22</b>
6.1 xSPI (Octal) interface .....	22
6.2 Device identification registers .....	22
6.3 Device configuration registers .....	23
6.3.1 Configuration register 0 (CR0) .....	23
6.3.2 Configuration register 1 .....	26
<b>7 Interface states .....</b>	<b>28</b>
<b>8 Power conservation modes .....</b>	<b>29</b>
8.1 Interface standby .....	29
8.2 Active clock stop .....	29
8.3 Hybrid sleep .....	29
8.4 Deep power down .....	30
<b>9 Electrical specifications .....</b>	<b>31</b>
9.1 Absolute maximum ratings .....	31
9.2 Input signal overshoot .....	31
9.3 Latch-up characteristics .....	32
9.4 Operating ranges .....	32
9.4.1 Temperature ranges .....	32
9.4.2 Power supply voltages .....	32
9.5 DC characteristics .....	33
9.5.1 Capacitance characteristics .....	35
9.6 Power-up initialization .....	36
9.7 Power down .....	37
9.8 Hardware reset .....	38



Table of contents

**10 Timing specifications .....39**  
10.1 Key to switching waveforms.....39  
10.2 AC test conditions .....39  
10.3 CLK characteristics .....40  
10.4 AC characteristics.....41  
10.4.1 Read transactions .....41  
10.4.2 Write transactions.....42  
10.5 Timing reference levels.....44  
**11 Physical interface .....45**  
11.1 FBGA 24-ball 5 x 5 array footprint .....45  
11.2 Package diagram .....46  
**12 Ordering information .....47**  
12.1 Ordering code definitions.....47  
**13 Acronyms .....48**  
**14 Document conventions.....49**  
14.1 Units of measure .....49  
**Revision history .....50**

## 1 Introduction

The 256 Mb pSRAM device is a high-speed CMOS, self-refresh DRAM, with xSPI (Octal) interface. The DRAM array uses dynamic cells that require periodic refresh. Refresh control logic within the device manages the refresh operations on the DRAM array when the memory is not being actively read or written by the xSPI interface master (host). Since the host is not required to manage any refresh operations, the DRAM array appears to the host as though the memory uses static cells that retain data without refresh. Hence, the memory is more accurately described as pseudo static RAM (PSRAM).

Since the DRAM cells cannot be refreshed during a read or write transaction, there is a requirement that the host limit read or write burst transfers lengths to allow internal logic refresh operations when they are needed. The host must confine the duration of transactions and allow additional initial access latency, at the beginning of a new transaction, if the memory indicates a refresh operation is needed.

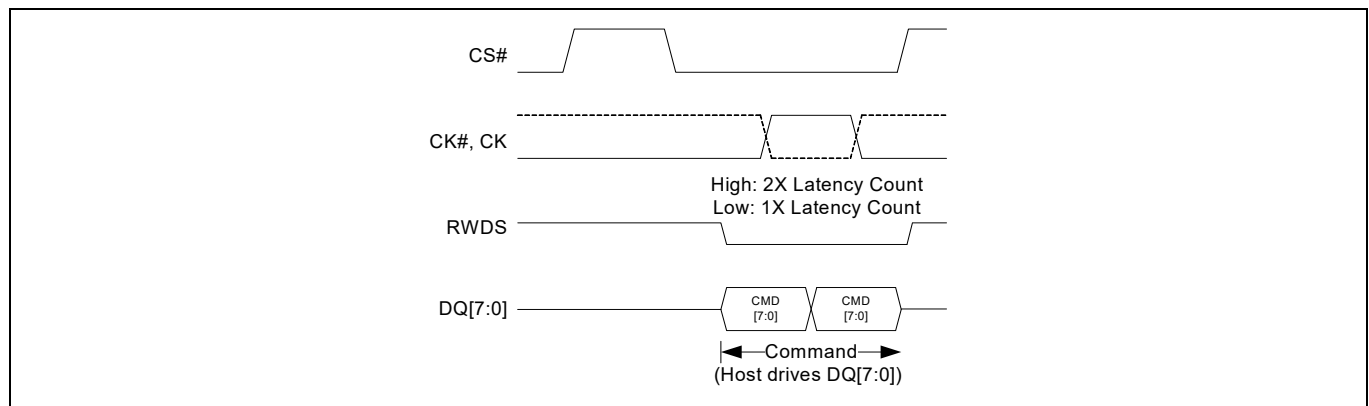
### 1.1 xSPI (Octal) interface

xSPI (Octal) is a SPI-compatible low signal count, DDR interface supporting eight I/Os. The DDR protocol in xSPI (Octal) transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on xSPI (Octal) consists of a series of 16-bit wide, one clock cycle data transfers at the internal RAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible. Device are available as 1.8 V  $V_{CC}/V_{CCQ}$  (nominal) for array ( $V_{CC}$ ) and I/O buffer ( $V_{CCQ}$ ) supplies, through different ordering part number (OPN).

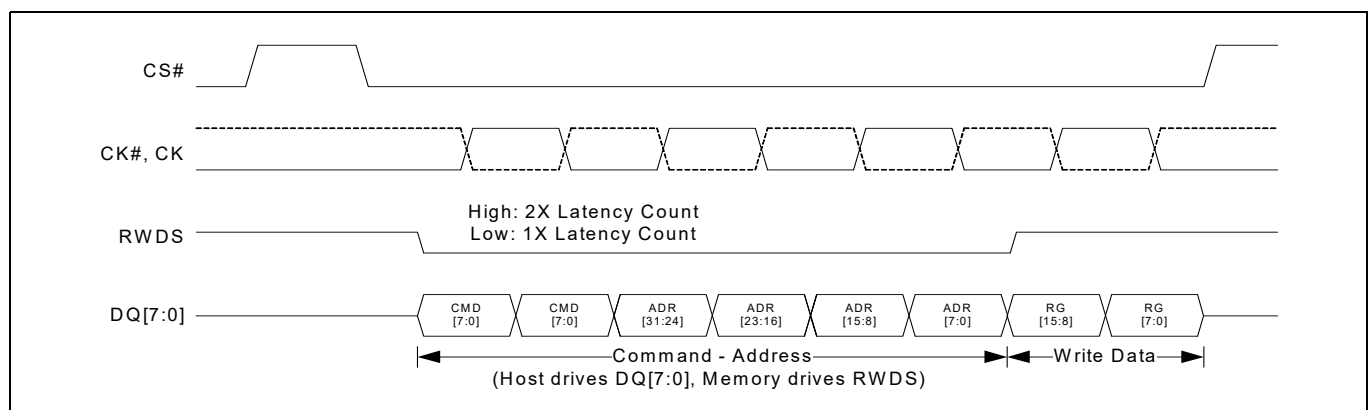
Each transaction on xSPI (Octal) must include a command whereas address and data are optional. The transactions are structures as follows:

- Each transaction begins with CS# going LOW and ends with CS# returning HIGH.
- The serial clock (CK) marks the transfer of each bit or group of bits between the host and memory. All transfers occur on every CK edge (DDR mode).
- Each transaction has a 16-bit command which selects the type of device operation to perform. The 16-bit command is based on two 8-bit opcodes. The same 8-bit opcode is sent on both edges of the clock.
- A command may be stand-alone or may be followed by address bits to select a memory location in the device to access data.
- Read transactions require a latency period after the address bits and can be zero to several CK cycles. CK must continue to toggle during any read transaction latency period. During the command and address parts of a transaction, the memory can indicate whether an additional latency period is needed for a required refresh time ( $t_{RFH}$ ) which is added to the initial latency period; by driving the RWDS signal to the HIGH state.
- Write transactions to registers do not require a latency period.
- Write transactions to the memory array require a latency period after the address bits and can be zero to several CK cycles. CK must continue to toggle during any write transaction latency period. During the command and address parts of a transaction, the memory can indicate whether an additional latency period is needed for a required refresh time ( $t_{RFH}$ ) which is added to the initial latency period by driving the RWDS signal to the HIGH state.
- In all transactions, command and address bits are shifted in the device with the most significant bits (MSb) first. The individual data bits within a data byte are shifted in and out of the device MSb first as well. All data bytes are transferred with the lowest address byte sent out first.

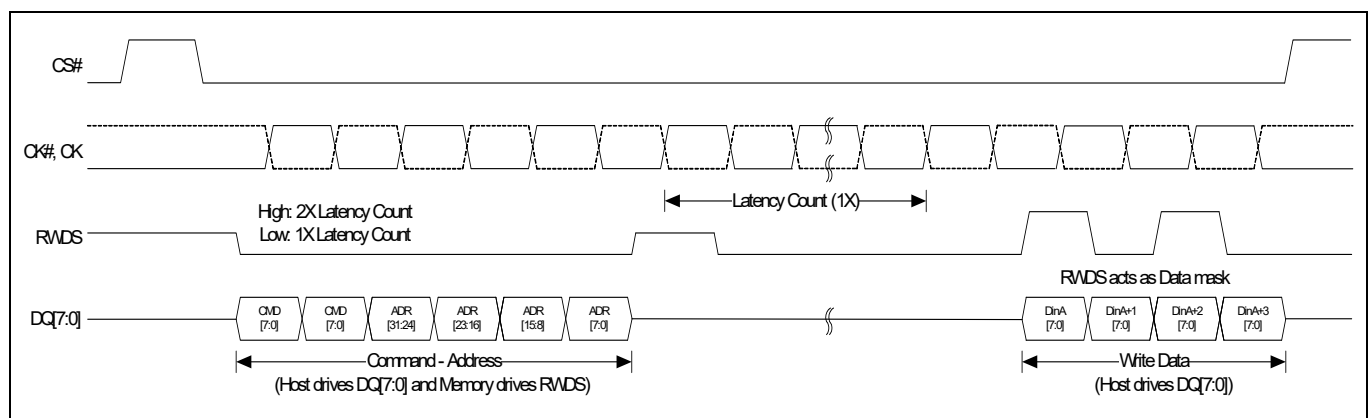
## Introduction



**Figure 1 xSPI (Octal) command only transaction (DDR)**



**Figure 2 xSPI (Octal) write with no latency transaction (DDR) (Register writes)<sup>[1]</sup>**

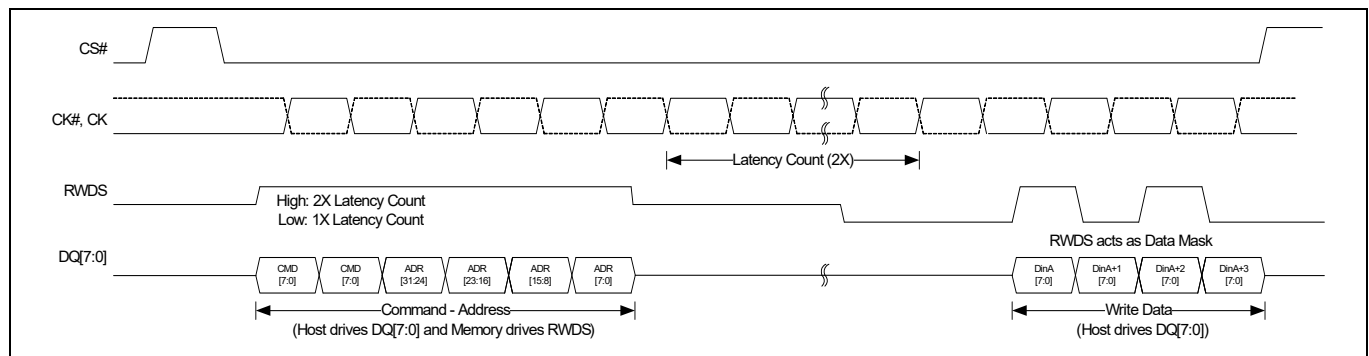


**Figure 3 xSPI (Octal) write with 1X latency transaction (DDR) (Memory array writes)<sup>[2, 3]</sup>**

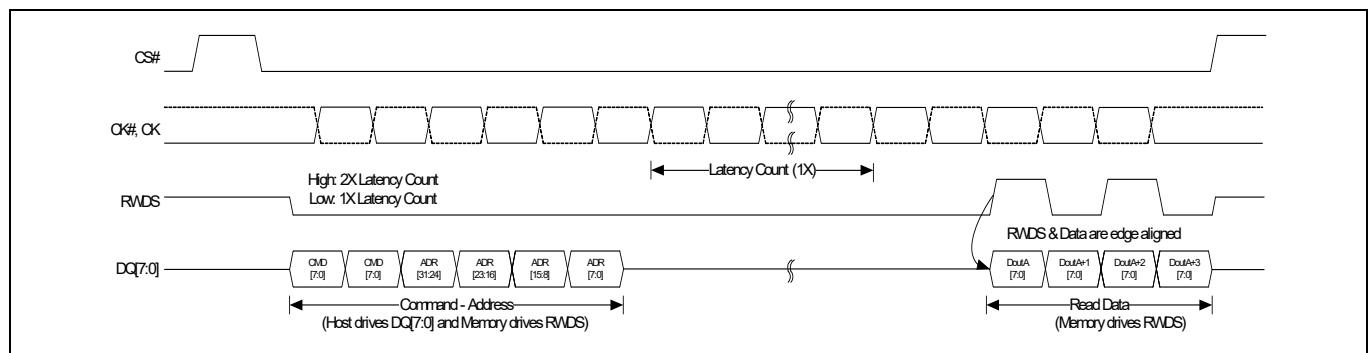
### Notes

1. Write with no latency transaction is used for register writes only.
2. RWDS driven by the host.
3. Data DinA and DinA+2 are masked.

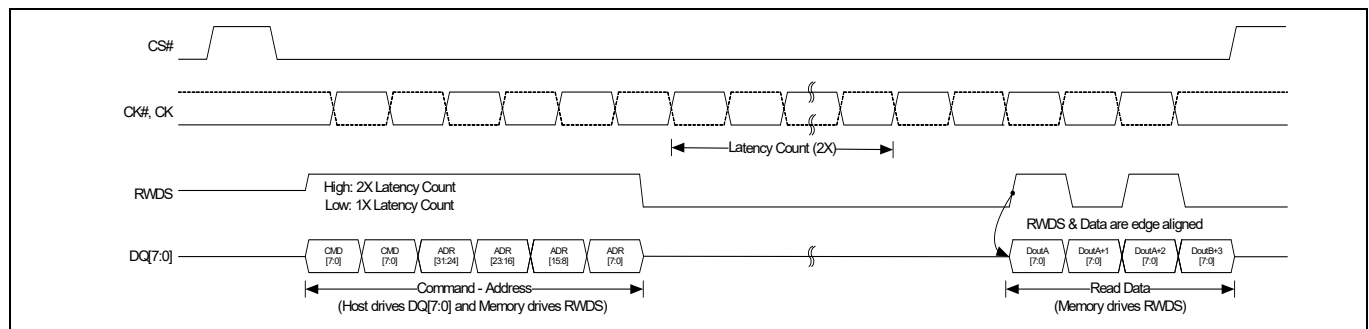
## Introduction



**Figure 4** xSPI (Octal) write with 2X latency transaction (DDR) (Memory array writes)<sup>[4, 5]</sup>



**Figure 5** xSPI (Octal) read with 1X latency transaction (DDR) (All reads)<sup>[6]</sup>



**Figure 6** xSPI (Octal) read with 2X latency transaction (DDR) (All reads)<sup>[7]</sup>

## Notes

4. RWDS driven by pSRAM during command & address cycles for 2X latency and then driven by the host for data masking.
5. Data DinA and DinA+2 are masked.
6. RWDS is driven by pSRAM phase aligned with data.
7. RWDS is driven by pSRAM during command & address cycles for 2X latency and then driven again phase aligned with data.

## 2 Product overview

The 256 Mb pSRAM device is 1.8 V array and I/O, synchronous self-refresh dynamic RAM (DRAM). The pSRAM device provides an xSPI (Octal) slave interface to the host system. The xSPI (Octal) interface has an 8-bit (1 byte) wide DDR data bus and use only word-wide (16-bit data) address boundaries. Read transactions provide 16 bits of data during each clock cycle (8 bits on both clock edges). Write transactions take 16 bits of data from each clock cycle (8 bits on each clock edge).

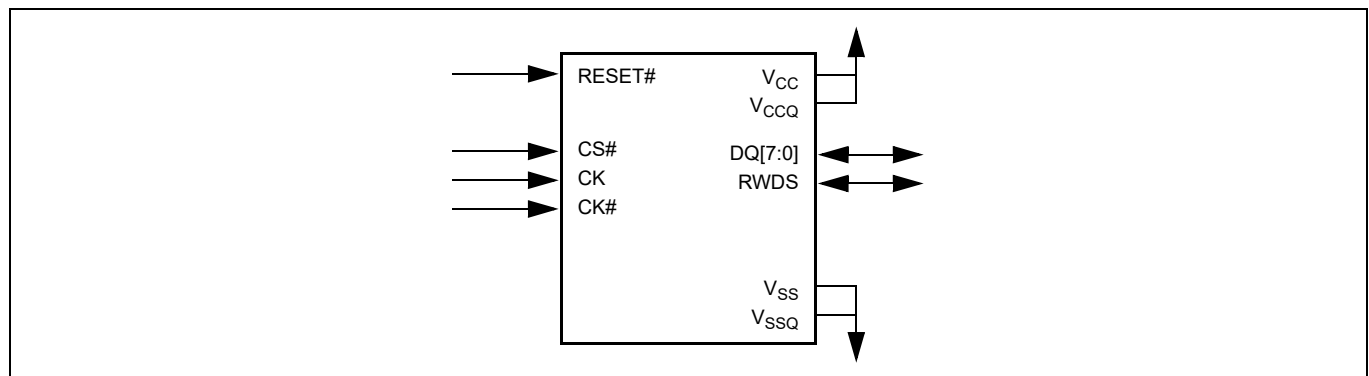


Figure 7 xSPI (Octal) pSRAM interface<sup>[8]</sup>

### 2.1 xSPI (Octal) interface

Read and write transactions require three clock cycles to define the target row/column address and then an initial access latency of  $t_{ACC}$ . During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time ( $t_{RFH}$ ) is added to the initial latency; by driving the RWDS signal to the HIGH state. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequence. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation that can provide a sustained data rate of 400 MBps (1 byte (8 bit data bus) \* 2 (data clock edges) \* 200 MHz = 400 MBps).

#### Note

8. CK# is used in differential clock mode, but optional.

## Signal description

### 3 Signal description

#### 3.1 Input/output summary

The xSPI (Octal) pSRAM signals are shown in [Table 1](#). The active low signal names have a hash symbol (#) suffix.

**Table 1** I/O summary

Symbol	Type	Description
CS#	Input	<b>Chip select.</b> Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave.
CK, CK#[9]	Input	<b>Differential clock.</b> Command, address, and data information is output with respect to the crossing of the CK and CK# signals. Use of differential clock is optional. <b>Single ended clock.</b> CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
DQ[7:0]	Input/output	<b>Data input/output.</b> Command, address, and data information is transferred on these signals during read and write transactions.
RWDS	Input/output	<b>Read-write data strobe.</b> During the command/address portion of all bus transactions RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge-aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. (HIGH = additional latency, LOW = no additional latency).
RESET#	Input, internal pull-up	<b>Hardware RESET.</b> When LOW, the slave device will self initialize and return to the standby state. RWDS and DQ[7:0] are placed into the HIGH-Z state when RESET# is LOW. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the HIGH state.
V <sub>CC</sub>	Power supply	<b>Array power</b>
V <sub>CCQ</sub>	Power supply	<b>Input/output power</b>
V <sub>SS</sub>	Power supply	<b>Array ground</b>
V <sub>SSQ</sub>	Power supply	<b>Input/output ground</b>
RFU	No connect	<b>Reserved for future use.</b> May or may not be connected internally, the signal/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The signal/ball may be used by a signal in the future.

#### Note

9. CK# is used in differential clock mode, but optional connection. Tie the CK# input pin to either V<sub>CCQ</sub> or V<sub>SSQ</sub> if not connected to the host controller, but do not leave it floating.

## **4 xSPI (Octal) transaction details**

The xSPI (Octal) master begins a transaction by driving CS# LOW while clock is idle. Then the clock begins toggling while CA words are transferred.

For memory read and write transactions, the xSPI (Octal) master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0 (Register write transactions do not require any latency count). The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is LOW during the CA cycles, one latency count is inserted. If RWDS is HIGH during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the RWDS and output the target data.

During the read data transfers, read data is output edge-aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is LOW. Note that burst transactions should not be so long as to prevent the memory from doing distributed refreshes.

During the write data transfers, write data is center-aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK. RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is HIGH the byte will be masked and the array will not be altered. When data is being written and RWDS is LOW the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the pSRAM device are able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Read transfers can be ended at any time by bringing CS# HIGH when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is HIGH.

## xSPI (Octal) transaction details

## 4.1 Command/address/data bit assignments

Table 2 Command set<sup>[10-14]</sup>

Command	Code	CA-Data	Address (bytes)	Latency cycles	Data (bytes)	Prerequisite
<b>Software reset</b>						
REST ENABLE	0x66	8-0-0	0	0	0	
RESET	0x99	8-0-0	0	0	0	RESET ENABLE
<b>Identification</b>						
READ ID <sup>[10]</sup>	0x9F	8-8-8	4 (0x00)	3-7	4	
<b>Power modes</b>						
DEEP POWER DOWN	0xB9	8-0-0	0	0	0	
<b>Read memory array</b>						
READ (DDR)	0xEE	8-8-8	4	3-7	1 to ∞	
<b>Write memory array</b>						
WRITE (DDR)	0xDE	8-8-8	4	3-7	1 to ∞	WRITE ENABLE
<b>Write enable / disable</b>						
WRITE ENABLE	0x06	8-0-0	0	0	0	
WRITE DISABLE	0x04	8-0-0	0	0	0	
<b>Read registers</b>						
READ ANY REGISTER	0x65	8-8-8	4	3-7	2	
<b>Write registers</b>						
WRITE ANY REGISTER	0x71	8-8-8	4	0	2	WRITE ENABLE

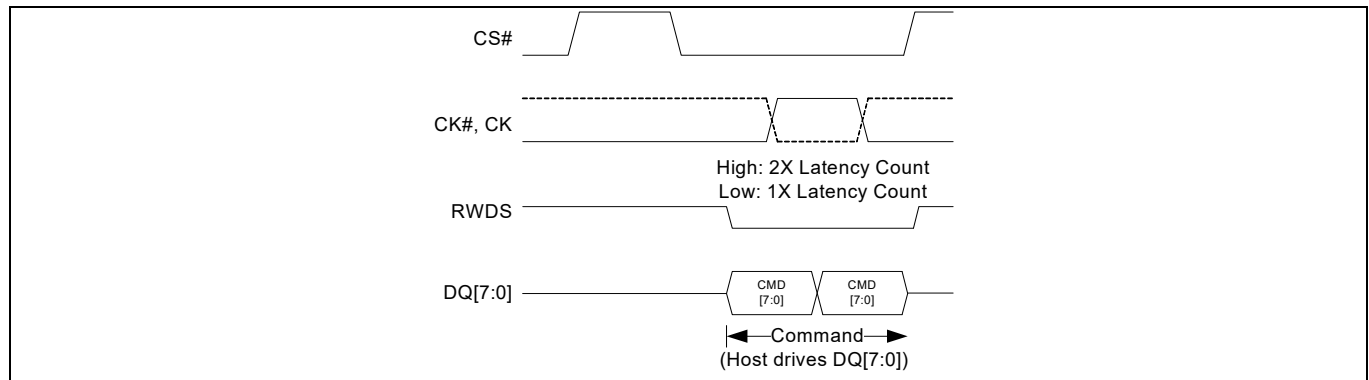
**Notes**

10. The two identification registers contents are read together - identification 0 followed by identification 1.
11. Write enable provides protection against inadvertent changes to memory or register values. It sets the internal write enable latch (WEL) which allows write transactions to execute afterwards.
12. Write disable can be used to disable write transactions from execution. It resets the internal write enable latch (WEL).
13. The WEL latch stays set to '1' at the end of any successful memory write transaction. After a power down / power up sequence, or a hardware/software reset, WEL latch is cleared to '0'.
14. The internal WEL latch is cleared to '0' at the end of any successful register write transaction.

## xSPI (Octal) transaction details

### 4.2 RESET ENABLE transaction

The RESET ENABLE transaction is required immediately before a RESET transaction. Any transaction other than RESET following RESET ENABLE will clear the reset enable condition and prevent a later RESET transaction from being recognized.



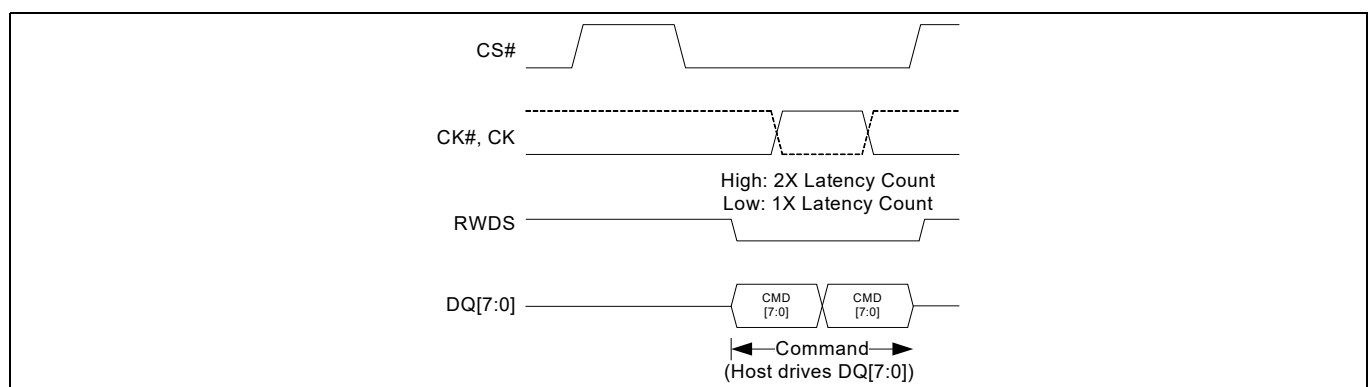
**Figure 8** RESET ENABLE transaction (DDR)

### 4.3 RESET transaction

The RESET transaction immediately following a RESET ENABLE will initiate the software reset process. The software reset provides a software method of returning the device to the standby state. During  $t_{SR}$  (400 ns, max) the device will draw  $I_{CC5}$  current. A software reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation during the software reset process - memory array data is considered invalid

After software reset finishes, the self-refresh operation will resume. Because self-refresh operation is stopped, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval. This may result in the loss of DRAM array data. The host system should consider DRAM array data is lost after software reset and reload any required data.



**Figure 9** RESET transaction (DDR)

## xSPI (Octal) transaction details

### 4.4 READ ID transaction

The READ ID transaction provides read access to device identification registers 0 and 1. The registers contain the manufacturer's identification along with device identification. The read data sequence is as follows.

**Table 3 READ ID data sequence**

Address space	Byte order	Byte position	Word data Bit	DQ
Register 0	Big-endian	A	15	7
			14	6
			13	5
			12	4
			11	3
			10	2
			9	1
			8	0
		B	7	7
			6	6
			5	5
			4	4
			3	3
			2	2
			1	1
			0	0
Register 1	Big-endian	A	15	7
			14	6
			13	5
			12	4
			11	3
			10	2
			9	1
			8	0
		B	7	7
			6	6
			5	5
			4	4
			3	3
			2	2
			1	1
			0	0

## xSPI (Octal) transaction details

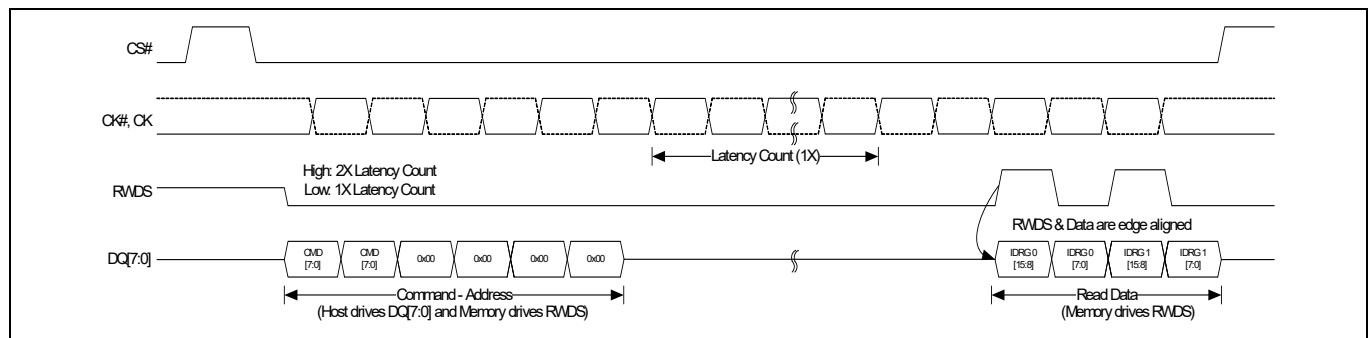


Figure 10 READ ID with 1X latency transaction (DDR)<sup>[15]</sup>

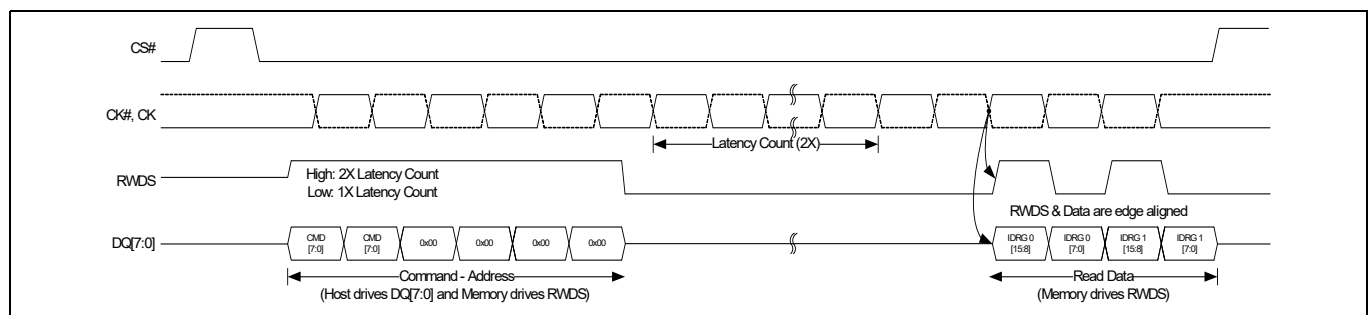


Figure 11 READ ID with 2X latency transaction (DDR)<sup>[16]</sup>

## 4.5 DEEP POWER DOWN transaction

DEEP POWER DOWN transaction brings the device into deep power down state which is the lowest power consumption state. Writing a "0" to CR0[15] will also bring the device in deep power down state. All register contents are lost in deep power down state and the device powers-up in its default state.

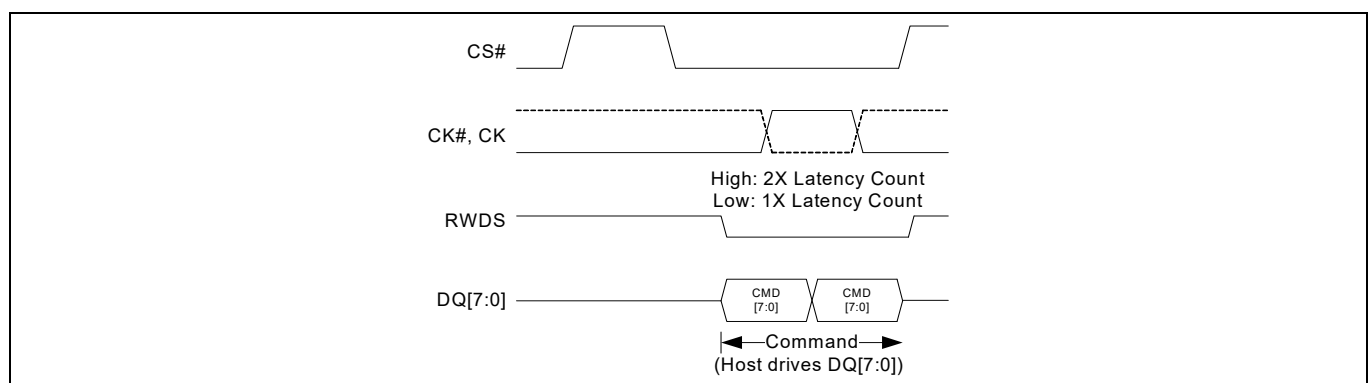


Figure 12 DEEP POWER DOWN transaction (DDR)

### Notes

15. RWDS is driven by pSRAM phase aligned with data.
16. RWDS is driven by pSRAM during command & address cycles for 2X latency and then is driven again phase aligned with data.

## xSPI (Octal) transaction details

### 4.6 READ transaction

The READ transaction reads data from the memory array. It has a latency requirement (dummy cycles) which allows the device's internal circuitry enough time to access the addressed memory location. During these latency cycles, the host can tristate the data bus DQ[7:0].

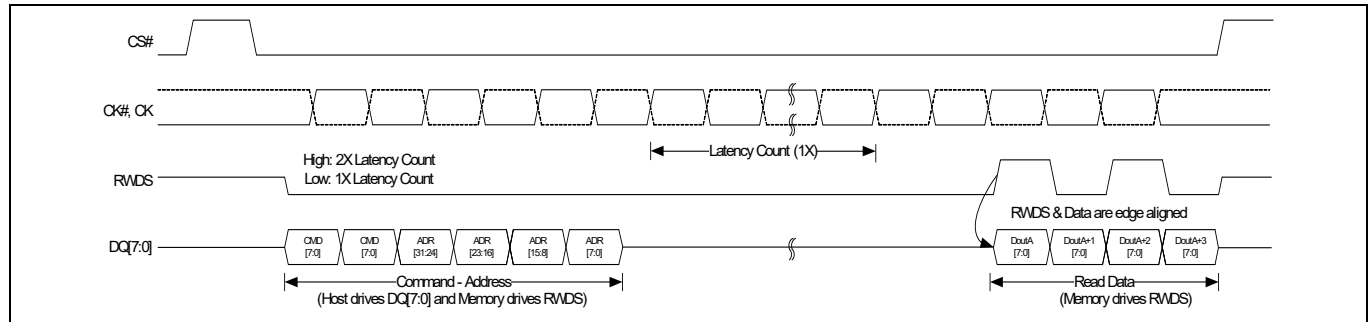


Figure 13 READ with 1X latency transaction (DDR)<sup>[17]</sup>

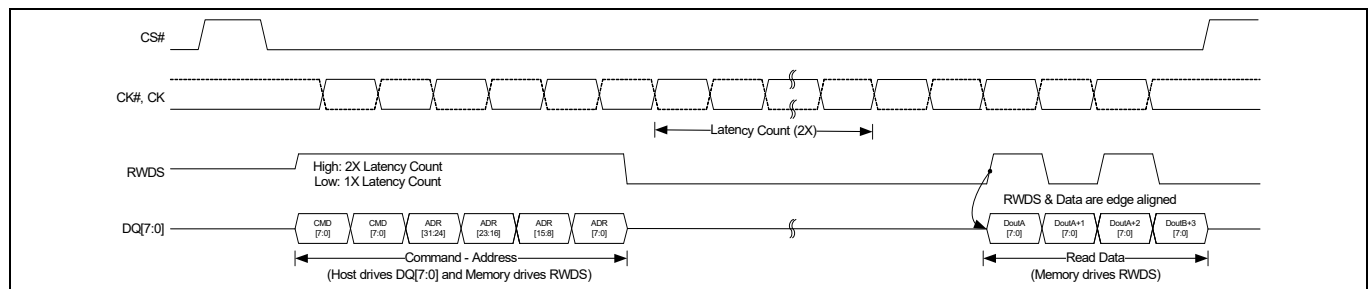


Figure 14 READ with 2X latency transaction (DDR)<sup>[18]</sup>

#### Notes

17. RWDS is driven by pSRAM phase aligned with data.

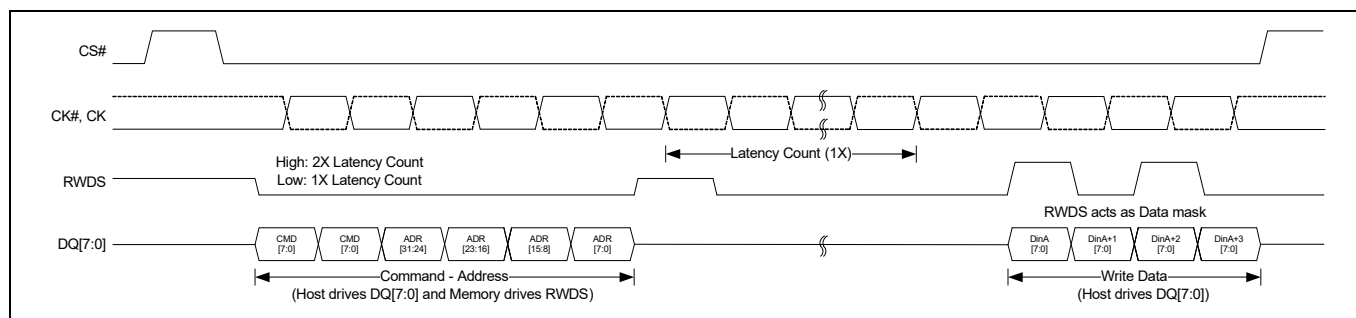
18. RWDS is driven by pSRAM during command & address cycles for 2X latency and then is driven again phase aligned with data.

## xSPI (Octal) transaction details

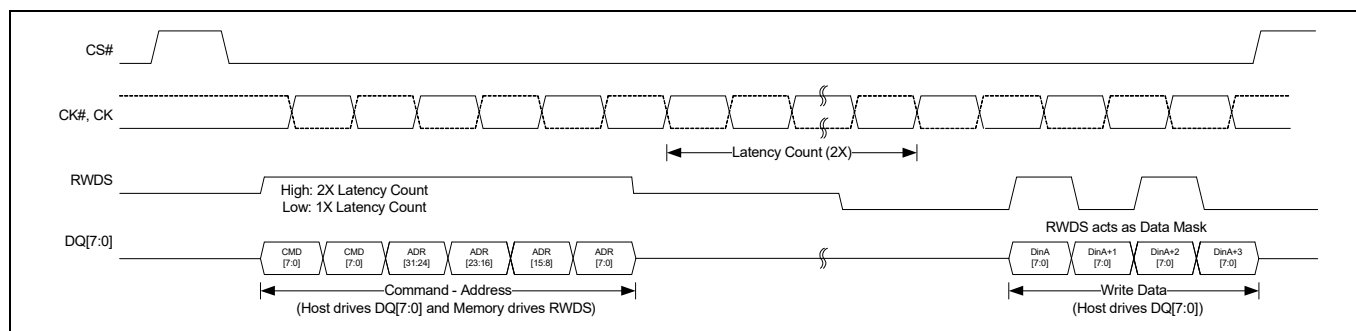
### 4.7 WRITE transaction

The WRITE transaction writes data to the memory array. It has a latency requirement (dummy cycles) which allows the device's internal circuitry enough time to access the addressed memory location. During these latency cycles, the host can tristate the data bus DQ[7:0].

WRITE ENABLE transaction which sets the WEL latch must be executed before the first WRITE. The WEL latch stays set to '1' at the end of any successful memory write transaction. It must be reset by WRITE DISABLE transaction to prevent any inadvertent writes to the memory array.



**Figure 15** WRITE with 1X latency transaction (DDR)<sup>[19, 20]</sup>

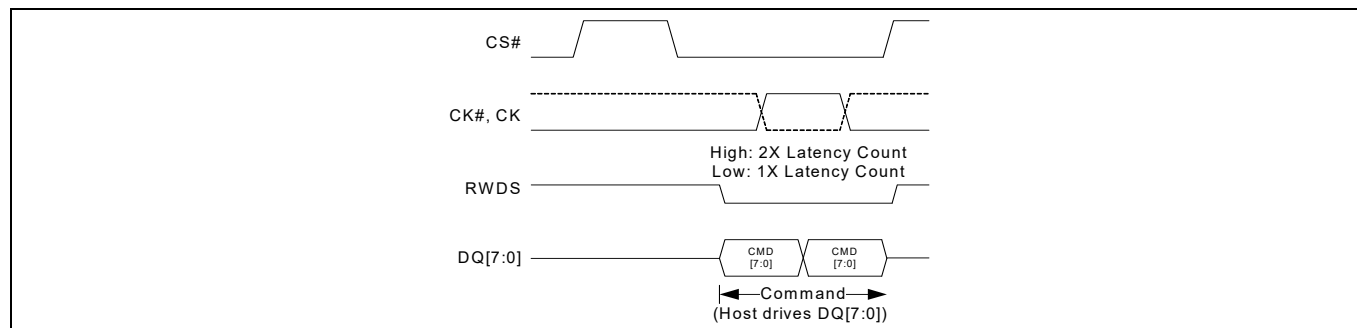


**Figure 16** WRITE with 2X latency transaction (DDR)<sup>[21, 22]</sup>

#### Notes

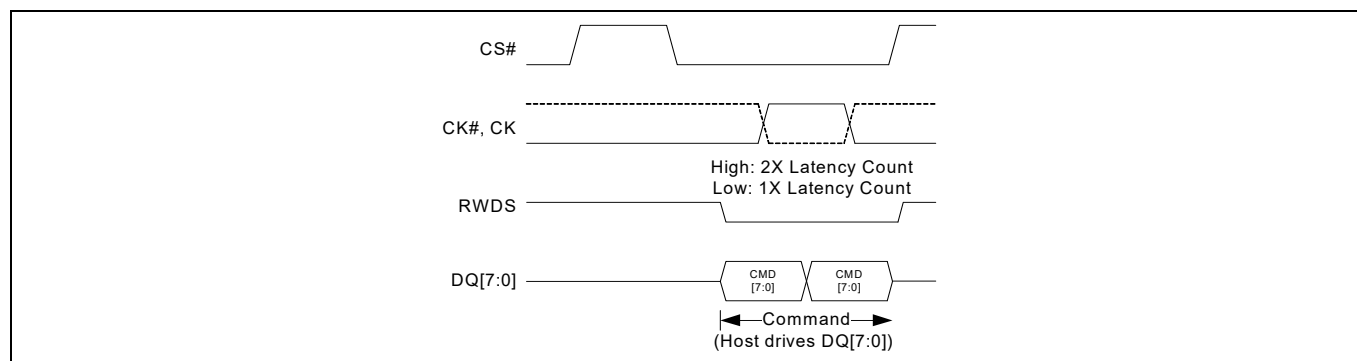
19. RWDS is driven by the host.
20. Data DinA and DinA+2 are masked.
21. RWDS is driven by pSRAM during command and address cycles for 2X latency and then is driven by the host for data masking.
22. Data DinA and DinA+2 are masked.

## 4.8 WRITE ENABLE transaction



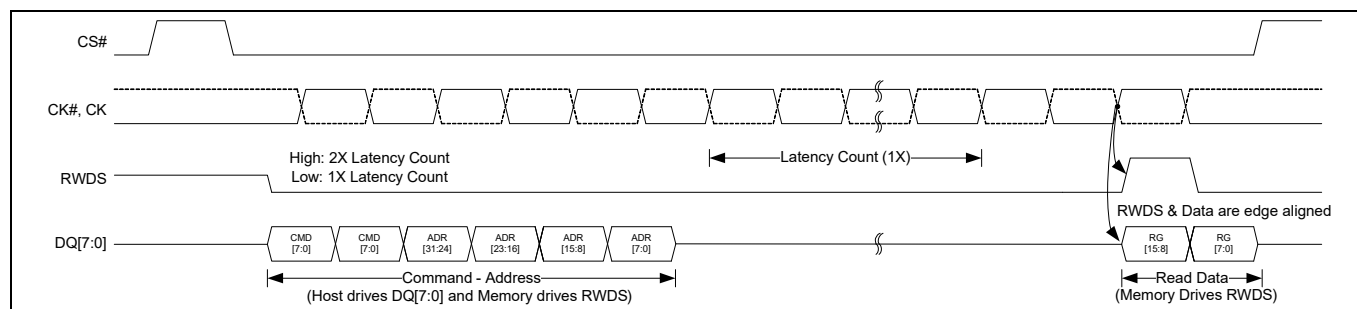
**Figure 17**      **WRITE ENABLE transaction (DDR)**

#### 4.9 WRITE DISABLE transaction



**Figure 18**      **WRITE DISABLE transaction (DDR)**

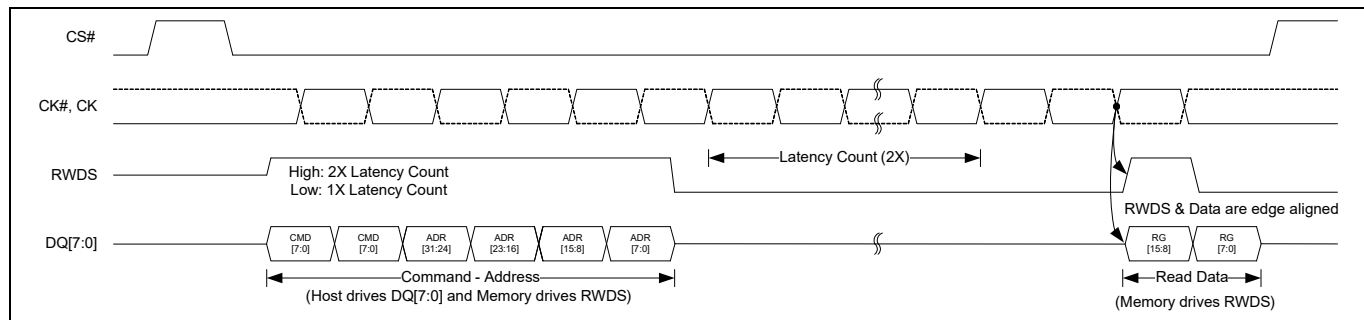
#### 4.10 READ ANY REGISTER transaction



**Figure 19**      **READ ANY REGISTER with 1X latency transaction (DDR)<sup>[23]</sup>**

23. RWDS is driven by pSRAM phase aligned with data.

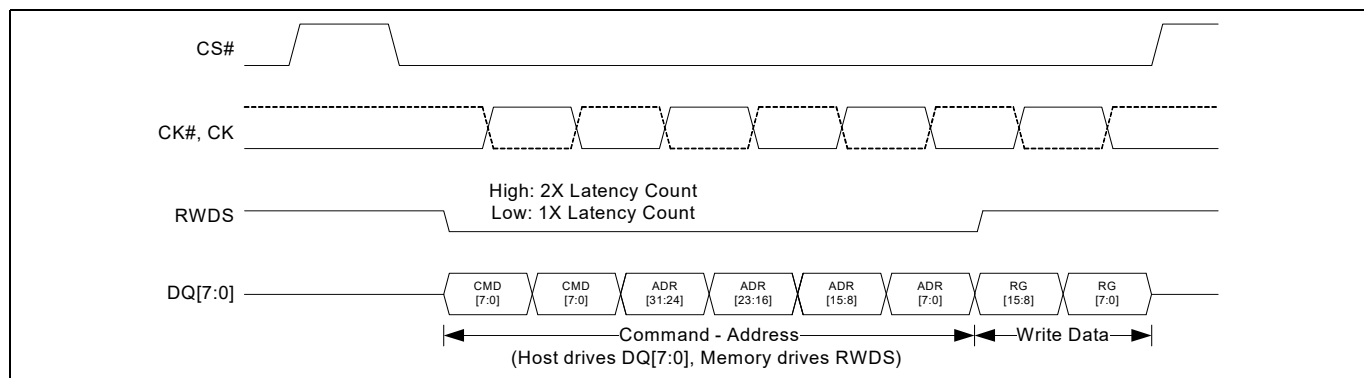
## xSPI (Octal) transaction details



**Figure 20** READ ANY REGISTER with 2X latency transaction (DDR)<sup>[24]</sup>

### 4.11 WRITE ANY REGISTER transaction

The WRITE ANY REGISTER transaction writes to the device registers. It does not have a latency requirement (dummy cycles).



**Figure 21** xSPI (Octal) write with no latency transaction (DDR) (Register writes)<sup>[25, 26]</sup>

#### Notes

24. RWDS is driven by pSRAM during command & address cycles for 2X latency and then driven again phase aligned with data.
25. Write with no latency transaction is used for register writes only.
26. Data mask on RWDS is not supported.

## 4.12 Data placement during memory READ/WRITE transactions

Data placement during memory read/write is dependent upon the host. The device will output data (read) as it was written in (write). Hence both Big Endian and Little Endian are supported for the memory array.

**Table 4 Data placement during memory READ and WRITE**

Address space	Byte order	Byte position	Word data bit	DQ	Bit order
Memory	Big-endian	A	15	7	<p>When data is being accessed in memory space: The first byte of each word read or written is the “A” byte and the second is the “B” byte. The bits of the word within the A and B bytes depend on how the data was written. If the word lower address bits 7-0 are written in the A byte position and bits 15-8 are written into the B byte position, or vice versa, they will be read back in the same order.</p> <p>Therefore, memory space can be stored and read in either little-endian or big-endian order.</p>
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
	Little-endian	A	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
		B	15	7	
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	

## xSPI (Octal) transaction details

### 4.13 Data placement during register READ/WRITE transactions

Data placement during register read/write is Big Endian.

**Table 5 Data placement during register READ/WRITE transactions**

Address space	Byte order	Byte position	Word data bit	DQ	Bit order
Register	Big-endian	A	15	7	When data is being accessed in register space: During a read transaction on the xSPI (Octal) two bytes are transferred on each clock cycle. The upper order byte A (Word[15:8]) is transferred between the rising and falling edges of RWDS (edge-aligned). The lower order byte B (Word[7:0]) is transferred between the falling and rising edges of RWDS.
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	During a write, the upper order byte A (Word[15:8]) is transferred on the CK rising edge and the lower order byte B (Word[7:0]) is transferred on the CK falling edge. So, register space is always read and written in Big-endian order because registers have device dependent fixed bit location and meaning definitions.
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	

## Memory space

## 5 Memory space

### 5.1 xSPI (Octal) interface

**Table 6** Memory space address map (byte based - 8 bits with least significant bit A(0) always set to '0')

Unit type	Count	System byte address bits	Address bits	Notes
Rows within 256 Mb device	32,768 (rows)	A24 - A10	24 - 10	–
Row	64 (half-pages)	A9 - A4	9 - 4	Each row has 64 half-pages. Each half-page has 16 bytes. Each column has 1K bytes).
Half-page	16 (byte addresses)	A3 - A0	3 - 0	Half-page (HP) address is also referenced as upper column address. A word within a HP address is also referenced as lower column address. A0 always set to "0"

### 5.2 Density and row boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the row address bit count and column address bit count fields in the ID0 register. For example: a 256 Mb pSRAM device has 10 column address bits and 15 row address bits for a total of 25 address bits (byte address) =  $2^{25} = 32\text{M}$  bytes (16M words). The 10 column address bits indicate that each row holds  $2^{10} = 1\text{K}$  bytes or 512 words. The row address bit count indicates there are 32768 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

## Register space access

## 6 Register space access

### 6.1 xSPI (Octal) interface

**Table 7** Register space address map (Address bit A0 always set to '0')

Registers	Address (Byte addressable)
Identification registers 0 (ID0[15:0])	0x00000000
Identification registers 1 (ID1[15:0])	0x00000002
Configuration registers 0 (ID0[15:0])	0x00000004
Configuration registers 1 (ID1[15:0])	0x00000006

### 6.2 Device identification registers

There are two read-only, nonvolatile, word registers, that provide information on the device selected when CS# is LOW. The device information fields identify:

- Manufacturer
- Type
- Density
  - Row address bit count
  - Column address bit count
- Refresh type

**Table 8** Identification register 0 (ID0) bit assignments

Bits	Function	Settings (binary)
[15:14]	Reserved	00b - Default
13	Reserved	0b - Default
[12:8]	Row address bit count	01110b - Fifteen row address bits (256 Mb)
[7:4]	Column address bit count	1001b - Ten column address bits (default)
[3:0]	Manufacturer	0110b

ID0 value for CYEL18V2563 is 0x0E96.

**Table 9** Identification register 1 (ID1) bit assignments

Bits	Function	Settings (binary)
[15:4]	Reserved	0000_0000_0000b (default)
[3:0]	Device type	0001b - pSRAM 2.0

## Register space access

## 6.3 Device configuration registers

### 6.3.1 Configuration register 0 (CR0)

Configuration register 0 (CR0) is used to define the power state and access protocol operating conditions for the pSRAM device. Configurable characteristics include:

- Wrapped burst length (16, 32, 64, or 128 byte aligned and length data group)
- Wrapped burst type
  - Legacy wrap (sequential access with wrap around within a selected length and aligned group)
  - Hybrid wrap (Legacy wrap once then linear burst at start of the next sequential group)
- Initial latency
- Variable latency
  - Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output drive strength
- Deep power down (DPD) mode

**Table 10 Configuration register 0 (CR0) bit assignments**

CR0 bit	Function	Settings (binary)
[15]	Deep power down enable	1 - Normal operation (default). pSRAM will automatically set this value to '1' after DPD exit 0 - Writing 0 causes the device to enter deep power down
[14:12]	Drive strength	000 - 34 $\Omega$ (default) 001 - 115 $\Omega$ 010 - 67 $\Omega$ 011 - 46 $\Omega$ 100 - 34 $\Omega$ 101 - 27 $\Omega$ 110 - 22 $\Omega$ 111 - 19 $\Omega$
[11:8]	Reserved	1 - Reserved (default) Reserved for future use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial latency	0000 - 5 clock latency @ 133 MHz Max frequency 0001 - 6 clock latency @ 166 MHz Max frequency 0010 - 7 clock latency @ 200 MHz Max frequency (default) 0011 - Reserved 0100 - Reserved ... 1101 - Reserved 1110 - 3 clock latency @ 85 MHz Max frequency 1111 - 4 clock latency @ 104 MHz Max frequency
[3]	Fixed latency enable	0 - Variable latency - 1 or 2 times initial latency depending on RWDS during CA cycles. 1 - Fixed 2 times initial latency (default)

## Register space access

**Table 10 Configuration register 0 (CR0) bit assignments** *(continued)*

CR0 bit	Function	Settings (binary)
[2]	Hybrid burst enable	0: Wrapped burst sequence to follow hybrid burst sequencing 1: Wrapped burst sequence in legacy wrapped burst manner (default)
[1:0]	Burst length	00 - 128 bytes 01 - 64 bytes 10 - 16 bytes 11 - 32 bytes (default)

### Wrapped burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

### Hybrid burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# HIGH. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical word. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

**Table 11 CR0[2] Control of wrapped burst sequence**

Bit	Default value	Setting details
CR0[2]	1b	Hybrid burst enable CR0[2] = 0: Wrapped burst sequence to follow hybrid burst sequencing CR0[2] = 1: Wrapped burst sequence in legacy wrapped burst manner

**Table 12 Example wrapped burst sequences (Addressing)**

Burst type	Wrap boundary (bytes)	Start address (Hex)	Sequence of byte addresses (Hex) of data words
Hybrid 64	64 wrap once then linear	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00 (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 42, 44, 46, 48, 4A, 4C, 4E, 50, 52, ...
Hybrid 64	64 wrap once then linear	XXXXXX2E	2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, 02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 42, 44, 46, 48, 4A, 4B, 4C, 4D, 4E, 4F, 50, 52, ...
Hybrid 16	16 wrap once then linear	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 00 (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 12, 14, 16, 18, 1A, ..

## Register space access

**Table 12** Example wrapped burst sequences (Addressing) (continued)

Burst type	Wrap boundary (bytes)	Start address (Hex)	Sequence of byte addresses (Hex) of data words
Hybrid 16	16 wrap once then linear	XXXXXX0C	0C, 0E, 00, 02, 04, 06, 08, 0A (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 12, 14, 16, 18, 1A, ...
Hybrid 32	32 wrap once then linear	XXXXXX0A	0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 00, 02, 04, 06, 08 (wrap complete, now linear beyond the end of the initial 32 byte wrap group) 20, 22, 24, 26, 28, 2A, ...
Wrap 64	64	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, ...
Wrap 64	64	XXXXXX2E	2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 00, 02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, 24, 26, 28, 2A, 2C, 2E, 30, ....
Wrap 16	16	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 00, ...
Wrap 16	16	XXXXXX0C	0C, 0E, 00, 02, 04, 06, 08, 0A, ...
Wrap 32	32	XXXXXX0A	0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 00, 02, 04, 06, 08, ...
Linear	Linear burst	XXXXXX02	02, 04, 06, 08, 0A, 0C, 0E, 10, 12, 14, 16, 18, 1A, 1C, 1E, 20, 22, ...

**Initial latency**

Memory space read and write transactions or register space read transactions require some initial latency to open the row selected by the CA. This initial latency is  $t_{ACC}$ . The number of latency clocks needed to satisfy  $t_{ACC}$  depends on the clock input frequency can vary from 3 to 7 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 7 clocks, allowing for operation up to a maximum frequency of 200MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a memory space read or write transaction or register space read transaction begins, the RWDS signal goes High during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register space write transactions always have zero initial latency. RWDS may be HIGH or LOW during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

**Fixed latency**

A configuration register option bit CR0[3] is provided to make all memory space read and write transactions or register space read transactions require the same initial latency by always driving RWDS HIGH during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven HIGH only when additional latency for a refresh is required.

**Drive strength**

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as

## Register space access

overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8 V) and 50°C. The impedance values may vary from the typical values depending on the process, voltage, and temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

### Deep power down

When the pSRAM device is not needed for system operation, it may be placed in a very low power consuming state called deep power down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within  $t_{DPDIN}$  time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# LOW then HIGH, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. For additional details, see “[Deep power down](#)” on page 30.

## 6.3.2 Configuration register 1

Configuration register 1 (CR1) is used to define the refresh array size, refresh rate and hybrid sleep for the pSRAM device. Configurable characteristics include:

- Partial array refresh
- Hybrid sleep state
- Refresh rate

**Table 13 Configuration register 1 (CR1) bit assignments**

CR1 bit	Function	Setting (binary)
[15:8]	Reserved	11111111 - Reserved (default) When writing this register, these bits should keep 0xFFh for future compatibility.
[7]	Burst type	1 - Linear burst (default) 0 - Wrapped burst
[6]	Master clock type	1 - Single ended - CK (default) 0 - Differential - CK#, CK
[5]	Hybrid sleep	1 - Causes the device to enter hybrid sleep state 0 - Normal operation (default)
[4:2]	Partial array refresh	000 - Full array (default) 001 - Bottom 1/2 array 010 - Bottom 1/4 array 011 - Bottom 1/8 array 100 - none 101 - Top 1/2 array 110 - Top 1/4 array 111 - Top 1/8 array
[1:0]	Distributed refresh interval	10 - $1 \mu s t_{CSM}$ ( $85^{\circ}C < T_A \leq 125^{\circ}C$ ) 11 - Reserved 00 - Reserved 01 - $4 \mu s t_{CSM}$ ( $T_A \leq 85^{\circ}C$ )

## Register space access

### Burst type

Two burst types, namely linear and wrapped, are supported in xSPI (Octal) mode by pSRAM. CR1[7] selects which type to use.

### Master clock type

Two clock types, namely single ended and differential, are supported. CR1[6] selects which type to use.

- In the single ended clock mode (by default), CK# input is not enabled; hence it may be left either floating or biased to HIGH or LOW.
- In the differential clock mode (when enabled), the CK# input can't be left floating. It must be either driven by the host, or biased to HIGH or LOW.

### Partial array refresh

The partial array refresh configuration restricts the refresh operation in pSRAM to a portion of the memory array specified by CR1[5:3]. This reduces the standby current. The default configuration refreshes the whole array.

### Hybrid sleep (HS)

When the pSRAM is not needed for system operation but data in the device needs to be retained, it may be placed in hybrid sleep state to save more power. Enter hybrid sleep state by writing 1 to CR1[5]. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit hybrid sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

### Distributed refresh interval

The pSRAM device is built with volatile DRAM array which requires periodic refresh of all bits in it. The refresh operation can be done by an internal self-refresh logic that will evenly refresh the memory array automatically. The automatic refresh operation can only be done when the memory array is not actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS high during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access. The evenly distributed refresh operations require a maximum refresh interval between two adjacent refresh operations. The maximum distributed refresh interval varies with temperature as shown in [Table 14](#).

**Table 14** Array refresh interval per temperature

Operating temperature	Refresh interval $t_{CSM}$	CR1[1:0]
$T_A \leq 85^\circ\text{C}$	4 $\mu\text{s}$	01b
$85^\circ\text{C} < T_A \leq 125^\circ\text{C}$	1 $\mu\text{s}$	10b

The distributed refresh operation requires that the host does not perform burst transactions longer than the distributed refresh interval to prevent the memory from unable doing the distributed refreshes operation when it is needed. This sets an upper limit on the length of read and write transactions so that the automatic distributed refresh operation can be done between transactions. This limit is called the CS# low maximum time ( $t_{CSM}$ ) and the  $t_{CSM}$  will be equal to the maximum distributed refresh interval. The host system is required to respect the  $t_{CSM}$  value by terminating each transaction before violating  $t_{CSM}$ . This can be done by host memory controller splitting long transactions when reaching the  $t_{CSM}$  limit, or by host system hardware or software not performing a single burst read or write transaction that would be longer than  $t_{CSM}$ .

As noted in [Table 14](#), the maximum refresh interval is longer at lower temperatures such that  $t_{CSM}$  could be increased to allow longer transactions. The host may determine the operating temperature from a temperature sensor in the system and use the  $t_{CSM}$  value from the table accordingly, or it may determine dynamically by reading the read only CR1[1:0] bits in order to set the distributed refresh interval prior to the pSRAM access.

## Interface states

## 7 Interface states

**Table 15** describes the required value of each signal for each interface state.

**Table 15** Interface states

Interface state	$V_{CC} / V_{CCQ}$	CS#	CK, CK#	DQ7-DQ0	RWDS	RESET#
Power-off	$< V_{LKO}$	X	X	HIGH-Z	HIGH-Z	X
Power-on (cold) reset	$\geq V_{CC} / V_{CCQ} \text{ min}$	X	X	HIGH-Z	HIGH-Z	X
Hardware (warm) reset	$\geq V_{CC} / V_{CCQ} \text{ min}$	X	X	HIGH-Z	HIGH-Z	L
Interface standby	$\geq V_{CC} / V_{CCQ} \text{ min}$	H	X	HIGH-Z	HIGH-Z	H
CA	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	Master output valid	Y	H
Read initial access latency (data bus turn around period)	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	HIGH-Z	L	H
Write initial access latency (RWDS turn around period)	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	HIGH-Z	HIGH-Z	H
Read data transfer	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	Slave output valid	Slave output valid Z or T	H
Write data transfer with initial latency	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	Master output valid	Master output valid X or T	H
Write data transfer without initial latency <sup>[27]</sup>	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	T	Master output valid	Slave output L or HIGH-Z	H
Active clock stop <sup>[28]</sup>	$\geq V_{CC} / V_{CCQ} \text{ min}$	L	Idle	Master or slave output valid or HIGH-Z	Y	H
Deep power down	$\geq V_{CC} / V_{CCQ} \text{ min}$	H	X or T	HIGH-Z	HIGH-Z	H
Hybrid sleep	$\geq V_{CC} / V_{CCQ} \text{ min}$	H	X or T	HIGH-Z	HIGH-Z	H

### Notes

27. Writes without initial latency (with zero initial latency), do not have a turn around period for RWDS. The pSRAM device will always drive RWDS during the CA period to indicate whether extended latency is required. Since master write data immediately follows the CA period the pSRAM device may continue to drive RWDS LOW or may take RWDS to HIGH-Z. The master must not drive RWDS during writes with zero latency. writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

28. Active clock stop is described in “**Active clock stop**” on page 29. DPD is described in “**Deep power down**” on page 30

### Legend

L =  $V_{IL}$ ; H =  $V_{IH}$ ; X = either  $V_{IL}$  or  $V_{IH}$ ; Y = either  $V_{IL}$  or  $V_{IH}$  or  $V_{OL}$  or  $V_{OH}$ ; Z = either  $V_{OL}$  or  $V_{OH}$ ; L/H = rising edge; H/L = falling edge; T = Toggling during information transfer; Idle = CK is LOW and CK# is HIGH; Valid = all bus signals have stable L or H level

## 8 Power conservation modes

### 8.1 Interface standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS# = HIGH). All inputs, and outputs other than CS# and RESET# are ignored in this state.

### 8.2 Active clock stop

Design Note: Active Clock Stop feature is pending device characterization to determine if it will be supported. The active clock stop state reduces device interface energy consumption to the  $I_{CC6}$  level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for  $t_{ACC} + 30$  ns. While in active clock stop state, read data is latched and always driven onto the data bus.  $I_{CC6}$  shown in “DC characteristics” on page 33.

Active clock stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be LOW throughout these extended data transfer cycles, the memory device host interface will go into the active clock stop current level at  $t_{ACC} + 30$  ns. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The active clock stop state must not be used in violation of the  $t_{CSM}$  limit. CS# must go HIGH before  $t_{CSM}$  is violated. Clock can be stopped during any portion of the active transaction as long as it is in the LOW state. Note that it is recommended to avoid stopping the clock during register access.

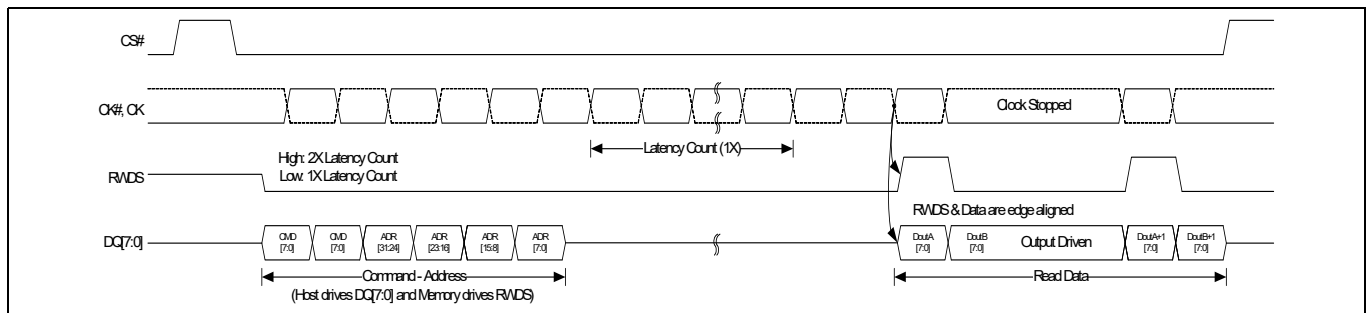


Figure 22 Active clock stop during read transaction (DDR)<sup>[29]</sup>

### 8.3 Hybrid sleep

In the hybrid sleep (HS) state, the current consumption is reduced ( $I_{HS}$ ). HS state is entered by writing a 1 to CR1[5]. The device reduces power within  $t_{HSIN}$  time. The data in memory space and register space is retained during HS state. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit hybrid sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost. Returning to standby state requires  $t_{EXITHS}$  time. Following the exit from HS due to any of these events, the device is in the same state as entering hybrid sleep.

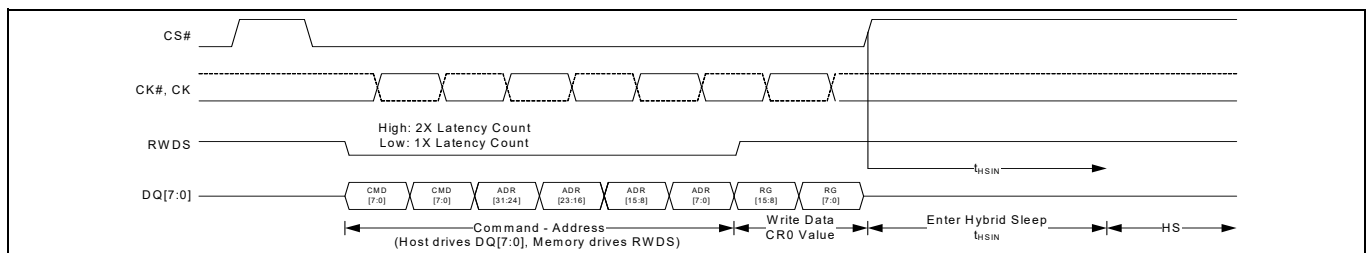
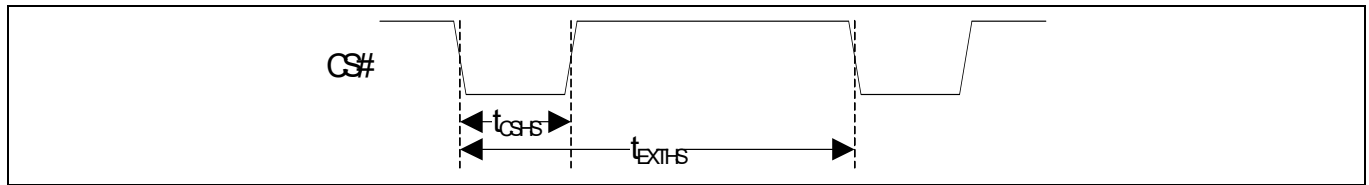


Figure 23 Enter HS transaction

#### Note

29. RWDS is LOW during the CA cycles. In this read transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

## Power conservation modes



**Figure 24** Exit HS transaction

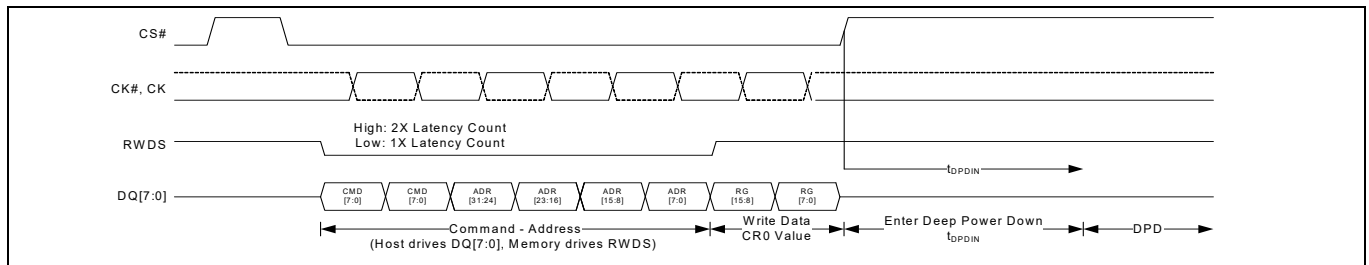
**Table 16** Hybrid sleep timing parameters

Parameter	Description	Min	Max	Unit
$t_{HSIN}$	Hybrid sleep CR1[5] = 0 register write to DPD power level	–	3	$\mu s$
$t_{CSHS}$	CS# pulse width to exit HS	60	3000	ns
$t_{EXTHS}$	CS# exit hybrid sleep to standby wakeup time	–	100	$\mu s$

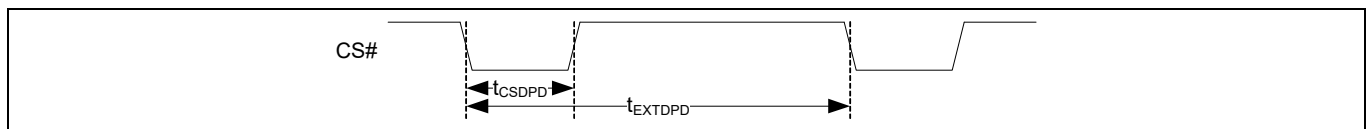
## 8.4 Deep power down

In the deep power down (DPD) state, current consumption is driven to the lowest possible level ( $I_{DPD}$ ). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within  $t_{DPDIN}$  time and all refresh operations stop. The data in memory space is lost, (becomes invalid without refresh) during DPD state. Driving CS# LOW then HIGH will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to standby state requires  $t_{EXTDPD}$  time. Returning to standby state following a POR requires  $t_{VCS}$  time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

**Note** In xSPI (Octal), deep power down transaction or write any register transaction can be used to enter DPD.



**Figure 25** Enter DPD transaction



**Figure 26** Exit DPD transaction

**Table 17** Deep power down timing parameters

Parameter	Description	Min	Max	Unit
$t_{DPDIN}$	Deep power down CR0[15] = 0 register write to DPD power level	–	3	$\mu s$
$t_{CSDPD}$	CS# pulse width to exit DPD	200	3000	ns
$t_{EXTDPD}$	CS# exit deep power down to standby wakeup time	–	150	$\mu s$

## Electrical specifications

## 9 Electrical specifications

### 9.1 Absolute maximum ratings

Table 18 Absolute maximum ratings

Storage temperature plastic packages	-65°C to +150°C
Ambient temperature with power applied	-65°C to +135°C
Voltage with respect to ground all signals <sup>[30]</sup>	-0.5 V to + (V <sub>CC</sub> + 0.5 V)
Output short circuit current <sup>[31]</sup>	100 mA
Voltage on V <sub>CC</sub> , V <sub>CCQ</sub> pins relative to V <sub>SS</sub>	-0.5 V to +2.5 V
Electrostatic discharge voltage: Human body model (JEDEC Std JESD22-A114-B) Charged device model (JEDEC Std JESD22-C101-A)	2000 V 500 V

### 9.2 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V<sub>SS</sub> and V<sub>CC</sub>. During voltage transitions, inputs or I/Os may negative overshoot V<sub>SS</sub> to -1.0V or positive overshoot to V<sub>CC</sub> +1.0V, for periods up to 20 ns.

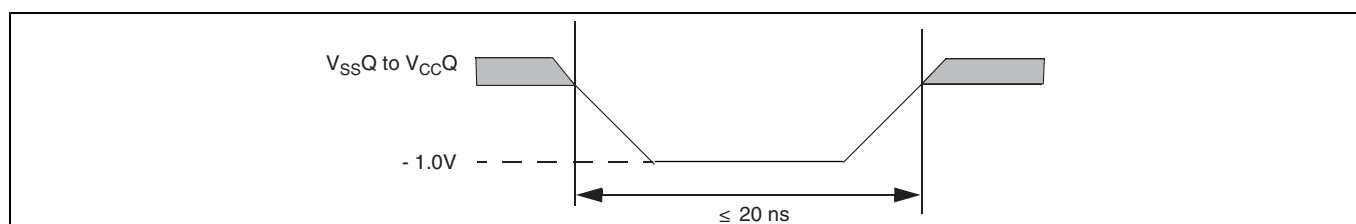


Figure 27 Maximum negative overshoot waveform

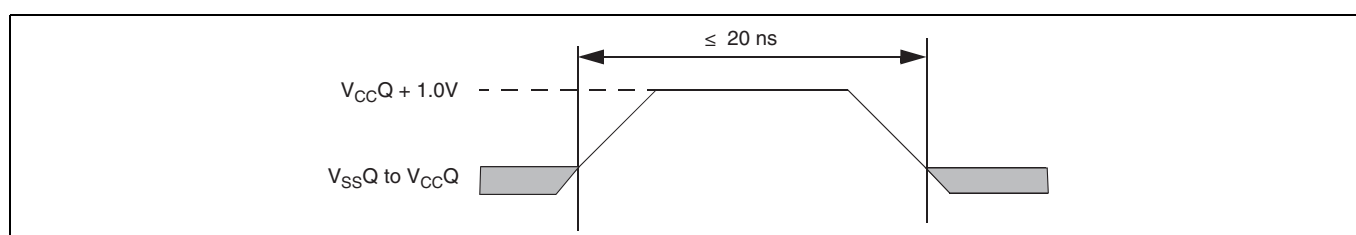


Figure 28 Maximum positive overshoot waveform

#### Notes

30. Minimum DC voltage on input or I/O signal is -1.0 V. During voltage transitions, input or I/O signals may undershoot V<sub>SS</sub> to -1.0V for periods of up to 20 ns. See [Figure 27](#). Maximum DC voltage on input or I/O signals is V<sub>CC</sub> +1.0 V. During voltage transitions, input or I/O signals may overshoot to V<sub>CC</sub> +1.0 V for periods up to 20 ns. See [Figure 28](#).
31. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
32. Stresses above those listed under “[Absolute maximum ratings](#)” on page 31 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical specifications

### 9.3 Latch-up characteristics

**Table 19** Latch-up specification<sup>[33]</sup>

Description	Min	Max	Unit
Input voltage with respect to $V_{SSQ}$ on all input only connections	-1.0	$V_{CCQ} + 1.0$	V
Input voltage with respect to $V_{SSQ}$ on all I/O connections	-1.0	$V_{CCQ} + 1.0$	
$V_{CCQ}$ current	-100	+100	mA

**Note**

33.Excludes power supplies  $V_{CC}/V_{CCQ}$ . Test conditions:  $V_{CC} = V_{CCQ}$ , one connection at a time tested, connections not being tested are at  $V_{SS}$ .

### 9.4 Operating ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

#### 9.4.1 Temperature ranges

**Table 20** Temperature ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient temperature	$T_A$	Extended (E)	-40	125	°C

#### 9.4.2 Power supply voltages

**Table 21** Power supply voltages

Description	Min	Max	Unit
$V_{CC}$ power supply	1.7	2.0	V

## Electrical specifications

### 9.5 DC characteristics

**Table 22** DC characteristics (CMOS compatible)

Parameter	Description	Test conditions	Value			Unit
			Min	Typ <sup>[34]</sup>	Max	
$I_{LI2}$	Input leakage current. Device reset signal HIGH	$V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$ max	–	–	2	$\mu A$
$I_{LI4}$	Input leakage current Device reset signal LOW <sup>[35]</sup>		–	–	15	
$I_{CC1}$	$V_{CC}$ Active read current Operating temperature range	$CS\# = V_{SS}$ , $CK@200$ MHz, $V_{CC} = V_{CC}$ max	–	14	20	mA
$I_{CC2}$	$V_{CC}$ Active write current Operating temperature range		–	16	22	
$I_{CC4}$	$V_{CC}$ standby current	$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; full array	–	470	2000	$\mu A$
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; bottom 1/2 array	–	–	1550	
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; bottom 1/4 array	–	–	1250	
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; bottom 1/8 array	–	–	1100	
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; top 1/2 array	–	–	1550	
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; top 1/4 array	–	–	1250	
		$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max; top 1/8 array	–	–	1100	
$I_{CC5}$	Reset current	$CS\# = V_{CC}$ , $RESET\# = V_{SS}$ , $V_{CC} = V_{CC}$ max	–	–	1	mA
$I_{CC6}$	Active clock stop current	$CS\# = V_{SS}$ , $RESET\# = V_{CC}$ , $V_{CC} = V_{CC}$ max	–	17	40	mA
$I_{CC7}$	$V_{CC}$ current during power up <sup>[34]</sup>	$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max, $V_{CCQ} = V_{CC}$	–	–	35	mA
$I_{DPD}$ <sup>[34]</sup>	Deep power down current	$CS\# = V_{CC}$ , $V_{CC} = V_{CC}$ max	–	–	20	$\mu A$

#### Notes

34. Not 100% tested.

35. RESET# LOW initiates exits from DPD state and initiates the draw of  $I_{CC5}$  reset current, making  $I_{LI}$  during RESET# LOW insignificant.

## Electrical specifications

**Table 22** DC characteristics (CMOS compatible) (continued)

Parameter	Description	Test conditions	Value			Unit
			Min	Typ <sup>[34]</sup>	Max	
$I_{HS}^{[34]}$	Hybrid sleep current	CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; full array	–	140	1500	$\mu\text{A}$
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; bottom 1/2 array	–	–	1150	
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; bottom 1/4 array	–	–	900	
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; bottom 1/8 array	–	–	750	
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; top 1/2 array	–	–	1150	
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; top 1/4 array	–	–	900	
		CS# = $V_{CC}$ ; $V_{CC} = V_{CC \text{ max}}$ ; top 1/8 array	–	–	750	
$V_{IL}$	Input low voltage	–	$-0.15 \times V_{CCQ}$	–	$0.30 \times V_{CCQ}$	V
$V_{IH}$	Input high voltage	–	$0.70 \times V_{CCQ}$	–	$1.15 \times V_{CCQ}$	
$V_{OL}$	Output low voltage	$I_{OL} = 100 \mu\text{A}$ for DQ[7:0]	–	–	0.2	
$V_{OH}$	Output high voltage		$V_{CCQ} - 0.20$	–	–	

**Notes**

34. Not 100% tested.

35. RESET# LOW initiates exits from DPD state and initiates the draw of  $I_{CC5}$  reset current, making  $I_{LI}$  during RESET# LOW insignificant.

## Electrical specifications

## 9.5.1 Capacitance characteristics

Table 23 Capacitive characteristics<sup>[36-38]</sup>

Description	Parameter	256 Mb	Unit
		Max	
Input capacitance (CK, CK#, CS#)	CI	3.0	pF
Delta input capacitance (CK, CK#)	CID	0.25	
Output capacitance (RWDS)	CO	3.0	
IO capacitance (DQx)	CIO	3.0	
IO capacitance delta (DQx)	CIOD	0.25	

**Notes**

36. These values are guaranteed by design and are tested on a sample basis only.

37. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer.  $V_{CC}$ ,  $V_{CCQ}$  are applied and all other signals (except the signal under test) floating. DQs should be in the high impedance state.

38. Note that the capacitance values for the CK, CK#, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (LOW) and data being presented on the DQ's bus.

Table 24 Thermal resistance

Parameter <sup>[39]</sup>	Description	Test conditions	24-ball FBGA package	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	40.8	°C/W
$\theta_{JC}$	Thermal resistance (junction to case)		8	

**Note**

39. This parameter is guaranteed by characterization; not tested in production.

## Electrical specifications

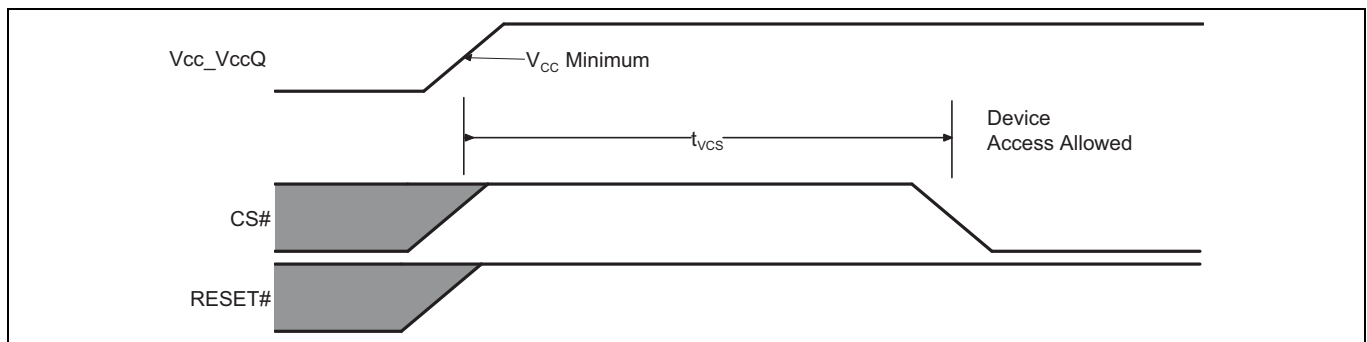
### 9.6 Power-up initialization

pSRAM products include an on-chip voltage sensor used to launch the power-up initialization process.  $V_{CC}$  and  $V_{CCQ}$  must be applied simultaneously. When the power supply reaches a stable level at or above  $V_{CC}(\text{min})$ , the device will require  $t_{VCS}$  time to complete its self-initialization process.

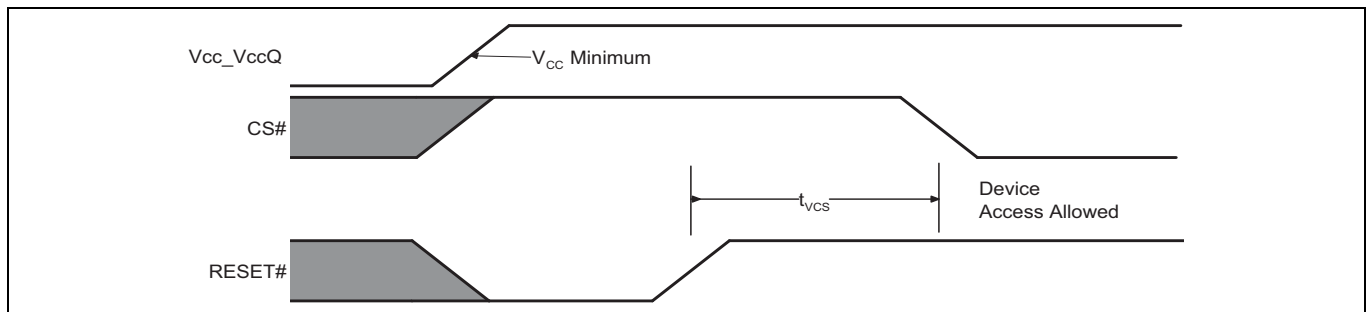
The device must not be selected during power-up.  $CS\#$  must follow the voltage applied on  $V_{CCQ}$  until  $V_{CC}(\text{min})$  is reached during power-up, and then  $CS\#$  must remain high for a further delay of  $t_{VCS}$ . A simple pull-up resistor from  $V_{CCQ}$  to chip select ( $CS\#$ ) can be used to insure safe and proper power-up.

If  $RESET\#$  is LOW during power up, the device delays start of the  $t_{VCS}$  period until  $RESET\#$  is HIGH. The  $t_{VCS}$  period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.



**Figure 29** Power-up with  $RESET\#$  HIGH



**Figure 30** Power-up with  $RESET\#$  LOW

**Table 25** Power up and reset parameters<sup>[40-42]</sup>

Parameter	Description	Min	Max	Unit
$V_{CC}$	$V_{CC}$ Power supply	1.7	2.0	V
$t_{VCS}$	$V_{CC}$ and $V_{CCQ} \geq$ minimum and $RESET\#$ HIGH to first access	–	150	$\mu\text{s}$

#### Notes

40. Bus transactions (read and write) are not allowed during the power-up reset time ( $t_{VCS}$ ).

41.  $V_{CCQ}$  must be the same voltage as  $V_{CC}$ .

42.  $V_{CC}$  ramp rate may be non-linear.

## Electrical specifications

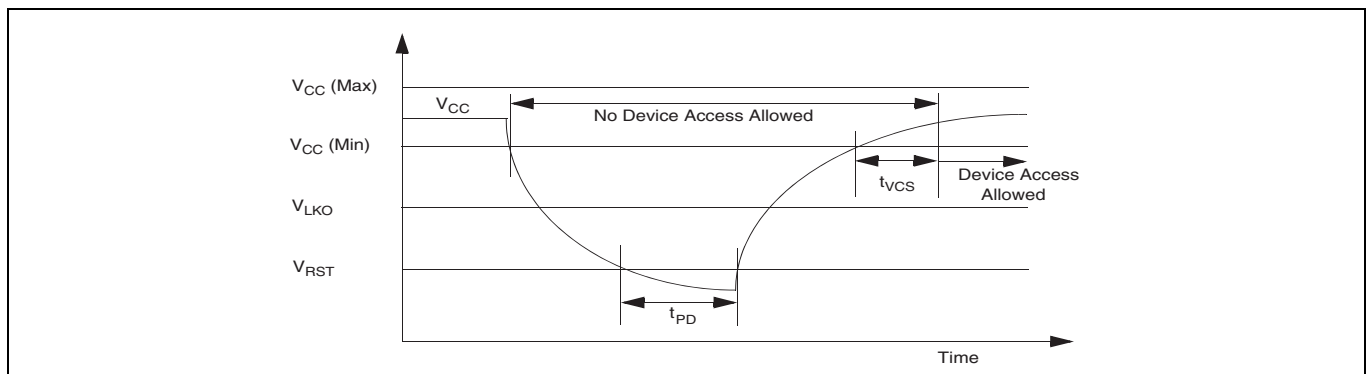
### 9.7 Power down

pSRAM devices are considered to be powered-off when the array power supply ( $V_{CC}$ ) drops below the  $V_{CC}$  lock-out voltage ( $V_{LKO}$ ). During a power supply transition down to the  $V_{SS}$  level,  $V_{CCQ}$  should remain less than or equal to  $V_{CC}$ . At the  $V_{LKO}$  level, the pSRAM device will have lost configuration or array data.

$V_{CC}$  must always be greater than or equal to  $V_{CCQ}$  ( $V_{CC} \geq V_{CCQ}$ ).

During power-down or voltage drops below  $V_{LKO}$ , the array power supply voltages must also drop below  $V_{CC}$  Reset ( $V_{RST}$ ) for a power down period ( $t_{PD}$ ) for the part to initialize correctly when the power supply again rises to  $V_{CC}$  minimum. See [Figure 31](#).

If during a voltage drop the  $V_{CC}$  stays above  $V_{LKO}$  the part will stay initialized and will work correctly when  $V_{CC}$  is again above  $V_{CC}$  minimum. If  $V_{CC}$  does not go below and remain below  $V_{RST}$  for greater than  $t_{PD}$ , then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the device is properly initialized.



**Figure 31** Power down or voltage drop

The following section describes pSRAM device dependent aspects of power down specifications.

**Table 26** Power-down voltage and timing<sup>[42]</sup>

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	$V_{CC}$ power supply	1.7	2.0	V
$V_{LKO}$	$V_{CC}$ lock-out below which re-initialization is required	1.5	–	V
$V_{RST}$	$V_{CC}$ low voltage needed to ensure initialization will occur	0.7	–	V
$t_{PD}$	Duration of $V_{CC} \leq V_{RST}$	50	–	$\mu s$

## Electrical specifications

## 9.8 Hardware reset

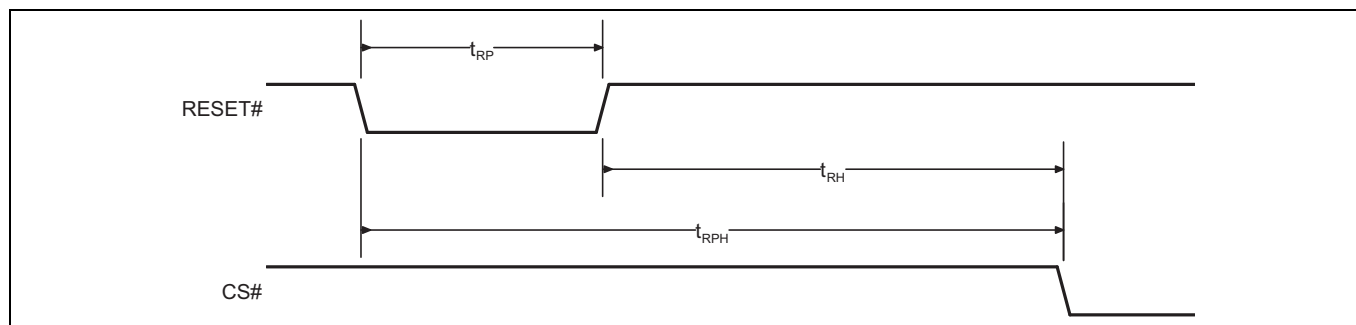
The RESET# input provides a hardware method of returning the device to the standby state.

During  $t_{RPH}$  the device will draw  $I_{CC5}$  current. If RESET# continues to be held LOW beyond  $t_{RPH}$ , the device draws CMOS standby current ( $I_{CC4}$ ). While RESET# is LOW (during  $t_{RP}$ ), and during  $t_{RPH}$ , bus transactions are not allowed.

A hardware reset will do the following:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is LOW - memory array data is considered as invalid
- Force the device to exit the hybrid sleep state
- Force the device to exit the deep power down state

After RESET# returns HIGH, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# LOW, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per [Table 14](#). This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after a hardware reset and reload any required data.



**Figure 32** Hardware reset timing diagram

**Table 27** Power-up and reset parameters

Parameter	Description	Min	Max	Unit
$t_{RP}$	RESET# Pulse Width	200	–	ns
$t_{RH}$	Time between RESET# (HIGH) and CS# (LOW)	200	–	ns
$t_{RPH}$	RESET# LOW to CS# LOW	400	–	ns

Timing specifications

## 10 Timing specifications

The following section describes pSRAM device dependent aspects of timing specifications.

### 10.1 Key to switching waveforms

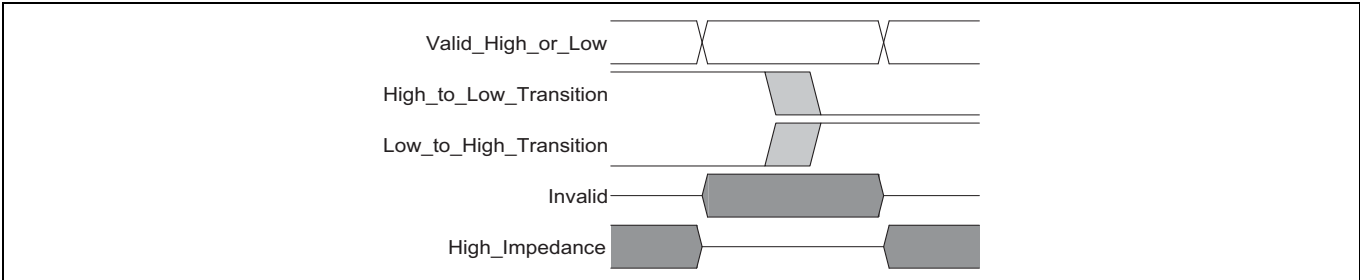


Figure 33 Key to switching waveforms

### 10.2 AC test conditions

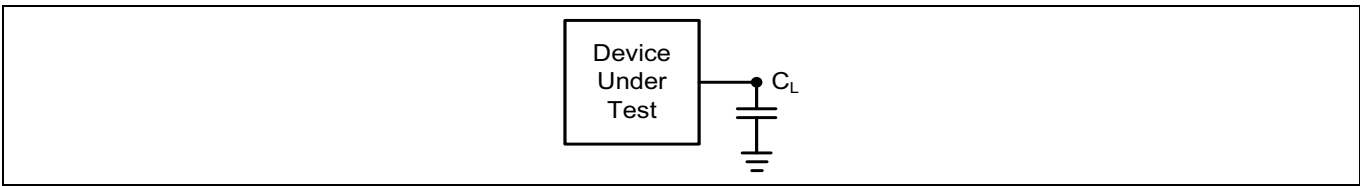


Figure 34 Test setup

Table 28 Test specification<sup>[44]</sup>

Parameter	All Speeds	Units
Output load capacitance, $C_L$	15	pF
Minimum input rise and fall slew rates (1.8 V) <sup>[43]</sup>	1.13	V/ns
Input pulse levels	0.0– $V_{CCQ}$	V
Input timing measurement reference levels	$V_{CCQ}/2$	V
Output timing measurement reference levels	$V_{CCQ}/2$	V

**Notes**

43.All AC timings assume this input slew rate.

44.Input and output timing is referenced to  $V_{CCQ}/2$  or to the crossing of CK/CK#.

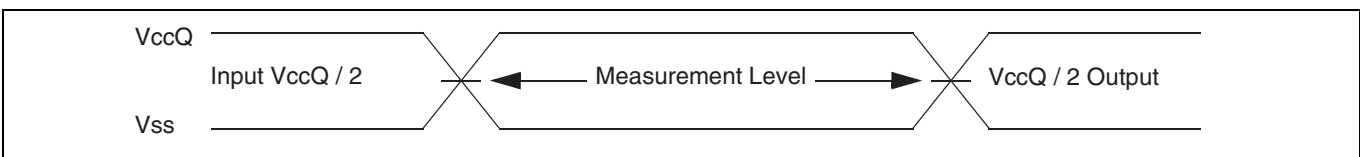


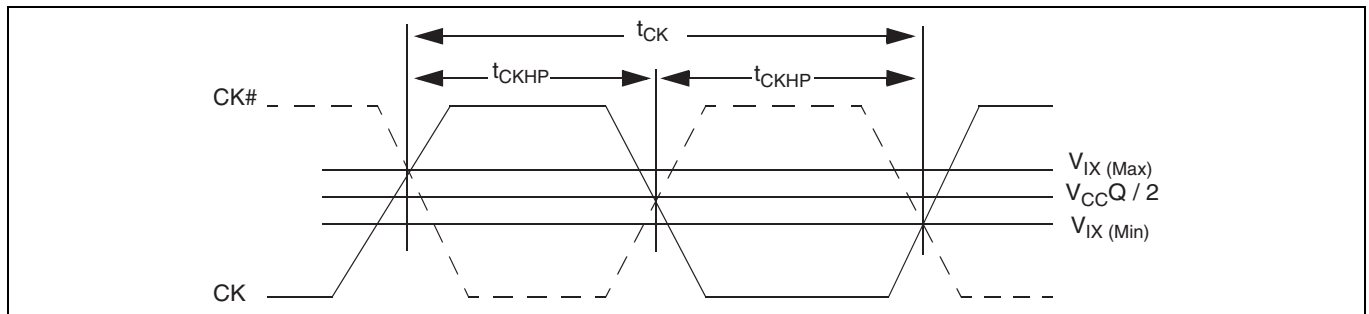
Figure 35 Input waveforms and measurement levels<sup>[45]</sup>

**Note**

45.Input timings for the differential CK/CK# pair are measured from clock crossings.

## Timing specifications

### 10.3 CLK characteristics



**Figure 36** Clock characteristics

**Table 29** Clock timings<sup>[46-48]</sup>

Parameter	Symbol	200 MHz		Unit
		Min	Max	
CK period	$t_{CK}$	5	–	ns
CK half period - duty cycle	$t_{CKHP}$	0.45	0.55	$t_{CK}$
CK half period at frequency Min = $0.45 t_{CK}$ min Max = $0.55 t_{CK}$ min	$t_{CKHP}$	2.25	2.75	ns

#### Notes

46.Clock jitter of  $\pm 5\%$  is permitted

47.Minimum frequency (Maximum  $t_{CK}$ ) is dependent upon maximum CS# low time ( $t_{CSM}$ ), initial latency, and burst length.

48.CK and CK# input slew rate must be  $\geq 1$  V/ns (2 V/ns if measured differentially).

**Table 30** Clock AC/DC electrical characteristics<sup>[49, 50]</sup>

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_{IN}$	-0.3	$V_{CCQ} + 0.3$	V
DC input differential voltage	$V_{ID(DC)}$	$V_{CCQ} \times 0.4$	$V_{CCQ} + 0.6$	V
AC input differential voltage	$V_{ID(AC)}$	$V_{CCQ} \times 0.6$	$V_{CCQ} + 0.6$	V
AC differential crossing voltage	$V_{IX}$	$V_{CCQ} \times 0.4$	$V_{CCQ} \times 0.6$	V

#### Notes

49. $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on CK#.

50.The value of  $V_{IX}$  is expected to equal  $V_{CCQ}/2$  of the transmitting device and must track variations in the DC level of  $V_{CCQ}$ .

## Timing specifications

### 10.4 AC characteristics

#### 10.4.1 Read transactions

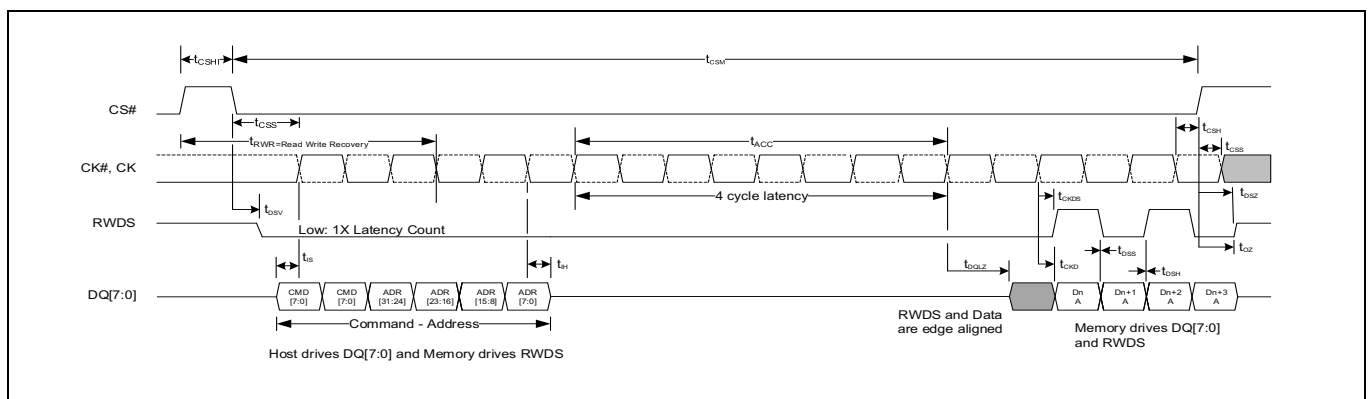
**Table 31** pSRAM-specific read timing parameters

Parameter	Symbol	200 MHz		Unit
		Min	Max	
Chip select high between transactions	$t_{CSHI}$	6.0	–	ns
pSRAM read-write recovery time	$t_{RWR}$	35	–	ns
Chip select setup to next CK rising edge	$t_{CSS}$	4.0	–	ns
Data strobe valid	$t_{DSV}$	–	5.0	ns
Input setup	$t_{IS}$	0.5	–	ns
Input hold	$t_{IH}$	0.5	–	ns
pSRAM read initial access time	$t_{ACC}$	35	–	ns
Clock to DQs Low Z	$t_{DQLZ}$	0	–	ns
CK transition to DQ valid	$t_{CKD}$	1.0	5.0	ns
CK transition to DQ invalid	$t_{CKDI}$	0	4.2	ns
Data valid ( $t_{DV}$ min = the lesser of: $t_{CKHP}$ min - $t_{CKD}$ max + $t_{CKDI}$ max) or $t_{CKHP}$ min - $t_{CKD}$ min + $t_{CKDI}$ min)	$t_{DV}^{[51, 52]}$	1.45	–	ns
CK transition to RWDS valid	$t_{CKDS}$	1.0	5.0	ns
RWDS transition to DQ valid	$t_{DSS}$	–0.4	+0.4	ns
RWDS transition to DQ invalid	$t_{DSH}$	–0.4	+0.4	ns
Chip select hold after CK falling edge	$t_{CSH}$	0	–	ns
Chip select inactive to RWDS High-Z	$t_{DSZ}$	–	5.0	ns
Chip select inactive to DQ High-Z	$t_{OZ}$	–	5.0	ns
Refresh time	$t_{RFH}$	35	–	ns
CK transition to RWDS low @CA phase @read	$t_{CKDSR}$	1.0	5.5	ns

#### Notes

51. Refer to [Figure 39](#) for data valid timing.

52. The  $t_{DV}$  timing calculation is provided for reference only, not to determine the spec limit. The spec limit is guaranteed by testing.



**Figure 37** Read timing diagram — No additional latency required



### Table 32 Write timing parameters

53.  $t_{CKD}$  and  $t_{CKDI}$  parameters define the beginning and end position of data valid period.

54.  $t_{DSS}$  and  $t_{DSH}$  define how early or late DQ may transition relative to RWDS. This is a potential skew between the CK to DQ delay  $t_{CKD}$  and CK to RWDS delay  $t_{CKDS}$ .

55. Since DQ and RWDS are the same output types, the  $t_{CKD}$ , and  $t_{CKDS}$  values track together (vary by the same ratio).

The timing diagram illustrates the relationship between several signals over time:

- CS#**: Chip select signal. It has a setup time  $t_{CS\#}$  before the first clock edge and a hold time  $t_{CSH}$  after the last clock edge.
- CK#, CK**: Clock signals. The period is  $t_{CK}$ . There are two phases shown, with a phase shift indicated by  $t_{CKP}$ .
- RWDS**: Read/Write Strobe signal. It has a setup time  $t_{RWS}$  before the first clock edge and a hold time  $t_{RWHS}$  after the last clock edge. The diagram shows "Additional Latency" and "4 cycle latency1" and "4 cycle latency2" periods relative to the clock edges.
- DQ[7:0]**: Data bus signal. It shows command and address cycles. Command cycles have a setup time  $t_s$  and a hold time  $t_h$ . Address cycles have a setup time  $t_a$  and a hold time  $t_b$ . The diagram also shows "Host drives DQ[7:0] and Memory drives RWDS" and "Host drives DQ[7:0] and RWDS".

Timing specifications

10.5 Timing reference levels

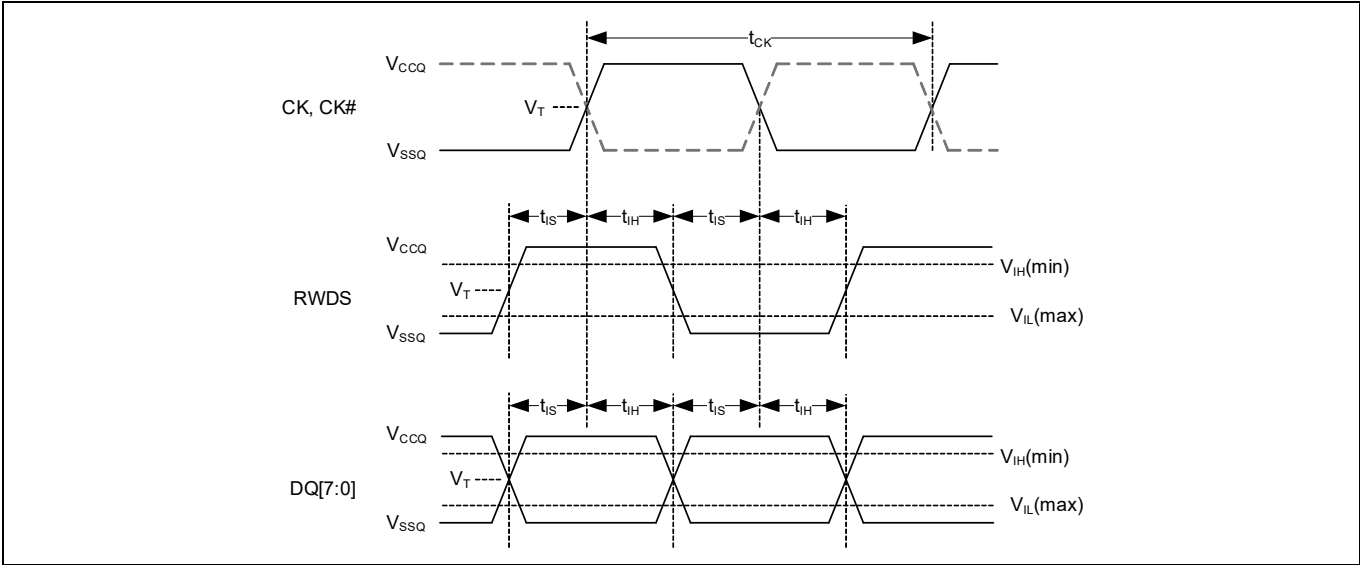


Figure 42 DDR input timing reference levels

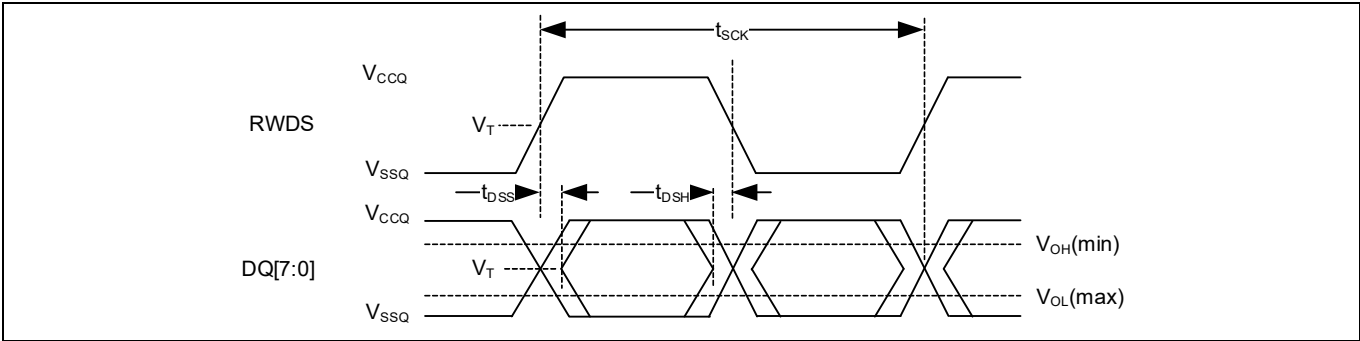


Figure 43 DDR output timing reference levels

Physical interface

# 11 Physical interface

## 11.1 FBGA 24-ball 5 x 5 array footprint

pSRAM devices are provided in fortified ball grid array (FBGA), 1 mm pitch, 24-ball, 5 x 5 ball array footprint, with 6mm x 8mm body.

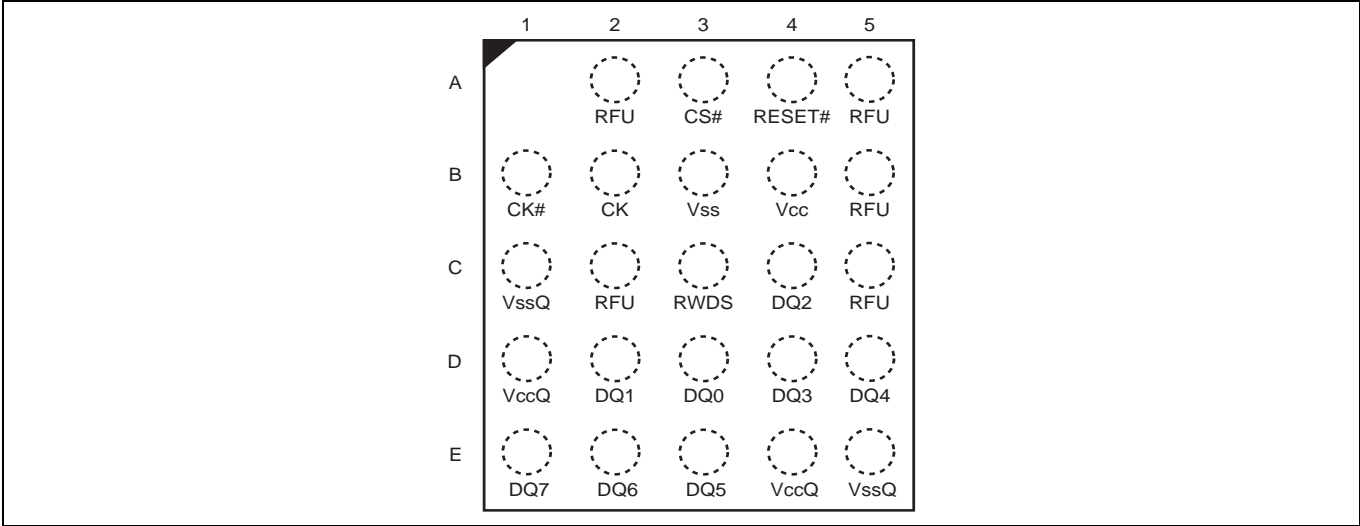
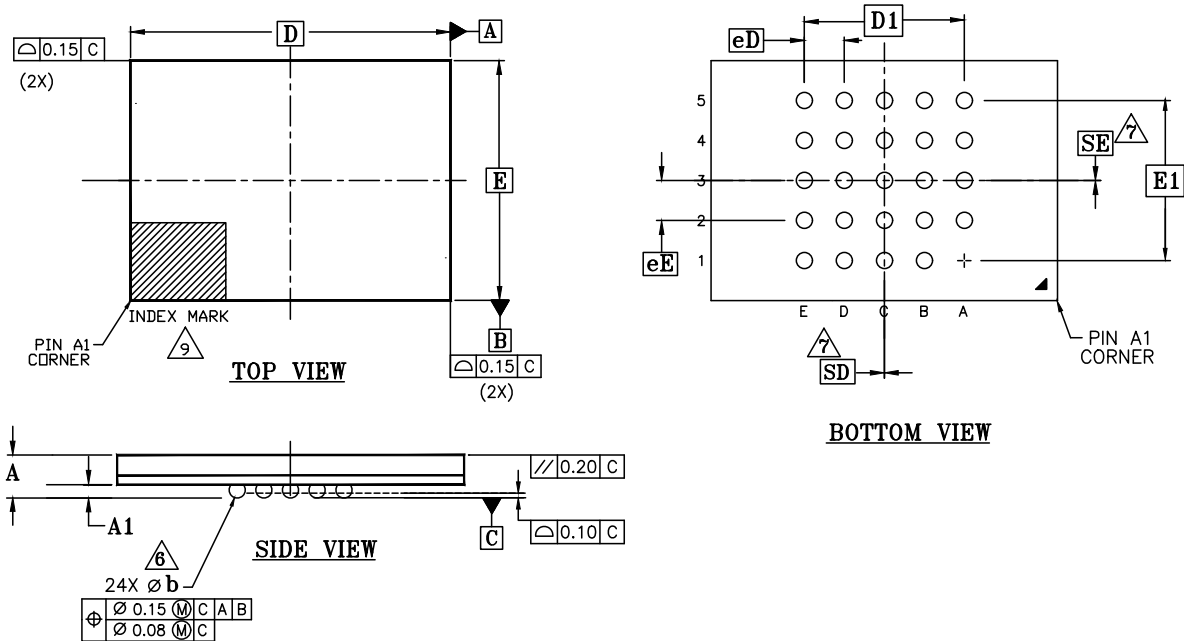


Figure 44 24-ball FBGA, 6 x 8 mm, 5 x 5 ball footprint, top view

## Physical interface

### 11.2 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	4.00 BSC		
E1	4.00 BSC		
MD	5		
ME	5		
N	24		
Ø b	0.35	0.40	0.45
eE	1.00 BSC		
eD	1.00 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

#### NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: MO-234E

002-15550 \*B

Figure 45 24-ball BGA (8.0 × 6.0 × 1.0 mm) VAA024/ELA024/E2A024, package outline (PG-BGA-24)

## Ordering information

## 12 Ordering information

**Table 33** Valid combinations

Product	Package diagram	Packing type	Operating range	Package marking
CYEL18V2563-200BKXE	002-15550	24-ball FBGA	Extended	EL18V2563GBXE

### 12.1 Ordering code definitions

The ordering part number is formed by a valid combination of the following:

CYEL	18	V	256	3	-	200	BK	X	E	
										<b>Temperature range / grade:</b> E = Extended Temperature Range (–40°C to +125°C)
										<b>X</b> = Pb-free
										<b>Package type:</b> BK = 24-ball FBGA, 1.00 mm pitch (5x5 ball footprint)
										<b>Speed:</b> 200 MHz
										<b>Device technology:</b> 2 = HYPERBUS™ 3 = Octal xSPI
										<b>Density:</b> 256 = 256-Mb
										<b>Voltage:</b> V = 1.7 V to 2.0 V
										<b>18</b> = pSRAM
										<b>CY</b> = CYPRESS (an Infineon company) <b>EL</b> = Enhanced Commercial for LEO

#### Note

56.All these parts are Pb-free. Contact your local Infineon sales representative for availability of these parts.

Acronyms

# 13 Acronyms

Table 34 Acronyms used in this document

Acronym	Description
CMOS	complementary metal oxide semiconductor
DCARS	DDR Center-Aligned Read Strobe
DDR	double data rate
DPD	deep power down
DRAM	dynamic RAM
HS	hybrid sleep
MSb	most significant bit
POR	power-on reset
PSRAM	pseudo static RAM
PVT	process, voltage, and temperature
RWDS	read-write data strobe
SPI	serial peripheral interface
xSPI	expanded serial peripheral interface

Document conventions

14 Document conventions

14.1 Units of measure

Table 35 Units of measure

Symbol	Unit of measure
°C	degree celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



Revision history

Revision history

Document revision	Date	Description of changes
**	2025-01-21	Initial release

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2025-01-21**

**Published by**

**Infineon Technologies AG  
81726 Munich, Germany**

**© 2025 Infineon Technologies AG.  
All Rights Reserved.**

**Do you have a question about this document?**

**Email:**  
[erratum@infineon.com](mailto:erratum@infineon.com)

**Document reference  
002-40987 Rev. \*\***

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.