

# 256 Kb (32K × 8) serial (I<sup>2</sup>C) radiation tolerant F-RAM

32K × 8, 3.4 MHz, Automotive grade

## Features

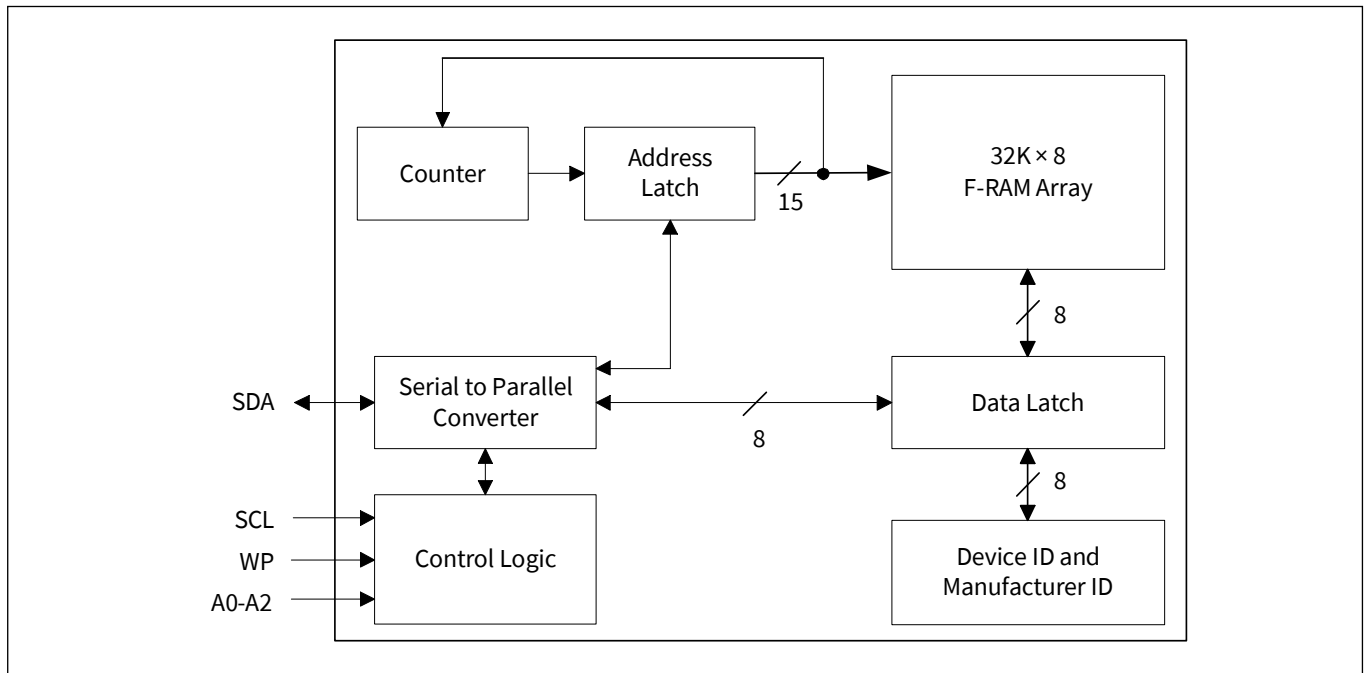
- 256-Kb ferroelectric random access memory (F-RAM) logically organized as 32K × 8
  - High-endurance 10 trillion (10<sup>13</sup>) read/writes
  - 121-year data retention (see **“Data retention and endurance”** on page 19)
  - No delay writes
  - Advanced high-reliability ferroelectric process
- Fast two-wire serial interface (I<sup>2</sup>C)
  - Up to 3.4 MHz frequency<sup>[1]</sup>
  - Direct hardware replacement for serial EEPROM
  - Supports legacy timings for 100 kHz and 400 kHz
- Device ID
  - Manufacturer ID and Product ID
- Low power consumption
  - 500 μA Active current at 100 kHz
  - 500 μA Standby current
  - 12 μA Sleep mode current
- Low-voltage operation: V<sub>DD</sub> (2.0 V to 3.6 V)
- Automotive AEC-Q100 Grade 1 temperature: -40°C to +125°C
- 8-pin small outline integrated circuit (SOIC) package
- Restriction of Hazardous Substances (RoHS) compliant
- Guaranteed TID radiation performance of 50 krad by radiation lot acceptance testing (RLAT)
- Single event latchup immunity >69 LET (125°C)
- Single lot date code and 100% guaranteed electrical testing
- Encapsulated plastic component for low-earth orbit satellite applications

## Note

1. The CYEL15B256J does not meet the NXP I<sup>2</sup>C specification in the Fast-mode Plus (Fm+, 1 MHz) for I<sub>OL</sub> and in the High Speed mode (Hs-mode, 3.4 MHz) for V<sub>hys</sub>. See to **“DC electrical characteristics”** on page 18 for more details.

Logic block diagram

Logic block diagram



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## **1 Functional description**

The CYEL15B256J is a 256-Kb nonvolatile memory employing an advanced ferroelectric process. An F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 121 years while eliminating the complexities, overhead, and system-level reliability problems caused by EEPROM and other nonvolatile memories.

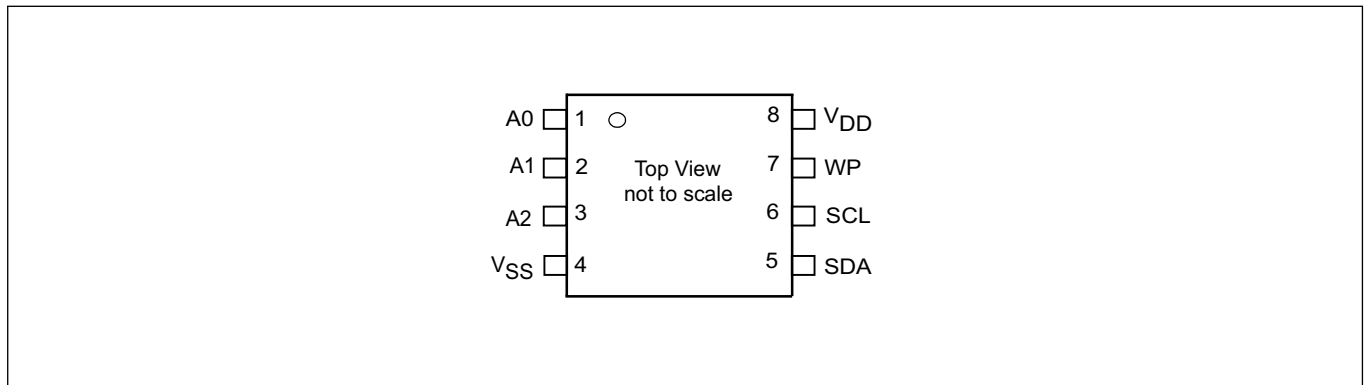
Unlike EEPROM, the CYEL15B256J performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. F-RAM also exhibits much lower power during writes than EEPROM because write operations do not require an internally elevated power supply voltage for write circuits. The CYEL15B256J is capable of supporting  $10^{13}$  read/write cycles, or 10 million times more write cycles than EEPROM.

These capabilities make the CYEL15B256J ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data logging, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The CYEL15B256J provides substantial benefits to users of serial EEPROM as a hardware drop-in replacement. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an Automotive AEC-Q100 Grade 1 temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Pinout

## 2 Pinout



**Figure 1** 8-pin SOIC pinout

**Table 1** Pin definitions

| Pin name | I/O type         | Description  |
|----------|------------------|--|
| A0–A2    | Input            | <b>Device select address 0–2.</b> These pins are used to select one of up to eight devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.   |
| SDA      | Input/<br>Output | <b>Serial data address.</b> This is a bidirectional pin for the two-wire interface. It is open-drain and is intended to be wire-AND'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required. |
| SCL      | Input            | <b>Serial clock.</b> The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.   |
| WP       | Input            | <b>Write protect.</b> When tied to $V_{DD}$ , addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses are write enabled. This pin is pulled down internally.   |
| $V_{SS}$ | Power supply     | Ground for the device. Must be connected to the ground of the system.  |
| $V_{DD}$ | Power supply     | Power supply input to the device.  |

### **3 Functional overview**

The CYEL15B256J is a serial F-RAM memory. The memory array is logically organized as 32,768 × 8 bits and is accessed using a two-wire (I<sup>2</sup>C) interface. The functional operation of the F-RAM is similar to serial EEPROM. The major difference between the CYEL15B256J and a serial EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

## 4 Memory architecture

When accessing the CYEL15B256J, the user addresses 32K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish other non-memory devices) and a two-byte address. The upper MSB bit of the address range is 'don't care' value. The complete address of 15 bits specifies each byte address uniquely.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the two-wire bus. Unlike a serial EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in [“Memory operation”](#) on page 12.

**Two-wire interface**

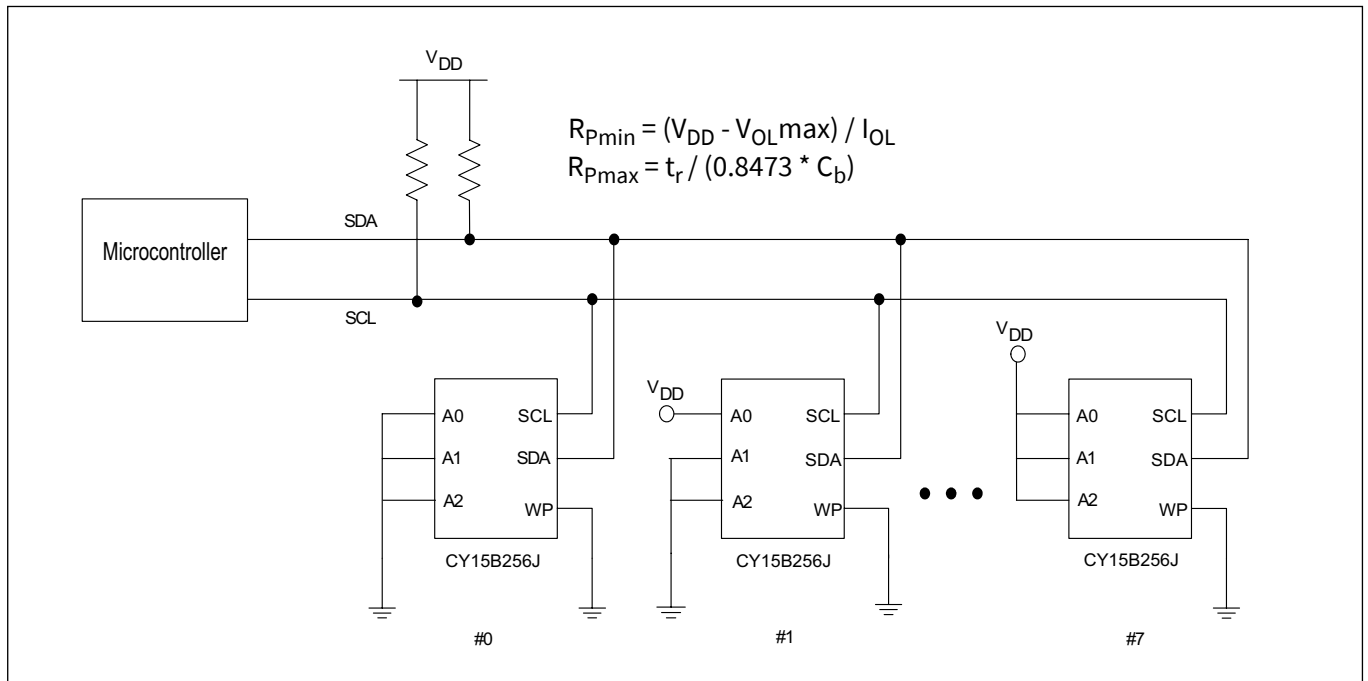
## 5 Two-wire interface

The CYEL15B256J employs a bidirectional two-wire bus protocol using few pins or board space. **Figure 2** illustrates a typical system configuration using the CYEL15B256J in a microcontroller-based system. The two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data to the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The CYEL15B256J is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. **Figure 3** and **Figure 4** illustrate the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

The CYEL15B256J does not meet the NXP I<sup>2</sup>C specification in the Fast-mode Plus (Fm+, 1 MHz) for I<sub>OL</sub> and in the High Speed mode (Hs-mode, 3.4 MHz) for V<sub>hys</sub>. See to “**DC electrical characteristics**” on page 18 for more details.



**Figure 2 System configuration using serial (I<sup>2</sup>C) F-RAM**

### 5.1 STOP condition (P)

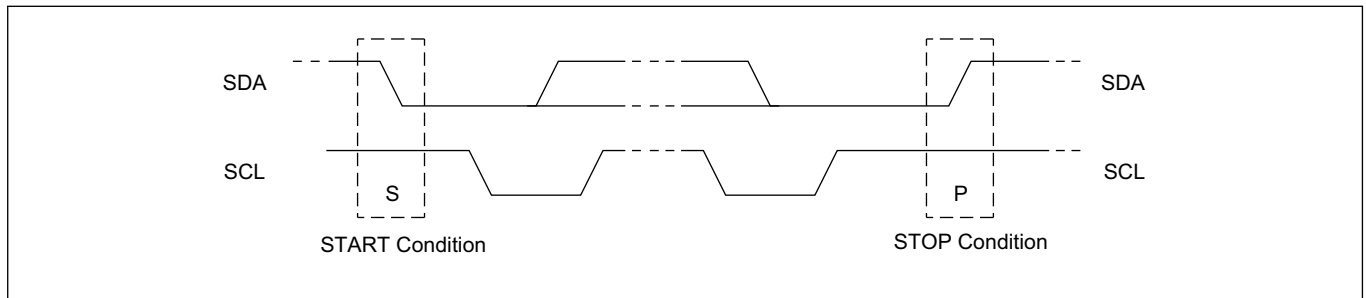
A STOP condition is indicated when the bus master drives SDA from low to HIGH while the SCL signal is HIGH. All operations using the CYEL15B256J should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of the SDA (not a memory read) to assert a STOP condition.

### 5.2 START condition (S)

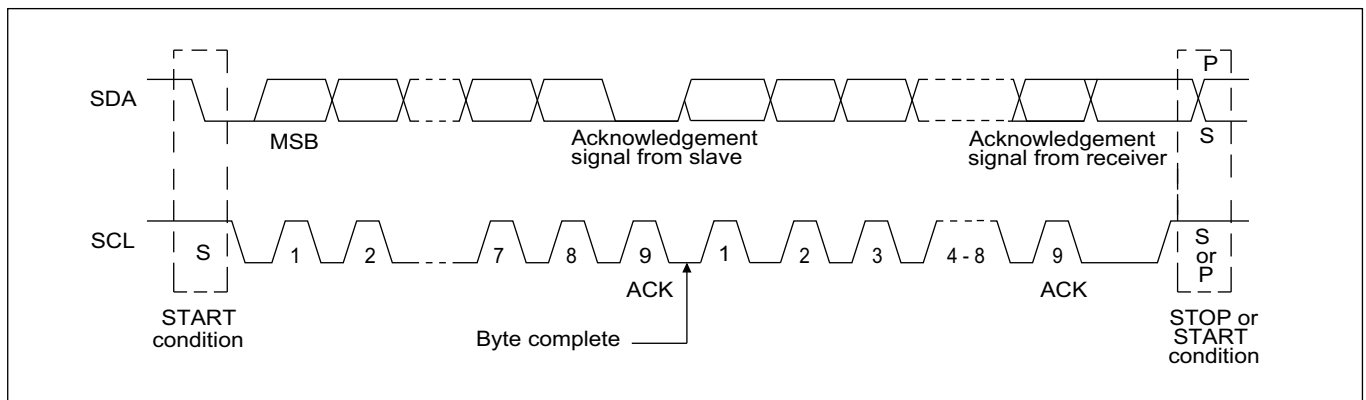
A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the CYEL15B256J for a new operation.

**Two-wire interface**

If the power supply drops below the specified  $V_{DD}$  minimum during operation, the system should issue a START condition prior to performing another operation.



**Figure 3 START and STOP conditions**



**Figure 4 Data transfer on the I<sup>2</sup>C bus**

**5.3 Data/Address transfer**

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

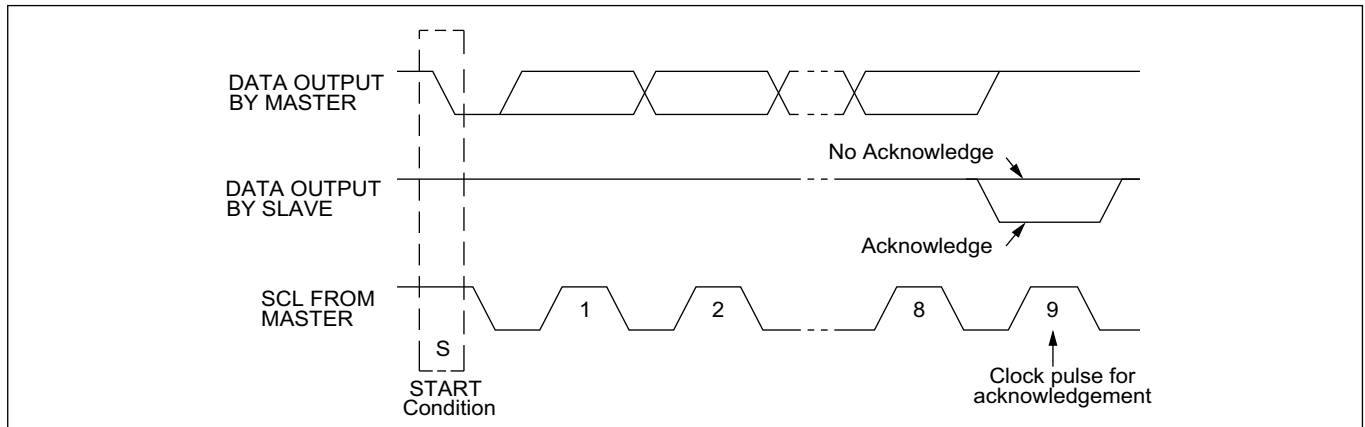
**5.4 Acknowledge/No-acknowledge**

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver will fail to acknowledge for two distinct reasons, the first being that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

The second and most common reason is that, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the CYEL15B256J will continue to place data on the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this causes the CYEL15B256J to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

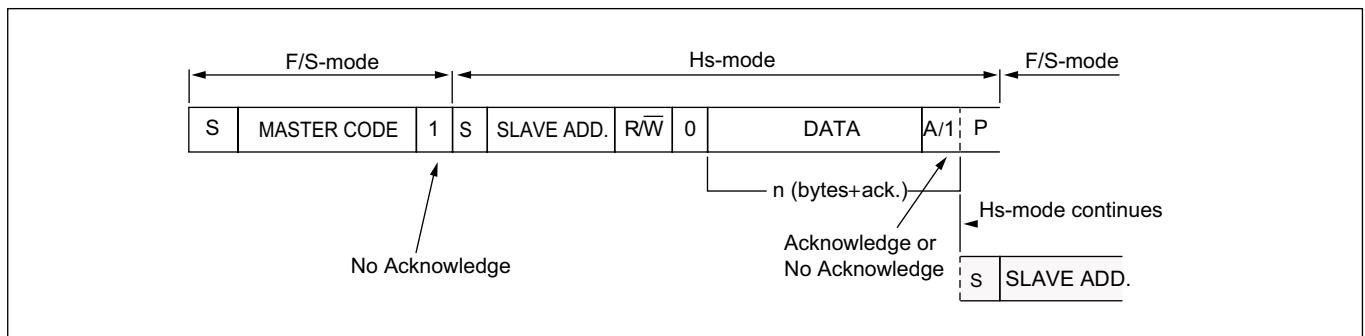
**Two-wire interface**



**Figure 5 Acknowledge on the I<sup>2</sup>C bus**

**5.5 High Speed mode (Hs-mode)**

The CYEL15B256J supports a 3.4 MHz High Speed mode (Hs-mode). A master code (00001XXXb) must be issued to place the device into the High Speed mode. Communication between master and slave will then be enabled for speeds up to 3.4 MHz. A STOP condition will exit Hs-mode. Single- and multiple-byte reads and writes are supported.

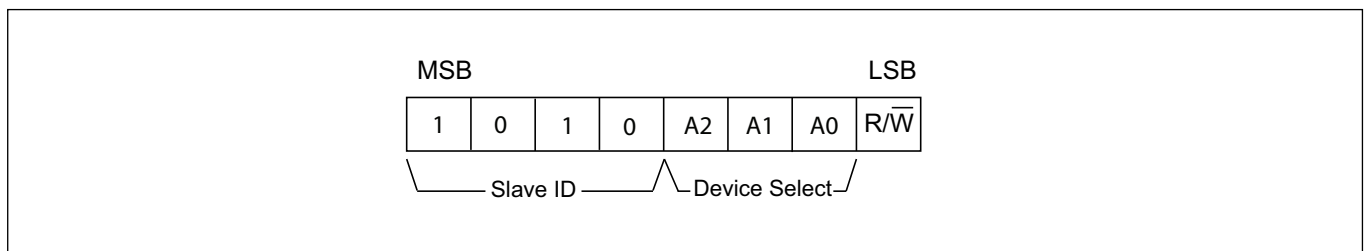


**Figure 6 Data transfer format in Hs-mode**

**5.6 Slave device address**

The first byte that the CYEL15B256J expects after a START condition is the slave address. As shown in [Figure 7](#), the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

Bits 7–4 are the device type (slave ID) and should be set to 1010b for the CYEL15B256J. These bits allow other function types to reside on the two-wire bus within an identical address range. Bits 3–1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to eight CYEL15B256J devices can reside on the same two-wire bus by assigning a different address to each. Bit 0 is the read/write bit (R/W). R/W = '1' indicates a read operation and R/W = '0' indicates a write operation.



**Figure 7 Memory Slave device address**

## **5.7 Addressing overview**

After the CYEL15B256J (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the CYEL15B256J increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

## **5.8 Data transfer**

After the address bytes have been transmitted, data transfer between the bus master and the CYEL15B256J can begin. For a read operation the CYEL15B256J will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the CYEL15B256J will transfer the next sequential byte. If the acknowledge is not sent, the CYEL15B256J will end the read operation. For a write operation, the CYEL15B256J will accept 8 data bits from the master then sends an acknowledge. All data transfer occurs at most significant bit (MSB) first.

**Memory operation**

## 6 Memory operation

The CYEL15B256J is designed to operate in a manner very similar to other two-wire interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the CYEL15B256J and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

### 6.1 Write operation

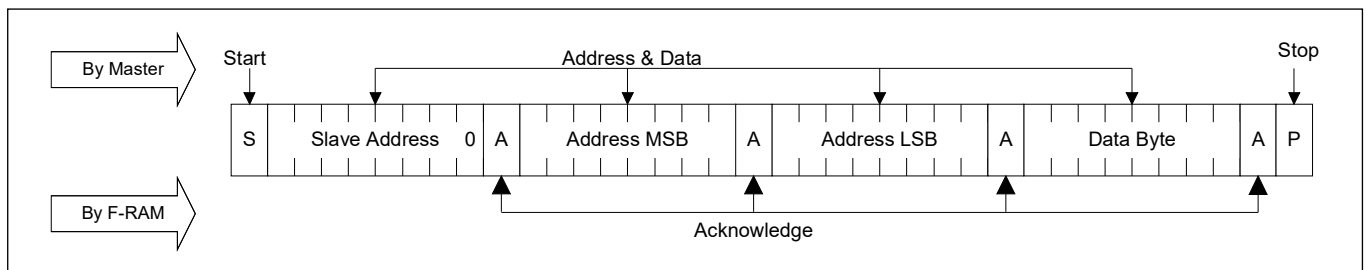
All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/W bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

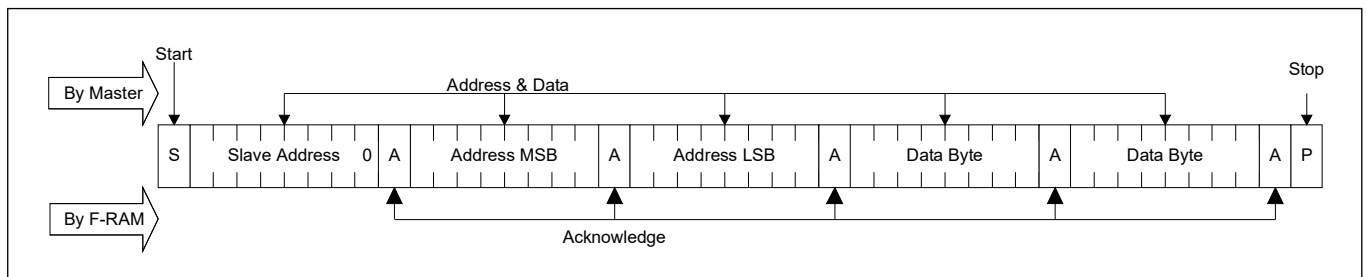
Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The CYEL15B256J uses no page buffering.

The memory array can be write-protected using the WP pin. Setting the WP pin to a HIGH condition ( $V_{DD}$ ) will write-protect all addresses. The CYEL15B256J will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a LOW state ( $V_{SS}$ ) will disable the write protect. WP is pulled down internally.

**Figure 8** and **Figure 9** below illustrate a single-byte and multiple-byte write cycles in Fast-mode Plus (Fm+). **Figure 10** illustrates a single-byte write cycles in Hs-mode.

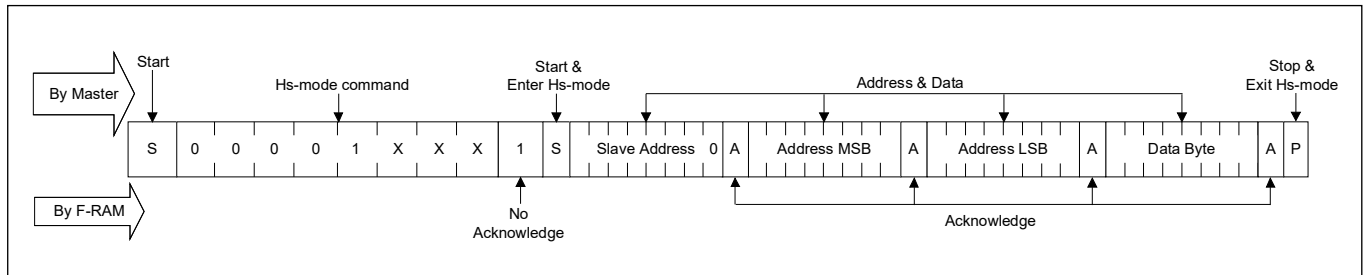


**Figure 8 Single-byte write**



**Figure 9 Multi-byte write**

**Memory operation**



**Figure 10 Hs-mode-byte write**

**6.2 Read operation**

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the CYEL15B256J uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

**6.2.1 Current address & sequential read**

As mentioned above the CYEL15B256J uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the CYEL15B256J will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

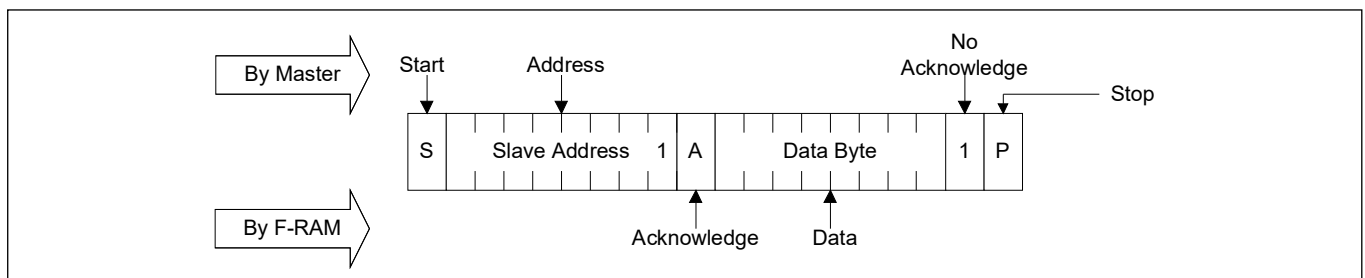
Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

**Note** Each time the bus master acknowledges a byte, this indicates that the CYEL15B256J should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the CYEL15B256J attempts to read out additional data onto the bus. The four valid methods are:

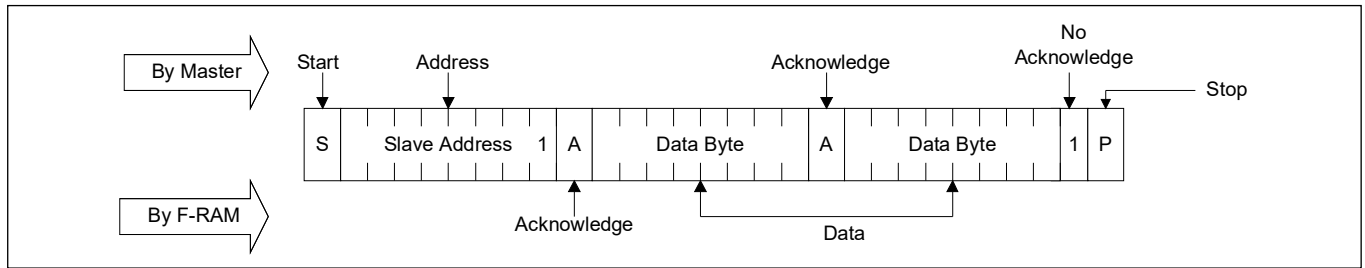
1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. **Figure 11** and **Figure 12** below show the proper operation for current address reads.

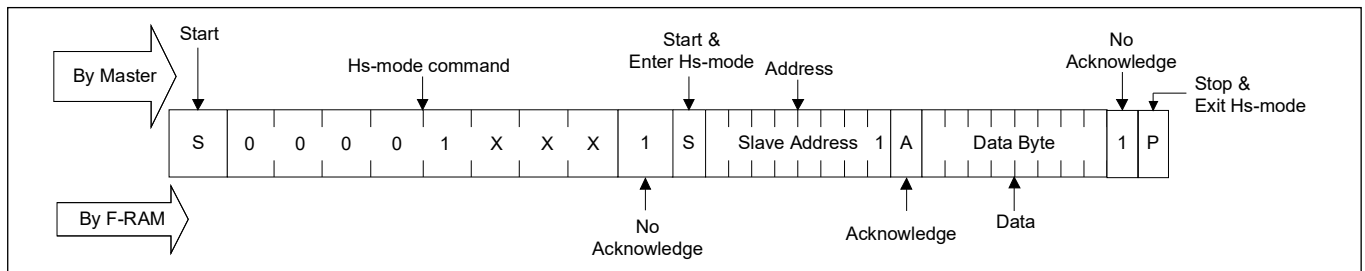


**Figure 11 Current address read**

**Memory operation**



**Figure 12 Sequential read**

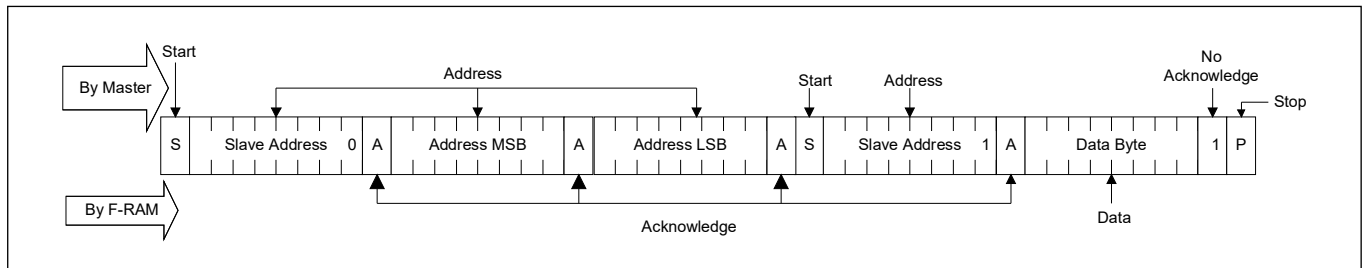


**Figure 13 Hs-mode current address read**

**6.2.2 Selective (Random) read**

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB ( $R/\bar{W}$ ) set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the CYEL15B256J acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.



**Figure 14 Selective (Random) read**

**6.3 Sleep mode**

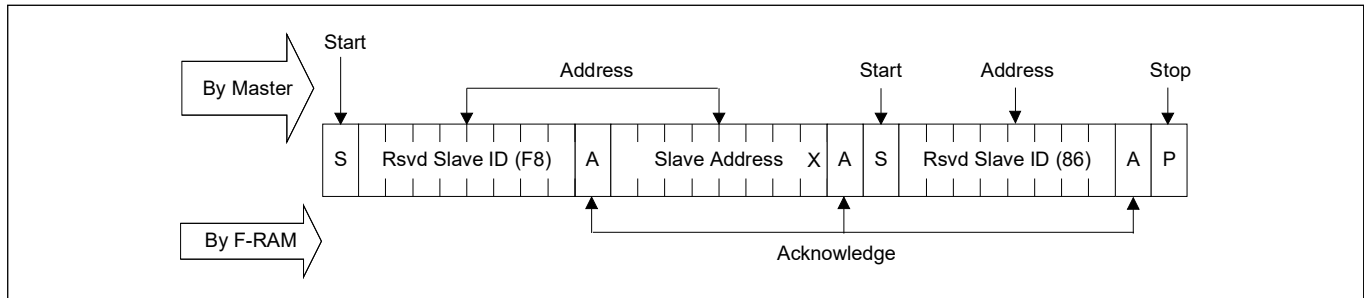
A low-power mode called Sleep mode is implemented on the CYEL15B256J device. The device will enter this low-power state when the Sleep command 86h is clocked-in. Sleep mode entry can be entered as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The CYEL15B256J sends an ACK.
4. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value ( $R/\bar{W}$  bit). Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
5. The CYEL15B256J sends an ACK.

**Memory operation**

6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0x86.
8. The CYEL15B256J sends an ACK.
9. The master sends STOP to ensure the device enters Sleep mode.

Once in Sleep mode, the device draws  $I_{ZZ}$  current, but the device continues to monitor the I<sup>2</sup>C pins. Once the master sends a Slave Address that the CYEL15B256J identifies, it will “wakeup” and be ready for normal operation within  $t_{REC}$  (400  $\mu$ s max.). As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK. While the device is waking up, it will NACK the master until it is ready.



**Figure 15 Sleep mode entry**

**Device ID**

## 7 Device ID

The CYEL15B256J device incorporates a means of identifying the device by providing three bytes of data, which are manufacturer, product ID, and die revision. The Device ID is read-only. It can be accessed as follows:

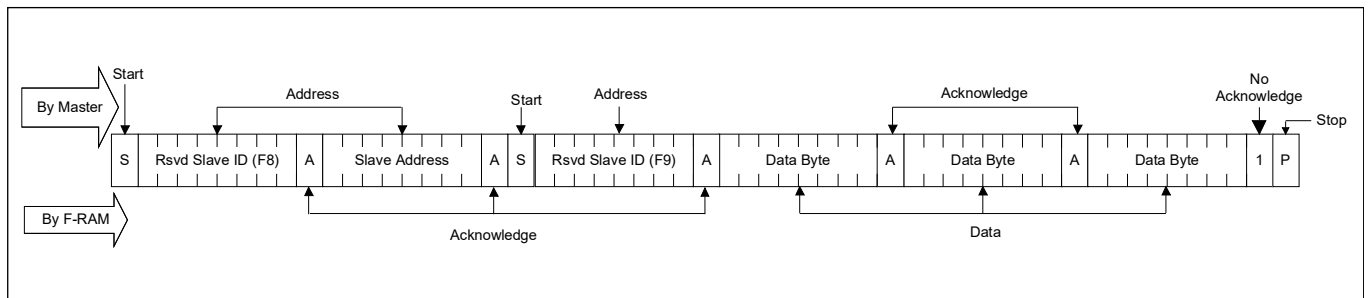
1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The CYEL15B256J sends an ACK.
4. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
5. The CYEL15B256J sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0xF9.
8. The CYEL15B256J sends an ACK.
9. The Device ID read can be done, starting with the 12 manufacturer bits, followed by the 9 part identification bits, and then the 3-die revision bits.
10. The master ends the Device ID read sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

**Note** The reading of the Device ID can be stopped anytime by sending a NACK command.

**Table 2 Device ID**

| Device ID<br>(3 bytes) | Device ID description |                  |                 |                 |
|------------------------|-----------------------|------------------|-----------------|-----------------|
|                        | 23–12<br>(12 bits)    | 11–8<br>(4 bits) | 7–3<br>(5 bits) | 2–0<br>(3 bits) |
|                        | Manufacturer ID       | Product ID       |                 |                 |
| Density                |                       | Variation        | Die rev         |                 |
| 004231h                | 000000000100          | 0010             | 00110           | 001             |

**Note** Product ID bits 0 and 4 are reserved.



**Figure 16 Read device ID**

**Maximum ratings**

## 8 Maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

**Table 3 Maximum ratings**

| Parameter  | Maximum ratings                                |
|--|--|
| Storage temperature  | -65°C to +150°C                                |
| <b>Maximum accumulated storage time</b>                                    |  |
| At 150°C ambient temperature   | 1000 h   |
| At 125°C ambient temperature   | 11000 h  |
| At 85°C ambient temperature  | 121 Years                                      |
| Ambient temperature with power applied                                     | -55°C to +125°C                                |
| Input voltage  | -1.0 V to +4.5 V and $V_{IN} < V_{DD} + 1.0 V$ |
| Supply voltage $V_{DD}$ relative to $V_{SS}$                               | -1.0 V to +4.5 V                               |
| DC voltage applied to outputs in HI-Z state                                | -0.5 V to $V_{DD} + 0.5 V$                     |
| Transient voltage (< 20 ns) on any pin to ground potential                 | -2.0 V to $V_{DD} + 2.0 V$                     |
| Package power dissipation capability ( $T_A = 25^\circ\text{C}$ )          | 1.0 W  |
| Surface mount lead soldering temperature (3 seconds)                       | +260°C   |
| Electrostatic discharge voltage Human Body Model (JEDEC Std JESD22-A114-B) | 2 kV   |
| Charged Device Model (JEDEC Std JESD22-C101-A)                             | 500 V  |
| Latch-up current   | > 140 mA                                       |

Exception: The " $V_{IN} < V_{DD} + 1.0 V$ " restriction does not apply to the SCL and SDA inputs.

**Table 4 Operating range**

| Range        | Ambient temperature ( $T_A$ ) | $V_{DD}$       |
|--------------|-------------------------------|----------------|
| Automotive-E | -40°C to +125°C               | 2.0 V to 3.6 V |

DC electrical characteristics

## 9 DC electrical characteristics

Over the “Operating range” on page 17

**Table 5 DC electrical characteristics**

| Parameter                       | Description                                 | Test conditions  | Min                        | Typ <sup>[2]</sup>         | Max                        | Unit |    |
|---------------------------------|---|--|----------------------------|----------------------------|----------------------------|------|----|
| V <sub>DD</sub>                 | Power supply                                | –  | 2.0                        | 3.3                        | 3.6                        | V    |    |
| I <sub>DD</sub>                 | Average V <sub>DD</sub> current             | SCL toggling between V <sub>DD</sub> – 0.2 V and V <sub>SS</sub> , other inputs V <sub>SS</sub> or V <sub>DD</sub> – 0.2 V | f <sub>SCL</sub> = 100 kHz | TID = 0 krad               | –                          | 500  | μA |
|                                 |   |  | f <sub>SCL</sub> = 1 MHz   |                            | –                          | 500  | μA |
|                                 |   |  | f <sub>SCL</sub> = 3.4 MHz |                            | –                          | 1000 | μA |
|                                 |   | f <sub>SCL</sub> = 100 kHz   | TID = 50 krad              | –                          | 1000                       | μA   |    |
|                                 |   |  |                            | f <sub>SCL</sub> = 1 MHz   | –                          | 2000 | μA |
|                                 |   |  |                            | f <sub>SCL</sub> = 3.4 MHz | –                          | 3000 | μA |
| I <sub>SB</sub>                 | V <sub>DD</sub> standby current             | SCL = SDA = V <sub>DD</sub> . All other inputs V <sub>SS</sub> or V <sub>DD</sub> . Stop command issued.                   | –                          | –                          | 500                        | μA   |    |
| I <sub>ZZ</sub>                 | Sleep mode current                          | SCL = SDA = V <sub>DD</sub> . All other inputs V <sub>SS</sub> or V <sub>DD</sub> . Stop command issued.                   | TID = 0 krad               | –                          | –                          | 12   | μA |
|                                 |   |  | TID = 50 krad              | –                          | –                          | 250  | μA |
| I <sub>LI</sub>                 | Input leakage current (Except WP and A2–A0) | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>  | –1                         | –                          | +1                         | μA   |    |
|                                 | Input leakage current (for WP and A2–A0)    | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>  | –1                         | –                          | +100                       | μA   |    |
| I <sub>LO</sub>                 | Output leakage current                      | V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>   | –1                         | –                          | +1                         | μA   |    |
| V <sub>IH</sub>                 | Input HIGH voltage (SDL, SDA)               | –  | 0.75 × V <sub>DD</sub>     | –                          | V <sub>DD(max)</sub> + 0.3 | V    |    |
|                                 | Input HIGH voltage (WP, A2–A0)              | –  | 0.75 × V <sub>DD</sub>     | –                          | V <sub>DD</sub> + 0.3      | V    |    |
| V <sub>IL</sub>                 | Input LOW voltage                           | –  | –0.3                       | –                          | 0.25 × V <sub>DD</sub>     | V    |    |
| V <sub>OL</sub> <sup>[3]</sup>  | Output LOW voltage                          | I <sub>OL</sub> = 3 mA   | –                          | –                          | 0.4                        | V    |    |
|                                 |   | I <sub>OL</sub> = 6 mA   | –                          | –                          | 0.6                        | V    |    |
| R <sub>in</sub> <sup>[4]</sup>  | Input resistance (WP, A2–A0)                | For V <sub>IN</sub> = V <sub>IL(Max)</sub>   | 50                         | –                          | –                          | kΩ   |    |
|                                 |   | For V <sub>IN</sub> = V <sub>IH(Min)</sub>   | 1                          | –                          | –                          | MΩ   |    |
| V <sub>hys</sub> <sup>[5]</sup> | Hysteresis of Schmitt Trigger inputs        | f <sub>SCL</sub> = 100 kHz, 400 kHz, 1 MHz   | 0.05 × V <sub>DD</sub>     | –                          | –                          | V    |    |
|                                 |   | f <sub>SCL</sub> = 3.4 MHz   | 0.06 × V <sub>DD</sub>     | –                          | –                          | V    |    |

**Notes**

- Typical values are at 25°C, V<sub>DD</sub> = V<sub>DD(typ)</sub>. Not 100% tested.
- The CYEL15B256J does not meet the NXP I<sup>2</sup>C specification in the Fast-mode Plus (Fm+, 1 MHz) for I<sub>OL</sub> of 20 mA at a V<sub>OL</sub> of 0.4 V.
- The input pull-down circuit is strong (50 kΩ) when the input voltage is below V<sub>IL</sub> and weak (1 MΩ) when the input voltage is above V<sub>IH</sub>.
- The CYEL15B256J does not meet the NXP I<sup>2</sup>C specification in the High Speed Mode (Hs-mode, 3.4 MHz) for V<sub>hys</sub> of 0.1 × V<sub>DD</sub>.

**DC electrical characteristics**

**Table 6 Data retention and endurance**

| Parameter       | Description    | Test condition             | Min              | Max | Unit   |
|-----------------|----------------|----------------------------|------------------|-----|--------|
| T <sub>DR</sub> | Data retention | T <sub>A</sub> = 125°C     | 11000            | –   | Hours  |
|                 |                | T <sub>A</sub> = 105°C     | 11               | –   | Years  |
|                 |                | T <sub>A</sub> = 85°C      | 121              | –   | Years  |
| NV <sub>C</sub> | Endurance      | Over operating temperature | 10 <sup>13</sup> | –   | Cycles |

Example of an F-RAM lifetime

## 10 Example of an F-RAM lifetime

An application does not operate under a steady temperature for the entire usage lifetime of the application. Instead, it is often expected to operate in multiple temperature environments throughout the application's usage lifetime. Accordingly, the retention specification for F-RAM in applications often needs to be calculated cumulatively. An example calculation for a multi-temperature thermal profiles is given below.

**Table 7 Multi-temperature thermal profiles**

| Temperature (T) | Time factor (t) | Acceleration factor with respect to Tmax (A) [6]  | Profile factor (P) | Profile lifetime, L (P)  |
|-----------------|-----------------|---|--------------------|--|
|                 |                 | $A = \frac{L(T)}{L(T_{max})} = e^{\frac{Ea}{k} \left( \frac{1}{T} - \frac{1}{T_{max}} \right)}$ |                    | $P = \frac{1}{\left( \frac{t1}{A1} + \frac{t2}{A2} + \frac{t3}{A3} + \frac{t4}{A4} \right)}$ |
| T1 = 125°C      | t1 = 0.1        | A1 = 1  | 8.33               | >10.46 years   |
| T2 = 105°C      | t2 = 0.15       | A2 = 8.67   |                    |  |
| T3 = 85°C       | t3 = 0.25       | A3 = 95.68  |                    |  |
| T4 = 55°C       | t4 = 0.50       | A4 = 6074.80  |                    |  |

**Table 8 Capacitance**

| Parameter [7]   | Description                        | Test conditions   | Max | Unit |
|-----------------|------------------------------------|---|-----|------|
| C <sub>IO</sub> | Input/Output pin capacitance (SDA) | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = V <sub>DD</sub> (typ) | 8   | pF   |
| C <sub>I</sub>  | Input pin capacitance              |   | 6   | pF   |

**Table 9 Thermal resistance**

| Parameter [7]   | Description                              | Test conditions  | 8-pin SOIC | Unit |
|-----------------|--|--|------------|------|
| Θ <sub>JA</sub> | Thermal resistance (junction-to-ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 146        | °C/W |
| Θ <sub>JC</sub> | Thermal resistance (junction-to-case)    |  | 48         | °C/W |

**Notes**

- Where k is the Boltzmann constant 8.617 × 10<sup>-5</sup> eV/K, T<sub>max</sub> is the highest temperature specified for the product, and T is any temperature within the F-RAM product specification. All temperatures are in Kelvin in the equation.
- This parameter is periodically sampled and not 100% tested.

## 11 AC test loads and waveforms

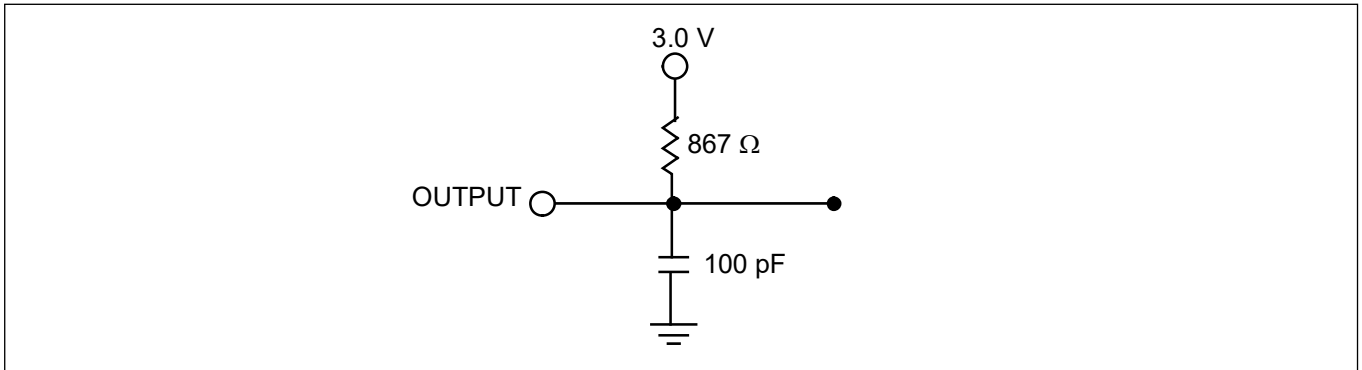


Figure 17 AC test loads and waveforms

Table 10 AC test condition parameters

| Test conditions parameters               | Range values            |
|--|-------------------------|
| Input pulse levels                       | 10% and 90% of $V_{DD}$ |
| Input rise and fall times                | 10 ns                   |
| Input and output timing reference levels | $0.5 \times V_{DD}$     |
| Output load capacitance                  | 100 pF                  |

AC switching characteristics

## 12 AC switching characteristics

Over the “Operating range” on page 17

**Table 11 AC switching characteristics**

| Parameters <sup>[8]</sup>       |                       | Description  | Fast-mode Plus (Fm+) <sup>[10]</sup> |     | Hs-mode <sup>[10]</sup> |     | Unit |
|---------------------------------|-----------------------|--|--------------------------------------|-----|-------------------------|-----|------|
| Infineon parameter              | Alt parameter         |  | Min                                  | Max | Min                     | Max |      |
| f <sub>SCL</sub> <sup>[9]</sup> |                       | SCL clock frequency  | –                                    | 1.0 | –                       | 3.4 | MHz  |
| t <sub>SU;STA</sub>             |                       | Start condition setup for repeated Start                         | 260                                  | –   | 160                     | –   | ns   |
| t <sub>HD;STA</sub>             |                       | Start condition hold time  | 260                                  | –   | 160                     | –   | ns   |
| t <sub>LOW</sub>                |                       | Clock LOW period   | 500                                  | –   | 160                     | –   | ns   |
| t <sub>HIGH</sub>               |                       | Clock HIGH period  | 260                                  | –   | 60                      | –   | ns   |
| t <sub>SU;DAT</sub>             | t <sub>SU;DATA</sub>  | Data in setup  | 50                                   | –   | 10                      | –   | ns   |
| t <sub>HD;DAT</sub>             | t <sub>HD;DATA</sub>  | Data in hold   | 0                                    | –   | 0                       | 70  | ns   |
| t <sub>DH</sub>                 |                       | Data output hold (from SCL at V <sub>IL</sub> )                  | 0                                    | –   | 0                       | –   | ns   |
| t <sub>R</sub> <sup>[11]</sup>  | t <sub>r</sub>        | Input rise time  | –                                    | 120 | 10                      | 80  | ns   |
| t <sub>F</sub> <sup>[11]</sup>  | t <sub>f</sub>        | Input fall time  | 20 × (V <sub>DD</sub> /5.5 V)        | 120 | 10                      | 80  | ns   |
| t <sub>SU;STO</sub>             |                       | STOP condition setup   | 260                                  | –   | 160                     | –   | ns   |
| t <sub>AA</sub>                 | t <sub>VDD;DATA</sub> | SCL LOW to SDA Data Out Valid                                    | –                                    | 450 | –                       | 130 | ns   |
| t <sub>VDD;ACK</sub>            |                       | ACK output valid time  | –                                    | 450 | –                       | 130 | ns   |
| t <sub>OF</sub> <sup>[11]</sup> |                       | Output fall time from V <sub>IH</sub> min to V <sub>IL</sub> max | 20 × (V <sub>DD</sub> /5.5 V)        | 120 | –                       | 80  | ns   |
| t <sub>BUF</sub>                |                       | Bus free before new transmission                                 | 500                                  | –   | 300                     | –   | ns   |
| t <sub>SP</sub>                 |                       | Noise suppression time constant on SCL, SDA                      | 0                                    | 50  | –                       | 5   | ns   |

### Notes

8. Test conditions assume signal transition time of 10 ns or less, timing reference levels of V<sub>DD</sub>/2, input pulse levels of 0 to V<sub>DD</sub>(typ), and output loading of the specified I<sub>OL</sub> and 100 pF load capacitance shown in [Figure 17](#).
9. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to f<sub>SCL</sub> (max).
10. Bus Load (Cb) considerations; Cb < 550 pF for I<sup>2</sup>C clock frequency (SCL) 1 MHz; Cb < 100 pF for SCL at 3.4 MHz.
11. These parameters are guaranteed by design and are not tested.

AC switching characteristics

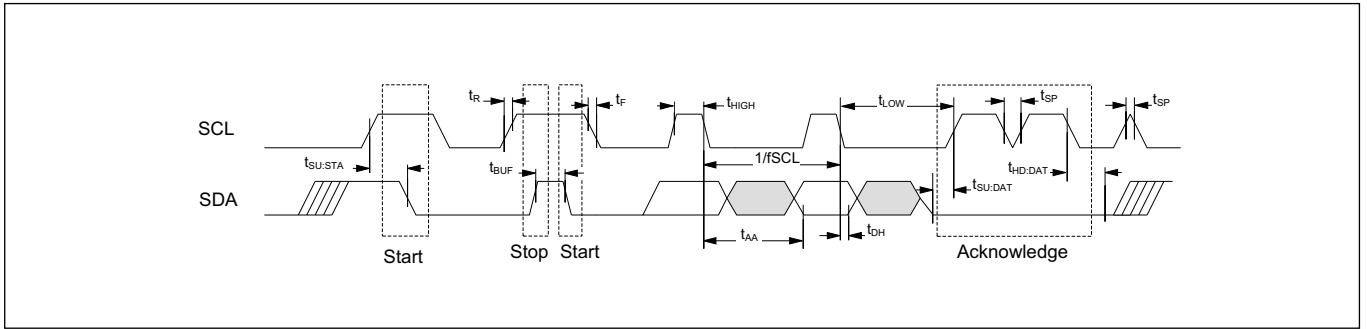


Figure 18 Read bus timing diagram

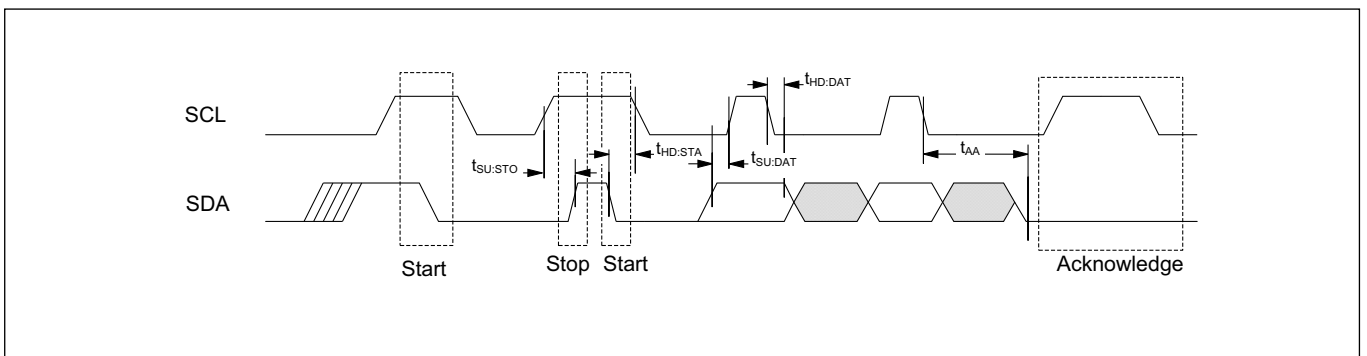


Figure 19 Write bus timing diagram

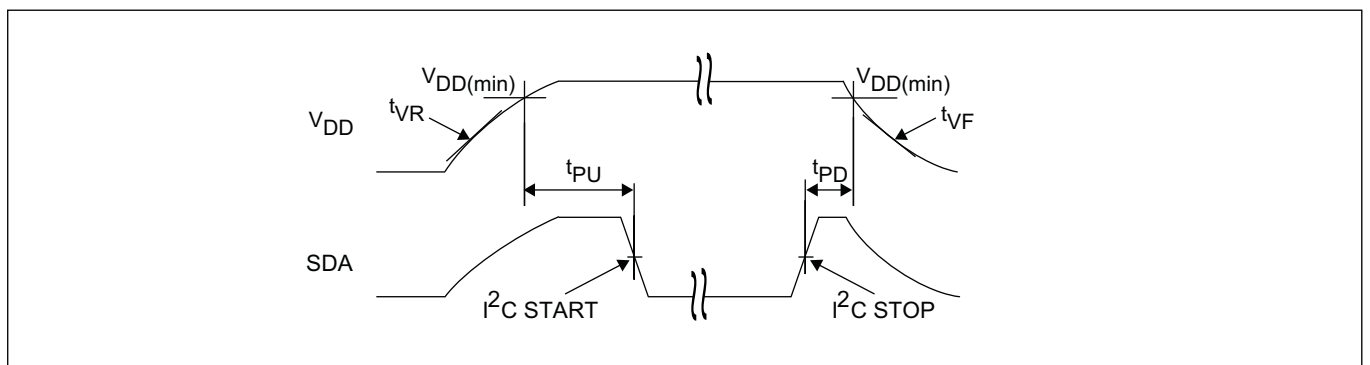
Power cycle timing

### 13 Power cycle timing

Over the “Operating range” on page 17

**Table 12** Power cycle timing parameters

| Parameter           | Description   | Min | Max | Unit                   |
|---------------------|---|-----|-----|------------------------|
| $t_{PU}$            | Power-up $V_{DD}(\text{min})$ to first access (START condition)     | 250 | –   | $\mu\text{s}$          |
| $t_{PD}$            | Last access (STOP condition) to power-down ( $V_{DD}(\text{min})$ ) | 0   | –   | $\mu\text{s}$          |
| $t_{VR}^{[12, 13]}$ | $V_{DD}$ power-up ramp rate   | 50  | –   | $\mu\text{s}/\text{V}$ |
| $t_{VF}^{[12, 13]}$ | $V_{DD}$ power-down ramp rate                                       | 100 | –   | $\mu\text{s}/\text{V}$ |
| $t_{REC}$           | Recovery time from Sleep mode                                       | –   | 400 | $\mu\text{s}$          |



**Figure 20** Power cycle timing

**Notes**

- 12.Slope measured at any point on the  $V_{DD}$  waveform.
- 13.These parameters are guaranteed by design and are not tested.

Ordering information

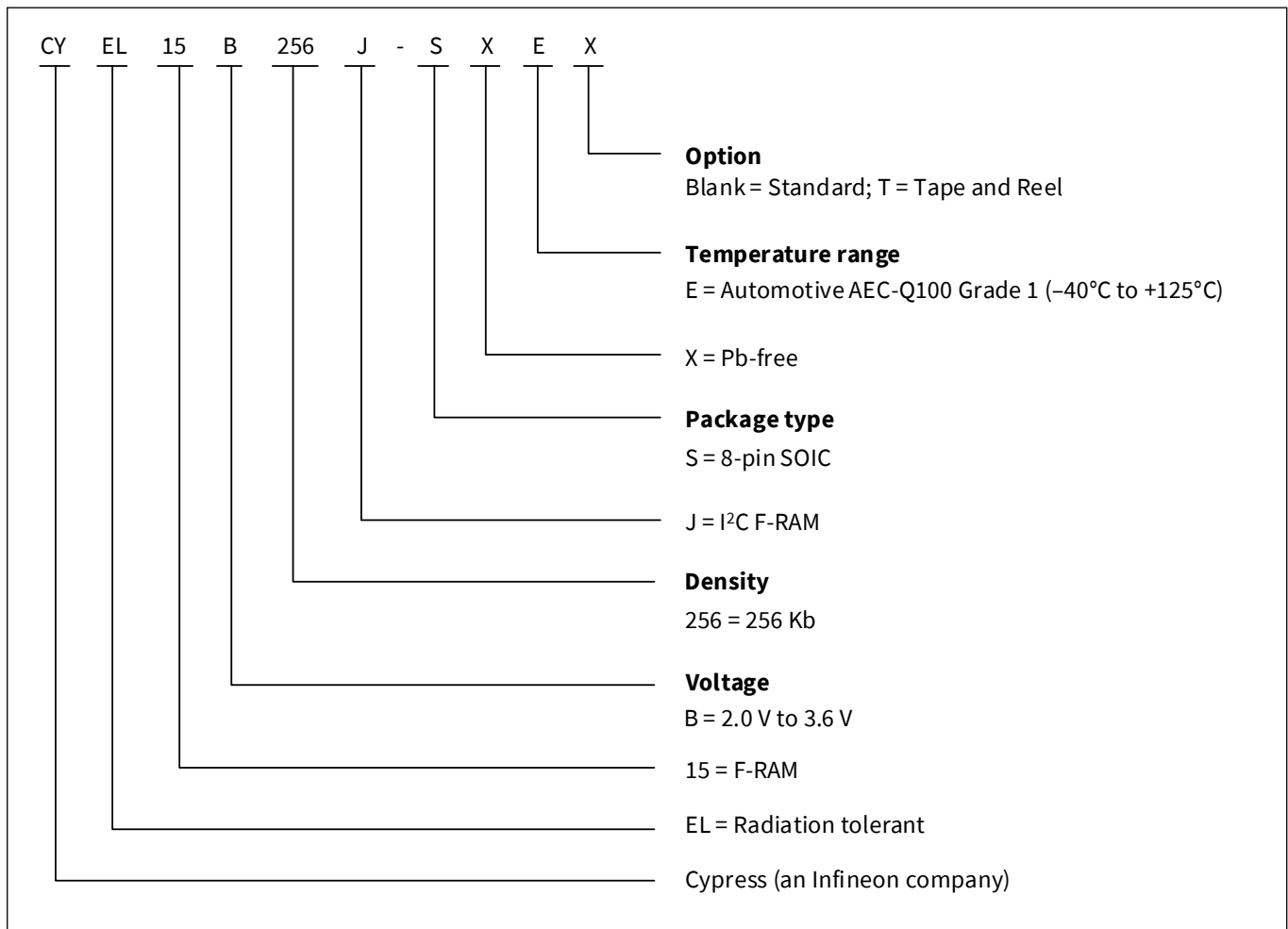
## 14 Ordering information

Table 13 Ordering information

| Product         | Package diagram | Package type | Operating range |
|-----------------|-----------------|--------------|-----------------|
| CYEL15B256J-SXE | 51-85066        | 8-pin SOIC   | Automotive-E    |

All these parts are Pb-free. Contact your local Infineon sales representative for availability of these parts.

### 14.1 Ordering code definition



Package diagram

# 15 Package diagram

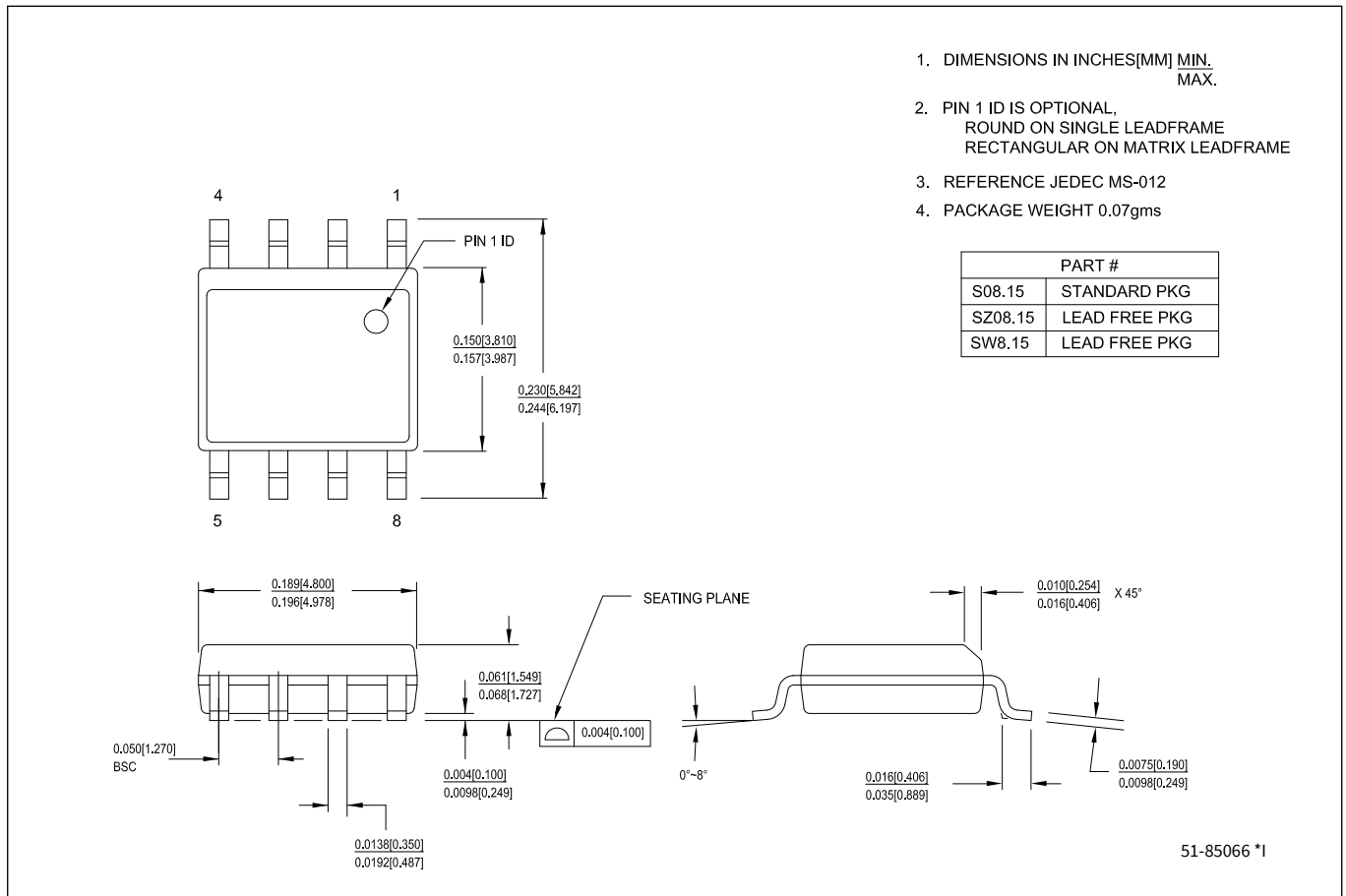


Figure 21 8-pin SOIC (150 mils) package outline (PG-DSO-8)

**Acronyms**

## **16 Acronyms**

**Table 14 Acronyms used in this document**

| <b>Acronym</b>    | <b>Description</b>                         |
|-------------------|--|
| ACK               | acknowledge                                |
| CMOS              | complementary metal oxide semiconductor    |
| EIA               | Electronic Industries Alliance             |
| I <sup>2</sup> C  | Inter-Integrated Circuit                   |
| I/O               | input/output                               |
| JEDEC             | Joint Electron Devices Engineering Council |
| LSB               | least significant bit                      |
| MSB               | most significant bit                       |
| NACK              | no acknowledge                             |
| RoHS              | Restriction of Hazardous Substances        |
| R/ $\overline{W}$ | read/write                                 |
| SCL               | serial clock line                          |
| SDA               | serial data access                         |
| SOIC              | small outline integrated circuit           |
| WP                | write protect                              |

**Document conventions**

## **17 Document conventions**

### **17.1 Units of measure**

**Table 15 Units of measure**

| <b>Symbol</b> | <b>Unit of measure</b> |
|---------------|------------------------|
| °C            | degrees celsius        |
| Hz            | hertz                  |
| Kb            | 1024 bits              |
| kHz           | kilohertz              |
| kΩ            | kilohms                |
| MHz           | megahertz              |
| MΩ            | megaohms               |
| μA            | microamperes           |
| μs            | microseconds           |
| mA            | milliamperes           |
| ms            | milliseconds           |
| ns            | nanoseconds            |
| Ω             | ohms                   |
| %             | percent                |
| pF            | picofarads             |
| V             | volts                  |
| W             | watts                  |

**Revision history**

**Revision history**

| <b>Document revision</b> | <b>Date</b> | <b>Description of changes</b> |
|--------------------------|-------------|-------------------------------|
| *B                       | 2026-03-16  | Publish to web.               |

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