PSOC™ Automotive 4100S MAX

General description

PSOC™ 4 MCU is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. PSOC™ 4100S Max is a member of the PSOC™ 4 MCU platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a multi-sense converter block supporting CAPSENSE™ with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSOC™ 4100S Max products will be upward compatible with members of the PSOC™ 4 MCU platform for new applications and design needs.

Features

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 384 KB of flash with Read Accelerator
  - Up to 32 KB of SRAM
  - 16-channel DMA engine
- Programmable analog
  - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes, and channel sequencer with signal averaging
  - Temperature sensor built into SAR ADC
  - Two low-power comparators that operate in Deep Sleep low-power mode
  - Any GPIO pin can be used for analog ADC sensing
- Programmable digital
  - Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs
- Low-power 1.71 V to 5.5 V operation
  - Deep Sleep mode with operational analog and 2.5 mA digital system current
- Capacitive block
  - Multi-sensing converter (MSC) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance for capacitive sensing
  - Software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- LCD drive capability
  - LCD segment drive capability on GPIOs
- Serial communication
  - Five independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I^2C, SPI, UART functionality, or LIN Slave functionality
- Audio I2S
  - I2S TX Master supported
- Timing and pulse-width modulation
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, edge, and pseudo-random modes

Features

  - Comparator-based triggering of kill signals for motor drive and other high-reliability digital logic applications
  - Quadrature decoder
- Clock sources
  - 4 to 33 MHz external crystal oscillator (ECO)
  - PLL to generate 48-MHz frequency
  - 32-kHz watch crystal oscillator (WCO)
  - ±2% internal main oscillator (IMO)
  - 40-kHz internal low-power oscillator (ILO)
- Cryptography accelerators
  - Hardware acceleration for symmetric and cryptographic methods and hash functions
  - True random number generator (TRNG) function
- CAN FD block
  - CAN FD block operating at up to 5 Mbps
- Temperature range
  - Grade-A: –40°C to +85°C
  - Grade-S: –40°C to +105°C
  - Grade-E: –40°C to +125°C
- Up to 84 programmable GPIO pins
  - 48-pin wettable QFN, 64-pin TQFP, and 100-pin TQFP packages
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable
- ModusToolbox™ TM design environment
  - Integrated Development Environment (IDE) provides configuration, program development, and build with debugging
  - Applications Programming Interface (API) for all fixed-function and programmable peripherals using Peripheral Driver Libraries (PDL)
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools

Errata: For information on silicon errata, see Errata. Details include trigger conditions, devices affected, and proposed workaround

Block diagram

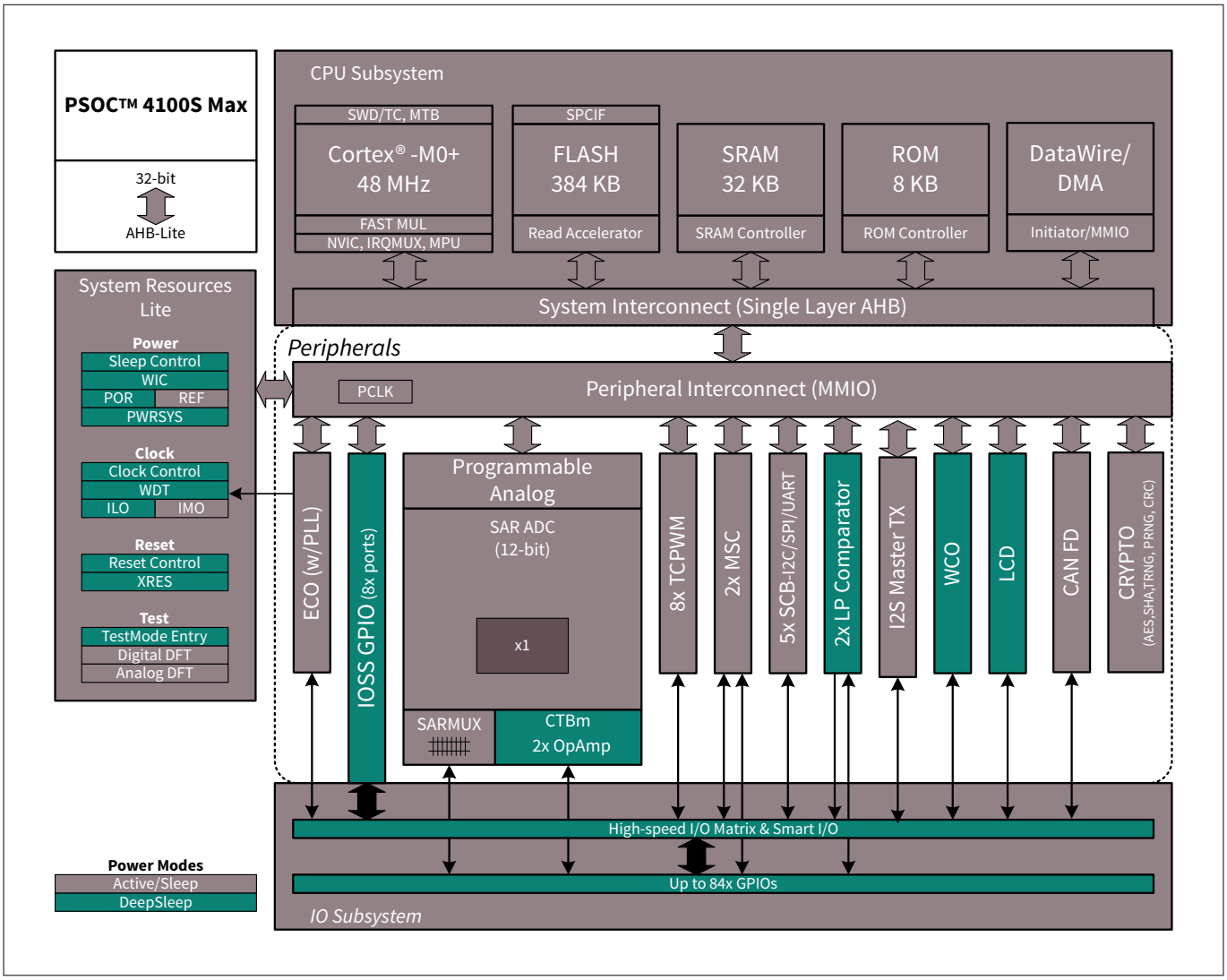

Figure 1 Block diagram

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1 Development ecosystem

There is a wealth of data at www.infineon.com to help you select the right PSOC™ device and quickly and effectively integrate it into your design. For a comprehensive list of resources, see the knowledge base article How to design with PSOC™ 3, PSOC™ 4, and PSOC™ 5LP - KBA86521. The following is an abbreviated, hyperlinked list of resources for PSOC™ 4 MCU:

- Overview:PSOC™ portfolio
- Product selectors:PSOC™ 1,PSOC™ 3, PSOC™ 4, PSOC™ 5LP
- Application notes cover a broad range of topics, from basic to advanced level, and include the following:
  - AN79953: Getting started with PSOC™ 4 MCU
  - AN88619: PSOC™ 4 MCU hardware design considerations
  - AN86439: PSOC™ 4 MCU - Using GPIO pins
  - AN57821 : Mixed signal circuit board layout
  - AN81623 : Digital design best practices
  - AN73854: Introduction to bootloaders
  - AN89610: Arm® Cortex® code optimization
  - AN85951: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide
- Reference manuals provide detailed descriptions of PSOC™ 4 MCU architecture and registers.
- Development kits:
  - CY8CKIT-041S-Max PSOC™ 4100S Max Pioneer Kit enables you to evaluate and develop with Infineon's fifth-generation low-power CAPSENSE™ solution using the PSOC™ 4100S Max devices.

The MiniProg4 device provides an interface for flash programming and debug.

- Development tools:
  - The ModusToolbox™ software enables cross-platform code development with a robust suite of tools and software libraries.
  - PSOC™ 4 CAD libraries provide footprint and schematic support for common tools. BSDL files are also available.
- Online:
  - In addition to print documentation, the Infineon Developer Community page connects you with fellow PSOC™ users and experts in PSOC™ from around the world, 24 hours a day, 7 days a week

2 ModusToolbox™ software

ModusToolbox™ software is a comprehensive collection of multi-platform tools and software libraries that enables an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code repositories on GitHub. This includes:

- Board Support Packages (BSPs) aligned with Infineon kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™, Bluetooth® Low Energy, and mesh networks
- An extensive set of thoroughly tested code example applications

***Note**: The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSOC™ 4 PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control.*

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™.

For information on using Infineon tools, see the documentation delivered with ModusToolbox™ software, and AN79953 - Getting started with PSOC™ 4 MCU.

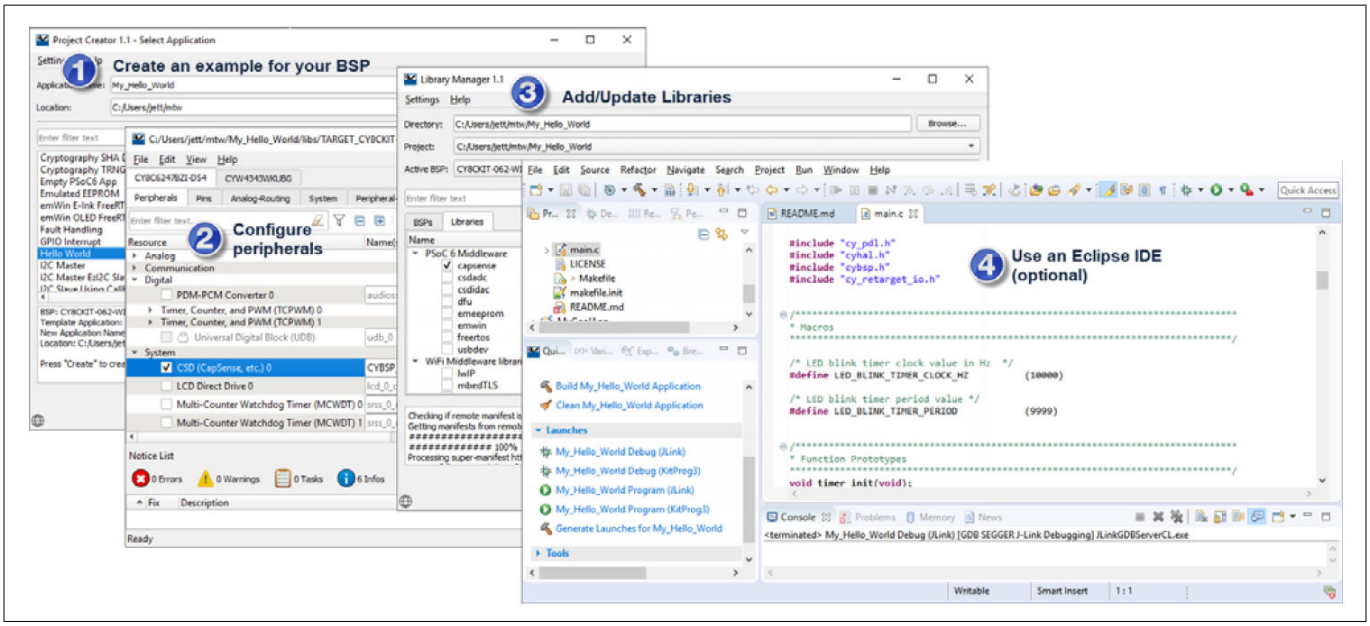


Figure 2 ModusToolbox™ software tools

3 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the Block diagram. For more detailed information, see the following documentation:

- Board Support Package (BSP) documentation
  - BSPs are available on GitHub. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example here. This search link finds all currently available BSPs on the Infineon GitHub site.
- Hardware Abstraction Layer API reference manual
  - The Infineon Hardware Abstraction Layer (HAL) provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The HAL API reference provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.
- Peripheral Driver Library (PDL) Application Programming Interface (API) reference manual
  - The Peripheral Driver Library (PDL) integrates device header files and peripheral drivers into a single package and supports all PSOC™ 4 product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the PDL API reference. Example applications that use the PSOC™ 4 PDL download it automatically from the GitHub repository.

PSOC™ 4100S Max devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® Serial-Wire Debug (SWD) interface supports all programming and debug features of the device. Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox™ IDE provides fully integrated programming and debug support for the PSOC™ 4100S Max devices. The SWD interface is fully compatible with industry-standard third-party tools. PSOC™ 4100S Max provides a level of security not possible with multi-chip application solutions or with microcontrollers.

It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSOC™ 4100S Max, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSOC™ 4100S Max allows the customer to make.

4 Functional definition

4.1 CPU and memory subsystem

4.1.1 CPU

The Cortex®-M0+ CPU in the PSOC™ 4100S Max is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU subsystem includes an 16-channel DMA engine and also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG. The debug configuration used for PSOC™ 4100S Max has four breakpoint (address) comparators and two watchpoint (data) comparators.

4.1.2 Flash

The PSOC™ 4100S Max device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

4.1.3 SRAM

32 KB of SRAM are provided with zero wait-state access at 48 MHz.

4.1.4 SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided

4.2 System resources

4.2.1 Power system

The power system is described in detail in the section Power. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brownout detection). PSOC™ 4100S Max operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSOC™ 4100S Max provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

4.2.2 Clock system

The PSOC™ 4100S Max clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSOC™ 4100S Max consists of the IMO, ILO, a 32-kHz Watch Crystal Oscillator (WCO), MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

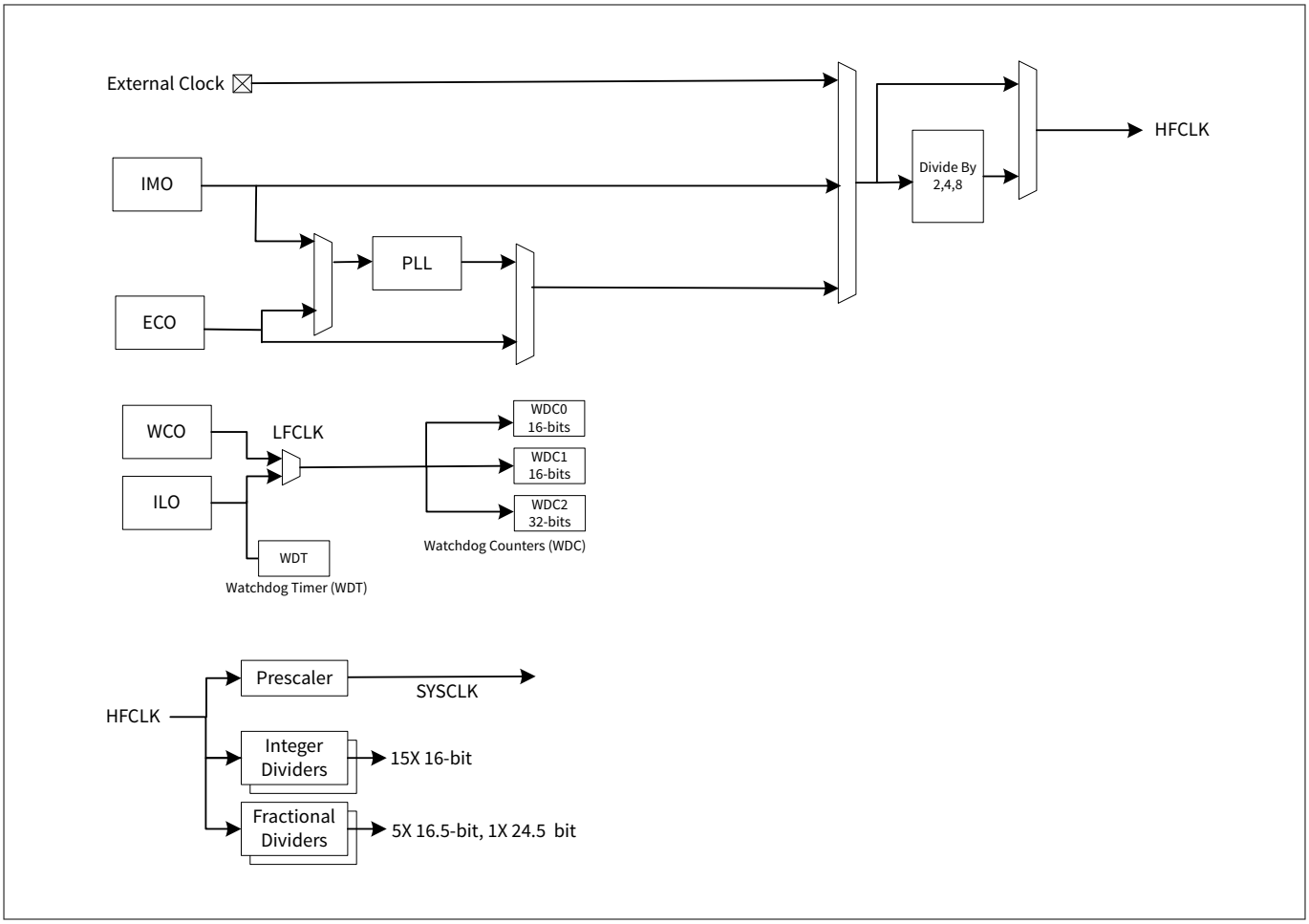


Figure 3 PSOC™ 4100S Max MCU clocking architecture

The HFCLK signal can be divided down as shown to generate synchronous clocks for the analog and digital peripherals. There are 21 clock dividers for the PSOC™ 4100S Max (six with fractional divide capability, fifteen with integer divide only). The fifteen 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

4.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSOC™ 4100S Max. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is ±2% over the entire voltage and temperature range.

4.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

4.2.5 Watch crystal oscillator (WCO)

The PSOC™ 4100S Max clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

4.2.6 External crystal oscillator (ECO)

The PSOC™ 4100S Max also implements a 4 to 33 MHz crystal oscillator.

4.2.7 Watchdog timer (WDT) and counter

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

4.2.8 Reset

PSOC™ 4100S Max can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

4.3 Analog blocks

4.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

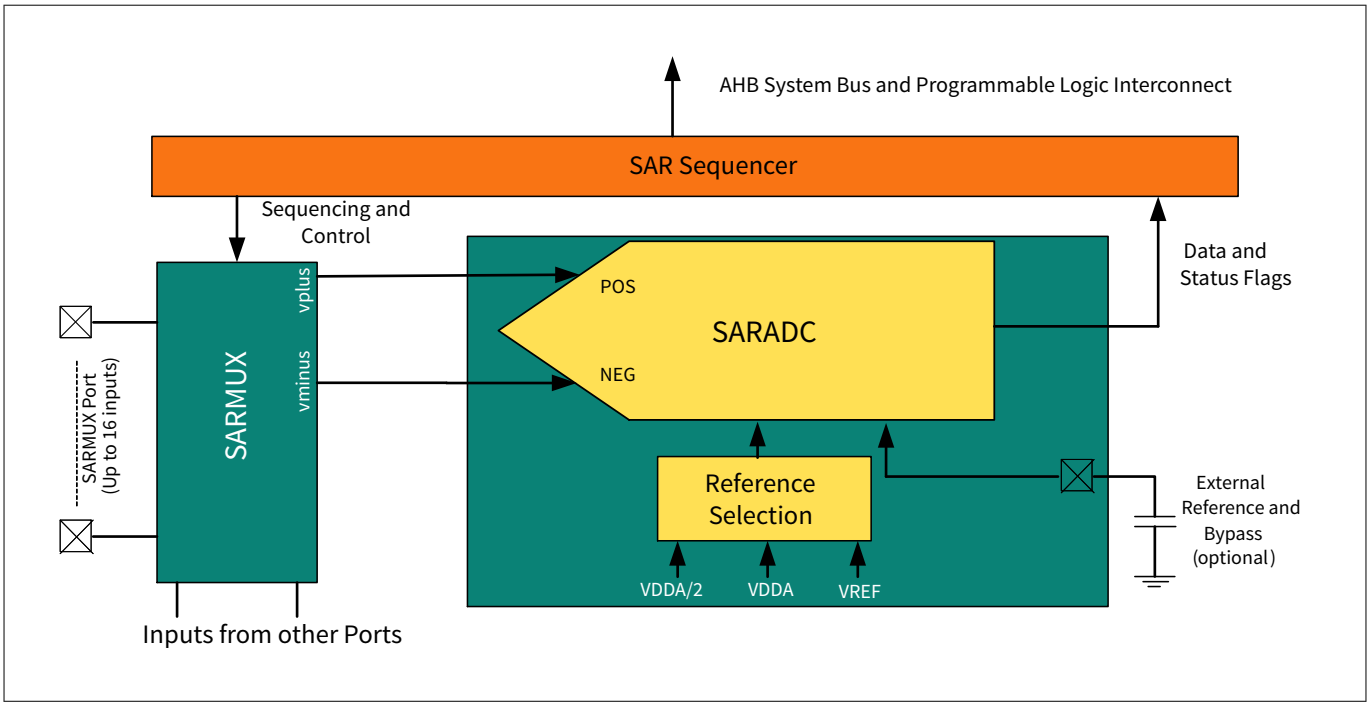


Figure 4 SAR ADC

4.3.2 Two opamps (Continuous-time block; CTB)

PSOC™ 4100S Max has two opamps with comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

4.3.3 Low-power comparators (LPC)

PSOC™ 4100S Max has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

4.3.4 Analog multiplexed buses

PSOC™ 4100S Max has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources to connect to any pin on the I/O Ports

4.4 Programmable digital blocks

4.4.1 Smart I/O block

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

4.5 Fixed function digital blocks

4.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a quadrature decoder. There are eight TCPWM blocks in PSOC™ 4100S Max

4.5.2 Serial Communication Block (SCB)

PSOC™ 4100S Max has five serial communication blocks, which can be programmed to have SPI, I^2C, UART, or LIN Slave functionality.

I^2C mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI^2C that creates a mailbox address range in the memory of PSOC™ 4100S Max and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I 2 C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

PSOC™ 4100S Max is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not over-voltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system

UART mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

LIN Slave mode: The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3, v2.1/2.2, ISO 17987-6, and SAE J2602-2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length.

4.6 CAN FD block

This device has one CAN FD block. The block includes time-stamp support and has a 4 KB message RAM. FD Data rates of up to 5 Mbps are supported. DMA transfers are supported.

4.7 I2S Master

This is an I2S TX master interface. The interface shall support transport of mono or stereo audio data, with sample sizes of 8,16, or 24 bits, up to at least CD Red Book audio quality rates.

In addition to the I2S protocol, the hardware shall be configurable to also support the left justified audio format.

As an I2S TX master, this interface requires three or four GPIO signals to interface to an external audio DAC:

- I2S_CLK – external I2S host clock (input)
- SCK – serial data clock (output) • SD – serial audio data (output)
- WS – serial word select (output)

When used with most audio DACs these GPIO are configured as LVTTL drivers/receivers

4.8 GPIO

PSOC™ 4100S Max has up to 84 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

4.9 Special function peripherals

4.9.1 CAPSENSE™

CAPSENSE™ is supported in PSOC™ 4100S Max via the MSC CAPSENSE™ block. There are two independent MSC blocks in the PSOC™ 4100S Max which can be used to scan sense inputs autonomously (without CPU sequencing and intervention) with support for DMA, or can operate via CPU firmware driven switch sequencing via the analog MUX Buses that any GPIO pin can be connected to. Therefore, the CAPSENSE™ function can be provided on a pin or group of pins in a system via autonomous scanning or via firmware control.

The PSOC™ 4100S Max MSC block provides the following improvements over previous generation capacitive sensing blocks:

- Improved SNR based on the all new ratio-metric analog architecture and advanced hardware filtering to enable modern sleek user interface solutions with superior liquid tolerance, and robust and reliable touch HMI solution for harsh environments
- Higher sensitivity to support smaller sensors, higher proximity detection range, and a much wider range of overlay thicknesses and materials
- Autonomous (that is, CPU independent) channel sequencing and scanning for low power optimization
- Improved shield drive method and support for wide range of shield electrode capacitance values for superior liquid tolerance
- Higher sensor capacitance range to support easier layout and wider variety of sensors
- Improved EMI performance
- The MSC block API is backwards compatible with the CSD block to preserve code compatibility

A driver is provided for the CAPSENSE™ block to make it very easy for the user to use. Shield drive for water tolerance is provided.

The CAPSENSE™ blocks provide both Self as well as Mutual capacitance sensing. Shield drive can be either Active (with an opamp) or passive (less power, for shield loads less than 20 pF).

It is possible to synchronize the two MSC blocks to provide true synchronized and synchronous sampling so that CSX operation can be extended to bigger displays and scan times are reduced. Synchronization can be extended to multiple chips for simultaneous sampling and increase the number of sensors.

4.9.2 LCD segment drive

PSOC™ 4100S Max has an LCD controller, which can drive between 2 and 8 commons, and between 62 and 56 segments respectively. The maximum number of combined commons and segments is 64. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

4.9.3 Cryptography accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

- The Crypto subsystem supports the following:
- Encryption/Decryption functions
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
- Hashing functions
  - Secure Hash Algorithm (SHA)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

5 Pinouts

Table 1 Pin list for PSOC™ 4100S Max

100-TQFP		64-TQFP		48-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
63	P0.0	39	P0.0	28	P0.0
64	P0.1	40	P0.1	29	P0.1
65	P0.2	41	P0.2	30	P0.2
66	P0.3	42	P0.3	31	P0.3
67	P0.4	43	P0.4	32	P0.4
68	P0.5	44	P0.5	33	P0.5
69	P0.6	45	P0.6	34	P0.6
70	P0.7	46	P0.7	35	P0.7
71	P8.0				
72	P8.1				
73	P8.2				
74	P8.3				
75	XRES	47	XRES	36	XRES
76	VCCD	48	VCCD	37	VCCD
77	VSSD	49	VSSD	38	VSSD
78	VDDD	50	VDDD	39	VDDD
79	P9.0				
80	P9.1				
81	P9.2				
82	P9.3				
83	P5.0	51	P5.0		
84	P5.1	52	P5.1		
85	P5.2	53	P5.2		
86	P5.3	54	P5.3		
87	P5.4				
88	P5.5	55	P5.5		
91	VDDA	56	VDDA	40	VDDA
92	VSSA	57	VSSA	41	VSSA
93	P1.0	58	P1.0	42	P1.0
94	P1.1	59	P1.1	43	P1.1
95	P1.2	60	P1.2	44	P1.2

(table continues...)

Table 1 (continued) Pin list for PSOC™ 4100S Max

100-TQFP		64-TQFP		48-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
96	P1.3	61	P1.3	45	P1.3
97	P1.4	62	P1.4	46	P1.4
98	P1.5	63	P1.5	47	P1.5
99	P1.6	64	P1.6	48	P1.6
100	P1.7	1	P1.7	1	P1.7
2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5
8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7
10	VSSD	10	VSSD		
11	VDDD	11	NC		
12	P10.0				
13	P10.1				
14	P10.2				
15	P10.3				
16	P10.4				
17	P10.5				
18	P6.0	12	P6.0		
19	P6.1	13	P6.1	10	P6.1
20	P6.2	14	P6.2	11	P6.2
21	P6.3				
22	P6.4	15	P6.4		
23	P12.0				
24	P12.1				
25	P6.5	16	P6.5		
26	VSSD	17	VSSD	12	VSSD
27	P3.0	18	P3.0	13	P3.0
28	P3.1	19	P3.1	14	P3.1

(table continues...)

Table 1 (continued) Pin list for PSOC™ 4100S Max

100-TQFP		64-TQFP		48-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
29	P3.2	20	P3.2	15	P3.2
30	P3.3	21	P3.3	16	P3.3
31	P3.4	22	P3.4	17	P3.4
32	P3.5	23	P3.5	18	P3.5
33	P3.6	24	P3.6	19	P3.6
34	P3.7	25	P3.7	20	P3.7
35	VDDD	26	VDDD		
36	P11.0				
37	P11.1				
38	P11.2				
39	P11.3				
40	P11.4				
41	P11.5				
42	VDDD			21	VDDD
43	P4.0	27	P4.0	22	P4.0
44	P4.1	28	P4.1	23	P4.1
45	P4.2	29	P4.2	24	P4.2
46	P4.3	30	P4.3	25	P4.3
47	P4.4	31	P4.4		
48	P4.5	32	P4.5		
49	P4.6	33	P4.6		
50	P4.7	34	P4.7		
51	VSSD				
52	NC				
53	P5.6	35	P5.6		
54	P5.7	36	P5.7		
55	P7.0	37	P7.0	26	P7.0
56	P7.1	38	P7.1	27	P7.1
57	P7.2				
58	P7.3				
59	P7.4				
60	P7.5				

(table continues...)

5 Pinouts

Table 1 (continued) Pin list for PSOC™ 4100S Max

100-TQFP		64-TQFP		48-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
61	P7.6				
62	P7.7				
89	NC				
90	NC				
1	NC				

***Note**: The NC pins are No Connect pins*

- *Descriptions of the power pins are as follows:*
- *VDDD: Power supply for the digital section*
- *VDDA: Power supply for the analog section*
- *VSSD, VSSA: Ground pins for the digital and analog sections respectively*
- *VCCD: Regulated digital supply (1.8 V ±5%)*

GPIOs by package:

Table 2 GPIOs by package

Number	100-TQFP	64-TQFP	48-QFN
GPIO	84	54	40

5 Pinouts

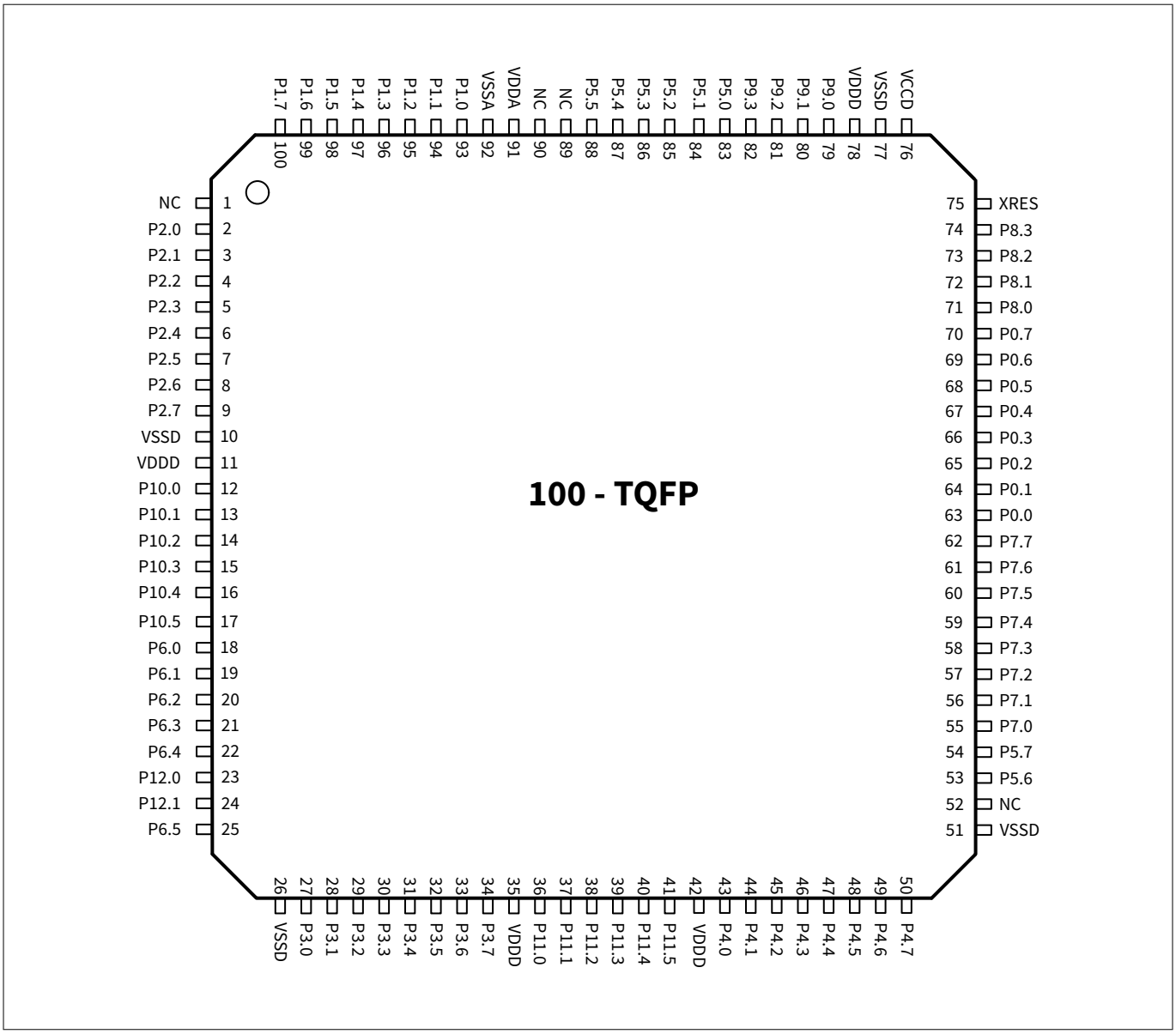


Figure 5 100-TQFP

5 Pinouts

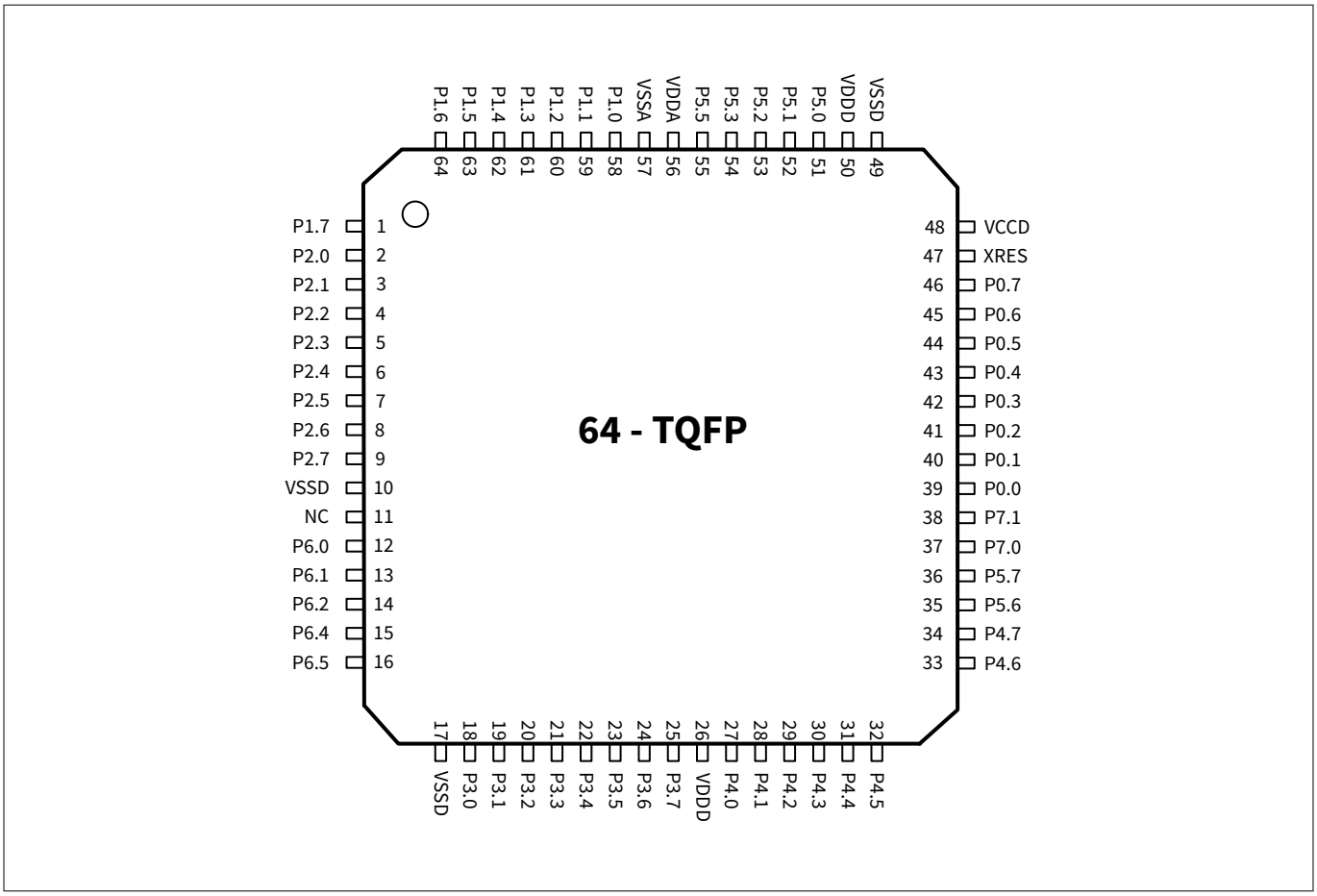


Figure 6 64-TQFP

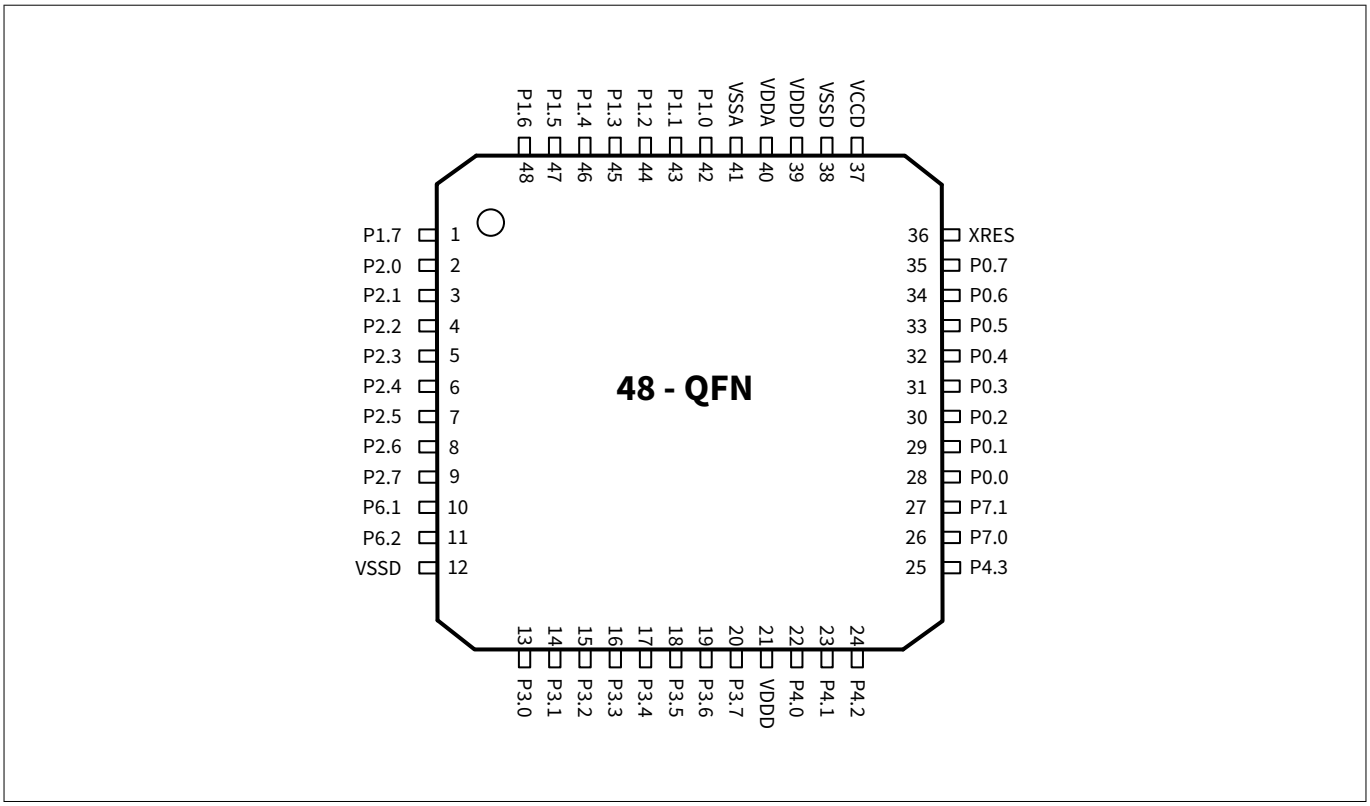


Figure 7 48-QFN

5.1 Alternate pin functions

Each port pin has multiple alternate functions. These are defined in Table 3. The columns ACT #x and DS #y denote Active and Deep Sleep mode signals respectively.

The notation for a signal is of the form “IPName[x].signal_name[u]:y”, where:

- IPName = Name of the block (such as tcpwm)
- x = Unique instance of the IP
- Signal_name = Name of the signal
- u = Signal number where there is more than one signal for a particular signal name
- y = Designates copies of the signal name

For example, the name “tcpwm[0].line_compl[3]:4” indicates that this is instance 0 of a TCPWM block, the signal is “line_compl # 3 (complement of the line output)”, and this is the fourth occurrence (copy) of the signal.

Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 3 Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P0.0	63	39	28		tcpwm.tr_in[0]	scb[2].uart_cts:0	lcd.com[0]	lcd.seg[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	64	40	29		tcpwm.tr_in[1]	scb[2].uart_rts:0	lcd.com[1]	lcd.seg[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	65	41	30			canfd.ttcan_rx[0]:1	lcd.com[2]	lcd.seg[2]	cpuss.swd_data:1	scb[0].spi_select3:0
P0.3	66	42	31			canfd.ttcan_tx[0]:1	lcd.com[3]:0	lcd.seg[3]	cpuss.swd_clk:1	scb[2].spi_select0:1
P0.4	67	43	32		scb[1].uart_rx:0	scb[2].uart_rx:0	lcd.com[4]	lcd.seg[4]	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	68	44	33		scb[1].uart_tx:0	scb[2].uart_tx:0	lcd.com[5]	lcd.seg[5]	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	69	45	34	srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1	lcd.com[6]	lcd.seg[6]		scb[1].spi_clk:1
P0.7	70	46	35	tcpwm.line[0]:3	scb[1].uart_rts:0		lcd.com[7]	lcd.seg[7]		scb[1].spi_select0:1
P8.0	71			tcpwm.line[4]:4	scb[4].uart_rx:2	audioss.clk_i2s_if:3	lcd.com[0]:1	lcd.seg[0]:1	scb[4].i2c_scl:1	scb[3].spi_mosi:2
P8.1	72			tcpwm.line_compl[4]:4	scb[4].uart_tx:2	audioss.tx_sck:3	lcd.com[1]:1	lcd.seg[1]:1	scb[4].i2c_sda:1	scb[3].spi_miso:2
P8.2	73			tcpwm.line[5]:4	scb[4].uart_cts:2	audioss.tx_ws:3	lcd.com[2]:1	lcd.seg[2]:1	lpcomp.comp[0]:3	scb[3].spi_clk:2
P8.3	74			tcpwm.line_compl[5]:4	scb[4].uart_rts:2	audioss.tx_sdo:3	lcd.com[3]:1	lcd.seg[3]:1	lpcomp.comp[1]:3	scb[3].spi_select0:2
P9.0	79			tcpwm.line[0]:4	scb[0].uart_rx:2	canfd.ttcan_rx[0]:2	lcd.com[8]:1	lcd.seg[8]:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P9.1	80			tcpwm.line_compl[0]:3	scb[0].uart_tx:2	canfd.ttcan_tx[0]:2	lcd.com[9]:1	lcd.seg[9]:1	scb[0].i2c_sda:2	scb[0].spi_miso:2
P9.2	81			tcpwm.line[1]:3	scb[0].uart_cts:2		lcd.com[10]:1	lcd.seg[10]:1		scb[0].spi_clk:2
P9.3	82			tcpwm.line_compl[1]:3	scb[0].uart_rts:2		lcd.com[11]:1	lcd.seg[11]:1		scb[0].spi_select0:2
P5.0	83	51		tcpwm.line[4]:2		scb[2].uart_rx:1	lcd.com[40]	lcd.seg[40]	scb[2].i2c_scl:1	scb[2].spi_mosi:0
P5.1	84	52		tcpwm.line_compl[4]:2		scb[2].uart_tx:2	lcd.com[41]	lcd.seg[41]	scb[2].i2c_sda:1	scb[2].spi_miso:0
P5.2	85	53		tcpwm.line[5]:2		scb[2].uart_cts:1	lcd.com[42]	lcd.seg[42]	lpcomp.comp[0]:2	scb[2].spi_clk:0
P5.3	86	54		tcpwm.line_compl[5]:2		scb[2].uart_rts:1	lcd.com[43]	lcd.seg[43]	lpcomp.comp[1]:0	scb[2].spi_select0:0
P5.4	87			tcpwm.[ine[6]:2			lcd.com[44]	[cd.seg[44]		scb[2].spi_se[ect1:0
P5.5	88	55		tcpwm.[ine_comp[[6]:2			lcd.com[45]	[cd.seg[45]		scb[2].spi_se[ect2:0
P1.0	93	58	42	tcpwm.[ine[2]:1	scb[0].uart_rx:1		lcd.com[8]	[cd.seg[8]	scb[0].i2c_sc[:0	scb[0].spi_mosi:1
P1.1	94	59	43	tcpwm.[ine_comp[[2]:1	scb[0].uart_tx:1		lcd.com[9]	[cd.seg[9]	scb[0].i2c_sda:0	scb[0].spi_miso:1

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P1.2	95	60	44	tcpwm.[ine[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	lcd.com[10]	[cd.seg[10]	scb[2].i2c_sc[:2	scb[0].spi_c[k:1
P1.3	96	61	45	tcpwm.[ine_comp[[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	lcd.com[11]	[cd.seg[11]	scb[2].i2c_sda:2	scb[0].spi_se[ect0:1
P1.4	97	62	46	tcpwm.[ine[6]:1			lcd.com[12]	[cd.seg[12]	scb[3].i2c_sc[:0	scb[0].spi_se[ect1:1
P1.5	98	63	47	tcpwm.[ine_comp[[6]:1			lcd.com[13]	[cd.seg[13]	scb[3].i2c_sda:0	scb[0].spi_se[ect2:1
P1.6	99	64	48	tcpwm.[ine[7]:1			lcd.com[14]	[cd.seg[14]		scb[0].spi_se[ect3:1
P1.7	100	1	1	tcpwm.[ine_comp[[7]:1			lcd.com[15]	[cd.seg[15]		scb[2].spi_c[k:1
P2.0	2	2	2	tcpwm.[ine[4]:0		tcpwm.tr_in[4]	lcd.com[16]	[cd.seg[16]	scb[1].i2c_sc[:1	scb[1].spi_mosi:2
P2.1	3	3	3	tcpwm.[ine_comp[[4]:0		tcpwm.tr_in[5]	lcd.com[17]	[cd.seg[17]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	4	4	4	tcpwm.[ine[5]:1			lcd.com[18]	[cd.seg[18]		scb[1].spi_c[k:2
P2.3	5	5	5	tcpwm.[ine_comp[[5]:1			lcd.com[19]	[cd.seg[19]		scb[1].spi_se[ect0:2
P2.4	6	6	6	tcpwm.[ine[0]:1	scb[3].uart_rx:1	audioss.tx_sck:1	lcd.com[20]	[cd.seg[20]		scb[1].spi_se[ect1:1

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P2.5	7	7	7	tcpwm.[ine_comp[[0]:1	scb[3].uart_tx:1	audioss.tx_ws:1	lcd.com[21]	[cd.seg[21]		scb[1].spi_se[ect2:1
P2.6	8	8	8	tcpwm.[ine[1]:1	scb[3].uart_cts:1	audioss.tx_sdo:1	lcd.com[22]	[cd.seg[22]		scb[1].spi_se[ect3:1
P2.7	9	9	9	tcpwm.[ine_comp[[1]:1	scb[3].uart_rts:1	audioss.c[k_i2s_if:1	lcd.com[23]	[cd.seg[23]	[pcomp.comp[0]:0	scb[2].spi_mosi:1
P10.0	12			tcpwm.[ine[7]:3		scb[2].uart_rx:2	lcd.com[16]:1	[cd.seg[16]:1	scb[2].i2c_sc[:3	scb[2].spi_mosi:2
P10.1	13			tcpwm.[ine_comp[[7]:3		scb[2].uart_tx:3	lcd.com[17]:1	[cd.seg[17]:1	scb[2].i2c_sda:3	scb[2].spi_miso:2
P10.2	14			tcpwm.[ine[2]:3		scb[2].uart_cts:2	lcd.com[18]:1	[cd.seg[18]:1		scb[2].spi_c[k:2
P10.3	15			tcpwm.[ine_comp[[2]:3		scb[2].uart_rts:2	lcd.com[19]:1	[cd.seg[19]:1		scb[2].spi_se[ect0:2
P10.4	16			tcpwm.[ine[3]:3		canfd.ttcan_rx[0]:3	lcd.com[20]:1	[cd.seg[20]:1		scb[2].spi_se[ect1:1
P10.5	17			tcpwm.[ine_comp[[3]:3		canfd.ttcan_tx[0]:3	lcd.com[21]:1	[cd.seg[21]:1		scb[2].spi_se[ect2:1
P6.0	18	12		tcpwm.[ine[4]:1	scb[3].uart_rx:0		lcd.com[48]	[cd.seg[48]	scb[3].i2c_sc[:1	scb[3].spi_mosi:0
P6.1	19	13	10	tcpwm.[ine_comp[[4]:1	scb[3].uart_tx:0	canfd.ttcan_rx[0]:0	lcd.com[49]	[cd.seg[49]	scb[3].i2c_sda:1	scb[3].spi_miso:0

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P6.2	20	14	11	tcpwm.[ine[5]:0	scb[3].uart_cts:0	canfd.ttcan_tx[0]:0	lcd.com[50]	[cd.seg[50]		scb[3].spi_c[k:0
P6.3	21			tcpwm.[ine_comp[[5]:0	scb[3].uart_rts:0		lcd.com[51]	[cd.seg[51]		scb[3].spi_se[ect0:0
P6.4	22	15		tcpwm.[ine[6]:0			lcd.com[52]	[cd.seg[52]	scb[4].i2c_sc[	scb[3].spi_se[ect1:0
P12.0	23			tcpwm.[ine[7]:2			lcd.com[62]:0	[cd.seg[62]:0	scb[1].i2c_sc[:3	scb[3].spi_se[ect3:0
P12.1	24			tcpwm.[ine_comp[[7]:2			lcd.com[63]:0	[cd.seg[63]:0	scb[1].i2c_sda:3	
P6.5	25	16		tcpwm.[ine_comp[[6]:0			lcd.com[53]	[cd.seg[53]	scb[4].i2c_sda	scb[3].spi_se[ect2:0
P3.0	27	18	13	tcpwm.[ine[0]:0	scb[1].uart_rx:1	audioss.c[k_i2s_if:0	lcd.com[24]	[cd.seg[24]	scb[1].i2c_sc[:2	scb[1].spi_mosi:0
P3.1	28	19	14	tcpwm.[ine_comp[[0]:0	scb[1].uart_tx:1		lcd.com[25]	[cd.seg[25]	scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2	29	20	15	tcpwm.[ine[1]:0	scb[1].uart_cts:1		lcd.com[26]	[cd.seg[26]	cpuss.swd_data:0	scb[1].spi_c[k:0
P3.3	30	21	16	tcpwm.[ine_comp[[1]:0	scb[1].uart_rts:1		lcd.com[27]	[cd.seg[27]	cpuss.swd_c[k:0	scb[1].spi_se[ect0:0
P3.4	31	22	17	tcpwm.[ine[2]:0		tcpwm.tr_in[6]	lcd.com[28]	[cd.seg[28]		scb[1].spi_se[ect1:0

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P3.5	32	23	18	tcpwm.[ine_comp[[2]:0		audioss.tx_sck:0	lcd.com[29]	[cd.seg[29]		scb[1].spi_se[ect2:0
P3.6	33	24	19	tcpwm.[ine[3]:0		audioss.tx_sdo:0	lcd.com[30]	[cd.seg[30]	scb[4].spi_se[ect3	scb[1].spi_se[ect3:0
P3.7	34	25	20	tcpwm.[ine_comp[[3]:0		audioss.tx_ws:0	lcd.com[31]	[cd.seg[31]	[pcomp.comp[1]:1	scb[2].spi_miso:1
P11.0	36			tcpwm.[ine[4]:3	scb[4].uart_rx:1		lcd.com[24]:1	[cd.seg[24]:1	scb[4].spi_mosi:1	scb[1].spi_mosi:3
P11.1	37			tcpwm.[ine_comp[[4]:3	scb[4].uart_tx:1		lcd.com[25]:1	[cd.seg[25]:1	scb[4].spi_miso:1	scb[1].spi_miso:3
P11.2	38			tcpwm.[ine[5]:3	scb[4].uart_cts:1		lcd.com[26]:1	[cd.seg[26]:1	scb[4].spi_c[k:1	scb[1].spi_c[k:3
P11.3	39			tcpwm.[ine_comp[[5]:3	scb[4].uart_rts:1		lcd.com[27]:1	[cd.seg[27]:1	scb[4].spi_se[ect0:1	scb[1].spi_se[ect0:3
P11.4	40			tcpwm.[ine[6]:3			lcd.com[28]:1	[cd.seg[28]:1	scb[4].spi_se[ect1:1	scb[1].spi_se[ect1:2
P11.5	41			tcpwm.[ine_comp[[6]:3			lcd.com[29]:1	[cd.seg[29]:1	scb[4].spi_se[ect2:1	scb[1].spi_se[ect2:2
P4.0	43	27	22		scb[0].uart_rx:0		lcd.com[32]	[cd.seg[32]	scb[0].i2c_sc[:1	scb[0].spi_mosi:0
P4.1	44	28	23		scb[0].uart_tx:0		lcd.com[33]	[cd.seg[33]	scb[0].i2c_sda:1	scb[0].spi_miso:0

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P4.2	45	29	24		scb[0].uart_cts:0		lcd.com[34]	[cd.seg[34]	[pcomp.comp[0]:1	scb[0].spi_c[k:0
P4.3	46	30	25		scb[0].uart_rts:0		lcd.com[35]	[cd.seg[35]	[pcomp.comp[1]:2	scb[0].spi_se[ect0:0
P4.4	47	31			scb[4].uart_rx		lcd.com[36]	[cd.seg[36]	scb[4].spi_mosi	scb[0].spi_se[ect1:2
P4.5	48	32			scb[4].uart_tx		lcd.com[37]	[cd.seg[37]	scb[4].spi_miso	scb[0].spi_se[ect2:2
P4.6	49	33		tcpwm.[ine[6]:4	scb[4].uart_cts		lcd.com[38]	[cd.seg[38]	scb[4].spi_c[k	scb[0].spi_se[ect3:2
P4.7	50	34		tcpwm.[ine_comp[[6]:4	scb[4].uart_rts		lcd.com[39]	[cd.seg[39]	scb[4].spi_se[ect0	scb[3].spi_se[ect2:1
P5.6	53	35		tcpwm.[ine[7]:0			lcd.com[46]	[cd.seg[46]	scb[4].spi_se[ect1	scb[2].spi_se[ect3:0
P5.7	54	36		tcpwm.[ine_comp[[7]:0			lcd.com[47]	[cd.seg[47]	scb[4].spi_se[ect2	scb[3].spi_se[ect1:1
P7.0	55	37	26	tcpwm.[ine[0]:2	scb[3].uart_rx:2		lcd.com[54]	[cd.seg[54]	scb[3].i2c_sc[:2	scb[3].spi_mosi:1
P7.1	56	38	27	tcpwm.[ine_comp[[0]:2	scb[3].uart_tx:2		lcd.com[55]	[cd.seg[55]	scb[3].i2c_sda:2	scb[3].spi_miso:1
P7.2	57			tcpwm.[ine[1]:2	scb[3].uart_cts:2		lcd.com[56]	[cd.seg[56]		scb[3].spi_c[k:1
P7.3	58			tcpwm.[ine_comp[[1]:2	scb[3].uart_rts:2	audioss.c[k_i2s_if:2	lcd.com[57]	[cd.seg[57]		scb[3].spi_se[ect2:2

(table continues...)

Table 3 (continued) Pin alternate function table for PSOC™ 4100S Max

Name	100-TQFP	64-TQFP	48-TQFP	ACT #0	ACT #1	ACT #2	DS #0	DS #1	DS #2	DS #3
P7.4	59			tcpwm.[ine[2]:2		audioss.tx_sck:2	lcd.com[58]	[cd.seg[58]		scb[3].spi_se[ect0:1
P7.5	60			tcpwm.[ine_comp[[2]:2		audioss.tx_sdo:2	lcd.com[59]:0	[cd.seg[59]:0		scb[3].spi_se[ect1:2
P7.6	61			tcpwm.[ine[3]:2		audioss.tx_ws:2	lcd.com[60]:0	[cd.seg[60]:0		scb[3].spi_se[ect3:1
P7.7	62			tcpwm.[ine_comp[[3]:2			lcd.com[61]:0	[cd.seg[61]:0		

Table 4 Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P0.0	63	39	28	lpcomp.in_p[0] msc[1].s[4]		msc[1].sense:14	msc[1].shield:14	amuxbus_a_msc1	amuxbus_b_msc1
P0.1	64	40	29	lpcomp.in_n[0] msc[1].s[5]		msc[1].sense:15	msc[1].shield:15	amuxbus_a_msc1	amuxbus_b_msc1
P0.2	65	41	30	lpcomp.in_p[1] msc[1].s[6]		msc[1].sense:16	msc[1].shield:16	amuxbus_a_msc1	amuxbus_b_msc1
P0.3	66	42	31	lpcomp.in_n[1] msc[1].s[7]		msc[1].sense:17	msc[1].shield:17	amuxbus_a_msc1	amuxbus_b_msc1
P0.4	67	43	32	wco.wco_in		msc[1].sense:18	msc[1].shield:18	amuxbus_a_msc1	amuxbus_b_msc1
P0.5	68	44	33	wco.wco_out		msc[1].sense:19	msc[1].shield:19	amuxbus_a_msc1	amuxbus_b_msc1
P0.6	69	45	34	exco.eco_in		msc[1].sense:20	msc[1].shield:20	amuxbus_a_msc1	amuxbus_b_msc1
P0.7	70	46	35	exco.eco_out		msc[1].sense:21	msc[1].shield:21	amuxbus_a_msc1	amuxbus_b_msc1
P8.0	71					msc[1].sense:22	msc[1].shield:22	amuxbus_a_msc1	amuxbus_b_msc1
P8.1	72					msc[1].sense:23	msc[1].shield:23	amuxbus_a_msc1	amuxbus_b_msc1
P8.2	73					msc[1].sense:24	msc[1].shield:24	amuxbus_a_msc1	amuxbus_b_msc1

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P8.3	74					msc[1].sense:25	msc[1].shield:25	amuxbus_a_msc1	amuxbus_b_msc1
P9.0	79			msc[1].s[8]		msc[1].sense:26	msc[1].shield:26	amuxbus_a_msc1	amuxbus_b_msc1
P9.1	80			msc[1].s[9]		msc[1].sense:27	msc[1].shield:27	amuxbus_a_msc1	amuxbus_b_msc1
P9.2	81			msc[1].s[10]		msc[1].sense:28	msc[1].shield:28	amuxbus_a_msc1	amuxbus_b_msc1
P9.3	82			msc[1].s[11]		msc[1].sense:29	msc[1].shield:29	amuxbus_a_msc1	amuxbus_b_msc1
P5.0	83	51		msc[1].s[12]		msc[1].sense:30	msc[1].shield:30	amuxbus_a_msc1	amuxbus_b_msc1
P5.1	84	52		msc[1].cmod1pads[2), 3)]		msc[1].sense:31	msc[1].shield:31	amuxbus_a_msc1	amuxbus_b_msc1
P5.2	85	53		msc[1].cmod2pads[2), 3)]		msc[1].sense:3	msc[1].shield:3	amuxbus_a_msc1	amuxbus_b_msc1
P5.3	86	54		msc[1].s[13]		msc[]1].sense:2	msc[1].shield:2	amuxbus_a_msc1	amuxbus_b_msc1
P5.4	87			msc[1].s[14]		msc[1].sense:1	msc[1].shield:1	amuxbus_a_msc1	amuxbus_b_msc1
P5.5	88	55		msc[1].s[15]		msc[1].sense:0	msc[1].shield:0	amuxbus_a_msc1	amuxbus_b_msc1
P1.0	93	58	42	ctb0_oa0+	smartio[2].io[0]	msc[0].sense:0	msc[0].shield:0	amuxbus_a_pass	amuxbus_b_pass
P1.1	94	59	43	ctb0_oa0-	smartio[2].io[1]	msc[0].sense:1	msc[0].shield:1	amuxbus_a_pass	amuxbus_b_pass

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P1.2	95	60	44	ctb0_oa0_out	smartio[2].io[2]	msc[0].sense:2	msc[0].shield:2	amuxbus_a_pass	amuxbus_b_pass
P1.3	96	61	45	ctb0_oa1_out	smartio[2].io[3]	msc[0].sense:3	msc[0].shield:3	amuxbus_a_pass	amuxbus_b_pass
P1.4	97	62	46	ctb0_oa1-	smartio[2].io[4]	msc[0].sense:4	msc[0].shield:4	amuxbus_a_pass	amuxbus_b_pass
P1.5	98	63	47	ctb0_oa1+	smartio[2].io[5]	msc[0].sense:5	msc[0].shield:5	amuxbus_a_pass	amuxbus_b_pass
P1.6	99	64	48	ctb0_oa0+	smartio[2].io[6]	msc[0].sense:6	msc[0].shield:6	amuxbus_a_pass	amuxbus_b_pass
P1.7	100	1	1	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1	smartio[2].io[7]	msc[0].sense:7	msc[0].shie[d:7	amuxbus_a_pass	amuxbus_b_pass
P2.0	2	2	2	sarmuxs[0]	smartio[0].io[0]	msc[0].sense:8	msc[0].shie[d:8	amuxbus_a_pass	amuxbus_b_pass
P2.1	3	3	3	sarmuxs[1]	smartio[0].io[1]	msc[0].sense:9	msc[0].shie[d:9	amuxbus_a_pass	amuxbus_b_pass
P2.2	4	4	4	sarmuxs[2]	smartio[0].io[2]	msc[0].sense:10	msc[0].shie[d:10	amuxbus_a_pass	amuxbus_b_pass
P2.3	5	5	5	sarmuxs[3]	smartio[0].io[3]	msc[0].sense:11	msc[0].shie[d:11	amuxbus_a_pass	amuxbus_b_pass
P2.4	6	6	6	sarmuxs[4]	smartio[0].io[4]	msc[0].sense:12	msc[0].shie[d:12	amuxbus_a_pass	amuxbus_b_pass

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P2.5	7	7	7	sarmuxs[5]	smartio[0].io[5]	msc[0].sense:13	msc[0].shied:13	amuxbus_a_pass	amuxbus_b_pass
P2.6	8	8	8	sarmuxs[6]	smartio[0].io[6]	msc[0].sense:14	msc[0].shied:14	amuxbus_a_pass	amuxbus_b_pass
P2.7	9	9	9	sarmuxs[7]	smartio[0].io[7]	msc[0].sense:15	msc[0].shied:15	amuxbus_a_pass	amuxbus_b_pass
P10.0	12					msc[0].sense:16	msc[0].shied:16	amuxbus_a_msc0	amuxbus_b_msc0
P10.1	13					msc[0].sense:17	msc[0].shied:17	amuxbus_a_msc0	amuxbus_b_msc0
P10.2	14					msc[0].sense:18	msc[0].shied:18	amuxbus_a_msc0	amuxbus_b_msc0
P10.3	15					msc[0].sense:19	msc[0].shied:19	amuxbus_a_msc0	amuxbus_b_msc0
P10.4	16					msc[0].sense:20	msc[0].shied:20	amuxbus_a_msc0	amuxbus_b_msc0
P10.5	17					msc[0].sense:21	msc[0].shied:21	amuxbus_a_msc0	amuxbus_b_msc0
P6.0	18	12				msc[0].sense:22	msc[0].shied:22	amuxbus_a_msc0	amuxbus_b_msc0
P6.1	19	13	10			msc[0].sense:23	msc[0].shied:23	amuxbus_a_msc0	amuxbus_b_msc0
P6.2	20	14	11			msc[0].sense:24	msc[0].shied:24	amuxbus_a_msc0	amuxbus_b_msc0
P6.3	21					msc[0].sense:25	msc[0].shied:25	amuxbus_a_msc0	amuxbus_b_msc0

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P6.4	22	15				msc[0].sense:26	msc[0].shie[d:26	amuxbus_a_msc0	amuxbus_b_msc0
P12.0	23					msc[0].sense:27	msc[0].shie[d:27	amuxbus_a_msc0	amuxbus_b_msc0
P12.1	24					msc[0].sense:28	msc[0].shie[d:28	amuxbus_a_msc0	amuxbus_b_msc0
P6.5	25	16		msc[0].s[0]		msc[0].sense:29	msc[0].shie[d:29	amuxbus_a_msc0	amuxbus_b_msc0
P3.0	27	18	13	msc[0].s[1]	smartio[1].io[0]	msc[0].sense:30	msc[0].shie[d:30	amuxbus_a_msc0	amuxbus_b_msc0
P3.1	28	19	14	msc[0].s[2]	smartio[1].io[1]	msc[0].sense:31	msc[0].shie[d:31	amuxbus_a_msc0	amuxbus_b_msc0
P3.2	29	20	15		smartio[1].io[2]	msc[0].sense:32	msc[0].shie[d:32	amuxbus_a_msc0	amuxbus_b_msc0
P3.3	30	21	16		smartio[1].io[3]	msc[0].sense:33	msc[0].shie[d:33	amuxbus_a_msc0	amuxbus_b_msc0
P3.4	31	22	17	msc[0].s[3]	smartio[1].io[4]	msc[0].sense:34	msc[0].shie[d:34	amuxbus_a_msc0	amuxbus_b_msc0
P3.5	32	23	18	msc[0].s[4]	smartio[1].io[5]	msc[0].sense:35	msc[0].shie[d:35	amuxbus_a_msc0	amuxbus_b_msc0
P3.6	33	24	19	msc[0].s[5]	smartio[1].io[6]	msc[0].sense:36	msc[0].shie[d:36	amuxbus_a_msc0	amuxbus_b_msc0
P3.7	34	25	20	msc[0].s[6]	smartio[1].io[7]	msc[0].sense:37	msc[0].shie[d:37	amuxbus_a_msc0	amuxbus_b_msc0
P11.0	36			msc[0].s[7]		msc[0].sense:38	msc[0].shie[d:38	amuxbus_a_msc0	amuxbus_b_msc0

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P11.1	37			msc[0].s[8]		msc[0].sense:39	msc[0].shie[d:39	amuxbus_a_msc0	amuxbus_b_msc0
P11.2	38			msc[0].s[9]		msc[0].sense:40	msc[0].shie[d:40	amuxbus_a_msc0	amuxbus_b_msc0
P11.3	39			msc[0].s[10]		msc[0].sense:41	msc[0].shield:41	amuxbus_a_msc0	amuxbus_b_msc0
P11.4	40			msc[0].s[11]		msc[0].sense:42	msc[0].shield:42	amuxbus_a_msc0	amuxbus_b_msc0
P11.5	41					msc[0].sense:43	msc[0].shield:43	amuxbus_a_msc0	amuxbus_b_msc0
P4.0	43	27	22	msc[0].cmod3pads[2), 3)]		msc[0].sense:44	msc[0].shield:44	amuxbus_a_msc0	amuxbus_b_msc0
P4.1	44	28	23	msc[0].cmod4pads[2), 3)]		msc[0].sense:45	msc[0].shield:45	amuxbus_a_msc0	amuxbus_b_msc0
P4.2	45	29	24	msc[0].cmod1pads[2), 3)]		msc[0].sense:46	msc[0].shield:46	amuxbus_a_msc0	amuxbus_b_msc0
P4.3	46	30	25	msc[0].cmod2pads[2), 3)]		msc[0].sense:47	msc[0].shield:47	amuxbus_a_msc0	amuxbus_b_msc0
P4.4	47	31		msc[0].s[12]		msc[0].sense:48	msc[0].shield:48	amuxbus_a_msc0	amuxbus_b_msc0
P4.5	48	32		msc[0].s[13]		msc[0].sense:49	msc[0].shield:49	amuxbus_a_msc0	amuxbus_b_msc0
P4.6	49	33		msc[0].s[14]		msc[0].sense:50	msc[0].shield:50	amuxbus_a_msc0	amuxbus_b_msc0
P4.7	50	34		msc[0].s[15]		msc[0].sense:51	msc[0].shield:51	amuxbus_a_msc0	amuxbus_b_msc0

(table continues...)

Table 4 (continued) Analog and special functions

Name	100-TQFP	64-TQFP	48-TQFP	Analog[1)]	SMARTIO	MSC_SENSE	MSC_SHIELD	AMUXA	AMUXB
P5.6	53	35		msc[1].s[0]		msc[1].sense:4	msc[1].shield:4	amuxbus_a_msc1	amuxbus_b_msc1
P5.7	54	36		msc[1].s[1]		msc[1].sense:5	msc[1].shield:5	amuxbus_a_msc1	amuxbus_b_msc1
P7.0	55	37	26	msc[1].cmod3pads[2)], [3)]		msc[1].sense:6	msc[1].shield:6	amuxbus_a_msc1	amuxbus_b_msc1
P7.1	56	38	27	msc[1].cmod4pads[2)], [3)]		msc[1].sense:7	msc[1].shield:7	amuxbus_a_msc1	amuxbus_b_msc1
P7.2	57					msc[1].sense:8	msc[1].shield:8	amuxbus_a_msc1	amuxbus_b_msc1
P7.3	58					msc[1].sense:9	msc[1].shield:9	amuxbus_a_msc1	amuxbus_b_msc1
P7.4	59					msc[1].sense:10	msc[1].shield:10	amuxbus_a_msc1	amuxbus_b_msc1
P7.5	60					msc[1].sense:11	msc[1].shield:11	amuxbus_a_msc1	amuxbus_b_msc1
P7.6	61			msc[1].s[2]		msc[1].sense:12	msc[1].shield:12	amuxbus_a_msc1	amuxbus_b_msc1
P7.7	62			msc[1].s[3]		msc[1].sense:13	msc[1].shield:13	amuxbus_a_msc1	amuxbus_b_msc1

1) The CAPSENSE™ block is termed as MSC, All msc[].s pins are CTRL MUX (control mux) pins.
2) CMOD pins cannot be re-purposed as mutual cap RX sensors - see errata item 2 in Errata.
3) The CTRL mux mode is not supported for CMOD pins re-purposed as sensor pad connections.

5.2 Function name description

Table 5 Function name description

Function name	Description	I/O
amuxbus_a_msc0	AMUXBUS A connection to MSC0 (Analog mux bus routing for MSC0)	I/O
amuxbus_a_msc1	AMUXBUS A connection to MSC1 (Analog mux bus routing for MSC1)	I/O
amuxbus_a_pass	AMUXBUS A connection to PASS (Programmable Analog Subsystem/analog routing)	I/O
amuxbus_b_msc0	AMUXBUS B connection to MSC0 (Analog mux bus routing for MSC0)	I/O
amuxbus_b_msc1	AMUXBUS B connection to MSC1 (Analog mux bus routing for MSC1)	I/O
amuxbus_b_pass	AMUXBUS B connection to PASS (Programmable Analog Subsystem/analog routing)	I/O
audioss.clk_i2s_if	I2S - External clock from host	I
audioss.tx_sck	I2S - Serial Clock	O
audioss.tx_sdo	I2S - Serial Data	O
audioss.tx_ws	I2S - Word Select	O
canfd.ttcan_rx[X]	CAN FD Receive[X]	I
canfd.ttcan_tx[X]	CAN FD Transmit[X]	O
cpuss.swd_clk	SWD_CLK (Programming/Debug)	I/O
cpuss.swd_data	SWD_Data (Programming/Debug)	I/O
ctb0_oa0+	Continuous Time Block (OPAMP [0]) positive Input terminal	I
ctb0_oa0-	Continuous Time Block (OPAMP [0]) negative Input terminal	I
ctb0_oa0_out	Continuous Time Block (OPAMP [0]) output terminal	O
ctb0_oa1+	Continuous Time Block (OPAMP [1]) positive Input terminal	I
ctb0_oa1	Continuous Time Block (OPAMP [1]) negative Input terminal	I
ctb0_oa1_out	Continuous Time Block (OPAMP [1]) output terminal	O
EXCO.eco_in	External Crystal Oscillator Input	I
EXCO.eco_out	External Crystal Oscillator output	O
lcd.com[X]	LDC Drive Common pad [X]	O
lcd.seg[X]	LDC Drive Segment pad [X]	O
lpcomp.comp[X]	Low Power Comparator Output for Block [X]	O
lpcomp.in_n[x]	Low Power Comparator Input - Negative of Block [X]	I
lpcomp.in_p[x]	Low Power Comparator Input - Positive of Block [X]	I
msc[X].cmod1pads[1)]	5th Gen CAPSENSE™ (MSC) block [X] CMOD1 pin	I/O

(table continues...)

Table 5 (continued) Function name description

Function name	Description	I/O
msc[X].cmod2pads[1)]	5th Gen CAPSENSE™ (MSC) block [X] CMOD2 pin	I/O
msc[X].cmod3pads[1)]	5th Gen CAPSENSE™ (MSC) block [X] CMOD3 pin	I/O
msc[X].cmod4pads[1)]	5th Gen CAPSENSE™ (MSC) block [X] CMOD4 pin	I/O
msc[X].s[Y]	5th Gen CAPSENSE™ (MSC) block [X] control mux supported pin [Y]	I/O
msc[X].sense[2)]	5th Gen CAPSENSE™ (MSC) block [X] sensing supported pin	I/O
msc[X].shield[2)]	5th Gen CAPSENSE™ (MSC) block [X] shield supported pin	O
sar_ext_verf0	SAR ADC external Vref voltage[0]	I
sar_ext_vref1	SAR ADC external Vref voltage[1]	I
sarmuxs[X]	SAR ADC MUX pads [X]	I
SCB[x].i2c_scl	Serial Communication Block [X] - I2C SCL	I/O
SCB[x].i2c_sda	Serial Communication Block [X] - I2C SDA	I/O
SCB[x].spi_clk	Serial Communication Block [X] - SPI Clock	I/O
SCB[x].spi_miso	Serial Communication Block [X] - SPI MISO	I/O
SCB[x].spi_mosi	Serial Communication Block [X] - SPI MOSI	I/O
scb[x].spi_select	Serial Communication Block - SPI select	O
SCB[x].uart_cts	Serial Communication Block [X] - UART Clear To Send	I
SCB[x].uart_rts	Serial Communication Block [X] - UART Ready To Send	O
SCB[x].uart_rx	Serial Communication Block [X] - UART Receive	I
SCB[x].uart_tx	Serial Communication Block [X] - UART Transmit	O
smartio[x].io[y]	Smart IO Block [X] - IO Pin [Y]	I/O
srss.ext_clk	External clock input	I
tcpwm.line[X]	Timer Counter PWM (TCPWM) Block [X] - Output	O
tcpwm.line_compl[X]	Timer Counter PWM (TCPWM) Block [X] - Output Complement	O
tcpwm.tr_in[y]	Timer Counter PWM (TCPWM) Block trigger input [Y] - for Reload/ Start/Stop/Count/Capture	I
WCO.wco_in	Watch Crystal Oscillator Input	I
WCO.wco_out	Watch Crystal Oscillator Output	O

1) A pair of CMOD capacitors is required for the operation of each respective CAPSENSE™ block (MSC[X])—either CMOD1 and CMOD2 or CMOD3 and CMOD4.

2) Any GPIO pin can be connected to the designated MSC[X] CAPSENSE™ block for sensing or shield operations via the AMUX. However, it is essential that the CMOD capacitors pair for the corresponding MSC[X] block are connected.

6 Power

The following power system diagram shows the set of power supply pins as implemented for the PSOC™ 4100S Max. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

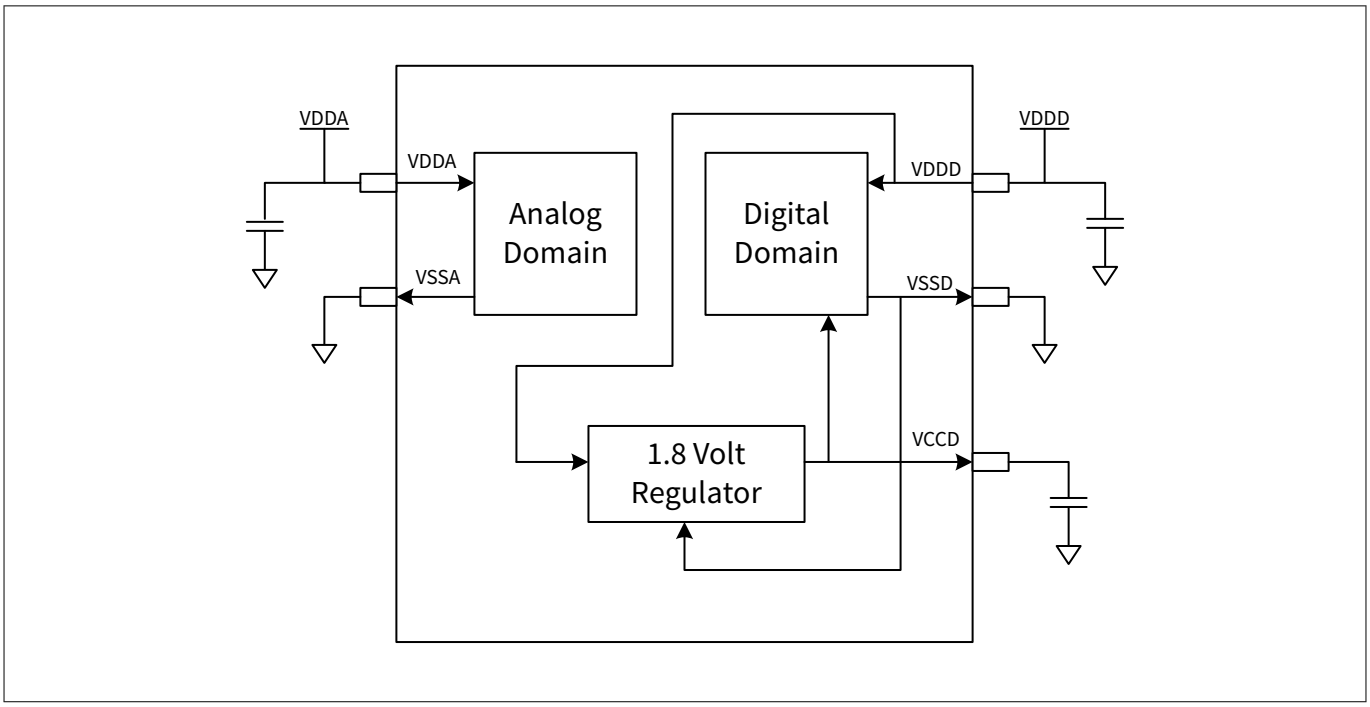


Figure 8 Power supply connections

There are two distinct modes of operation. In Mode 1, the supply voltage range is 2.0 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

6.1 Mode 1: 2.0 V to 5.5 V external supply

In this mode, PSOC™ 4100S Max is powered by an external power supply that can be anywhere in the range of 2.0 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 2.0 V. In this mode, the internal regulator of PSOC™ 4100S Max supplies the internal logic and its output is connected to the VCCD pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

6.2 Mode 2: 1.8 V ±5% external supply

In this mode, PSOC™ 4100S Max is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

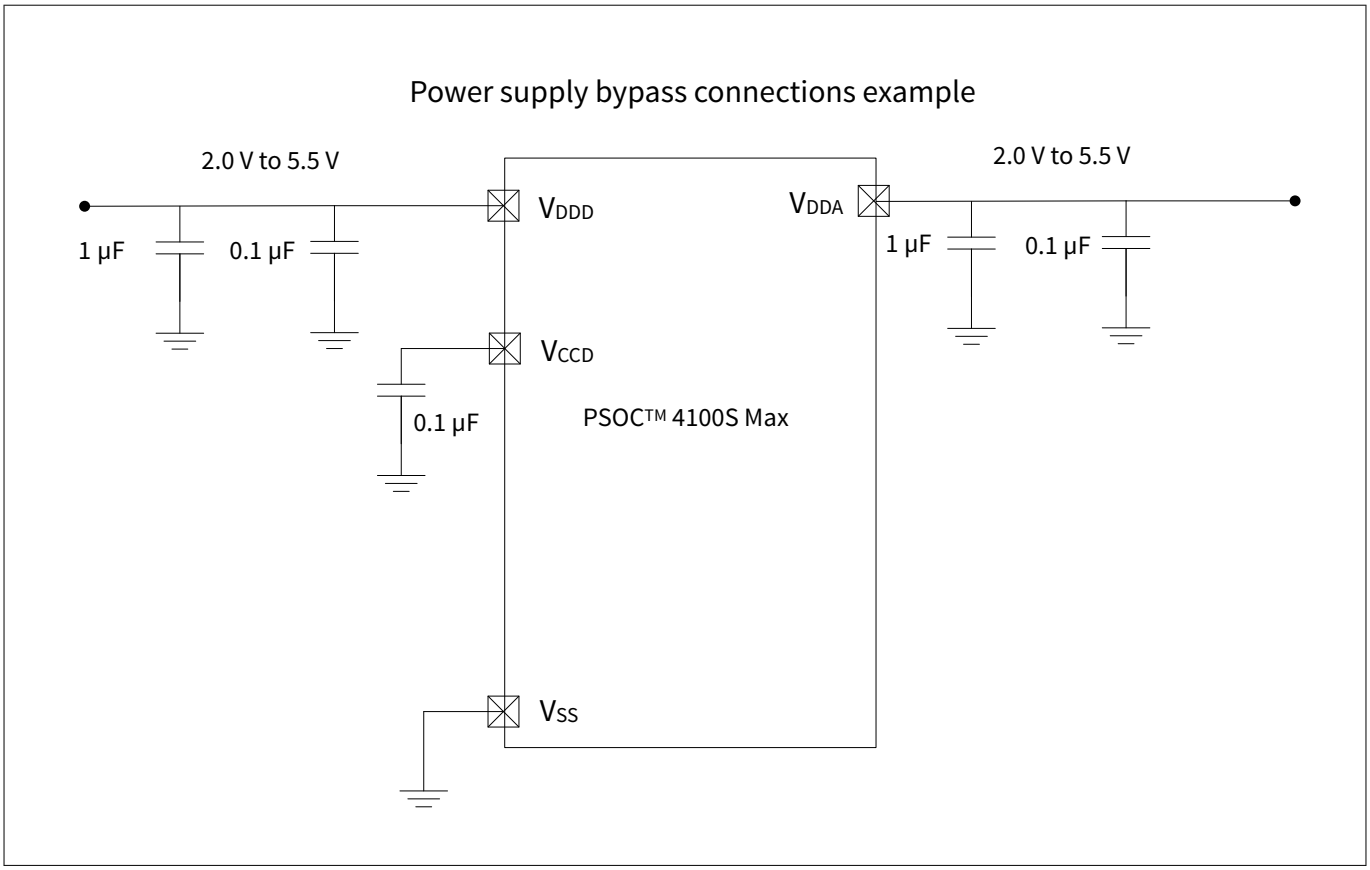


Figure 9 External supply range from 2.0 V to 5.5 V with internal regulator active

7 Electrical specifications

7.1 Absolute maximum ratings

Table 6 Absolute maximum ratings[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID1	VDDD_ABS	Digital supply relative to VSS	–0.5	–	6	V	–
SID2	VCCD_ABS	Direct digital core voltage input relative to VSS	–0.5	–	1.95		–
SID3	VGPIO_ABS	GPIO voltage	–0.5	–	VDD + 0.5		–
SID4	IGPIO_ABS	Maximum current per GPIO	–25	–	25	mA	–
SID5	IGPIO_injection	GPIO injection current, Max for VIH > VDDD, and Min for VIL < VSS	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2000	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

1) Usage above the absolute maximum conditions listed in Table 6 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

7.2 Device-level specifications

All specifications are valid for –40°C ≤ TA ≤ 85°C for Grade-A devices, –40°C ≤ TA ≤ 105°C for Grade-S devices, and –40°C <= TA <= 125°C for Grade-E devices[1)]. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 7 DC specifications Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID53	VDD	Power supply input voltage	2.0	–	5.5	V	Internally regulated supply
SID255	VDD	Power supply input voltage (VCCD = V_{DDD} = VDDA)	1.71	–	1.89	V	Internally unregulated supply
SID54	VCCD	Output voltage (for core logic)	–	1.8	–	V	–
SID55	CEFC	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	CEXC	Power supply bypass capacitor	–	1	–	µF	
Active mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25°C.							
SID10	IDD5	Execute from flash; CPU at 6 MHz	–	2.1	3.5	mA	Max is at 5.5 V and 125°C
SID16	IDD8	Execute from flash; CPU at 24 MHz	–	5.8	7.5	mA	
SID19	IDD11	Execute from flash; CPU at 48 MHz	–	11.2	12.5	mA	
Sleep mode, V_{DDD} = 2.0 V to 5.5 V (Regulator on)							

(table continues...)

1 Grade-E specifications (at +125°C) are preliminary. Contact Infineon Support for the availability of Grade-E devices.

Table 7 (continued) DC specifications Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID22	IDD17	I²C wakeup WDT, and comparators on	–	1.3	2.9	mA	6 MHz, Max is at 5.5 V and 125°C
SID25	IDD20	I²C wakeup, WDT, and comparators on	–	1.85	3.7	mA	12 MHz, Max is at 5.5 V and 125°C
Sleep mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I²C wakeup, WDT, and comparators on	–	1.2	2.9	mA	6 MHz, Max is at 5.5 V and 125°C
SID28A	IDD23A	I²C wakeup, WDT, and comparators on	–	1.5	3.7	mA	12 MHz, Max is at 5.5 V and 125°C
Deep Sleep mode, V_{DD} = 2.0 V to 3.6 V (Regulator on)							
SID30	IDD25	I²C wakeup and WDT on; T = –40°C to 60°C	–	3.7	60	µA	T = –40°C to 60°C
SID31	IDD26	I²C wakeup and WDT on	–	3.7	500	µA	Max is at 3.6 V and 125°C
Deep Sleep mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID33	IDD28	I²C wakeup and WDT on; T = –40°C to 60°C	–	3.7	60	µA	T = –40°C to 60°C
SID34	IDD29	I²C wakeup and WDT on	–	3.7	500	µA	Max is at 5.5 V and 125°C
Deep Sleep mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID36	IDD31	I²C wakeup and WDT on; T = –40°C to 60°C	–	2.5	70	µA	T = –40°C to 60°C
SID37	IDD32	I²C wakeup and WDT on	–	3.2	550	µA	Max is at 1.8 V and 125°C
XRES current							

(table continues...)

Table 7 (continued) DC specifications Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID307	IDD_XR	Supply current while XRES asserted	–	2	5	mA	–

7.2.1 GPIO

Table 8 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID48	FCPU	CPU frequency	DC	–	48	MHz	1.71 ≤ V_{DD} ≤ 5.5
SID49[1)]	TSLEEP	Wakeup from Sleep mode	–	0	–	µs	–
SID50[1)]	TDEEPSLEEP	Wakeup from Deep Sleep mode	–	35	–		–

1) Guaranteed by characterization.

Table 9 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID57	V_{IH}[1)]	Input voltage high threshold	0.7 X V_{DDD}	–	–	V	CMOS Input
SID58	VIL	Input voltage low threshold	–	–	0.3 X VDDD		CMOS Input
SID241	V_{IH}[1)]	LVTTL input, V_{DDD} < 2.7 V	0.7 X V_{DDD}	–	–		–
SID242	VIL	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 X VDDD		–
SID243	V_{IH}[1)]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	VIL	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	VOH	Output voltage high level	V_{DDD} – 0.6	–	–		I_{OH} = 4 mA at 3 V VDDD

(table continues...)

Table 9 (continued) GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID60	VOH	Output voltage high level	V_{DDD} – 0.5	–	–		I_{OH} = 1 mA at 1.8 V VDDD
SID61	VOL	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V VDDD
SID62	VOL	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V VDDD
SID62A	VOL	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V VDDD
SID63	RPULLUP	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	RPULLDOWN	Pull-down resistor	3.5	5.6	8.5		–
SID65	IIL	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID65A	IIL_CTBM	Input leakage on CTBM input pins	–	–	4		–
SID66	CIN	Input capacitance	–	–	7	pF	–
SID67[1)]	VHYSTTL	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68[1)]	VHYSCMOS	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		VDD < 4.5 V
SID68A[1)]	VHYSCMOS5V5	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[1)]	IDIODE	Current through protection diode to VDD/VSS	–	–	100	µA	–

(table continues...)

Table 9 (continued) GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID69A[1)]	ITOT_GPIO	Maximum total source or sink chip current	–	–	200	mA	–

1) V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 10 GPIO AC specifications (Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID70	TRISEF	Rise time in fast strong mode	2	–	12	ns	3.3 V VDDD, Cload = 25 pF
SID71	TFALLF	Fall time in fast strong mode	2	–	12		3.3 V VDDD, Cload = 25 pF
SID72	TRISES	Rise time in slow strong mode	10	–	60	–	3.3 V VDDD, Cload = 25 pF
SID73	TFALLS	Fall time in slow strong mode	10	–	60	–	3.3 V VDDD, Cload = 25 pF
SID74	FGPIOUT1	GPIO $_{FOUT}$; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	FGPIOUT2	GPIO FOUT; 1.71 V ≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	FGPIOUT3	GPIO $_{FOUT}$; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle

(table continues...)

Table 10 (continued) GPIO AC specifications (Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID245	FGPIOUT4	GPIO FOUT; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	FGPIOIN	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48		90/10% VIO

7.2.2 XRES

Table 11 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID77	VIH	Input voltage high threshold	0.7 × VDDD	–	–	V	CMOS Input
SID78	VIL	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID79	RPULLUP	Pull-up resistor	–	60	–	kΩ	–
SID80	CIN	Input capacitance	–	–	7	pF	–
SID81[1)]	VHYSXRES	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V
SID82	IDIODE	Current through protection diode to VDD/VSS	–	–	100	µA	–

1) Guaranteed by characterization.

Table 12 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID83[1)]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[1)]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

7.3 Analog peripherals

7.3.1 CTBm opamp

Table 13 CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
	IDD	Op Amp Block current. External load					
SID269	IDD_HI	power = hi	-	1100	1900	µA	-
SID270	IDD_MED	power = med	-	550	1020		-
SID271	IDD_LOW	power = lo	-	150	370		-
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V					
SID272	GBW_HI	power = hi	6	-	-	MHz	Input and output are 0.2 V to $_{VDDA-0.2}$ V
SID273	GBW_MED	power = med	3	-	-		Input and output are 0.2 V to $_{VDDA-0.2}$ V
SID274	GBW_LO	power = lo	-	1	-		Input and output are 0.2 V to $_{VDDA-0.2}$ V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
	IOUT_MAX	VDDA = > 2.7 V, 500 mV from rail					
SID275	IOUT_MAX_HI	IOUT_MAX_HI	10	-	-	mA	Output is 0.5 $V_{VDDA-0.5}$ V
SID276	IOUT_MAX_MID	power = mid	10	-	-		Output is 0.5 $V_{VDDA-0.5}$ V
SID277	IOUT_MAX_LO	power = lo	-	5	-		Output is 0.5 $V_{VDDA-0.5}$ V
	IOUT	VDDA = 1.71 V, 500 mV from rail					
SID278	IOUT_MAX_HI	power = hi	4	-	-	mA	Output is 0.5 $V_{VDDA-0.5}$ V
SID279	IOUT_MAX_MID	power = mid	4	-	-	mA	Output is 0.5 $V_{VDDA-0.5}$ V
SID280	IOUT_MAX_LO	power = lo	-	2	-	mA	Output is 0.5 $V_{VDDA-0.5}$ V
	IDD_Int	Op Amp Block current. Internal Load.					
SID269_I	IDD_HI_Int	power = hi	-	1500	1700	µA	-
SID270_I	IDD_MED_Int	power = med	-	700	980		-
SID271_I	IDD_LOW_Int	power = lo	-	-	405		-
	GBW	VDDA = 2.7 V	-	-	-		-
SID272_I	GBW_HI_Int	power = hi	8	-	-	MHz	Output is 0.25 V to VDDA-0.25 V
	SID273_IGBW_MED_Int	power = med	4				Output is 0.25V to VDDA-0.25 V
SID274_I	GBW_LO_Int	power = lo	1				Output is 0.25 V to VDDA-0.25 V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
		General opamp Specs for both Internal and External Modes					
SID281	VIN	Charge-pump on, VDDA = > 2.7 V	-0.05	-	VDDA-0.2	V	
SID282	VCM	Charge-pump on, VDDA => 2.7 V	-0.05	-	VDDA-0.2	V	-
	VOUT	VDDA=> 2.7 V					-
SID283	VOUT_1	power = hi, Iload=10 mA	0.5	-	V_{DDA} -0.5	V	-
SID284	VOUT_2	power = hi, Iload=1 mA	0.2	-	V_{DDA} -0.2	V	-
SID285	VOUT_3	power = med, Iload = 1 mA	0.2	-	V_{DDA} -0.2	V	-
SID286	VOUT_4	power = lo, Iload = 0.1 mA	0.2	-	V_{DDA} -0.2	V	-
SID288	VOS_TR	Offset voltage, trimmed	-1	+/-0. 5	1	mV	High mode, input 0 V to VDDA-0.2 V
SID288A	VOS_TR	Offset voltage, trimmed	-	+/-1	-	mV	Medium mode, input 0 V to $_{VDDA-0.2}$ V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID288B	VOS_TR	Offset voltage, trimmed	-	+/-2	-	mV	Low mode, input 0 V to VDDA-0.2 V
SID290	VOS_DR_TR	Offset voltage drift, trimmed	-10	+/-3	10	µV/°C	High mode
SID290A	VOS_DR_TR	Offset voltage drift, trimmed	-	+/10	-		Medium mode
SID290B	VOS_DR_TR	Offset voltage drift, trimmed	-	+/-10	-		Low mode
SID291	CMRR	DC	70	80	-	dB	Input is 0V to $_{VDDA-0.2}$ V, Output is 0.2 V to VDDA-0.2 V
SID292	PSRR	At 1 kHz, 10 mV ripple	70	85	-		V_{DDD} = 3.6 V, high power mode, input is 0.2 V to VDDA-0.2 V
	Noise						
SID293	VN1	input-referred, 1 Hz - 1 GHz, power = Hi	-	94	-	µVrms	Input and Output are at 0.2 V to $_{VDDA-0.2}$ V
SID294	VN2	input-referred, 1 kHz, power = Hi	-	72	-	nV/rtHz	Input and Output are at 0.2 V to $_{VDDA-0.2}$ V
SID295	VN3	input-referred, 10 kHz, power = Hi	-	28	-		Input and Output are at 0.2 V to VDDA-0.2V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID296	VN4	input-referred, 100 kHz, power = Hi	-	15	-		Input and Output are at 0.2 V to $V_{DDA-0.2}$ V
SID297	CLOAD	Stable up to maximum load. Performance specs at 50 pF.	-	-	125	pF	-
SID298	SLEW_RATE	Cload = 50 pF, Power = High, VDDA => 2.7 V	4	-	-	V/µs	-
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	-	-	25	µs	-
SID299A	OL_GAIN	Open Loop Gain		90		dB	-
	COMP_MODE	Comparator mode; 50 mV drive, Trise = Tfall (approx.)					
SID300	TPD1	Response time; power = hi	-	150	-	ns	Input is 0.2 V to VDDA-0.2 V
SID301	TPD2	Response time; power = med	-	500	-		Input is 0.2 V to VDDA-0.2 V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID302	TPD3	Response time; power = lo	-	2500	-		Input is 0.2 V to VDDA-0.2 V
SID303	VHYST_OP	Hysteresis	-	10	-	mV	-
SID304	WUP_CTB	Wake-up time from Enabled to Usable	-	-	25	µs	-
	DEEP SLEEP MODE	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	IDD_HI_M1	Mode 1, High current	-	1400	-	µA	25°C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	-	700	-		25°C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	-	200	-		25°C
SID_DS_4	IDD_HI_M2	Mode 2, High current	-	120	-		25°C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	-	60	-		25°C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	-	15			25°C
SID_DS_7	GBW_HI_M1	Mode 1, High current	-	4	-	MHz	20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	-	2	-		20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	-	0.5	-		20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V
SID_DS_10	GBW_HI_M2	Mode 2, High current	-	0.5	-		20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	-	0.2	-		20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V
SID_DS_12	GBW_Low_M2	Mode 2, Low current	-	0.1	-		20 pF load, no DC load 0.2 V to $_{VDDA-0.2}$ V
SID_DS_13	VOS_HI_M1	Mode 1, High current	-	5	-	mV	With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	-	5	-		With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	-	5	-		With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	-	5	-		With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	-	5	-		With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	-	5	-		With trim 25°C, 0.2 V to VDDA-0.2 V
SID_DS_19	IOUT_HI_M!	Mode 1, High current	-	10	-	mA	Output is 0.5 V to VDDA-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	-	10	-		Output is 0.5 V to VDDA-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	-	4	-		Output is 0.5 V to VDDA-0.5 V

(table continues...)

Table 13 (continued) CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID_DS_22	IOUT_HI_M2	Mode 2, High current	-	1	-		-
SID_DS_23	IOU_MED_M2	Mode 2, Medium current	-	1	-		-
SID_DS_24	IOU_LOW_M2	Mode 2, Low current	-	0.5	-		-

7.3.2 Comparator

Table 14 Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID84	VOFFSET1	Input offset voltage, Factory trim	–	–	±10	mV	–
SID85	VOFFSET2	Input offset voltage, Custom trim	–	–	±4		–
SID86	VHYST	Hysteresis when enabled	–	10	35		–
SID87	VICM1	Input common mode voltage in normal mode	0	–	VDDD-0.1	V	Modes 1 and 2
SID247	VICM2	Input common mode voltage in low power mode	0	–	VDDD		–

(table continues...)

Table 14 (continued) Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID247A	VICM3	Input common mode voltage in ultra low power mode	0	–	VDDD- 1.15		VDDD ≥ 2.2 V at –40°C
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	CMRR	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V
SID89	ICMP1	Block current, normal mode	–	–	400	µA	–
SID248	ICMP2	Block current, low power mode	–	–	100		–
SID259	ICMP3	Block current in ultra low-power mode	–	6	28		V_{DDD} ≥ 2.2 V at –40°C
SID90	ZCMP	DC Input impedance of comparator	35	–	–	MO	–

Table 15 Comparator AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	–

(table continues...)

Table 15 (continued) Comparator AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	$V_{DDD} \geq 2.2$ V at –40°C

7.3.3 Temperature sensor

Table 16 Temperature sensor specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +125°C

7.3.4 SAR ADC

Table 17 SAR ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SAR ADC DC specifications							
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		–
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes

(table continues...)

Table 17 (continued) SAR ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1 V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–
SID260	VREFSAR	Trimmed internal reference to SAR	1.188	1.2	1.212	V	–
SAR ADC AC specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	–
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz

(table continues...)

Table 17 (continued) SAR ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID110	A_BW	Input bandwidth without aliasing	–	–	A_sam p/2	kHz	–
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 to VDD
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 to VDD
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 to VDD
SID112	A_DNL	Differential non linearity. VDD = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 to VDD
SID112A	A_DNL	Differential non linearity. VDD = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 to VDD
SID112B	A_DNL	Differential non linearity. VDD = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 to VDD
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz

(table continues...)

Table 17 (continued) SAR ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID261	FSARINTREF	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution

7.3.5 CAPSENSE™ block (MSC) specifications

Table 18 MSC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
MSC specifications							
SID.MSC.1	VDD_RIPPLE	Max allowed ripple on power supply, 1 kHz to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25°C TA, Sensitivity = 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SID.MSC.2	VDD_RIPPLE_1.8	Max allowed ripple on power supply, 1 kHz to 10 MHz	–	–	±25	mV	V_{DD} > 1.75 V (with ripple), 25°C T_A, Sensitivity = 50 counts/0.1 pF, 2 pF < Cs < 50 pF

(table continues...)

Table 18 (continued) MSC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.MSC.x1	Fmod	Clock frequency	–	–	48	MHz	V_{DD} > 2 V (with ripple), 25°C T_A, Sensitivity = 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SID.MSC.x2	FMOD_1.8	Clock frequency	–	–	36	MHz	V_{DD} > 1.75 V (with ripple), 25°C T_A, Sensitivity = 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SID.MSC.3	IMSC_VDDA	Current drawn by block from VDDA	–	650	–	µA	Current drawn from VDDA during a scan. CSD scan with Cs < 20 pF, VDDA = 3.3 V, Fmod = 48 MHz, Fs = 1 MHz
SID.MSC.5	VMSC	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5%, 3.3 V±10%, 5.5 V ±10% (spec will change – depending on device operation)

(table continues...)

Table 18 (continued) MSC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.MSC.6	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 50 pF, Sensitivity = 50 counts/pF. V_{DDA} > 2 V.
SID.MSC.7	CMOD	External modulator capacitor.	–	2.2	–	nF	6-V rating (or higher), X7R cap, or NP0/C0G cap for hot temperature operation
SID.MSC.x7	CMOD tolerance	External modulator capacitor.	-5	–	5	%	Tolerance on CMOD capacitor.
SID.MSC.x8	Fsense	Capacitive sense freq. range	45	–	6000	kHz	–
SID.MSC.9	Noise Floor (CNS)	Capacitive noise sensitivity	–	–	0.1	fF	With 8-pF input capacitance
SID.MSC.10	Input Range (CIN)	Input capacitance range	2	–	200	pF	–

7.4 Digital peripherals

7.4.1 Timer counter pulse-width modulator (TCPWM)

Table 19 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)

(table continues...)

Table 19 (continued) TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPW_{MFREQ}$	Operating frequency	–	–	Fc	MHz	Fc maximum = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWMENEXT	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[1)]
SID.TCPWM.5	TPWMEXT	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TCRES	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

1) Guaranteed by characterization.

7.4.2 I²C

Table 20 Fixed I²C DC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID149	II2C1	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	II2C2	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	II2C3	Block current consumption at 1 Mbps	–	–	310	µA	–
SID151H	II2C5	Block current consumption at 3.4 Mbps	–	–	1000	µA	–
SID152	II2C4	Block current in Deep Sleep mode	–	1	–	µA	–

1) Guaranteed by characterization.

Table 21 Fixed I²C AC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID153	FI2C1	Bit rate	–	–	3.4[1)]	Msps	–

1) Slave only in HS mode.

7.4.3 SPI

Table 22 SPI DC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–

(table continues...)

Table 22 (continued) SPI DC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

1) Guaranteed by characterization.

Table 23 SPI AC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID166	FSPI	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–
Fixed SPI Master Mode AC specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC specifications							
SID170	TDMI	MOSI Valid before Sclock	40	–	–	ns	–
		Capturing edge					
SID171	TDSO	MISO Valid after Sclock	–	–	42 + (3 ×		T_{CPU} = 1/FCPU
		driving edge			Tcpu)		

(table continues...)

Table 23 (continued) SPI AC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

7.4.4 UART

Table 24 UART DC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID160	IUART1	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	IUART2	Block current consumption at 1000 Kbps	–	–	312	µA	–

1) Guaranteed by characterization.

Table 25 UART AC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID162	FUART	Bit rate	–	–	1	Mbps	–

Table 26 CAN FD specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.CAN.1	FCANFD	CAN FD peak frequency	–	–	5	MHz	–

7.4.5 LCD direct drive

Table 27 LCD direct drive DC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID154	ILCDLOW	Operating current in low power mode	–	5	–	µA	16 x 4 small segment disp. at 50 Hz
SID155	CLCDCAP	LCD capacitance per segment/ common driver	–	500	5000	pF	–
SID156	LCDOFFSET	Long-term segment offset	–	20	–	mV	–
SID157	ILCDOP1	LCD system operating current Vbias = 5 V	–	2	–	mA	32 x 4 segments at 50 Hz 25°C
SID158	ILCDOP2	LCD system operating current Vbias = 3.3 V	–	2	–		32 x 4 segments at 50 Hz 25°C

1) Guaranteed by characterization.

Table 28 LCD direct drive AC specifications[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID159	FLCD	LCD frame rate	10	50	150	Hz	–

7.5 Memory

7.5.1 Flash

Table 29 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID173	VPE	Erase and program voltage	1.71	–	5.5	V	–

(table continues...)

Table 29 (continued) Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID173A	IPW	Page write current at 16 MHz	–	–	3.5	mA	5.5 V VDD

Table 30 Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID174	TROWWRITE[1)]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	TROWERASE[1)]	Row erase time	–	–	16		–
SID176	TROWPROGRAM[1)]	Row program time after erase	–	–	4		–
SID178	TBULKERASE[1)]	Bulk erase time (64 KB)	–	–	35		–
SID180[2)]	TDEVPROG[1)]	Total device program time	–	–	7	Seconds	–
SID181[2)]	FEND	Flash endurance	100K	–	–	Cycles	–
SID182[2)]	FRET	Flash retention. T_A £ 55°C, 100K P/E cycles	20	–	–	Years	–
SID182A[2)]	–	Flash retention. T_A £ 85°C, 10K P/E cycles	10	–	–		–
SID182B	–	Flash retention. T_A £ 105°C, 10K P/E cycles, £ three years at T_A ≥ 85°C	10	–	20		–

(table continues...)

Table 30 (continued) Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

1) It can take as much as 20 milliseconds to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
2) Guaranteed by characterization.

7.6 System resources

7.6.1 Power-on reset (POR)

Table 31 Power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1[1)]	–	67	V/ms	At power-up
SID185[2)]	VRISEIPOR	Rising trip voltage	0.80	–	1.5	V	–
SID186[2)]	VFALLIPOR	Falling trip voltage	0.70	–	1.4		–

1) If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp (1.5 V > VDDD > 1.0 V for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I2C bus could occur during voltage ramp in this case.
2) Guaranteed by characterization.

7.6.2 Brown-out detect (BOD)

Table 32 Brown-out detect (BOD) for VCCD

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID190[1)]	VFALLPPOR	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–

(table continues...)

Table 32 (continued) Brown-out detect (BOD) for VCCD

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID192[1)]	VFALLDPSLP	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

1) Guaranteed by characterization.

7.6.3 SWD interface

Table 33 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} £ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[1)]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID216[1)]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		–
SID217[1)]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T		–
SID217A[2)]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

1) Guaranteed by design.
2) Guaranteed by characterization.

7.6.4 Internal main oscillator

Table 34 IMO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID218	IIMO1	IMO operating current at 48 MHz	–	–	250	µA	–

(table continues...)

Table 34 (continued) IMO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID219	IIMO2	IMO operating current at 24 MHz	–	–	180	µA	–

Table 35 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID223	FIMOTOL1	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	–40°C ≤ TA ≤ 105°C
SID223A	FIMOTOL1A	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2.5	%	–40°C ≤ TA ≤ 125°C
SID333	IMOWCO	All IMO settings	–	–	±0.25	%	IMO variation in WCO-locked DPLL mode
SID226	TSTARTIMO	IMO startup time	–	–	7	µs	–
SID228	TJITRMSIMO 2	RMS jitter at 24 MHz	–	145	–	ps	–

7.6.5 Internal low-speed oscillator

Table 36 ILO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID231	IILO1	ILO operating current	–	0.3	1.05	µA	–

Table 37 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID234[1)]	TSTARTILO1	ILO startup time	–	–	2	ms	–
SID236[1)]	TILODUTY	ILO duty cycle	40	50	60	%	–
SID237	FILOTRIM1	ILO frequency range	20	40	80	kHz	–

1) Guaranteed by characterization.

7.6.6 Watch crystal oscillator (WCO)

Table 38 WCO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive Level	–	–	1	µW	–
SID402	TSTART	Startup time	–	–	500	ms	–
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	–
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	–
SID405	IWCO1	Operating Current (high power mode)	–	–	8	µA	–

7.6.7 External clock

Table 39 External clock specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID305[1)]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306[1)]	ExtClkDuty	Duty cycle; measured at VDD/2	45	–	55	%	–

1) Guaranteed by design.

7.6.8 External crystal oscillator and PLL

Table 40 External crystal oscillator (ECO) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID316[1)]	IECO1	ECO Block operating current	–	–	1.5	mA	–
SID317[1)]	FECO	Crystal frequency range	4	–	33	MHz	–

1) Guaranteed by characterization.

Table 41 PLL specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	µA	–
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	µA	–
SID412	Fpllin	PLL input frequency	1	–	48	MHz	–
SID413	Fpllint	PLL intermediate frequency; prescaler out	1	–	3	MHz	–

(table continues...)

Table 41 (continued) PLL specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID414	Fpllvco	VCO output frequency before post-divide	22.5	–	104	MHz	–
SID415	Divvco	VCO Output post-divider range; PLL output frequency is Fpplvco/ Divvco	1	–	8		–
SID416	Plllocktime	Lock time at startup	–	–	250	µs	–
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed by design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed by design

7.6.9 System clock

Table 42 Block specs

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID262[1)]	TCLKSWITCH	System clock source switching time	3	–	4	Periods	–

1) Guaranteed by characterization.

7.6.10 Smart I/O

Table 43 Smart I/O pass-through time (Delay in Bypass mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	–

7.6.11 I2S

Table 44 I2S Master mode (TX specifications only)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID413M	I2S_WORD	Length of I2S Word	8	–	24	bits	–
SID414M	I2S_WS_U	Word clock frequency	–	–	48	kHz	3.072 MHz bit clock with 32-bit word
SID415S	I2S_SCK	Output clock frequency	–	–	2.304	MHz	24 bits L-R channels at 48 kHz
SID437U	TD_WS_U	WS transition delay from falling edge of SCK	–20	–	20	ns	–
SID438U	TD_SDO	SDO transition delay from falling edge of SCK	–20	–	20	ns	–
SID443	TSCKCY	SCK bit clock duty cycle	45	–	55	%	–
SID445	FMCLK_SOC	MCLK_SOC frequency in LP mode	1.024	–	48	MHz	
SID446	TMCLKCY	MCLK_SOC duty cycle	45	–	55	%	–

8 Ordering information

Table 45 lists the marketing part numbers (MPNs) for the PSOC™ 4100S Max devices.

Table 45 Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZA-S548	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4147AZE-S548	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X
CY8C4147AZS-S548	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-
CY8C4147AZA-S555	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	X	-	-
CY8C4147AZS-S555	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZE-S555	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	-	X
CY8C4147AZA-S558	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4147AZS-S558	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-
CY8C4147AZE-S558	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X
CY8C4147AZA-S565	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZS-S565	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4147AZE-S565	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X
CY8C4147AZA-S568	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-
CY8C4147AZS-S568	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-
CY8C4147AZE-S568	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZA-S575	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-
CY8C4147AZS-S575	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4147AZE-S575	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X
CY8C4147AZA-S578	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-
CY8C4147AZS-S578	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZE-S578	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X
CY8C4147AZA-S585	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	X	-	-
CY8C4147AZS-S585	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	X	-
CY8C4147AZE-S585	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	-	X
CY8C4147AZA-S588	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZS-S588	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	X	-
CY8C4147AZE-S588	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	-	X
CY8C4147AZA-S595	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	X	-	-
CY8C4147AZS-S595	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	X	-
CY8C4147AZE-S595	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147AZA-S598	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	X	-	-
CY8C4147AZS-S598	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	X	-
CY8C4147AZE-S598	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	-	X
CY8C4148AZA-S545	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	X	-	-
CY8C4148AZS-S545	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZE-S545	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	-	X
CY8C4148AZA-S548	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4148AZS-S548	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-
CY8C4148AZE-S548	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X
CY8C4148AZA-S555	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZS-S555	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	X	-
CY8C4148AZE-S555	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	-	X
CY8C4148AZA-S558	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4148AZS-S558	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-
CY8C4148AZE-S558	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZA-S565	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-
CY8C4148AZS-S565	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4148AZE-S565	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X
CY8C4148AZA-S568	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-
CY8C4148AZS-S568	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZE-S568	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X
CY8C4148AZA-S575	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-
CY8C4148AZS-S575	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4148AZE-S575	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X
CY8C4148AZA-S578	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZS-S578	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-
CY8C4148AZE-S578	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X
CY8C4148AZA-S585	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	X	-	-
CY8C4148AZS-S585	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	X	-
CY8C4148AZE-S585	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZA-S588	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	X	-	-
CY8C4148AZS-S588	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	X	-
CY8C4148AZE-S588	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	-	X
CY8C4148AZA-S595	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	X	-	-
CY8C4148AZS-S595	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148AZE-S595	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	-	X
CY8C4148AZA-S598	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	X	-	-
CY8C4148AZS-S598	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	X	-
CY8C4148AZE-S598	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	-	X
CY8C4149AZA-S545	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZS-S545	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	X	-
CY8C4149AZE-S545	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	-	X
CY8C4149AZA-S548	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4149AZS-S548	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-
CY8C4149AZE-S548	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZA-S555	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	X	-	-
CY8C4149AZS-S555	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	X	-
CY8C4149AZE-S555	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	54	-	X	-	-	-	X
CY8C4149AZA-S558	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	X	-	-
CY8C4149AZS-S558	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZE-S558	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	84	X	-	-	-	-	X
CY8C4149AZA-S565	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-
CY8C4149AZS-S565	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4149AZE-S565	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X
CY8C4149AZA-S568	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZS-S568	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-
CY8C4149AZE-S568	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X
CY8C4149AZA-S575	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	X	-	-
CY8C4149AZS-S575	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	X	-
CY8C4149AZE-S575	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	54	-	X	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZA-S578	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	X	-	-
CY8C4149AZS-S578	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	X	-
CY8C4149AZE-S578	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	84	X	-	-	-	-	X
CY8C4149AZA-S585	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	X	-	-
CY8C4149AZS-S585	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZE-S585	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	54	-	X	-	-	-	X
CY8C4149AZA-S588	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	X	-	-
CY8C4149AZS-S588	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	X	-
CY8C4149AZE-S588	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	84	X	-	-	-	-	X
CY8C4149AZA-S595	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149AZS-S595	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	X	-
CY8C4149AZE-S595	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	54	-	X	-	-	-	X
CY8C4149AZA-S598	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	X	-	-
CY8C4149AZS-S598	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	X	-
CY8C4149AZE-S598	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	84	X	-	-	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147LDA-S543	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-
CY8C4147LDE-S543	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4147LDS-S543	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-
CY8C4147LDA-S553	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-
CY8C4147LDS-S553	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147LDE-S553	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4147LDA-S563	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-
CY8C4147LDS-S563	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4147LDE-S563	48	128	16	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X
CY8C4147LDA-S573	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147LDS-S573	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4147LDE-S573	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X
CY8C4147LDA-S583	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	X	-	-
CY8C4147LDS-S583	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	X	-
CY8C4147LDE-S583	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4147LDA-S593	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	X	-	-
CY8C4147LDS-S593	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	X	-
CY8C4147LDE-S593	48	128	16	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	-	X
CY8C4148LDA-S543	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-
CY8C4148LDS-S543	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148LDE-S543	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4148LDA-S553	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-
CY8C4148LDS-S553	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-
CY8C4148LDE-S553	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4148LDA-S563	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148LDS-S563	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4148LDE-S563	48	256	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X
CY8C4148LDA-S573	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-
CY8C4148LDS-S573	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4148LDE-S573	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148LDA-S583	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	X	-	-
CY8C4148LDS-S583	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	X	-
CY8C4148LDE-S583	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	-	X
CY8C4148LDA-S593	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	X	-	-
CY8C4148LDS-S593	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	X	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4148LDE-S593	48	256	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	-	X
CY8C4149LDA-S543	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-
CY8C4149LDS-S543	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-
CY8C4149LDE-S543	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4149LDA-S553	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	X	-	-

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149LDS-S553	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	X	-
CY8C4149LDE-S553	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	-	40	-	-	X	-	-	X
CY8C4149LDA-S563	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-
CY8C4149LDS-S563	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4149LDE-S563	48	384	32	2	-	-	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X

(table continues...)

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149LDA-S573	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	X	-	-
CY8C4149LDS-S573	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	X	-
CY8C4149LDE-S573	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	-	40	-	-	X	-	-	X
CY8C4149LDA-S583	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	X	-	-
CY8C4149LDS-S583	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	X	-

(table continues...)

8 Ordering information

Table 45 (continued) Ordering information

Product	Features																Packages			Temperature		
	Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CAPSENSE™	I2S	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB Blocks	WCO	ECO	Smart I/Os	CAN FD	CRYPTO	GPIO	100-TQFP	64-TQFP	48-QFN	-40 to +85°C	-40 to +105°C	-40 to +125°C
CY8C4149LDE-S583	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	-	X	40	-	-	X	-	-	X
CY8C4149LDA-S593	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	X	-	-
CY8C4149LDS-S593	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	X	-
CY8C4149LDE-S593	48	384	32	2	2	X	X	1000 Ksps	2	8	5	X	X	24	1	X	40	-	-	X	-	-	X

8 Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Table 46 Part number convetion

Field	Description	Values	Meaning
CY8C	Infineon prefix		
4	Architecture	4	PSOC™ 4
A	Family	1	4100 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	7	128 KB
		8	256 KB
		9	384 KB
DE	Package code	AZ	TQFP (0.5-mm pitch)
		LD	QFN
F	Temperature range	A	Automotive (AEC-Q100: –40°C to +85°C)
		S	Automotive (AEC-Q100: –40°C to +105°C)
		E	Automotive (AEC-Q100: –40°C to +125°C)
S	Silicon family	S	PSOC™ 4 S-series
		M	PSOC™ 4 M-series
		L	PSOC™ 4 L-series
		BL	PSOC™ 4 Bluetooth® LE-series
XYZ	Attributes code	000-999	Code of feature set in the specific family

The following is an example of a part number:

8 Ordering information

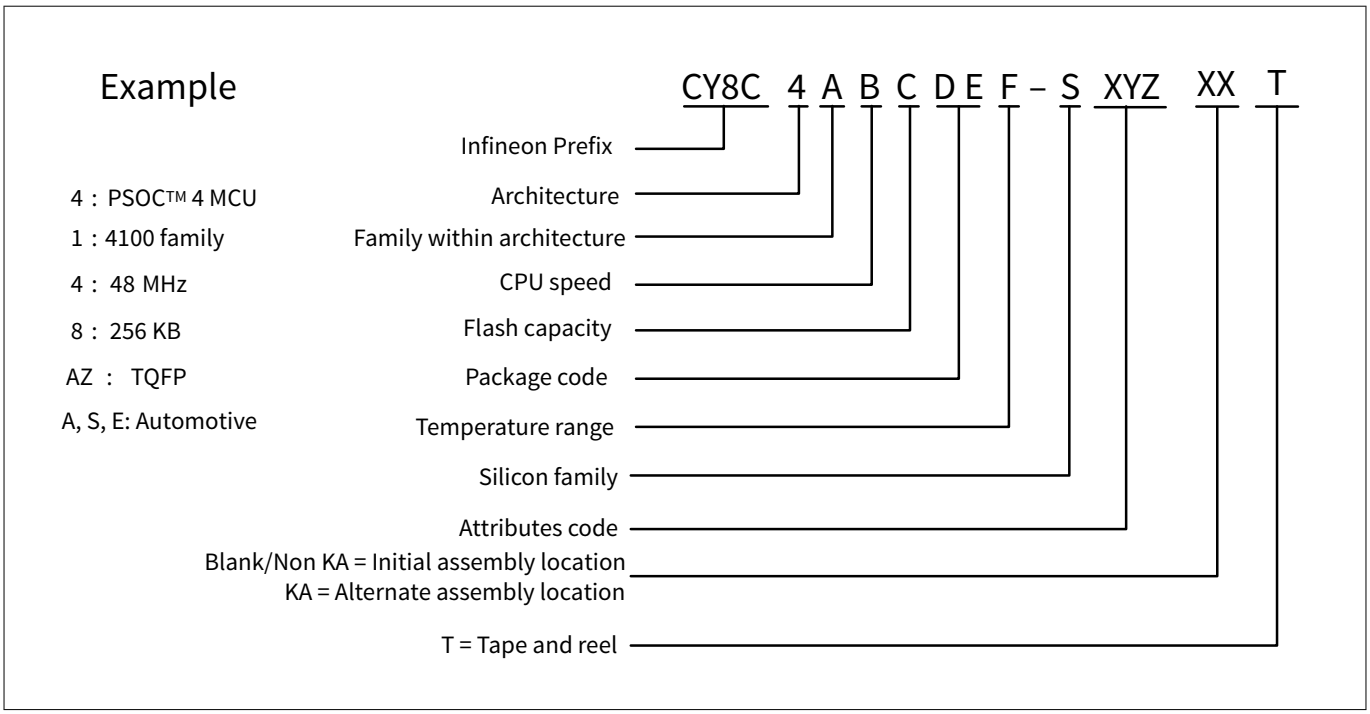


Figure 10 Part number nomenclature

9 Packaging

The PSOC™ 4100S Max will be offered in 48-pin QFN, 64-pin TQFP, and 100-pin TQFP packages. Table 47 provides the package dimensions and Infineon drawing numbers.

Table 47 Package list

Spec ID#	Package	Description	Package drawing
BID27	64-pin TQFP	10 × 10 × 1.4-mm height with 0.5-mm pitch	51-85051
BID34	100-pin TQFP	14 × 14 × 1.4-mm height with 0.5-mm pitch	51-85048
BID34B	48-pin QFN	7 × 7 × 0.9-mm height with 0.5-mm pitch with wettable flanks	002-33925

Table 48 Package thermal characteristics

Parameter	Description	Package	Conditions	Min	Typ	Max	Unit
TA	Operating ambient temperature	–	For A-grade devices	–40	25	85	°C
			For S-grade devices	–40	25	105	
			For E-grade devices	–40	25	125	
TJ	Operating junction temperature	–	For A-grade devices	–40	–	100	
			For S-grade devices	–40	–	115	
			For E-grade devices	–40	–	140	
TJA	Package θJA	64-pin TQFP (0.5-mm pitch)	–	–	44.8	–	°C/Watt
		100-pin TQFP		–	35.2	–	
		48-pin QFN		–	13.18	–	
TJC	Package θJC	64-pin TQFP (0.5-mm pitch)	–	–	6	–	°C/Watt
		100-pin TQFP		–	4.2	–	
		48-pin QFN		–	6.41	–	

9 Packaging

Table 49 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All	260°C	30 seconds

Table 50 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

9.1 Package diagram

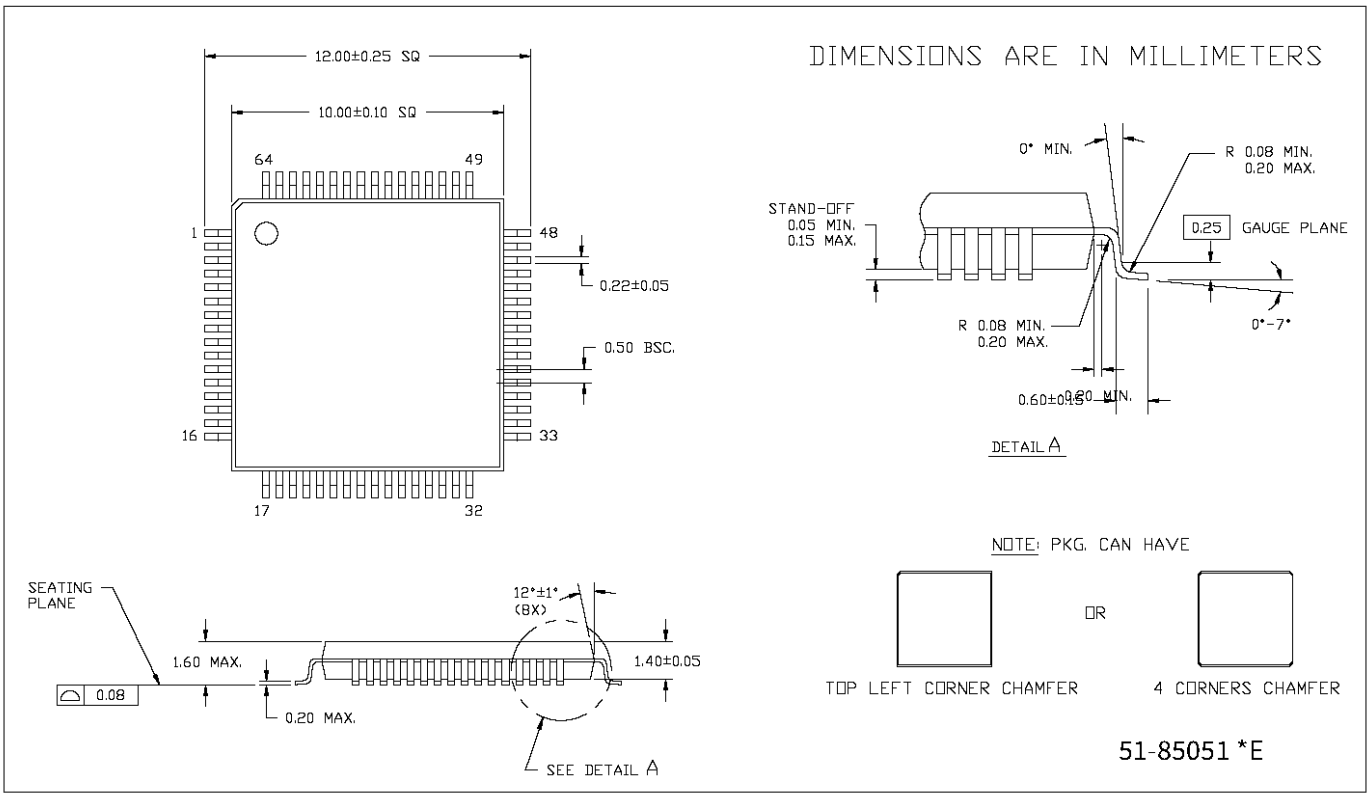


Figure 11 64-pin TQFP (10 × 10 × 1.4 mm) package outline (PG-TQFP-64-802)

9 Packaging

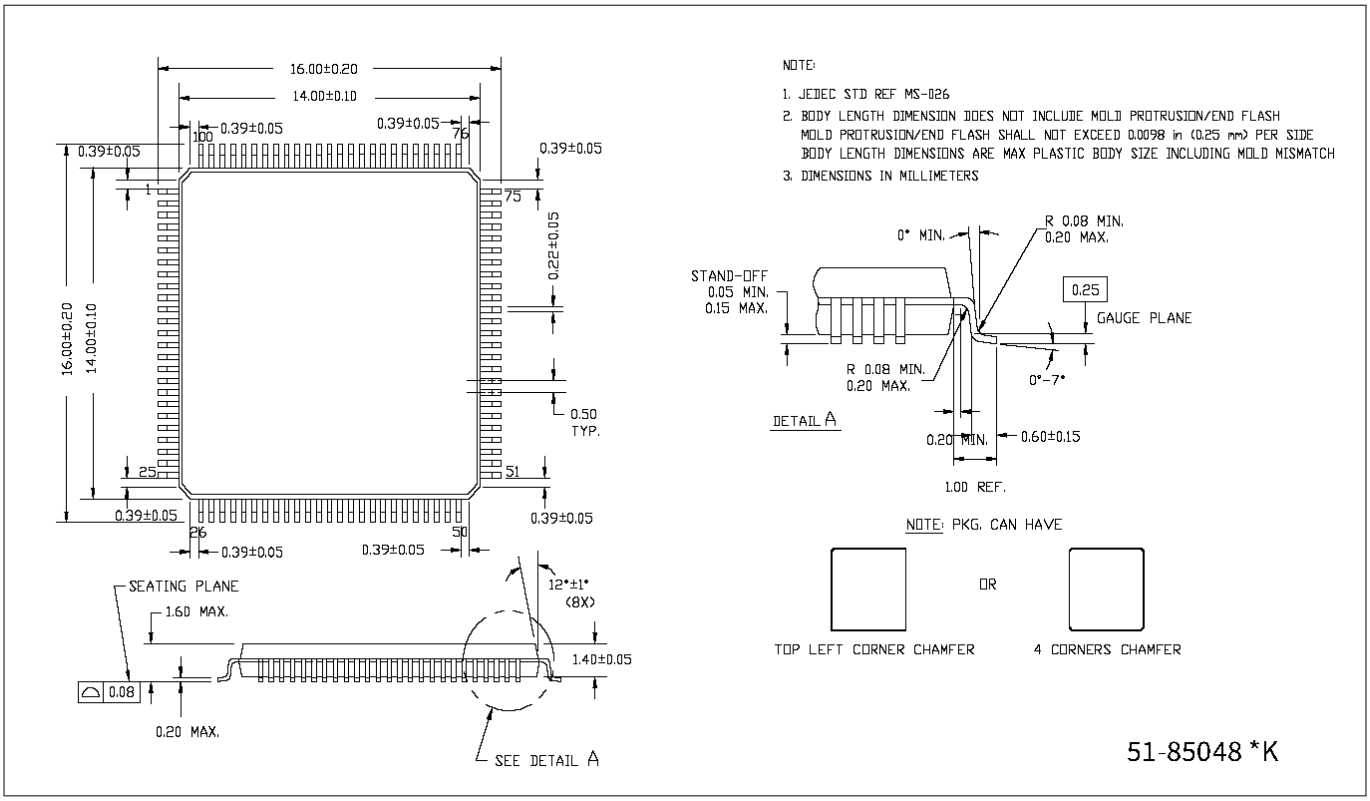
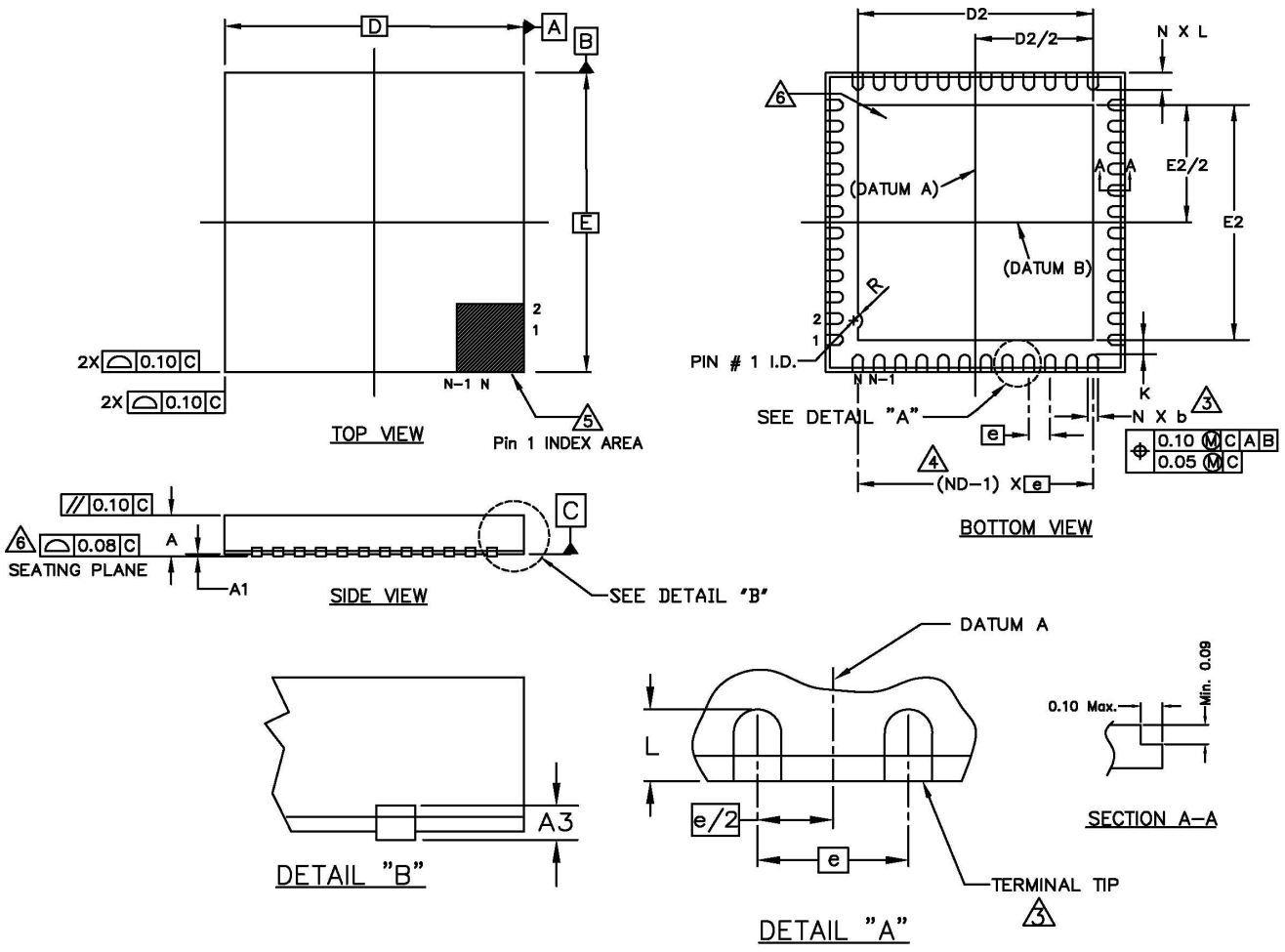


Figure 12 100-pin TQFP (14 × 14 × 1.4 mm) package outline (PG-TQFP-100-801)

9 Packaging



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		48	
ND		12	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
D		7.00 BSC	
E		7.00 BSC	
A	-	-	0.90
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.35 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-33925 *B

Figure 13 48-pin QFN (7 × 7 × 0.9 mm) package outline, 002-33925

10 Acronyms

Table 51 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame

(table continues...)

10 Acronyms

Table 51 (continued) Acronyms used in this document

Acronym	Description
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSOCTM pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt

(table continues...)

Table 51 (continued) Acronyms used in this document

Acronym	Description
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSOCTM	Programmable system on chip
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data

(table continues...)

10 Acronyms

Table 51 (continued) Acronyms used in this document

Acronym	Description
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSOCTM pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

11 Document conventions

11.1 Units of measure

Table 52 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kQ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MQ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million

(table continues...)

Table 52 (continued) Units of measure

Symbol	Unit of measure
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

12 Errata

This section describes the errata for the PSOC™ 4100S Max. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Sales Representative if you have questions.

Part numbers affected

Table 53 Part number effected

Part number	Device characteristics
CY8C414X-S5XX	PSOC™ 4100S Max

PSOC™ 4100S errata summary

The following table defines the errata applicability to available PSOC™ 4100S Max family devices.

Items	PSOC™ 4100S Max	Silicon revision	Fix status
#unique_3/unique_3_Connect_42_entry_eg5_z5s_bkc	All	Pre-production silicon	No silicon fix planned.
#unique_3/unique_3_Connect_42_entry_hp2_1vs_bkc			

1. Mutual cap sensors may not get initialized correctly in CTRLMUX connection method.	
Problem definition	Incorrect raw count may be obtained in CTRLMUX mode
Parameters affected	Raw count
Trigger condition(s)	CTRLMUX mode
Scope of impact	Incorrect sensor reading
Workaround	One of the following workarounds may be used. 1. Increase the number of init sub-conversions to allow correct Cmod initialization. 2. Group all CSX sensors to consecutive slots. Set the inactive sensor connection to VDD/2 and add an extra scan for the first CSX sensor, ignore the raw count result of this extra scan. 3. Use the AMUXBUS sensor connection method. See thePSOC™ 4 and PSOC™ 6 CAPSENSE™ design guide for details on how to implement the above workarounds.
Fix status	No fix planned.

When using the CTRLMUX sensor connection method, the Rx nodes of mutual cap sensors may not get initialized to VDD/2 as expected, leading to improper Cmod initialization and improper raw counts, unless enough number of init sub-conversions are configured. In some cases, the raw count value may saturate to the maximum value.

***Note**: The raw count output for the same Rx node when scanned again for a different Tx (i.e., a touchpad where a sensor is connected to the same Rx but another Tx) will be correct because the Rx would have been properly initialized to VDD/2 during the previous sensor scan connected to this Rx.*

This defect does not impact the raw count when using the AMUXBUS sensor connection method as the sensor Rx does get initialized to VDDA/2 during Cmod initialization.

2. CMOD pins (MSC Block 0 - P4.0, P4.1, P4.2, P4.3) (MSC Block 1 – P5.1, P5.2, P7.0, P7.1) cannot be repurposed as mutual cap RX sensors	
Problem definition	Mutual cap RX operation is not possible when CMOD pins are configured as sensors.
Parameters affected	Raw count, CAPSENSE™ CSX operation affected
Trigger condition	CMOD pins used as mutual cap RX electrodes
Scope of impact	Raw count saturation
Workaround	None – these pins must not be assigned as CSX RX pins
Fix status	No fix planned

Do not assign CMOD pins for mutual cap RX sensor connections since this may lead to raw count saturation as this is not supported by the silicon.

Additional note: The CTRL mux mode is not supported for CMOD pins as sensor connection.

Revision history

Document version	Date of release	Description of changes
*D	2023-08-18	Datasheet to final
*E	2023-09-15	Updated Table 7 Updated Table 13. Updated Table 30. Updated Table 31
*F	2024-01-24	UpdateLCD segment drive Added footnotes and deleted the DSI column inTable 4. Updated CMOD capacitor recommendation. Added errata item 2.
*G	2025-03-11	Updated Features Added Figure 4, Figure 5 andFigure 6. Updated Figure 9. Updated Table 3, Table 4 and Table 5. Added Function name description
*H	2026-08-18	Template update Updated Table 5 Updated Table 13 Updated Table 40

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