

# PSOC™ 4 HVPA-144K

Based on 32-bit Arm® Cortex®-M0+

## General description

PSOC™ 4 high voltage precision analog (HVPA)-144K is a fully integrated programmable embedded system for lead acid battery monitoring and management. The system features an Arm® Cortex® M0+ processor and programmable and reconfigurable analog and digital blocks.

## Features

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- 32-bit MCU subsystem
  - 24 or 48 MHz Arm® Cortex® M0+ CPU with DMA controller
  - Up to 128 KB of code flash with ECC
  - Up to 8 KB of data flash with ECC
  - Up to 8 KB of SRAM with ECC
  - 1 KB of supervisory flash (SFlash) available for storing constants
- Precision analog
  - Two precision  $\Delta\Sigma$  ADCs (16-20+ bits)
  - Current channel with automatic gain
  - Voltage channel with HV input divider
  - Temperature and diagnostic channels
  - Supports both internal and external temperature sensing
  - Digital filtering, accumulators, and threshold comparisons on all channels
- High-voltage subsystem
  - Operates directly off 12 V/24 V battery (tolerates up to 42 V)
  - Integrated LIN transceiver
  - ADC input voltage divider
- Functional safety
  - The device is developed compliant to ISO 26262, meeting all process requirements for ASIL C and hardware architectural metrics for ASIL B (acc. ISO26262-10:2018E, clause 9).
  - Memory protection unit (MPU)
  - Window watchdog timer (WDT) with challenge-response functionality
  - Supply monitoring; detection of overvoltage and brownout events for 3.3 V and 1.8 V supplies
  - Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash)
  - Analog diagnostics (backup reference voltage, redundancy in voltage, current, and temperature measurement paths)
- Timing and pulse-width modulation
  - Four 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, Edge, and pseudo-random modes
  - Quadrature decoder
- Clock sources
  - $\pm 2\%$  up to 49.152 MHz internal main oscillator (IMO)
  - $\pm 1\%$  2 MHz high-precision oscillator (HPOSC)
  - $\pm 5\%$  or  $\pm 7\%$  32 kHz precision internal low-power oscillator (PILO) based on the part number
  - $\pm 1\%$  or  $\pm 1.5\%$  accuracy on IMO and PILO when software calibrated to the HPOSC based on the part number
  - 40 kHz internal low-speed oscillator (ILO)

## Features

- Communication
  - One independent run-time reconfigurable serial communication block (SCB) with re-configurable I<sup>2</sup>C, SPI, UART, or LIN Slave functionality
  - One independent local interconnect network (LIN) block with two channels
  - LIN protocol compliant with LIN 2.2A, 2.1, 2.0, 1.3, SAE J2602, and ISO 17987
- Package
  - 32-QFN with wettable flanks (6 x 6 mm)
  - Up to 9 GPIOs

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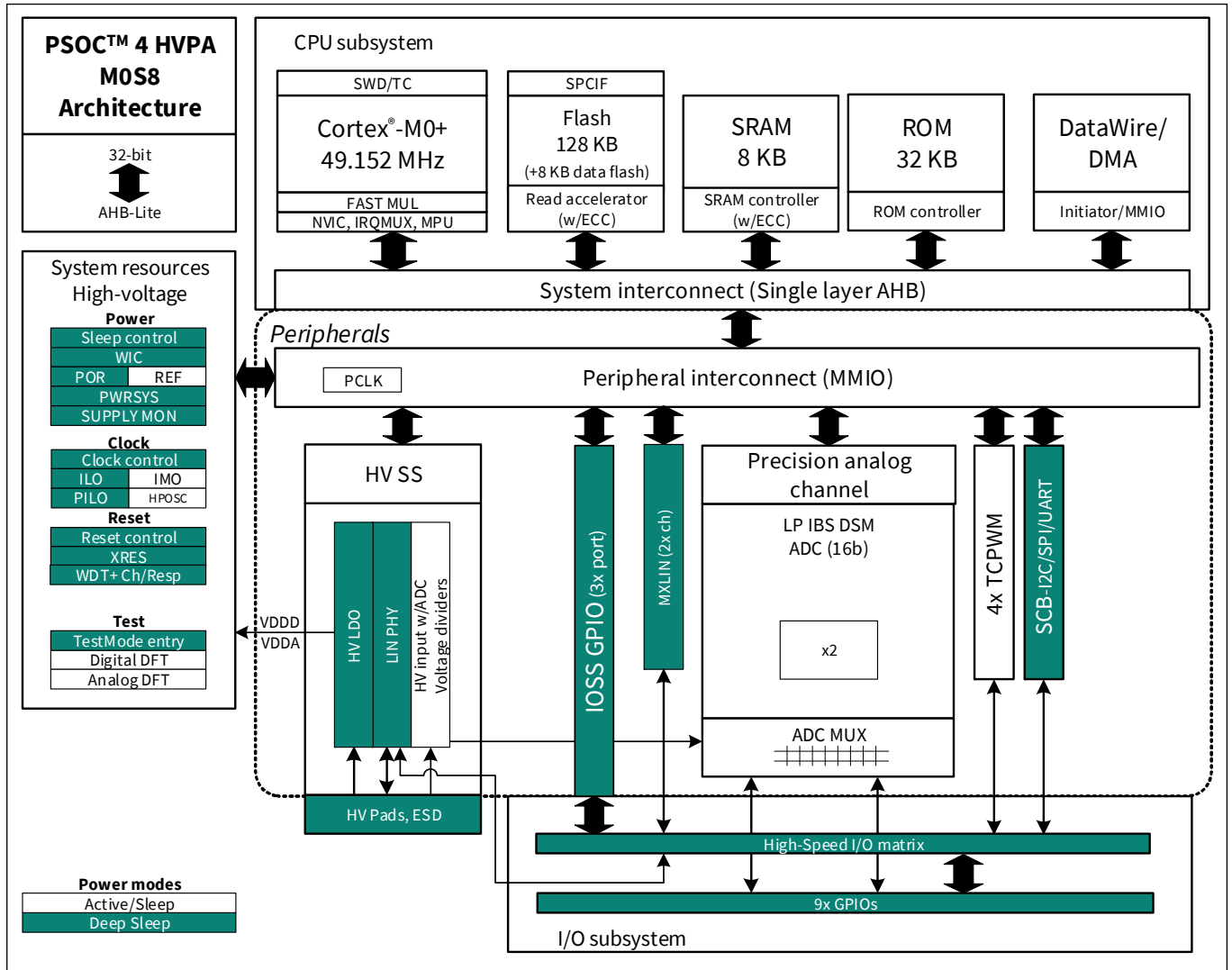
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**Block diagram**

**Block diagram**



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**Functional definition**

## **1 Functional definition**

### **1.1 CPU and memory subsystem**

#### **1.1.1 CPU**

The Arm® Cortex®-M0+ CPU in the PSOC™ 4 HVPA is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and includes a wakeup interrupt controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Arm® Cortex®-M0+ CPU provides a non-maskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

Programs can execute from SROM, SRAM, or Flash memory.

The CPU also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSOC™ 4 HVPA has four break-point (address) comparators and two watchpoint (data) comparators. The CPU also implements a design time configurable memory protection unit (MPU).

#### **1.1.2 Memory with ECC**

Flash and SRAM include error correction code (ECC) circuitry capable of correcting single-bit errors and detecting 2-bit errors. If a single-bit error occurs, the data is corrected in-line, error information is stored (address and data), and an error flag is set which can generate an interrupt. If a multi-bit error is detected, the error information is stored and either an interrupt or reset is generated.

#### **1.1.3 Flash**

The PSOC™ 4 HVPA has a flash module with separate controllers for code flash and data flash. The flash controller includes an accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% single-cycle SRAM access performance on average. Part of a flash module can be used to emulate EEPROM.

#### **1.1.4 SRAM**

Volatile static memory (SRAM) is used by the processor for storing variables and can program code, which can be written and executed in SRAM. SRAM memory is retained in all power modes (Active, Sleep, and Deep Sleep). At power-up, SRAM is uninitialized and should be written by application code before reading.

#### **1.1.5 SROM**

A supervisory read-only memory (ROM) contains boot and configuration routines which can't be modified.

#### **1.1.6 DMA**

A DMA engine with eight channels is provided that can do 32-bit transfers and has chainable ping-pong descriptors. This DMA engine allows data transfer between memory, registers, and peripherals without CPU intervention. DMA transfers can occur while the CPU is sleeping. Descriptors identify the data source and destination along with other information.

**Functional definition**

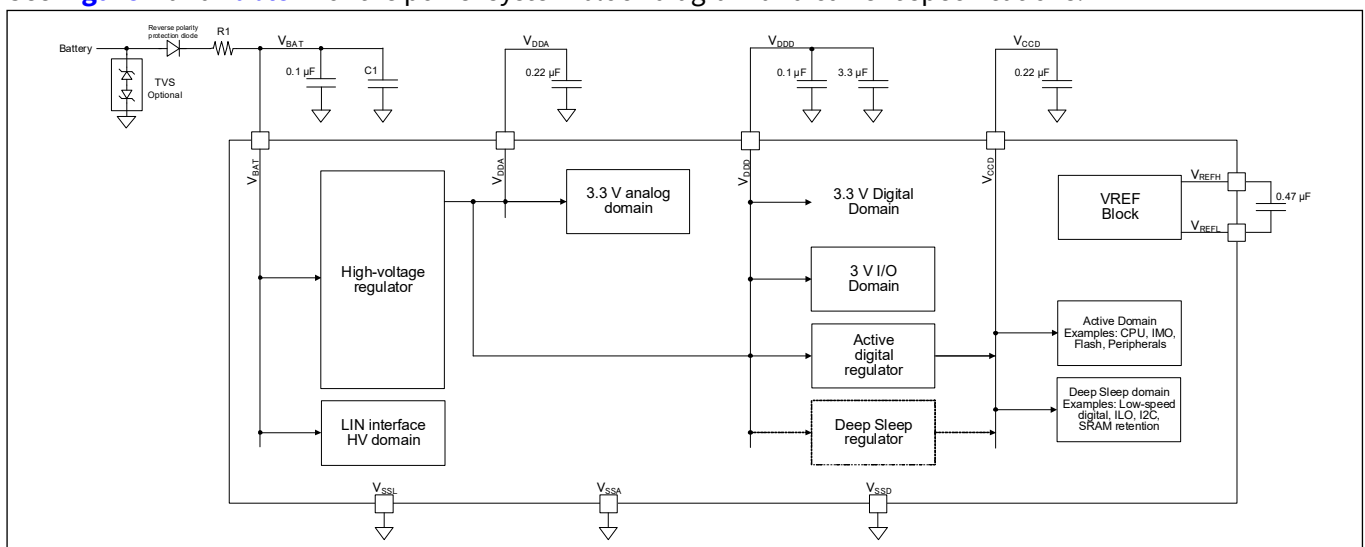
**1.2 System resources**

**1.2.1 Power system**

The power system includes regulators to generate appropriate voltages. The PSOC™ 4 HVPA operates at full performance from a single supply on VBAT over a voltage range of 3.6 V to 28 V and remains functional up to 42 V. In addition to an active mode, the PSOC™ 4 HVPA has two low-power modes called Sleep and Deep Sleep. Transitions between the three power modes are managed by the power system in the system resources subsystem (SRSS).

The high-voltage regulator generates a 3.3 V supply from VBAT for V<sub>DDA</sub> and V<sub>DDD</sub>. V<sub>DDA</sub> powers analog circuits, while V<sub>DDD</sub> provides power for I/Os (GPIOs) and the 1.8 V core power regulators. There are different internal core regulators to support the various power modes. These include an active digital regulator and a Deep Sleep regulator.

See [Figure 1](#) and [Table 1](#) for the power system block diagram and current specifications.



**Figure 1 Power system block diagram**

**Table 1 R1/C1 max current specifications**

Configuration	R1	C1	Max current
1	10-15 Ω	2.2 μF	20 mA
2	6.6-10 Ω	2 × 2.2 μF	30 mA

**Functional definition**

Bypass capacitors must be used from  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{CCD}$  to ground. These capacitors should typically be X7R ceramic or better.

**Table 2 Bypass capacitors**

Supply pair	Nominal cap	Tolerance
$V_{BAT} - V_{SSD}$	0.1 $\mu$ F 2.2 $\mu$ F	+65% / -65% +10% / -50%
$V_{DDD} - V_{SSD}$	0.1 $\mu$ F 3.3 $\mu$ F	+65% / -65% +10% / -50%
$V_{DDA} - V_{SSA}$	0.22 $\mu$ F	+10% / -50%
$V_{CCD} - V_{SSD}$	0.22 $\mu$ F	+10% / -50%
$V_{REFH} - V_{REFL}$	0.47 $\mu$ F	+38% / -48%

The system has a high-voltage (HV) regulator which generates 3.3 V supplies and several regulators for various low-voltage core domains. The analog circuits run directly from the VDDA supply generated by the HV regulator. The core regulators include an Active Digital regulator for digital circuitry and a separate regulator for Deep Sleep.

The HV regulator is always enabled. The active digital regulator is enabled during the Active or Sleep power modes. It is turned off in the Deep Sleep power mode. The Deep Sleep regulator fulfills power requirements in the low-power modes.

**Table 3 Regulators and operating modes**

Mode	HV regulator	Active regulator	Deep Sleep regulator
Active	On	On	On
Sleep	On	On	On
Deep Sleep	On	Off	On

**1.2.2 Power system supervision and monitoring**

The power supply includes supervision and monitoring to assure voltage levels as required exist for the respective modes. The voltage monitoring system includes power-on-reset (POR) and brownout detection (BOD). The supervisor either delays mode transitions (on POR, for example) until required voltage levels are achieved for proper function or generates resets (BOD, OVD) as appropriate.

- **Power-on reset (POR):** POR circuits provide a reset pulse during the initial power ramp. POR circuits monitor  $V_{DD}$  voltage. The POR threshold is between 0.8 V and 1.5 V and guarantees all circuits have been properly initialized prior to release. POR circuits are used during initial chip power-up and then disabled
- **Brownout detect (BOD):** The BOD circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. BOD circuit monitors the  $V_{CCD}$  voltage. The BOD circuit generates a reset if core voltage dips below the minimum safe operating voltage (1.48 V–1.62 V in Active/Sleep and 1.11 V–1.5 V in Deep Sleep). The system will not come out of RESET until the supply is detected to be valid again. To enable firmware to distinguish a normal power cycle from a brownout event, a special register is provided (RES\_CAUSE), which will not be cleared after a BOD generated RESET. However, this register will be cleared if the device goes through POR or XRES
- **Voltage references:** The SRSS includes a bandgap and current references for use by analog circuits and SRSS voltage regulators. The HV regulator has another reference and the precision analog subsystem has a high-precision voltage reference which provides accurate voltage references for the ADCs. The ADCs may measure the SRSS and HV regulator references and all supply voltages ( $V_{DD}$ ,  $V_{DDA}$ ,  $V_{CCD}$ , and  $V_{SS}$  and  $V_{SSA}$ ) pins for diagnostic purposes. To allow better SNR and better absolute accuracy, an external reference or an external capacitor on the reference pin can improve accuracy by reducing noise

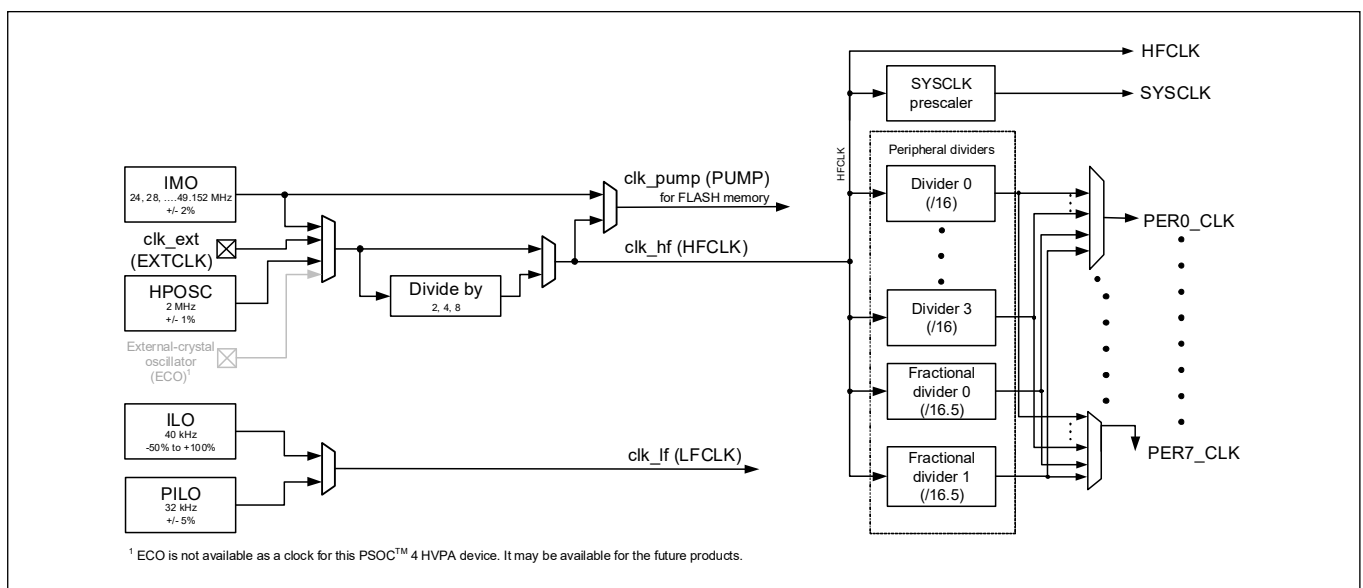
**Functional definition**

**1.2.3 Clock system**

The PSOC™ 4 HVPA clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching and for synchronizing clocks operating on different frequency domains to prevent meta-stable conditions. There are four oscillators implemented:

- One IMO for CPU and peripheral clock generation, which can be programmed for frequencies from 24 MHz to 48 MHz in 4 MHz steps. The 48 MHz setting can be boosted to 49.152 MHz
- One high-precision fixed frequency 2 MHz oscillator for precision timing (HPOSC)
- One low-power 40 kHz low-speed oscillator (ILO)
- One 32 kHz precision low-power oscillator (PILO) for wakeup timers and watchdog timers

There are also provisions for an external clock supplied by a GPIO pin. The ILO and PILO are permanently powered in all power modes.



**Figure 2 PSOC™ 4 HVPA clocking architecture**

Software can lock the IMO and ILO to the HPOSC to increase precision of those oscillators. Software can also lock any of the oscillators to external time references such as the external clock input or LIN bit rate. Software lock is accomplished with dedicated calibration counters that are available in the system resources subsystem. The oscillators are designed in such a way that trim changes do not glitch or disturb clock outputs.

- **IMO clock source:** The IMO is the primary source of internal clocking in the PSOC™ 4 HVPA. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The 48 MHz setting can be boosted to 49.152 MHz using "Special" calibration data stored in SFLASH. IMO tolerance with Infineon-provided calibration settings is ±2%. This clock runs in Active and Sleep modes
- **HPOSC clock source:** The HPOSC is a 2 MHz 1% precision oscillator, which is on in Active power and Sleep mode and off in Deep Sleep modes. During Active mode, high-frequency precision is required for accurate timing of ADC measurements to accurately determine charge and discharge energy (amp-hour) balance. This is achieved with the IMO slaved to the HPOSC with software tracking

## Functional definition

- **PILO clock source:** The precision internal low speed oscillator (PILO) is a very low power oscillator with a nominal frequency of 32 kHz. It is primarily used to generate clocks for peripherals in low power modes. The PILO is implemented with the focus on low-power in the Deep Sleep to keep supply current under 50  $\mu$ A. The accuracy over temperature and lifetime without periodic synchronization to the HPOSC is  $f_{PILO\_ACC1}$ . By means of regular synchronization with the HPOSC at least once per second, the same accuracy as in normal mode can be achieved ( $f_{PILO\_ACC2}$ ). This accuracy can be maintained at least 60s after the last synchronization calibration while temperature and voltage are stable. The PILO clocks low-power digital blocks including the watchdog timers and a lifetime counter. In Active mode, it can also generate strobes enabling TCPWM counters to be used with software for calibrating of the ILO
- **ILO clock source:** The ILO operates with no external components and outputs a stable clock at 40 kHz nominal. The ILO is relatively low power and low accuracy. The ILO is available in all power modes. The ILO is a relatively inaccurate ( $-50\%$  to  $+100\%$  over voltage and temperature) oscillator, which is used to generate low-frequency clocks
- **Lifetime counter:** A 32-bit lifetime counter with a prescaler ( $/2$  to  $/32$ ) is available and triggered from the PILO clock. This counter runs in all modes and can be reset by POR. With the prescaler, the net resolution of the counter becomes 37-bit causing an overflow every 50 days. The counter will continue counting upon overflow

### 1.2.4 Reset

The PSOC™ 4 HVPA can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

The following events cause resets:

- POR
- Brownout/overvoltage
- Watchdog reset
- Software reset
- External reset via XRES pin
- Fault system
- Protection violation

**Watchdog timers (WDT)** . The WDTs are used to automatically reset the device in the event of an unexpected firmware execution path. There are two WDTs, one that is available in the Deep Sleep mode, and a challenge-response WDT (CRWDT). The CRWDT includes a window watchdog function, generating timeout events if the CRWDT is serviced too soon, too late, or with the wrong software key. A register identifies the timeout cause. It generates a watchdog reset or interrupt if serviced too soon or too late. Service too soon potentially means an infinite loop including watchdog service is executing, while too late means the processor could be stuck and not processing properly. The challenge/response means the watchdog service routines must present specific data or “keys” in the order expected by the watchdog or a fault will occur. The fault will generate a watchdog reset or interrupt with the reset recorded in the Reset Cause register. The causes can be conditions such as watchdog too soon, watchdog late, or wrong key received. For more details on CRWDT, see the reference manual.

**Functional definition**

**1.3 Fixed function digital**

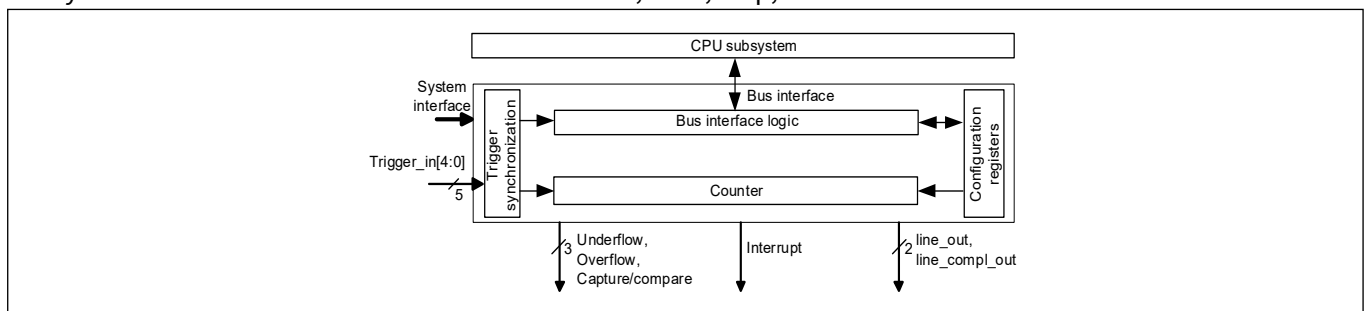
**1.3.1 Timer/counter/PWM (TCPWM) block**

The TCPWM in PSOC™ 4 HVPA implements 16-bit timer, counter, pulse width modulator (PWM), and quadrature decoder functionality. Four TCPWM blocks exist on PSOC™ 4 HVPA. The block can be used to measure the period and pulse width of an input signal (timer), count several events (counter), generate PWM signals, or decode quadrature signals.

The block provides true and complementary outputs with programmable offset between them to allow dead-band between outputs for driving complementary PWM loads. It also has a Kill input to force outputs to a predetermined state; this is used to inhibit outputs when faults are detected without requiring the need and delay of software intervention.

Features:

- The TCPWM block supports the following operational modes:
  - Timer, Counter, Capture, Quadrature decoding
  - Pulse width modulation (PWM) including Pseudo-random PWM and PWM with dead time
  - PWM uses a period counter and capture counter - complementary outputs are available
- Multiple counting modes - up, down, and up/down
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Generate triggers based on Compare, Overflow, or Underflow
- Supports interrupt on:
  - Terminal count: The final value in the counter register is reached (zero or period count)
  - Capture: When a capture event occurs (the counter value at the time of capture is saved)
  - Compare: When the count equals the compare value
  - Synchronized counters: The counters can reload, start, stop, and count at the same time



**Figure 3 TCPWM block diagram**

## Functional definition

### 1.4 Local interconnect network (LIN) block

PSOC™ 4 HVPA features a dedicated LIN communication block that supports autonomous transfer of the LIN frame to offloading the CPU. Some of the key features of this block include:

- Certified at C&S according to LIN 2.2A / ISO 17987 standards
- MXLIN has two channels: One is wired (through HSIOM) to the internal PHY and the other is available to GPIOs for an external PHY. They can both be used simultaneously, or they can be used in loop-back mode for testing
- LIN protocol support in hardware according to LIN 2.2A / ISO 17987 standard
  - Master and slave functionality
    - Master node
      - Autonomous header transmission and autonomous response transmission and reception
    - Slave node
      - Autonomous header reception and autonomous response transmission and reception
  - Message buffer for PID, data, and checksum fields
  - Classic and enhanced checksum
  - Timeout detection
  - Error detection
  - Test modes including hardware error injection
  - Baud rate detection
  - 16x bit time oversampling

### 1.5 Serial communication block (SCB)

SCB supports three serial interface protocols: SPI, UART, and I<sup>2</sup>C. Only one of the protocols is supported by an SCB at any given time. The PSOC™ 4 HVPA has one SCB.

This block supports the following features:

- UART with standard, SmartCard reader, Local Interconnect Network (LIN), and IrDA protocols
- UART with LIN slave functionality with LIN v1.3 and LIN v2.1/2.2/2.2A specification compliance
- SPI master and slave functionality with Motorola, TI, and NSC protocols
- I<sup>2</sup>C master and slave functionality
- EZ mode for SPI and I<sup>2</sup>C, which enables operation without CPU intervention
- Low-power (Deep Sleep) mode of operation for SPI and I<sup>2</sup>C protocols (using external clocking)

#### 1.5.1 UART mode

This is a full-feature UART operating at up to 1 Mbps supporting automotive single-wire interface (LIN), infra-red interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the PSOC™ 4 HVPA UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

The universal asynchronous receiver/transmitter (UART) protocol is an asynchronous serial interface protocol. UART communication is typically point-to-point.

The UART interface consists of two signals:

- TX: Transmitter output
- RX: Receiver input

The UART can also connect to the internal local interconnect network (LIN) PHY.

The UART mode has the following features:

- Asynchronous transmitter and receiver functionality
- Supported UART protocols include Standard UART, LIN, SmartCard (ISO7816) reader, and IrDA

## Functional definition

- LIN support includes
  - Break detection
  - Baud rate detection
  - Collision detection (detect a dominant bus state when transmitting a recessive bit)
- Multi-processor mode
- Data frame size programmable from 4 to 9 bits
- Programmable number of STOP bits, which can be set in terms of half-bit periods between 1 and 4
- Parity (odd and even parity)
- Interrupt or polling CPU interface
- Programmable oversampling

### 1.5.2 SPI mode

The serial peripheral interconnect (SPI) mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

The SPI protocol is a synchronous serial interface protocol. Devices operate in either master or slave mode. The master initiates the data transfer. The SCB supports single-master-multiple-slaves topology for SPI. Multiple slaves are supported with individual slave select lines.

You can use the SPI master mode when the PSOC™ must communicate with one or more SPI slave devices. The SPI slave mode can be used when the PSOC™ must communicate with an SPI master device.

The SPI mode has the following features:

- Supports master and slave functionality
- Supports three types of SPI protocols:
  - Motorola SPI - modes 0, 1, 2, and 3
  - Texas Instruments SPI, with coinciding and preceding data frame indicator for mode 1
  - National Semiconductor (MicroWire) SPI for mode 0
- Supports up to four slave select lines
- Data frame size programmable from 4 bits to 16 bits
- Interrupts or polling CPU interface
- Programmable oversampling
- Supports EZ mode of operation - EZSPI mode allows for operation without CPU intervention
- Supports externally clocked slave operation:
  - In this mode, the slave operates in Active, Sleep, and Deep Sleep system power modes

A standard SPI interface consists of four signals as follows. These signals connect to GPIO pins:

- **SCLK:** Serial clock (clock output from the master, input to the slave)
- **MOSI:** Master-out-slave-in (data output from the master, input to the slave)
- **MISO:** Master-in-slave-out (data input to the master, output from the slave)
- **Slave Select (SS):** Usually an active low signal (output from the master, input to the slave)

### 1.5.3 I<sup>2</sup>C mode

The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSOC™ 4 HVPA and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. The block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

## Functional definition

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

PSOC™ 4 HVPA is not completely compliant with the I<sup>2</sup>C spec in the following respect:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system

The I<sup>2</sup>C mode has the following features:

- Master, slave, and master/slave mode
- Slow-mode (50 kbps), standard-mode (100 kbps), fast-mode (400 kbps), and fast-mode plus (1000 kbps) data-rates
- 7- or 10-bit slave addressing (10-bit addressing requires firmware support)
- Clock stretching and collision detection
- Programmable oversampling of I<sup>2</sup>C clock signal (SCL)
- Error reduction using a digital filter on the input path of the I<sup>2</sup>C data signal (SDA)
- Glitch-free signal transmission with an analog glitch filter
- Interrupt or polling CPU interface

### 1.5.4 LIN Slave mode

The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN Slave is compliant with LIN v1.3, v2.1/2.2, ISO 17987-6, and SAE J2602-2 specification standards. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40 meter cable length.

## 1.6 GPIO

This section describes the PSOC™ 4 HVPA I/O system. The GPIO pins are grouped into ports; a port can have a maximum of eight GPIOs. The PSOC™ 4 HVPA has 9 GPIOs.

The GPIOs have these features:

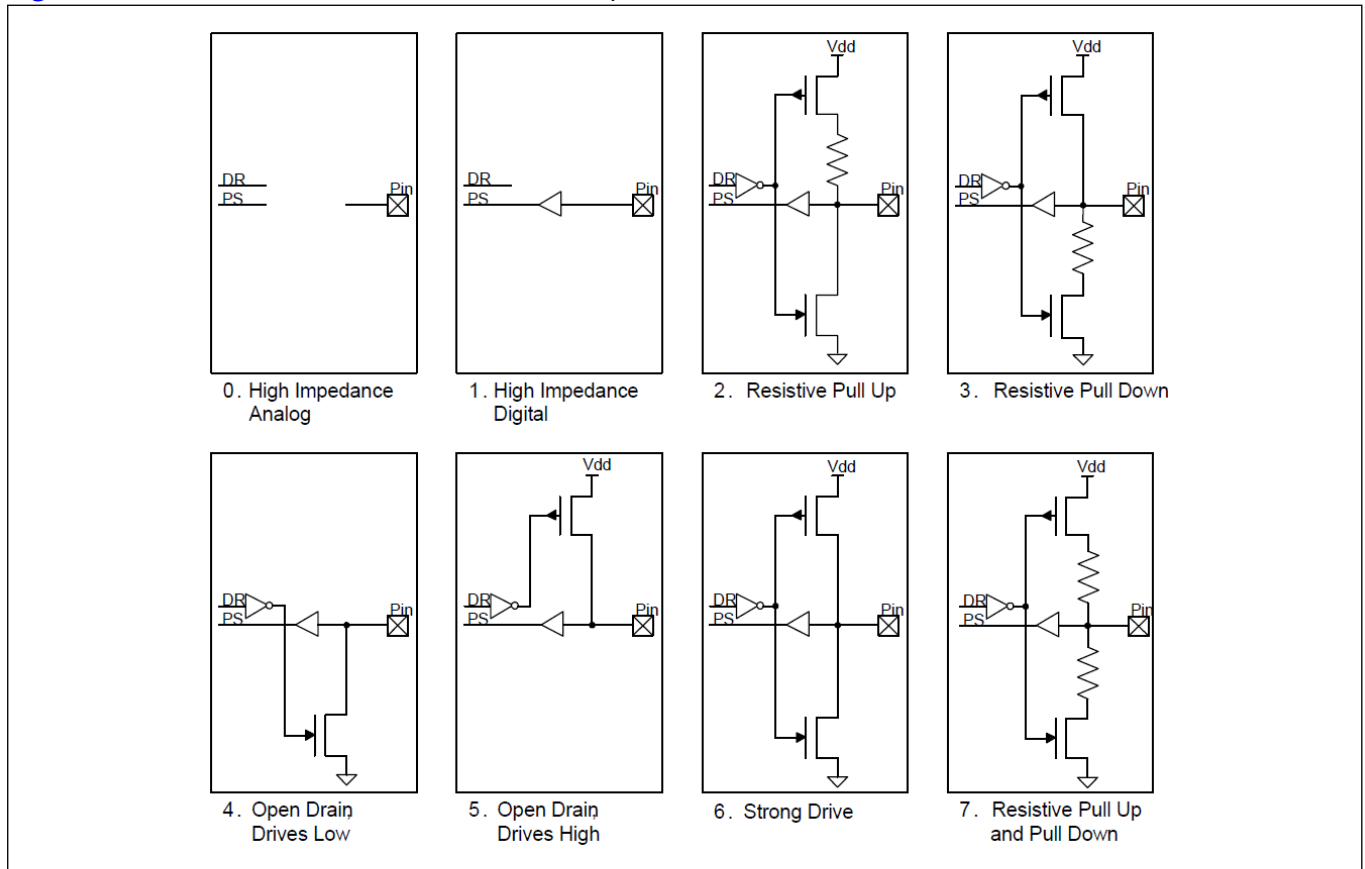
- Output drive modes include push-pull (strong or weak), open drain/source, high-z, and pull-up/pull-down
- Selectable CMOS and low-voltage LVTTTL input buffer mode
- Edge-triggered interrupts on rising edge, falling edge, or on both the edges, on pin basis
- Individual control of input and output disables
- Hold mode for latching previous state (for retaining I/O state in Deep Sleep)
- Selectable slew rates allowing dV/dt control to assist with noise control to improve EMI

All GPIOs can be used to receive analog input signals for the ADCs.

During power-on and reset, GPIO outputs are disabled to prevent conflict with externally applied signals and prevent crowbar and/or excessive turn-on current. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. An interconnect network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin.

**Functional definition**

**Figure 4** illustrates the various available GPIO output drive modes.



**Figure 4 GPIO output drive modes**

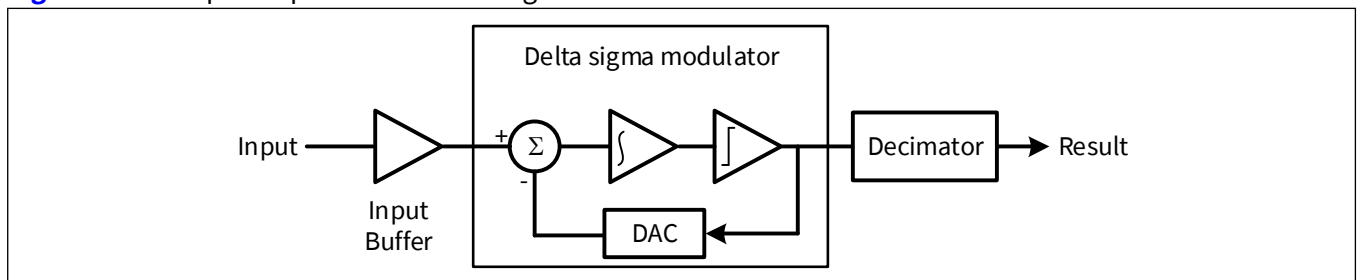
Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The PSOC™ 4 HSPA HV  $V_{DD}$  regulator has enough capacity to drive internal loads and external loads up to 10 mA. DC GPIO loads are considered external loads. The combined DC GPIO and external load current must not exceed the available 10 mA. Care must be taken when driving DC loads, such as LEDs, to make sure the total current being sourced from the GPIOs does not exceed this limit.

**1.7 Precision analog channel subsystem (PACSS)**

The PSOC™ 4 HSPA Precision Analog Channel Subsystem (PACSS) is a high-performance data acquisition system consisting of two delta-sigma analog-to-digital converters (ADCs) and support circuitry. The two ADCs can quickly switch between input sources to create a third “virtual” ADC. The PACSS includes an analog input multiplexer, input buffer amplifiers, delta-sigma modulators, decimators, and digital signal processing channels. There is also a precision voltage reference, current references, and temperature sensors.

**Figure 5** is a simplified picture of a delta sigma ADC.



**Figure 5 PACSS overview**

---

## Functional definition

The delta-sigma ADC works by using a modulator, taking the difference between input and feedback signals (delta) and accumulating that difference (sigma) to produce a digital output. The digital stream goes to a decimator which converts the fast-oversampled bit stream into slower high-resolution results.

The PSOC™ 4 HVPA PACSS has two delta-sigma analog-to-digital converters (ADCs) to perform 16-bit measurements at a sample rate of up to 48 ksp/s for continuous measurements. Higher resolution can be achieved at slower sample rates by accumulating more modulator results in the decimator.

The PSOC™ 4 HVPA PACSS analog multiplexer selects between the differential input voltages including two HV voltage dividers, GPIO pads, internal temperature sensors, an external NTC temperature sensor, and diagnostic voltages. All analog signals can be supplied to either of the analog ADCs, which improves diagnostics since both ADCs can measure and compare the same signals.

The analog portion of the ADCs consists of a programmable gain amplifier, an anti-alias filter, a buffer, and a multi-level delta-sigma modulator (DSM). The output of the modulator goes to the digital portion of the channel and features a scaler, decimator, FIR filter, adder/multiplier to reduce gain and offset errors, averaging, and threshold comparisons.

There are four digital channels, which process outputs from either of the two analog DSMs. Two channels are with the FIR filter, and the other two are without the FIR Filter. The channels are typically used for current, voltage, temperature, and diagnostic measurements although they can be associated with any inputs (for example,  $V_{SENSE}$  can be measured by one channel while  $V_{DIAG}$  is measured by another).

The current channel has an automatic gain control, which allows a large dynamic range that enables measuring large starting currents or small battery-off currents. The gain of the current channel ranges from 1 to 512. Automatic gain can be disabled and set to a fixed value. A scaler between the modulator and decimator adjusts the weight of modulator data based on gain so the input to the LSB of the data going into the decimator is always 0.715 mA.

The gain of other channels is static instead of dynamic. Static gain is typically set to 1 but any value from 1 to 512 in powers of 2 can be used. The HV input channels have resistor voltage dividers, which attenuate the input voltage. The nominal divider ratio is 24x (28.8 V full-scale) with an optional value of 16x (19.2 V full scale).

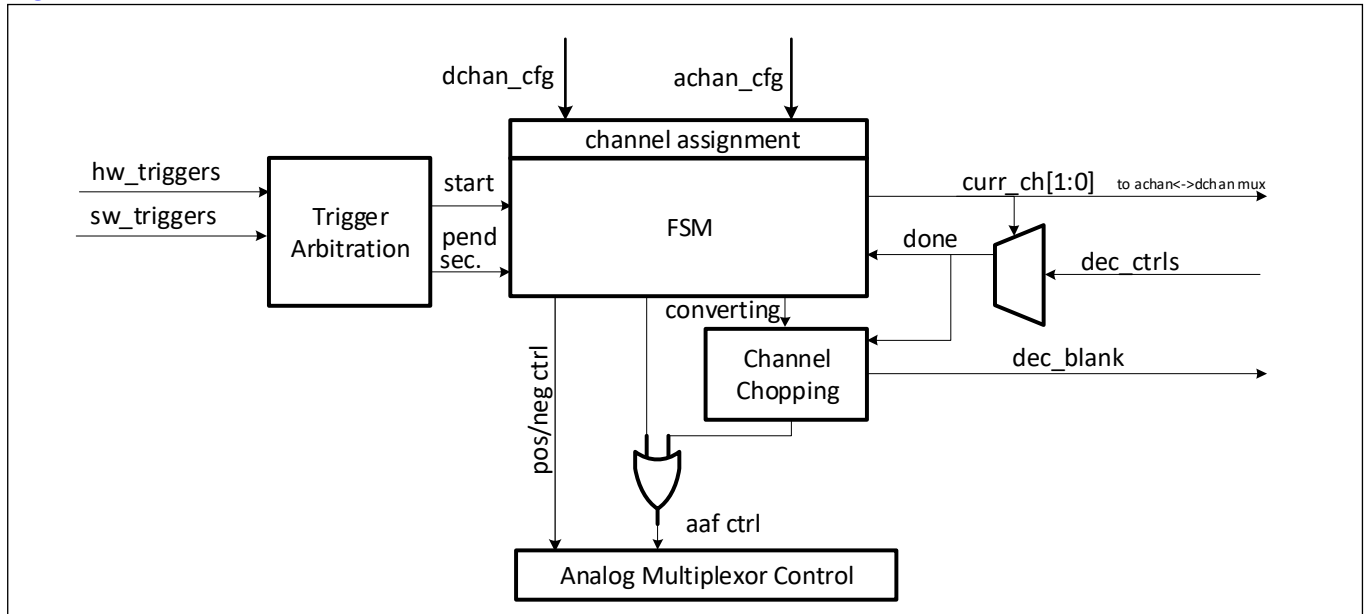
Chopping is used to minimize offset voltage error. Channel chopping is implemented to further reduce offset error. Channel chopping is making a measurement followed by a second measurement with inputs swapped and result multiplied by -1. The two samples are averaged, which removes any residual channel offset.

ADC measurements can be triggered by software or hardware. Hardware triggers can be generated by timers or GPIO inputs. The ADCs can be triggered independently or simultaneously. A SYNC function can be implemented to allow multiple PSOC™ 4 HVPA chips to perform simultaneous measurements. One device uses a GPIO output to simultaneously trigger the on-chip ADC measurements while signaling other PSOC™ 4 HVPA chips to trigger measurements. The SYNC signal can be set using either a timer or software to write to the GPIO.

Functional definition

### 1.7.1 PACSS sequencer and timing

The PACSS sequencer generates control signals for performing analog-to-digital conversion, as shown in **Figure 6**.



**Figure 6** PACSS sequencer

A peripheral clock from the system-wide resource clock system is used for sequencer timing. The same clock is used for all ADC channels. The clock goes to the delta-sigma modulator (DSM) controller, which generate timing strobes with a finite state machine which are used by other sections of the sequencer. The DSM controller also includes control and status registers which are accessed from the  $\mu$ C and DMA channels using the AHB bus. The controller also generates interrupt and DMA requests.

ADC conversions are initiated by triggers from generated by other sources. Those sources include timers (TCPWM), input signals from GPIOs, software requests, and end-of-conversion commands from an active ADC. Triggers can start one or two ADCs - when triggering two ADCs, both ADCs start together. An arbiter is used to prioritize ADC conversion requests and start conversions when the ADCs become available.

The arbiter also controls the analog multiplex or control block, which selects the analog input associated with the trigger. The analog multiplex or control sends the appropriate select signals to the analog multiplex or to connect analog inputs to the ADCs.

The two ADC channels have a channel controller which generates timing for that channel. There are separate controls for the analog and digital portion of the channels. The analog timing signals control the delta-sigma modulator and chopping switches, while the digital timing signals clock data path registers including the decimator, finite impulse response filter, and comparators and accumulators.

At the beginning of the conversion sequence, a four-cycle reset of the modulator clears state from previous conversions (the integrators in the modulator are initialized by this reset). The length of a conversion cycle requires the same number of clocks as the OSR setting. After the modulator is reset, the decimation filter needs to stabilize before output data is valid. For continuous measurements, the decimator needs to be one order higher than the modulator to maintain stability over time, and therefore a Sinc3 decimator (one order higher than the third order modulator) is used. This means that the decimator output is valid after the fourth conversion and then every conversion thereafter. For example, an OSR of 64 with a 3.072 MHz clock requires  $\sim 1.3 \mu$ s for reset,  $\sim 20.8 \mu$ s per conversion (or 48 kps) in continuous mode, and  $86.6 \mu$ s for the initial result.

For incremental (one-shot) conversions, the decimator can be the same order as the modulator, so a Sinc3 is used which reduces latency to three conversion cycles. Using the same conditions as the example above, the result requires  $64 \mu$ s.

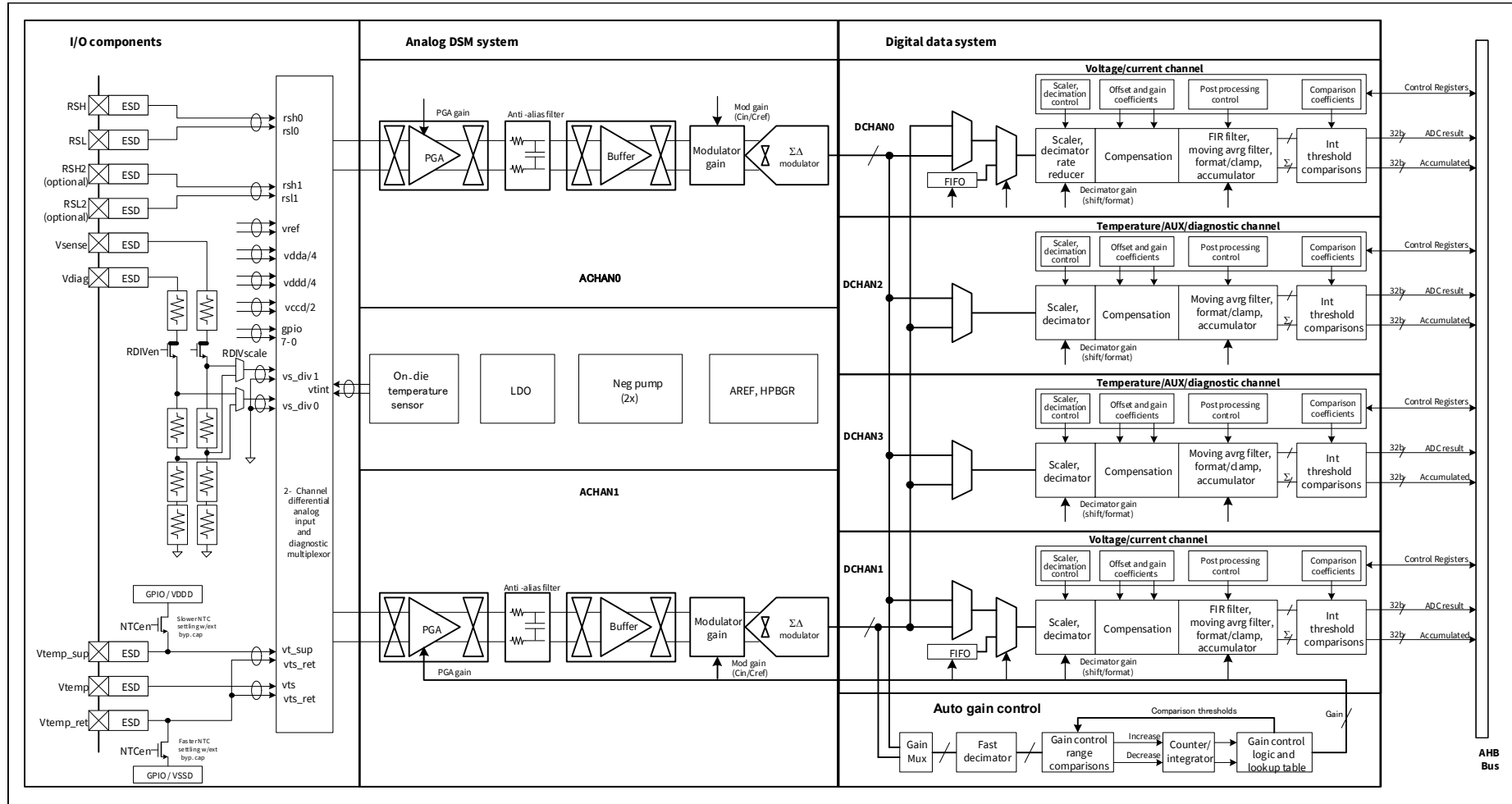
## Functional definition

The incremental measurement mode can be used to measure several different voltage sources each conversion sequence while maintaining an aggregate sample rate. The sample rate can be adjusted by changing the OSR setting. With an OSR of 64 and a 3.072 MHz clock, the incremental sample rate is 16 ksps. If this mode is used to measure continuously, measure two different sources, the sample rate for each signal is half of the single source rate.

PSOC™ 4 HVPA takes advantage of the incremental mode to create three channels with only two analog front-ends.

Since lead-acid battery sensing applications only need 8 ksps on the main voltage and current channels, the third channel can use either one of the analog front-ends, which is not being used between V/I measurements. This channel can be used for temperature measurement, to measure other signals, or for diagnostics. Diagnostics can include measuring power supplies, references, and even the same signal measured by the other channel. The main advantage of using shared analog front-ends is power reduction.

# 1.8 PACSS measurement/acquisition system



**Figure 7 PACSS measurement/acquisition**

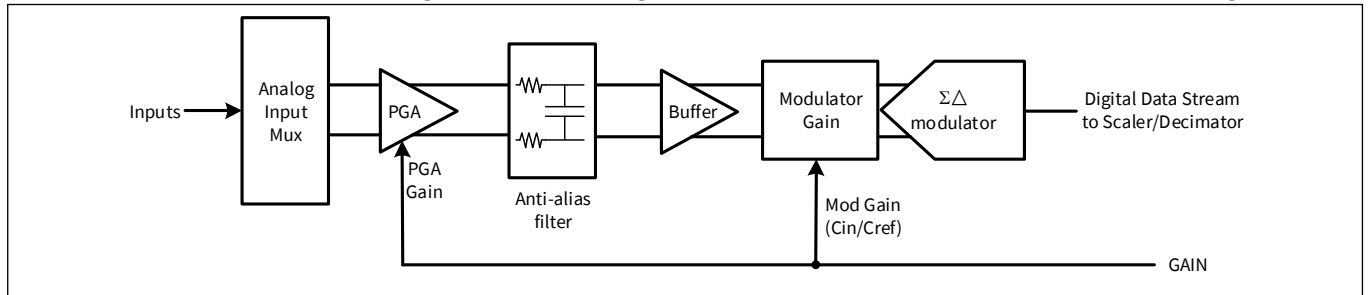
An analog multiplexer connects input signals to the two physical analog DSM channels. Several input sources are available including signals from I/O input. The analog channels have choppers, gain, filters, and DSM modulators. Several integrated multiplexers facilitate diagnostics and channel switching without disturbing filters. The digital section has four channels with one dedicated channel for each analog channel and two auxiliary channels, which can use either analog channel. The following sections provide more details about these blocks.



**Functional definition**

**1.8.1 Analog DSM channel**

**Figure 8** is a simplified diagram of an analog delta-sigma modulator (DSM) channel and part of the digital channel. For better clarity, the diagram omits analog multiplexers to bypass and swap blocks for diagnostics.

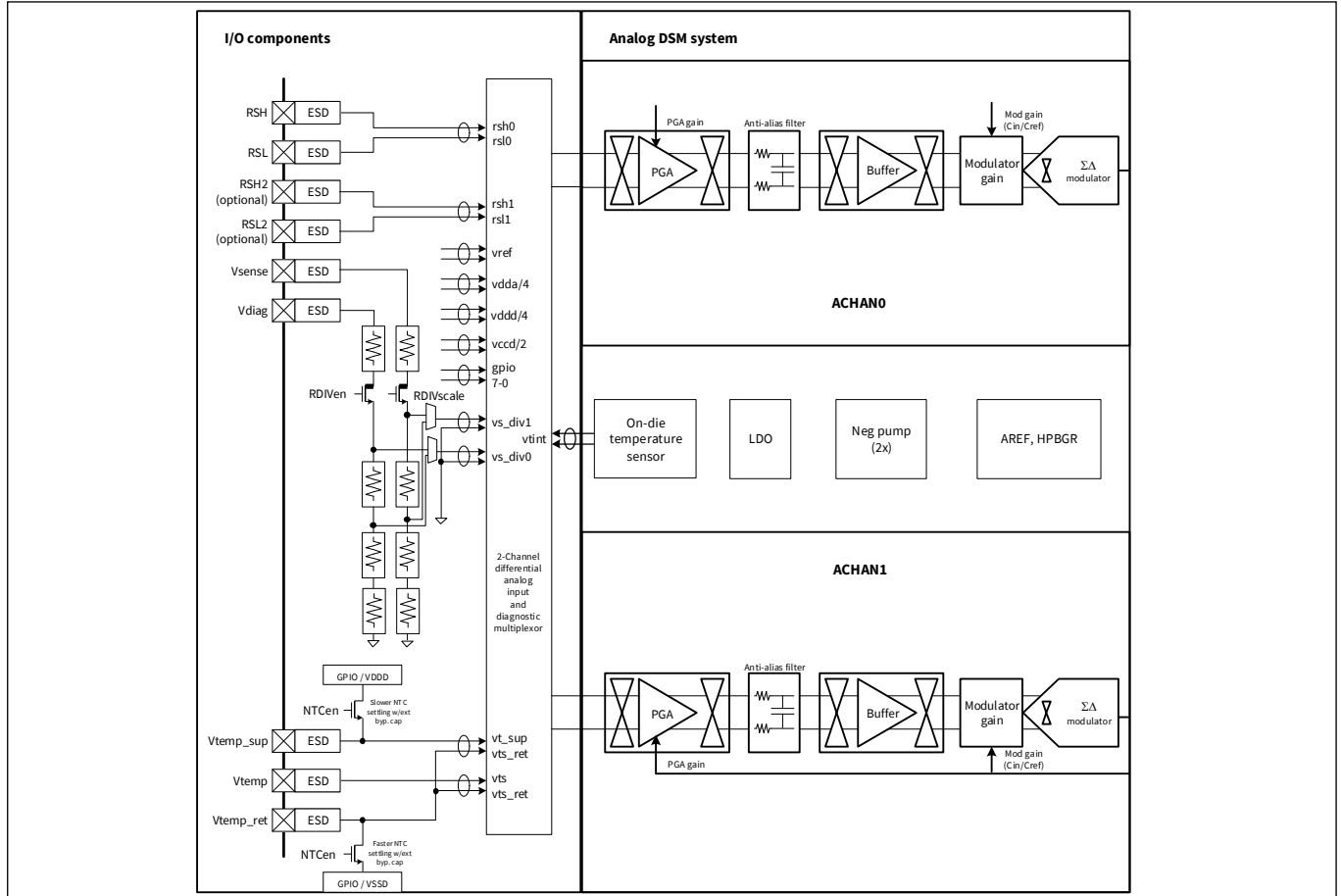


**Figure 8 Analog DSM channel**

The analog DSM channel receives a differential signal selected by an analog multiplexer. This differential signal is received by a programmable gain amplifier (PGA). The output of the PGA feeds a low-pass anti-alias filter (AAF) with a bandwidth of ~30 kHz. A buffer amplifier drives the DSM modulator - this amplifier has high bandwidth to settle the modulator capacitors to better than 16 bits each time they are settled. The modulator uses capacitor dividers to set gain - the modulator disturbs its input each time the input is sampled - the inputs need to settle before the next sample or errors result. The modulator is a third order with switched capacitor amplifier circuits. The modulator produces a multi-level digital bitstream sent to the digital channel.

**1.8.2 Analog DSM system**

**Figure 9** shows the analog DSM system.



**Figure 9 Analog DSM system**

**Functional definition**

The DSM sequencer previously described controls conversions. The sequencer selects the analog input signal by controlling the analog mux, connecting the input to an analog DSM channel. Signals from GPIOs, on-chip power supplies and grounds, the high-voltage input voltage divider, and on-chip sensors and references can be selected.

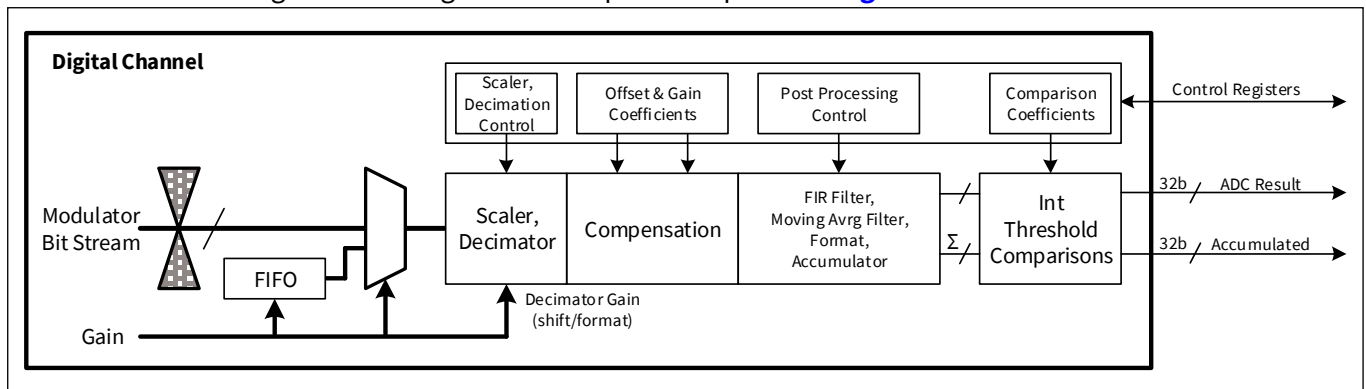
GPIOs not directly connected to the analog multiplexer can use an analog input bus called the analog multiplex bus (AMUXBUS). The AMUXBUS has two signals (AMUXBUSA and AMUXBUSB), which can connect GPIOs to ADC using software controlled analog switches inside each I/O.

The analog DSM channel includes choppers and multiplexers in addition to the PGA, anti-alias filter, buffer amplifier, and DSM modulator. The choppers minimize offset error while the multiplexers assist input signal switching and diagnosis. To alternately measure two signals with one channel, the anti-alias filter can be bypassed since the AAF needs about 64  $\mu$ s to settle to 16 bits before conversions can start - the measurement sample rate needs to slow to 4 ksp/s if the AAF is not bypassed. The other paths allow the input, PGA, and AAF signals to be swapped to the other channel for diagnostics.

This section also includes a precision reference system (voltage and current) and temperature sensor.

**1.8.3 Digital channel data path**

The digital data channel converts the modulator bit-stream output to parallel data and includes scaling, filtering and compensation. It also compares ADC values with thresholds to generate interrupts when thresholds are exceeded. A block diagram of the digital channel path is depicted in **Figure 10**.



**Figure 10 Digital channel data path**

The modulator bit stream first goes to a channel chopper, which can multiply the bit stream by +1 or -1 (corresponding with a chopper that swaps inputs in the analog signal path). The voltage channel uses programmable fixed gain while the current channel can use either fixed or automatic gain.

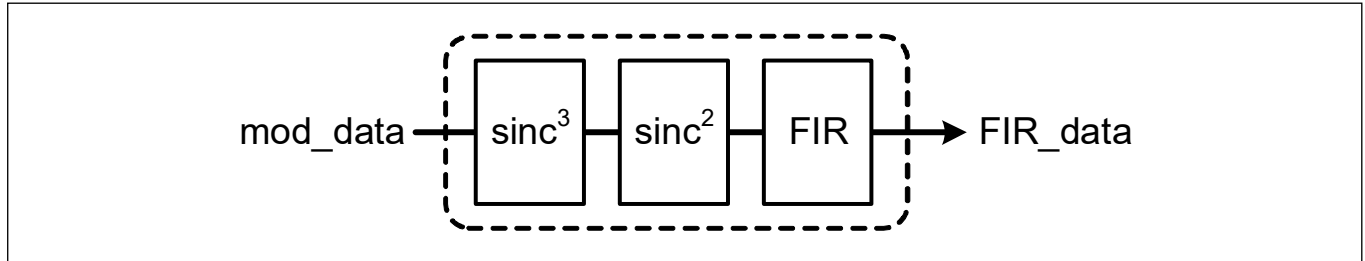
A scaler is used so that the LSB of the ADC can have the same weight regardless of gain. The LSB is established by the ADC resolution at maximum gain – for the current channel, the LSB is 0.715 mA with a gain of 512. The scaler multiplies the output of the modulator by 512/Gain to normalize results and maintain 0.715 mA for the LSB regardless of gain setting. To multiply by 2, the scaler shifts results up one bit. To cover a gain range of 1 to 512 means results can be shifted up to 9 bits.

The output of the decimator goes to a compensation block, which multiplies results for gain adjustment and adds constants for offset correction. A 16-stage finite impulse filter (FIR) with programmable coefficients follows the compensation block. Results are then normalized to remove unused bits and averaging, accumulation, and threshold detection can be performed. Threshold comparison uses a window comparator, which can be programmed for high and low thresholds which trigger interrupts.

Channel control registers are programmed by the CPU using the AHB bus. Results can be transferred by DMA or CPU. A trigger can initiate a DMA transfer and an interrupt can notify the availability of the CPU data. These operations can be performed in parallel. The CPU can also poll for end-of-conversion to determine if data is available.

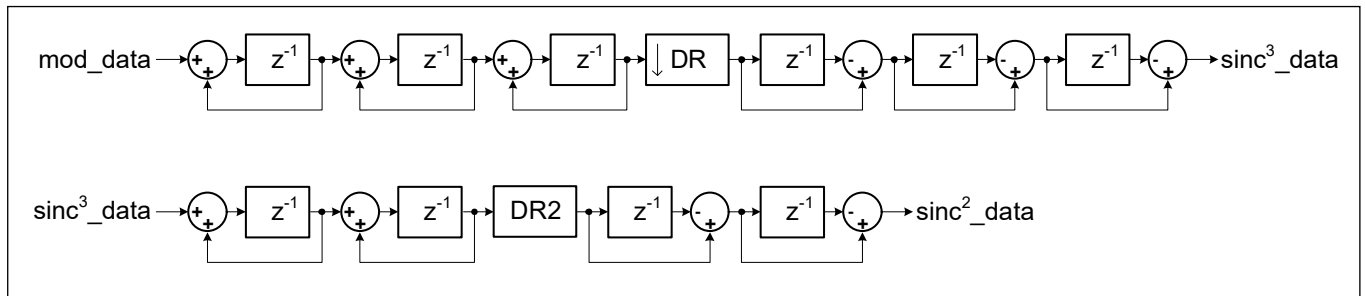
Functional definition

The ADC Channel digital back end has two decimators and a FIR filter. Over sampling rate (DR and DR2) of decimators is programmable. FIR filter coefficients and number of taps is also programmable. A high-level block diagram of the digital backend is shown in **Figure 11**.



**Figure 11 High level block diagram of digital back end**

Decimator, also known as CIC filters are used to filter quantization noise of the Delta-Sigma ADC. **Figure 12** shows the block diagram of sinc3 and sinc2 decimators.



**Figure 12 Block diagram of sinc3 and sinc2 decimators**

The z-domain transfer function of an Lth-order CIC filter is typically presented as:

Eq. 1

$$H(z) = \left[ \frac{1 - z^{-DR}}{1 - z^{-1}} \right]^L$$

where,

- L is the filter order
- DR is the Over sampling rate

The sinc response is equal to zero at integer multiples of the data rate. This means that the magnitude response will show notches at these frequencies. Therefore:

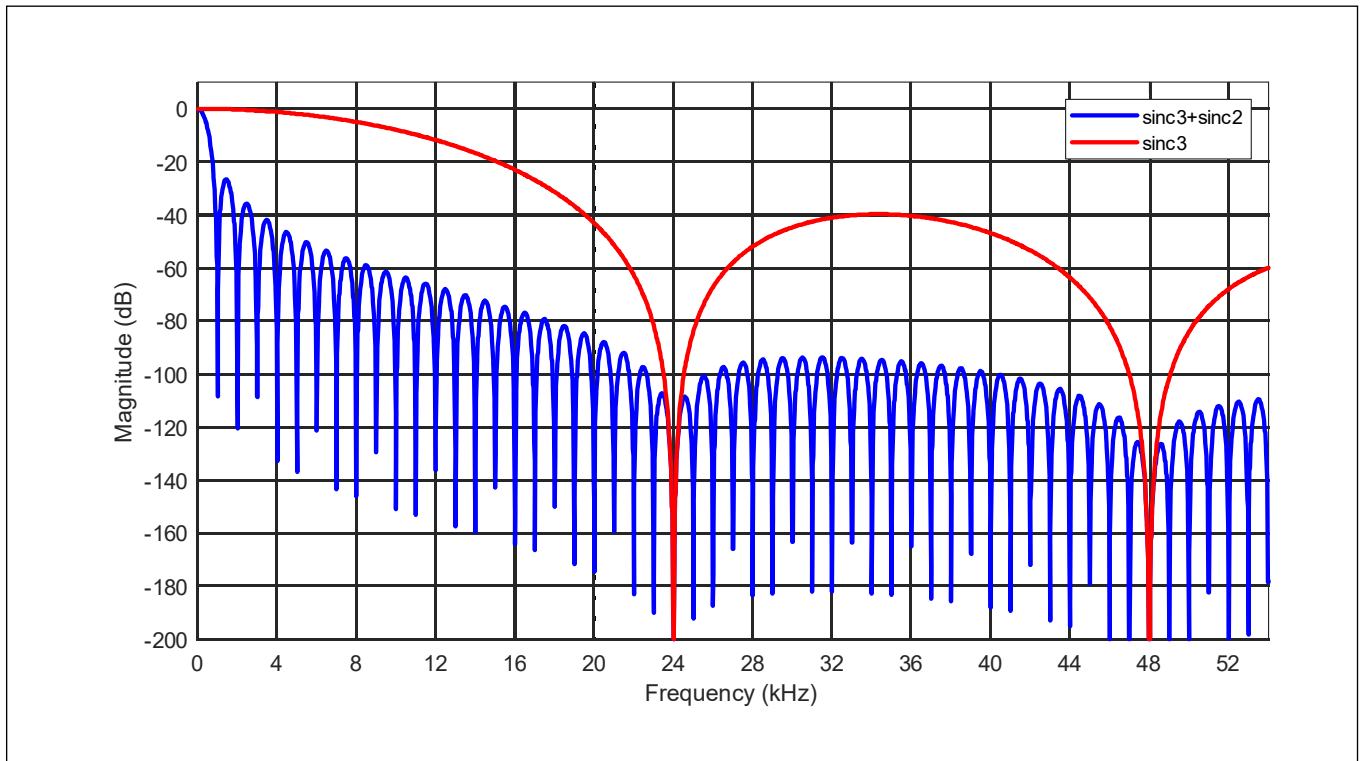
- sinc3 has notches at  $N \cdot F_s / DR$  [notches at 24 kHz, 48 kHz, ...]
- sinc2 has notches at  $N \cdot F_s / (DR \cdot DR2)$  [notches at 1 kHz, 2 kHz, 3 kHz, ...]

where,

- N is integer number
- DR is the Over sampling rate of sinc3 decimator
- DR2 is the Over sampling rate of sinc2 decimator
- $F_s$  is the ADC sample clock rate

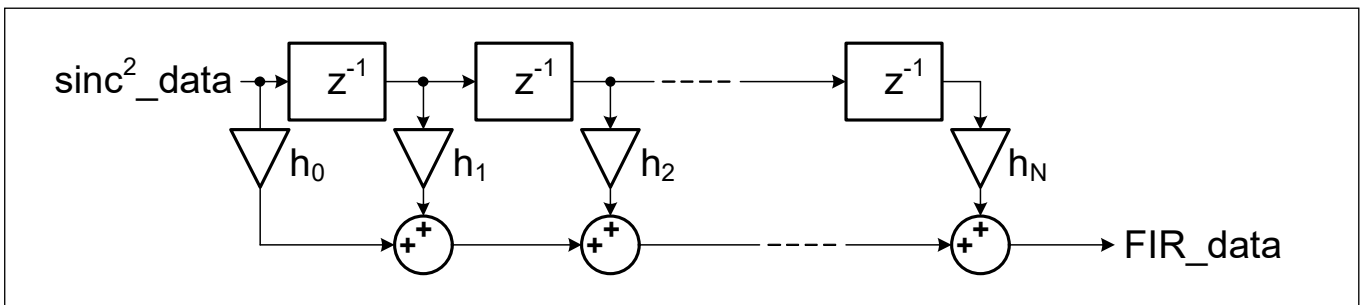
**Functional definition**

Example response for DR = 128, DR2 = 24 case is shown in **Figure 13**. ADC sample clock rate is  $F_s = 3.072$  MHz. Data rate of this configuration is 1 kpsps.



**Figure 13** **sinc3 and sinc3+sinc2 output comparison**

In addition, an FIR filter can be used to further reduce bandwidth. The FIR filter is fully programmable and has 64 taps (see **Figure 14**).

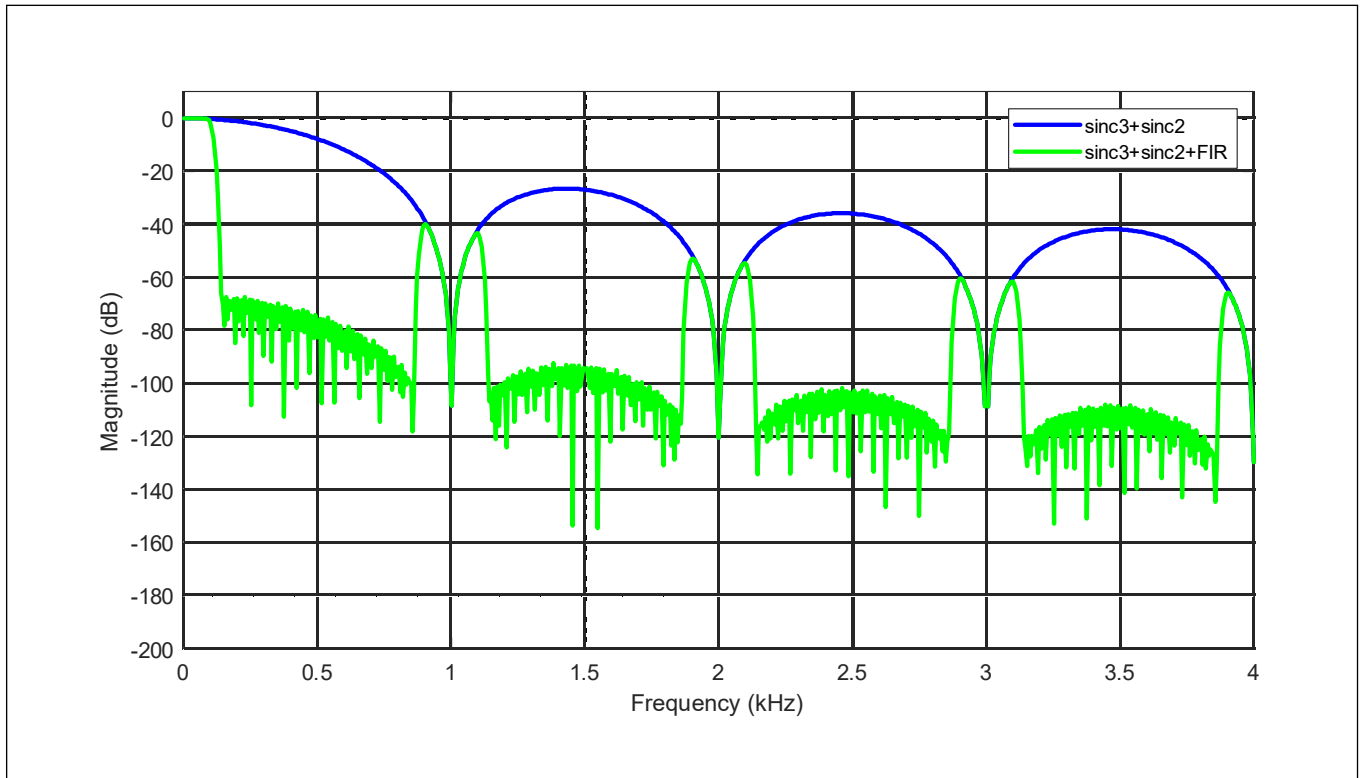


**Figure 14** **General structure of the FIR filter**

**Functional definition**

**Figure 15** shows the combined output with 16-tap FIR filter. DR = 128, DR2 = 24, ADC sample clock rate is  $F_s = 3.072$  MHz. Coefficients used for the FIR filter are:

[-0.00414 -0.01741 -0.02674 -0.0151 0.02896 0.1049 0.18756 0.24197  
 0.24197 0.18756 0.1049 0.02896 -0.0151 -0.02674 -0.01741 -0.00414]



**Figure 15 Combined output of the Back End**

### 1.8.4 Digital data system

**Figure 16** shows the complete digital data system. There are four data channels, of which two are dedicated channels associated with their respective analog channels while the third and fourth can receive data from either analog channel. This allows the analog channel to feed alternate analog measurements from two different signal sources to the two data channels with appropriate configuration for those measurements. It also facilitates diagnosis by allowing either analog channel to be used to measure the same signals.

Parameters for the alternate digital channel, especially compensation values, must be programmed to appropriate values corresponding to the analog channel being measured. The AGC function is described in the next section.

Functional definition

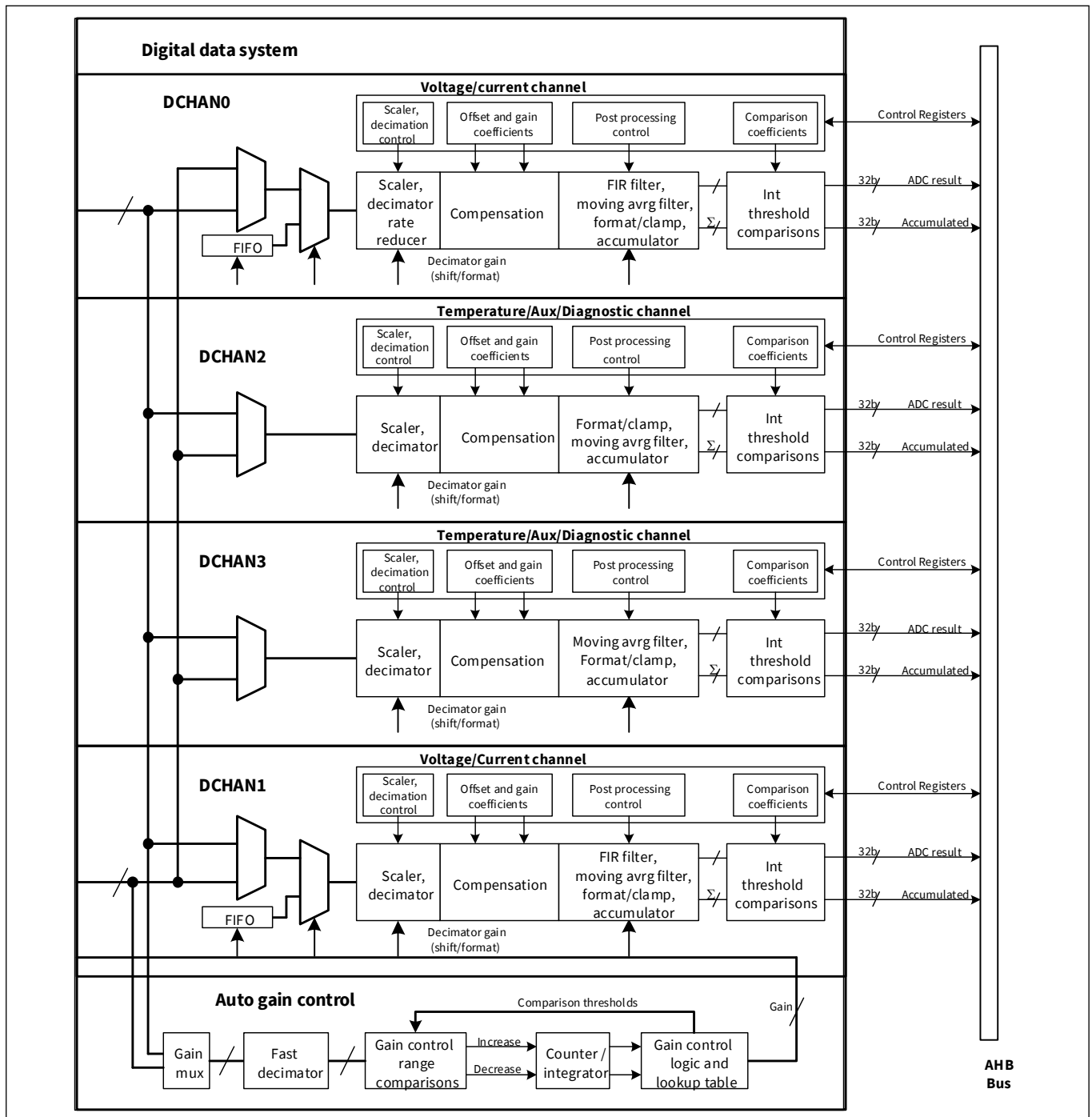
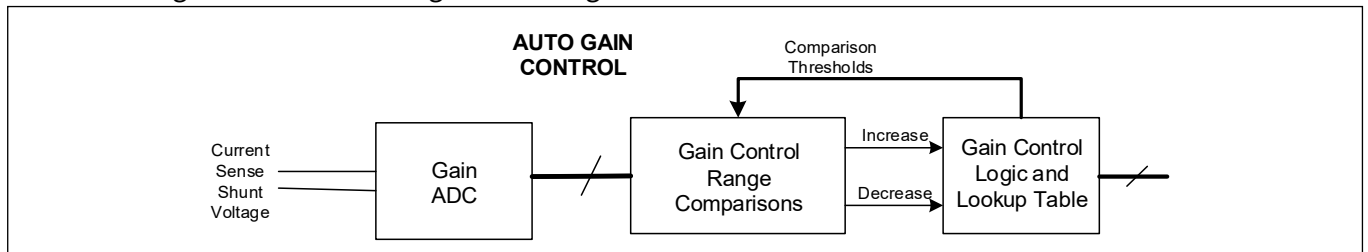


Figure 16 Digital channel data system

Functional definition

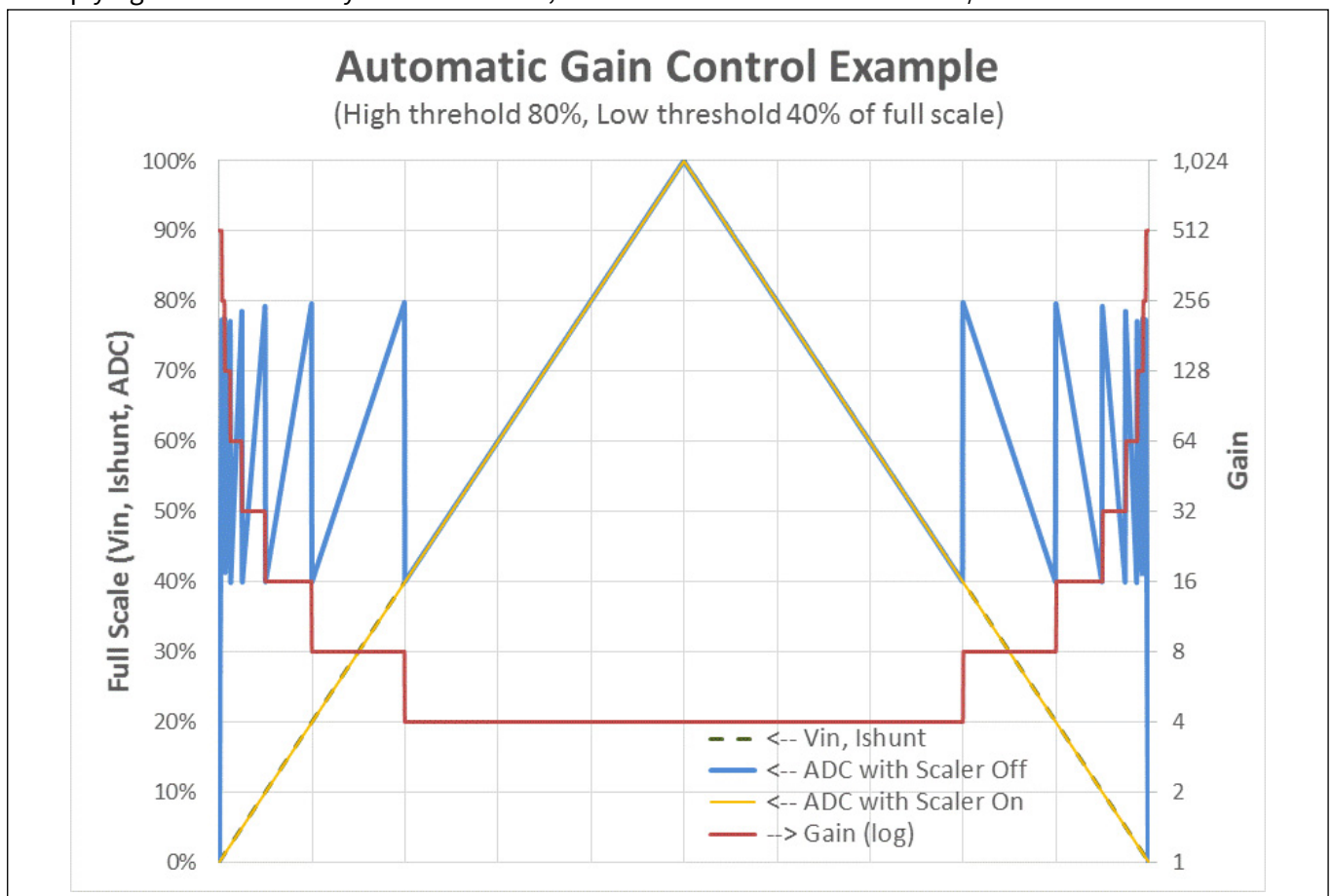
### 1.8.5 Current channel automatic gain control

The current channel includes an automatic gain control (AGC) mechanism shown in **Figure 17**. This functions by measuring the analog channel input voltage with an ADC and increasing or decreasing gain when programmable thresholds are reached. The output of the gain control comparators is used by a look-up table to set scaler, PGA, and modulator gain settings. To minimize input referred noise, it is advisable to configure the gain table to increase PGA gain before increasing modulator gain.



**Figure 17** Auto gain control

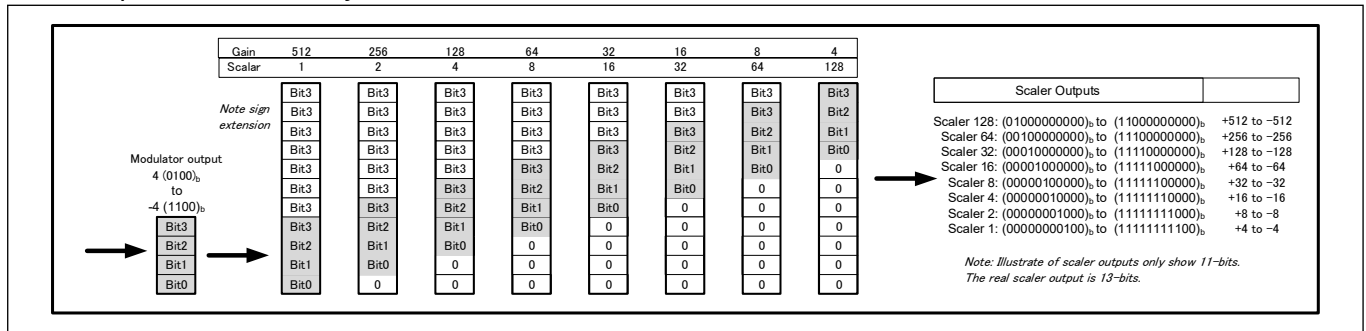
**Figure 18** is an example of the AGC with current going from 0% to 100% of full scale (3000A). **Figure 19** shows full-scale amperes, resolution, and scaler values for gains from 4-512. As described in the previous sections, the scaler is used to normalize results so the LSB always has the same weight (0.715 mA) which is accomplished by multiplying the modulator by the scaler value; the scaler value is the same as  $512/\text{Gain}$ .



**Figure 18** Automatic gain control example

**Functional definition**

**Figure 19** illustrates scaler operation. In this example, a 4-bit modulator input from ±4 is scaled by 1 to 128. For example, when scaled by 128, ±4 becomes ±4\*128 (= ±512).



**Figure 19 Scaler operation**

The AGC can be configured to increase or decrease gain by factors of 2 or more. Large steps can track large current changes faster by reducing the number of gain changes needed for tracking.

**1.8.6 Temperature sensor**

Temperature measurements are performed by measuring the difference in base-emitter voltage (VBE) of PNP bipolar transistors at two different current densities - temperature is directly proportional to the voltage difference. The principle of operation is:

- VBE = nkT/q\*ln(I/I<sub>S</sub>); (1) VBE voltage at a given current and temperature
- dVBE = nkT/q\*ln(M\*I/I<sub>S</sub>) - nkT/q\*ln(I/I<sub>S</sub>) = nkT\*ln(M); (2) Difference in VBE at two different current densities (current ratio "M")
- T(°K) = dVBE\*q/(nk\*ln(M)) (3) Temperature as a function of dVBE

Where VBE is the base-emitter diode voltage, dVBE is the difference in diode voltage at two different current densities (the ratio of current density is M), n is the base-emitter diode ideality factor, k is Boltzman's constant, q is the charge of an electron, I is the diode current, and I<sub>S</sub> is the diode saturation current.

Note that I<sub>S</sub> cancels as does the magnitude of I; n, k, and ln(M) are constants, which produce a nominal voltage of 179 μV/°K with M=8.

Temperature is calculated from dVBE using a polynomial with factory-supplied calibration coefficients to compensate for errors and drift in n and M, which can vary slightly with temperature and temperature-related package stress. Boltzman constant k and electron charge q are physical constants which do not drift.

Two independent current reference sources are available to diagnose current reference malfunctions by comparing results using the two independent references. Similar redundancy is provided by changing transistor current density either by changing the magnitude of the current source or the size of the transistor.

Temperature measurement is usually performed with an interrupt routine, which can either be software or timer triggered.

**1.9 High-voltage subsystem**

The PSOC™ 4 HVPA high-voltage subsystem includes the following functions:

- An AHB bus interface and control/status registers
- The V<sub>BAT</sub> to V<sub>DD</sub>/V<sub>D</sub>A HV regulator (3.6 to 28 V input, 3.3 V nominal outputs)
- An input attenuator/voltage divider for V<sub>SENSE</sub> and V<sub>DIAG</sub> ADC inputs
- A LIN transceiver (physical interface or PHY)

**Functional definition**

**1.9.1 AHB interface**

The AHB includes the control and status registers needed for the HV subsystem.

**1.9.1.1 HV regulator**

The high-voltage regulator is always on, supplied by VBAT, and provides V<sub>DDP</sub> and V<sub>DDA</sub>. It supplies a nominal output voltage of 3.3 V but may drop as low as 2.7 V when V<sub>BAT</sub> drops below 4 V.

**1.9.1.2 HV input attenuator**

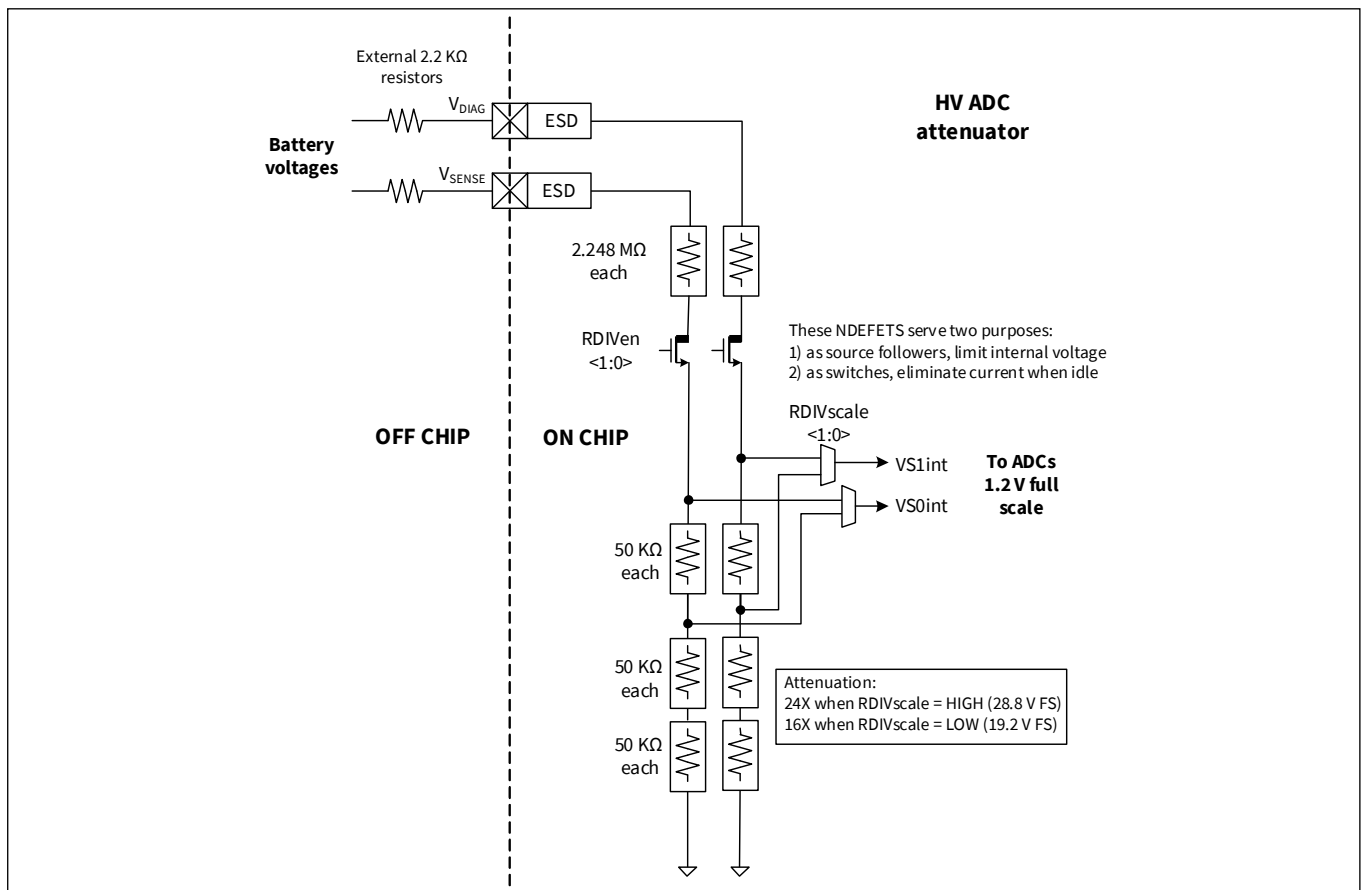
The HV input attenuator is a voltage divider used on the V<sub>SENSE</sub> and V<sub>DIAG</sub> to scale battery voltage to levels compatible with the ADCs, so battery voltages can be measured.

In typical lead-acid battery sensing applications, the V<sub>SENSE</sub> input is normally connected directly to the battery with a series 2.2 kΩ resistors to measure battery voltage. V<sub>DIAG</sub> can be used to measure voltage at other locations such as the ECU or other loads where monitoring is desired. It is sometimes used to measure ignition switch voltages such as the run bus (KL15), the start bus (KL50), or the always-on battery bus (KL-30).

The external 2.2 kΩ resistors in series with voltage sources limit current during ESD and transient voltage events. Since the nominal resistance of the on-chip voltage divider is about 2.4 MΩ, the accuracy of the external resistors is not critical since their contribution is only 0.1% of the total divider.

The voltage divider slightly loads the source being measured with the 2.4 MΩ resistor. A small current from source to ground flows through the divider (for example, 6 μA when measuring a 12 V source). The voltage divider can be switched off using the RDIVen control bits.

The RDIVscale control bits select whether the voltage divider input-to-output ratio is 24 or 16. Since the ADC full scale input voltage is 1.2 V, the 24X ratio corresponds to 28.8 V full scale and 16X ratio corresponds to 19.2 V full scale. Voltage divider matching error results in a gain error, which can be corrected with gain correction in the ADC.



**Figure 20 HV DC attenuator**

**Functional definition**

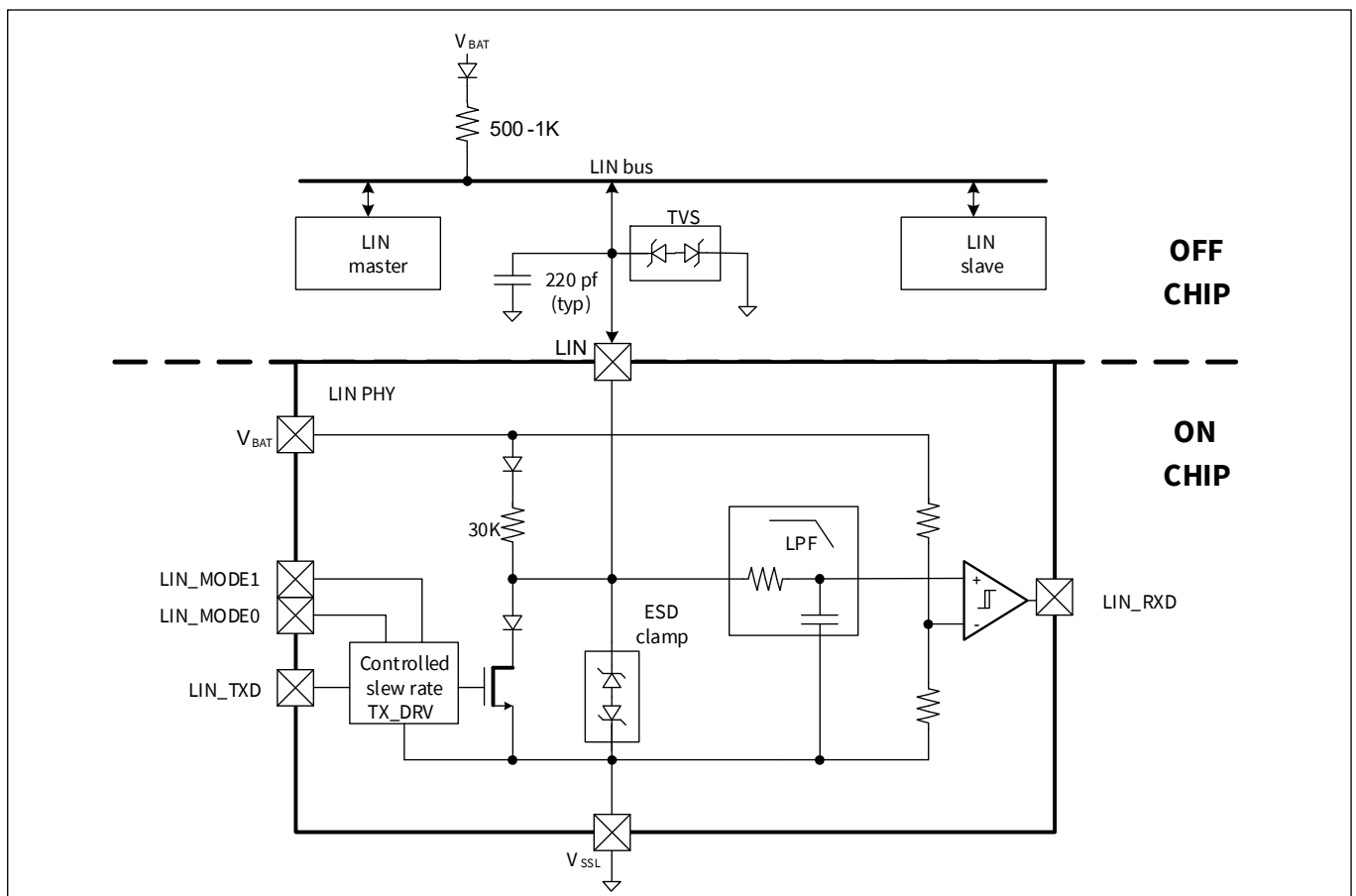
**1.9.1.17 LIN transceiver**

The LIN transceiver meets the requirements of LIN standard 2.2A and is downward compatible with the LIN 2.0. Data rates of 10 kbps and 20 kbps are supported. A non-LIN fast slew rates mode is available providing 100 kbps data rates for fast downloads for factory and field flash program updates using the LIN pin.

The LIN transceiver is guaranteed not to block the LIN bus with a dominant bit when the VBAT voltage is below the minimum LIN supply voltage (7V, VBAT\_LIN, LIN 2.2A Parameter 10) and may continue to operate below that voltage but communication is not guaranteed. The LIN transceiver is inhibited if VCCD is not valid to prevent erroneous control signals from interference with the LIN bus. A timer is also present clocked by the low-speed clock system which disables the LIN if the bus is dominant for too long. The timer can generate an interrupt if the LIN bus wakeup signal (LIN bus in dominant state for 250 μs to 5 ms) is detected. LIN compliance testing is facilitated by making the transceiver data signals available on GPIO pins (LIN\_RX, LIN\_TX) as are the serial control block UART signals are also available (UART\_RX, UART\_TX).

The LIN transceiver has an open drain output and digital receiver connected to the LIN pin which connects to the LIN bus. The bus has pullups to VBAT with total pullup resistance between 500 Ω and 1 kΩ. A series diode between VBAT and the pull-ups prevents the bus from powering VBAT. The diode and pull-up resistor are usually located at or near the LIN master. The transceiver has a weak slave resistor (nominally 30 kΩ) on-chip and the driver can be configured to provide a weak, normal, or fast pull-down. Both the pull-up and weak pull-down can be used for diagnostics without disturbing LIN bus communications.

The pull-up resistor and ESD networks prevent parasitic current paths if VBAT or ground become disconnected. The LIN driver will withstand differences of ±1 V if shorted to another ground and if continuously shorted to another ground or VBAT will not be permanently damaged. The LIN transceiver complies with Q100-2/IEC6100-4-2 ESD and ISO 7637 capacitively coupled transient pulses. Heating of LIN driver in normal operation does not affect measurement accuracy.



**Figure 21 LIN transceiver**

**Functional definition**

**Table 4 LIN Transceiver Truth Table**

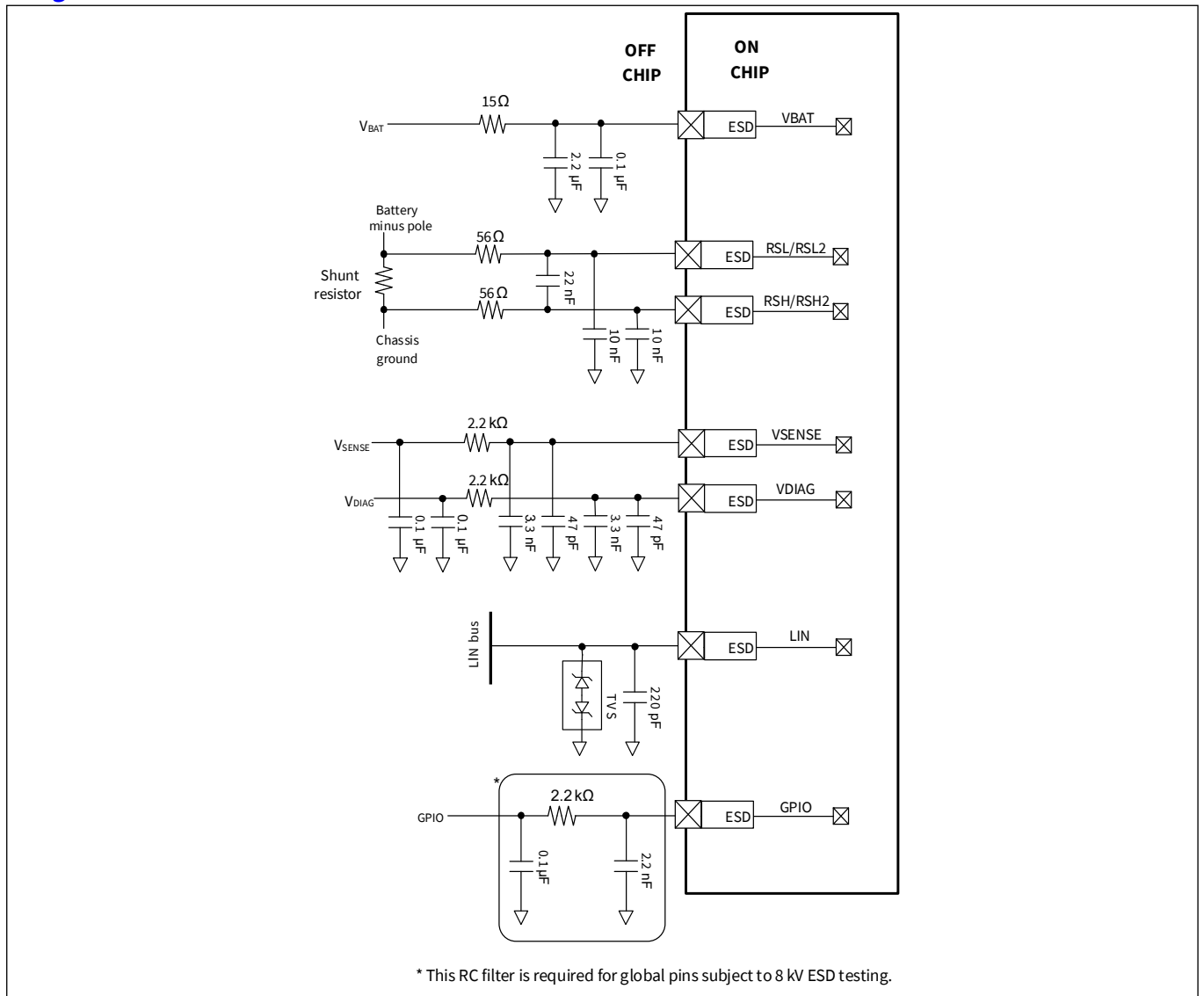
LIN transceiver function	LIN_MODE1	LIN_MODE0	DRIVER			Slave Pull-up
			Slew control	LIN_TXD=1	LIN_TXD=0	
Fast mode (non-LIN)	1	1	No	Z (rec)	LOW (dom)	On
Normal/Enabled	1	0	Yes	Z (rec)	LOW (dom)	On
Weak (diagnosis)	0	1	No	Z (rec)	LOW (weak)	On*
Disabled	0	0	No	Z (rec)	Z	Off

rec - recessive; dom - dominant; Z - driver off; For LIN\_TXD and LIN\_RXD recessive=1, dominant=0

\* In weak (diagnosis) mode, slave pull-up is ON when LIN\_TXD=1, OFF when LIN\_TXD=0

**1.10 ESD protection**

PSOC™ 4 HVPA requires sufficient protection to withstand the high voltage ESD on specific pins. The ESD on LIN, VBAT, VSENSE, VDIAG, RSH, RSL, RSH2, and RSL2 is rated at ±8 kV (SIDA2), and is required to be protected as shown in [Figure 22](#).



**Figure 22 ESD protection**

## Functional definition

### 1.11 Device programming & debugging

PSOC™ 4 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The SWD interface is fully compatible with industry-standard third-party tools. PSOC™ 4 provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

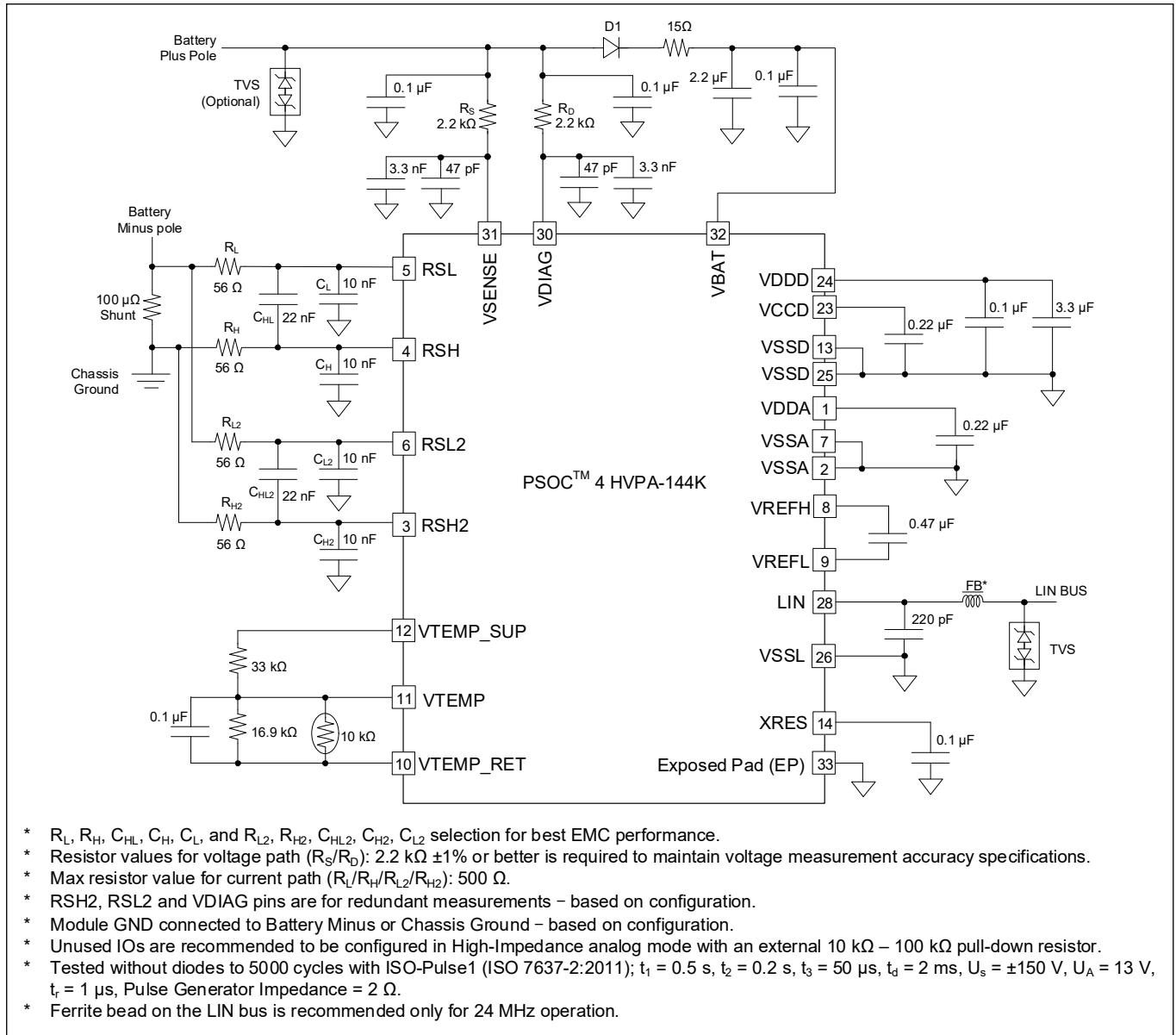
- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus, firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSOC™ 4, with device security-enabled, may not be returned for failure analysis. This is a trade-off the PSOC™ 4 allows the customer to make.

**Sample application schematic**

**2 Sample application schematic**



**Pinouts**

### 3 Pinouts

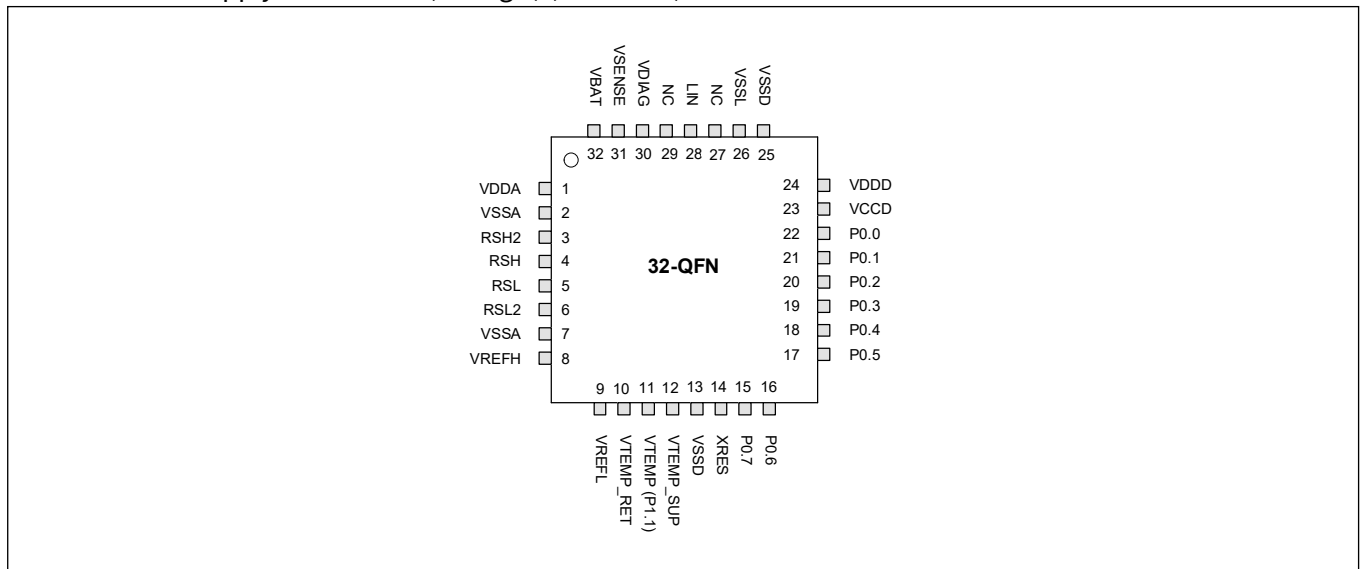
**Table 5** provides the pin list for PSOC™ HVPA for the 32-pin QFN package.

**Table 5 32-QFN pin description**

32-QFN		32-QFN	
Pin	Name	Pin	Name
1	VDDA	17	P0.5
2	VSSA	18	P0.4
3	RSH2	19	P0.3
4	RSH	20	P0.2
5	RSL	21	P0.1
6	RSL2	22	P0.0
7	VSSA	23	VCCD
8	VREFH	24	VDDD
9	VREFL	25	VSSD
10	VTEMP_RET	26	VSSL
11	VTEMP	27	NC
12	VTEMP_SUP	28	LIN
13	VSSD	29	NC
14	XRES	30	VDIAG
15	P0.7	31	VSENSE
16	P0.6	32	VBAT

**Descriptions of the power pins are as follows:**

- **VDDD:** Power supply for the digital section
- **VDDA:** Power supply for the analog section
- **VSSD, VSSA:** Ground pins for the digital and analog sections respectively
- **VCCD:** Power supply for the core (LV Logic) (1.8 V ±5%)



**Figure 23 Pin assignment**

### 3.1 Alternate pin functions

Each port pin can be assigned to one of multiple functions; it can, for example, be an analog I/O or a digital peripheral function. The pin assignments are shown in [Table 6](#).

**Table 6** Alternate pin functions

Name	Analog	ACTIVE				DEEP SLEEP		
		ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2
P0.0	amuxbus_a/amuxbus_b	tcpwm.tr_in[0]	lin.lin_rx[0]	scb.uart_rx:1	tcpwm.line[0]	scb.spi_clk	–	scb.i2c_scl
P0.1	amuxbus_a/amuxbus_b	tcpwm.tr_in[1]	lin.lin_tx[0]	scb.uart_tx:1	tcpwm.line_compl[0]	scb.spi_mosi	–	scb.i2c_sda
P0.2	amuxbus_a/amuxbus_b	tcpwm.tr_in[2]	lin.lin_en[0]	–	tcpwm.line[1]	scb.spi_miso	–	–
P0.3	amuxbus_a/amuxbus_b	tcpwm.tr_in[3]	–	–	tcpwm.line_compl[1]	scb.spi_select0	–	–
P0.4	amuxbus_a/amuxbus_b	peri.virt_in_0	–	–	tcpwm.line[2]	scb.spi_select1	–	cpuss.fault_out[0]
P0.5	amuxbus_a/amuxbus_b	srss.ext_clk	–	–	tcpwm.line_compl[2]	scb.spi_select2	–	cpuss.fault_out[1]
P0.6	amuxbus_a/amuxbus_b	peri.virt_in_1	–	–	–	scb.spi_select3	–	cpuss.swd_data
P0.7	amuxbus_a/amuxbus_b	peri.virt_in_2	–	–	–	–	–	cpuss.swd_clk
VTEMP_RET	pacss.vtemp_ret	–	–	–	–	–	–	–
VTEMP (P1.1)	pacss.vtemp	–	–	–	–	–	–	–
VTEMP_SUP	pacss.vtemp_sup	–	–	–	–	–	–	–
VirtLinEn(P2.2) <sup>[1]</sup>	–	–	lin.lin_en[1]	–	–	–	–	–
VirtLinTxd(P2.1) <sup>[1]</sup>	–	–	lin.lin_tx[1]	scb.uart_tx	–	–	–	–
VirtLinRxd(P2.0) <sup>[1]</sup>	–	–	lin.lin_rx[1]	scb.uart_rx	–	–	–	–

**Note**

1. Internal connections to the integrated LIN PHY.

**Electrical specifications**

## 4 Electrical specifications

### 4.1 Absolute maximum ratings

Within the maximum ratings, no damage shall occur. Parametric and functionality may deviate from specifications. All analog voltages are relative to  $V_{SSA}$  and all digital voltages are relative to  $V_{SSD}$ . A negative current if flowing out of a pin, and positive current into a pin.

**Table 7 Absolute maximum ratings**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SIDA1	$V_{ESDHBM}$	$V_{HBM}$ ESD on all pins	±2000	–	–	V	–
SIDA2	$V_{ESDHV}$	ESD on LIN, $V_{BAT}$ , $V_{SENSE}$ , $V_{DIAG}$ , RSH, RSL, RSH2, RSL2, GPIO	±8000	–	–	V	As per ISO10605 With required external protection as per the guidelines in the “ <b>ESD protection</b> ” on page 30 section
SIDA3	$V_{ESDCDMCOR}$	CDM ESD on Corner Pins	±750	–	–	V	–
SIDA4	$V_{ESDCDM}$	CDM ESD on non-corner pins	±500	–	–	V	–
SIDA5	$V_{BAT}$	Supply voltage $V_{BAT}$ <sup>[2]</sup>	–0.3	–	42	V	–
SIDA6	$V_{SHV}$	$V_{SENSE}/V_{DIAG}$ ADC sense voltage <sup>[2]</sup>	–0.3	–	42	V	–
SIDA7	$V_{SHV}$	$V_{SENSE}/V_{DIAG}$ ADC sense voltage <sup>[2]</sup>	–40	–	42	V	With external 2.2 kΩ resistor
SIDA8	$I_{SH}$	$V_{SENSE}/V_{DIAG}$ current <sup>[2]</sup>	–20	–	1	mA	Forced externally
SIDA9	$I_{CS}$	$R_{SH}/R_{SL}/R_{SH2}/R_{SL2}$ current <sup>[2]</sup>	–1	–	1	mA	Forced externally
SIDA10	$V_{LIN}$	LIN pin voltage <sup>[2]</sup>	–27	–	42	V	–
SIDA11	$I_{LIN}$	LIN pin current <sup>[2]</sup>	–	–	200	mA	–
SIDA12	$V_{GPIO}$	GPIO pin input voltage	–0.5	–	$V_{DDD} + 0.5$	V	–
SIDA13	$V_{DDA}, V_{DDD}$	$V_{DDA}, V_{DDD}$ supply voltage	–0.3	–	4.7	V	–
SIDA13A	$I_{BAT}$	$V_{BAT}$ supply current <sup>[3]</sup>	–	–	160	mA	–
SIDA13B	$I_{BATABSDC}$	$V_{BAT}$ supply current, long-term average	–	–	40	mA	–
SIDA14	$V_{CCD}$	VCC core supply voltage	–0.3	–	1.95	V	–
SIDA16	$I_{GPIO}$	Current per GPIO pin	–20	–	20	mA	–
SIDA17	$V_{SLV}$	RSHx, RSLx, VTEMP	–0.3	–	$V_{DDA} + 0.3$		–
SIDA18	$T_A$	Ambient temperature	–40	–	125	°C	–
SIDA19	$T_S$	Storage temperature	–55	–	125	°C	–
SIDA20	$T_J$	Junction temperature	–40	–	150	°C	–
SIDA21	$T_{LIFE}$	Life time	15	–	–	Years	–
SIDA22	$T_{STORAGE1}$	Storage time	5	–	–	Years	$T_A = 55\text{ °C}, 85\% \text{ r.H.}$
SIDA23	$T_{STORAGE2}$	Storage time	15	–	–	Years	$T_A = 40\text{ °C}, 80\% \text{ r.H.}$

**Notes**

- To prevent damage caused by high-voltage pulses, external protection (that is, series resistor, diode, TVS) may be required. To allow a minimum system level supply voltage of 4.5 V, external protection circuits including reverse protection diodes are designed in a way that guarantees the device minimum functional voltage  $V_{BAT}$  of at least 3.6 V.
- Absolute max current includes inrush / transient current during power-up.

**Electrical specifications**

**Table 7 Absolute maximum ratings**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SIDA24	$t_{SCVHVREG}$	Short circuit tolerance time: HVREG <sup>[4]</sup>	-	-	60	min	$V_{BAT}$ : 3.6 V to 28 V
			-	-	500	ms	$V_{BAT}$ : 28 V to 42 V
SIDA24A	$t_{SCLIN}$	Short circuit tolerance: LIN	-	-	60 <sup>[5]</sup>	min	$V_{BAT} = LIN$ : 3.6 V to 28 V
			-	-	500	ms	$V_{BAT} = LIN$ : 28 V to 42 V

Unless otherwise noted, functionality and parameters are valid over operating voltage and temperature range. All analog voltages are relative to  $V_{SSA}$ , all digital voltages are relative to  $V_{SSD}$ . A negative current if flowing out of a pin, and positive current into a pin.

**Table 8 Operating conditions**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID1	$V_{BAT}$	Supply voltage VBAT	3.6	-	28	V	-
SID2	$V_{BAT\_LIN}$	VBAT range for LIN communications	7	-	18	V	LIN 2.2 A Parameter 10
SID2A	$V_{BAT\_LIN\_ext}$	VBAT range for LIN communications <sup>[6]</sup>	6	-	28	V	Extended LIN 2.2 A specification
SID3	$V_{SENSE}$	VBAT sense voltage	3.6	-	28	V	-
SID4	$V_{DIAG}$	VDIAG sense voltage	3.6	-	28	V	-
SID4A	$I_{SENSE}$	$V_{SENSE}/V_{DIAG}$ current	-	5	20	$\mu A$	-
SID5	$V_{LIN}$	LIN output voltage	6	-	28	V	-
SID6	$R_{LIN,PU}$	LIN pull-up resistor	20	30	47	k $\Omega$	-
SID7	$V_{RSx}$	Input range ( $R_{SH}$ , $R_{SL}$ )	-0.3	-	0.3	V	-
SID7A	$I_{CS}$	RSH/RSL/RSH2/RSL2 Current	-2000	-	20	nA	$V_{INADC}$ : -0.3 to 0.3 V   -40 to +125°C
SID7B			-200	-	20	nA	$V_{INADC}$ : -0.15 to +0.15 V   -40 to +125 °C
SID7C			-20	-	20	nA	$V_{INADC}$ : -0.075 to +0.075 V   -40 to +125 °C
SID7D			-12	-	12	nA	$V_{INADC}$ : -0.003 to +0.003 V   -40 to +125 °C
SID7E			-4	-	4	nA	$V_{INADC}$ : -0.003 to +0.003 V   -40 to +85 °C
SID7F	$I_{CS\_diff}$	Difference of leakage current for an RSH-RSL pair	-1	-	1	nA	$V_{INADC}$ : -0.003 to +0.003 V   -40 to +85°C

**Notes**

- Current limited to prevent thermal runaway and catastrophic part damage. If junction temperature exceeds limits in SIDA20, part operation is not guaranteed and part reliability might be affected.
- 60 minutes is cumulative and applies only when the local transmitter is enabled and driving dominant state on to the LIN bus. Part testing is performed for 60 minutes with LIN driving dominant state continuously.
- The LIN interface should only be active when the supply voltage is within  $V_{BAT\_LIN}$ . Outside  $V_{BAT\_LIN}$ , the LIN module will not interfere with bus communications (will not block the bus with a dominant bit). LIN V2.2A specifications are based on  $7V \leq V_{BAT} \leq 18V$ , the AC/DC behavior can change for  $6V \leq V_{BAT} < 7V$  and  $18V < V_{BAT} < 28V$ .

**Electrical specifications**

**Table 8**      **Operating conditions** (continued)

<b>Spec ID#</b>	<b>Parameter</b>	<b>Description</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Details/ Conditions</b>
SID8	R <sub>SENSE</sub>	Shunt current sense resistor	25	100	200	μΩ	–
SID9	V <sub>INADC</sub>	ADC input voltage range	–0.3	–	1.2	V	–
SID9A	V <sub>INGPIO</sub>	GPIO input voltage range (digital)	–0.3	–	V <sub>DD</sub> +0.3	V	–
SID10	T <sub>A</sub>	Ambient temperature range	–40	–	125	°C	–

## 4.2 Device-level specifications

Unless otherwise noted, functionality and parameters are valid over operating conditions and lifetime (range of functionality). All analog voltages are relative to  $V_{SSA}$ , digital voltages are relative to  $V_{SSD}$ . A negative current is flowing out of a pin, positive current into a pin.

### 4.2.1 Operating current and wakeup times

**Table 9** Operating current and wakeup times

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID12			–	6	8	mA	IMO = 49.152 MHz, HFCLK = IMO/2, CPU Core only
SID12A	$I_{BAT\_NORM\_24}$	Average supply current in active mode	–	12	14	mA	<p>Clocks: IMO = 49.152 MHz HFCLK = IMO/2 SYSCLK = HFCLK SRSS PUMP Clock = Disabled</p> <p>TCPWM: 1 counter enabled</p> <p>LIN: 10 kHz, 25% active dominant, 25% active recessive, 50% standby</p> <p>PACSS: Both channels enabled and continuously converting Power settings: Buffer = 78%, PGA = 58%, Modulator = 88%, Sample rate = 8 ksps, FIR enabled, 15 taps MOD_FCHOP = /32</p> <p>PACSS Pump clock sourced from HFCLK</p> <p>CPU: void main() { int i = 1; while(1) { i = i + 1; i = i + 2; i = i + 3; i = i + 4; i = i + 5; }} Designed to provide constant activity + code flash access, not absolute worst case CPU current Prefetch enabled, flash wait states = 1 for 24.576 MHz<sup>[7]</sup></p>

**Note**

7. See the reference manual for more details on the ACHAN power chopping configuration and pump clock configuration details.

**Table 9** Operating current and wakeup times (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID13			–	10	12	mA	IMO = 49.152 MHz, HFCLK = IMO, CPU Core only
SID13A	I <sub>BAT_NORM_48</sub>	Average supply current in active mode	–	16	18	mA	<p>Clocks: IMO = 49.152 MHz HFCLK = IMO SYSCLK = HFCLK SRSS PUMP Clock = Disabled</p> <p>TCPWM: 1 counter enabled</p> <p>LIN: 10 kHz, 25% active dominant, 25% active recessive, 50% standby</p> <p>PACSS: Both channels enabled and continuously converting Power settings: Buffer = 78%, PGA = 58%, Modulator = 88%, Sample rate = 8 ksps, FIR enabled, 15 taps MOD_FCHOP = /32</p> <p>PACSS Pump clock sourced from HFCLK</p> <p>CPU: void main() { int i = 1; while(1) { i = i + 1; i = i + 2; i = i + 3; i = i + 4; i = i + 5; }}</p> <p>Designed to provide constant activity + code flash access, not absolute worst case CPU current Prefetch enabled, flash wait states = 3 for 49.152 MHz<sup>[7]</sup></p>
SID14	I <sub>BAT_NOCPU</sub>	Average current with CPU in Sleep mode <sup>[8]</sup>	–	3	–	mA	HFCLK = IMO = 24MHz, SWD pins grounded.
SID15A.3	I <sub>BAT_STOP</sub>	Average supply current in Deep Sleep mode with once-per-second wakeup <sup>[9]</sup>	–	85	100	μA	Max value at T <sub>A</sub> = 85°C; HV dividers off; VBAT >= 5V
SID17A.3	I <sub>BAT_SLEEP</sub>	Average current in Deep Sleep mode without periodic wakeup and no periodic calibration <sup>[10]</sup>	–	35	60	μA	Max value at T <sub>A</sub> = 85 °C; HV dividers off; VBAT >= 5V
SID19	I <sub>BAT_XRES</sub>	Current with XRES low	–	65	–	μA	XRES input low
SID20	t <sub>STARTUP</sub>	Start time from reset release	–	–	8	ms	XRES or POR release Includes the ROM boot time and the SWD listen window.

**Table 9** Operating current and wakeup times (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID21	t <sub>SLEEP</sub>	Wakeup from Sleep power mode	–	–	6	SYSCLK cycles	–
SID22	t <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep power mode	–	–	35	μs	–

**Notes**

- 8. PSOC™ 4 power mode = sleep, CPU powered down, all other high- and low-speed clocks are active; peripherals off; DMA inactive, RAM retained.
- 9. PSOC™ 4 power mode = Deep Sleep: μC powered down, high-speed clocks and peripherals off, low-power oscillator and timer active, all RAM and registers except internal μC registers retained. LIN and watchdog timers active. Includes once-per-second wakeup for measurements periodic measurements.
- 10. Same as IBAT\_STOP (PSOC 4 Power mode = Deep Sleep) without cyclic wakeup (no periodic calibration or measurements).

**Electrical specifications**

**4.2.2 Voltage regulators**

**Table 10 Voltage regulators**

SPEC ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID23	V <sub>DDA</sub>	Analog regulator voltage	3	3.3	3.6	V	–
SID24	I <sub>DDA</sub>	Analog regulator current	–	N/A	–	–	Not to be used off-chip
SID25	V <sub>DDD</sub>	Digital regulator voltage, V <sub>BAT</sub> > 4 V	3	3.3	3.6	V	–
SID26	V <sub>DDD</sub>	Digital regulator voltage, 4 V ≥ V <sub>BAT</sub> ≥ 3.6 V	2.7	–	3.6	V	–
SID27	I <sub>DD</sub>	Digital regulator current	–	–	30	mA	Core, GPIO, & Ext. loads
SID27A	I <sub>DDGPIO</sub>	Digital regulator current (GPIOs)	–	–	10	mA	For GPIO & Ext. loads
SID28	V <sub>CCD</sub>	Core regulator voltage	1.75	1.8	1.95	V	–
SID29	I <sub>CC</sub>	Core regulator current	–	N/A	–	–	Not to be used off-chip

**4.2.3 GPIO**

**Table 11 GPIO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID30	V <sub>IH</sub>	Input voltage high threshold	0.7*V <sub>DDD</sub>	–	–	V	CMOS Input
SID31	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3*V <sub>DDD</sub>	V	CMOS Input
SID32	V <sub>IH</sub>	LVTTL input, V <sub>DDD</sub> ≥ 2.7 V	2	–	–	V	–
SID33	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> ≥ 2.7 V	–	–	0.8	V	–
SID34	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.45	–	–	V	I <sub>OH</sub> = –4 mA   V <sub>DDD</sub> ≥ 3 V I <sub>OH</sub> = –1 mA   2.7 V ≤ V <sub>DDD</sub> < 3 V
SID35	V <sub>OL</sub>	Output voltage low level	–	–	0.45	V	I <sub>OL</sub> = 10 mA   V <sub>DDD</sub> ≥ 2.7 V
SID36	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID37	R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID38	I <sub>IL</sub>	Input leakage current (absolute value)	–	2	–	nA	25°C, V <sub>DDD</sub> = 3.0 V
SID38A	I <sub>IL</sub>	Input leakage current (absolute value)	–	–	1	μA	T <sub>J</sub> = 150°C, V <sub>DDD</sub> = 3.0 V
SID40	C <sub>IN</sub>	Input capacitance	–	–	10	pF	–
SID41	V <sub>HYSTTL</sub>	Input hysteresis LVTTL V <sub>DDD</sub> > 2.7 V	25	40	–	mV	–
SID42	V <sub>HYS CMOS</sub>	Input hysteresis CMOS	0.05*V <sub>DDD</sub>	–	–	V	–

**Electrical specifications**

**Table 11** GPIO DC specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID43	I <sub>DIODE</sub>	Current through protection diode to V <sub>DDD</sub> /V <sub>SS</sub>	–	–	100	µA	100 µA is an absolute value; V <sub>DDD</sub> + 0.25 V = source current, V <sub>SS</sub> - 0.25 V = sink current
SID44	I <sub>TOT_GPIO</sub>	Maximum total source or Sink chip current	–	–	10	mA	Sum of GPIO Source or Sink current.

**Table 12** GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID45	t <sub>RISEF</sub>	Rise time in Fast Strong Mode	1.5	–	12	ns	3.3 V V <sub>DDD</sub> , Load = 25 pF
SID46	t <sub>FALLF</sub>	Fall time in Fast Strong Mode	1.5	–	12	ns	3.3 V V <sub>DDD</sub> , Load = 25 pF
SID47	t <sub>RISES</sub>	Rise time in Slow Strong Mode	10	–	60	ns	3.3 V V <sub>DDD</sub> , Load = 25 pF
SID48	t <sub>FALLS</sub>	Fall time in Slow Strong Mode	10	–	60	ns	3.3 V V <sub>DDD</sub> , Load = 25 pF
SID49	f <sub>GPIOUTF</sub>	GPIO f <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 3.6 V. Fast Strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID50	f <sub>GPIOUTS</sub>	GPIO f <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 3.6 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID51	f <sub>GPIOIN</sub>	GPIO input operating frequency; 2.7 V ≤ V <sub>DDD</sub> ≤ 3.6 V	–	–	48	MHz	90/10% V <sub>IO</sub>

**4.2.4 XRES**

**Table 13** XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDX1	V <sub>IH</sub>	Input voltage high threshold	0.7*V <sub>DDD</sub>	–	–	V	CMOS Input
SIDX2	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3*V <sub>DDD</sub>	V	CMOS Input
SIDX3	R <sub>PULLUP</sub>	Pull-up resistor	–	60	–	kΩ	–
SIDX4	C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
SIDX5	V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	Guaranteed by design
SIDX6	I <sub>DIODE</sub>	Current through protection diode to V <sub>DDD</sub> /V <sub>SS</sub>	–	–	100	µA	100 µA is an absolute value; V <sub>DDD</sub> + 0.25 = source current, V <sub>SS</sub> - 0.25 = sink current

**Electrical specifications**

**Table 14 XRES AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDX7	t <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–
SIDX8	t <sub>RESETWAKE</sub>	Wake-up time from Reset release <sup>[11]</sup>	–	–	8	ms	–

**4.2.5 Clocks**

**Table 15 Internal oscillators and clocks**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID53	f <sub>IMO</sub>	IMO clock frequency <sup>[12]</sup>	–	–	49.152	MHz	–
SID53A <sup>[13]</sup>	f <sub>SYSCLK</sub>	System (CPU) clock frequency	–	–	49.152	MHz	–
SID53B <sup>[14]</sup>	f <sub>SYSCLK</sub>	System (CPU) clock frequency	–	–	24.576	MHz	–
SID54	f <sub>IMO_ACCY1</sub>	IMO frequency variation (not locked to HPOSC)	–2.0	–	2.0	%	–40°C < T <sub>A</sub> < 105°C; f <sub>IMO</sub> = 48 MHz or 49.152 MHz
SID54A	f <sub>IMO_ACCY1a</sub>		–3.0	–	3.0	%	T <sub>A</sub> ≥ 105°C; f <sub>IMO</sub> = 48 MHz or 49.152 MHz
SID55 <sup>[17]</sup>	f <sub>IMO_ACCY</sub>	IMO frequency variation (locked to HPOSC)	–1.0	–	1.0	%	f <sub>IMO</sub> = 48 MHz or 49.152 MHz
SID55A <sup>[18]</sup>			–1.5	±1.0	1.5		
SID56	f <sub>HPOSC</sub>	Precision 2 MHz reference oscillator	–	2.0	–	MHz	–
SID57 <sup>[17]</sup>	f <sub>HPOSC_ACCY</sub>	Precision 2 MHz reference oscillator	–1.0	–	1.0	%	–
SID57A <sup>[18]</sup>	f <sub>HPOSC_ACCYa</sub>		–1.5	±1.0	1.5	%	–
SID58	f <sub>PILO</sub>	Precision internal low speed oscillator (PILO) <sup>[15]</sup>	–	32	–	kHz	–
SID59 <sup>[17]</sup>	f <sub>PILO_ACCY</sub>	PILO accuracy (no periodic calibration)	–5.0	–	5.0	%	–
SID59A <sup>[18]</sup>			–7.0	±5.0	7.0		–
SID60 <sup>[17]</sup>	f <sub>PILO_ACCY2</sub>	PILO accuracy (with periodic calibration) <sup>[16]</sup>	–1.0	–	1.0	%	–
SID60A <sup>[18]</sup>	f <sub>PILO_ACCY2a</sub>		–1.5	±1.0	1.5	%	–

**Notes**

11. Includes the ROM boot time and the SWD listen window.
12. f<sub>IMO</sub> is factory trimmed and is user adjustable between 24 MHz and 48 MHz in 4-MHz steps. The 48 MHz setting can be boosted to 49.152 MHz using "Special" calibration data stored in SFLASH.
13. For CY8C414x devices. See [Ordering information](#).
14. For CY8C412x devices. See [Ordering information](#).
15. The PILO runs in all power modes and is used for low power interval timers and counters.
16. Periodic calibration - locked to HPOSC at least once per second during stop mode. Power required for periodic calibration is included in average stop mode supply current (IBAT\_STOP).
17. For 0.1% and 0.15% voltage accuracy parts (-HV413, -HV423). See [Ordering information](#).
18. For 0.25% voltage accuracy part (-HV403). See [Ordering information](#).

**Electrical specifications**

**4.3 Analog**

**4.3.1 LIN transceiver**

**Table 16 LIN transceiver specifications<sup>[19]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDL63	I <sub>BUS_LIM</sub>	LIN output current	40	–	200	mA	Param 12
SIDL64	I <sub>BUS_PAS_dom</sub>	Receiver dominant state input leakage (Driver off; V <sub>BUS</sub> =0 V, V <sub>BAT</sub> =12 V)	–1	–	1	mA	Param 13
SIDL66	I <sub>BUS_PAS_rec</sub>	Receiver recessive state input leakage (Driver off; 7 V<V <sub>BUS</sub> <18 V, 7 V<V <sub>BAT</sub> <18 V)	–	–	20	μA	Param 14
SIDL68	I <sub>BUS_NO_GND</sub>	Loss of local ground (V <sub>SS</sub> =V <sub>BAT</sub> <18 V, 7 V<V <sub>BUS</sub> <V <sub>BAT</sub> <18 V)	–1	–	1	mA	Param 15
SIDL70	I <sub>BUS_NO_BAT</sub>	Loss of battery power (V <sub>BAT</sub> disconnected, 7 V<V <sub>BUS</sub> <18 V)	–	–	100	μA	Param 16
SIDL72	V <sub>BUSdom</sub>	Receiver dominant state	–	–	0.4	V <sub>BAT</sub>	Param 17
SIDL73	V <sub>BUSrec</sub>	Receiver recessive state	0.6	–	–	V <sub>BAT</sub>	Param 18
SIDL74	V <sub>BUScnt</sub>	Receiver center voltage	0.475	0.5	0.525	V <sub>BAT</sub>	Param 19
SIDL75	V <sub>BUShys</sub>	Receiver hysteresis	–	–	0.175	V <sub>BAT</sub>	Param 20
SIDL76	V <sub>OH</sub>	Bus transmitter recessive output voltage	V <sub>BAT</sub> -2	–	V <sub>BAT</sub>	V	Not a LIN 2.2 A specification
SIDL77	V <sub>OL</sub>	Bus transmitter dominant output voltage (V <sub>BAT</sub> =V <sub>BUS</sub> =7 V)	–	–	1.2	V	RL = 500 Ω (I <sub>OL</sub> <12 mA)
SIDL79	V <sub>OL</sub>	Bus transmitter dominant output voltage (V <sub>BAT</sub> =V <sub>BUS</sub> =18 V)	–	–	2	V	RL = 500 Ω (I <sub>OL</sub> <32 mA)
SIDL81	V <sub>SerDiode</sub>	Voltage drop at external series diodes	0.4	0.7	1	V	Param 21
SIDL82	R <sub>LIN,PU</sub>	Internal slave pull-up resistor <sup>[20]</sup>	20	30	47	kΩ	Param 26 (R <sub>SLAVE</sub> )
SIDL83	R <sub>LIN,PD</sub>	Internal pull-down resistor for diagnosis	20	30	47	kΩ	Not a LIN 2.2A specification
SIDL84	D1	Duty cycle 1 (20 kbps)	0.396	–	–	–	Param 27 D1 = t <sub>Bus_rec</sub> (min) / (2 x t <sub>Bit</sub> ) for baud rate = 20 kbps, V <sub>BAT_LIN</sub> = 7 V to 18 V
SIDL84a	D1a		0.35	–	–	–	LIN 2.2 A spec Param 27 with extended range, (functionality will not block the LIN bus) D1 = t <sub>Bus_rec</sub> (min) / (2x t <sub>Bit</sub> ) for baud rate = 20 kbps, V <sub>BAT_LIN</sub> = 6 V to 7 V & 18 V to 28 V

**Notes**

- 19.LIN V2.2A specifications are based on 7 V ≤ V<sub>BAT</sub> ≤ 18 V, the AC/DC behavior can change for 6 V ≤ V<sub>BAT</sub> < 7 V and 18 V < V<sub>BAT</sub> ≤ 28 V.  
20.LIN V2.2A specifies 20 kΩ ≤ R<sub>SLAVE</sub> ≤ 60 kΩ. Infineon is specifying a lower maximum R<sub>SLAVE</sub> value of 47 kΩ..

**Electrical specifications**

**Table 16 LIN transceiver specifications<sup>[19]</sup> (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDL85	D2	Duty Cycle 2 (20 kbps)	-	-	0.581	-	Param 28 D2 = tBus_rec(max) / (2 x tBit) for baud rate = 20 kbps, V <sub>BAT_LIN</sub> = 7.6 V to 18 V
SIDL85a	D2a		-	-	0.65	-	LIN 2.2 A spec Param 28 with extended range, (functionality will not block the LIN bus) D2 = tBus_rec (max) / (2x tBit) for baud rate = 20 kbps, V <sub>BAT_LIN</sub> = 18V to 28 V
SIDL86	D3	Duty Cycle 3 (10 kbps)	0.417	-	-	-	Param 29 D3 = tBus_rec(min) / (2 x tBit) for baud rate = 10.4 kbps
SIDL87	D4	Duty Cycle 4 (10 kbps)	-	-	0.59	-	Param 30 D4 = tBus_rec(max) / (2 x tBit) for baud rate = 10.4 kbps
SIDL88	t <sub>rx_pd</sub>	Propagation delay of receiver	-	-	6	μs	Param 31
SIDL89	t <sub>rx_sym</sub>	Symmetry of receiver propagation delay	-2	-	2	μs	Param 32
SIDL90	t <sub>r</sub>	Rise Time	3.5	-	22.5	μs	1 nf/1 kΩ, 6.8 nf / 660 Ω, 10 nf / 500 Ω
SIDL91	t <sub>f</sub>	Fall Time	3.5	-	22.5	μs	1 nf/1 kΩ, 6.8 nf/ 660 Ω, 10 nf/500 Ω
SIDL92	d(t <sub>r</sub> -t <sub>f</sub> )	Difference between rise time to fall time	-4	-	4	μs	1 nf/1 kΩ, 6.8 nf/ 660 Ω, 10 nf/500 Ω
SIDL93	f <sub>LIN10K</sub>	Baud rate for LIN 10 kbps mode	-	10	-	kbps	-
SIDL94	f <sub>LIN20K</sub>	Baud rate for LIN 20 kbps mode	-	20	-	kbps	-
SIDL95	f <sub>PROG</sub>	Baud rate for 100 kbps for fast program transfer mode <sup>[21]</sup>	-	100	-	kbps	LIN 2.2 A specifications are not applicable in this mode

Per LIN 2.2 A, comments reference appropriate LIN specification parameters. If no parameter is included in the comment, this parameter is not a requirement of the LIN 2.2 A specification.

**Note**

21. Fast program transfer mode exceeds the 20 kbps maximum LIN 2.2 A transfer rate and is not a LIN compliant operating mode. In this mode, LIN Bus specification parameters do not apply. This mode can be used for factory and field software updates.

**Electrical specifications**

**4.3.2 Temperature channel**

Temperature channel refers to  $V_{TINT}$  (die temp sensor) or  $V_{TEMP}$  (external temp sensor) measurements using ACHAN1 + DCHAN2/3.

**Table 17 Temperature channel specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID96	$T_{RMEAS}$	Measurement range ( $T_J$ )	-40	-	125	°C	-
SID97	$T_{ACC}$	Accuracy including lifetime and temperature drift	-2.5	-	2.5	°C	Primary temp sensor; Includes firmware filtering Alternating VBE measurements are required, refer to the reference manual for more details; $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$
SID97a	$T_{ACC\_alternate}$	Accuracy including lifetime and temperature drift	-3	±1	3	°C	Secondary/Alternate temp sensor; $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$
SID98	$T_{RES}$	Resolution	-	-	0.1	°C	-
SID99a	$f_{TUPDATE}$	Effective signal update rate output <sup>[22]</sup>	0.36	-	16	ksps	Measurement using secondary channel configuration and single shot mode Max spec is defined for DR=64, DR2=1, single shot mode; Min spec is for information only to show the lowest update rate possible
SID100	$N_{ADC\_TEMP}$	Resolution	16	-	-	bits	No missing codes
SID101	$V_{TNOISE}$	Output referred noise	-	-	0.16	°C <sub>rms</sub>	Using SID99a configuration and with firmware 8-tap moving average filter.
SID102	$T_{LATENCY\_MUX}$	Measurement valid delay <sup>[23]</sup>	-	64.7	65.72	µs	See reference manual "PACSS clock cycle equations" DR=64, DR2=0, Sinc3, AVG_MODE=0, OCOR_EN=GCOR_EN=FIR_EN=PP_EN=0 CLK_SYS=48 MHz, CLK_DSM=3.072 MHz
SID103	$V_{TRMEAS}$	VTEMP measurement range	0	-	$V_{DD}/3$	V	External thermistor ADC input. ADC reference is set to VTS_REF, which is $V_{DD}/3$ .
SID103A	ACC_VT	VTEMP accuracy including lifetime and temperature drift (including reference error)	-1.6	-	1.6	%	External thermistor ADC input. Using ACHAN1 + DCHAN2/3 where ADC reference is set to VTS_REF.

**Notes**

22. Temperature measurement requires two VBE measurements. Effective temperature update rate of 16 ksps with an assumption that first VBE measurement is already done.

23. First valid decimator output using a 3.072 MHz ADC clock with OSR = 64 and decimator = Sinc3. Digital FIR filtering and averaging may add more delay.

**Electrical specifications**

**4.3.3 Diagnostic channel**

**Table 18 Diagnostic channel specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID302	NOISE_D	Input referred integrated noise	-	50	90	μVrms	DR = 64, DR2 = 1, Incremental mode, gain 1x
SID303 <sup>[24]</sup>	V <sub>OFF_D</sub>	Diagnostic Channel Input referred offset error for V <sub>SENSE</sub> or V <sub>DIAG</sub> measurements	-130	-	130	μV	1X gain and V <sub>BAT</sub> <18V and T <sub>A</sub> <125°C
SID303A <sup>[24]</sup>	I <sub>OFF_D_LOW_I</sub>	Diagnostic channel input referred offset error for V <sub>SHUNT</sub> measurements	-7	-	7	μV	I < 140A and V <sub>BAT</sub> <18V and T <sub>A</sub> <125°C Corresponds to Gains 256X and 512X
SID303B <sup>[24]</sup>	I <sub>OFF_D_HIGH_I</sub>	Diagnostic Channel Input referred offset error for V <sub>SHUNT</sub> measurements	-1024/ gain	-	1024/ gain	μV	140A < I < 3000A and V <sub>BAT</sub> < 18V and T <sub>A</sub> < 125°C (Corresponds to Gains 4X - 128X)
SID304	DNL_D	Differential non-linearity	-0.05	-	0.05	%	
SID305 <sup>[25]</sup>	ACC_D	Accuracy including lifetime and temperature drift	-0.25	±0.05	0.25	%	3.6 V < V <sub>BAT</sub> < 28 V, -40°C < T <sub>A</sub> < 125 °C; Vin_range = 0 to 1.2V; Gain = 1x

**Notes**

24.Configuration: Incremental conversion mode, DR=64, DR2=1. AAF bypassed.

25.For diagnostic current (V<sub>SHUNT</sub>) measurements using ACHAN1+DCHAN2/3 or voltage (V<sub>SENSE</sub>, V<sub>DIAG</sub>) measurements using ACHAN0/1 + DCHAN2/3, see [Table 19](#) and [Table 20](#).

**Electrical specifications**

**4.3.4 Current channel.**

**Table 19 Current channel specifications**

All the current channel specifications are valid with the automatic gain control (AGC) on, unless specified. Current channel refers to the voltage measurement across RSx shunt pins using ACHAN0 + DCHAN0 channel

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID104	I <sub>RMEAS_G8</sub>	Measurement range (gain=8)	-3000	-	3000	A	For a typical shunt (SID8, 100 μΩ) Guaranteed by design
SID105	I <sub>RMEAS_G512</sub>	Range with gain=512	-93.75	-	93.75	A	Guaranteed by design
SID106 <sup>[26]</sup>	GE1_I	Gain error including lifetime and temperature drift	-0.3	±0.03	0.3	%	V <sub>BAT</sub> < 18 V and T <sub>A</sub> < 105°C
SID106A <sup>[26]</sup>	GE2_I	Gain error including lifetime and temperature drift	-0.5	±0.05	0.5	%	V <sub>BAT</sub> > 18 V or T <sub>A</sub> > 105°C
SID107	DNL_I	Differential non-linearity	-0.1	-	0.1	%	-
SID108 <sup>[27, 29]</sup>	I <sub>OFF_LOW_I</sub>	Current Channel input referred offset error Using ACHAN0 as Current Channel	-0.5	-	0.5	μV	I < 140 A and V <sub>BAT</sub> < 18 V and T <sub>A</sub> < 105°C Corresponds to Gains 256X and 512X
SID109 <sup>[27, 29]</sup>	I <sub>OFF_HIGH_I</sub>	Current channel input referred offset error Using ACHAN0 as current channel	-144/ gain	-	144/ gain	μV	140 A < I < 3000 A and V <sub>BAT</sub> < 18 V and T <sub>A</sub> < 105°C Corresponds to Gains 4X - 128X
SID108A <sup>[28, 29]</sup>	I <sub>OFF_LOW_I</sub>	Current Channel Input referred offset error Using ACHAN0 as Current Channel	-1.5	± 0.5	1.5	μV	I < 140 A and V <sub>BAT</sub> < 18 V and T <sub>A</sub> < 105°C Corresponds to Gains 256X and 512X
SID109A <sup>[28, 29]</sup>	I <sub>OFF_HIGH_I</sub>	Current channel input referred offset error; Using ACHAN0 as current channel	-224/ gain	± 144/ gain	224/ gain	μV	140 A < I < 3000 A and V <sub>BAT</sub> < 18 V and T <sub>A</sub> < 105°C Corresponds to Gains 4X - 128X
SID110 <sup>[27, 29]</sup>	I <sub>OFF_HIGH_V_T_LOW_I</sub>	Current channel input referred offset error Using ACHAN0 as current channel	-1.0	-	1.0	μV	I < 140 A and V <sub>BAT</sub> > 18 V or T <sub>A</sub> > 105°C Corresponds to Gains 256X and 512X
SID110A <sup>[27, 29]</sup>	I <sub>OFF_HIGH_V_T_HIGH_I</sub>	Current channel input referred offset error Using ACHAN0 as current channel	-176/ gain	-	176/ gain	μV	140 A < I < 3000 A and V <sub>BAT</sub> > 18 V or T <sub>A</sub> > 105°C Corresponds to Gains 4X - 128X
SID110B <sup>[28, 29]</sup>	I <sub>OFF_HIGH_V_T_LOW_I</sub>	Current channel input referred offset error Using ACHAN0 as current channel	-1.5	± 1	1.5	μV	I < 400 A and V <sub>BAT</sub> > 18 V or T <sub>A</sub> > 105°C Corresponds to Gains 256X and 512X
SID110C <sup>[28, 29]</sup>	I <sub>OFF_HIGH_V_T_HIGH_I</sub>	Current Channel Input referred offset error Using ACHAN0 as Current Channel	-224/ gain	± 176/ gain	224/ gain	μV	140 A < I < 3000 A and V <sub>BAT</sub> > 18 V or T <sub>A</sub> > 105°C Corresponds to Gains 4X - 128X

**Notes**

26.Current Channel Accuracy Error for a given shunt current (Iin) is calculated using the Gain Error (GE) from SID106/106A and Offset Error (IOFF) from SID108/109/110 with the formula: Accuracy Error = Iin \* GE ± IOFF.

27.For 0.1% & 0.15% voltage accuracy parts (-HV413, -HV423). See [Table 36](#).

28.For 0.25% voltage accuracy parts (-HV403). See the ordering information table.

29.Configuration: Continuous conversion mode for all valid data rates or incremental conversion with at least DR=64 and DR2=4. AAF enabled.

**Electrical specifications**

**Table 19** Current channel specifications (continued)

All the current channel specifications are valid with the automatic gain control (AGC) on, unless specified. Current channel refers to the voltage measurement across RSx shunt pins using ACHAN0 + DCHAN0 channel

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID111	I <sub>RES1</sub>	Resolution (current measurements)	–	0.715	–	mA	Gain = 512, typical shunt
SID111A	I <sub>RES1A</sub>	Resolution of accumulated current interrupt	–	0.715	–	mA	Gain = 512, typical shunt
SID112	I <sub>RES2</sub>	Resolution (voltage measurements)	–	36.6	–	μV	Differential, Gain = 1 Input range: –0.3 V to +1.2 V differential
SID113	I <sub>NOISE</sub>	Input referred noise	–	7	12	nVrms /√Hz	Gain = 512, equal to 4 mA rms with a 100 μΩ shunt at 1 ksps update rate
SID114	V <sub>IN,RSx</sub>	RSHx, RSLx differential input voltage range	–0.3	–	0.3	V	–
SID115	G <sub>PGA</sub>	Programmable gain	4	–	512	V/V	–
SID116	G <sub>OP</sub>	Fixed gain (voltage mode)	–	1	–	V/V	ADC Range: –0.3 V to +1.2 V differential
SID117	N <sub>ADC_LP_CUR</sub>	ADC digital channel resolution <sup>[30]</sup>	23	–	–	bits	No missing codes
SID120	f <sub>IUPDATE</sub>	Signal update rate output	0.75	–	48	ksps	Continuous measurement signal update rate range (for reference)
			–	1	–	–	Continuous measurements (DR=128, DR2=24)
			–	2	–	–	Typical use-case; continuous measurements (DR=128, DR2=12)
			–	4	–	–	Continuous measurements (DR=128, DR2=6)
			–	8	–	–	Continuous measurements (DR=64, DR2=6)
SID121	f <sub>IAF</sub>	Anti-alias LPF corner frequency	–	30	–	kHz	Guaranteed by design
SID122	R <sub>SHDIAG</sub>	Minimum shunt resistance.	10	–	–	kΩ	
SID122A	R <sub>SHDIAGA</sub>	Higher resistance is detected as an open circuit <sup>[31]</sup>	1	–	–	kΩ	V <sub>SH</sub> limit of ±0.05 V

**Notes**

30. Decimator output minimum data width is 23-bits to accommodate automatic gain of 4-512 while maintaining LSB with same weight regardless of trim (same mA/LSB); this is accomplished by weighting or shifting modulator output/decimator input by gain.

31. The current measurement channel detects disconnect shunt connections by switching internal pull-up resistors to the shunt pins. If the resistance between the RSHx or RSLx to ground is more than 10 kΩ, an open pin fault can be detected.

**Electrical specifications**

**4.3.5 Voltage channel**

**Table 20 Voltage channel specifications**

Voltage channel refers to the VSENSE, VDIAG voltage measurements with internal resistor divider using ACHAN1 + DCHAN1 channel.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID123 <sup>[32]</sup>	V <sub>RMEAS</sub>	HV measurement range	4	-	28	V	With HVATTEN = 24
SID124	V <sub>RMEASLV</sub>	LV measurement range	0	-	1.2	V	-
SID125 <sup>[33]</sup>	V <sub>ACC_1</sub>	Accuracy including lifetime and temperature drift	-0.5	-	0.5	%	3.6 V < V <sub>BAT</sub> ≤ 4.5 V, -40°C < T <sub>A</sub> < 125°C
SID125A <sup>[33]</sup>	V <sub>ACC_2</sub>		-0.25	±0.05	0.25	%	4.5 V < V <sub>BAT</sub> ≤ 28 V, -40°C < T <sub>A</sub> < 125°C
SID125B <sup>[33, 34]</sup>	V <sub>ACC_3.1</sub>		-0.25	±0.05	0.25	%	11 V < V <sub>BAT</sub> < 14 V, -40°C < T <sub>A</sub> < 85°C
SID126 <sup>[33, 35]</sup>	V <sub>ACC_3.2</sub>	Accuracy including lifetime and temperature drift	-0.15	±0.03	0.15	%	11 V < V <sub>BAT</sub> < 14 V, -40°C < T <sub>A</sub> < 85°C
SID126A <sup>[33, 36]</sup>	V <sub>ACC_3.3</sub>		-0.1	±0.03	0.1	%	11 V < V <sub>BAT</sub> < 14 V, -40°C < T <sub>A</sub> < 85°C
SID126B	V <sub>REF1</sub>	Primary high precision reference	-	1.2	-	V	Measured differentially between V <sub>REFH</sub> and V <sub>REFL</sub>
		Accuracy including lifetime and temperature drift	-0.15	-	0.15	%	0°C < T <sub>A</sub> ≤ 85°C; higher channel measurement accuracy is achieved through channel calibration.
			-0.2	-	0.2	%	-40°C < T <sub>A</sub> ≤ 0°C and 85°C ≤ T <sub>A</sub> < 125°C
SID126C <sup>[37]</sup>	V <sub>REF2</sub>	Secondary reference	-	1.2	-	V	-
		Accuracy including lifetime and temperature drift	-2	-	2	%	-
SID127	DNL_V	Differential non-linearity	-0.05	-	0.05	%	-
SID128	V <sub>RES</sub>	Resolution	-	0.293	-	mV	4 V - 18 V input range (RDIV = 16), V <sub>adc_range</sub> = 1.2 V, Gain = 1, V <sub>res</sub> = 16 x 1.2 / (2 <sup>16</sup> x 1) = 0.293 mV
SID129	V <sub>RES</sub>	Resolution	-	0.439	-	mV	4 V - 28 V input range (RDIV = 24), V <sub>adc_range</sub> = 1.2 V, Gain = 1, V <sub>res</sub> = 24 x 1.2 / (2 <sup>16</sup> x 1) = 0.439 mV
SID130	NOISE_V	Input referred noise	-	4	6	μVrms/√Hz	At 1 ksp/s update rate

**Notes**

- 32. HV measurement range can functionally support 0 to 4 V.
- 33. Accuracy includes the effect of leakage current of the 2.2 kΩ resistor as well as gain and offset errors. Measured with only one HV attenuator is enabled.
- 34. For 0.25% voltage accuracy part (-HV403). See [Table 36](#).
- 35. For 0.15% voltage accuracy part (-HV423). See [Table 36](#).
- 36. For 0.1% voltage accuracy parts (-HV413). See [Table 36](#).
- 37. Secondary reference with its associated ground can be measured as an input to the ADC (not available on V<sub>REFH</sub> and V<sub>REFL</sub> pins)

**Electrical specifications**

**Table 20 Voltage channel specifications (continued)**

Voltage channel refers to the VSENSE, VDIAG voltage measurements with internal resistor divider using ACHAN1 + DCHAN1 channel.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID131	N <sub>ADC_VOL</sub>	ADC resolution	16	–	–	Bits	No missing codes
SID134	f <sub>VUPDATE</sub>	Signal update rate output	0.75	–	48	ksps	Continuous measurement signal update rate range (for reference)
			–	1	–		Continuous measurements (DR=128, DR2=24)
			–	2	–		Typical use-case; continuous measurements (DR=128, DR2=12)
			–	4	–		Continuous measurements (DR=128, DR2=6)
			–	8	–		Continuous measurements (DR=64, DR2=6)
SID135	f <sub>VAF</sub>	Anti-Alias LPF corner frequency	–	30	–	kHz	For open circuit detection Guaranteed by design
SID136	T <sub>LATENCY_MUX</sub>	Measurement valid delay <sup>[38]</sup>	–	64.7	65.72	μs	See the reference manual "PACSS clock cycle equations" DR=64, DR2=0, Sinc3, AVG_MODE=0, OCOR_EN=GCOR_EN=FIR_EN=PP_EN=0 CLK_SYS=48 MHz, CLK_DSM=3.072 MHz
–			2587	–	μs	See the reference manual "PACSS clock cycle equations" DR=128, DR2=12, Sinc3, AVG_MODE=0, OCOR_EN=GCOR_EN=PP_EN=0, FIR_EN=1 FIR_taps = 4, CLK_SYS=48 MHz, CLK_DSM=3.072 MHz PACSS clock cycle time = 1087 μs Typ: 1087 μs + (FIR_taps - 1) * DR * DR2 / CLK_DSM = 2587 μs	
SID136B	t <sub>Phasedelay</sub>	Phase delay with the current channel	–	–	5	μs	Both channels have FIR enabled, Automatic gain control on current channel
SID137	HV <sub>ATTEN</sub>	High-voltage divider ratio for V <sub>SENSE</sub> , V <sub>DIAG</sub> inputs	–	16	–	V/V	Selectable under program control, includes 2.2-kΩ external resistor
SID137A	HV <sub>ATTEN</sub>	High-voltage divider ratio for V <sub>SENSE</sub> , V <sub>DIAG</sub> inputs	–	24	–	V/V	
SID138	R <sub>HVATTEN</sub>	HV resistance to V <sub>SSA</sub>	1.68	2.4	3.72	MΩ	–
SID139	I <sub>HVATTEN</sub>	HV divider off leakage	–	0	1	μA	V <sub>SENSE</sub> , V <sub>DIAG</sub> < 15 V

**Note**

38. First valid decimator output with a 3.072 MHz ADC clock with OSR=64 and decimator=Sinc3. Digital FIR filtering and averaging may add more latency.

**Electrical specifications**

**4.4 Digital peripherals**

**4.4.1 TCPWM**

**Table 21 TCPWM specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID140	$I_{TCPWM1}$	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID141	$I_{TCPWM2}$	Block current consumption at 12 MHz	–	–	155	μA	All modes (TCPWM)
SID142	$I_{TCPWM3}$	Block current consumption at 49.152 MHz	–	–	650	μA	All modes (TCPWM)
SID143	$f_{TCPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = $f_{SYSCLK}$ max = 49.152 MHz Guaranteed by design
SID144	$t_{TPWMENEXT}$	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Guaranteed by design
SID145	$t_{TPWMEXT}$	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs Guaranteed by design
SID146	$t_{CRES}$	Counter Resolution	1/Fc	–	–	ns	Minimum time between successive counts Guaranteed by design
SID147	$t_{PWMRES}$	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output Guaranteed by design
SID148	$t_{QRES}$	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Guaranteed by design

**4.4.2 LIN**

**Table 22 LIN specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID249	$f_{LIN}$	Internal clock frequency to the LIN block	–	–	2	MHz	Guaranteed by design
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	–
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	–

Electrical specifications

4.4.3 Serial communication block

Table 23 I<sup>2</sup>C DC specifications<sup>[39]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	150		–
SID151	I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	310		–
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	–	–	2		–

Table 24 I<sup>2</sup>C AC specifications<sup>[39]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	f <sub>I2C1</sub>	Bit rate	–	–	1	Msp/s	–

Table 25 SPI DC specifications<sup>[39]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID163	I <sub>SPI1</sub>	Block current consumption at 1 Mbps	–	–	360	μA	–
SID164	I <sub>SPI2</sub>	Block current consumption at 4 Mbps	–	–	560		–
SID165	I <sub>SPI3</sub>	Block current consumption at 8 Mbps	–	–	800		–

Table 26 SPI AC specifications<sup>[39]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID166	f <sub>SPI</sub>	SPI operating frequency (Master; 6X oversampling)	–	–	F <sub>c</sub>	MHz	F <sub>c</sub> max = f <sub>SYSCLK</sub> /6. F <sub>cpu</sub> maximum = 49.152 MHz

Note

<sup>39</sup>.Guaranteed by characterization.

**Electrical specifications**

**Table 27 SPI Master mode AC specifications<sup>[40]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID167	$t_{DMO}$	MOSI valid after SClk driving edge	–	–	15	ns	–
SID168	$t_{DSI}$	MISO valid before SClk capturing edge	20	–	–		Full clock, late MISO sampling
SID169	$t_{HMO}$	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge

**Table 28 SPI Slave mode AC specifications<sup>[40]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID170	$t_{DMI}$	MOSI valid before SClk capturing edge	30	–	–	ns	–
SID171	$t_{DSO}$	MISO valid after SClk driving edge	–	–	48+ 3* $T_{SCB}$		–
SID171A	$t_{DSO\_EXT}$	MISO valid after SClk driving edge in Ext. Clk mode	–	–	48		–
SID172	$t_{HSO}$	Previous MISO data hold time	0	–	–		–
SID172A	$t_{SSELSSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

**Table 29 UART DC specifications<sup>[40]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID160	$I_{UART1}$	Block current consumption at 100 Kbps	–	–	60	$\mu A$	–
SID161	$I_{UART2}$	Block current consumption at 1000 Kbps	–	–	320	$\mu A$	–

**Table 30 UART AC specifications<sup>[40]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID162	$f_{UART}$	Bit rate	–	–	1	Mbps	–

**Note**  
40. Guaranteed by characterization.

**Electrical specifications**

**4.4.4 SWD interface**

**Table 31 SWD interface specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID213	f <sub>SWDCLK</sub>	SWD clock input frequency	–	–	14	MHz	f <sub>SWDCLK</sub> ≤ 1/3 f <sub>CPU</sub>
SID215 <sup>[41]</sup>	t <sub>SWDI_SETUP</sub>	SWDI setup time	0.25*T	–	–	ns	T = 1/f <sub>SWDCLK</sub>
SID216 <sup>[41]</sup>	t <sub>SWDI_HOLD</sub>	SWDI hold time	0.25*T	–	–		T = 1/f <sub>SWDCLK</sub>
SID217 <sup>[41]</sup>	t <sub>SWDO_VALID</sub>	SWDO valid time	–	–	0.5*T		T = 1/f <sub>SWDCLK</sub>
SID217A <sup>[41]</sup>	t <sub>SWDO_HOLD</sub>	SWDO hold time	1	–	–		T = 1/f <sub>SWDCLK</sub>

**4.5 Memory**

**Table 32 Flash AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID174	t <sub>ROWWRITE</sub> <sup>[42]</sup>	Row (block) write time (erase and program)	–	–	24	ms	Row (block) = 128 bytes
SID175	t <sub>ROWERASE</sub> <sup>[42]</sup>	Row erase time	–	–	17		
SID176	t <sub>ROWPROGRAM</sub> <sup>[42]</sup>	Row program time after erase	–	–	7		
SID178	t <sub>BULKERASE</sub>	Bulk erase time (32 KB)	–	–	35		–
SID180 <sup>[43]</sup>	t <sub>DEVPROG</sub> <sup>[42]</sup>	Total device program time	–	–	8	s	Using Bulk Erase + Program Row APIs
SID181 <sup>[43, 44]</sup>	F_END	Flash endurance	100 K	–	–	Cycles	
SID182	F_RET	Flash retention.	15	–	–	years	Guaranteed by characterization. T <sub>A</sub> ≤ 105 °C, 10K P/E cycles, ≤ three years at T <sub>A</sub> ≥ 85 °C
SID183	t <sub>RESUMESYSCALL</sub>	Time for non-blocking system calls to be resumed	–	–	25	ms	Non-blocking system calls should be used only for data flash
SID256	WS48	Number of Wait states at 49.152 MHz	3	–	–	–	CPU execution from Flash
SID257	WS36	Number of Wait states at 36 MHz	2	–	–	–	CPU execution from Flash Guaranteed by design
SID258	WS24	Number of Wait states at 24.576 MHz	1	–	–	–	CPU execution from Flash. Guaranteed by design
SID259	WS12	Number of Wait states at 12 MHz	0	–	–	–	CPU execution from Flash. Guaranteed by design

**Notes**

41. Guaranteed by design.

42. It can take as much as 24 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

43. Guaranteed by characterization.

44. Data flash: 100k cycles per row with cyclical write; Code flash: 100k cycles total

**Electrical specifications**

**4.6 System resources**

**Table 33 Power-on reset (PRES)**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID185	V <sub>I</sub> POR_VDD	POR trip voltage for V <sub>DD</sub>	0.7	–	1.5	V	–

**Table 34 Brown-out detect (BOD) for V<sub>DD</sub>, V<sub>CCD</sub>**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID190	V <sub>DD</sub> _BOD	BOD trip voltage for V <sub>DD</sub>	2.34	–	2.63	V	–
SID190A	V <sub>CCD</sub> _BOD	BOD trip voltage for V <sub>CCD</sub>	1.64	–	1.74		–
SID190B	V <sub>CCD</sub> _BOD_DPSLP	BOD trip voltage for V <sub>CCD</sub> in Deep Sleep	1.1	–	1.5		–

**Table 35 Overvoltage detect (OVD) for V<sub>DD</sub>, V<sub>CCD</sub>**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID192	V <sub>DD</sub> _OVD	OVD trip voltage for V <sub>DD</sub>	3.62	–	3.96	V	–
SID192A	V <sub>CCD</sub> _OVD	OVD trip voltage for V <sub>CCD</sub>	1.97	–	2.17		–

**Ordering information**

## 5 Ordering information

The marketing part numbers for the PSOC™ 4 HVPA devices are listed in [Table 36](#).

**Table 36 PSOC™ 4 HVPA-144K ordering information**

Product	Features											Packages	Operating Temp	Silicon ID	
	Max CPU speed (MHz)	Code Flash (KB) with ECC	SRAM (KB) with ECC	Data flash (KB) with ECC	SFlash (KB) for storing constants	16-20 bit precision ΔΣ ADC	Voltage measurement accuracy	TCPWM blocks	LIN blocks	SCB	High-voltage subsystem (LDO, LIN PHY)				GPIO
CY8C4126LCE-HV403	24.576	64	4	8	1	2	0.25%	4	1	1	Y	9	Y	Y	0x320026C2
CY8C4126LCE-HV413	24.576	64	4	8	1	2	0.1% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320126C2
CY8C4126LCE-HV423	24.576	64	4	8	1	2	0.15% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320226C2
CY8C4127LCE-HV403	24.576	128	8	8	1	2	0.25%	4	1	1	Y	9	Y	Y	0x320326C2
CY8C4127LCE-HV413	24.576	128	8	8	1	2	0.1% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320426C2
CY8C4127LCE-HV423	24.576	128	8	8	1	2	0.15% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320526C2
CY8C4147LCE-HV403	49.152	128	8	8	1	2	0.25%	4	1	1	Y	9	Y	Y	0x320926C2
CY8C4147LCE-HV413	49.152	128	8	8	1	2	0.1% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320A26C2
CY8C4147LCE-HV423	49.152	128	8	8	1	2	0.15% <sup>[45]</sup>	4	1	1	Y	9	Y	Y	0x320B26C2

The nomenclature used in [Table 37](#) is based on the following part numbering convention:

**Table 37 Part number nomenclature**

Field	Description	Values	Meaning
CY8C	Cypress prefix, an Infineon company	-	-
4	Architecture	4	PSOC™ 4
A	Family	1	4100 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	6	64 KB
		7	128 KB
DE	Package code	LC	QFN with wettable flanks
F	Temperature range	E	Automotive (-40°C to +125°C)
S	Series designator	HV	PSOC™ 4 High voltage series
XYZ	Attributes code	000-999	Code of feature set in the specific family

**Note**

45.11 V < V<sub>BAT</sub> < 14 V, -40°C < T<sub>A</sub> < 85°C.

**Packaging**

## 6 Packaging

The PSOC™ 4 HVPA device is offered in a 32-QFN package. Package dimensions and Infineon drawing numbers are in [Table 38](#) to [Table 41](#).

**Table 38 Package list**

Spec ID#	Package	Description	Package diagram
BID20	32-pin QFN with wettable flanks	6 × 6 × 1 mm height with 0.5 mm pitch	002-29344

**Table 39 Package thermal characteristics<sup>[46]</sup>**

Parameter	Description	Package	Min	Typ	Max	Unit
T <sub>A</sub>	Operating ambient temperature	–	–40	25	125	°C
T <sub>J</sub>	Operating junction temperature	–	–40	–	150	°C
T <sub>JA</sub>	Package θ <sub>JA</sub>	32-pin QFN	–	–	15.1	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub>	32-pin QFN	–	–	1.2	°C/Watt

**Table 40 Solder reflow peak temperature**

Package	Maximum peak temperature	Maximum time at peak temperature
32-pin QFN	260°C	30 seconds

**Table 41 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020**

Package	MSL
32-pin QFN	MSL 3

**Note**

46. Simulated value, four-layered PCB per JESD51-7.

Packaging

6.1 Package diagram

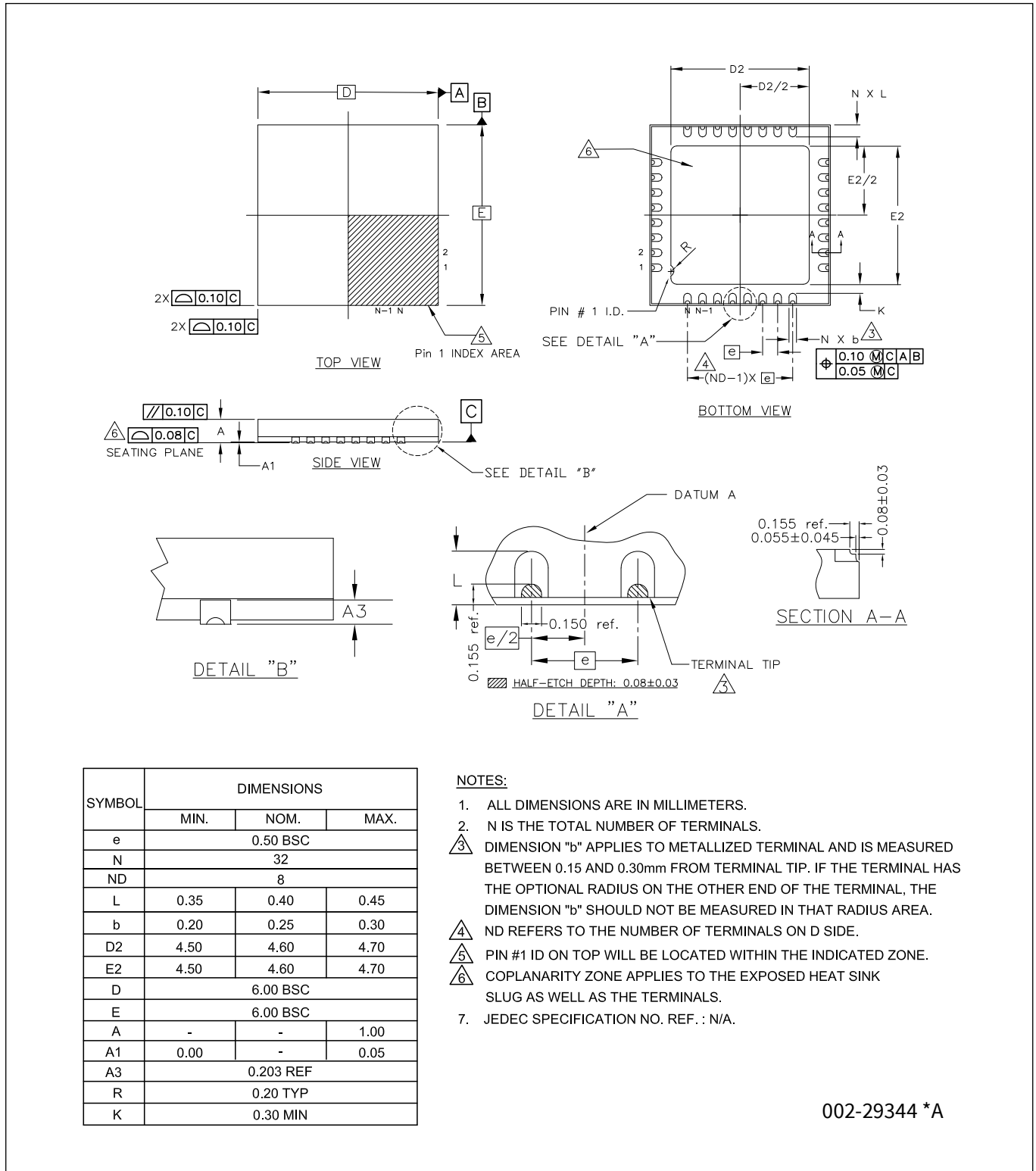


Figure 24 32-pin QFN (6.0X6.0X1.0 mm) LV32B, (4.60X4.60 mm) EPAD (Dimple wettable flank, SAW type) (PG-VQFN-32)

**Acronyms**

## 7 Acronyms

**Table 42 Acronyms used in this document**

<b>Acronym</b>	<b>Description</b>
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR

**Acronyms**

**Table 42** Acronyms used in this document *(continued)*

<b>Acronym</b>	<b>Description</b>
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSOC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub

**Acronyms**

**Table 42** Acronyms used in this document *(continued)*

<b>Acronym</b>	<b>Description</b>
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSOC™	Programmable System-on-Chip
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier

**Acronyms**

**Table 42**      **Acronyms used in this document** *(continued)*

<b>Acronym</b>	<b>Description</b>
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSOC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## **8 Document conventions**

### **8.1 Unit of measure**

**Table 43 Unit of measure**

<b>Symbol</b>	<b>Unit of measure</b>
°C	degrees celsius
dB	decibel
fF	femtofarad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilo-ohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohm
pF	picofarads
ppm	parts per million
ps	picoseconds
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Revision history

Document revision	Date	Description of changes
**	2019-11-07	New datasheet for new device family
*A	2020-03-24	<p>Changed 'Programmable Analog' to 'Precision Analog'. Added 'Challenge Response functionality'. <b>Lifetime counter: A 32-bit lifetime counter with a prescaler (/2 to /32) is available and triggered from the PILO clock. This counter runs in all modes and can be reset by POR. With the prescaler, the net resolution of the counter becomes 37-bit causing an overflow every 50 days. The counter will continue counting upon overflow</b> Changed description with correct values. Updated <b>Watchdog timers (WDT)</b> Updated <b>Table 2, Table 3</b> Added <b>Section 1.4</b> for LIN Block features. Updated text in <b>Section 1.7</b>. Updated <b>Figure 6</b> Updated all figures in <b>Section 1.8</b>. Fixed typo in dVBE formula ('t' --&gt; 'T') in <b>Section 1.8.6</b>. Updated <b>Pinouts</b> based on planned implementation Updated <b>Packaging</b> based on latest package specification. Updated power system block diagram in <b>Section 1.2</b>. Update bypass capacitor values in <b>Section 1.2</b>.</p> <p><b>Electrical specifications:</b> SIDA13A - Added supply current absolute max SID4A - I<sub>SH</sub>: Added nominal specs for V<sub>SENSE</sub>/V<sub>DIAG</sub> current SID7A - I<sub>CS</sub>: Added nominal specs for R<sub>SH</sub>/R<sub>SL</sub>/R<sub>SH2</sub>/R<sub>SL2</sub> current SID19 - Added unit 'µA' SID27 - Changed I<sub>DD</sub> spec to include regulator current including core SID27A - Added I<sub>DDGPIQ</sub> spec to capture regulator current only for GPIOs SID47 - Added unit 'ms' SID48 - Added unit 'ms' SID49 - Changed parameter name from F<sub>GPIOUT1</sub> to F<sub>GPIOUTF</sub> (Fast strong mode) SID50 - Changed parameter name from F<sub>GPIOUT3</sub> to F<sub>GPIOUTS</sub> (Slow strong mode) SIDL62 - Removed LIN Output voltage spec SIDL76 - Added max for V<sub>OH</sub> -&gt; LIN Bus transmitted recessive output voltage SIDL83 - Added unit 'kΩ' SIDL84 - Added formula for duty cycle calculation (D1) in 'conditions' SIDL85 - Added formula for duty cycle calculation (D2) in 'conditions' SIDL86 - Added formula for duty cycle calculation (D3) in 'conditions' SIDL87 - Added formula for duty cycle calculation (D4) in 'conditions' SID106 - Added typical value (TBD) for current channel accuracy SID106A - Added typical value (TBD) for current channel accuracy SID112 - Added ADC Range for resolution (under 'conditions') SID122A - Added new spec for Shunt disconnect threshold for a limited V<sub>SH</sub> SID125 - Added typical value (TBD) for voltage channel accuracy SID126 - Added typical value (TBD) for voltage channel accuracy SID126A - Added typical value (TBD) for voltage channel accuracy SID129 - Added unit 'mV' SID131 - Added 'No missing codes' under 'conditions' SID173 - Removed V<sub>PE</sub> spec (Erase and Program Voltage) SID249 - Updated max value SIDA13 - Updated max value SID99 - Updated min value SID9 - Updated max value SID.CLK#6 - Updated to SID184. Removed SID214 SID21 - Updated max value SID57 - Added conditions Added spec SID57A (New HPOSC accuracy spec for T<sub>A</sub> &gt;105 °C) SID42 - Changed unit from mV to V SID43 - Added conditions SIDX6 - Added conditions SID166 - Updated spec and conditions</p>

**Revision history**

<b>Document revision</b>	<b>Date</b>	<b>Description of changes</b>
*A (Contd.)	2020-03-24	Added SID137A SID35 - Updated max value SID45 and SID46 - Updated min value SID170 - Updated min value SID176 - Updated max value Updated <b>XRES DC specifications</b> and <b>XRES AC specifications</b> . Updated <b>Power-on reset (PRES)</b> , <b>Brown-out detect (BOD) for VDDD</b> , <b>VCCD</b> , and <b>Overvoltage detect (OVD) for VDDD, VCCD</b> .
*B	2020-08-07	Updated <b>Digital channel data path</b> . Updated <b>Figure 1</b> and added <b>Table 1</b> . Updated values and conditions for the following spec IDs: SIDA2, SID9, SID12, SID13, SID43, SIDX6, SID99, SID110, SID118, SID119, SID120, SID132, SID133, SID134, SID175. Added SID12A and SID13A. Added footnote for SIDA13A. Removed SID184. Updated <b>Ordering information</b> .
*C	2020-08-19	Updated ROM to 16 KB in . Updated <b>R1/C1 max current specifications</b> . Updated <b>Alternate pin functions</b> Updated footnote 3. Updated <b>Package thermal characteristics[46]</b> .
*D	2020-11-12	Updated ROM to 32 KB in . Updated <b>PACSS sequencer and timing</b> . Updated <b>Figure 22</b> . Updated number of GPIOs. Updated <b>CPU and memory subsystem</b> . Updated <b>Pinouts</b> . Updated SID4A parameter name. Added SID9A. Removed min value for SID11. Updated min and max values for SID28. Updated SID49, SID50, SID51 descriptions. Updated conditions for SID97, SID101, SID103. Updated conditions for SID102, SID136, and SID174. Added SID103A and SID136A. Added footnotes for SID181, SID125, SID126, SID126A. Added spec SID190B. Updated T <sub>JC</sub> for SID301. Added specs SID302, 303, 304, and 305. Added <b>Diagnostic channel specifications[27]</b> . Added Sflash column in <b>Ordering information</b> . Updated T <sub>JC</sub> value in <b>Package thermal characteristics[46]</b> . Added footnote for T <sub>JA</sub> in <b>Package thermal characteristics[46]</b> .
*E	2021-01-22	Updated the title to PSOC 4 HV Precision Analog 144 K Datasheet. Updated ILO clock source information in <b>Features</b> . Changed VDD references to VDDD. Updated min value for SIDL76. Updated typ and max values for SID122 and SID122A. Updated SID126B and SID126C. Updated conditions for SID139. Added SID178. Updated description for SID258. Parameter names aligned with the internal documentation.
*F	2021-04-07	<b>System resources</b> Added <b>Sample application schematic</b> . Updated “guaranteed by design” note for the relevant electrical specs. Updated <b>Absolute maximum ratings</b> and <b>Operating current and wakeup times</b> : - SID12A, SID13A: Updated conditions - SIDA2: Update pin list for system-level ESD - SIDA24, SIDA24A: New specifications added for defining short circuit tolerance on the HVREG and LIN pins - SID26: Corrected the min Vbat condition.

**Revision history**

<b>Document revision</b>	<b>Date</b>	<b>Description of changes</b>
*G	2021-05-11	<p>Added footnote for <b>Alternate pin functions</b>.  Updated <b>Table 2</b>.  Updated <b>PACSS measurement/acquisition system</b>.  Updated <b>ESD protection</b>.  Updated <b>Sample application schematic</b>.  Removed conditions for SID54.  Updated min and max values for SIDL83.  Updated conditions for SID305.  Added footnote for SID15A, SID16A, SID17A, and SID18A.  Updated conditions for SID112.  Updated description for SID213.  Updated max value and conditions for SID302.  Updated <b>Flash AC specifications</b> - added new spec SID183.</p>
*H	2022-09-22	<p>Updated to Infineon template.  Added details about ADC channel digital backend in <b>Digital channel data path</b>.  Updated <b>Temperature sensor</b>.  Updated <b>Clock system</b> and <b>Local interconnect network (LIN) block</b>.  Updated <b>Sample application schematic</b>.  Updated <b>Figure 7</b> and <b>Figure 9</b>.  Updated <b>Table 16, Table 17, Table 18, Table 19</b>.  Updated <b>Figure 16, Figure 20, Figure 22</b>.  Updated <b>Electrical specifications</b>:  SIDA2 - Updated description  SIDA24, 24A - Added footnotes  SID2 - Updated values  SID2A - New spec  SID7E - Updated values  SID7F - New spec  SID12, 12A, 13, 13A - Updated values &amp; conditions  SID15A, 16A, 17A, 18A - Updated values &amp; conditions  SID19 - Updated values  SID21 - Updated Unit  SID40 - Updated values  SID43 - Updated conditions  SIDX6 - Updated conditions  SID53 - Updated values &amp; footnotes  SID54 - Updated conditions  SID54A, 55A, 59A - New specs  SID55, SID59, SID60- Added footnotes  SIDL84, 85 - Updated conditions  SIDL84A, 85A - New specs  SID97, 103 - Updated conditions  SID97A, 99A - New spec  SID99, 102A - Removed specs  SID101 - Updated values &amp; conditions  SID302 - Updated values &amp; conditions  SID303, 303A, 303B, 303C, 303E - New specs  SID105 - Updated values &amp; conditions  SID106, 106A - Updated description &amp; values  SID108, 109, 108A, 109A, 110, 110A, 110B, 110C - New specs  SID111, 111A - Updated values  SID112, 116 - Updated conditions  SID118, 119 - Removed specs  SID120 - New specs  SID122, 122A - Updated description, values &amp; conditions  SID125, 125A, 125B, 126, 126A - New &amp; updated specs  SID126B, SID128, 129 - Updated values &amp; conditions  SID132, 133 - Removed specs  SID134 - New specs  SID136A - Updated conditions  SID138 - Updated values  SID142 - Updated values  SID213 - Updated description  SID174, 175, 180 - Updated values &amp; conditions  SID182 - Updated description</p>

**Revision history**

<b>Document revision</b>	<b>Date</b>	<b>Description of changes</b>
*I	2023-03-01	Updated <b>Sample application schematic</b> . Updated specs SID55A, SID59A, SID97, 102, 103A, 303, 303A, 303B, 303C, 303D, 303E, 305, 108, 108A, 109A, 110B, 110C, 136, 136A. Changed conditions for SID54, 54A, 55, 55A, 102, 305, 125A, 128, 129, 136, 136A. Added SID57A and SID60A. Added silicon ID information in <b>Ordering information</b> . Added <b>Revision history</b> . Changed datasheet status to Final.
*J	2023-09-21	Updated <b>Features</b> . Updated the number of GPIOs to 9. Updated <b>Pinouts</b> . Added min/max specs for SID55A, 57A, 59A, 60A, 108A, 109A, 110B, 110C. Updated temperature accuracy spec - SID97. Added typ values - SID302, 305, 113, 130. Updated PILO spec - SID60A. Removed SID303C, 303D, 303E & covered through SID303, 303A, 303B for all 3 device variants. Added Errata ID 24.
*K	2024-03-19	Updated “Functional safety” features. Changed HV PA to HVPA throughout the document. Changed lifetime counter prescaler value to /2. Updated <b>Alternate pin functions</b> . Updated SID15A.3, SID17A.3, and removed SID18A. Removed SID16A. Updated typ value of SID97a. Updated typ, max values and conditions for SID102. Updated typ and max values and conditions for SID136 and SID136A. Updated package diagram. Updated Silicon ID in <b>Ordering information</b> . Updated workaround for Errata item 7.
*L	2026-05-01	Removed Errata section. Updated PSoC™ to PSOC™ at all instances in the document. Updated document to standard datasheet template. Updated all images aligning to Infineon branding guidelines. Changed UltraLite to High-voltage in <b>Block diagram</b> .

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