Military 1 Mb (128K × 8) Static RAM

Features

- Pin- and function-compatible with the industrial version of CY7C1018CV33 and CY7C1019CV33
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 60 mA @ 10 ns
- Low CMOS standby power
  - I_{SB2} = 3 mA
- 2.0 V data retention
- 100% tested to military temperature range –55°C to 125°C
- Automatic power down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Available in Pb-free 32L SOJ 400 MILS V32.4 (molded SOJ V33) package

Functional description

CY7C1019DV33 is a high-performance CMOS Static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a High-Z state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

CY7C1019DV33 is available in Pb-free 32L SOJ 400 MILS V32.4 (molded SOJ V33) package.

Logic block diagram

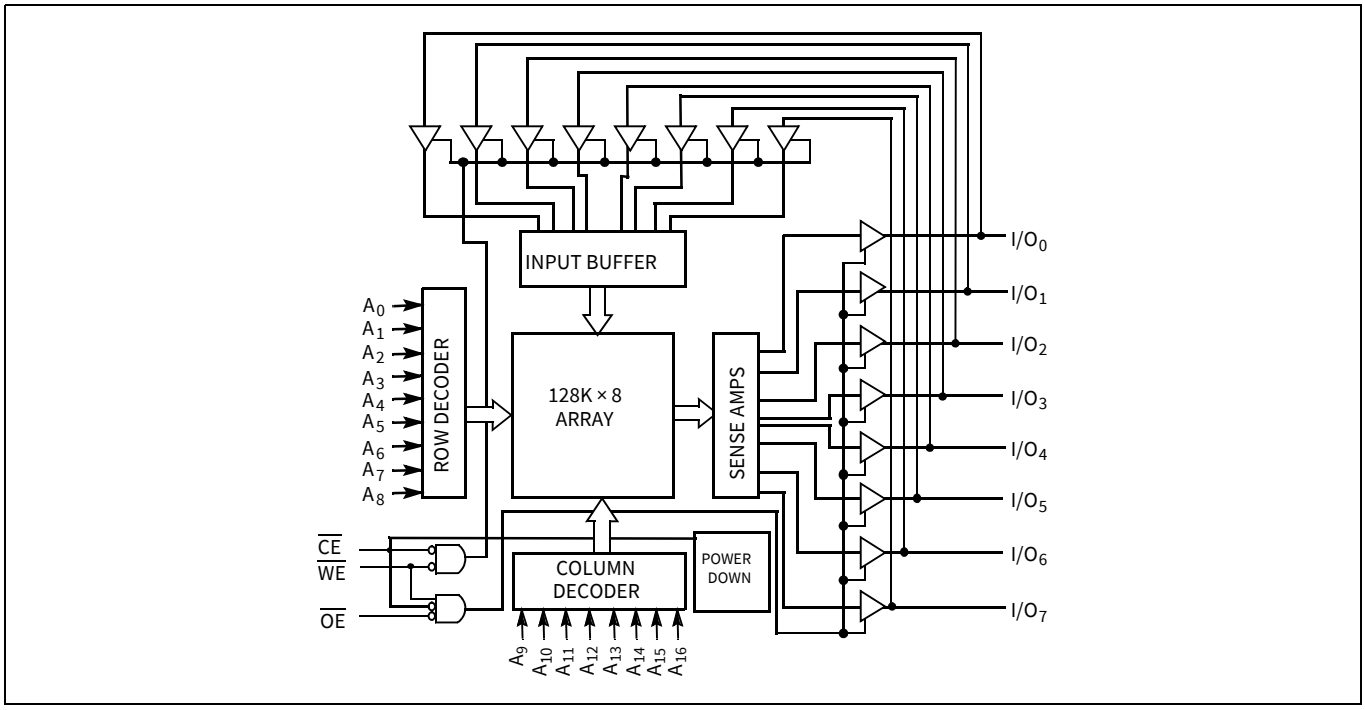


Table of contents

1 Selection guide

Description	-10 (Military)	Unit
Maximum access time	10	ns
Maximum operating current	60	mA
Maximum standby current	3	

2 Pin configurations

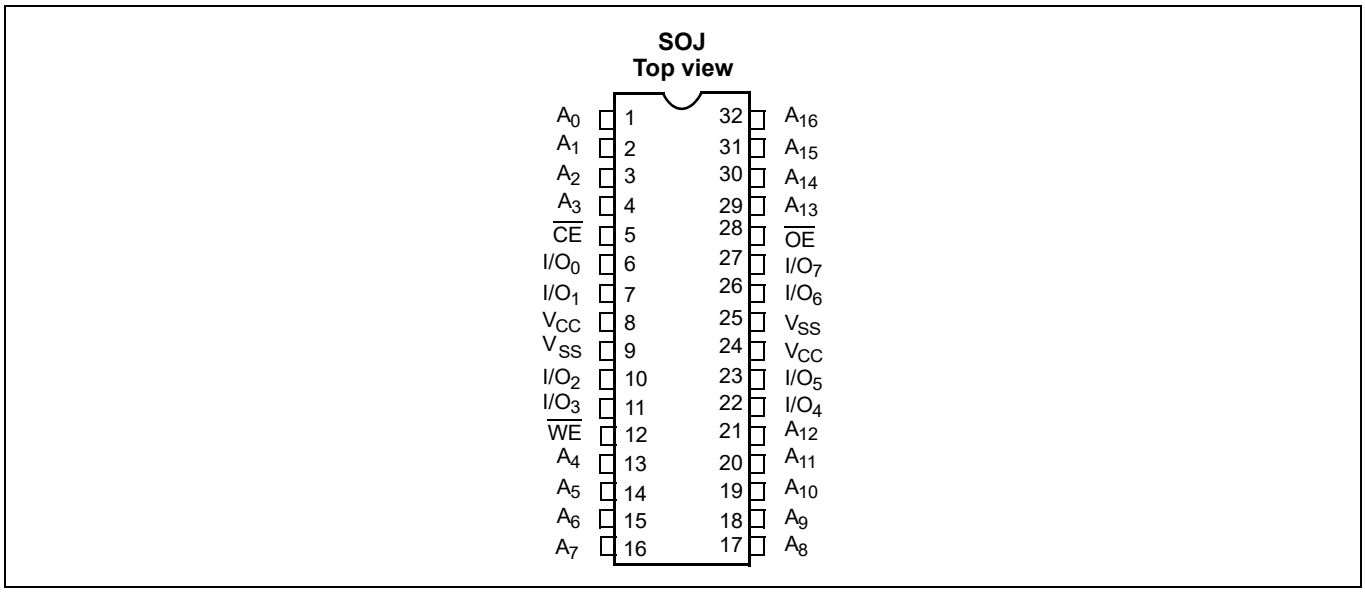


Figure 1 32L SOJ (top view)

3 Maximum ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65°C to +150°C
Ambient temperature with power applied	–55°C to +125°C
Supply voltage on V_{CC} to relative GND[1]	–0.3 V to +4.6 V
DC voltage applied to outputs in High-Z state[1]	–0.3 V to V_{CC} + 0.3 V
DC input voltage[1]	–0.3 V to V_{CC} + 0.3 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001 V
Latch-up current	> 200 mA

Note

1. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 5 ns.

4 Operating range

Range	Ambient temperature	V_{CC}	Speed
Military	–55°C to +125°C	3.3 V ± 0.3 V	10 ns

5 Electrical characteristics

Over the operating range

Parameter	Description	Test conditions		-10 (Military)		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA		–	0.4	
V_{IH}	Input HIGH voltage	–		2.0	V_{CC} + 0.3	
V_{IL}	Input LOW voltage[2]			–0.3	0.8	
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{IN} ≤ V_{CC}, output disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	60	mA
			83 MHz		55	
			66 MHz		45	
			40 MHz		30	
I_{SB1}	Automatic CE power down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	10	
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0			3s	

Note

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 5 ns.

6 Capacitance

Parameter[3]	Description	Test conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25°C, f = 1\ MHz, V_{CC} = 3.3\ V$	8	pF
C_{OUT}	Output capacitance		8	

Note
3. Tested initially and after any design or process changes affects these parameters.

7 Thermal resistance

Parameter[4]	Description	Test conditions	32L SOJ	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	56.29	°C/W
Θ_{JC}	Thermal resistance (junction to case)		38.14	

Note
4. Tested initially and after any design or process changes affects these parameters.

8 AC test loads and waveforms

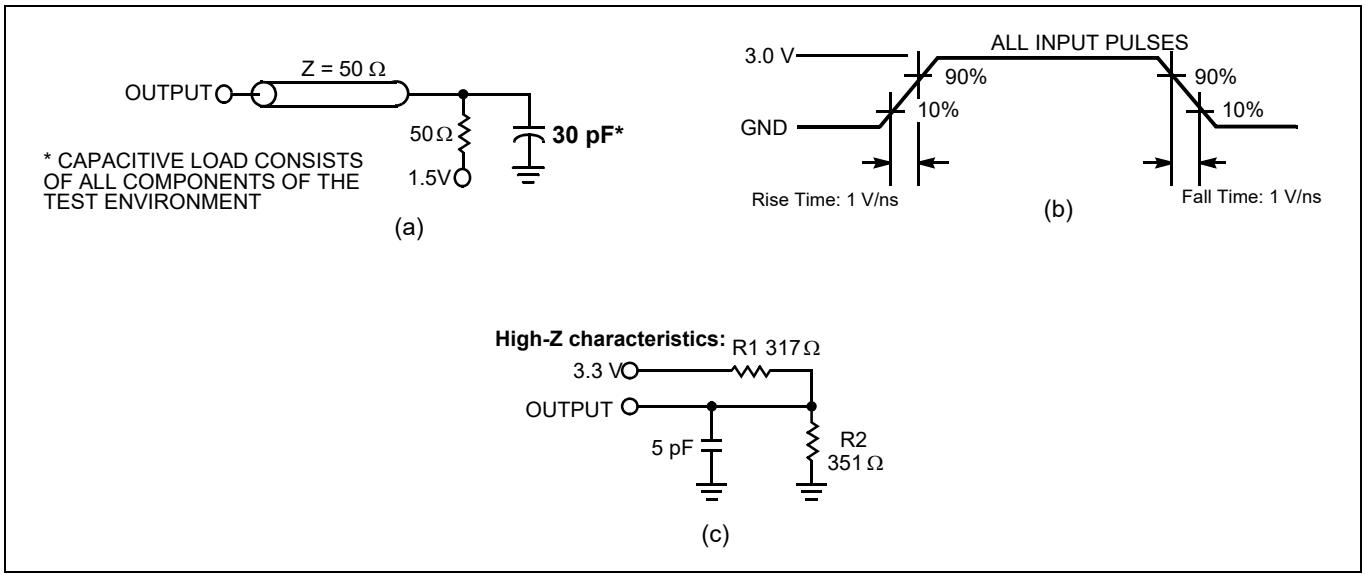


Figure 2 AC test loads and waveforms[5]

Note

5. AC characteristics (except High-Z) are tested using the load conditions shown in **Figure 2** (a). High-Z characteristics are tested for all speeds using the test load shown in **Figure 2** (c).

9 Data retention characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\,V, \overline{CE} \geq V_{CC} - 0.3\,V,$ $V_{IN} \geq V_{CC} - 0.3\,V$ or $V_{IN} \leq 0.3\,V$	–	3	mA
t_{CDR} [6]	Chip deselect to data retention time	–	0	–	ns
t_R [7]	Operation recovery time		t_{RC}		

Notes

6. Tested initially and after any design or process changes affects these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\,\mu s$ or stable at $V_{CC(min)} \geq 50\,\mu s$.

10 Data retention waveform

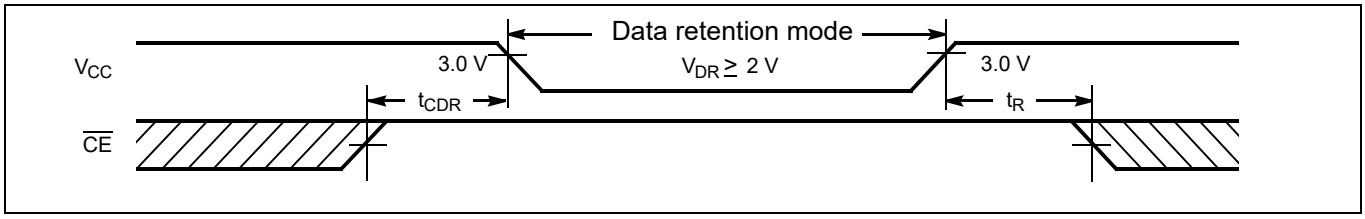


Figure 3 Data retention waveform

11 Switching characteristics

Over the operating range

Parameter[8]	Description	-10 (Industrial)		Unit
		Min	Max	
Read cycle				
t_{power}[9]	V_{CC} (typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	
t_{OHA}	Data hold from address change	3	–	
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	
t_{DOE}	$\overline{OE}$ LOW to data valid		5	
t_{LZOE}[10]	$\overline{OE}$ LOW to Low-Z	0	–	
t_{HZOE}[10, 11]	$\overline{OE}$ HIGH to High-Z	–	5	
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[10]	3	–	
t_{HZCE}[10, 11]	$\overline{CE}$ HIGH to High-Z	–	5	
t_{PU}[12]	$\overline{CE}$ LOW to power-up	0	–	
t_{PD}[12]	$\overline{CE}$ HIGH to power-down	–	10	
Write cycle[13, 14]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8		
t_{AW}	Address set-up to write end	8		
t_{HA}	Address hold from write end	0		
t_{SA}	Address set-up to write start	0		
t_{PWE}	$\overline{WE}$ pulse width	7		
t_{SD}	Data setup to write end	5		
t_{HD}	Data hold from write end	0		
t_{LZWE}[10]	$\overline{WE}$ HIGH to Low-Z	3		
t_{HZWE}[10, 11]	$\overline{WE}$ LOW to High-Z	–	5	

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in **Figure 2** (c). Transition is measured when the outputs enter a High-Z state.
12. This parameter is guaranteed by design and is not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

12 Switching waveforms

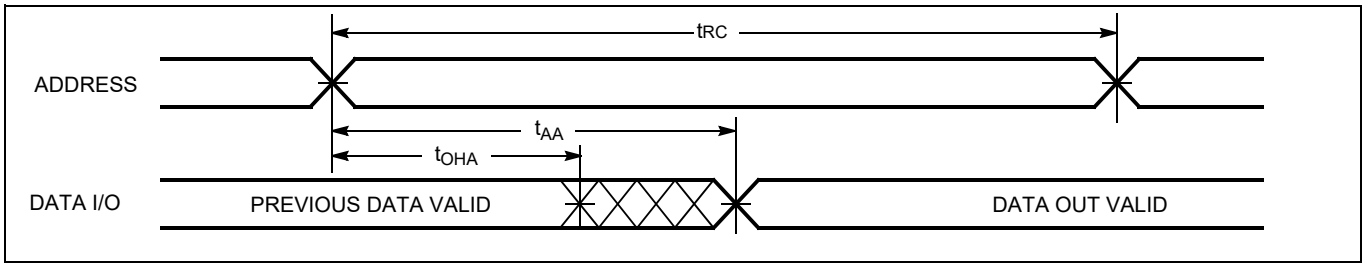


Figure 4 Read cycle no. 1 (address transition controlled)[15, 16]

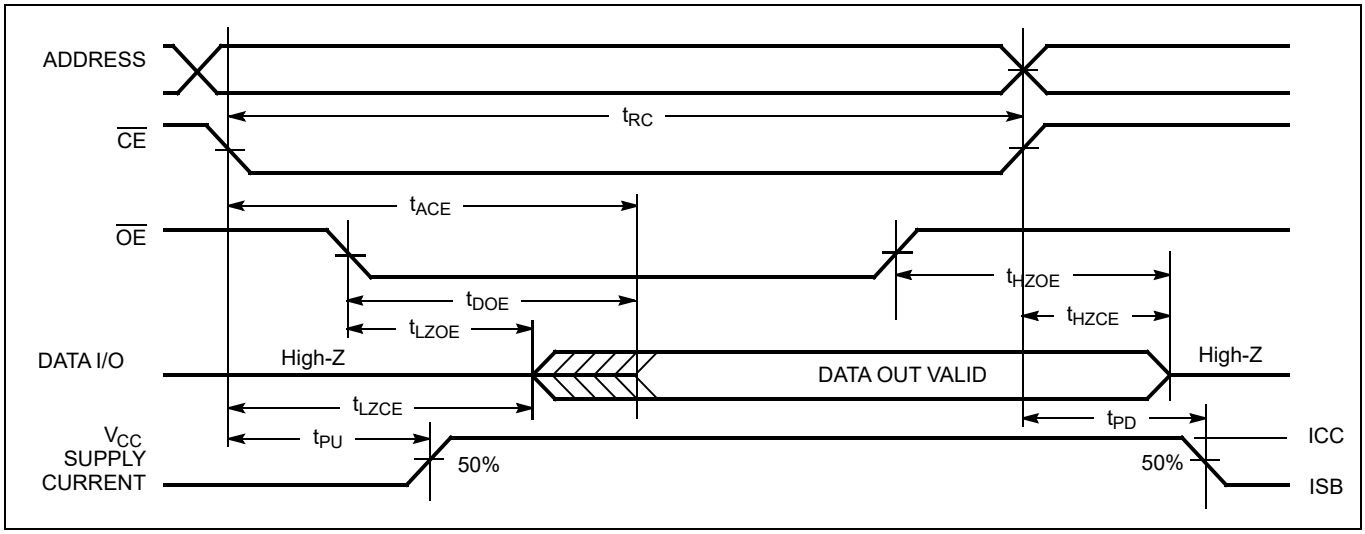


Figure 5 Read cycle no. 2 ($\overline{OE}$ controlled)[16, 17]

Notes
15. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching waveforms

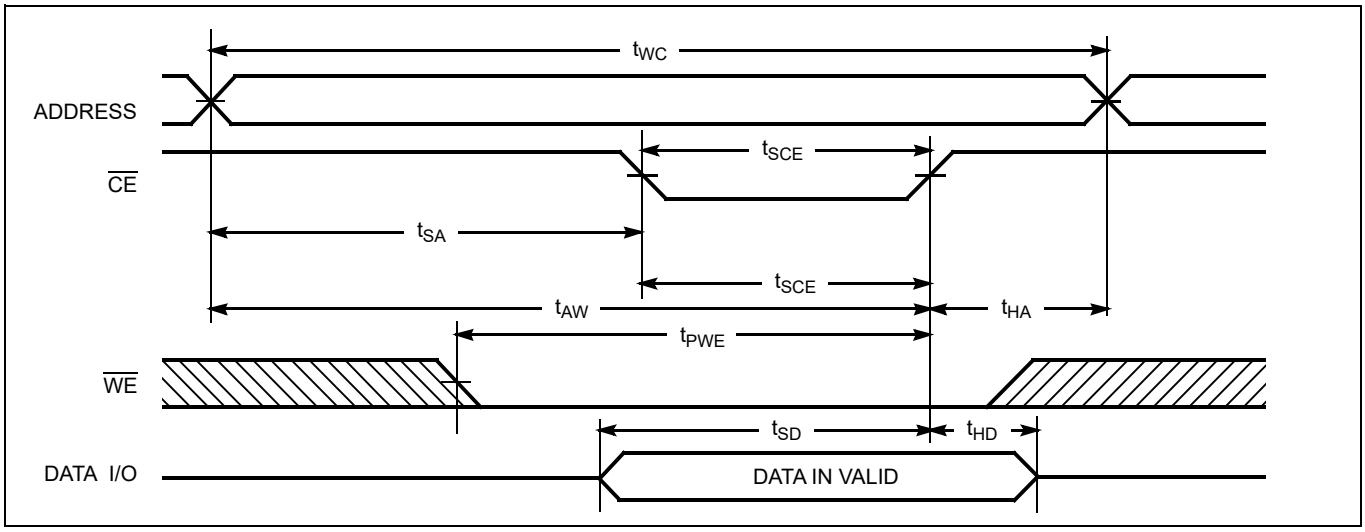


Figure 6 Write Cycle no. 1 (CE controlled)[18, 19]

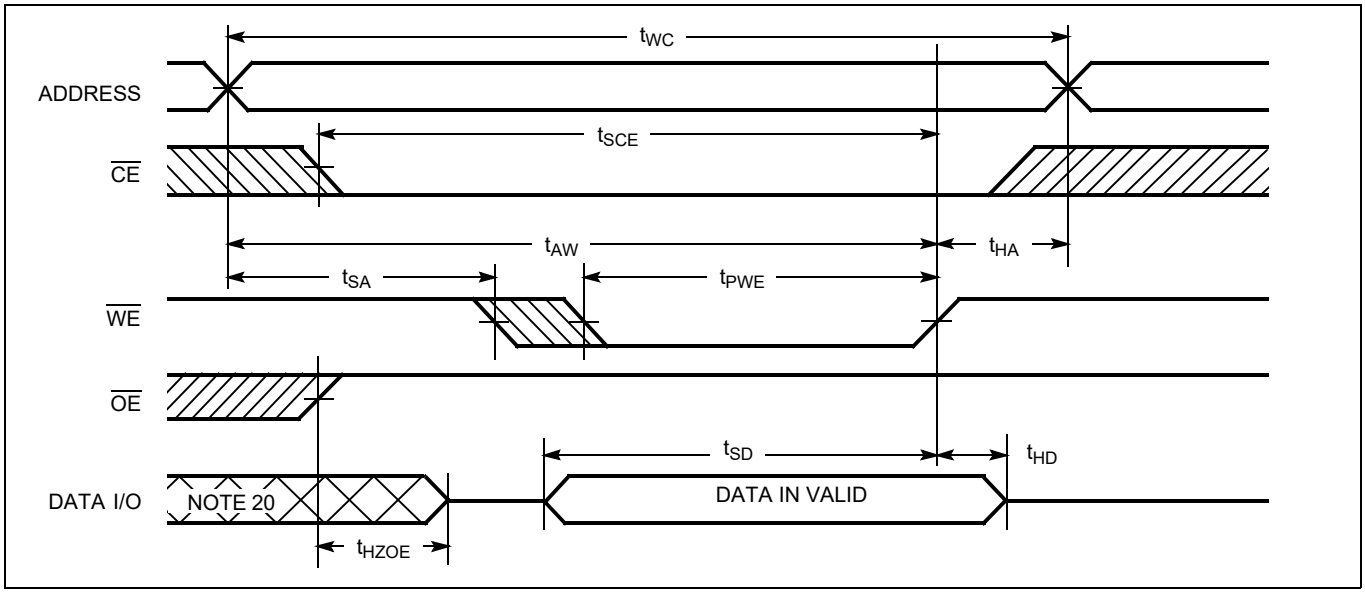


Figure 7 Write Cycle no. 2 (WE controlled, OE HIGH during write)[18, 19]

Notes
18. Data I/O is High-Z if OE = VIH.
19. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a state.
20. During this period, the I/Os are in the output state and input signals are not applied.

Switching waveforms

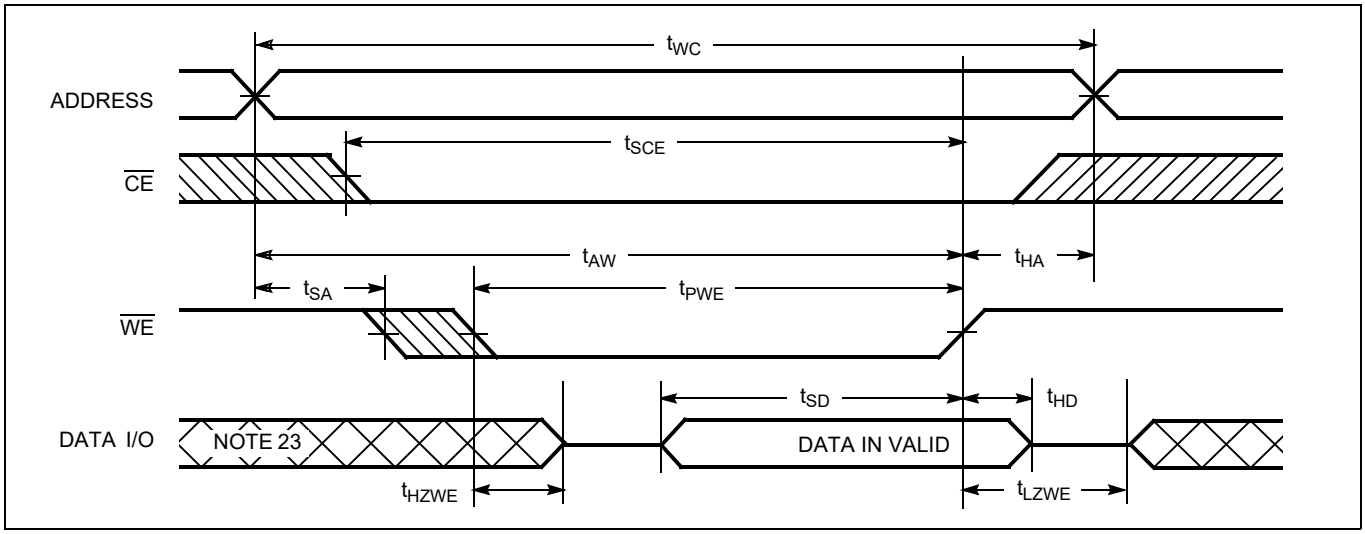


Figure 8 Write cycle no. 3 (WE controlled, OE LOW)[21, 22]

Notes

21. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a High-Z state.
22. The minimum write cycle time for write cycle no. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
23. During this period the I/Os are in the output state and input signals are not applied.

13 Truth table

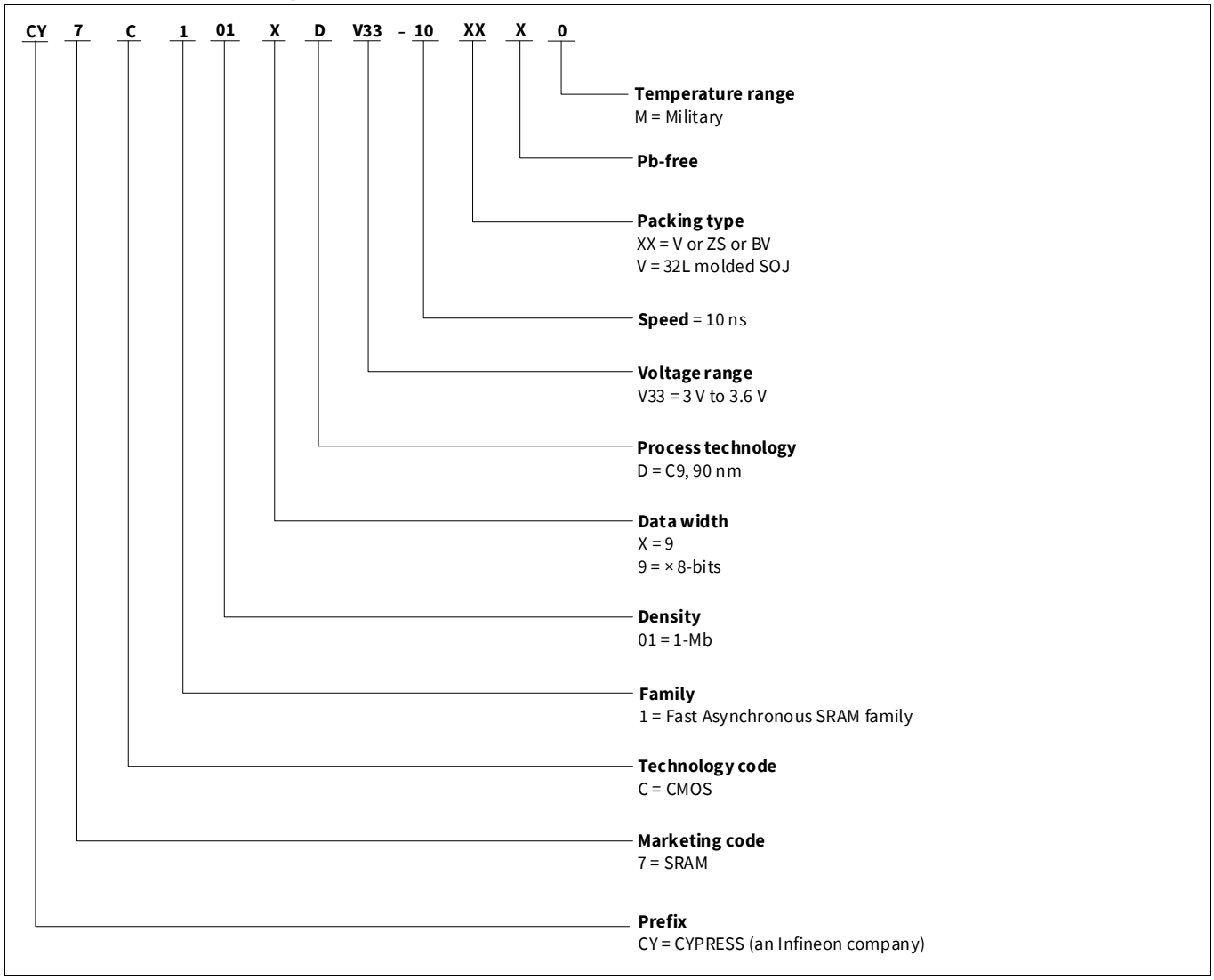
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data out	Read	Active (I_{CC})
L	X	L	Data in	Write	Active (I_{CC})
L	H	H	High-Z	Selected, outputs disabled	Active (I_{CC})

14 Ordering Information

Speed (ns)	Product	Package diagram	Package type	Operating range
10	CY7C1019DV33-10VXM	51-85033	32L SOJ 400 MILS V32.4 (molded SOJ V33) (Pb-free)	Military

Note Contact the local Infineon sales representative for availability of these parts.

14.1 Ordering code definitions



15 Package diagram

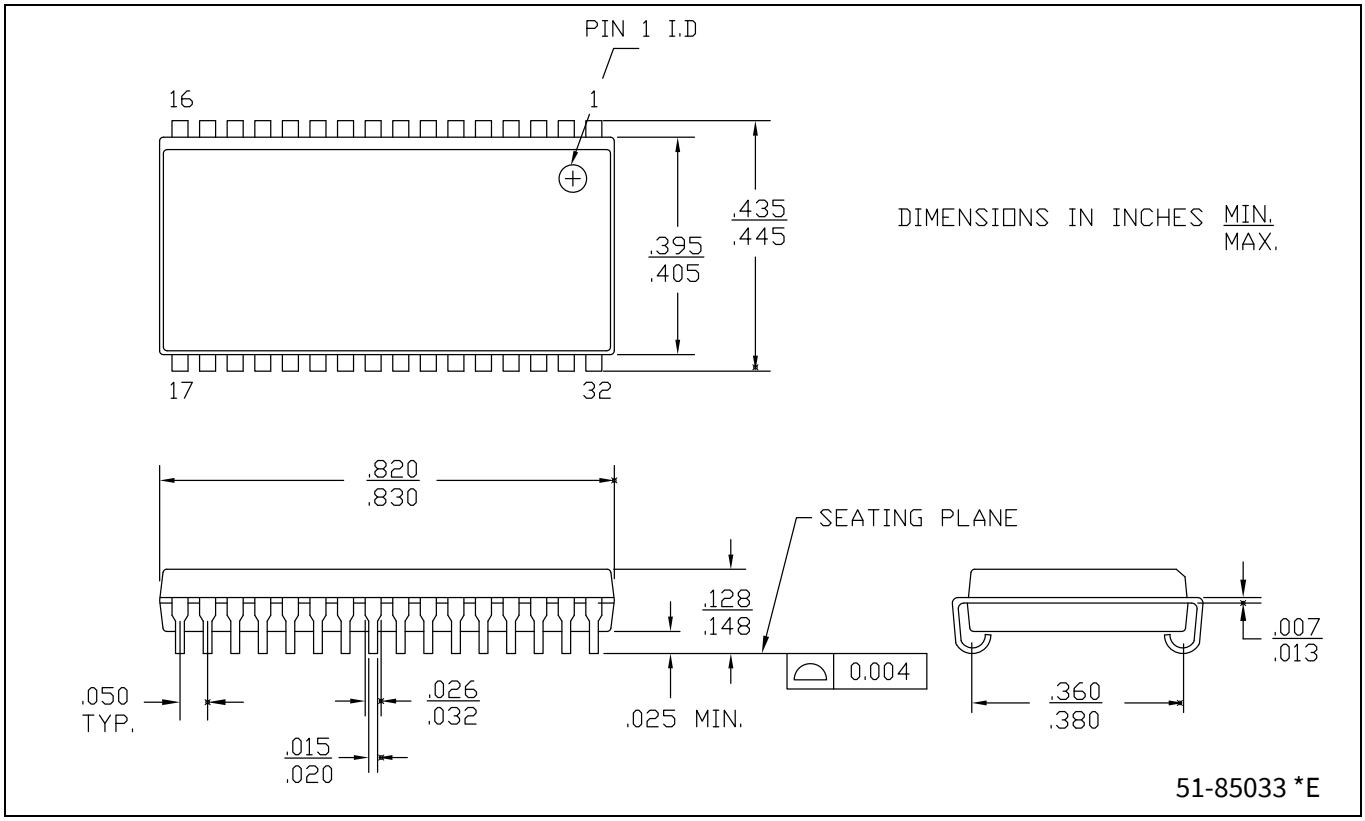


Figure 9 32L SOJ 400 MILS V32.4 (molded SOJ V33), package outline (PG-SOJ-32)

16 Acronyms

Table 1 Acronyms used in this document

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	complementary metal oxide semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SOJ	Small outline J-lead
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	Write Enable

17 Document conventions

17.1 Units of measure

Table 2 Units of measure

Symbol	Unit of measure
°C	degree celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Revision history

Document revision	Date	Description of changes
*A	2024-01-12	Updated document status to final.
*B	2024-01-22	Releasing to web.

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