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**Continuity of ordering part numbers**

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CY62177G30/CY62177GE30 MoBL

# 32-Mbit (2M words × 16-bit/ 4M words × 8-bit) Static RAM with Error-Correcting Code (ECC)

## Features

- Ultra-low standby current
  - Typical standby current: 3 µA
  - Maximum standby current: 19 µA
- High speed: 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction[1]
- Operating voltage range: 2.2 V to 3.6 V
- 1.5-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 48-pin TSOP I package configurable as 2M × 16 or 4M × 8 SRAM
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

## Functional Description

CY62177G30 and CY62177GE30 are high-performance CMOS, low-power (MoBL®) SRAM devices with embedded ECC[2]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62177GE30 device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable ($\overline{CE}$) input LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and $CE_2$ as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on the device data pins ($I/O_0$ through $I/O_{15}$) and address pins ($A_0$ through $A_{20}$) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls $I/O_8$ through $I/O_{15}$ and $\overline{BLE}$ controls $I/O_0$ through $I/O_7$.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. You can access read data on the I/O lines ($I/O_0$ through $I/O_{15}$). To perform byte accesses, assert the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH / $CE_2$ LOW for a dual chip enable device), or the control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

These devices have a unique Byte Power-down feature where, if both the Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are disabled, the devices seamlessly switch to the standby mode irrespective of the state of the chip enables, thereby saving power.

On the CY62177GE30 devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table – CY62177G30/CY62177GE30 on page 15 for a complete description of read and write modes.

The CY62177G30 and CY62177GE30 devices are available in a Pb-free 48-pin TSOP I package and 48-ball VFBGA packages. The logic block diagrams are on page 2.

The device in the 48-pin TSOP I package can also be configured to function as a 4M words × 8 bit device. Refer to the Pin Configurations section for details.

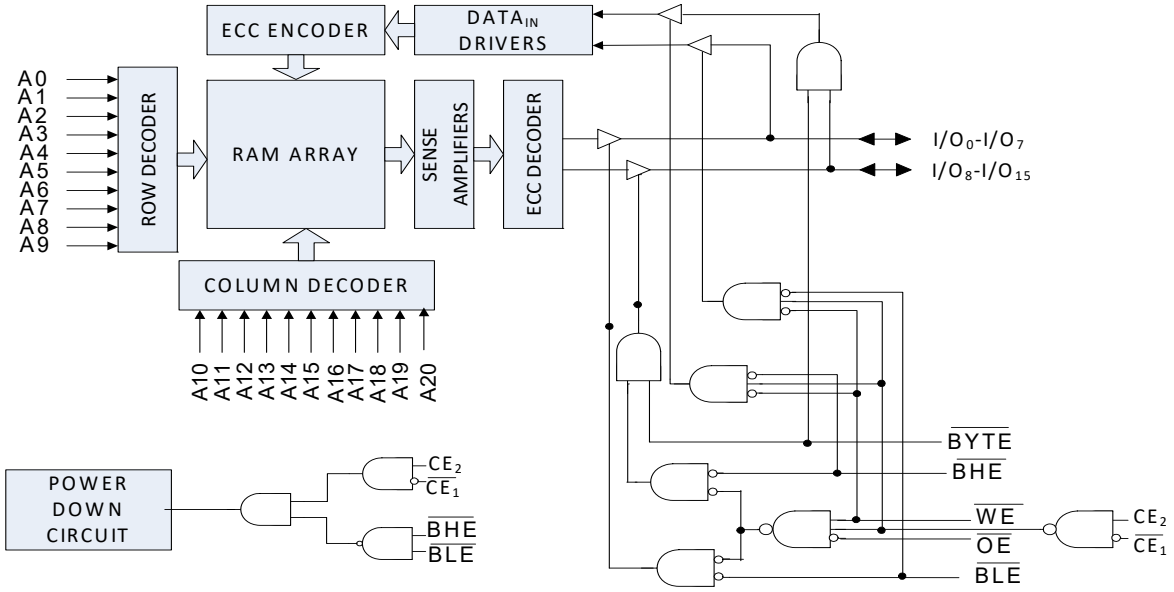
For a complete list of related documentation, click here.

## Product Portfolio

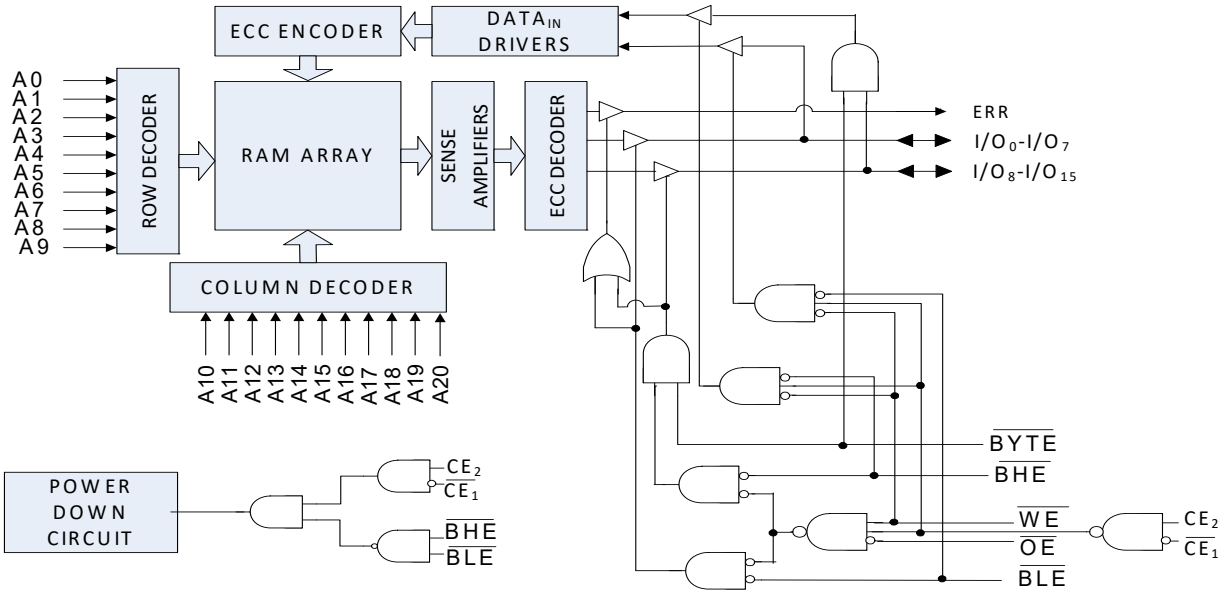
| Product | Features and Options (see Pin Configurations section) | Range | $V_{CC}$ Range (V) | Speed (ns) | Current Consumption | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$, (mA) | | Standby, $I_{SB2}$ (µA) | |
| | | | | | f = $f_{max}$ Typ[3] | Max | Typ[3] | Max |
| CY62177G30/CY62177GE30 | Single or dual Chip Enables Optional ERR pin | Industrial | 2.2 V–3.6 V | 55 | 35 | 45 | 3 | 19 |

**Notes**
1. SER FIT rate <0.1 FIT/Mb. Refer to AN88889 for details.
2. This device does not support automatic write-back on error detection.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V), $T_A$ = 25 °C.

## Logic Block Diagram – CY62177G30




## Logic Block Diagram – CY62177GE30



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## Pin Configuration – CY62177G30

**Figure 1. 48-ball VFBGA/BGA Pinout (Dual Chip Enable without ERR) – CY62177G30[4]**

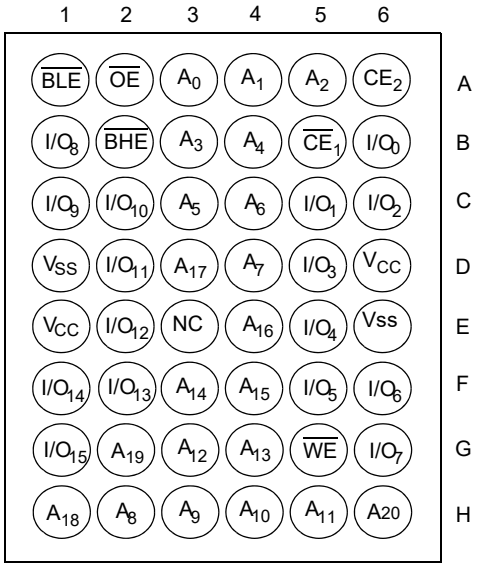
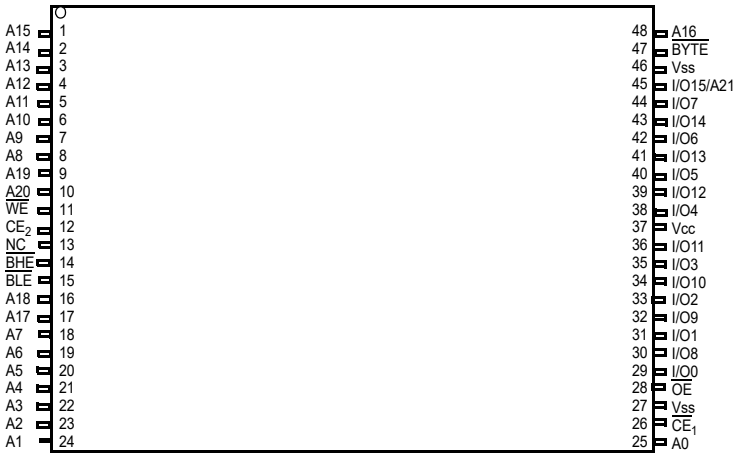



**Figure 2. 48-pin TSOP I Pinout (Dual Chip Enable without ERR) – CY62177G30[4, 5]**




**Notes**

4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
5. Tie the $\overline{BYTE}$ pin in the 48-pin TSOP I package to $V_{CC}$ to use the device as a 2M × 16 SRAM. The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the $\overline{BYTE}$ signal to $V_{SS}$. In the 4M × 8 configuration, pin 45 is the extra address line A21, while $\overline{BHE}$, $\overline{BLE}$, and $I/O_8$ to $I/O_{14}$ pins are not used and can be left floating.

## Pin Configuration – CY62177GE30

**Figure 3. 48-ball VFBGA/BGA Pinout (Single Chip Enable with ERR) – CY62177GE30** [6, 7]

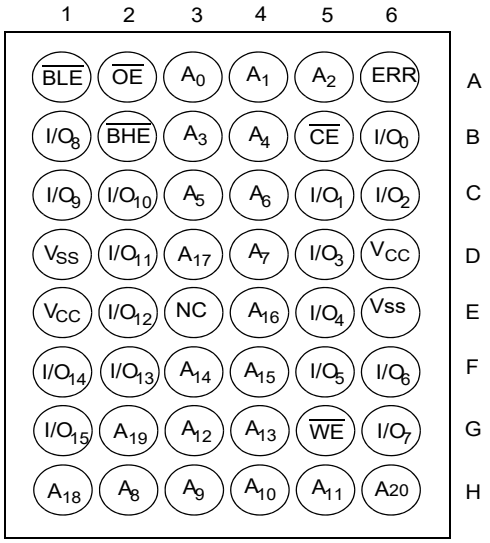
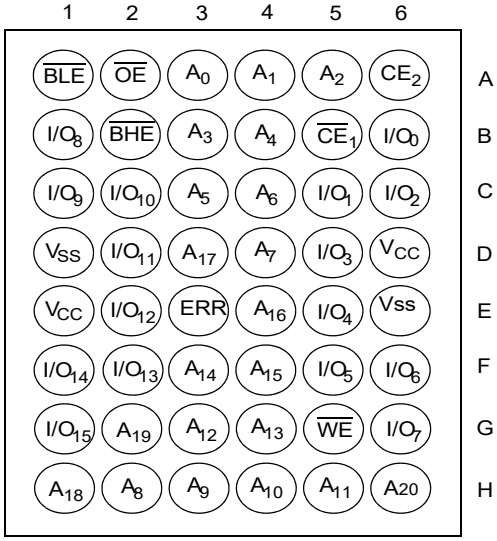



**Figure 4. 48-ball VFBGA/BGA Pinout (Dual Chip Enable with ERR) – CY62177GE30** [6, 7]

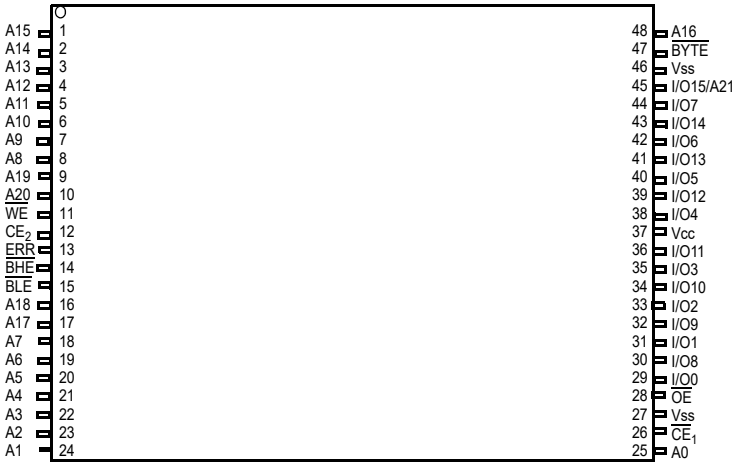



**Notes**

6. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
7. ERR is an Output pin. If not used, this pin should be left floating.

## Pin Configuration – CY62177GE30 (continued)

**Figure 5. 48-pin TSOP I Pinout (Dual Chip Enable with ERR) – CY62177GE30** [8, 9]




**Notes**

8. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
9. Tie the BYTE pin in the 48-pin TSOP I package to $V_{CC}$ to use the device as a 2M × 16 SRAM. The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the BYTE signal to $V_{SS}$. In the 4M × 8 configuration, pin 45 is the extra address line A21, while the BHE, BLE, and $I/O_8$ to $I/O_{14}$ pins are not used and can be left floating.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to $V_{CC}$ + 0.5 V

DC voltage applied to outputs in High Z state[10]..... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage[10] ..... –0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

| Grade | Ambient Temperature | $V_{CC}$[11] |
|---|---|---|
| Industrial | –40 °C to +85 °C | 2.2 V to 3.6 V |

## DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

| Parameter | Description | | Test Conditions | | 55 ns | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ[12] | Max | |
| $V_{OH}$ | Output HIGH voltage | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | 2.0 | – | – | V |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | | 2.4 | – | – | |
| $V_{OL}$ | Output LOW voltage | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | – | – | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OL}$ = 2.1 mA | | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage[10] | 2.2 V to 2.7 V | – | | 1.8 | – | $V_{CC}$ + 0.3 | |
| | | 2.7 V to 3.6 V | – | | 2.0 | – | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input LOW voltage[10] | 2.2 V to 2.7 V | – | | –0.3 | – | 0.6 | |
| | | 2.7 V to 3.6 V | – | | –0.3 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | –1.0 | – | +1.0 | µA |
| $I_{OZ}$ | Output leakage current | | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output disabled | | –1.0 | – | +1.0 | |
| $I_{CC}$ | $V_{CC}$ operating supply current | | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, CMOS levels | f = 22.22 MHz (45 ns) | – | 35.0 | 45.0 | mA |
| | | | | f = 1 MHz | – | 10.0 | 18.0 | |
| $I_{SB1}$[13] | Automatic Power-down Current – CMOS Inputs; $V_{CC}$ = 2.2 V to 3.6 V | | $\overline{CE}_1$ ≥ $V_{CC}$ – 0.2 V or $CE_2$ ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≤ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC}$ = $V_{CC(max)}$ | | – | 3.0 | 19.0 | µA |
| $I_{SB2}$[13] | Automatic Power-down Current – CMOS Inputs $V_{CC}$ = 2.2 V to 3.6 V | | $\overline{CE}_1$ ≥ $V_{CC}$ – 0.2V or $CE_2$ ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V or $V_{IN}$ ≤ 0.2 V, f = 0, $V_{CC}$ = $V_{CC(max)}$ | | – | 3.0 | 19.0 | µA |

**Notes**

10. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of less than 20 ns.
11. Full device AC operation assumes a 100-µs ramp time from 0 to $V_{CC}$ (min) and 400-µs wait time after $V_{CC}$ stabilizes to its operational value.
12. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
13. The $I_{SB2}$ maximum limits at 25 °C are guaranteed by design and not 100% tested.

## Capacitance

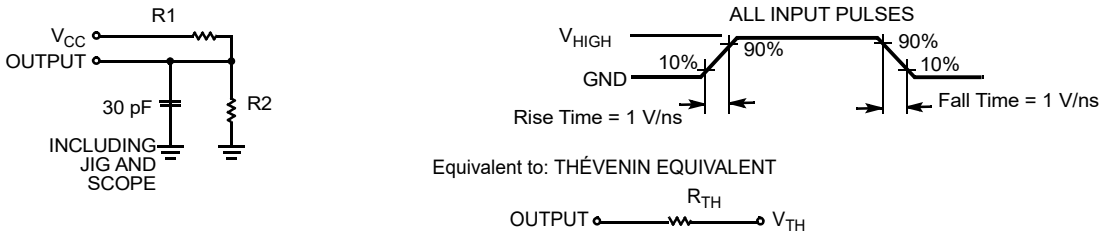
| Parameter [14] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 15.0 | pF |
| $C_{OUT}$ | Output capacitance | | 15.0 | |

## Thermal Resistance

| Parameter [14] | Description | Test Conditions | 48-ball VFBGA | 48-ball FBGA | 48-pin TSOP I | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 54.8 | 51.5 | 50.98 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 11.9 | 7.8 | 9.4 | |

## AC Test Loads and Waveforms

**Figure 6. AC Test Loads and Waveforms**




| Parameters | 2.5 V | 3.0 V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | |
| $R_{TH}$ | 8000 | 645 | |
| $V_{TH}$ | 1.20 | 1.75 | V |
| $V_{HIGH}$ | 2.5 | 3.0 | |

**Note**
14. Tested initially and after any design or process changes that may affect these parameters.

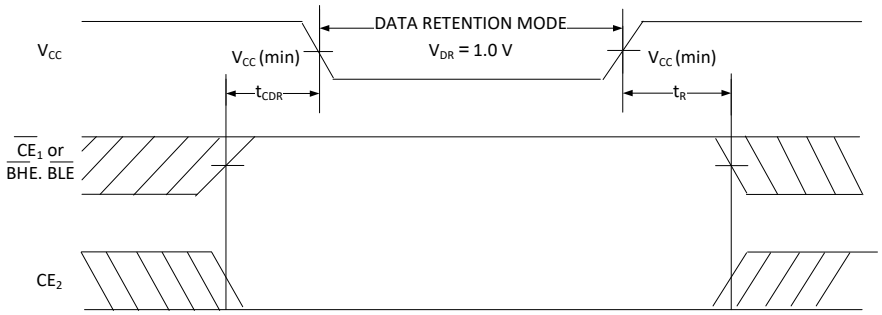
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ [15] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | – | 1.5 | – | – | V |
| $I_{CCDR}$[16, 17] | Data retention current | 2.2 V ≤ $V_{CC}$ ≤ 3.6 V<br>$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 3.0 | 19.0 | µA |
| | | 1.5 V ≤ $V_{CC}$ ≤ 2.2 V,<br>$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | – | 20.0 | |
| $t_{CDR}$[18] | Chip deselect to data retention time | – | 0.0 | – | – | – |
| $t_R$[18, 19] | Operation recovery time | – | 55 | – | – | ns |

## Data Retention Waveform

**Figure 7. Data Retention Waveform** [20]




**Notes**

15. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
16. Chip enables ($\overline{CE}_1$ and $CE_2$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
17. $I_{CCDR}$ is guaranteed only after the device is first powered up to $V_{CC(min)}$ and then brought down to $V_{DR}$.
18. These parameters are guaranteed by design and are not tested.
19. Full-device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)}$ ≥ 400 µs or stable at $V_{CC(min)}$ ≥ 400 µs.
20. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

| Parameter[21] | Description | 55 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 55.0 | – | ns |
| $t_{AA}$ | Address to data valid / Address to ERR valid | – | 55.0 | |
| $t_{OHA}$ | Data hold from address change / ERR hold from address change | 10.0 | – | |
| $t_{ACE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid / $\overline{CE}$ LOW to ERR valid | – | 55.0 | |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid | – | 25.0 | |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [22, 23] | 5.0 | – | |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [22, 23, 24] | – | 18.0 | |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z [22, 23] | 10.0 | – | |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z [22, 23, 24] | – | 18.0 | |
| $t_{PU}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up [25] | 0.0 | – | |
| $t_{PD}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down [25] | – | 55.0 | |
| $t_{DBE}$ | BLE / BHE LOW to data valid | – | 55.0 | |
| $t_{LZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [22] | 5.0 | – | |
| $t_{HZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [22, 24] | – | 18.0 | |
| **Write Cycle** [26, 27] | | | | |
| $t_{WC}$ | Write cycle time | 55.0 | – | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to write end | 40.0 | – | |
| $t_{AW}$ | Address setup to write end | 40.0 | – | |
| $t_{HA}$ | Address hold from write end | 0 | – | |
| $t_{SA}$ | Address setup to write start | 0 | – | |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 40.0 | – | |
| $t_{BW}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to write end | 40.0 | – | |
| $t_{SD}$ | Data setup to write end | 25.0 | – | |
| $t_{HD}$ | Data hold from write end | 0.0 | – | |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [22, 23, 24] | – | 18.0 | |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [22, 23] | 10.0 | – | |

**Notes**

21. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to $V_{CC}$ (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in Figure 6 on page 8, unless specified otherwise.
22. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
23. Tested initially and after any design or process changes that may affect these parameters.
24. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
25. These parameters are guaranteed by design and are not tested.
26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 8. Read Cycle No. 1 of CY62177G30 (Address Transition Controlled)** [28, 29]

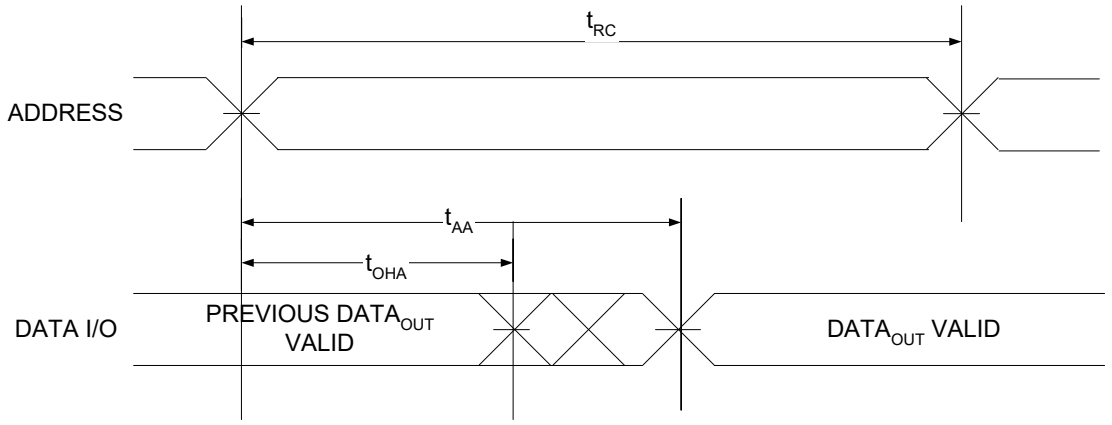
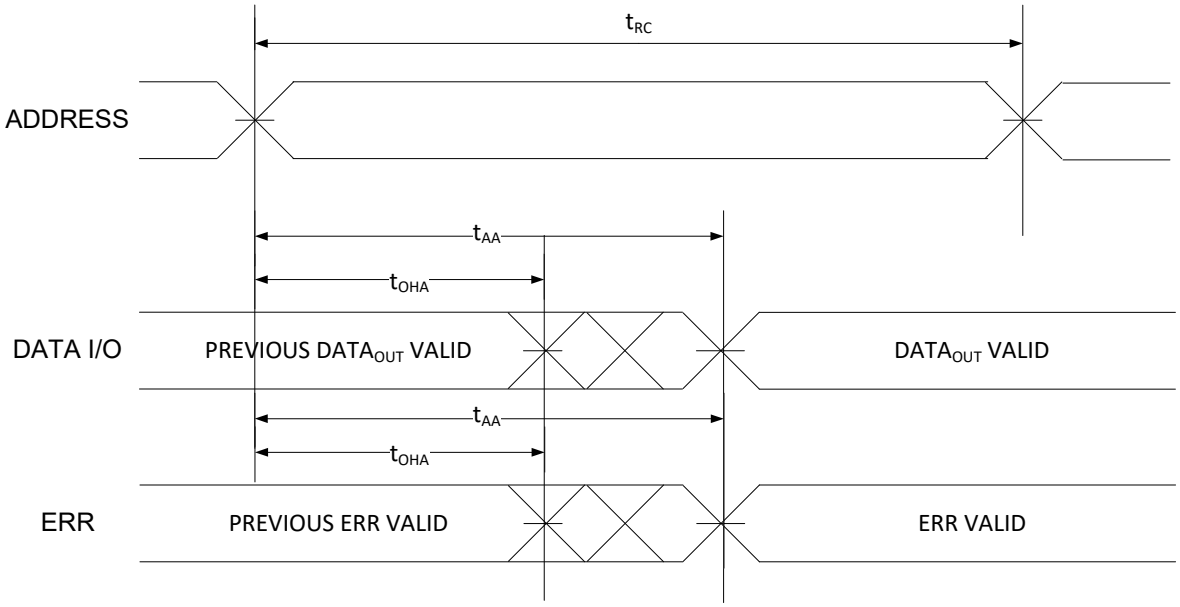



**Figure 9. Read Cycle No. 1 of CY62177GE30 (Address Transition Controlled)** [28, 29]




**Notes**

28. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$, or both $= V_{IL}$.
29. $\overline{WE}$ is HIGH for read cycle.

## Switching Waveforms (continued)

**Figure 10. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [30, 31, 32, 34]

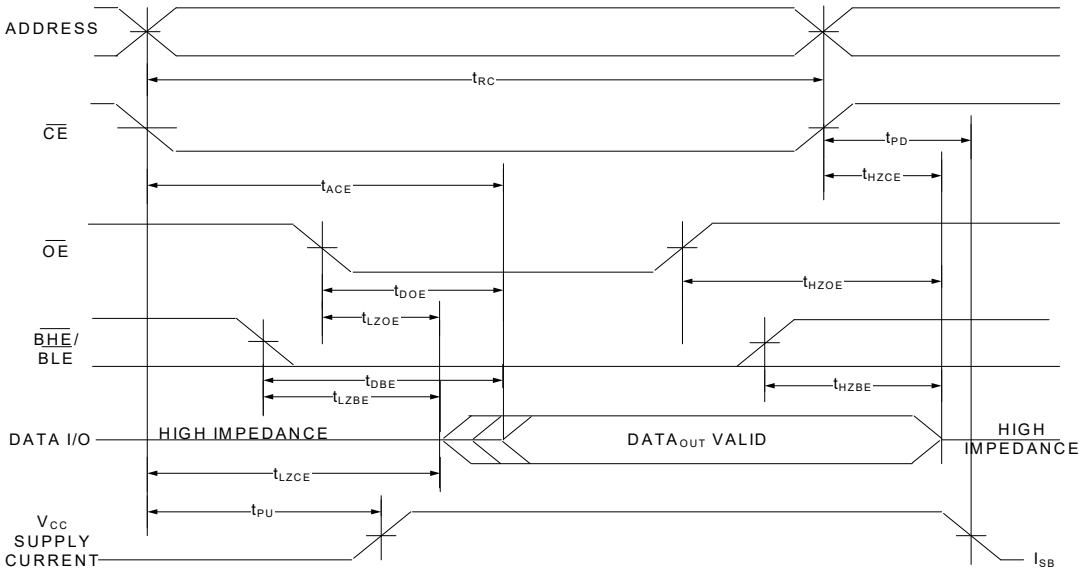
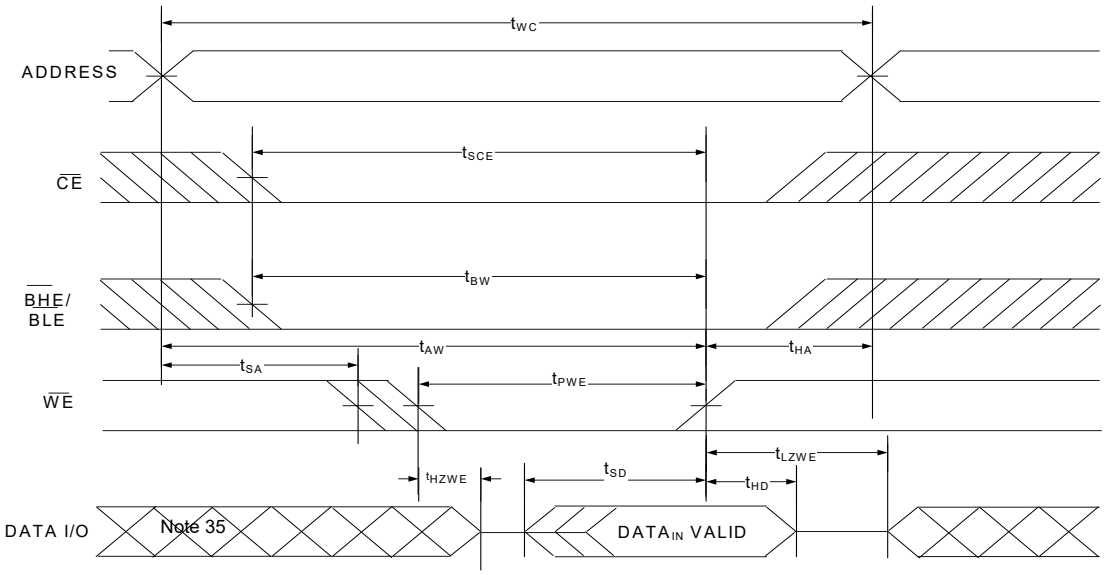



**Figure 11. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [31, 33, 34, 35]

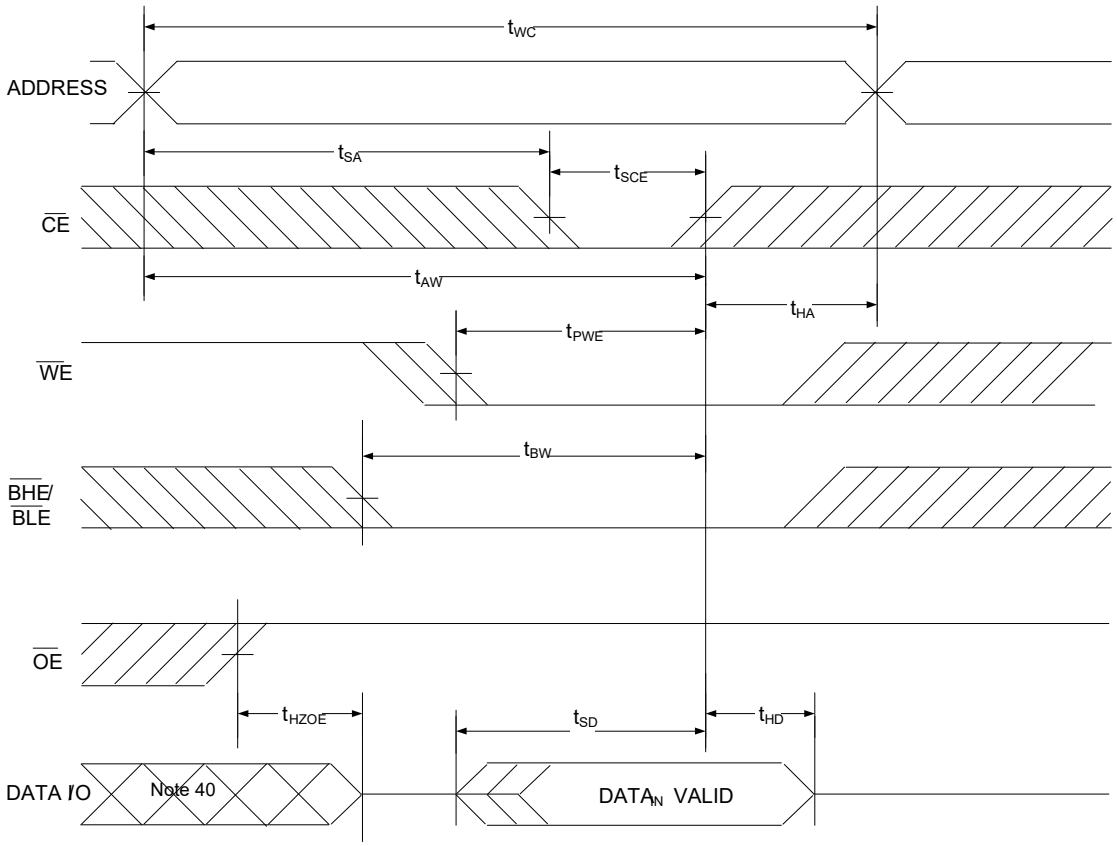



**Notes**

30. $\overline{WE}$ is HIGH for read cycle.
31. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
32. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
33. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$, or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
34. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
35. During this period, the I/Os are in the output state. Do not apply input signals.
36. The minimum write cycle pulse width should be equal to the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms (continued)

**Figure 12. Write Cycle No. 2 ($\overline{CE}$ Controlled)** [37, 38, 39]




**Notes**

37. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
38. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
39. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
40. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 13. Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)** [41, 42, 43]

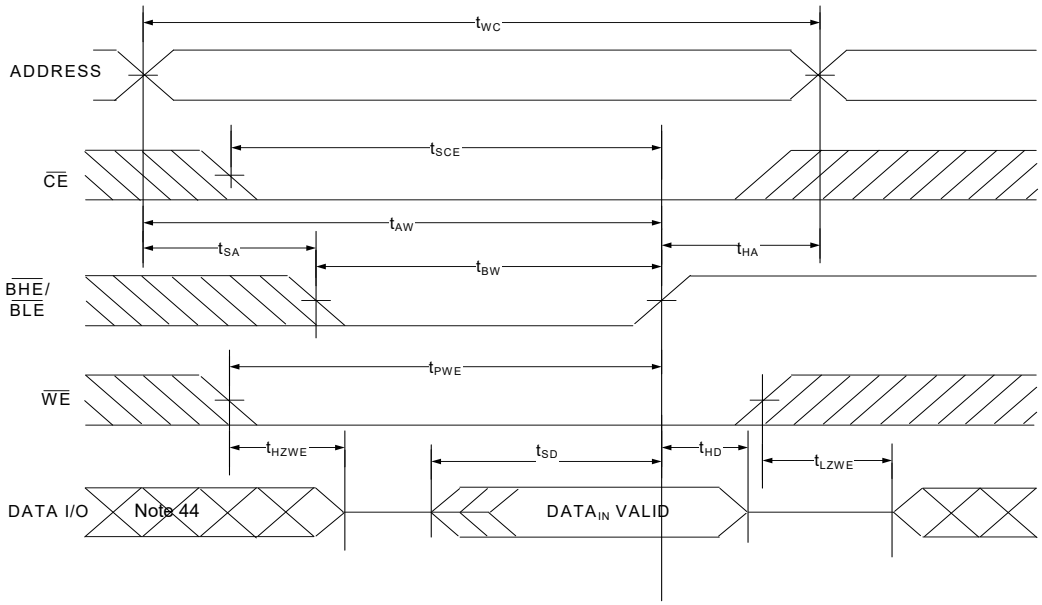
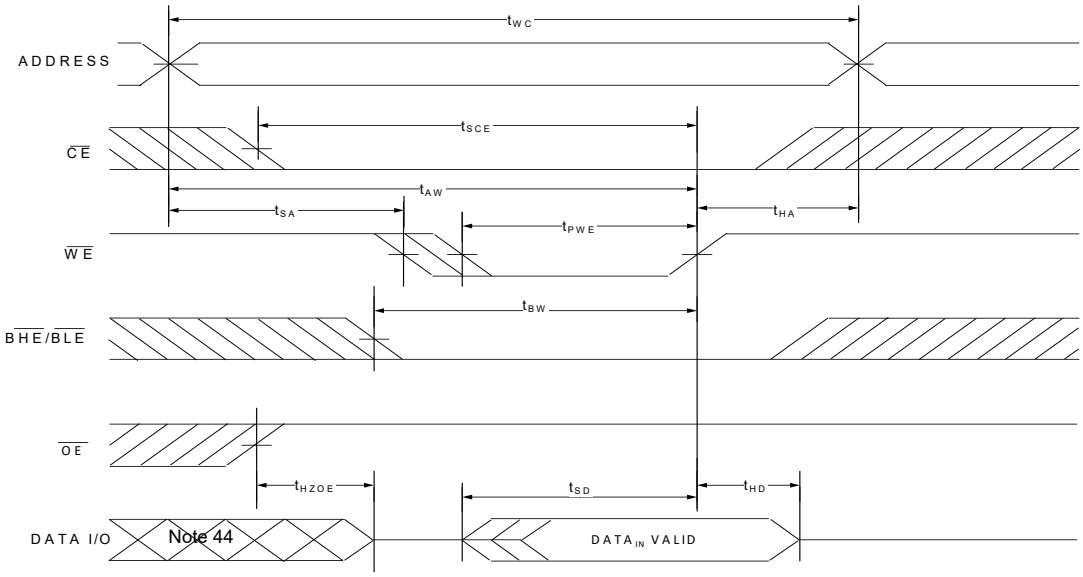



**Figure 14. Write Cycle No. 5 ($\overline{WE}$ Controlled)** [41, 42, 43]




**Notes**

41. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
42. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
43. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
44. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table – CY62177G30/CY62177GE30

| $\overline{BYTE}$[45] | $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power | Configuration |
|---|---|---|---|---|---|---|---|---|---|---|
| X[46] | H | X[46] | X | X | X | X | High-Z | Deselect/Power-down | Standby ($I_{SB}$) | 4M × 8/2M × 16 |
| X | X[46] | L | X | X | X | X | High-Z | Deselect/Power-down | Standby ($I_{SB}$) | 4M × 8/2M × 16 |
| X | X[46] | X[46] | X | X | H | H | High-Z | Deselect/Power-down | Standby ($I_{SB}$) | 2M × 16 |
| H | L | H | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); High-Z ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | H | L | L | H | High Z ($I/O_0$–$I/O_7$); Data Out ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | H | H | L | H | High-Z | Output disabled | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | H | H | H | L | High-Z | Output disabled | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | H | H | L | L | High-Z | Output disabled | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | L | X | H | L | Data In ($I/O_0$–$I/O_7$); High-Z ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) | 2M × 16 |
| H | L | H | L | X | L | H | High-Z ($I/O_0$–$I/O_7$); Data In ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) | 2M × 16 |
| L | L | H | H | L | X | X | Data Out ($I/O_0$–$I/O_7$) | Read | Active ($I_{CC}$) | 2M × 16 |
| L | L | H | H | H | X | X | High-Z | Output disabled | Active ($I_{CC}$) | 2M × 16 |
| L | L | H | L | X | X | X | Data In ($I/O_0$–$I/O_7$) | Write | Active ($I_{CC}$) | 4M × 8 |

## ERR Output – CY62177GE30

| Output[47] | Mode |
|---|---|
| 0 | Read operation, no single-bit error in the stored data. |
| 1 | Read operation, single-bit error detected and corrected. |
| High-Z | Device deselected / outputs disabled / Write operation |

**Notes**

45. This pin is available only in the 48-pin TSOP I package. Tie the $\overline{BYTE}$ to $V_{CC}$ to configure the device in the 2M × 16 option. The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the $\overline{BYTE}$ signal to $V_{SS}$.
46. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.
47. ERR is an Output pin. If not used, this pin should be left floating.

## Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Key Features / Differentiators | ERR Pin / Ball | Operating Range |
|---|---|---|---|---|---|---|---|
| 55 | 2.2 V–3.6 V | CY62177G30-55BAXI | 51-85191 | 48-ball FBGA | Dual Chip Enable | No | Industrial |
| | | CY62177G30-55BAXIT | | | | | |
| | | CY62177G30-55BKXI | 51-85193 | 48-ball VFBGA | | | |
| | | CY62177G30-55BKXIT | | | | | |
| | | CY62177G30-55ZXI | 51-85183 | 48-pin TSOP I | | | |
| | | CY62177G30-55ZXIT | | | | | |
| | | CY62177GE30-55ZXI | | | | Yes | |

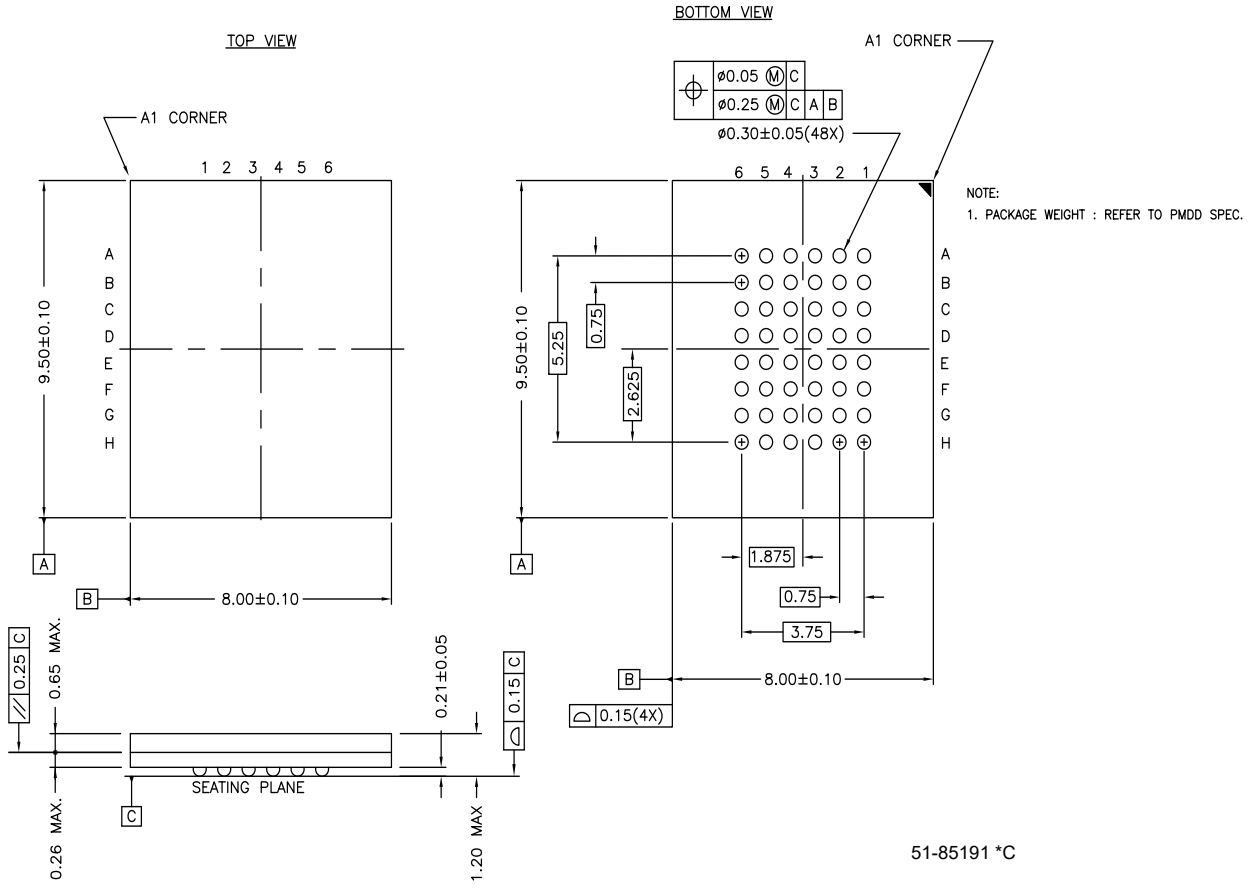
### Ordering Code Definitions

CY 621 7 7 G E 30 - 55 XX X X I X

- X = blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Grade: I = Industrial
- Pb-free
- X = blank or 1
  blank = Dual Chip Enable; 1 = Single Chip Enable
- Package Type: XX = BA or BK or Z
  BA = 48-ball FBGA; BK = 48-ball VFBGA; Z = 48-pin TSOP I
- Speed Grade: XX: 55 = 55 ns
- Voltage Range: 30 = 3 V typ
- ERR Output: Single-bit error correction indicator
- Process Technology: Ultra Low-power
- Bus Width: 7 = ×16
- Density: 7 = 32-Mbit
- Family Code: 621 = MoBL® SRAM family
- Company ID: CY = Cypress

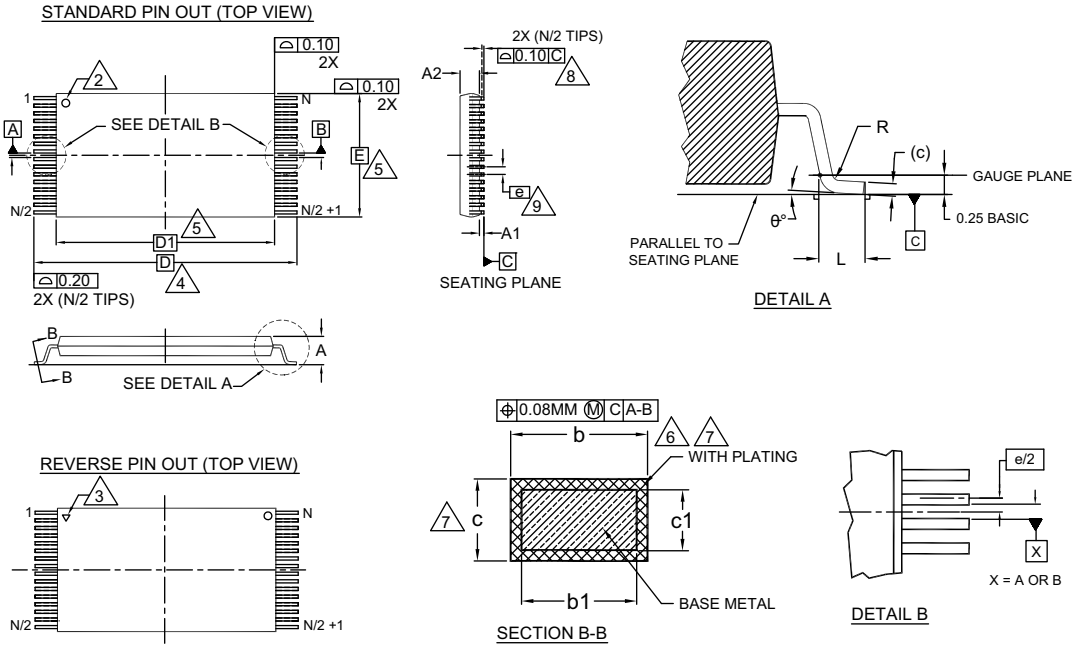
## Package Diagrams

**Figure 15. 48-ball FBGA (8 × 9.5 × 1.2 mm) Package Outline, 51-85191**



## Package Diagrams (continued)

**Figure 16. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

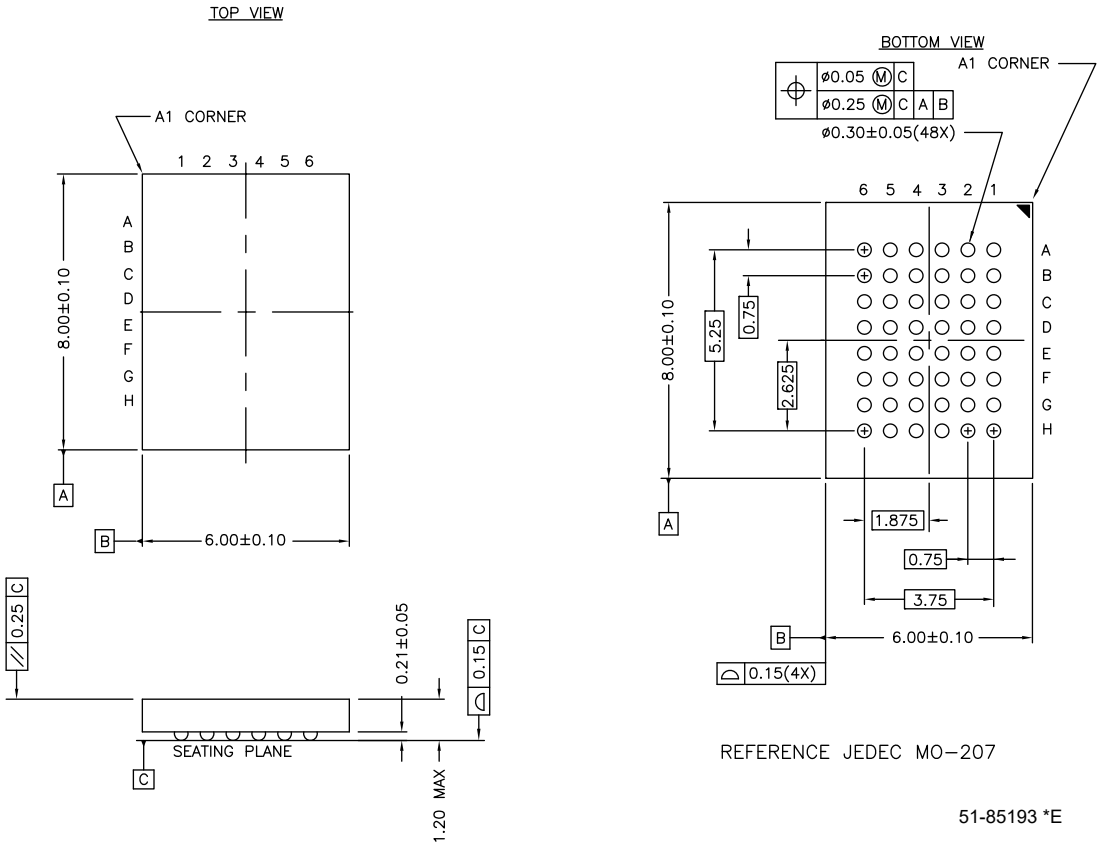
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

## Package Diagrams (continued)

**Figure 17. 48-pin FBGA (6 × 8 × 1.2 mm) Package Outline, 51-85193**



## Acronyms

**Table 1. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| $\overline{BHE}$ | Byte High Enable |
| $\overline{BLE}$ | Byte Low Enable |
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary metal oxide semiconductor |
| I/O | Input/output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static random access memory |
| TSOP | Thin small outline package |
| VFBGA | Very fine-pitch ball grid array |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

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|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *C | 7085237 | 02/09/2021 | Release to web. |

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