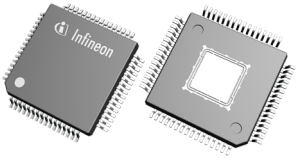
英飞凌 OPTIREG™ PMIC CLF4D985QKV03R1

适用于高达 ASIL D 功能安全等级的系统的多轨电源管理 IC

AEC Qualified　RoHS　ISO 26262 compliant

特性



- 符合 AEC -Q100 Grade 1 高温任务规范
- 宽输入电压范围：3.8 V 至 60 V
- 用于备用电源的 3.3V、30mA 低压差稳压器
- 5.5 V、4.0 V、10 A 预调节器
- 用于微控制器供电的 7A 多相同步降压转换器，可配置为 0.7 V 至 1.1 V，步进为 12.5 mV
- 1.8V、1.2A 降压后置稳压器，用于高速通信接口
- 用于微控制器 IO 电源的 3.3V、600mA 低压降调节器
- 用于低速通信电源的 5.0 V、600 mA 低压降调节器
- 5.0 V ±1%, 150 mA ADC 电源参考电压
- 用于安全开关和反向电池的外部 MOSFET 的控制电路
- 具备复位和中断功能的电压监测，内置自检功能
- 输入电压过压关断监测
- 两个安全状态控制输出、可配置功能看门狗和窗口看门狗
- 支持 CPU 和系统虚拟化的内部状态机
- 32 位 SPI，带 CRC
- 符合 ISO 26262 标准的独立安全单元（SEooC），支持 ASIL D 等级安全要求
- 英飞凌车规级质量
- 绿色产品（符合 RoHS 标准）

潜在应用

- 汽车动力总成和变压器应用：逆变器、发动机管理
- 卡车应用、CAV 应用
- 与传感器融合
- 域控制器、区域控制器
- 连接网关

产品验证

适合对温度要求更高的汽车应用。产品依据 AEC-Q100, Grade 1 进行验证。

描述

英飞凌 OPTIREG™ PMIC CLF4D985QKV03R1 是一款高效的功能安全 PMIC（电源管理集成电路）。

Description

Type	Package	Marking (Line 1 / Line 2)
CLF4D985QKV03R1	PG-LQFP-64	CLF4D985 V03R1

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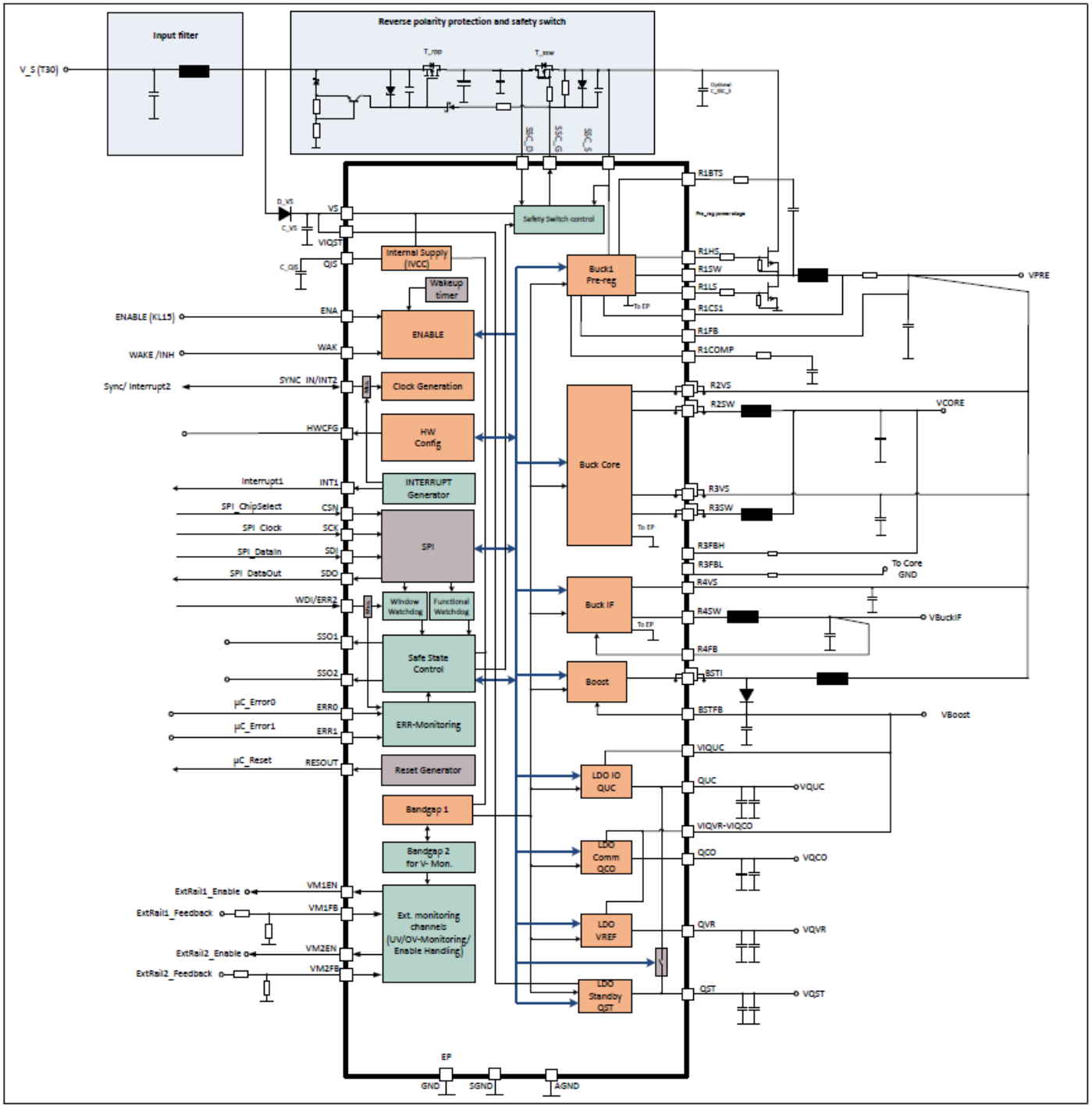
Input filter
Reverse polarity protection and safety switch
V_S (T30)
Safety Switch control
Internal Supply (IVCC)
Wakeup timer
ENABLE (KL15)
WAKE /INH
Sync/ Interrupt2
HWCFG
Interrupt1
SPI_ChipSelect
SPI_Clock
SPI_DataIn
SPI_DataOut
WDI/ERR2
SSO1
SSO2
µC_Error0
µC_Error1
µC_Reset
ExtRail1_Enable
ExtRail1_Feedback
ExtRail2_Enable
ExtRail2_Feedback
ENABLE
Clock Generation
HW Config
INTERRUPT Generator
SPI
Window Watchdog
Functional Watchdog
Safe State Control
ERR-Monitoring
Reset Generator
Bandgap 1
Bandgap 2 for V- Mon.
Ext. monitoring channels (UV/OV-Monitoring/ Enable Handling)
Buck1 Pre-reg
Buck Core
Buck IF
Boost
LDO IO QUC
LDO Comm QCO
LDO VREF
LDO Standby QST
VPRE
VCORE
To Core GND
VBuckIF
VBoost
VQUC
VQCO
VQVR
VQST
To EP
EP
GND
SGND
AGND

图 1 框图

2 Pin configuration

2 引脚配置

2.1 引脚分配

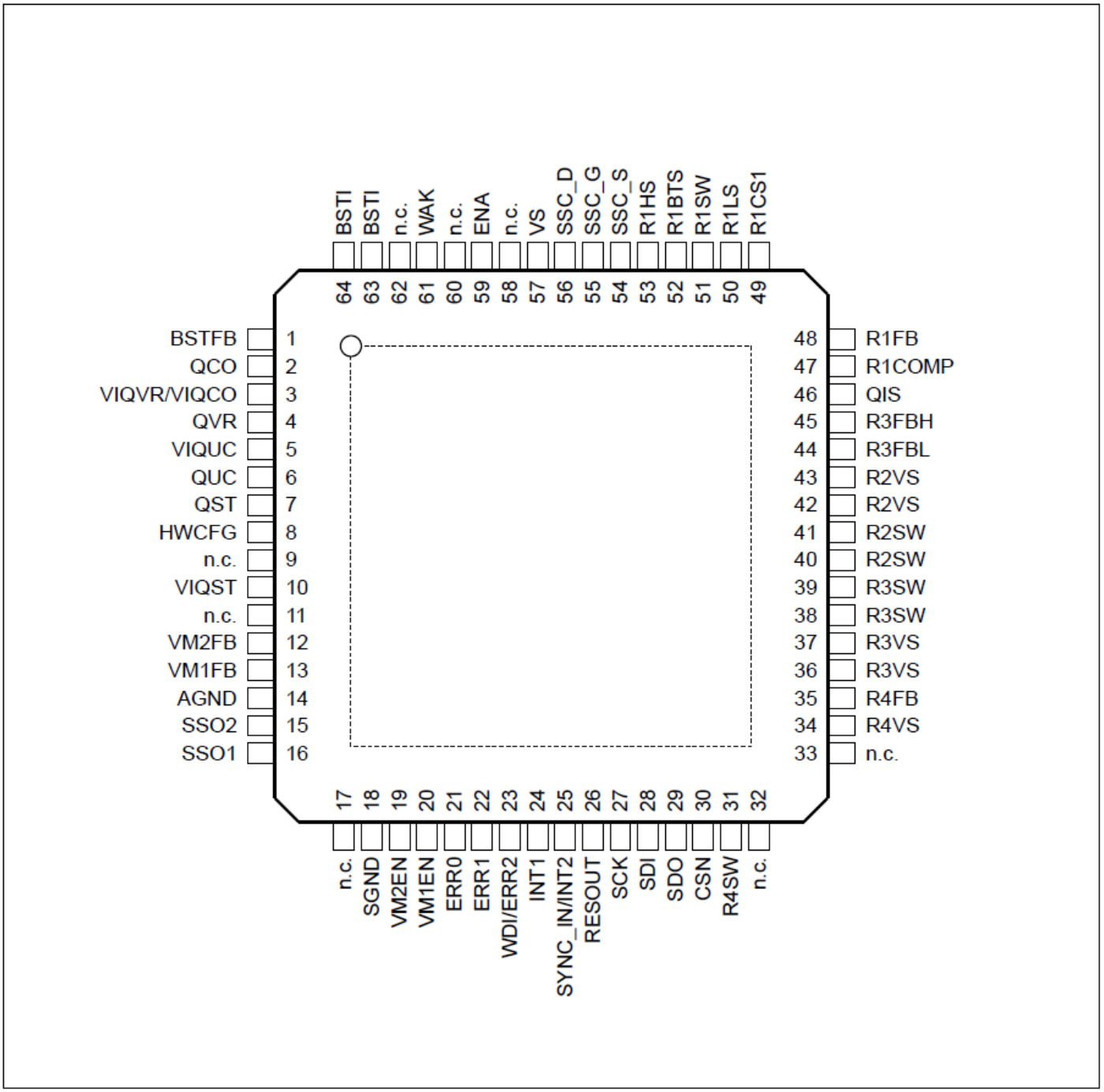

图 2 PG-LQFP-64 封装引脚分配

2.2 引脚定义和功能

表 1 引脚定义和功能

Pin	Name	Type	Function

（表格续下页……）

表 1 （续）引脚定义和功能

1	BSTFB	AI	Boost voltage feedback (connect to R1FB if BOOST not used)
2	QCO	SO	Communication supply voltage
3	VIQVR - VIQCO	SI	Input voltage for voltage reference regulator (QVR) and communication supply regulator (QCO)
4	QVR	SO	ADC reference supply voltage
5	VIQUC	SI	Input voltage for microcontroller IO regulator
6	QUC	SO	Microcontroller IO supply voltage
7	QST	SO	Standby regulator output voltage
8	HWCFG	AO	Hardware configuration setting
9	n.c.	–	Not connected - do not connect to any potential and leave floating
10	VIQST	SI	Input voltage for standby regulator and internal peripherals
11	n.c.	–	Not connected - do not connect to any potential and leave floating
12	VM2FB	AI	Feedback for external voltage monitoring 2
13	VM1FB	AI	Feedback for external voltage monitoring 1
14	AGND	GND	Analog ground connection
15	SSO2	AO	Safe state control output 2
16	SSO1	AO	Safe state control output 1
17	n.c.	–	Not connected - do not connect to any potential and leave floating
18	SGND	GND	Safety ground connection (ground for safety corner SSO1 and SSO2)
19	VM2EN	DIO	Enable for external voltage monitoring 2
20	VM1EN	DIO	Enable for external voltage monitoring 1
21	ERR0	DI	Error monitoring 0 input
22	ERR1	DI	Error monitoring 1 input
23	WDI/ ERR2	DI	Watchdog input/ Error monitoring 2 input WDI option is the default function If REDUCED OPERATION is enabled the integrator must ensure to use the functionality correctly and exclusively use WDI/ERR2 for either one of the watchdogs or ERR2
24	INT1	DO	Interrupt 1 output
25	SYNC_IN/ INT2	DIO	Synchronization input/ Interrupt 2 output
26	RESOUT	DO	Reset output
27	SCK	DI	SPI clock input
28	SDI	DI	SPI data input
29	SDO	DO	SPI data output

(table continues...)

表 1 （续）引脚定义和功能

30	CSN	DI	SPI chip select input
31	R4SW	AO	Switching node buck interface
32	n.c.	–	Not connected - do not connect to any potential and leave floating
33	n.c.	–	Not connected - do not connect to any potential and leave floating
34	R4VS	SI	Input voltage buck interface
35	R4FB	AI	Feedback voltage buck interface regulator
36	R3VS	SI	Input voltage buck core regulator
37	R3VS	SI	Input voltage buck core regulator
38	R3SW	AO	Switching node buck core
39	R3SW	AO	Switching node buck core
40	R2SW	AO	Switching node buck core
41	R2SW	AO	Switching node buck core
42	R2VS	SI	Input voltage buck core regulator
43	R2VS	SI	Input voltage buck core regulator
44	R3FBL	AI	Feedback BUCKCORE regulator: Remote ground GND
45	R3FBH	AI	Feedback buck core regulator
46	QIS	SO	Buffer capacitor for internal supply
47	R1COMP	AO	Buck pre-regulator compensation
48	R1FB	AI	Feedback voltage buck pre-regulator
49	R1CS1	AI	Current feedback shunt positive
50	R1LS	AO	Gate external low side FET for buck pre-regulator
51	R1SW	AI	Switch node pre-regulator
52	R1BTS	SI	Bootstrap input voltage
53	R1HS	AO	Gate external high side FET for buck pre-regulator
54	SSC_S	AI	Safety switch source (If the safety switch is not used, connect to the input of PREREG)
55	SSC_G	AO	Safety switch gate (If the safety switch is not used, connect to the input of PREREG)
56	SSC_D	SI	Safety switch drain (If the safety switch is not used, connect to GND)
57	VS	SI	Main supply voltage
58	n.c.	–	Not connected - do not connect to any potential and leave floating
59	ENA	AI	Enable - edge sensitive
60	n.c.	–	Not connected - do not connect to any potential and leave floating
61	WAK	AI	Wake - level sensitive

(table continues...)

表 1 （续）引脚定义和功能

62	n.c.	–	Not connected - do not connect to any potential and leave floating
63	BSTI	AO	Switch node boost regulator (connect to GND if BOOST not used)
64	BSTI	AO	Switch node boost regulator (connect to GND if BOOST not used)
–	Exposed pad	–	Connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink.

注释：

AI：模拟输入

AO：模拟输出

AIO：模拟输入输出

SI：电源输入

SO：电源输出

DI：数字输入

DO：数字输出

DIO：数字输入输出

3 产品一般特性

注释:

- *超过此处所列的压力可能会对器件造成永久性损坏。长时间在绝对最大额定值条件下工作可能会影响器件的可靠性。*
- *集成的保护功能旨在防止 IC 在数据手册所述故障条件下被毁坏。故障情况被认为超出了正常工作范围。保护功能不是为了连续重复的操作而设计的。*

3.1 绝对最大额定值

表 2 绝对最大额定值

T_j = -40°C 至 +150°C，所有电压相对于地，正向电流流入引脚（除非另有规定）

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Pins							
Input voltage for standby regulator QST	V_{VIQST}	-0.3	–	60	V	–	DS-1661
Safety switch drain	V_{SSC_D}	-0.3	–	60	V	–	DS-1662
Safety switch gate	V_{SSC_G}	-0.3	–	60	V	–	DS-1663
Safety switch source	V_{SSC_S}	-0.3	–	60	V	–	DS-1664
Main supply voltage	V_{VS}	-0.3	–	60	V	–	DS-1665
Enable	V_{ENA}	-0.3	–	60	V	–	DS-1666
Wake	V_{WAK}	-0.3	–	60	V	–	DS-1667
Switch node BUCK PREREG	V_{R1SW}	-2	–	60	V	–	DS-1668
Bootstrap input voltage	V_{R1BTS}	-0.3	–	60	V	–	DS-1669
Gate external high-side FET for BUCK PREREG	V_{R1HS}	-0.3	–	60	V	–	DS-1670
Switch node BOOST regulator	V_{BSTI}	-0.3	–	7	V	–	DS-1671
Current feedback shunt positive	V_{R1CS1}	-0.3	–	7	V	–	DS-1672
Feedback voltage BUCK PREREG	V_{R1FB}	-0.3	–	7	V	–	DS-1673
Input voltage BUCK IF regulator	V_{R4VS}	-0.3	–	7	V	–	DS-1674
Feedback for BUCK IF regulator	V_{R4FB}	-0.3	–	7	V	–	DS-1675
Input voltage BUCK CORE 2 regulator	V_{R3VS}	-0.3	–	7	V	–	DS-1676

（表格续下页……）

表 2　　（续）绝对最大额定值

T_j = -40°C 至 +150°C，所有电压相对于地，正向电流流入引脚（除非另有规定）

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch node BUCK CORE 2 regulator	V_{R3SW}	-0.3	–	7	V	–	DS-1677
Switch node BUCK CORE 1 regulator	V_{R2SW}	-0.3	–	7	V	–	DS-1678
Input voltage BUCK CORE 1 regulator	V_{R2VS}	-0.3	–	7	V	–	DS-1679
Compensation	V_{R1COMP}	-0.3	–	7	V	–	DS-1680
Buffer capacitor for internal supply	V_{QIS}	-0.3	–	7	V	–	DS-1681
Feedback BUCK CORE 2 regulator	V_{R3FBH}	-0.3	–	7	V	–	DS-1682
Switch node BUCK IF regulator	V_{R4SW}	-0.3	–	7	V	–	DS-1683
SPI chip select input	V_{CSN}	-0.3	–	6	V	–	DS-1684
Feedback for external voltage monitoring 2	V_{VM2FB}	-0.3	–	60	V	–	DS-1685
Feedback for external voltage monitoring 1	V_{VM1FB}	-0.3	–	6	V	–	DS-1686
SPI data output	V_{SDO}	-0.3	–	6	V	–	DS-1687
SPI data input	V_{SDI}	-0.3	–	6	V	–	DS-1688
SPI clock input	V_{SCK}	-0.3	–	6	V	–	DS-1689
Hardware configuration setting	V_{HWCFG}	-0.3	–	60	V	–	DS-1690
Output voltage for standby regulator QST	V_{QST}	-0.3	–	6	V	Max value increases to 7 V if QUC is OFF and QST is ON	DS-1691
Microcontroller IO supply voltage	V_{QUC}	-0.3	–	6	V	–	DS-1692
Input voltage for microcontroller IO regulator	V_{VIQUC}	-0.3	–	7	V	–	DS-1693
ADC reference supply voltage	V_{QVR}	-0.3	–	6	V	–	DS-1694
Input voltage reference and communication regulator	$V_{VIQVR-VIQCO}$	-0.3	–	7	V	–	DS-1695
Communication supply voltage	V_{QCO}	-0.3	–	6	V	–	DS-1696

(table continues...)

表 2 （续）绝对最大额定值

T_j = -40°C 至 +150°C，所有电压相对于地，正向电流流入引脚（除非另有规定）

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Boost voltage feedback	V_{BSTFB}	-0.3	–	7	V	–	DS-1697
Safe state control output 1	V_{SSO1}	-0.3	–	60	V	–	DS-1698
Safe state control output 2	V_{SSO2}	-0.3	–	60	V	–	DS-1699
Reset output	V_{RESOUT}	-0.3	–	6	V	–	DS-1700
Synchronization input / interrupt output 2	$V_{SYNC\_IN/INT2}$	-0.3	–	6	V	–	DS-1701
Interrupt output 1	V_{INT1}	-0.3	–	6	V	–	DS-1702
Watchdog input / error input 2	$V_{WDI/ERR2}$	-0.3	–	6	V	–	DS-1703
Error input 0	V_{ERR0}	-0.3	–	6	V	–	DS-1704
Error input 1	V_{ERR1}	-0.3	–	6	V	–	DS-1705
Enable for external voltage monitoring 1	V_{VM1EN}	-0.3	–	6	V	–	DS-1706
Enable for external voltage monitoring 2	V_{VM2EN}	-0.3	–	6	V	–	DS-1707
Safety ground connection	V_{SGND}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1708
Power ground - exposed pad	V_{EP}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1709
Analog ground connection	V_{AGND}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1710
Connection to buck core ground	V_{R3FBL}	-0.3	–	0.3	V	Respect to AGND	DS-1711
Gate external low-side FET for BUCK PREREG	V_{R1LS}	-0.3	–	7	V	Respect to AGND	DS-1712
ESD robustness							
ESD voltage HBM parameter	V_{ESD_HBM}	-2	–	2	kV	2) HBM	DS-1732
ESD robustness not corner pins (CDM)	V_{ESD_CDM}	-500	–	500	V	3) CDM	DS-1733
ESD robustness corner pins (CDM)	$V_{ESD\_CDM\_Corner}$	- 750	–	750	V	3) CDM	DS-1734
Differential parameters							
Differential voltage between R1BTS - R1SW	$\Delta V_{R1BTS-R1SW}$	-0.3	–	7	V	$\Delta V_{R1BTS-R1SW} = V_{R1BTS} - V_{R1SW}$	DS-2060

(table continues...)

表 2　　（续）绝对最大额定值

T_j = -40°C 至 +150°C，所有电压相对于地，正向电流流入引脚（除非另有规定）

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Differential voltage between R1HS- R1SW	$\Delta V_{R1HS-R1SW}$	-0.3	–	7	V	$\Delta V_{R1HS-R1SW} = V_{R1HS} - V_{R1SW}$	DS-2061
Differential voltage between SSC_G - SSC_S	$\Delta V_{SSC\_G-SSC\_S}$	-0.3	–	7	V	$\Delta V_{SSC\_G-SSC\_S\_max} = V_{SSC\_G} - V_{SSC\_S}$	DS-2062

1) 未经过生产测试，由设计指定。
2) 根据 JEDEC HBM 人体模型 ANSI/ESDA/JEDEC JS001 （1.5 kΩ，100 pF）的人体模型 (HBM)。
3) 符合 ESDA STM5.3.1 或 ANSI /ESD S.5.3.1 的带电器件模型 (CDM) 的稳定性。

3.2　功能范围

3.2.1　功能范围描述

注释: *在功能或工作范围内，器件按照电路说明中的描述运行。电气特性是在相关电气特性表中注明的条件下指定的。*

3.2.2　电气特性：功能范围

表 3　　功能范围

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage for normal operation of internal blocks with BOOST	V_S	3.8	–	36	V	For V_{VS} < 6 V, max temp is 105°C; Same voltage applied to VS and VIQST pins; Device must already be operating *1)*	DS-2143
Supply voltage for normal operation of internal blocks without BOOST	V_S	6	–	36	V	Same voltage applied to VS and VIQST pins *1)*	DS-1932

（表格续下页……）

表 3 （续）功能范围

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Device start-up time	t_{start_up}	–	–	11	ms	From first battery connection to release of microcontroller reset RESOUT; Default reset delay time t_{RD} = 2ms; V_{SSC_S} < 1V at startup; Capacitance at SSC_S pin = 1uF[Max] 1)	DS-2084
Supply voltage range, load dump	V_{VS_LD}			V_{VS_OV}	V	Load dump condition, device transitions to FAILSAFE mode if severe overvoltage is detected on VS pin; Same voltage applied to VS and VIQST pins; 1)	DS-2132
PREREG input voltage with boost	$V_{SSC\_S\_PREREG\_BOOST}$	3.6	–	36	V	For V_{SSC_S} ≤ 6.5 V: T_j = -40°C to 105°C; BOOST max load: 650 mA; PREREG max load: 3.5 A (including BOOST load); dV_{SSC_S}/dt ≤ 8 V/ms; PREREG efficiency >= 88% 1)	DS-2144
PREREG input voltage without boost	$V_{SSC\_S\_PREREG\_noBOOST}$	6.6	–	36	V	V_{SSC_S} > 6.6V needed for startup without boost; 1)	DS-2157
Temperatures							
Junction temperature	T_j	-40	–	150	°C	Continuous operation; 1)	DS-1931
Storage temperature	T_{stg}	-55	–	150	°C	1)	DS-2069

1） 未经过生产测试，由设计指定

3.3 热阻

表 4 热阻

V_{VS}= 6.0V 至 40V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	4.8	–	K/W	Fixed temperature for bottom[1)]	DS-2018
Junction to top	R_{thJTop}	–	16.9	–	K/W	Fixed temperature for top side[1)]	DS-2020
Junction to ambient - 2s2p	R_{thJA_2s2p}	–	24.4	–	K/W	JEDEC 2s2p PCB[1) 2)]	DS-2022
Junction to ambient - 2s4p	R_{thJA_2s4p}	–	19.3	–	K/W	2s4p PCB[1) 3)]	DS-2024

1) 未经过生产测试，由设计指定

2) 指定的 R_{thJA}值根据 JEDEC JESD51-2,-5,-7 在 FR4 2s2p 板上自然对流；产品（芯片和封装）在具有两层外部信号铜层（2×70 µm）以及两层内部铜层（2×35 µm）的76.2 × 114.3 × 1.5 mm^3 板上进行模拟。在适当的情况下，位于封装旁的导热过孔阵列与第一层内部铜层连接。

3) 指定的 R_{thJA} 值是根据 FR4 2s4p 板上自然对流的内部应用板测得的；产品（芯片和封装）在 74.2 × 74.2 × 1.688 mm^3 的电路板上进行模拟，该电路板具有两层外部铜层（2×53µm）和四层内部铜层（4×33µm Cu）。导热过孔阵列与第二层和第三层内部铜层接触。

4 DC - DC 开关频率生成和时钟同步

表 5 电气特性：DC-DC 开关频率生成和时钟同步

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DCDC switching frequency default	f_{DCDC}	2.2 + f_{DCDC_acc}[MIN]	2.2	2.2 + f_{DCDC_acc}[MAX]	MHz	–	DS-1719
DCDC switching frequency accuracy	f_{DCDC_acc}	-10	–	+10	%	–	DS-1720

4.1 功能描述

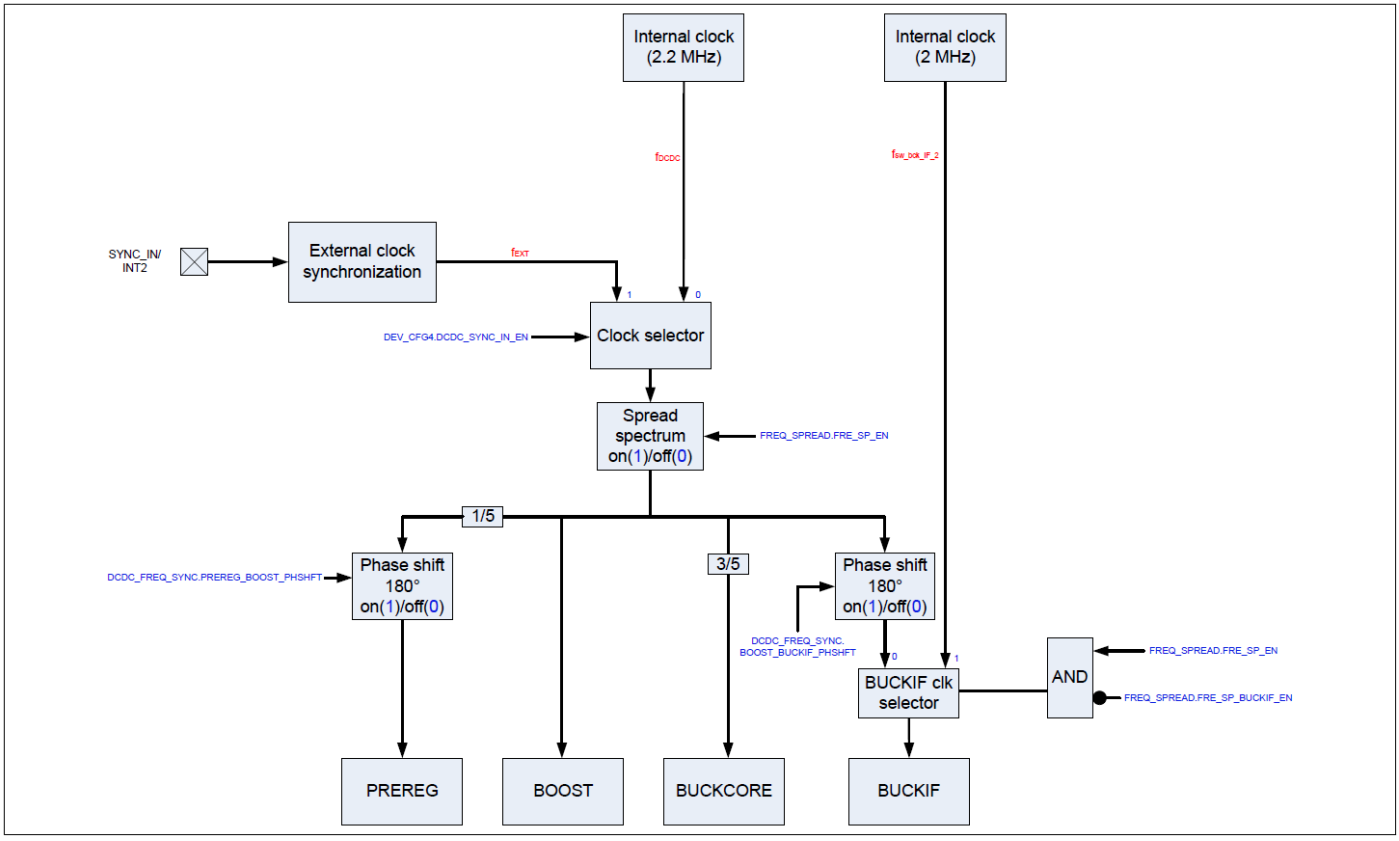

图 3 DC-DC 时钟生成和时钟管理器

不同集成式 DC-DC 转换器的开关频率由集成时钟发生器或外部同步频率信号生成。

主开关频率 ($f_{DC\text{-}DC}$) 可通过 SPI 位**DCDC_FREQ_SYNC.DCDC_FREQSEL** 进行调整，范围为 1.8 MHz 至 2.4 MHz，步进分辨率为 100 kHz。

外部时钟同步

该器件在 SYNC_IN/INT2 引脚上提供 DC- DC 开关频率 f_{DC-DC} 的外部同步功能，外部时钟源的范围为 1.6 MHz至2.6 MHz。这种同步功能可以提高 EMC/EMI 性能并减少对负载的串扰。

可以通过 SPI 位 DEV_CFG4.DCDC_SYNC_IN_EN 启用或禁用同步，默认禁用 (DEV_CFG4.DCDC_SYNC_IN_EN = 0)。

该器件可处理外部时钟源频率中 100 kHz 的变化， 开关频率上的建立时间为 50 µs 。

4.1.1 EMC 特性

展频

该器件采用展频调制来提高 EMC/EMI 性能。展频调制应用于主时钟源，因此影响所有电源转换器。

展频调制默认禁用，可以通过 SPI 位 **FREQ_SPREAD.FRE_SP_EN** 来启用。

使能展频 (**FREQ_SPREAD.FRE_SP_EN = 1)**后，器件允许配置展频功能，也可通过 SPI 位 **FREQ_SPREAD.FRE_SP_BUCKIF_EN** 应用于降压 IF 调节器。

展频调制方式、调制频率和幅度的配置可以通过 SPI 寄存器 **FREQ_SPREAD 进行选择。**

相位偏移

为了进一步提高 EMC 性能，该器件允许通过 SPI 配置 BUCK PREREG 和 BOOST 调节器之间以及 BUCK IF 和 BOOST 调节器之间的相位关系：

- 器件可在 BOOST 和 BUCK IF之间实现 180° 相位偏移，前提是 SPI **DCDC_FREQ_SYNC.BOOST_BUCKIF_PHSHFT** 置位为 1。
- 器件可在 BOOST 和 PREREG 之间实现 180° 相位偏移，前提是 SPI **DCDC_FREQ_SYNC.PREREG_BOOST_PHSHFT** 置位为 1。

压摆率控制

器件还通过 SPI 寄存器 CDC_FREQ_SYNC 为所有电源转换器提供开关斜率的可配置性

5 电源功能

5.1 BUCK PREREG (降压预调节器)

5.1.1 功能描述：BUCK PREREG

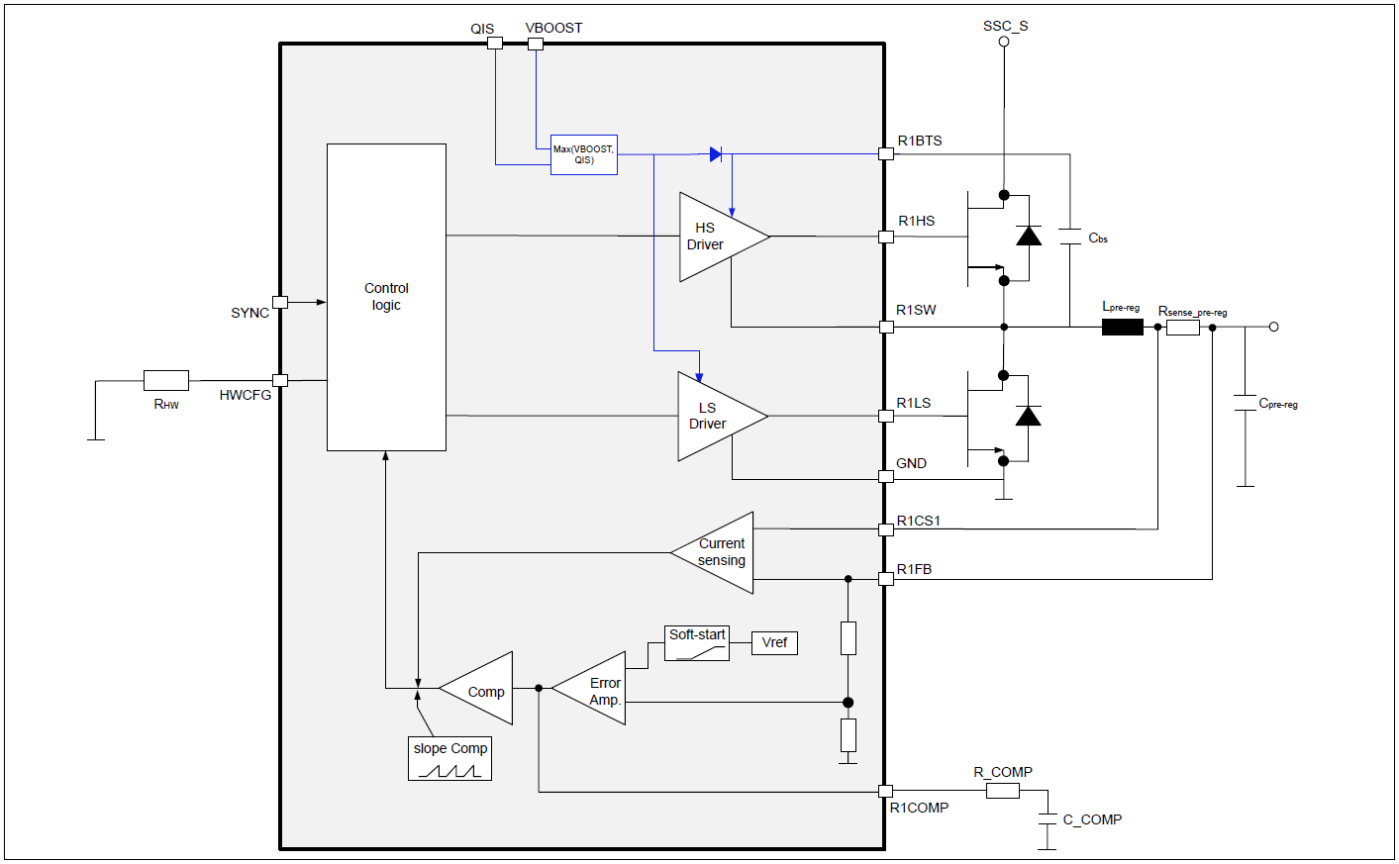

图 4 PREREG 框图

预调节器是一个同步降压控制器，带有两个外部功率开关（NMOS，增强型），为内部电路、降压、升压、LDO 和其他外部负载供电。

预调节器将引脚 SSC_S 处的输入电压转换为带有 I_{bck_prereg} 输出电流的输出电压 V_{R1FB}

预调节器的输出电压可由硬件配置。
根据引脚 HWCFG 上外部电阻的值，输出电压 $V_{R1FB} = V_{R1FB\_4V0}$ 或 $V_{R1FB} = V_{R1FB\_5V5}$
预调节器以 PWM 模式运行，具有峰值电流控制和外部电压控制环路。

输出电流通过外部检流电阻（R_{sense}）与电感串联进行感测，最大电流能力由外部元器件（NMOS 栅极电荷、电感、检流电阻）、栅极驱动器电流能力和开关频率定义。实施过流检测以保护外部 MOSFET。如果在 HS 最小 TON 时间后检测到过流，HS 将关闭，并在开关时钟的下一个上升沿再次打开。过流会导致占空比减少，从而导致输出电压逐渐下降。

BUCK PREREQ 根据下表所示的外部元器件参考值进行外部补偿：

表 6 外部滤波元器件降压预调节器

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{PR}	-20 %	6.8	20%	µH	–	DS-1890
External inductor series resistance	$DCRL_{PR}$	–	8	10	mΩ	Max value to guarantee the efficiency	DS-1891
External capacitor	C_{PR}	-20 %	66	20%	µF	–	DS-1892
External capacitor series resistance	R_{C_PR}	–	10	20	mΩ	Max value to guarantee the efficiency and the stability	DS-1893
External bootstrap capacitor	C_{R1BTS}	-20 %	100	20%	nF	–	DS-1894
External bootstrap capacitor resistance	R_{C_R1BTS}	–	50	–	mΩ	–	DS-1895
External sense resistor	R_{sense}	-1%	10	+1%	mΩ	For 10 A current capability	DS-1896
External sense resistor	R_{sense}	-1%	20	+1%	mΩ	For 5 A current capability	DS-1897
External compensation capacitor	C_{comp}	-20 %	1.5	+20 %	nF	For 5 A current capability	DS-1898
External compensation capacitor	C_{comp}	-20 %	2.7	+20 %	nF	For 10 A current capability	DS-1899
External compensation resistance	R_{comp}	-1%	25	+1%	kΩ	For 5 A current capability	DS-1900
External compensation resistance	R_{comp}	-1%	12	+1%	kΩ	For 10 A current capability	DS-1901

1) 未经过生产测试。

5.1.2 电气特性：BUCK PREREG

表 7 电气特性：BUCK PREREG

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
4.0 V output voltage	V_{R1FB_4V0}	3.6	4	4.4	V	V_{SSC_S} ≥ 5.5 V; dI/dt ≤ 390 A/ms; Output voltage is set to 4 V by HWCFG	DS-1407

（表格续下页……）

表 7 (续) 电气特性：BUCK PREREG

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
4.0 V output voltage accuracy	$V_{R1FB\_4V0\_acc}$	3.88	–	4.08	V	Static; V_{SSC_S} ≥ 5.5 V	DS-2151
5.5 V output voltage	V_{R1FB_5V5}	4.95	5.5	6.05	V	V_{SSC_S} ≥ 6.5 V; dI/dt ≤ 390 A/ms; Output voltage is set to 5V5 by HWCFG	DS-2154
5.5 V output voltage accuracy	$V_{R1FB\_5V5\_acc}$	5.34	–	5.61	V	Static; V_{SSC_S} ≥ 6.5V	DS-2152
Maximum output current	I_{bck_prereg}	5	–	10	A	Max = 10 A with R_{sense} = 10 mΩ; Max = 5 A with R_{sense} = 20 mΩ; I_{bck_prereg} < 5 A if V_{SSC_S} ≤ 8V	DS-2155
Sense input current high side	I_{R1CS1}			100	µA	V_{SSC_S} > 3.6 V; I_{bck_prereg} = 0 *1)*	DS-1410
Sense input current low-side	I_{R1FB}			100	µA	V_{SSC_S} > 3.6 V; I_{bck_prereg} = 0 *1)*	DS-1411
Overcurrent peak detection threshold	$V_{shunt\_R1FB\_OC}$	120	150	180	mV	Overcurrent case not including R_{sense} tolerance	DS-1412
Switching frequency	$f_{sw\_bck\_prereg}$	f_{DCDC} [MIN]/5	f_{DCDC} /5	f_{DCDC} [MAX]/5	MHz	$f_{sw\_bck\_prereg}$ = f_{DCDC}/5	DS-1413
Soft-start time	$t_{ss\_bck\_prereg}$	–	400	715	us	Voltage at pin V_{R1FB} ramps up from 10% to 90% of V_{R1FB}	DS-1414
Maximum duty cycle	$D_{max\_bck\_prereg}$			98	%		DS-1415
High-side peak sourcing current	I_{R1HS_SRC}	200 * x	–	850 * x	mA	V_{R1HS} - V_{R1SW} from 1 V to 4 V V_{QIS} = 5.5 V I_{R1HS_SRC} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; *1)*	DS-2087

（表格续下页……）

表 7　　(续) 电气特性：BUCK PREREG

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High-side peak sinking current	I_{R1HS_SNK}	200 * x		850 * x	mA	V_{R1HS} - V_{R1SW} from 4 V to 1 V; V_{QIS} = 5.5 V I_{R1HS_SNK} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2088
Low-side peak sourcing current	I_{R1LS_SRC}	200 * x	-	850 * x	mA	V_{R1LS} from 1 V to 4 V; V_{QIS} = 5.5 V; I_{R1LS_SRC} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2089
Low-side peak sinking current	I_{R1LS_SNK}	200 * x		850 * x	mA	V_{R1LS} from 4 V to 1 V; V_{QIS} = 5.5 V I_{R1LS_SNK} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2090
Low-side high level gate output voltage vs. source	ΔV_{R1LS}	3.5	4.5	6	V	$\Delta V_{R1LS} = V_{R1LS} - V_{GND}$; $V_{VS} = V_{VIQST} > 6$ V 1)	DS-1514
High-side high level gate output voltage vs. source	$\Delta V_{HS\_R1HS\_R1SW}$	3.5	4.5	6	V	$\Delta V_{HS\_R1HS\_R1SW} = V_{R1HS} - V_{R1SW}$; $V_{VS} = V_{VQST} > 6$ V 1)	DS-1515
High-side gate rise time	t_{R1HS_r}	23	–	55	ns	V_{R1HS} from 10% to 90%; C_{R1HS} = 3 nF 1)	DS-1516
High-side gate fall time	t_{R1HS_f}	24	–	51	ns	V_{R1HS} from 90% to 10%; C_{R1HS} = 3 nF 1)	DS-1517

（表格续下页……）

表 7　　(续) 电气特性：BUCK PREREG

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low-side gate rise time	t_{R1LS_r}	23	–	55	ns	V_{R1LS} from 10% to 90%; C_{R1LS} = 3 nF 1)	DS-1518
Low-side gate fall time	t_{R1LS_f}	24	–	51	ns	V_{R1LS} from 90% to 10%; C_{R1LS} = 3 nF 1)	DS-1519

1）　未经过生产测试，由设计指定

5.2　　BUCK CORE（降压核心调节器）

5.2.1 功能描述：BUCK CORE

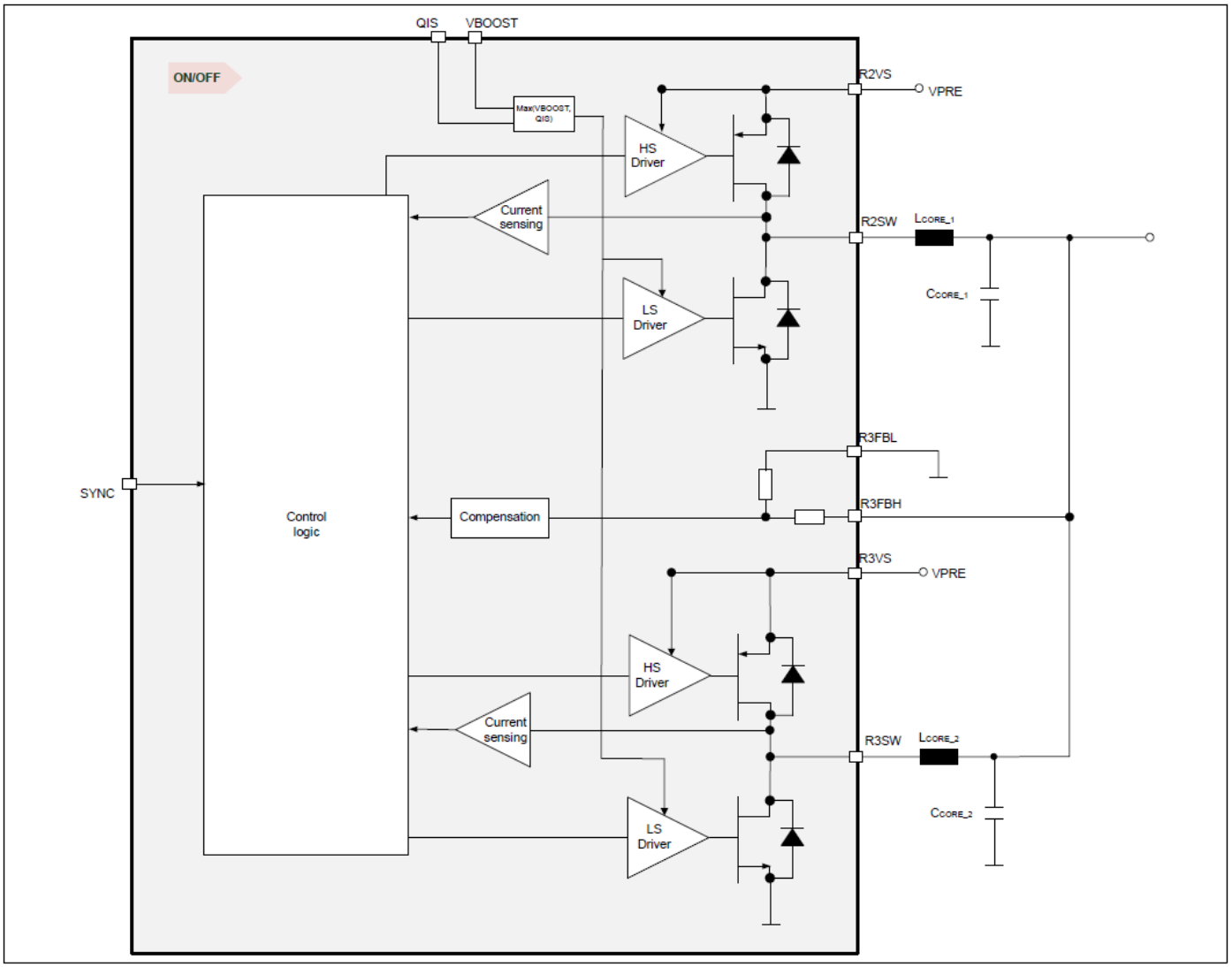

图 5 BUCK CORE 调节器框图

该器件提供双相降压调节器，可在V_{R3FBH}和 V_{R3FBL} 之间生成输出电压，并以 I_{bck_core} 输出电流为微控制器核心供电。

降压核心的默认输出电压可以在 SPI 寄存器位 **VCORESTAT.VOUT** 读取。

降压核心的输出电压可以通过 SPI 寄存器位 **BUCK_CORE_PW_VSEL.VSEL**进行调整。

该器件根据 SPI 接口的请求，在 V_{R3FBH_rg} 范围内以 V_{R3FBHL_step} 为单位步进提供电压调节。当启动或从 R1 复位级别事件恢复（参见复位级别）时，调节器将以其默认值 1.025 V 启动。

其他默认 OTP（一次性可编程）值可作为默认选项使用：

0.7 V, 0.8 V, 0.9 V, 0.95 V, 0.9625 V, 0.975 V, 0.9875 V, 1.0 V, 1.0125 V, 1.025 V, 1.0375 V, 1.05 V, 1.15 V

注释： *用于配置BUCKCORE 输出电压的相应寄存器（BUCK_CORE_PW_VSEL、BUCK_CORE_RS_VSEL、VCORESTAT、VCOREMONSTAT）的复位值与用户在器件启动或从复位事件恢复时读取的值不对应。启动过程中，该寄存器将被预先设置的默认值覆盖。*

降压核心的欠压和过压监测阈值根据静态电压调节期间选择的调节器设置点进行调整。

实现了逐周期限制模式下最大 $I_{OC\_bck\_core}$ 的过流保护。

降压核心调节器通过低边 MOSFET 中的过载保护来实现，并在源-漏极方向上限制 $I_{OL\_bck\_core}$

降压核心调节器根据下表给出的外部元器件参考进行内部补偿：

表 8　　外部滤波元器件（BOM）降压核心调节器

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor 1	$L_{buck\_core\_1}$	-20 %	1	20%	µH	–	DS-1902
External inductor series resistance 1	$DCR_{L\_buck\_core\_1}$	–	30	37	mΩ	–	DS-1903
External inductor 2	$L_{buck\_core\_2}$	-20 %	1	20%	µH	–	DS-1904
External inductor series resistance 2	$DCR_{L\_buck\_core\_2}$	–	30	37	mΩ	–	DS-1905
External capacitor 1	$C_{buck\_core\_1}$	-20 %	47	20%	µF	–	DS-1906
External capacitor series resistance 1	$ESR_{C\_buck\_core\_1}$	–	–	5	mΩ	–	DS-1907
External capacitor 2	$C_{buck\_core\_2}$	-20 %	47	20%	µF	–	DS-1908
External capacitor series resistance 2	$ESR_{C\_buck\_core\_2}$	–	–	5	mΩ	–	DS-1909

1)　未经过生产测试

5.2.2　电气特性：BUCK CORE

表 9　　电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{R*VS}	V_{R1FB_4V0}	–	V_{R1FB_5V5}	V	$V_{R*VS} = V_{R2VS} = V_{R3VS}$	DS-1418
Default output voltage	V_{R3FBH}	–	1.025	–	V	–	DS-2085
Maximum output current	$I_{bck\_core\_ph}$	–	–	3.5	A	Per phase	DS-1421

（表格续下页……）

表 9 (续) 电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Minimum output current	$I_{bck\_core\_min}$	1	–	–	mA	1)	DS-1428
Overcurrent limitation	$I_{OC\_bck\_core\_ph}$	4.3	–	5.3	A	Per phase	DS-1423
Overload limitation	$I_{OL\ bck\ core\ ph}$	4.3	–	5.3	A	Per phase	DS-1529
Static voltage range	V_{R3FBH_rg}	0.7	–	1.1	V	V_{R3FBH_rg} is programmable (6 bits) between 0.7V and 1.1V via SPI with a default value V_{R3FBH} From 0.7V to 0.8875V: V_{R2VS} = V_{R3VS} = V_{R1FB_4V0}	DS-1419
Static voltage steps	V_{R3FBH_step}	–	12.5	–	mV	–	DS-1530
Switching frequency	$f_{sw\_bck\_core}$	(f_{DCDC}[MIN]/5) × 3	(f_{DCDC}/5) × 3	(f_{DCDC}[MAX]/5) × 3	MHz	–	DS-1531
Static tolerance including ripple	dV_{R3FBHL_stat}	-2	–	+2	%	Under static output load.	DS-1420
Response time for static voltage scaling	$T_{R\_TO\_SVS}$	0.9 * $T_{R\_TO\_SVS}$[typ]	20 + 50 * ((V_{R3FBH_end} - V_{R3FBH_start}) / dV_{R3FBH_step}) + 20	1.1 * $T_{R\_TO\_SVS}$[typ]	us	V_{R3FBH_end} is the target V_{R3FBH} output voltage; V_{R3FBH_start} is the starting V_{R3FBH} output voltage; I_{bck_core} ≥ 200 mA to guarantee the BUCK_CORE response time for static voltage scaling 1)	DS-1422

（表格续下页……）

表 9 (续) 电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Peak efficiency	$P_{eff\_bck\_core}$	83	87	–	%	50% of max load (I_{bck_core}/2) including typical external components and excluding board parasitics at RT 1)	DS-1424
Soft-start time	$t_{ss\_bck\_core}$	–	0.5	–	ms	Voltage at pin V_{R3FBH} ramps up from 10% to 90% of V_{R3FBH}	DS-1425
Load step response for high load	dV_{R3FBH_HL}	-0.04 *V_{R3FBH}	–	0.04 *V_{R3FBH}	mV	(1) 0.7 V ≤ V_{R3FBH} ≤ 0.9 V; V_{R2VS} = V_{R3VS} = 4 V; (2) 0.9 V < V_{R3FBH} ≤ 1.1 V; V_{R2VS} = V_{R3VS} = 5.5 V or V_{R2VS} = V_{R3VS} = 4 V; dI_{buck_core} < 1200 mA; 100 mA ≤ I_{bck_core} ≤ 5000 mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs dI_{buck_core} > -1200 mA; 2100mA ≤ I_{bck_core} ≤ 7000mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs series resistance 10mOhm between R3FBH and load (VDD supply pin MCU); series resistance 5 mΩ between R3FBL and load ground (supply ground pin of MCU); Including static output voltage accuracy 1)	DS-2147

（表格续下页……）

表 9 (续) 电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Load step response for medium load	dV_{R3FBH_ML}	-0.035*V_{R3FBH}	–	0.035*V_{R3FBH}	mV	(1) 0.7 ≤ V_{R3FBH} ≤ 0.9; V_{R3VS} = 4V (2) 0.9 < V_{R3FBH} ≤ 1.1V; V_{R3VS} = 5.5V or V_{R3VS} = 4V dI_{buck_core} < 500mA; 100mA ≤ I_{bck_core} ≤ 6500mA; load step rise/fall time = 100ns; $t_{settling}$=10µs dI_{buck_core} > -500mA; 600mA ≤ I_{bck_core} ≤ 7000mA; load step rise/fall time = 100ns; $t_{settling}$=10µs series resistance 10mOhm between R3FBH and load (VDD supply pin MCU); series resistance 5mOhm between R3FBL and load ground (supply ground pin of MCU); Including static output voltage accuracy [1)]	DS-2148
Line step response	dV_{R3FBH_line}	-0.015*V_{R3FBH}	–	0.015*V_{R3FBH}	mV	(1) Maximum load: dV/dT = 50 V/ms; step on V_{R2VS} = V_{R3VS} from 3.6 V to 4.4 V if V_{R1FB} = V_{R1FB_4V0}; 100 mA ≤ I_{bck_core} ≤ 7000 mA (2) Maximum load: dV/dT = 50 V/ms; step on V_{R2VS} = V_{R3VS} from 4.95 V to 6.05 V if V_{R1FB} = V_{R1FB_5V5}; 100 mA ≤ I_{bck_core} ≤ 7000 mA [1)]	DS-1429
Internal pull-down resistor	R_{R3FBH_PD}	2.5	–	8.5	Ω	V_{R3FBH} = 1 V	DS-1532
BUCKCORE high side on-resistance (4V0)	$R_{DS(on)\_HS\_BUCKCORE\_4V0}$	–	67	118	mΩ	V_{R1FB} = V_{R1FB_4V0} [1)]	DS-2053
BUCKCORE high side on-resistance (5V5)	$R_{DS(on)\_HS\_BUCKCORE\_5V5}$	–	58	101	mΩ	V_{R1FB} = V_{R1FB_5V5}	DS-2063
BUCKCORE low side on-resistance	$R_{DS(on)\_LS\_BUCKCORE}$	–	33	63	mΩ	–	DS-2146

（表格续下页……）

表 9　　(续) 电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_core\_5V5}$	4.2	–	6.3	V/ns	$V_{R2VS} = V_{R3VS} = 5.5$ V $SR_{bck\_core\_5V5} = 0.8 * V_{R2VS} / trise$, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 00_b 1)	DS-2094
Switching output slew rate	$SR_{bck\_core\_5V5}$	2.8		5.9	V/ns	$V_{R2VS} = V_{R3VS} = 5.5$ V $SR_{bck\_core\_5V5} = 0.8 * V_{R2VS} / trise$, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 01_b 1)	DS-2099
Switching output slew rate	$SR_{bck\_core\_5V5}$	1.1	–	3.6	V/ns	$V_{R2VS} = V_{R3VS} = 5.5$ V $SR_{bck\_core\_5V5} = 0.8 * V_{R2VS} / trise$, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 10_b 1)	DS-2098
Switching output slew rate	$SR_{bck\_core\_4V}$	2.8	–	4.9	V/ns	$V_{R2VS} = V_{R3VS} = 4$ V $SR_{bck\_core\_4V} = 0.8 * V_{R2VS} / trise$, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 00_b 1)	DS-2097

（表格续下页……）

表 9 (续) 电气特性：BUCK CORE

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_core\_4V}$	1		4.4	V/ns	$V_{R2VS} = V_{R3VS} = 4$ V $SR_{bck\_core\_4V} = 0.8 * V_{R2VS}$ / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 01_b 1)	DS-2096
Switching output slew rate	$SR_{bck\_core\_4V}$	0.38	–	1.3	V/ns	$V_{R2VS} = V_{R3VS} = 4$ V $SR_{bck\_core\_4V} = 0.8 * V_{R2VS}$ / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 10_b 1)	DS-2095

1） 未经过生产测试，由设计指定

5.3 BUCK IF（接口调节器）

5.3.1 功能描述：BUCK IF

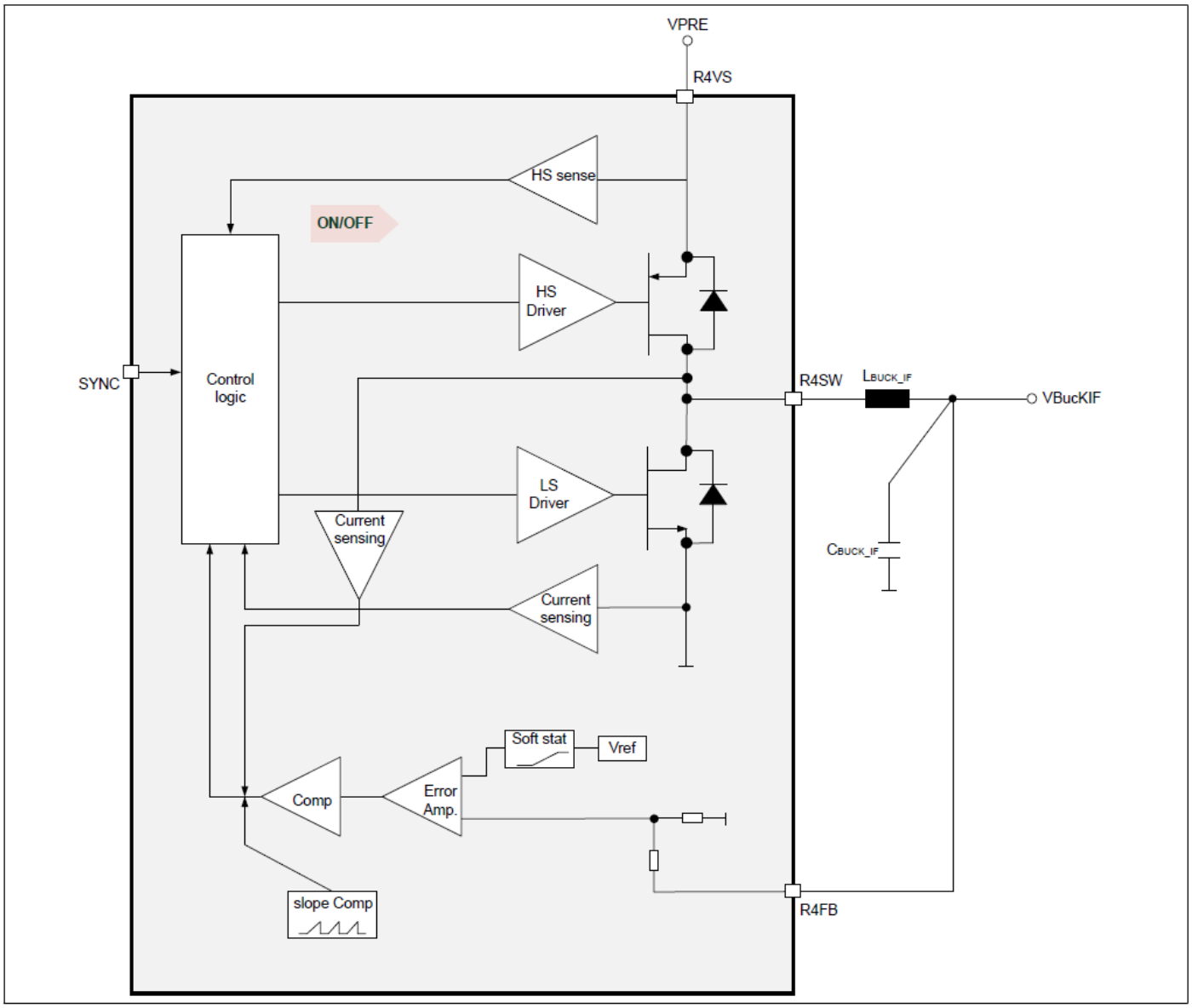

图 6 BUCKIF 框图

该器件提供降压接口调节器，可通过引脚 R4FB 处的 I_{bck_if} 输出电流将 PREREG 输出电压 VPRE 降压至输出电压 $V_{VBUCKIFo}$

***注释：**该电压可用于为高速接口供电。*

BUCK IF 调节器在逐周期限制模式下通过最大 $I_{OC\_bck\_if}$ 的过流保护来实现。

BUCK IF 调节器通过低边 MOSFET 中的过载保护来实现，并在源-漏极方向上限制 $I_{OL\ bck\ ifo}$

如果应用中使用了 BUCK IF 调节器，则器件在启动期间提供自动检测。如果不使用，BUCKIF 的引脚必须按照以下配置连接：

- R4VS：连接接地点
- R4FB：悬空
- R4SW：悬空

注释：　如果不使用，BUCK IF 将被排除在电源序列之外。

BUCK IF 调节器根据下表所示的内部补偿方式，对外部元器件参考值进行补偿：

表 10　外部滤波元器件（BOM）BUCK IF

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{BUCK_IF}	-20 %	2.2	20%	µH	–	DS-1910
External inductor series resistance	$D_{CRL\_BUCK\_IF}$		20	80	mΩ	Max value to guarantee the efficiency	DS-1911
External capacitor	C_{BUCK_IF}	25	47	(+20 %)	µF	–	DS-1912
External capacitor series resistance	$ESR_{C\_BUCK\_IF}$		8	15	mΩ	Max value to guarantee the efficiency	DS-1913

1)　未经过生产测试

5.3.2　电气特性：BUCK IF

表 11　电气特性：BUCK IF

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{R4VS}	V_{R1FB_4V0}	–	V_{R1FB_5V5}	V	–	DS-1431
Output voltage excluding ripple	V_{R4FB}	1.764	1.8	1.836	V	Static output voltage excluding ripple; minimum load: $I_{bck\_if} \geq$ 20mA	DS-1433
Maximum output current	I_{bck_if}	–	–	1.2	A	*1)*	DS-1434
Minimum output current	$I_{buck\_if\_min}$	200	–	–	µA	*1)*	DS-2042
Overcurrent limitation	$I_{OC\_bck\_if}$	1.5	–	2.6	A	–	DS-1435
Peak efficiency	$P_{eff\_bck\_if}$	80	88	–	%	I_{buck_if} from 0.2 A up to 1 A, including typical external components at RT *1)*	DS-1436
Switching frequency	$f_{sw\_bck\_IF}$	f_{DCDC} [MIN]	f_{DCDC}	f_{DCDC} [MAX]	MHz	–	DS-1523

（表格续下页……）

表 11　　（续）电气特性：BUCK IF

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching frequency 2	$f_{sw\_bck\_IF\_2}$	0.9 * $f_{sw\_bck\_IF\_2}$[typ]	2	1.1 * $f_{sw\_bck\_IF\_2}$[typ]	MHz	Only applicable if: FREQ_SPREAD.FRE_SP_EN = 1 AND FREQ_SPREAD.FRE_SP_BUCKIF_EN = 0	DS-2050
Soft-start time	$t_{ss\_bck\_if}$	–	230	400	µs	Voltage at pin V_{R4FB} ramps up from 10% to 90% of V_{R4FB} 5 mA < I_{R4FB} < 500 mA	DS-1437
Load step response	ΔV_{R4FB_load}	-67	–	67	mV	ΔI_{bck_if} < 500 mA; 20 mA ≤ I_{bck_if} ≤ 500 mA; load step rise/fall time = 100 ns; ΔI_{bck_if} > -500 mA; 1000 mA ≤ I_{bck_if} ≤ 520 mA; load step rise/fall time = 100 ns 1)	DS-1439
Load step response max dynamic range	$\Delta V_{R4FB\_load\_mdr}$	-45	–	45	mV	ΔI_{bck_if} > -700 mA; I_{bck_if} = 1000 mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs 1)	DS-1441
Line step response	ΔV_{R4FB_line}	-45	–	45	mV	Step on V_{R4VS} from 3.88 V to 3.66 V in 10 us and from 3.66 V to 3.88 V in 10 us if V_{R1FB} = V_{R1FB_4V0}; Step on V_{R4VS} from 5.61 V to 5.97 V in 10 us and from 5.97 V to 5.61 V in 10 us if V_{R1FB} = V_{R1FB_5V5}; 20mA ≤ I_{bck_if} ≤ 1000mA 1)	DS-1443
Overload limitation	$I_{OL\ bck\ if}$	1.5	–	2.1	A	–	DS-1522
Internal pull-down resistor	R_{R4FB_PD}	2.5	–	13.5	Ω	–	DS-1525
BUCKIF high side on-resistance (4V0)	$R_{DS(on)\_HS\_BUCKIF\_4V0}$	–	214	372	mΩ	V_{R1FB} = V_{R1FB_4V0} 1)	DS-2055
BUCKIF high side on-resistance (5V5)	$R_{DS(on)\_HS\_BUCKIF\_5V5}$	–	181	309	mΩ	V_{R1FB} = V_{R1FB_5V5}	DS-2065

（表格续下页……）

表 11　　（续）电气特性：BUCK IF

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BUCKIF low side on-resistance (4V0)	$R_{DS(on)\_LS\_BUCKIF\_4V0}$	–	92	158	mΩ	$V_{R1FB} = V_{R1FB\_4V0}$ 1)	DS-2056
BUCKIF low side on-resistance (5V5)	$R_{DS(on)\_LS\_BUCKIF\_5V5}$	–	82	139	mΩ	$R_{DS(on)\_HS\_BUCKIF\_5V5}$	DS-2066
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 00_b 1)	DS-2100
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 01_b 1)	DS-2101
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 10_b 1)	DS-2102

（表格续下页……）

表 11　（续）电气特性：BUCK IF

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_if\_4V}$	1.3	–	2.6	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 00_b *1)*	DS-2103
Switching output slew rate	$SR_{bck\_if\_4V}$	1.3	–	2.6	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 01_b *1)*	DS-2104
Switching output slew rate	$SR_{bck\_if\_4V}$	1.1	–	2.1	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 10_b *1)*	DS-2105

1)　未经过生产测试，由设计指定

5.4　BOOST（升压调节器）

5.4.1 功能描述：BOOST

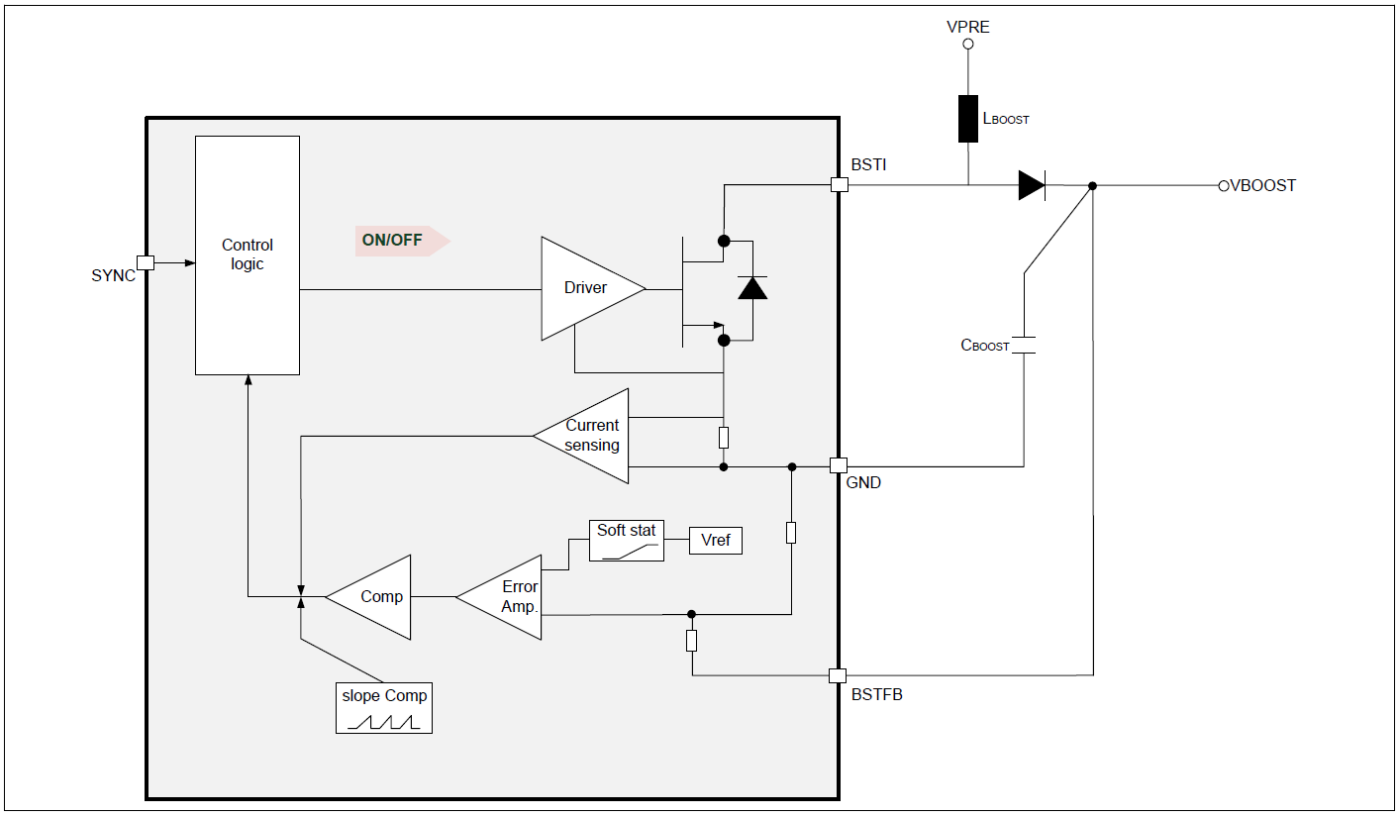

图 7 BOOST 框图

器件提供了一个升压调节器，可将 PREREG 输出电压 VPRE 提升至具有外部二极管的输出电压 VBOOST，以确保后期功率块。

如果应用中使用了升压调节器，则器件会在启动期间提供自动检测。如果在应用中不使用 BOOST，请确保 BSTI 和 BSTFB 引脚连接如下：

- BSTI：连接到接地点
- BSTFB： 连接到 R1FB

升压调节器根据下表所示的内部补偿方式，对外部元器件参考值进行补偿：

表 12 外部滤波元器件 BOOST

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{bst}	-20 %	3.3	20%	µH	–	DS-1914
External inductor series resistance	DCR_{L_bst}	–	20	50	mΩ	–	DS-1915
External capacitor	C_{bst}	-20 %	10	20%	µF	–	DS-1916

（表格续下页……）

表 12　（续）外部滤波元器件 BOOST

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External capacitor series resistance	ESR_{C_bst}	–	10	20	mΩ	–	DS-1917
External Schottky diode forward voltage	V_{Dbst}	–	0.4	0.52	V	@I_{D_boost} =1 A	DS-1951

1)　未经过生产测试

5.4.2　电气特性：BOOST

表 13　电气特性：BOOST

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{in_boost}	2.7	–	5.61	V	1)	DS-2150
Output voltage	V_{BSTFB}	5.63	5.8	5.97	V	I_{LOAD_BOOST} < 1A: 3.9 V ≤ V_{R1FB_4V0} ≤ 4.1 V, 5.33V ≤ V_{R1FB_5V5} ≤ 5.61 V; I_{LOAD_BOOST} < 0.650 A; 2.59 V ≤ V_{R1FB} ≤ 2.71 V	DS-1447
Load current	I_{LOAD_BOOST}	–	–	1	A	Total load (internal and external load)	DS-1509
Switching frequency	f_{sw_bst}	f_{DCDC} [MIN]	f_{DCDC}	f_{DCDC} [MAX]	MHz	–	DS-1526
Overcurrent limitation	I_{OC_BSTI}	3.5	4	4.5	A	–	DS-1448
Efficiency	P_{eff_bst}	81	85	–	%	Including typical BOM; @27°C; 150mA ≤ I_{LOAD_BOOST} ≤ 950mA 1)	DS-1449
Soft-start time	t_{ss_boost}	–	650	1000	µs	Voltage at pin V_{BSTFB} ramps up from 10% to 90% of V_{BSTFB}	DS-1450
Pull-down resistor	R_{BSTFB_PD}	12	–	76	Ω	–	DS-1527
BOOST low side on-resistance	$R_{DS(on)\_LS\_BOOST}$	–	114	221	mΩ	–	DS-2057

（表格续下页……）

表 13　　（续）电气特性：BOOST

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	SR_{bst}	0.50		2.2	V/ns	SR_{bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 00_b 1)	DS-2091
Switching output slew rate	SR_{bst}	0.4		1.5	V/ns	S_{R_bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 01_b 1)	DS-2092
Switching output slew rate	SR_{bst}	0.15		0.8	V/ns	S_{R_bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 10_b 1)	DS-2093

1）　未经过生产测试，由设计指定

5.5　通信 LDO（QCO）

5.5.1 功能描述：通信 LDO（QCO）

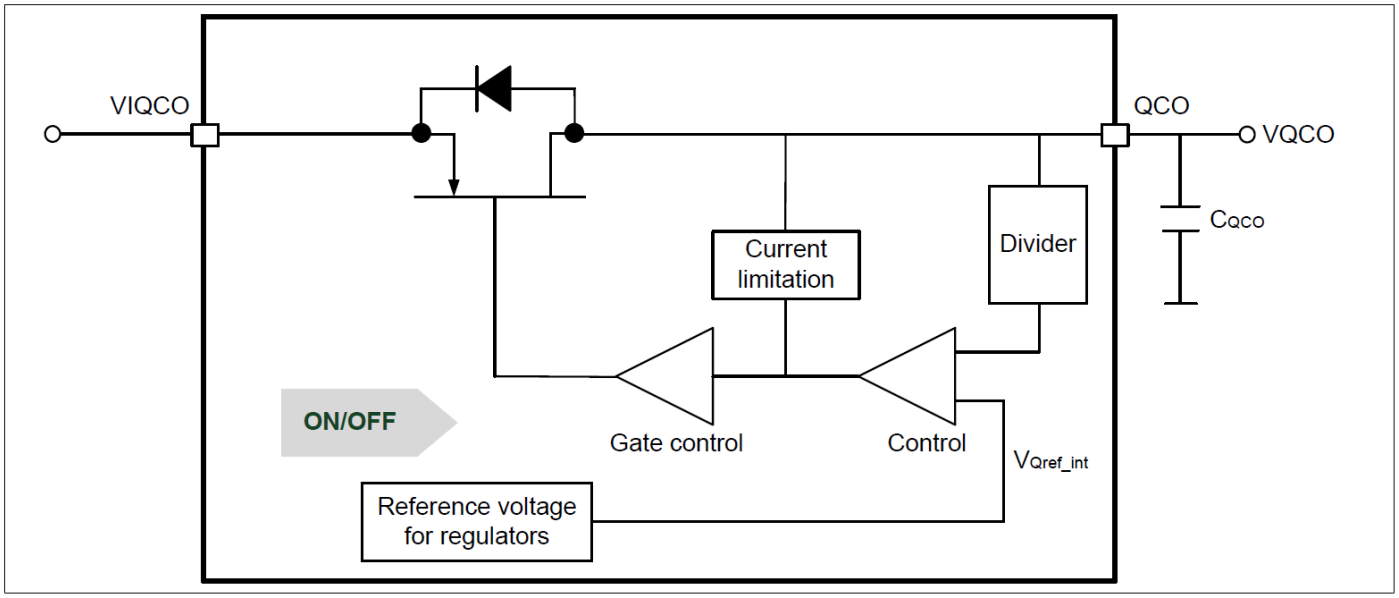

图 8 LDO-QCO 框图

该器件提供低压差线性稳压器 (LDO-QCO)，可通过产生稳压输出电压 V_{QCO}和 I_{QCO} 输出电流来为微控制器供电。调节器由升压调节器输出供电。作为配置选项，调节器也可以直接从预调节器输出提供。

控制环路的稳定性取决于负载电流、输出电容的特性和芯片结温。根据下表指定的电气特性选择输出电容（电容值 C_{QCO}和等效串联电阻 ESR_{C_QCO}），以确保稳定运行。输出电容可以是一个电容，也可以是遵循整个电容范围的一组电容。

注释： *该电压可用于为通信器件供电，例如CAN 收发器。*

为了保护通信电源免受过载影响，限流将输出电流 I_{QCO} 限制为指定限值I_{QCO_max}。

5.5.2 电气特性：通信 LDO (QCO)

表 14 电气特性：通信 LDO (QCO)

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QCO}	4.9	5	5.1	V	0 mA < I_{QCO} < 600 mA	DS-1453
Output current	I_{QCO}	0	–	600	mA	–	DS-1454
Output current limitation	I_{QCO_max}	650	–	1100	mA	–	DS-1455

（表格续下页……）

表 14　（续）电气特性：通信 LDO (QCO)

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drop voltage	V_{dr_QCO}	–	–	500	mV	I_{QCO} < 600 mA	DS-1456
Power supply ripple rejection	$PSRR_{QCO}$	26	–	–	dB	V_{VIQVR_VIQCO} = 5.8V with 100mVpp at 2.2 MHz and Iload ≤ I_{QCO} ESR_{C_QCO} ≤ 50mΩ 1)	DS-1457
Load regulation	ΔV_{QCO}	–	40	70	mV	100 µA < I_{QCO} < 600 mA	DS-1458
Output capacitor	C_{QCO}	1	–	47	µF	1)	DS-1459
Output capacitor equivalent series resistance	ESR_{C_QCO}	–	–	100	mΩ	1)	DS-1460
Soft-start time	t_{ss_QCO}	–	290	500	µs	Voltage at pin QCO ramps up from 10% to 90% of V_{QCO}; -60 mA < I_{QCO} < -5 mA; C_{QCO} = 4.7 µF	DS-2046

1)　未经过生产测试，由设计指定

5.6　基准 LDO (QVR)

5.6.1　功能描述：基准LDO (QVR)

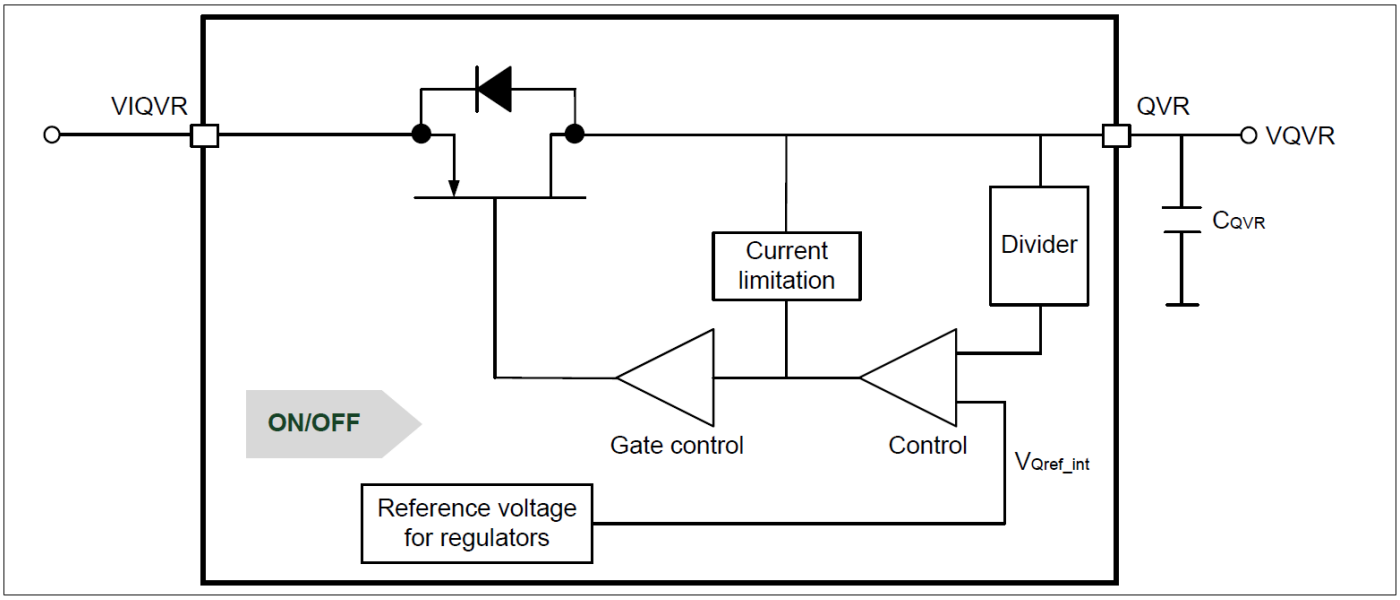

图 9　LDO-QVR 框图

该器件提供一个低压差调节器 LDO-VREF，它生成一个调节输出电压 V_{QVR} 和 I_{QVR}输出电流，为微控制器供电。调节器由升压调节器输出供电。作为配置选项，调节器也可以直接从预调节器输出提供。

控制环路的稳定性取决于负载电流、输出电容的特性和芯片结温。根据下表指定的电气特性选择输出电容（电容值 C_{VREF}和等效串联电阻 ESR_{C_QVR}），以确保稳定运行。输出电容可以是一个电容，也可以是整个电容范围内的一组电容。

注释： *该电压可用作微控制器中ADC 的基准电压。*

为了保护通信电源免受过载影响，限流将输出电流 I_{QVR} 限制为指定限值 I_{QVR_max}。

可以通过寄存器读取 OC 故障状态，并且一旦 OC 故障过期，就可以通过 SPI 的写入命令清除该状态。

5.6.2 电气特性：基准 LDO (QVR)

表 15 电气特性：基准 LDO (QVR)

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QVR}	4.95	5	5.05	V	0 mA < I_{QVR} < 150 mA	DS-1462
Output current	I_{QVR}	0	–	150	mA	–	DS-1463
Output current limitation	I_{QVR_max}	170	–	345	mA	–	DS-1464
Drop voltage	V_{dr_QVR}	–	–	400	mV	I_{QVR} < 150 mA	DS-1465
Load regulation	ΔV_{QVR}	–	4.5	9	mV	100 µA < I_{QVR} < 150 mA	DS-1466
Power supply ripple rejection	$PSRR_{QVR}$	26	–	–	dB	V_{IQVR_VIQCO} = 5.8V with 100mVpp at 2.2 MHz and Iload ≤ I_{QVR} ESR_{C_QVR} ≤ 50mΩ 1)	DS-1467
Output capacitor	C_{QVR}	1	–	10	µF	1)	DS-1468
Output capacitor equivalent series resistance	ESR_{C_QVR}	–	–	100	mΩ	1)	DS-1469
Soft-start time	t_{ss_QVR}	–	280	520	µs	Voltage at pin QVR ramps up from 10% to 90% of V_{QVR}; -15 mA < I_{QVR} < -5 mA; C_{QVR} = 4.7 µF	DS-2048

1) 未经过生产测试，由设计指定

5.7 MCU-LDO（QUC）

5.7.1 功能描述：MCU-LDO（QUC）

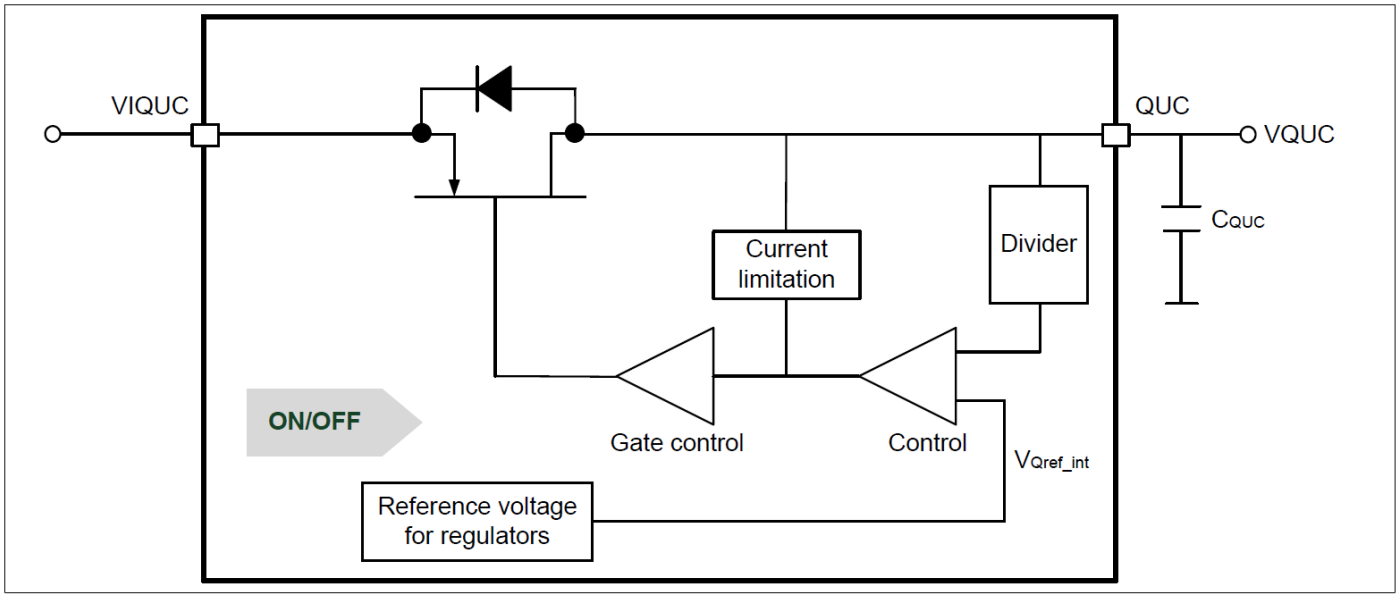

图 10 LDO-QUC 框图

该器件提供一个低压差调节器 LDO -QUC，它生成一个调节输出电压 V_{QUC} 和 I_{QUC} 输出电流，为微控制器供电。调节器由升压调节器输出供电。作为配置选项，调节器也可以直接从预调节器输出提供。

控制环路的稳定性取决于负载电流、输出电容的特性和芯片结温。根据下面指定的电气特性表选择输出电容（电容值 C_{QUC} 和等效串联电阻 ESR_{C_QUC}），以确保稳定运行。输出电容可以是一个电容，也可以是遵循整个电容范围的一组电容。

为了保护 QUC 电源免受过载影响，限流将输出电流 I_{QUC} 限制为指定限值 I_{QUC_max}。

***注释：** 当输出引脚QUC 吸收的电流受到限制时，输出电压V_{QUC}将下降。*

5.7.2 电气特性：MCU-LDO（QUC）

表 16 电气特性：MCU-LDO（QUC）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QUC}	3.23	3.3	3.37	V	0 mA < I_{QUC}< 600 mA	DS-1472
Output current	I_{QUC}	0	–	600	mA	–	DS-1473
Output current limitation	I_{QUC_max}	650	–	1100	mA	–	DS-1474
Drop voltage	ΔV_{QUC}	–	–	500	mV	I_{QUC}< 600 mA	DS-1476
Load regulation	ΔV_{QUC_load}	–	40	60	mV	100 µA < I_{QUC}< 600 mA	DS-1478

（表格续下页……）

表 16　（续）电气特性：MCU-LDO（QUC）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output capacitor	C_{QUC}	2.2	4.7	22	µF	1)	DS-1479
Output capacitor equivalent series resistance	ESR_{C_QUC}	–	–	100	mΩ	1)	DS-1480
Power supply ripple rejection	$PSRR_{QUC}$	26	–	–	dB	V_{IQUC} = 5.8 V with 100 mVpp at 2.2 MHz and Iload ≤ I_{QUC} ESR_{C_QUC} ≤ 50 mΩ 1)	DS-1481
Soft-start time	t_{ss_QUC}	–	290	500	µs	Voltage at pin QUC ramps up from 10% to 90% of V_{QUC}; -60 mA < I_{QUC} < -5 mA; C_{QUC} = 4.7 µF 1)	DS-2047

1)　未经过生产测试，由设计指定

5.8　待命 LDO（QST）

5.8.1　功能描述：待命 LDO（QST）

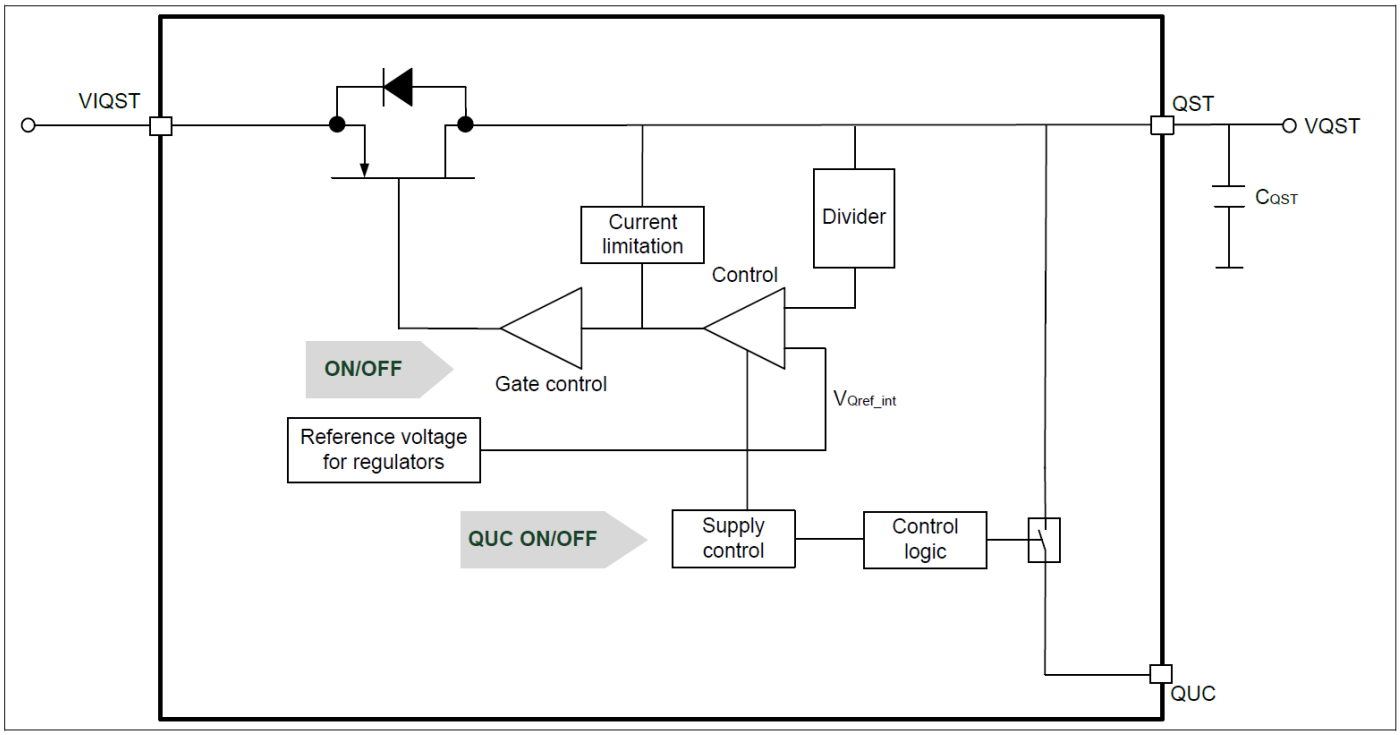

图 11　LDO QST 框图

该器件提供一个线性低压差调节器 LDO-QST，它可以生成一个调节输出电压 V_{QST} 和 I_{QST}输出电流。

器件启动后，引脚 QST 上的输出电压 V_{QST} 由输入电压 V_{IQST} 生成。
如果 LDO-QUC 启用，则输出电压 V_{QST} 由引脚 QUC 处的输入电压 V_{QUC} 提供，以优化电源拓扑，获得更高的效率。

控制环路的稳定性取决于负载电流、输出电容的特性和芯片结温。根据下表指定的电气特性选择输出电容（电容值 C_{QST}和等效串联电阻 ESR_{C_QST}），以确保稳定运行。输出电容可以是一个电容，也可以是整个电容范围内的一组电容。

QST 调节器可以通过受保护的 SPI 通信来启用或禁用。
为了保护备用电源免受过载影响，限流将输出电流 I_{QST} 限制为指定的限值 I_{QST_max}。
可以通过寄存器读取 OC 故障状态，并且一旦 OC 故障过期，就可以通过 SPI 的写入命令清除该状态。

注释： *当输出引脚QST 吸收的电流受到限制时，输出电压V_{QST}将下降。*

5.8.2 电气特性：待命 LDO（QST）

表 17 电气特性：待命 LDO（QST）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QST}	3.17	3.3	3.43	V	0 mA < I_{QST} < 30 mA	DS-1487
Output current	I_{QST}	0	–	30	mA	QUC OFF	DS-1498
Output current limitation	I_{QST_max}	40	60	90	mA	QUC OFF	DS-1488
Soft-start time	$t_{ss\_QST.}$	–	255	–	µs	Voltage at pin QST ramps up from 10% to 90% of V_{QST}; -5 mA < I_{QST} < -1 mA; C_{QUC} = 4.7 µF	DS-1497
Transient line regulation 1	$\Delta V_{QST\_tr\_line}$	–	–	70	mV	I_{QST} < 30 mA; V_{IQST} from 10 V to 14 V voltage step in Δt = 30 µs; QUC OFF	DS-1490
Transient line regulation 2	$\Delta V_{QST\_tr\_line2}$	–	–	140	mV	I_{QST} < 30 mA; V_{IQST} from 6 V to 14 V voltage step in Δt = 500 µs; QUC OFF	DS-1491
Load regulation	ΔV_{QST_load}	–	20	40	mV	100 µA < I_{QST} < 15 mA; QUC OFF	DS-1493

（表格续下页……）

表 17　　（续）电气特性：待命 LDO（QST）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply ripple rejection	$PSRR_{QST}$	30	–	–	dB	Vbatt = 13.5 V, 100 mVpp, ESR <= 50 mOhm, f = 100 Hz and f = 100 kHz 1)	DS-1496
Output capacitor	C_{QST}	0.47	–	10	µF	1)	DS-1494
Output capacitor equivalent series resistance	ESR_{C_QST}	–	–	200	mΩ	1)	DS-1495
Drop voltage RT	ΔV_{QST_RT}	–	–	380	mV	I_{QST} < 30 mA; at T_j = 27°C	DS-1721
Drop voltage HT	ΔV_{QST_HT}	–	–	600	mV	I_{QST} < 30 mA; at T_j = 155°C	DS-1489
Dropout voltage when QUC ON	ΔV_{QUC_QST}	–	–	300	mV	I_{QST} = 30 mA	DS-2003

1）　未经过生产测试，由设计指定

5.9　　激活放电

由器件的调节器之一生成的每个输出轨都包含激活放电功能。该放电功能由一个内部下拉电阻组成。当调节器通过 SPI 被禁用或因检测到故障而关闭时（这也包括状态转换到 FAILSAFE），放电路径被激活并对相应的输出轨放电。除了升压调节器外，如果在 SLEEP 或 STANDBY 状态没有使用调节器，则此放电特性在此期间也保持激活状态。

6 安全开关 (SSW)

6.1 功能描述：安全开关 (SSW)

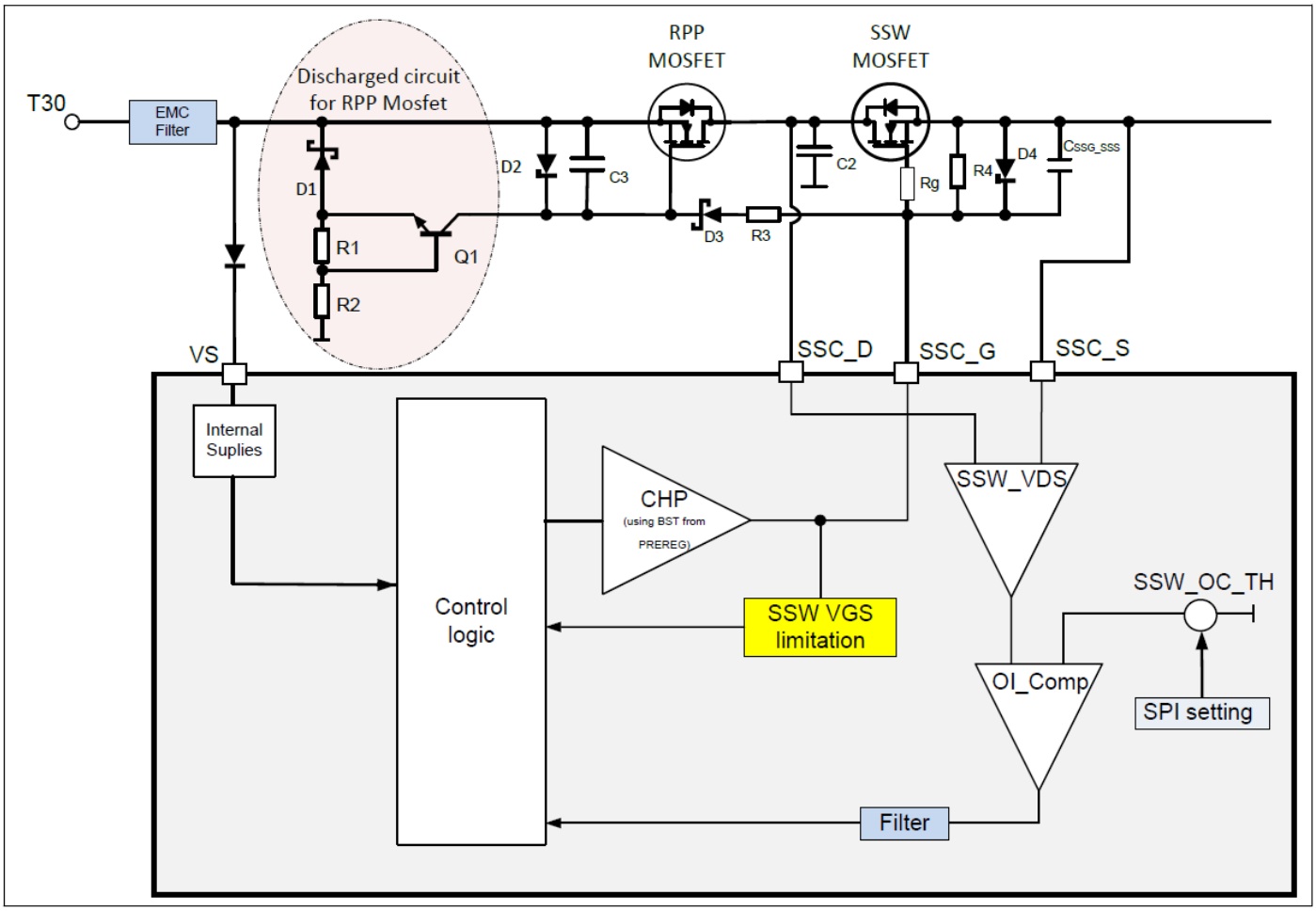

图 12 SSW 和 RPP 框图

器件提供一个驱动器来控制外部 n 沟道功率 MOSFET（反接保护（RPP）MOSFET和安全开关（SSW）MOSFET）。

两个 MOSFET 的栅极都连接到 SSC_G。

外部功率 MOSFET 的激活是根据故障反应表和运行模式驱动的。

在反向电池的情况下，RPP MOSFET的栅极通过外部电路放电。SSW MOSFET 的源极连接到 SSC_S 引脚，漏极连接到 SSC_D 引脚。

驱动器电路包括 SSW MOSFET 上的过流检测（检测源极和漏极之间的压降）。

过流检测的阈值可通过 SPI 寄存器位 **DEV_PW_CFG2.SSW_OC_TH** 进行编程。

如果漏源电压超过检测阈值（SSW_{OC_TH}）的时间长于过流检测时间（t_{fil_OC}），则检测到过流。

器件在启动时自动检测输入侧安全开关保护 MOSFET 的使用情况，并将自动检测结果存储到状态寄存器中。

如果未使用安全开关，则必须按照以下配置连接相应的引脚：

- SSC_D：连接到接地点

- SSC_G： 连接到 PREREG 的输入端
- SSC_S： 连接到 PREREG 的输入端

6.2 电气特性：安全开关（SSW）

表 18 电气特性：安全开关

V_{VS}= 6.0 V 至 36 V； T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level gate output voltage vs. source	ΔV_{SSG_SSS}	4	4.5	–	V	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; $C_{BTS} > 20 \times C_{SSG\_SSS}$; BUCK PREREG in CCM; $I_{bck\_prereg} \geq 1$ A 1)	DS-1500
[SSW] High level Gate output voltage vs. Source (light load)	ΔV_{SSG_SSS}	3.4	4.5	–	V	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; $C_{BTS} > 20 * C_{SSG\_SSS}$; BUCK PREREG in CCM; $I_{bck\_prereg} < 1$ A 1)	DS-2041
Gate rise time	$t_{SSC\_G\_r}$	–	–	320	µs	ΔV_{SSG_SSS} from 0 V to 4 V $V_{VS} > V_{VS}$[MIN] C_{SSG_SSS} = 3 nF From R1SW rising edge 1)	DS-1501
Gate fall time	$t_{SSC\_G\_f}$	–	–	3	µs	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; ΔV_{SSG_SSS} from 4.0V to 0.7V C_{SSG_SSS} = 1nF $V_{VS} > V_{VS}$ [MIN] 1)	DS-2141
Over current detection threshold for SSW	SSW_{OC_TH}	x * 0.63	x	x * 1.73	V	SSW_{OC_TH} is programmable by SPI; x: 0.755 V, 0.944 V, 1.04 V, 1.22 V; Default value: 0.755V; $V_{SSC_D} \geq 5$V, for x: 0.755V $V_{SSC_D} \geq 6.5$V, for x: 0.944V, 1.04V, 1.22V $V_{VS} > V_{VS}$[MIN]	DS-2136
Filter time for over current detection	t_{fil_OC}	-	60	-	ns	$V_{VS} > V_{VS}$[MIN] 1)	DS-1947

（表格续下页……）

表 18　　（续）电气特性：安全开关

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SSW over current detection and reaction time	$t_{SSW\_OC\_SD}$	-	500	-	ns	V_{SSG_SSS} is off V_{VS} > V_{VS}[MIN] 1)	DS-1948

1)　未经过生产测试，由设计指定

7 唤醒功能

7.1 介绍

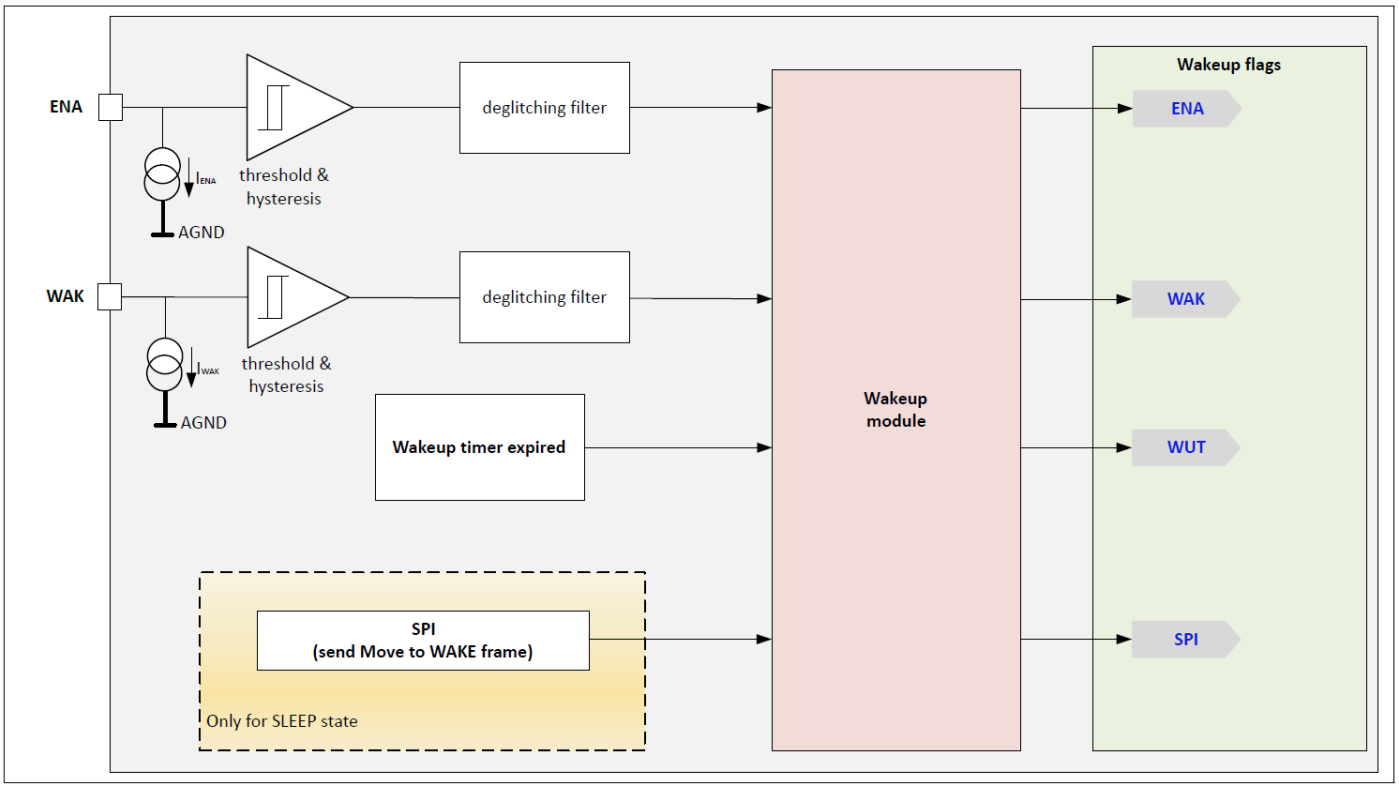

图 13 唤醒功能框图

该模块提供以下唤醒源：

- ENA 引脚（边沿敏感输入）
- WAK 引脚（电平敏感输入）
- 内部唤醒计时器（WUT）
- SPI

为了确定哪个唤醒事件导致器件启动，寄存器 **WAKE_STAT_APP1/2** 存储以下唤醒事件：

- ENA
- WAK
- WUT
- SPI

任何唤醒事件都可能触发状态转移和中断事件，请参见第 9 章 和 中断 [自动编号]。

ENA 唤醒信号通常是来自车辆点火开关的信号。WAK 唤醒信号通常是来自收发器的信号。

7.2 使能（ENA）

7.2.1 功能描述：使能（ENA）

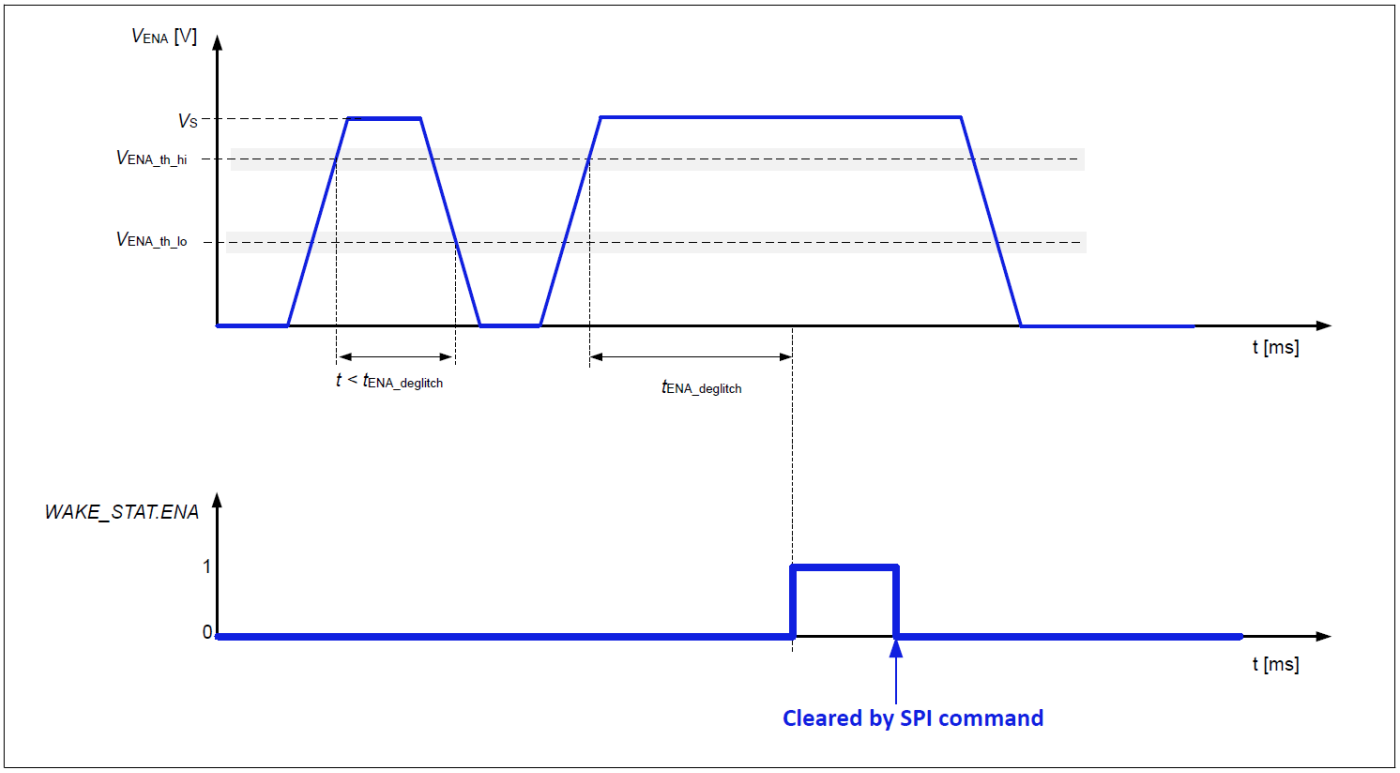

图 14 使能 (ENA) 信号图

ENA 引脚对边沿敏感。

上升沿检测

如果 ENA 引脚上的电压超过阈值$V_{ENA_th_lo}$ 并且超过阈值 $V_{ENA_th_hi}$的时间长于去毛刺滤波器时间 $t_{ENA\_deglitch}$，则器件检测到上升沿。

ENA 位设置

如果 FSM 状态变化是由 ENA 引脚上的上升沿检测引起的，则该器件会设置 **WAKE_STAT_APPx.ENA** 位。可以通过 SPI 清除 **WAKE_STAT_APPx.ENA** 位，而无需考虑 ENA 引脚上的电压电平。

7.2.2 电气特性：使能（ENA）

表 19 电气特性：使能（ENA）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ENA threshold "high" voltage	$V_{ENA\_th\_hi}$	1.3	1.65	2.0	V	V_{ENA} increasing; $V_S \geq 6$ V	DS-1971
ENA threshold "low" voltage	$V_{ENA\_th\_lo}$	1	1.2	1.4	V	V_{ENA} decreasing; $V_S \geq 6$ V	DS-1972

（表格续下页……）

表 19　（续）电气特性：使能（ENA）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ENA deglitch filter time	$t_{ENA\_deglitch}$	20	30	40	µs	V_S ≥ 6 V	DS-1973
ENA pin "high" input current	I_{ENA_hi}	–	–	5	µA	V_{ENA} ≥ 2 V	DS-1974
ENA pin "low" input current	I_{ENA_lo}	–	0.1	2	µA	V_{ENA} ≤ 1 V	DS-1975
ENA threshold hysteresis	V_{ENA_HYST}	200	400	550	mV	V_S ≥ 6 V	DS-1976

7.3　唤醒（WAK）

7.3.1　功能描述：唤醒（WAK）

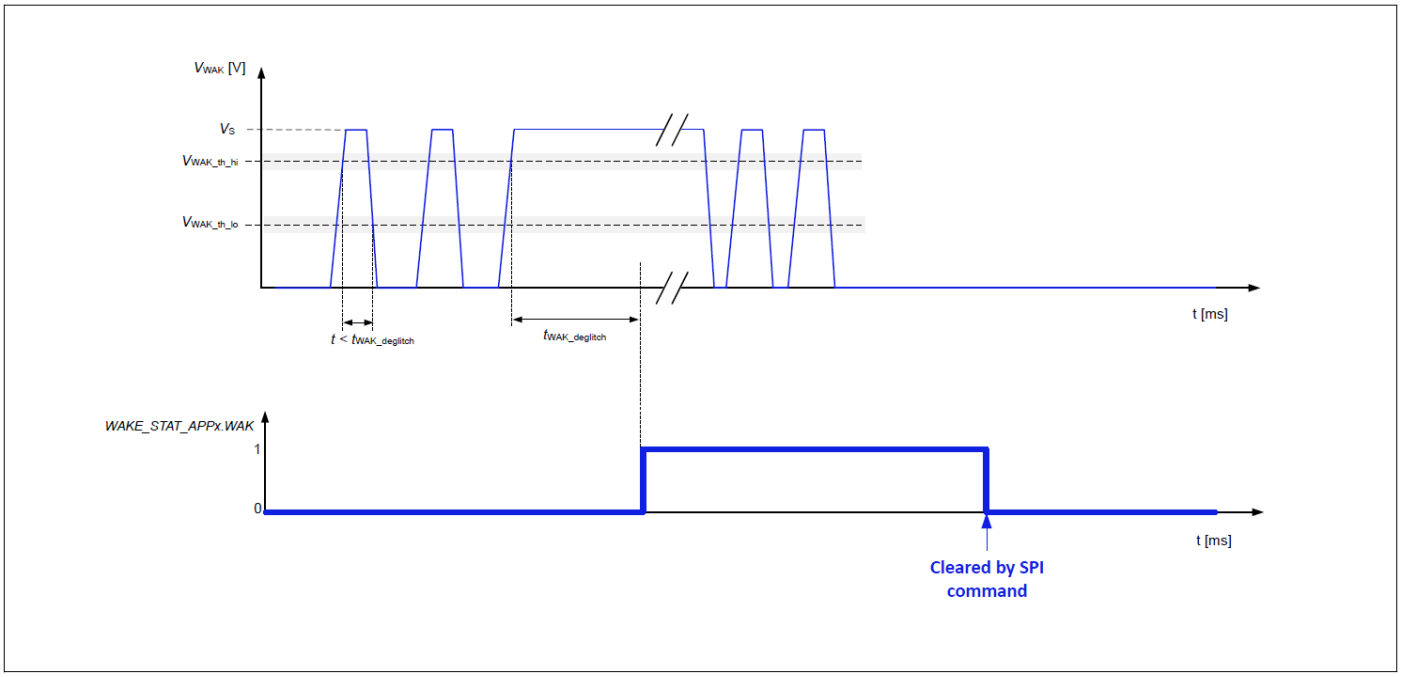

图 15　唤醒（WAK）信号图

WAK 引脚对电平敏感。

电平定义

如果 WAK 引脚上的电压电平低于阈值 $V_{WAK\_th\_lo}$ 的时间超过去毛刺滤波时间 $t_{WAK\_deglitch}$，则检测到有效的“低”信号。

如果 WAK 引脚上的电压电平高于阈值 $V_{WAK\_th\_hi}$ 的时间超过去毛刺滤波时间 $t_{WAK\_deglitch}$，则检测到有效的“高”信号。

WAK 位设置

如果唤醒是由 WAK 引脚上的有效“高”电平检测引起的，则该器件会设置 **WAKE_STAT_APPx.WAK** 位可以通过 SPI 清除 **WAKE_STAT_APPx.WAK** 位。

7.3.2 电气特性：唤醒（WAK）

表20 电气特性：唤醒（WAK）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
WAK threshold "high" voltage	$V_{WAK\_th\_hi}$	1.3	1.65	2.0	V	V_{WAK} increasing; $V_S \geq 6$ V	DS-1977
WAK threshold "low" voltage	$V_{WAK\_th\_lo}$	1.0	1.2	1.4	V	V_{WAK} decreasing; $V_S \geq 6$ V	DS-1978
WAK deglitch filter time	$t_{WAK\_deglitch}$	20	30	40	µs	$V_S \geq 6$ V	DS-1979
WAK pin "high" input current	I_{WAK_hi}	–	–	5	µA	$V_{WAK} \geq 2$ V	DS-1980
WAK pin "low" input current	I_{WAK_lo}	–	0.1	2	µA	$V_{WAK} \leq 1$ V	DS-1981
WAK threshold hysteresis	V_{WAK_HYST}	200	400	550	mV	$V_S \geq 6$ V	DS-1982

7.4 唤醒计时器（WUT）

7.4.1 功能描述：唤醒计时器（WUT）

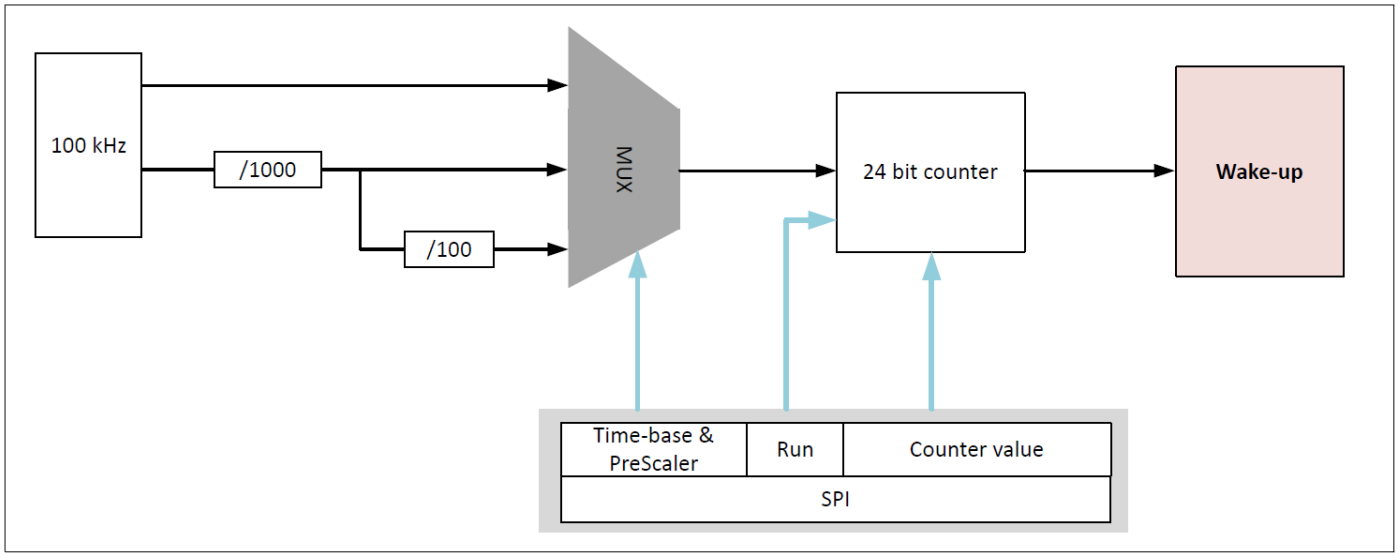

图 16 唤醒计时器功能框图

唤醒计时器配置

唤醒计时器可以通过 SPI 在 24 位宽唤醒计时器中进行配置
WUT_CFG0 和 **WUT_CFG1** 以及时基可以通过 **DEV_CFG4** 寄存器进行配置。

唤醒计时器是一个 24 位计数器，其时钟频率可选择为 100 kHz、1 kHz、100 Hz 或 1 Hz（时基）。

表 21　　唤醒计时器配置

Timebase		Clock	Timer resolution	Timer range (timebase resolution × timer value)
WUT_CYC	WUT_PRESC			
0	0	100 kHz	10 µs	10 µs to 168 s
0	1	1 kHz	1 ms	1 ms to 4.6 h
1	0	100Hz	10 ms	10 ms to 1.9 days

该器件允许通过 **DEV_CFG4.WUT_EN** 启用和禁用唤醒计时器。

唤醒计时器启动和停止

当 DEV_CFG4.WUT_EN=1 且进入 STANDBY 状态或 SLEEP 状态时，计数器会加载唤醒计时器寄存器的值并开始递减。

器件在下列任一条件下停止计时器：

- 唤醒计时器过期
- 器件退出 SLEEP 状态或 STANDBY 状态。剩余的计时器数值可以通过 SPI 读回，以评估剩余的理论时间和相应的已用时间（**WUT_STAT0.TIMVALL**、**WUT_STAT1.TIMVALH**、**WUT_STAT1.PRESC**、**WUT_STAT1.CYC**）

唤醒计时器位

如果唤醒计时器过期，器件将设置唤醒计时器位 **WAKE_STAT_APPx.WUT = 1**。
WUT 位可以通过 SPI 清零。

7.4.2　　电气特性：唤醒计时器

表 22　　电气特性：唤醒计时器

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Wake-up timer accuracy	d_{acc_WUT}	-10	–	10	%	–	DS-2059

7.5　　通过 SPI 帧唤醒

仅当器件处于 SLEEP 状态且 BUCKCORE 和 QUC 已启用时，才能通过 SPI 进行唤醒。只有这样，器件才能通过相应写入 **DEV_PW_CFG3.FSM_STATEREQ = WAKE** 发送状态转移请求至 WAKE 状态来唤醒。写入状态转移请求中不涉及的任何其他寄存器不会导致器件被唤醒。

8 硬件配置（HWCFG）

表 23 电气特性：硬件配置电阻

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External resistor accuracy	R_{HWCFG_acc}	-5	-	+5	%	1)	DS-2017

1） 未经过生产测试，由设计指定

8.1 功能描述

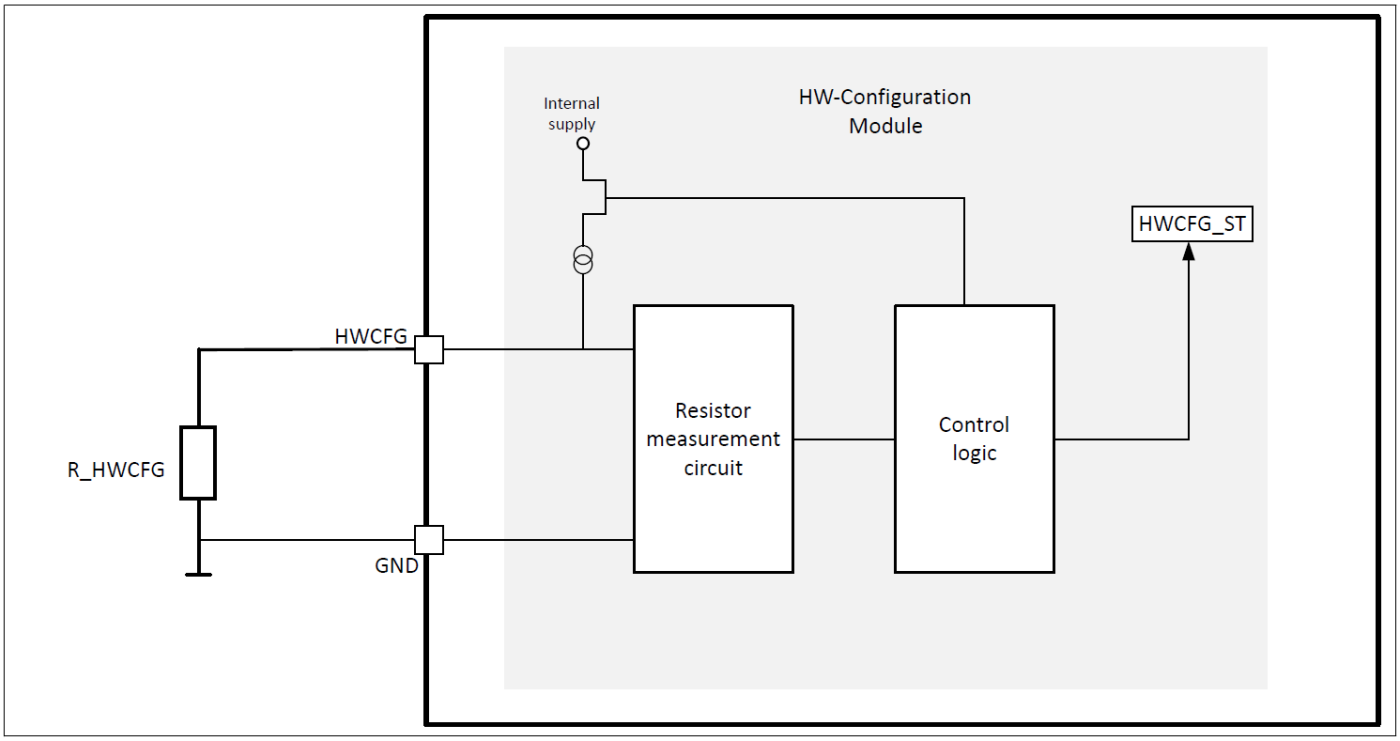

图 17 硬件配置框图

器件提供硬件配置模块。连接在引脚 (HWCFG) 上的外部电阻 (R_HWCFG) 用于：

- 定义内部调节器的启动时序
- 定义预调节器输出电压
- 定义复位延迟时间的默认值
- 激活 MPS 模式

（根据下表。）

表 24 硬件配置（HWCFG）

HWCFG resistor setting kΩ, 5% tolerance	RESOUT start-up delay	Pre-regulator output voltage (VPRE)	Start-up sequence of the regulator	MPS mode activation	SPI bits readout DEV_CFG1.HWCFG_STAT
	2 ms/10 ms (TBD)	4V/5V5	Schema (A)/ Schema (B)	ON/OFF	
< 1.0 or GND	10 ms	4V	A	OFF	0000
2.2	2 ms	4V	A	OFF	0001
3.3	2 ms	4V	B	OFF	0010
4.7	10 ms	4V	B	OFF	0011
6.8	2 ms	5V5	A	OFF	0100
10	10 ms	5V5	A	OFF	0101
15	2 ms	5V5	B	OFF	0110
22	2 ms	5V5	B	ON	1001
33	2 ms	5V5	A	ON	1010
47	10 ms	4V	B	ON	1011
68	2 ms	4V	B	ON	1100
100	2 ms	4V	A	ON	1101
150	10 ms	4V	A	ON	1110
> 200 or open	10 ms	4V	A	OFF	1111

启动器件后，微控制器可以通过读取 SPI 状态寄存器 **DEV_CFG1.HWCFG_STAT** 来验证所选设置，其中存储了 HWCFG 电阻值

9 状态机（FSM）

9.1 功能描述：状态机（FSM）

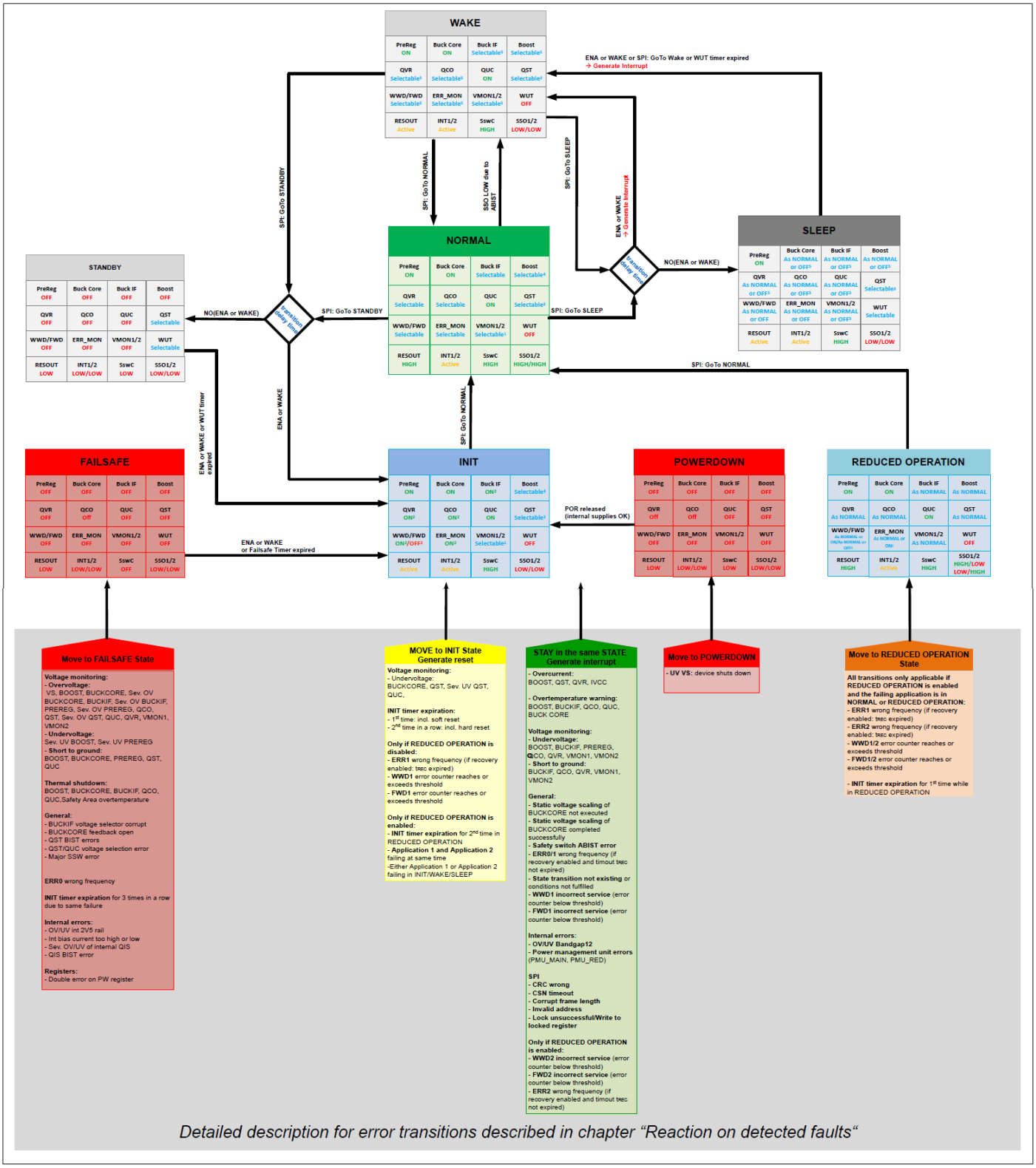

图 18　　状态机流程图

(1)：可通过 VMxEN 在启动时选择功能；可通过 SPI 关闭。进入 INIT 时重新启动

(2)：进入 INIT 或 REDUCED OPERATION 状态时 ON 或 OFF，然后可通过 SPI 配置。

(3)：当 QST_MODE 配置为 USER_MODE 时，QST 电源的 ON 或 OFF 状态可通过 SPI 进行配置；否则，当 QST_MODE 配置为 PMIC_MODE（默认值）时，QST 与 QST_EN 无关，始终为 ON

(4)：仅当 VPREREG=5V5 标称值时，才可选择启动自动检测。否则为 ON

(5)：WD：可配置为在 SLEEP 状态下保持激活状态；所有其他模块必须在包含 SLEEP 指令的同一 SPI 帧内禁用；唤醒后，模块将恢复到 SLEEP 前的状态

9.1.1 状态描述

器件提供以下状态：

- INITIALIZATION 状态：
  - INIT
  - WAKE
- OPERATIONAL 状态：
  - NORMAL
- LOW QUIESCENT 状态：
  - SLEEP
  - STANDBY
- ERROR 状态
  - FAILSAFE
  - REDUCED OPERATION

9.1.1.1 POWERDOWN 状态

POWERDOWN 状态表示器件未上电的条件。VS 引脚处的电压不可用。

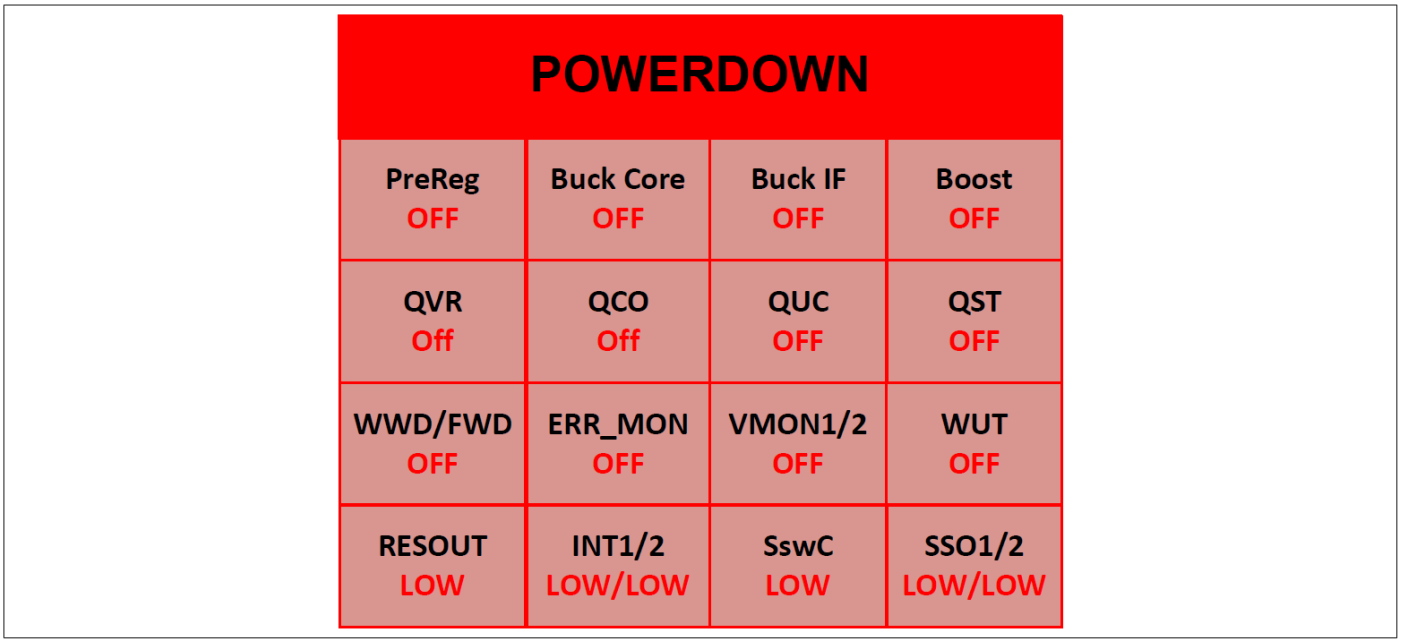

图 19 POWERDOWN 状态

表 25 POWERDOWN 状态

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off
QUC	OFF	Microcontroller supply is off
QST	OFF	Standby supply is off
WWD/FWD	OFF	Watchdog is off
ERR_MON	OFF	Error monitoring function ERR MON is off
VMON1/2	OFF	External voltage monitoring VMON1/2 is off
WUT	OFF	Wake up timer (WUT) is off
RESOUT	LOW	RESOUT output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

9.1.1.2 INIT 状态

在 INIT 状态下，设备启动其内部电源，以及配置好的外部电压轨。在每次进入时，RESOUT 将被拉低至 tRD_2ms/tRD_10ms 或其配置值，并在电源启动序列执行后释放。如果进入时电压轨仍处于标称电压，则在电源启动序列中将被跳过。正在执行内部检查，设备等待初始化成功。由微控制器在 INIT 计时器 t_{INIT} 超时之前执行。

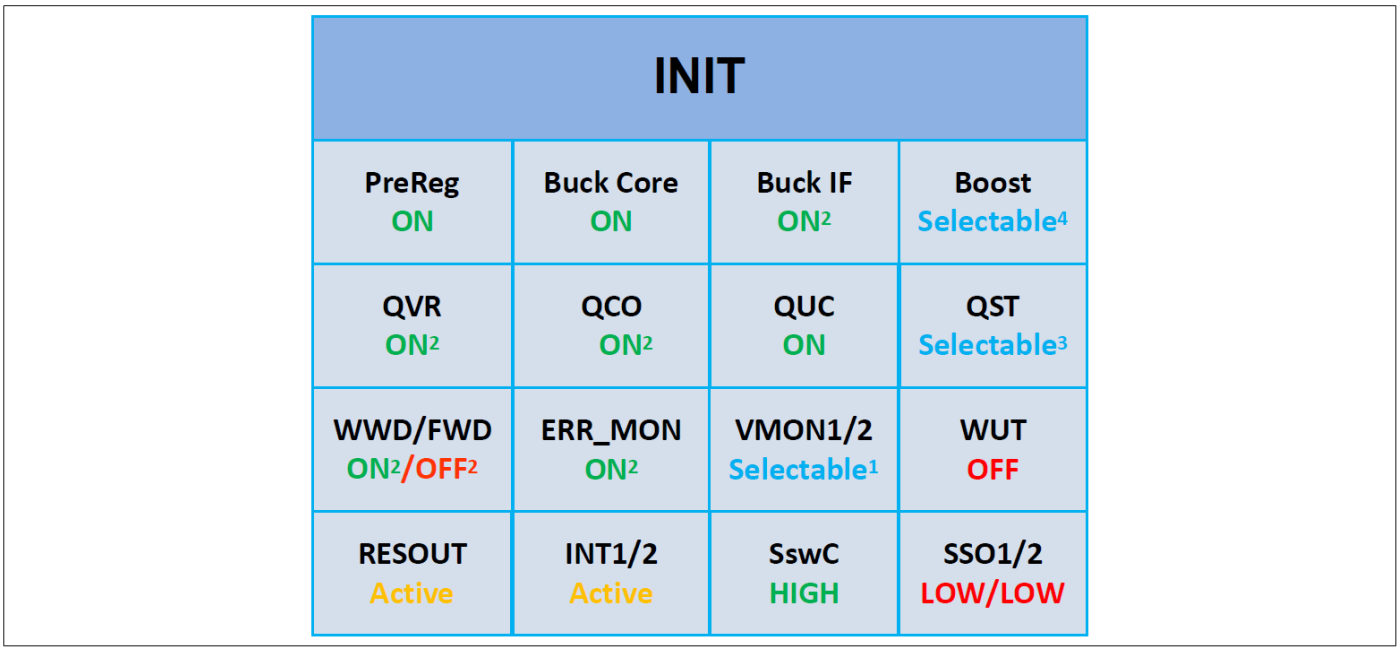

图 20　　INIT 状态

表 26　　INIT 状态

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	ON	Buck regulator for interface supply is on, if automated use-detection identified the usage; then configurable via SPI
Boost	Selectable	Boost regulator is selectable with start-up autodetect only if V_{OUT_PreReg} = 5V5 nominal otherwise, it is on.
QVR	ON	Voltage reference is on; then configurable via SPI
QCO	ON	Communication supply is on; then configurable via SPI
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD	ON	Window watchdog is on; then configurable via SPI
FWD	OFF	Functional Watchdog is off; then configurable via SPI
ERR_MON	ON	Error monitoring function ERR MON is on; then configurable via SPI
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	Active	RESOUT output released ("high") after power-up sequence has finished and reset delay time has expired

（表格续下页……）

表 26 （续）INIT 状态

Part/Function	Value	Description
INT1/2	Active	Interrupt outputs are active (INT2 only active if "REDUCED OPERATION" is enabled)
SswC	High	External safety switch is on
SSO1/2	LOW	Safe state outputs are low

注释：

以下情况下，未执行“移至NORMAL SPI ”指令：

- *由于执行自动检测，在移至INIT后900 µs 内不会执行*
- *在所有启用的电压轨都处于调节范围（高于UV 阈值）之前不会执行。注释：所有调节器在进入 INIT 时再次打开（如果之前禁用）*

通常情况下，由于RESOUT 在低电平下，应用不会受到此限制的影响，但以下情况除外：

- *tRD 值较低（<1ms）*
- *如果MPS 开启（对于WD/ERR 监测故障，RESOUT 保持高电平，因此应用可能会受到此类限制）。*

9.1.1.3 NORMAL 状态

器件具有 NORMAL 状态，并且只有安全状态输出（SSO1/2）为高电平的状态。

注释： *在此状态下，器件为应用中的微控制器和外设模块供电。*

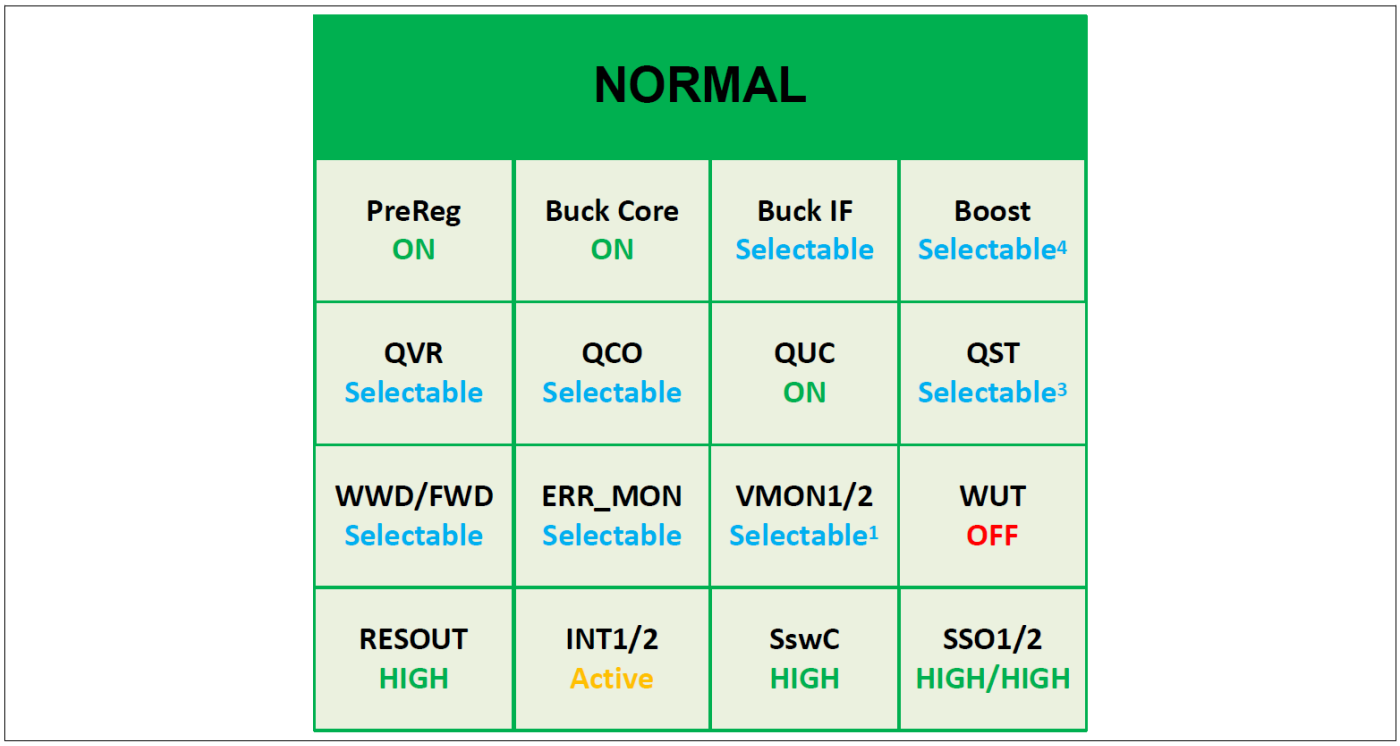

图 21 NORMAL 状态

表 27 NORMAL 状态

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	Selectable	Buck regulator for interface supply can be switched on or off, if it has been detected via automated use detection during start-up
Boost	Selectable	Boost regulator is selectable with start-up autodetect only if V_{R1FB} = 5V5 nominal. Otherwise it is on
QVR	Selectable	Voltage reference can be selected by SPI to be on or off
QCO	Selectable	Communication supply can be selected by SPI to be on or off
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	Selectable	Watchdog can be selected by SPI to be on or off
ERR_MON	Selectable	Error monitoring function ERR MON can be selected by SPI to be on or off
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	High	RESOUT output is high
INT1/2	Active	Interrupt outputs are active (INT2 only active if "REDUCED OPERATION" is enabled)
SswC	High	External safety switch is on
SSO1/2	High/High	Safe state outputs are high

9.1.1.4 WAKE 状态

当器件从 SLEEP 进入 WAKE 状态时，模块会恢复到进入 SLEEP 状态之前的状态。如果在 SLEEP 状态下 RESOUT 为低电平，则在 WAKE 状态下，器件会在 INIT 计时器 tINIT 过期之前等待微控制器成功初始化。

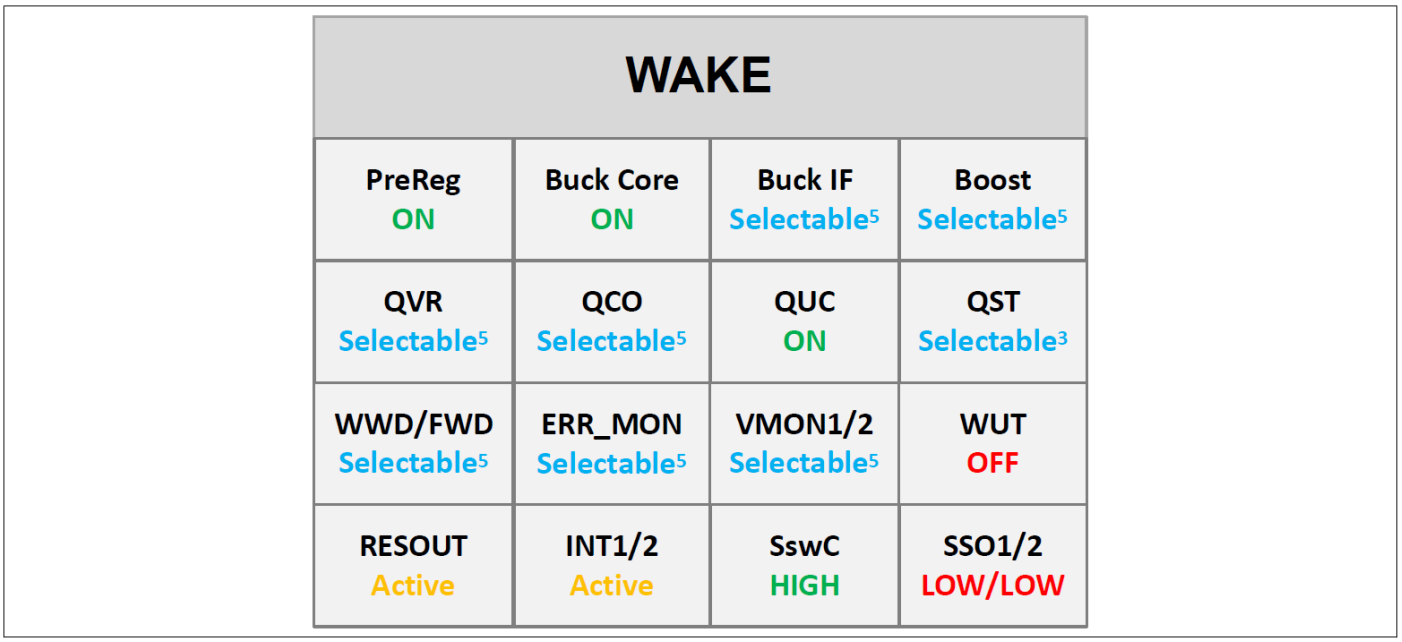

图 22 WAKE 状态

表 28 WAKE 状态

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	Selectable	Buck regulator for interface supply is configurable, if it has been detected via automated use detection during start-up
Boost	Selectable	Boost regulator is configurable with start-up autodetect only if VR1FB =5V5 nominal otherwise, it is on
QVR	Selectable	Voltage reference is configurable via SPI
QCO	Selectable	Communication supply is configurable via SPI
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	Selectable	Watchdog is configurable via SPI
ERR_MON	Selectable	Error monitoring function ERR MON is configurable via SPI
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	Active	RESOUT output is active
INT1/2	Active	Interrupt outputs are active
SswC	HIGH	External safety switch is on
SSO1/2	LOW	Safe state outputs are low

9.1.1.5 REDUCED OPERATION 状态

当器件本身处于 NORMAL 状态或 REDUCED OPERATION 状态时，器件提供 REDUCED OPERATION 状态，仅允许在应用的子部分上发生严重的安全反应。此外，MCU 必须在 INIT 计时器过期前初始化成功。如果 REDUCED OPERATION 是启用的 (REDOP_RS_CFG1.EN = 1)，则器件会显示对特定事件的差异化反应。特别是引入了附加的应用复位功能。与正常复位相比，该应用复位的不同之处在于其可配置脉冲宽度，并且相应地在输出 INT1/2 处发出（**REDOP_RS_CFG2.REDOP_RESOUT_APP1_DUR**、**REDOP_RS_CFG2.REDOP_RESOUT_APP2_DUR**）。通过启用此状态，ERR2 和 WD2 也会自动启用。在 ERR1 或 WD1 检测到的事件会通过 INT1 以应用复位的形式报告，在 ERR2 和 WD2 检测到的事件会通过 INT2 以应用复位的形式报告。此外，如果 ERR2 或 WD2 报告错误，则会在 INT1 发出正常中断；反之，如果 ERR1 或 WD1 报告错误，则会在 INT2 发出正常中断。但是，可以通过 **REDOP_RS_CFG1.INT1_DIS** 和 **REDOP_RS_CFG1.INT2_DIS** 中的配置禁用此跨应用通知。有关 REDUCED OPERATION 中的初始化、故障反应、中断生成和应用错误的更多信息，请参阅以下章节：

- INIT 计时器功能
- 故障反应
- 中断功能（INT）
- 应用复位（EDUCED OPERATION ENABLE）

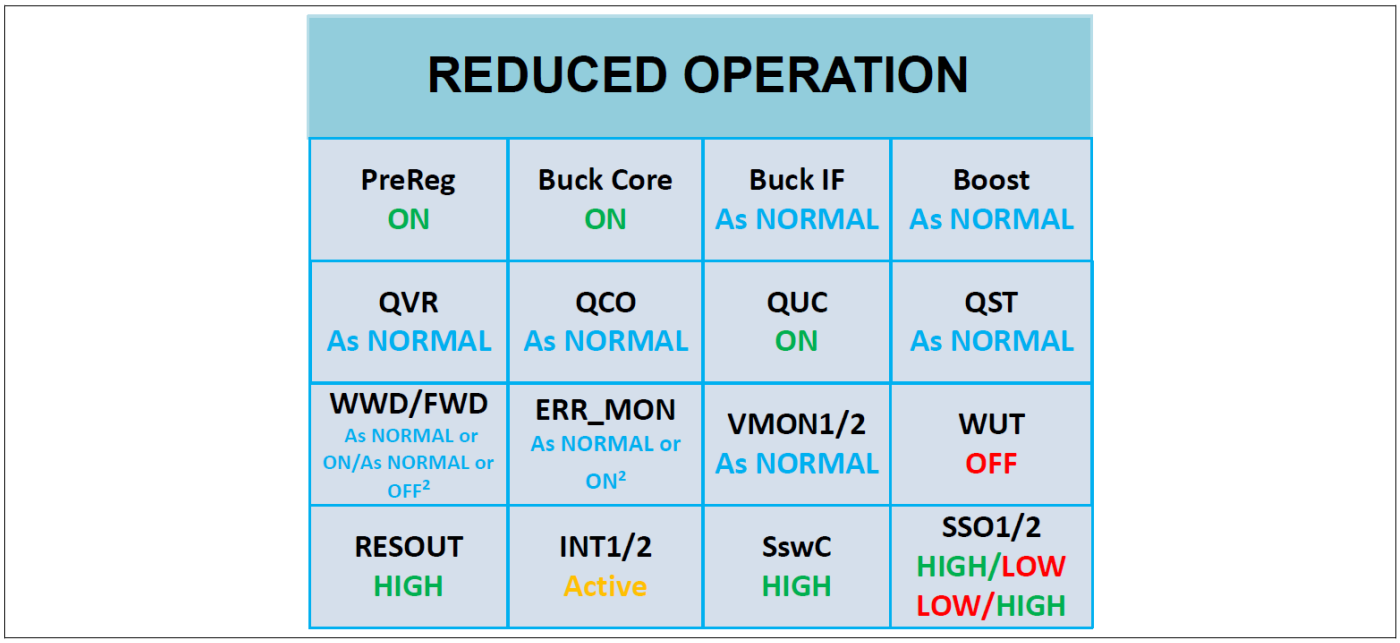

图 23 REDUCED OPERATION 状态

表 29 REDUCED OPERATION 状态

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	As NORMAL	Buck regulator for interface supply has same configuration as in NORMAL state
Boost	As NORMAL	Boost regulator has the same configuration as in NORMAL
QVR	As NORMAL	Voltage reference has same configuration as in NORMAL state
QCO	As NORMAL	Communication supply has same configuration as in NORMAL state

（表格续下页……）

表 29 （续）REDUCED OPERATION 状态

Part/Function	Value	Description
QUC	ON	Microcontroller supply is on
QST	As NORMAL	Standby supply has same configuration as in NORMAL state
WWD	Failing application: ON Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and remains ON. Waits for trigger and/or configuration via SPI. Non failing application: Keeps configuration as for NORMAL state and needs to be serviced as in NORMAL state.
FWD	Failing application: OFF Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and OFF. Non failing application: Keeps configuration and stays ON as in NORMAL. Trigger must be done accordingly.
ERR_MON	Failing application: ON Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and remains ON. Waits for correct ERR pin signal and/or configuration via SPI. Non failing application: Keeps configuration as for NORMAL state and needs to be serviced as in NORMAL state.
VMON1/2	As NORMAL	External voltage monitoring VMON1/2 have same configuration as in NORMAL state
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	High	RESOUT output is high
INT1/2	Active	Interrupt outputs are active
SswC	High	External safety switch is on
SSO1/2	High/Low or Low/High	Safe state outputs are low or high depending on the failing cluster/ application

注释： *在 REDUCED OPERATION 状态下，集成商必须确保，除了触发看门狗并重新配置应用特定的监测 ERR1/2 或 WD1/2 之外，不得对器件进行任何其他配置，例如禁用或启用电压轨。否则，可能会干扰器件的内部监测，并导致在 REDUCED OPERATION 状态下出现有误的错误报告。此外，还需指出，当释放相关的 INTx 时，相应的 WWDx 和 ERRx 功能将被重新启用，而 FWD 功能将被禁用。*

9.1.1.6 FAILSAFE 状态

在 FAILSAFE 状态下，所有产生的电压轨均被关闭。

进入 FAILSAFE 状态时，故障安全计时器启动。

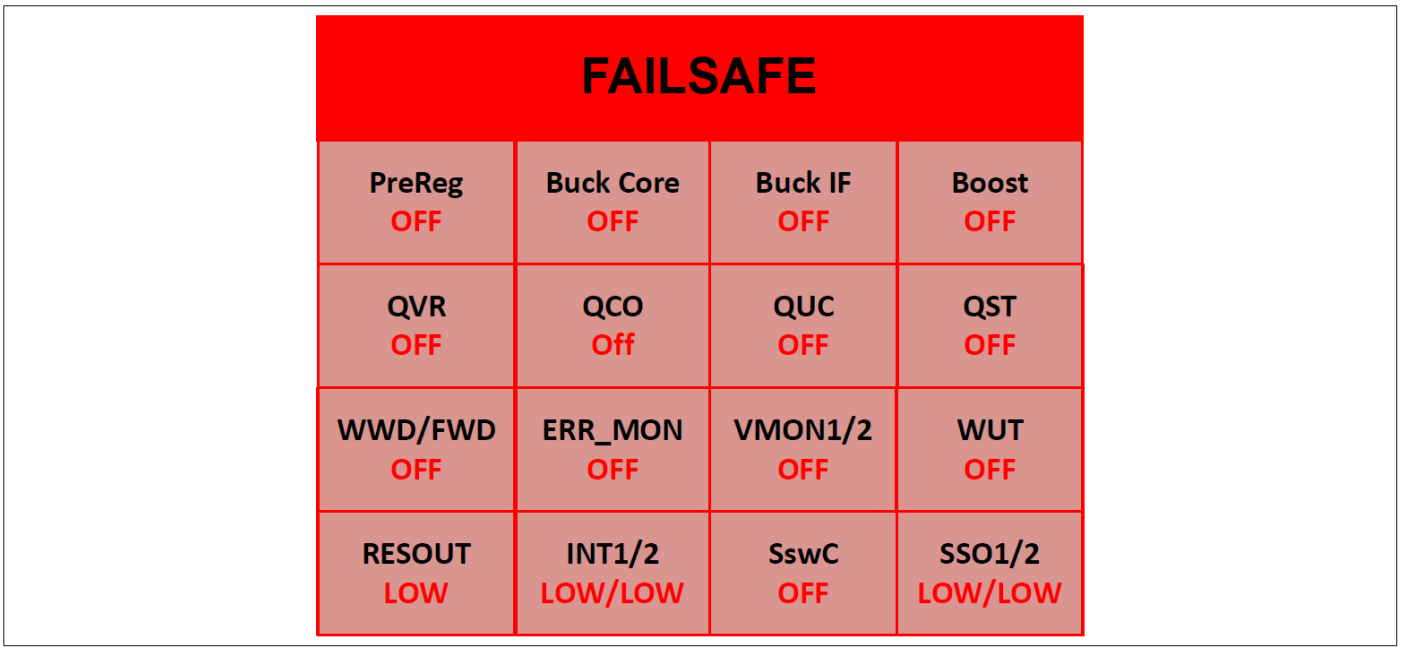

图 24　　FAILSAFE 状态

表 30　　FAILSAFE 状态

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off
QUC	OFF	Microcontroller supply is off
QST	OFF	Standby supply is off
WWD/FWD	OFF	Watchdog is off
ERR_MON	OFF	Error monitoring function ERR MON block is off
VMON1/2	OFF	External voltage monitoring VMON1/2 are off
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	LOW	RESOUT output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

9.1.1.7　　SLEEP 状态

为了最大限度减少应用中的操作限制，可以将器件置于 SLEEP 状态，从而实现仅操作器件的选定模块的配置。与 NORMAL 状态相比，这使得应用能够在功能集减少的同时消耗更少的热量。

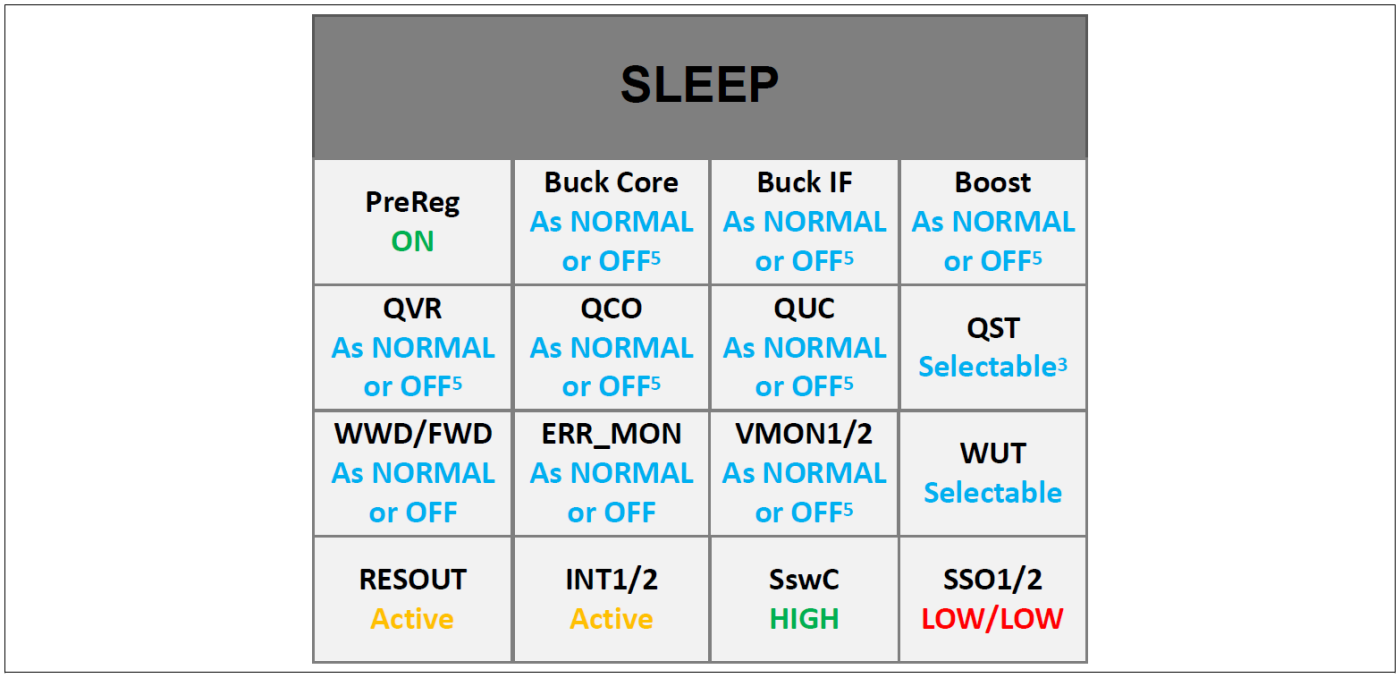

图 25　　SLEEP 状态

表 31　　SLEEP 状态

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	As NORMAL or OFF	Buck core regulator has same configuration as in NORMAL state or is off if configured
Buck IF	As NORMAL or OFF	Buck regulator for interface supply has same configuration as in NORMAL state or is off if configured
Boost	As NORMAL or OFF	Boost regulator has same configuration as in NORMAL state or is off if configured
QVR	As NORMAL or OFF	Voltage reference has same configuration as in NORMAL state or is off if configured
QCO	As NORMAL or OFF	Communication supply has same configuration as in NORMAL state or is off if configured
QUC	As NORMAL or OFF	Microcontroller supply has same configuration as in NORMAL state or is off if configured
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	As NORMAL or OFF	Watchdog has same configuration as in NORMAL state or is off if configured
ERR_MON	As NORMAL or OFF	Error monitoring function ERR MON has same configuration as in NORMAL state or is off if configured
VMON1/2	As NORMAL or OFF	External voltage monitoring VMON1/2 have same configuration as in NORMAL state or they are off if configured

（表格续下页……）

表31 （续）SLEEP 状态

Part/Function	Value	Description
WUT	Selectable	Wake-up timer (WUT) is selectable to be on or off
RESOUT	Active	RESOUT output is active (LOW if either BUCKCORE or QUC are OFF)
INT1/2	Active	Interrupt outputs are active (LOW if QUC is OFF)
SswC	HIGH	External safety switch is on
SSO1/2	LOW	SSO1 and SSO2 are low

注释：在SLEEP 状态下，集成商必须确保除维护看门狗之外，不对器件进行任何其他配置，例如禁用或启用电压轨，或更改WD1/2 或ERR1/2 的配置。这可能会干扰器件的内部监测，并导致在SLEEP 状态下出现有误的错误报告。

9.1.1.8 STANDBY 状态

STANDBY 状态代表器件的低电流模式。

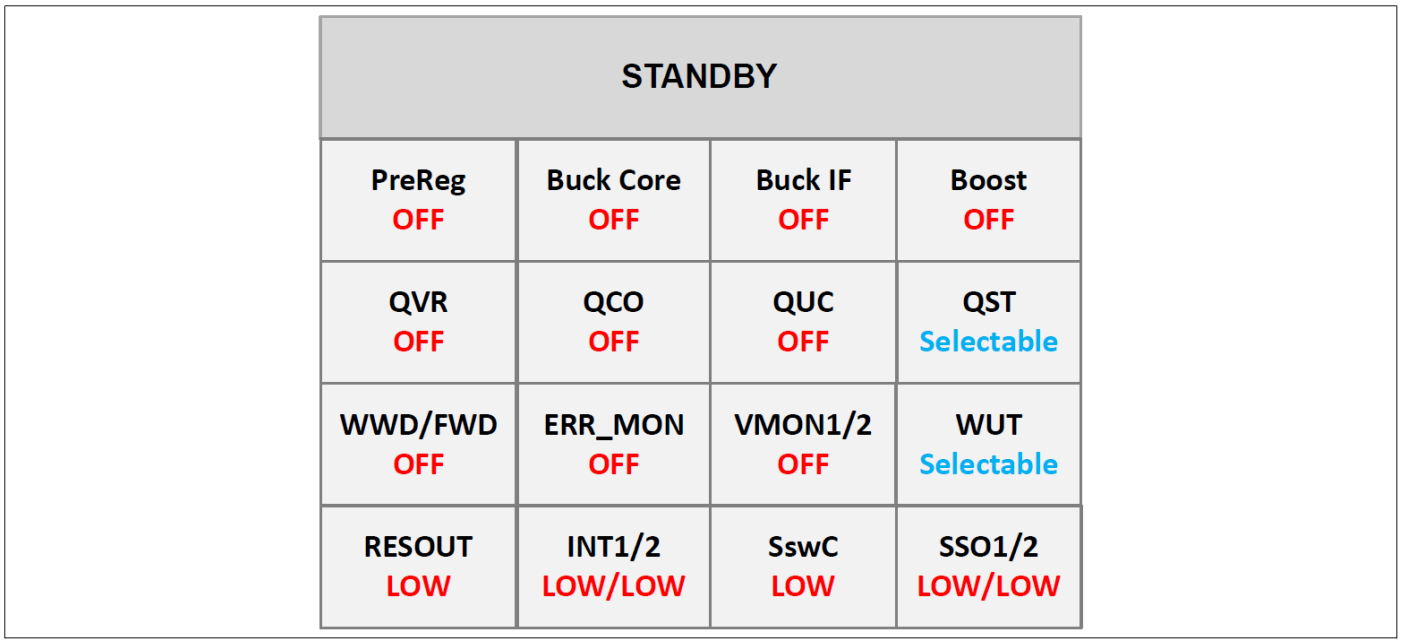

图 26 STANDBY 状态

表 32 STANDBY 状态

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off

（表格续下页……）

表 32 （续） STANDBY 状态

Part/Function	Value	Description
QUC	OFF	Microcontroller supply is off
QST	Selectable	Standby supply is on or off, can be configurable by SPI
WWD/FWD	OFF	Watchdog interface is off
ERR_MON	OFF	Error monitoring block is off
VMON1/2	OFF	Monitoring blocks are off
WUT	Selectable	Wake block is selected to be on or off
RESOUT	LOW	Control reset output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

注释： *只有当WUT 和QST 都关闭时才能达到最低静态电流。这允许器件关断所有不需要的内部电压轨。*

9.1.2 INIT 计时器功能

INIT 计时器为微控制器提供了一个较长的启动时间窗口，使其能够正确启动并与 PMIC 同步。复位输出释放后，基本监控功能会在 t_{INIT} 过期之前建立或禁用。以下段落将详细介绍 INIT 计时器的一般工作原理。

启动 INIT 计时器

- 如果器件处于 REDUCED OPERATION 状态，则 INIT 计时器在相应 INT1/2 引脚的应用复位脉冲上升沿启动。
- 如果器件处于 INIT 或 WAKE 状态，INIT 计时器将从 RESOUT 引脚的上升沿开始。

STOP INIT 计时器

如果满足以下所有条件，器件将停止 INIT 计时器并复位其过期计数器：

- WD1/2 是否已通过 SPI 正确触发或禁用，请参阅看门狗功能。
- ERRMON0/1/2 信号已正确施加或已通过 SPI 禁用，请参阅错误监测

INIT TIMER FAULT

如果 INIT 计时器在过期前未能成功停止，则器件会检测到 INIT_TIMER_FAULT。

注释： *WD2 和ERR2 仅在REDUCED OPERATION 为启用的情况下才需要初始化(**REDOP_RS_CFG1.EN = 1**)。*

如果 INIT 计时器在 INIT 状态下过期**一次**，则器件：

- 生成 INIT_TIMER_FAULT，
- 激活软复位
- 存储故障
- 复位寄存器属于复位级别 R3
- 移至 INIT 状态，请参阅状态机

如果 INIT 计时器在 INIT 状态下过期**两次**，则器件

- 生成一个 INIT_TIMER_FAULT
- 激活硬复位
- 存储故障

- 复位寄存器属于复位级别 R3
- 执行配置的下电序列
- 重新启动配置的电源序列
- 移至 INIT 状态，请参阅状态机

如果 INIT 计时器在 INIT 状态过期**第三次**，则器件

- 存储故障
- 复位寄存器属于复位级别 R2
- 移至故障安全状态，请参阅状态机

如果 INIT 计时器在有限操作状态下过期**一次**，则器件：

- 生成一个 INIT_TIMER_FAULT
- 激活与失败的应用对应的新应用复位
- 置位 **INIT_ERR_APPx.REDOP_RES1**

如果INIT 计时器在 REDUCED OPERATION 状态下过期**两次**，则器件

- 生成 INIT_TIMER_FAULT，
- 激活软复位
- 设置故障位**INIT_ERR_APPx.REDOP_RES2**
- 移至 INIT 状态，请参阅状态机

如果 INIT 计时器在 WAKE 状态下过期**一次**，则器件

- 生成 INIT_TIMER_FAULT，
- 激活软复位
- 存储故障
- 复位寄存器属于复位级别 R3
- 移至 INIT 状态，请参阅状态机

注释： *WAKE 中的第一次过期已经视作在 INIT 状态下发生的第一次过期。*

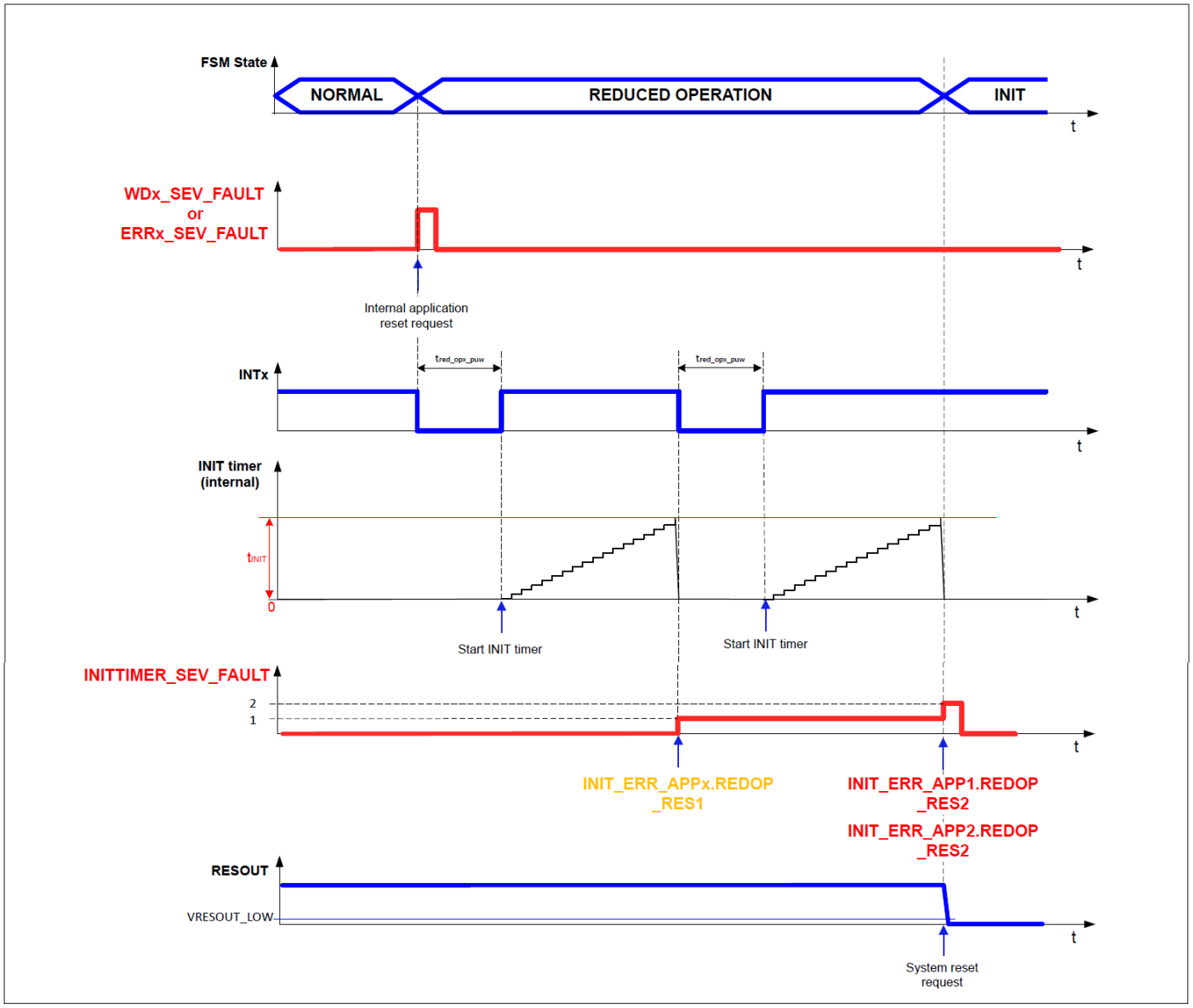

图 27　　REDUCED OPERATION 状态下系统复位激活信号图

x = 1, 2

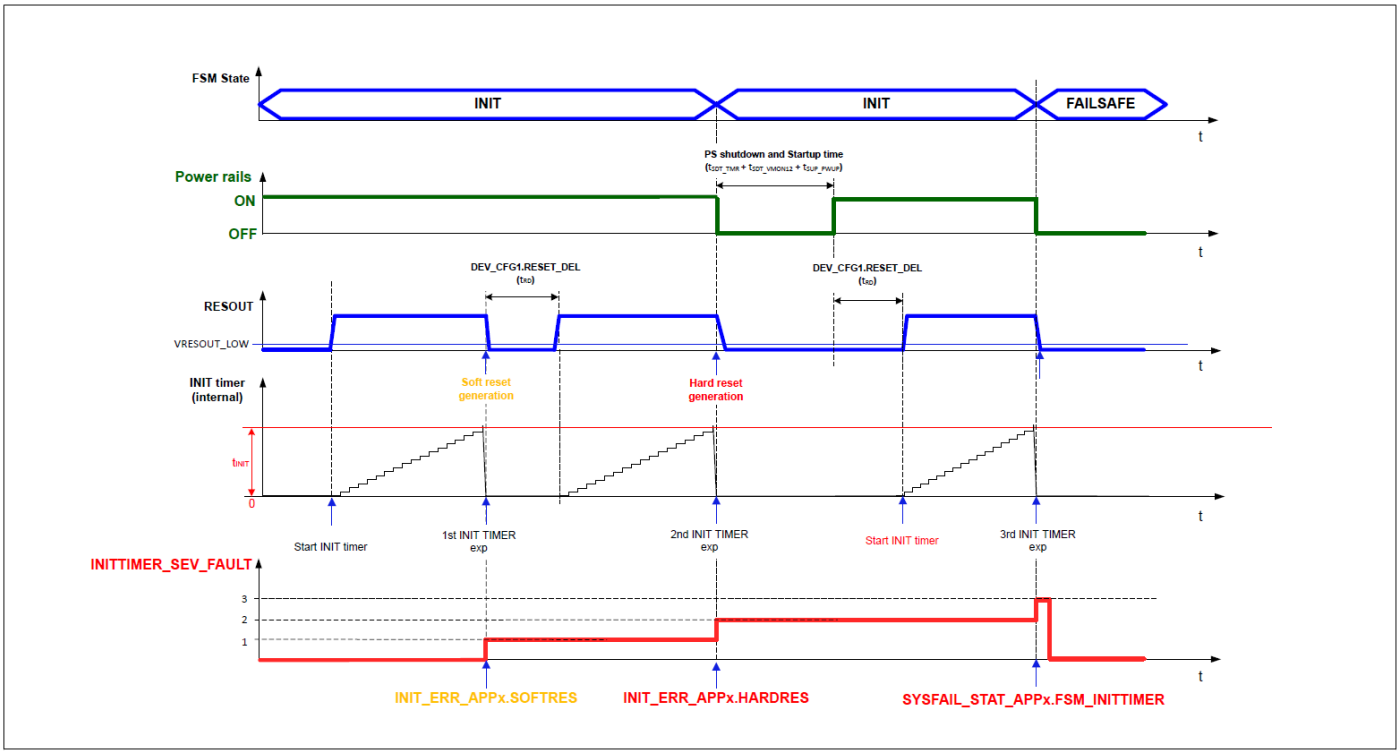

图 28　　由于 INIT 状态下 3xINIT 计时器过期而导致系统关闭的信号图

x = 1, 2

9.1.3　状态转移

通过写入位字段 **DEV_PW_CFG3.FSM_STATEREQ** 请求状态转移。所做的更改将在 SPI 通信成功完成并重新锁定受保护的写入寄存器后生效。这发生在用锁定密钥写入 **PROT_CFG.KEY** 后释放 CSN 时。如果请求的状态转移源自 NORMAL 状态，则在写入锁定密钥后释放 CSN 也标志着输出 SSOx 被拉低的时刻。SSO1 和 SSO2 之间可能配置的延迟时间仍然有效。

如果在器件执行上电或下电序列时收到状态请求，则状态转移被拒绝，并且位 **SYS_STAT_APP1.FSM_NOOP** 为置位，同时发出中断（如果 REDUCED OPERATION 启用，则 **SYS_STAT_APP2.FSM_NOOP** 也为置位）。如果请求的状态转移未在状态转移表中列出（无效的状态转移请求），也会发生相同的反应。如果在已经处于进入 SLEEP 或 STANDBY 状态的转换延迟中时请求有效的状态转移，则当前延迟将被中止并且发生转换，就好像检测到 ENA 或 WAK 信号一样。允许从一种状态转换到自身状态。

如果 WAK、ENA 在延迟时间过期后发生，则已开始的下电序列将结束，然后立即发生唤醒。

(x = 1,2)

9.1.3.1　状态转移表

Old State	New state	Conditions	Comments
POWERDOWN	INIT	Internal POR (internal supplies OK)	The configured power sequencing is applied, see Hardware configuration (HWCFG)

INIT	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–
NORMAL	SLEEP	(SPI command: Move to SLEEP) AND (No ENA) AND (No WAK)	- If a move to SLEEP is unsuccessful an interrupt is issued and the device moves into WAKE - The configured power sequencing is applied, see Hardware configuration (HWCFG)
NORMAL	STANDBY	(SPI command: Move to STANDBY) AND (No ENA) AND (No WAK)	- If a move to STANDBY is unsuccessful an interrupt is issued and the device moves into INIT - The configured power sequencing is applied, see Hardware configuration (HWCFG)
SLEEP	WAKE	ENA OR WAK OR WUT timer expired OR (SPI command: Move to WAKE)	- Upon wake-up from SLEEP an interrupt is issued, if QUC was on in SLEEP - The wake-up information is stored - Restores regulator configuration as it has been before entering SLEEP, following the power-up sequence and skipping the respective regulators, see Hardware configuration (HWCFG)
WAKE	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–

WAKE	SLEEP	(SPI command: Move to SLEEP) AND (No ENA) AND (No WAK)	- If a move to SLEEP is unsuccessful an interrupt is issued and the device moves into WAKE - The configured power sequencing is applied, see Hardware configuration (HWCFG)
WAKE	STANDBY	(SPI command: Move to STANDBY) AND (No ENA) AND (No WAK)	- If a move to STANDBY is unsuccessful an interrupt is issued and the device moves into INIT - The configured power sequencing is applied, see Hardware configuration (HWCFG)
STANDBY	INIT	ENA OR WAK OR WUT timer expired	The configured power sequencing is applied
FAILSAFE	INIT	ENA OR WAK OR Failsafe Timer expired	- The automated wake-up from FAILSAFE upon expiration of the failsafe timer only works if FAILSAFE has not been entered three times consecutively caused by the same failure - The configured power sequencing is applied
REDUCED OPERATION	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–

注释： *当请求状态转移到SLEEP 或STANDBY 时，必须在发送状态转移请求之前完成目标状态的所有配置。*

9.1.3.2 可编程转移延迟时间

从 NORMAL 到 SLEEP 、从 NORMAL 到 STANDBY、从 WAKE 到 SLEEP 以及从 WAKE 到 STANDBY 的转换，都存在可配置的转换延迟时间。一旦微控制器请求进行上述状态转换，转换将在转换延迟时间 t_{TR_DEL} 过期后进行。

如果在转换延迟时间内收到状态请求，则该转换不会成功，并分别移至 INIT 或 WAKE 状态。

配置在 **DEV_CFG4.FSM_TRDEL** 中完成。

9.1.3.3 从 FAILSAFE 自动唤醒

进入 FAILSAFE 后，器件将保持该模式$t_{FAILSAFE_min}$*。之后，器件会尝试执行一次自动重启，除非因同一错误源连续 3 次进入 FAILSAFE；如果出现这种情况，器件将保持 FAILSAFE 状态，并等待 ENA 或 WAK 再次尝试重启。如果失败，器件将按照上述相同的序列运行。

*) 如果过温事件是进入 FAILSAFE 的原因，则器件将保持在该状态下t_{TSD_min}。

9.1.4 电源序列

BUCK PREREG 和 QST 是内部上电复位（POR）释放时第一个进行升压的调节器。但 QST 输出电压电平对电源序列没有影响，并且不影响其他电源轨的启动。此外，调节器的 UV 事件会被屏蔽，直到输出超过其欠压阈值。

如果调节器在 t_{StG} 过期之前未能建立高于其欠压阈值的电压，则适用以下情况之一：

1. 移至 FAILSAFE：
   - BUCK PREREG
   - BOOST（如果检测到使用情况）
   - QUC
   - BUCK CORE
   - QST
2. 跳过相应调节器的启动并将其禁用。根据故障反应中接地短路检测的故障反应发出中断（不阻塞上电序列）
   - BUCK IF (如果检测到使用情况)
   - VMON1（如果检测到使用情况）
   - QVR
   - QCO
   - VMON2（如果检测到使用情况）

在完成上电序列后，当 QUC、QST 和 BUCKCORE 超过其欠压阈值时，就会发生初始复位释放（RESOUT 变为“高”）。有关复位功能的更多详细信息，请参见复位功能（RESOUT）

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当引脚 VS 和 VIQST 上的输入电压高于$V_{PWD_TH_H}$且经过 t_{SUP_PWUP} 时间后，PREREG 开始切换。

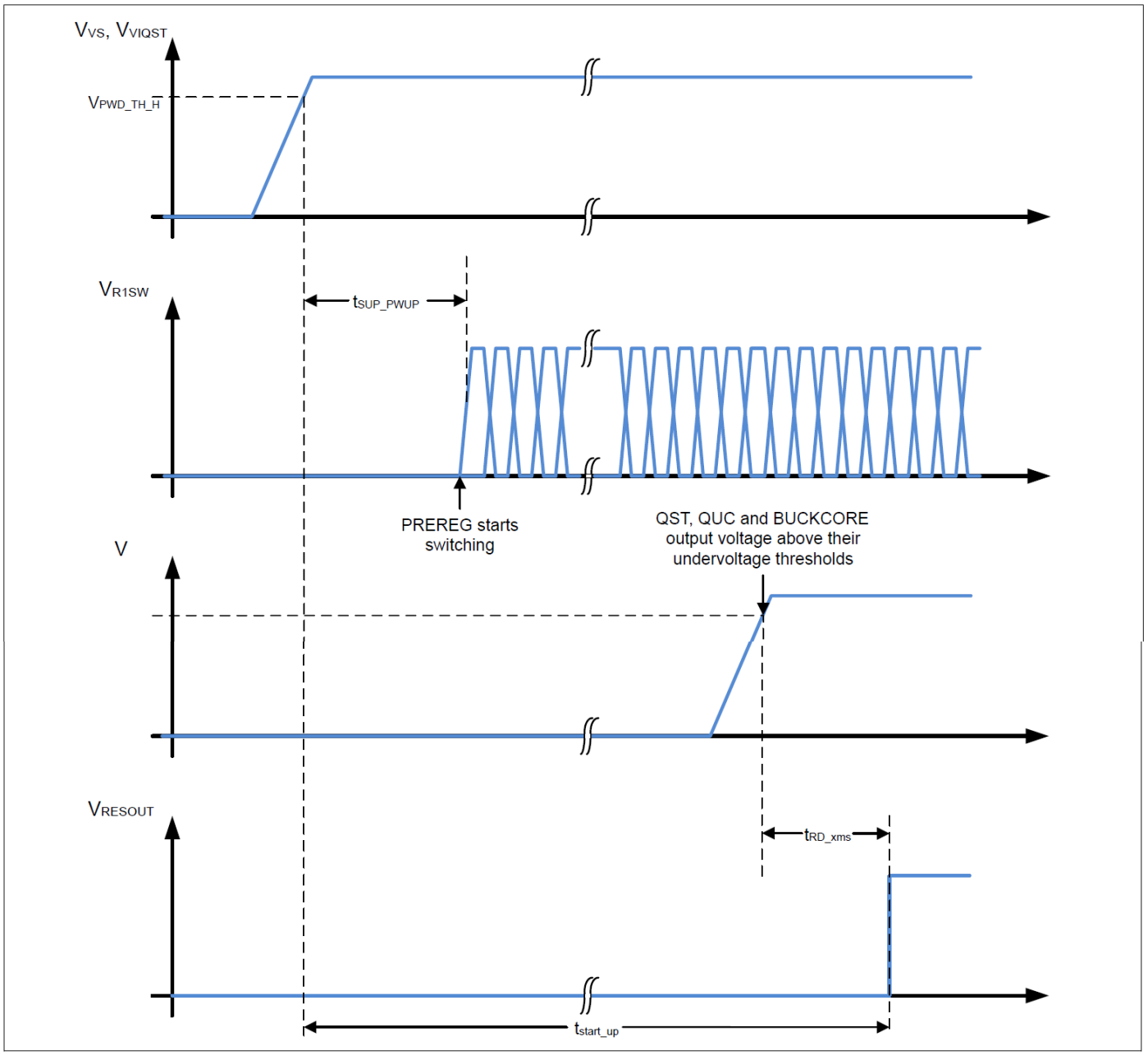


图 29　　系统启动时序

如果在器件执行下电或上电序列时发出状态转移请求，则以下几点适用：

- 指令被忽略
- 触发中断
- 故障信息存储在专用寄存器中

器件通过 DEV_STAT 中的寄存器状态标志提供静态配置（激活稳压器）的状态信息。

9.1.4.1　　上电序列方案 A

硬件配置（HWCFG）决定启动序列为方案 A 或方案 B。

如果选择上电序列方案 A，则执行如下所述的序列。因此，只有当前一个输出电压轨超过其欠压阈值时，下一个电压轨才会逐渐升高。QST 独立于其他稳压器启动，并且不是另一个调节器的先决条件。

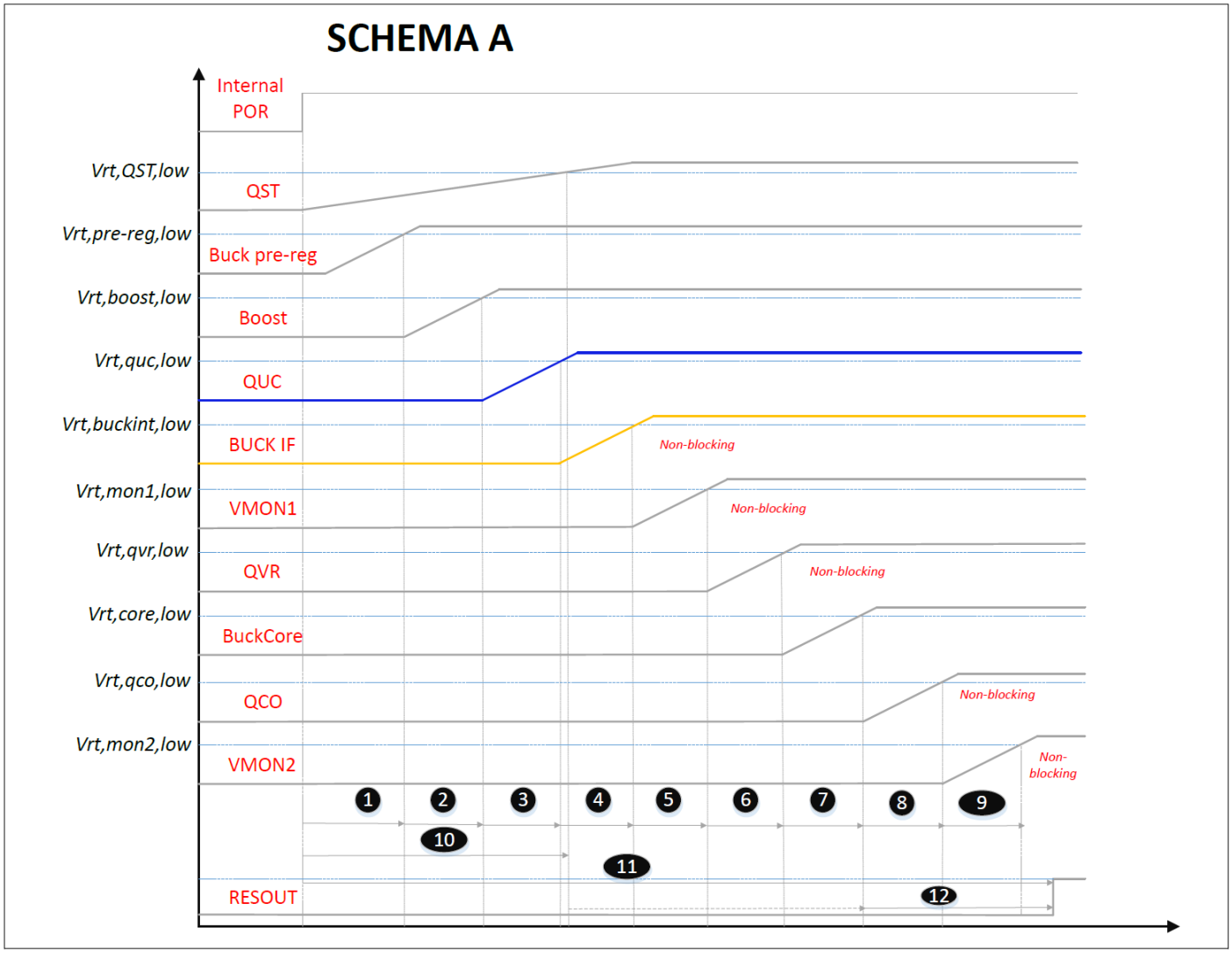


图 30　　上电序列方案 A

1 -> PREREG 启动
2 -> BOOST 启动（仅当自动检测到时）
3 -> QUC 启动
4 -> BUCKIF 启动（仅在首次上电序列中自动检测到时）
5 -> VMON1 启动（仅在首次上电序列中自动检测到时）
6 -> QVR 启动
7 -> BUCK CORE 启动
8 -> QCO 启动
9 -> VMON2 启动（仅在首次上电序列中自动检测到时）
10 -> QST 启动
11 -> 完整启动所需时间：t_{start_up}
12 -> RESOUT 延迟时间（更多信息参见复位功能（RESOUT）

9.1.4.2　　上电序列方案 B

如果选择上电序列方案 B，则执行如下所述的序列。因此，只有当前一个输出电压轨超过其欠压阈值时，下一个电压轨才会逐渐升高。QST 独立于其他稳压器启动，并且不是另一个调节器的先决条件。

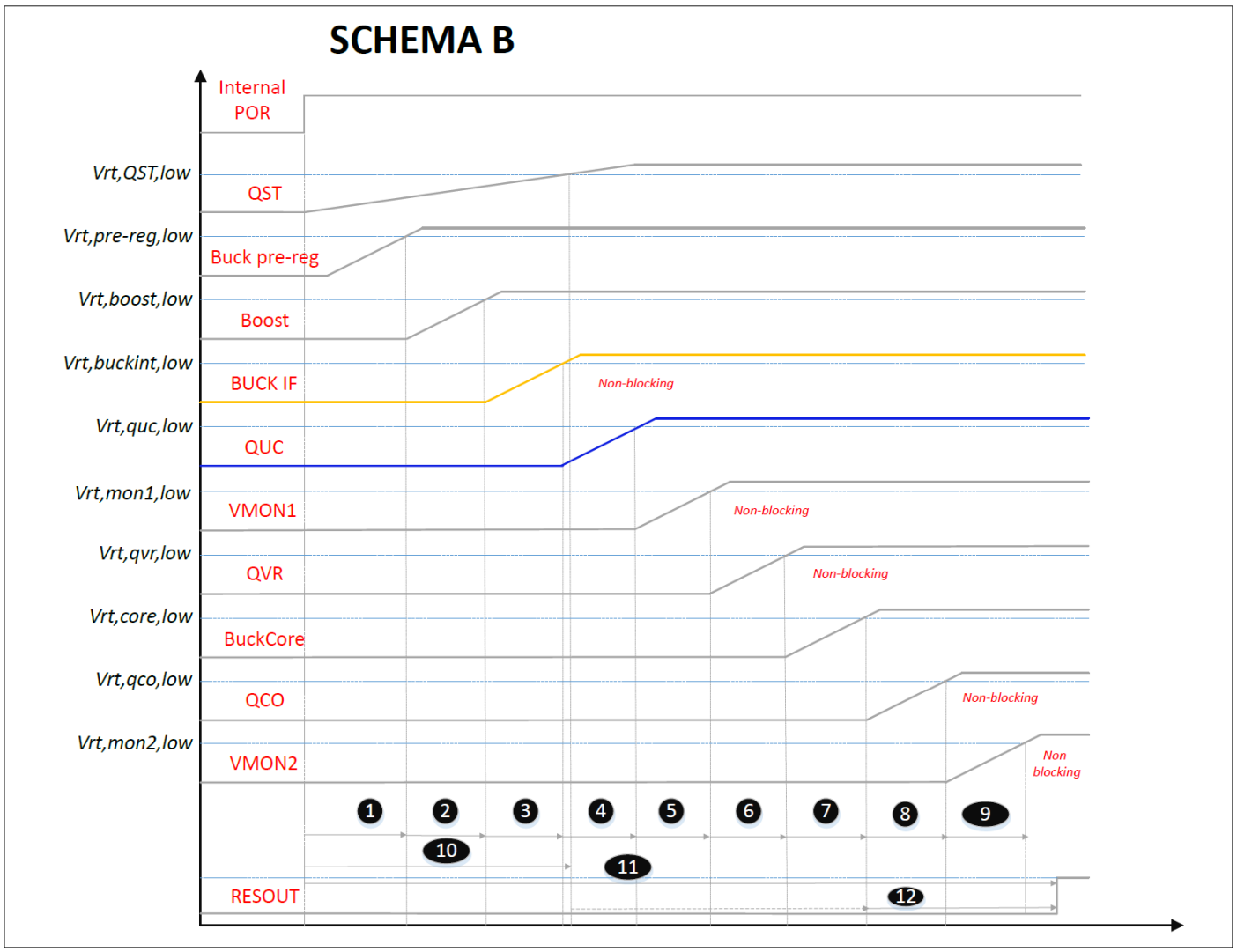


图31　　电源序列方案 B

1 -> PREREG 启动
2 -> BOOST 启动（仅当自动检测到时）
3 -> BUCKIF 启动（仅在首次上电序列中自动检测到时）
4 -> QUC 启动
5 -> VMON1 启动（仅在首次上电序列中自动检测到时）
6 -> QVR 启动
7 -> BUCK CORE 启动
8 -> QCO 启动
9 -> VMON2（仅在首次上电过程中自动检测到时）
10 -> QST 启动
11 -> 完整启动所需时间：t_{start_up}
12 -> RESOUT 延迟时间（更多信息参见复位功能（RESOUT））

9.1.4.3　　下电序列

如果器件转换为 STANDBY 或 SLEEP，则器件会在相应的下电序列之后禁用输出电压轨。当转换到 SLEEP 时，序列将忽略配置为保持开启的轨道和相关延迟。

如果选择了上电序列方案 A

1. 禁用 VMON2
2. 等待 t_{SDT_VMON12}
3. 禁用 QCO
4. 等待 t_{SDT_TMR}
5. 禁用 BUCK CORE
6. 等待 t_{SDT_TMR}
7. 禁用 QVR
8. 等待 t_{SDT_TMR}
9. 禁用 VMON1
10. 等待 t_{SDT_VMON12}
11. 禁用 BUCK IF
12. 等待 t_{SDT_TMR}
13. 禁用 QUC
14. 等待 t_{SDT_TMR}
15. 禁用 BOOST
16. 等待 t_{SDT_TMR}
17. 禁用 BUCK PREREG
18. 等待 t_{SDT_TMR}

如果选择了上电序列方案 B

1. 禁用 VMON2
2. 等待 t_{SDT_VMON12}
3. 禁用 QCO
4. 等待 t_{SDT_TMR}
5. 禁用 BUCK CORE
6. 等待 t_{SDT_TMR}
7. 禁用 QVR
8. 等待 t_{SDT_TMR}
9. 禁用 VMON1
10. 等待 t_{SDT_VMON12}
11. 禁用 QUC
12. 等待 t_{SDT_TMR}
13. 禁用 BUCK IF
14. 等待 t_{SDT_TMR}
15. 禁用 BOOST
16. 等待 t_{SDT_TMR}
17. 禁用 BUCK PREREG
18. 等待 t_{SDT_TMR}

器件在相应的下电序列后禁用输出电压轨。

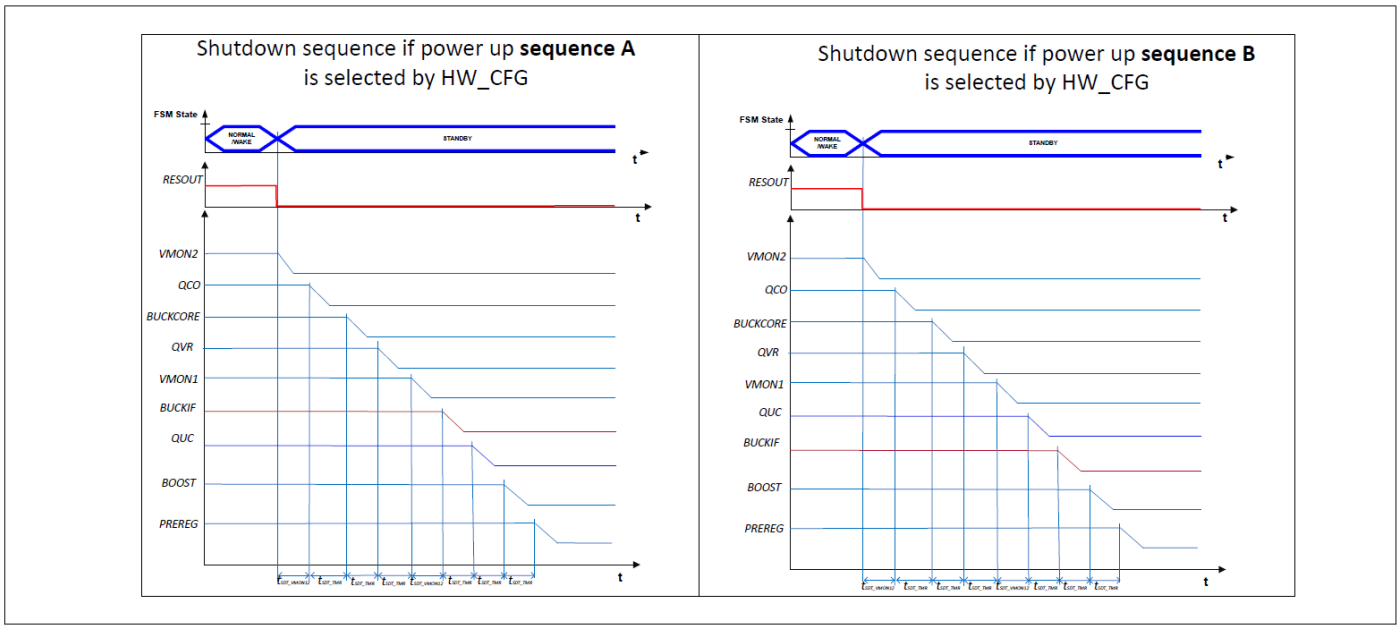


图 32 下电序列

注释：参数 t_{SDT_TMR} 和 t_{SDT_VMON12} 表示内部延迟，不受外部条件控制。

9.2 电气特性：状态机（FSM）

表 33 电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supplies start-up time	t_{SUP_PWUP}	–	4	6	ms	• V_{VS} and $V_{VIQST} \geq V_{PWD\_TH\_H}$ (V_S and V_{IQST} pins assumed to be connected together externally) • V_{SSC_S} < 1V at startup • Max. Capacitance at SSC_S pin is 1uF	DS-2083
Power up threshold	$V_{PWD\_TH\_H}$	–	–	6	V	V_{VS} increasing	DS-2156
Power down threshold low	$V_{PWD\_TH\_L}$	2.5	–	5.5	V	V_{VS} decreasing BOOST not used	DS-1555
System shutdown time	t_{SDT}	–	–	15	ms	–	DS-1536
Thermal shutdown time	t_{TSD_min}	0.9	1	1.1	s	–	DS-1548

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal voltage rails shutdown delay	t_{SDT_TMR}	0.9*t_{SDT_TMR}	t_{SDT_TMR}	1.1*t_{SDT_TMR}	µs	t_{SDT_TMR}: Programmable via SPI in DEV_CFG4.FSM_SDT_TMR	DS-1936
VMON1/2 shutdown time	t_{SDT_VMON12}	0.9*t_{SDT_VMON12}	t_{SDT_VMON12}	1.1*t_{SDT_VMON12}	µs	t_{SDT_VMON12}: Programmable via SPI in DEV_CFG4.FSM_SDT_VMON12	DS-1937
Short to ground detection time for internal regulators except QST	t_{STG}	0.9	1	1.1	ms	–	DS-1538
Short to ground detection time for QST regulator	t_{STG_QST}	1.8	2	2.2	ms	–	DS-1537
FAILSAFE time	$t_{FAILSAFE\_min}$	18	20	22	ms	–	DS-1547
INIT timer	t_{INIT}	540	600	660	ms	–	DS-1549
Low power state transition time	t_{TR_DEL}	100	–	1600	µs	t_{TR_DEL} is programmable between 100 µs and 1.6 ms via SPI The default value is set to 900 µs	DS-1503
Accuracy for low power state transition time	$t_{TR\_DEL\_ACC}$	-20	–	20	%	–	DS-1550
State transition time	t_{TR}	–	–	200	µs	–	DS-1551
State transition time to Initialization state	t_{TR_INIT}	–	–	3	ms	Transition from STANDBY/ FAILSAFE to INIT state: Measured from rising edge of ENA/WAKE to R1SW rising edge; Move to INIT faults: Measured from RESOUT falling edge to QVR enable or R1SW rising edge	DS-1552

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption							
SLEEP state current consumption	I_{q_SLEEP}	–	7	10	mA	Current consumptions are measured from V_S(T30) without load current applied to post regulators: • BUCK PREREG, QUC, BUCK IF, QCO and QST are enabled • BUCK CORE and QVR are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V; • T_j ≤ 85°C	DS-2077

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	7.9	13.2	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG enabled • BOOST, BUCK CORE, QUC, BUCK IF, QCO and QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2106

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.2	10.3	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG and BOOST are enabled • BUCK CORE, QUC, BUCK IF, QCO and QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2108

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.3	10.5	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST and QUC are enabled • BUCK CORE, BUCK IF, QCO and QST and QVR are switched off; • V_{R1FB} = V_{R1FB_4V}; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • T_j ≤ 85°C	DS-2110

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.8	11.3	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF and QUC are enabled • BUCK CORE, QCO, QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2112

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	7.8	13	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF, QVR and QUC are enabled • BUCK CORE, QCO, QST are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2114

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	10.2	17	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF, QVR, BUCK CORE, QCO and QUC are enabled • QST is switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2116

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	5.1	8.5	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG is enabled • BUCK IF, QVR, BUCK CORE, QCO, QUC and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2118

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	5.4	9	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG and QUC are enabled • BUCK IF, QVR, BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2120

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6	10	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF and QUC are enabled • QVR, BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2122

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.7	11.2	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF, QVR and QUC are enabled • BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2124

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	8.2	13.7	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF, QVR, BUCK CORE, QCO and QUC are enabled • QST is switched off; • BOOST is not populated; • V_{R1FB} = V_{R1FB_5V5}; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq$ 85°C	DS-2126

（表格续下页……）

表 33 （续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption	$I_{q\_STANDBY\ OFF}$	–	20	24	µA	Current consumptions are measured from V_S(T30): • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QST, QCO) are switched off • VMON1 and VMON2 are disabled • Error pin monitoring and all watchdog channels are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2079

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with QST ON	$I_{q\_STANDBY\_ON}$	–	54	70	µA	Current consumptions are measured from V_S(T30): • QST is switched ON • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-1544

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with WUT ON	$I_{q\_WUT\_ON}$	–	–	50	µA	Current consumptions are measured from V_S(T30): • QST is switched OFF • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is enabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2052

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with QST and WUT ON	$I_{q\_STANDBY\_WUT\_ON}$	–	–	70	µA	Current consumptions are measured from V_S(T30): • QST is switched ON • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and FWD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is enabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2051
Operational state current consumption	$I_{q\_Operational}$	–	20	30	mA	Current consumptions are measured from V_S(T30) without load current applied to post regulators: • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QTS, QVR, QCO) are switched on • ERRx pin monitoring, WWD and FWD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • f_{DCDC} = 2.2 MHz • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C	DS-2080

（表格续下页……）

表 33　　（续）电气特性：状态机（FSM）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向流入引脚的电流（除非另有说明）[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FAILSAFE state current consumption	$I_{q\_FAILSAFE}$	–	120	200	µA	Current consumptions are measured from V_S(T30): • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QST, QCO) are switched off • ERRx pin monitoring, WWD and FWD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 18 V • T_j ≤ 40°C • $t_{FAILSAFE}$ > $t_{FAILSAFE\_min}$ • Quiescent current also depending on the leakage of diode D3	DS-1546

1)　未经过生产测试，由设计指定

10 监测功能

10.1 看门狗功能（WD）

10.1.1 看门狗功能介绍（WD）

看门狗的目的是通过时间和逻辑程序序列监测来为应用微控制器提供监测机制。看门狗可以检测有缺陷的 MCU 程序序列，其中各个程序元素（例如：软件模块、子程序或指令）以错误的序列或在错误的时间段内进行处理，或者处理器的时钟出现故障。

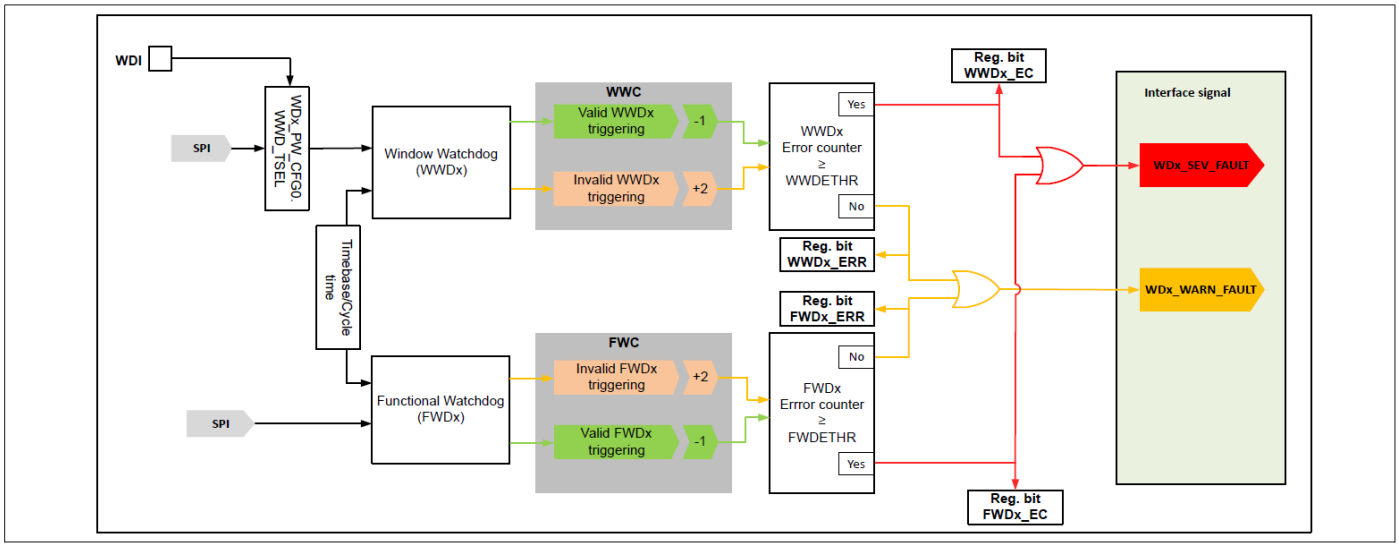


图 33 看门狗功能的功能框图

(x = 1; 2)

该器件包含两个独立的看门狗实例（WD）。每个实例由一个窗口看门狗模块（WWD）和一个功能看门狗模块（FWD）组成：

- WD1：由 WWD1 和 FWD1 组成
- WD2：由 WWD2 和 FWD2 组成

注释： *看门狗实例2 仅在REDUCED OPERATION 为启用的情况下才能使用(**REDOP_RS_CFG1.EN = 1**)。*

看门狗模块区分以下服务：

- "有效 WWDx 触发" 或"无效 WWDx 触发"
- "有效 FWDx 触发" 或"无效 FWDx 触发"

每个 WWD 模块和每个 FWD 模块都有自己的错误计数器，并监控看门狗触发器。这使得 WWD 和 FWD 并行操作成为可能。WWDx 与其对应的 FWDx 共享相同的时基。

基本时基配置由寄存器位 WDx_PW_CFG0.CYC 完成。为了进一步缩短时基，可以启用一个额外的除以 10 的分频器，这会产生如图所示的时基：

$$time\ \ base\ \ = \frac{WDx\_RS\_CFG0.CYC}{WDx\_RS\_CFG1.CYC\_DIV}\ \text{(interpreted value)}$$

公式 1

配置

每个看门狗模块都可以在寄存器位 **WDx_PW_CFG0.WWD_EN** 和 **WDx_PW_CFG0.FWD_EN** 中独立激活和停用。

可以在寄存器位 **WDx_PW_CFG1.SLP_EN** 中配置进入 SLEEP 状态时看门狗的自动停用。

10.1.2 窗口看门狗（WWD）

10.1.2.1 功能描述：窗口看门狗（WWD）

窗口看门狗（WWDx）可在 **WDx_PW_CFG0.WWD_TSEL** 中配置为由下列事件之一触发：

- 数字输入引脚 WDI 的下降沿
- 通过 SPI 写入 WWD1_TRIG.TRIG。为了触发看门狗：
  - 读取通过 SPI 接收到的最后一个内部服务值（**WWDx_TRIG.TRIG_STAT**）
  - 将（**WWDx_TRIG.TRIG_STAT**）的反转值写入 **WWDx_TRIG.TRIG** 位字段

如果触发事件发生在打开窗口期间 (OW)，则器件检测到**“有效 WWDx 触发”**。此时，打开窗口立即关闭，关闭窗口开始运行。

如果在打开窗口期间没有发生触发事件，或者触发事件发生在关闭窗口期间（CW），则器件检测到**“无效 WWDx 触发”**。

打开窗口 t_{OW} 和关闭窗口 t_{CW} 的持续时间可用以下公式计算：

$$t_{OW} = (\text{WWDx\_PW\_OW\_CFG.OW} + 1) \times 50 \times time\ base$$

公式 2

$$t_{CW} = (\text{WWDx\_PW\_CW\_CFG.CW} + 1) \times 50 \times time\ base$$

公式 3

窗口看门狗的关闭窗口的持续时间也可以配置为 0。如果使用此设置（**WWDx_PW_CW_CFG.CW_DIS**= 1），则在打开窗口中成功触发将立即再次初始化一个新的打开窗口。

10.1.2.1.1 窗口看门狗有效触发

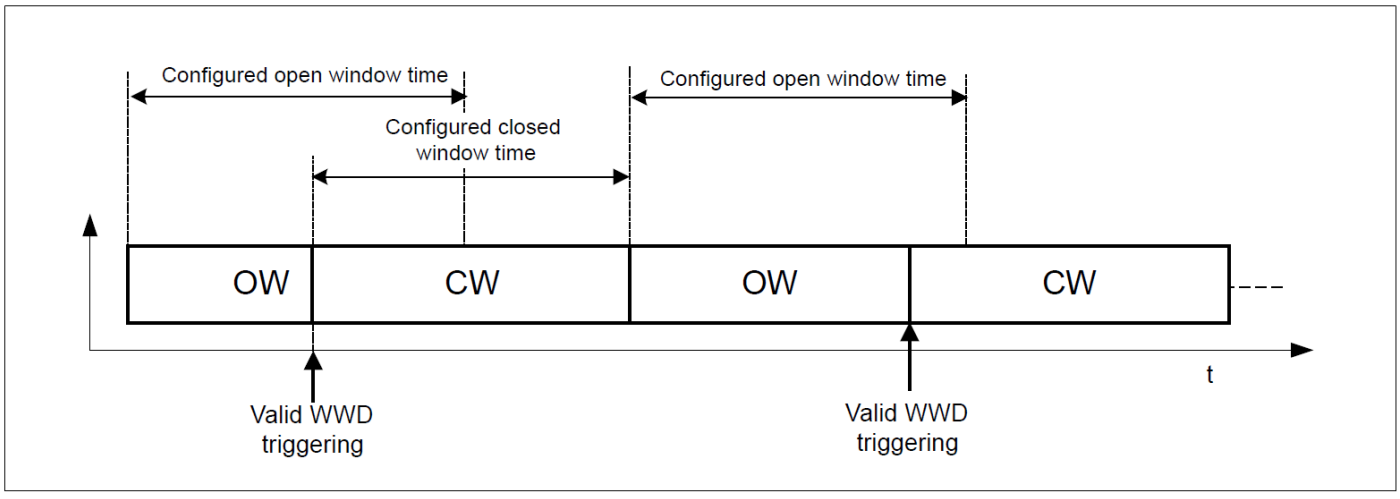


图 34 窗口看门狗有效触发

最初，窗口看门狗以打开窗口开始运行。如果成功触发，打开窗口会立即关闭，并启动一个关闭窗口。关闭窗口激活达到设定的时间后，会再次启动一个打开窗口。重新配置后，窗口看门狗以配置的打开窗口启动，其相应的错误计数器为复位。

10.1.2.1.2 由于开窗期间未触发导致的无效触发

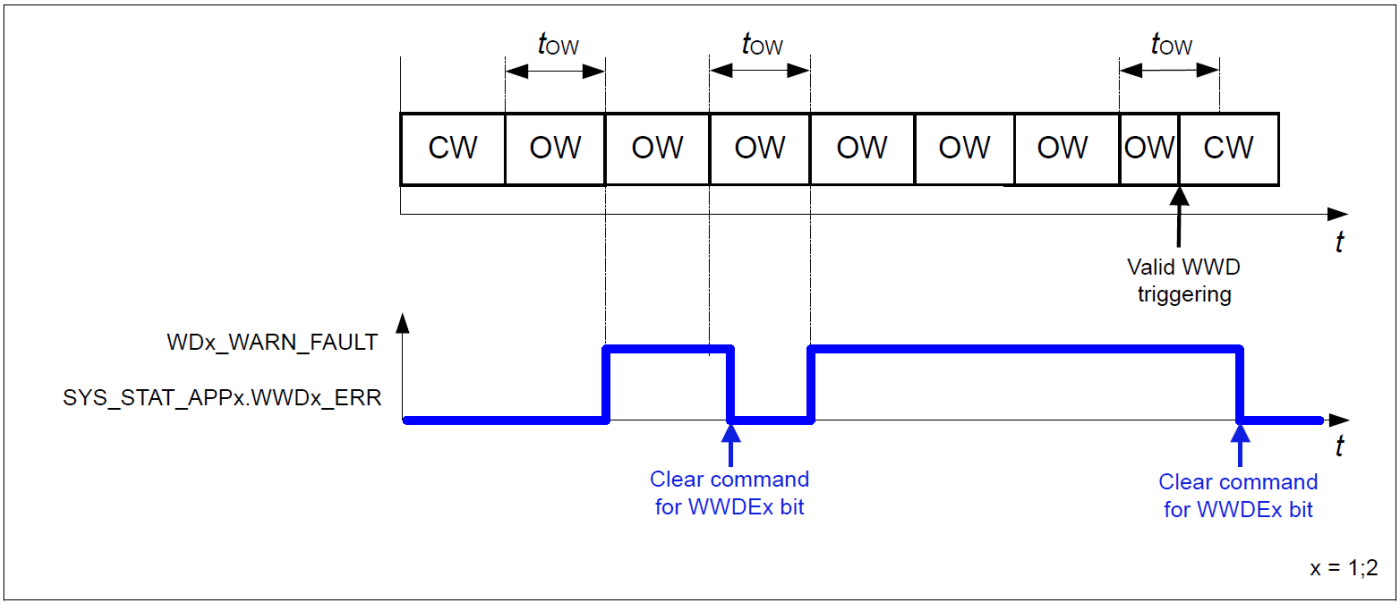


图 35 由于开窗期间未触发导致的无效服务（假设错误计数器始终小于阈值）

如果打开窗口在没有任何触发的情况下过期，则看门狗会以打开窗口开始一个新的时序序列，并且器件将执行以下操作：

1. 将对应的错误计数器值递增 2，参见章节 10.1.2.1.5
2. 如果错误计数器始终低于配置的阈值：
   - 则：
     - 生成看门狗警告故障 WDx_WARN_FAULT
     - 设置对应的错误位 **SYS_STAT_APPx.WWDx_ERR**，该错误位可通过 SPI 清除
   - 否则：
     - 生成看门狗严重故障 WDx_SEV_FAULT

(x = 1; 2)

10.1.2.1.3 由于关窗期间触发导致的无效触发

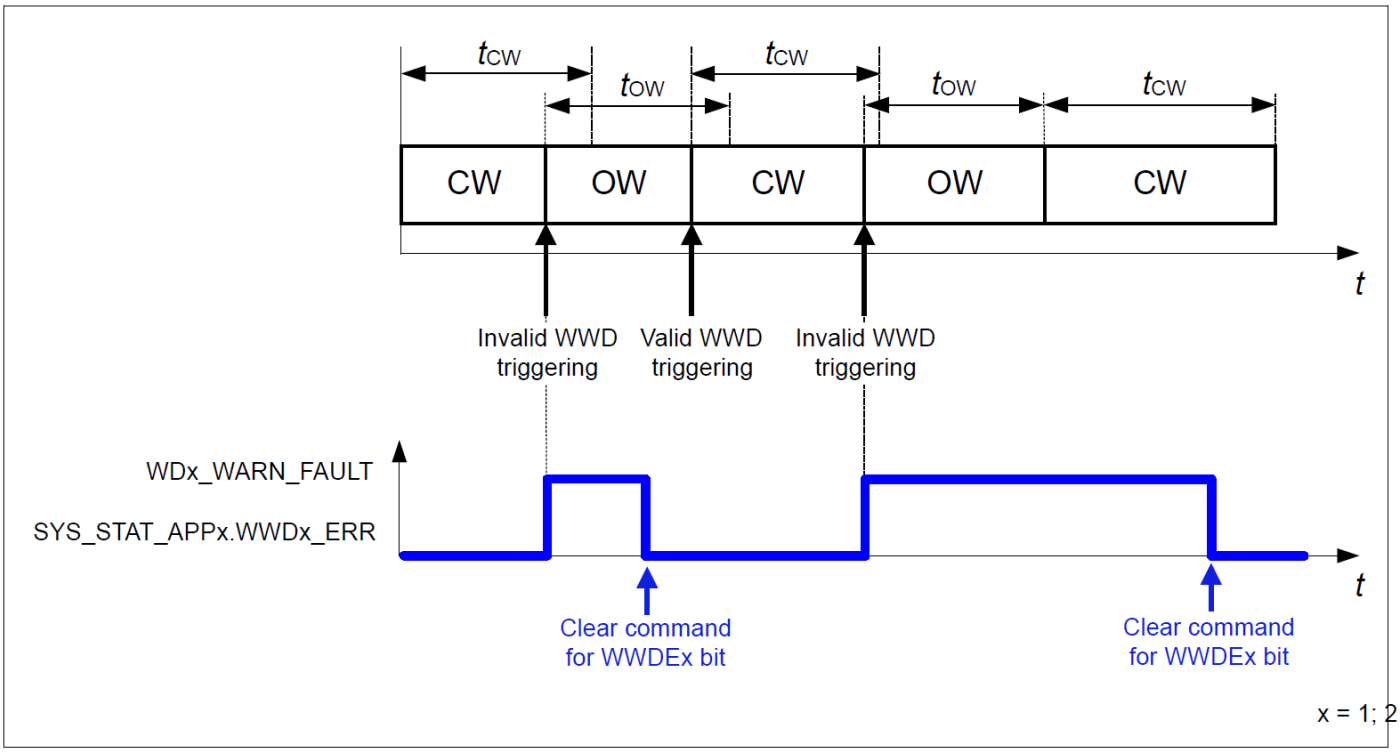


图 36 由于关窗期间触发导致的无效触发（假设错误计数器始终小于阈值）

如果在关闭窗口期间触发看门狗，则它会在打开窗口时启动一个新的看门狗时序序列，并且器件执行以下操作：

1. 将对应的错误计数器值递增 2，参见章节 10.1.2.1.5
2. 如果错误计数器始终低于配置的阈值：
   - 则：
     - 生成看门狗警告故障 WDx_WARN_FAULT
     - 设置对应的错误位 **SYS_STAT_APPx.WWDx_ERR**，该错误位可通过 SPI 清除
   - 否则：
     - 生成看门狗严重故障 WDx_SEV_FAULT

(x = 1; 2)

10.1.2.1.4 看门狗启动行为（使能和复位）

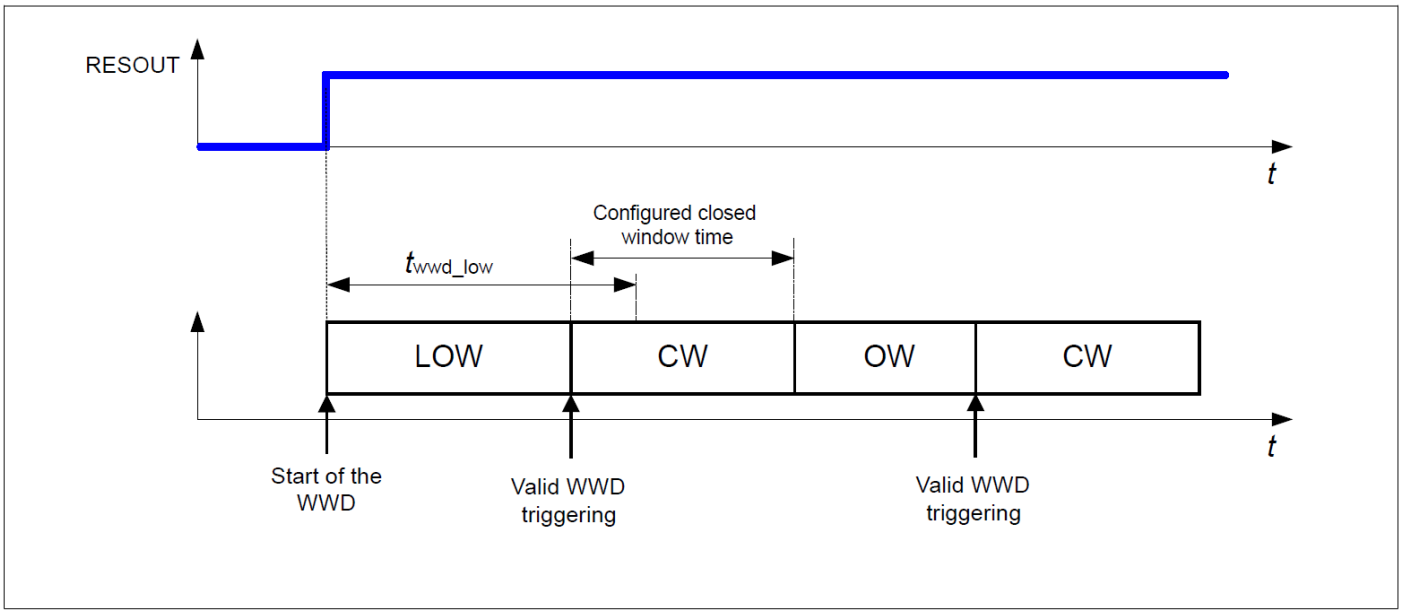


图 37 看门狗初始化阶段

当进入 INIT 状态且 RESOUT 被释放（引脚 RESOUT 变为高电平）时，看门狗被启用，并开始第一个看门狗时序窗口序列，该时序窗口为长开窗口。长开窗口持续时间t_{WWD_LOW} 与 INIT 计时器持续时间 t_{INIT} 相匹配。如果在 t_{WWD_LOW} 内收到有效触发信号， 则看门狗开始按本章所述的方式运行；否则，看门狗长开窗口与 INIT 计时器同时超时， 并生成 INIT_TIMER_FAULT 错误。

10.1.2.1.5 窗口看门狗错误计数器

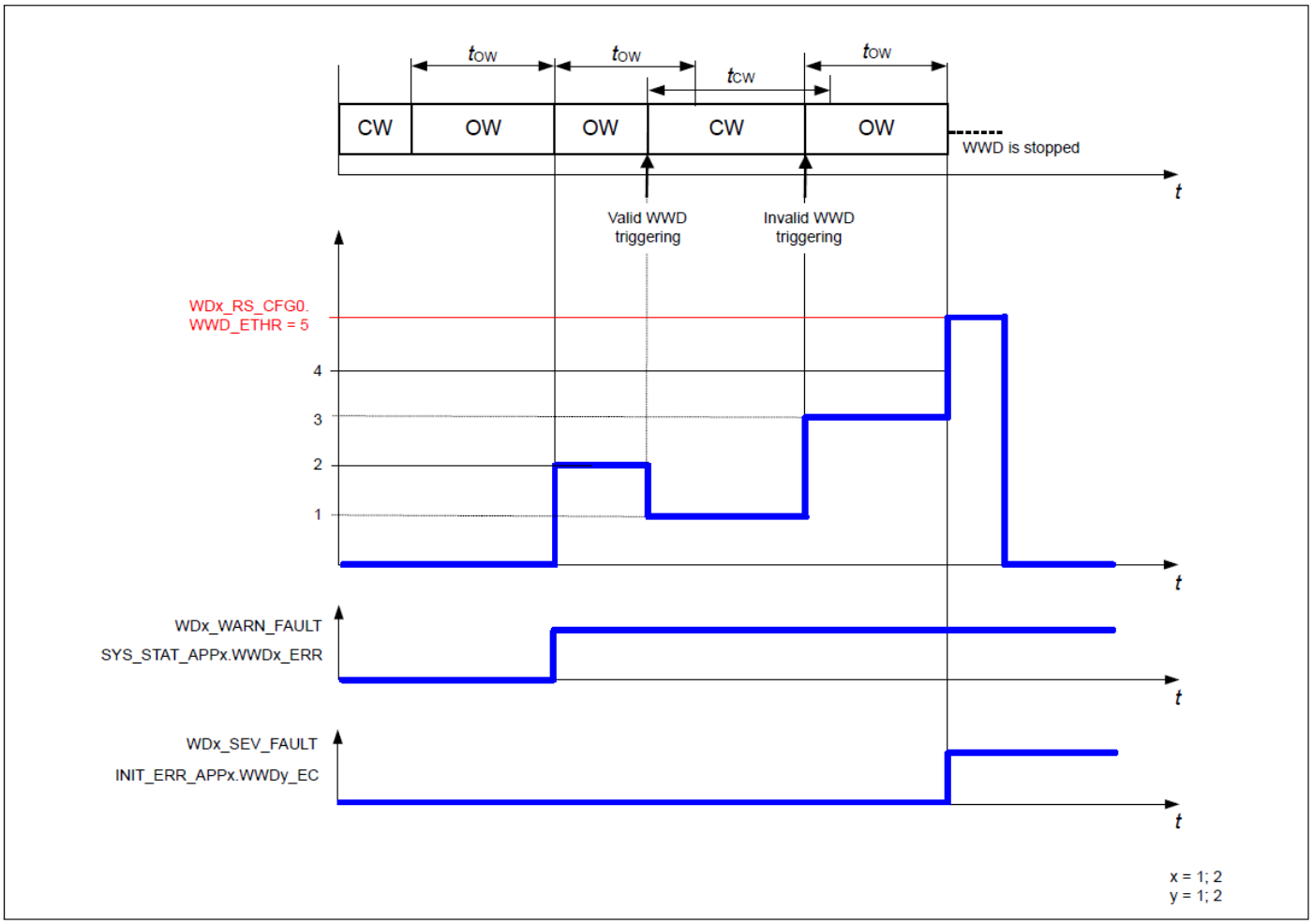


图 38 窗口看门狗错误计数器

如果器件检测到无效触发，则将 **WWDx_ECNT_STAT.ECNT** 的值加 2。如果器件检测到有效触发，则将 **WWDx_ECNT_STAT.ECNT** 的值减 1。
如果 ECNT 位字段的值达到配置的 WWD 错误计数阈值 **WDx_RS_CFG0.WWD_ETHR** 的值，器件将执行以下操作：

- 生成看门狗严重故障 WDx_SEV_FAULT
- 设置对应的错误位 **INIT_ERR_APPx.WWDy_EC**，该错误位可通过 SPI 清除
- 清除错误计数器

10.1.2.1.6 配置看门狗后的时序约束和行为

在配置看门狗之后和第一次服务之前，存在一个需要遵守的时序约束。微控制器对看门狗的新配置，例如打开/关闭窗口时间，可能需要最长 $t_{config\_delay\_wd}$ 的时间才会被激活。因为看门狗配置寄存器属于受保护的寄存器，所以必须发送解锁和锁定指令。只有成功接收到对看门狗配置所做的锁定指令更改后，才会将镜像到相应的反应状态寄存器，并由此提供给 PMIC 模块。因此，锁定指令标志着在通过 SPI 接收第一个触发信号并将其应用于新配置之前时序的开始。然而，此时序约束不适用于通过 WDI 引脚触发，因为采样时间 t_{WDI_spl} 和滤波标准的组合将始终长于 $t_{config\_delay\_wd}$。

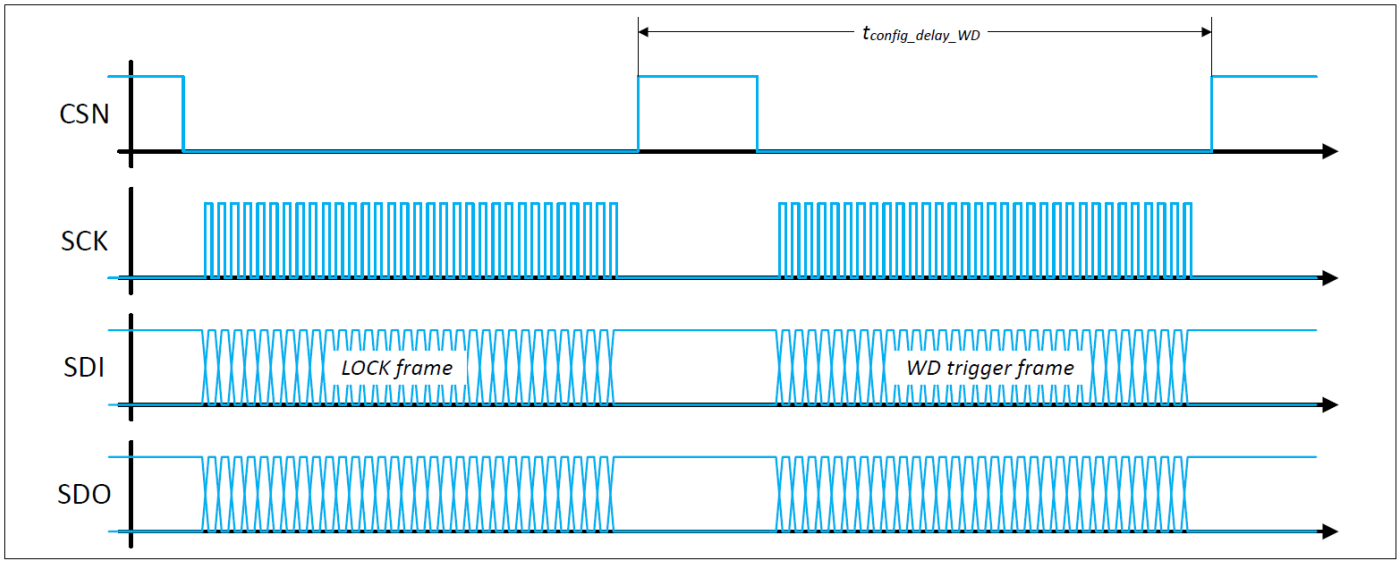


图 39　　看门狗模块配置后的看门狗触发延时

10.1.2.2　电气特性：窗口看门狗（WWD）

表 34　　电气特性：窗口看门狗（WWD）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cycle time	$t_{wwd\_cycle\_0}$	90	100	110	µs	Selectable via SPI	DS-1660
Cycle time, default	$t_{wwd\_cycle\_1}$	900	1000	1100	µs	Selectable via SPI	DS-1659
Long open window time	t_{wwd_low}	540	600	660	ms	Used for the initial WWD activation, or after each WWD restart due to recovery from a fault condition	DS-1653
WDI sample time	t_{WDI_spl}	45	50	55	µs	2) 1)	DS-2166
WD configuration-trigger delay	$t_{config\_delay\_wd}$	–	–	22	µs	2)	DS-2068

1)　由于 ERR2 和 WDI 共用同一个引脚，因此它们的电压电平、滞后和电流规格等电气特性也相同。因此，它被称为表 电气特性：错误监测 （ERR MON）[EC-Table-P]
.

2)　未经过生产测试，由设计指定

10.1.3 功能看门狗 (FWD)

10.1.3.1 功能描述：功能看门狗（FWD）

功能看门狗（FWD，也称为问答看门狗）从一个表中生成一个问题，并将心跳计数器从零开始计数。为了正确触发功能看门狗，必须在心跳周期内，按特定顺序将每个问题的正确响应字节写入应答寄存器。

心跳计时器会递增，直到达到其配置的心跳计时器周期。该周期通过寄存器 **FWDx_PW_HBTP_CFG.HBTP** 配置。周期长度遵循以下心跳周期公式：

$$heartbeat\ \ time = (\mathrm{FWD}x\_\mathrm{RS\_HBTP\_CFG}.\mathrm{HBTP} + 1) \times 50 \times time\ \ base \quad (\text{interpreted value})$$

公式 4

10.1.3.1.1 功能看门狗服务

启用或重新配置 FWD 后，其相应的 HBT 开始运行。它会等待 4 个字节连续写入 FWDx_RSP.RSP 或 FWDx_RSP_SYNC.RSP_SYNC。响应字节必须与从 FWDx_STAT.QUEST 读取的问题相匹配。如果在 HBT 过期之前所有字节都正确写入，则服务成功，错误计数器递减，并从 FWDx_STAT.QUEST 中的下一个问题开始新的序列。收到第 4 个响应字节后，检查接收到的字节是否正确。如果响应不正确，并且最后一个字节写入了 FWDx_RSP_SYNC.RSP_SYNC，则 FWDx 的错误计数器会递增。此外，如果 HBT 过期，则相应的错误计数器会递增。状态寄存器 FWDx_STAT 在 FWD 重新配置时复位。

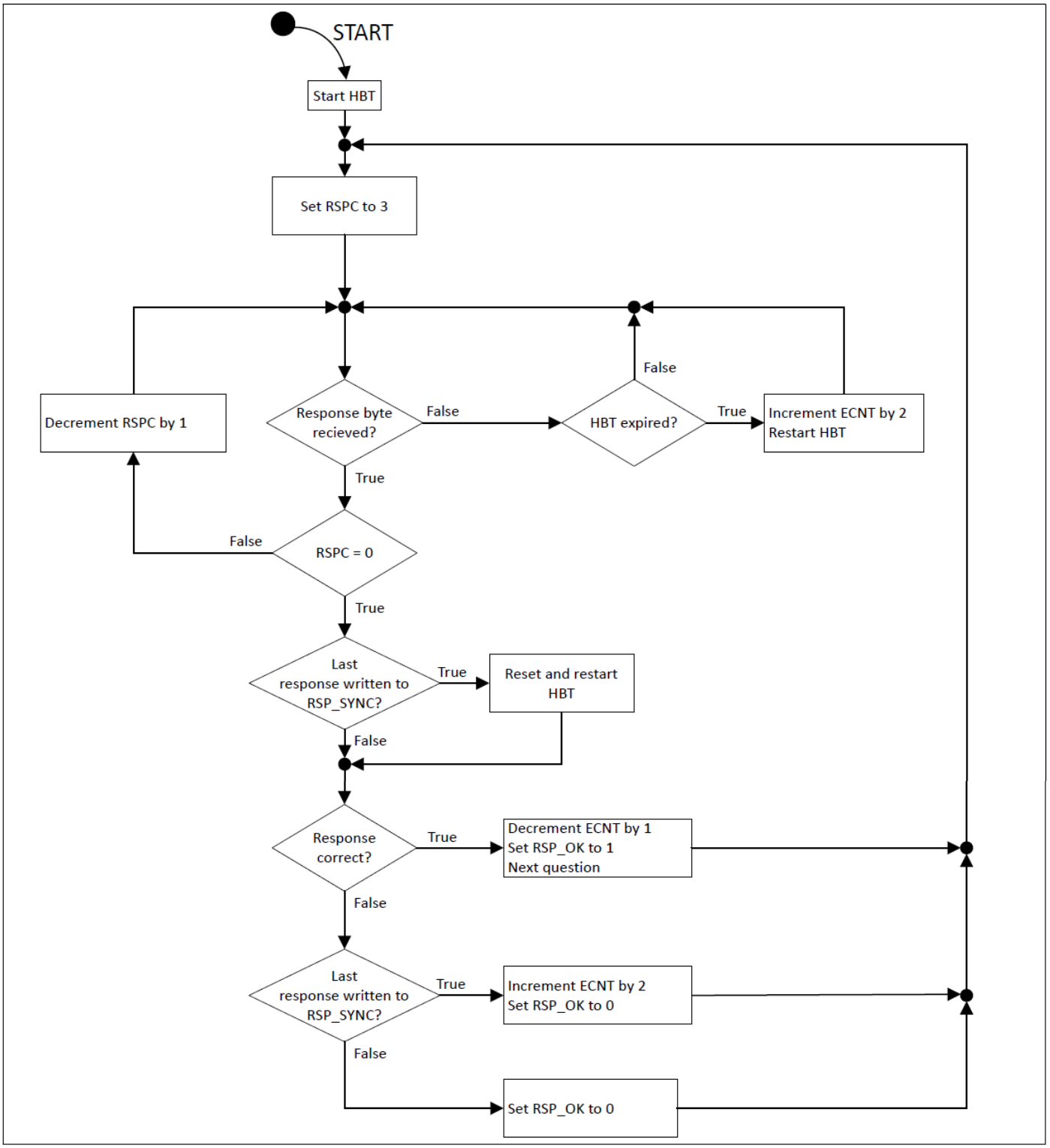


图 40　　FWD 流程图

功能看门狗的有效触发

问题由 4 位组成，相应的应答由四个连续的应答字节组成。

寄存器 **FWDx_STAT.QUEST** 中每个问题的应答都需要写入响应寄存器 **FWDx_RSP.RSP** 或 **FWDx_RSP_SYNC.RSP_SYNC** 中。

表 35 功能看门狗问题和响应

QUEST[3:0]	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

如果某个问题满足以下所有条件，则 FWD 被正确触发（有效触发）：

- 四个响应字节的顺序正确，从 RESP3 到 RESP0
- 四个响应字节均已正确写入响应寄存器。

要复位心跳计数器，必须将最后一个响应 (RESP0) 写入同步响应寄存器**FWDx_RSP_SYNC.RSP_SYNC** 。

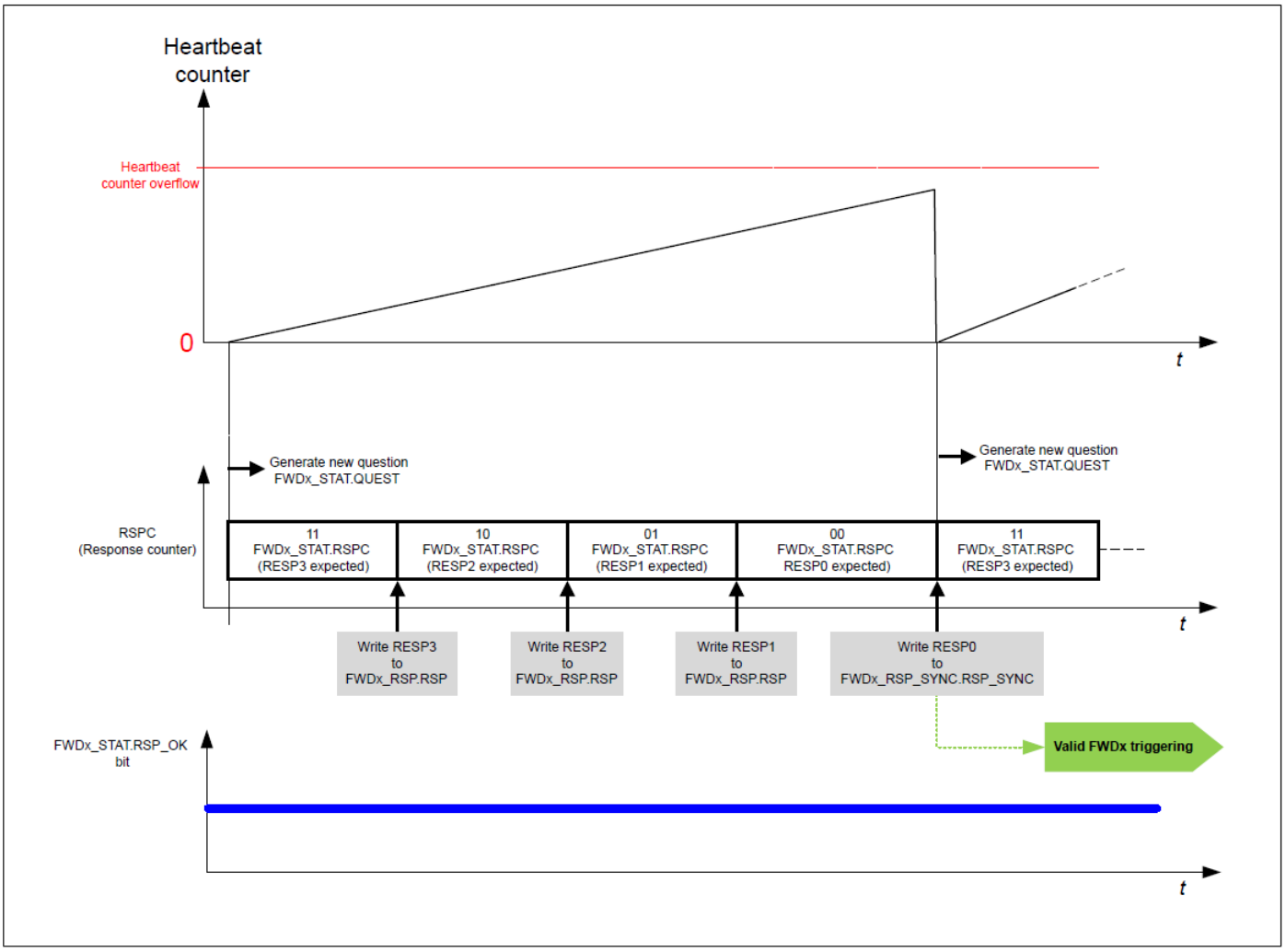


图 41　　示例 FWD：可能的有效触发

检测到有效触发信号后，器件将执行以下操作：

- 生成新问题
- 将响应计数器 RSPC 复位为 3
- 如果相应的错误计数器值不为 0，则将其减 1，参见章节 10.1.2.1.5
- 将响应字节 **FWDx_STAT.RSP_OK** 的对应状态位设置为 1
- 如果最后一个字节已写入 **FWDx_RSP_SYNC.RSP_SYNC**，则 HBT 周期也会复位并重新启动

功能看门狗触发无效

如果满足以下任一条件，则 FWD 被错误触发（无效触发）：

- 四个响应字节的顺序或内容有误
- 心跳周期过期（心跳计数器溢出）

当检测到无效触发信号时，器件将执行以下操作：

- HBT 过期：
  - 将错误计数 **FWDx_STAT.ECNT** 加 2，请参见章节 10.1.3.1.2
  - 复位并重启 HBT
- 如果第 4个字节写入了 **FWDx_RSP_SYNC.RSP_SYNC**：
  - 复位并重启 HBT

- 设置状态位 **FWDx_STAT.RSP_OK**为 0
- 将错误计数器 **FWDx_STAT.ECNT** 加 2，请参阅章节 10.1.3.1.2

• 如果第 4 个字节写入了 **FWDx_RSP.RSP**：

- 设置状态位 **FWDx_STAT.RSP_OK**为 0

• 如果错误计数器 **FWDx_STAT.ECNT**增加（参见故障反应）：

- 如果错误计数器仍低于配置的错误阈值，则生成看门狗警告故障 WDx_WARN_FAULT，请参阅第 9 章
- 设置相应的错误位 **SYS_STAT_APPx.FWDx_ERR**，该错误位可通过 SPI 清除

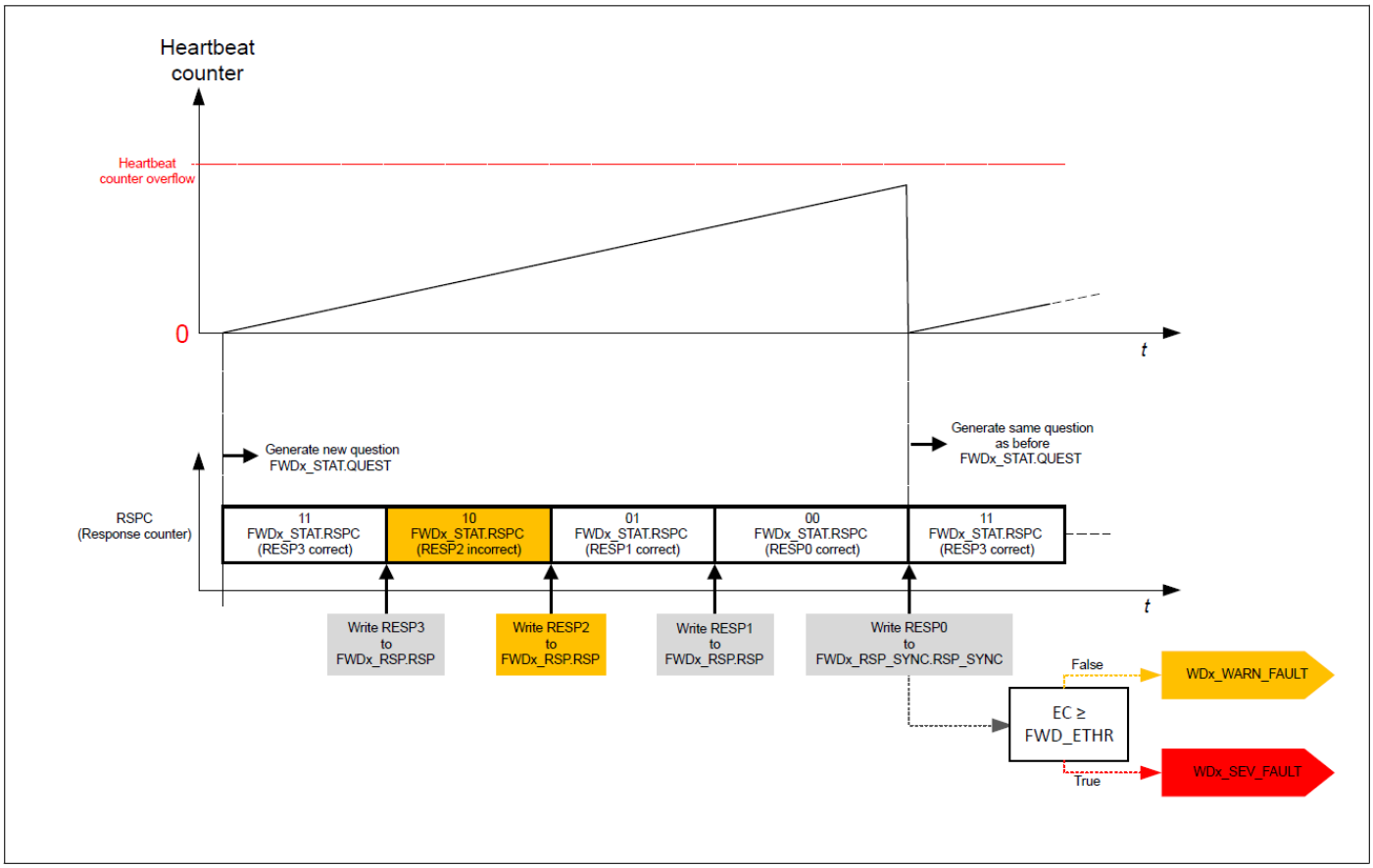


图 42　　FWD：错误响应 (RESP2) 时序图

(x = 1, 2)

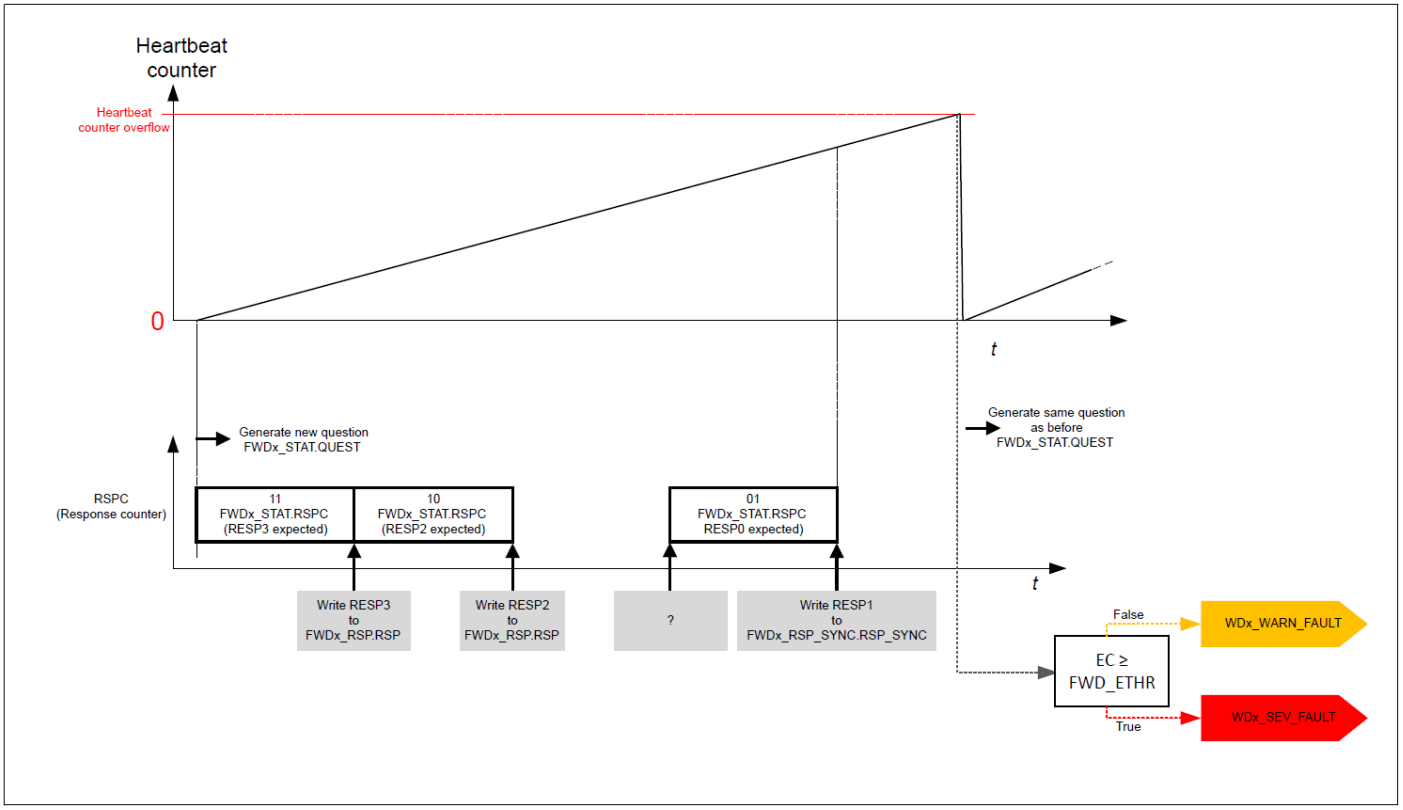


图 43　　缺失响应时序图

(x = 1, 2)

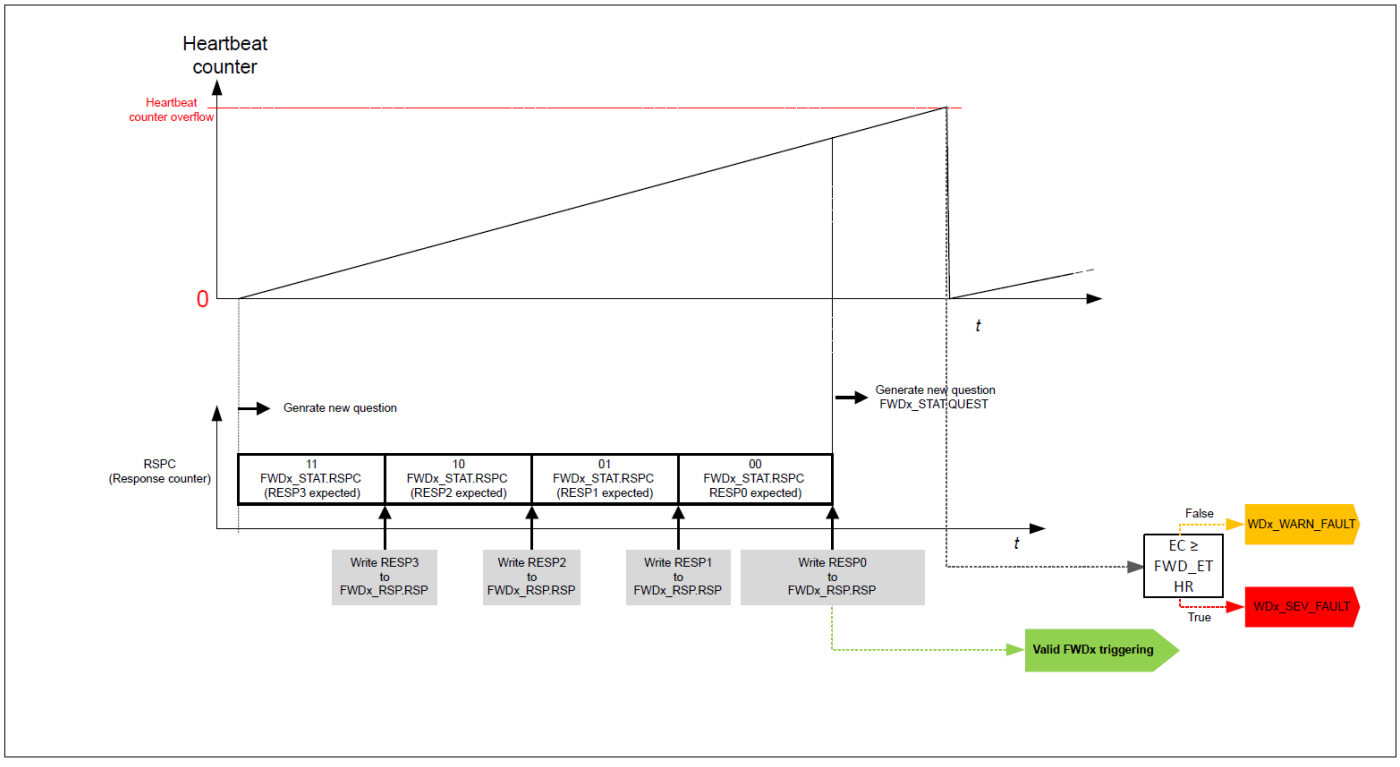


图 44　　缺失同步时序图

(x = 1, 2)

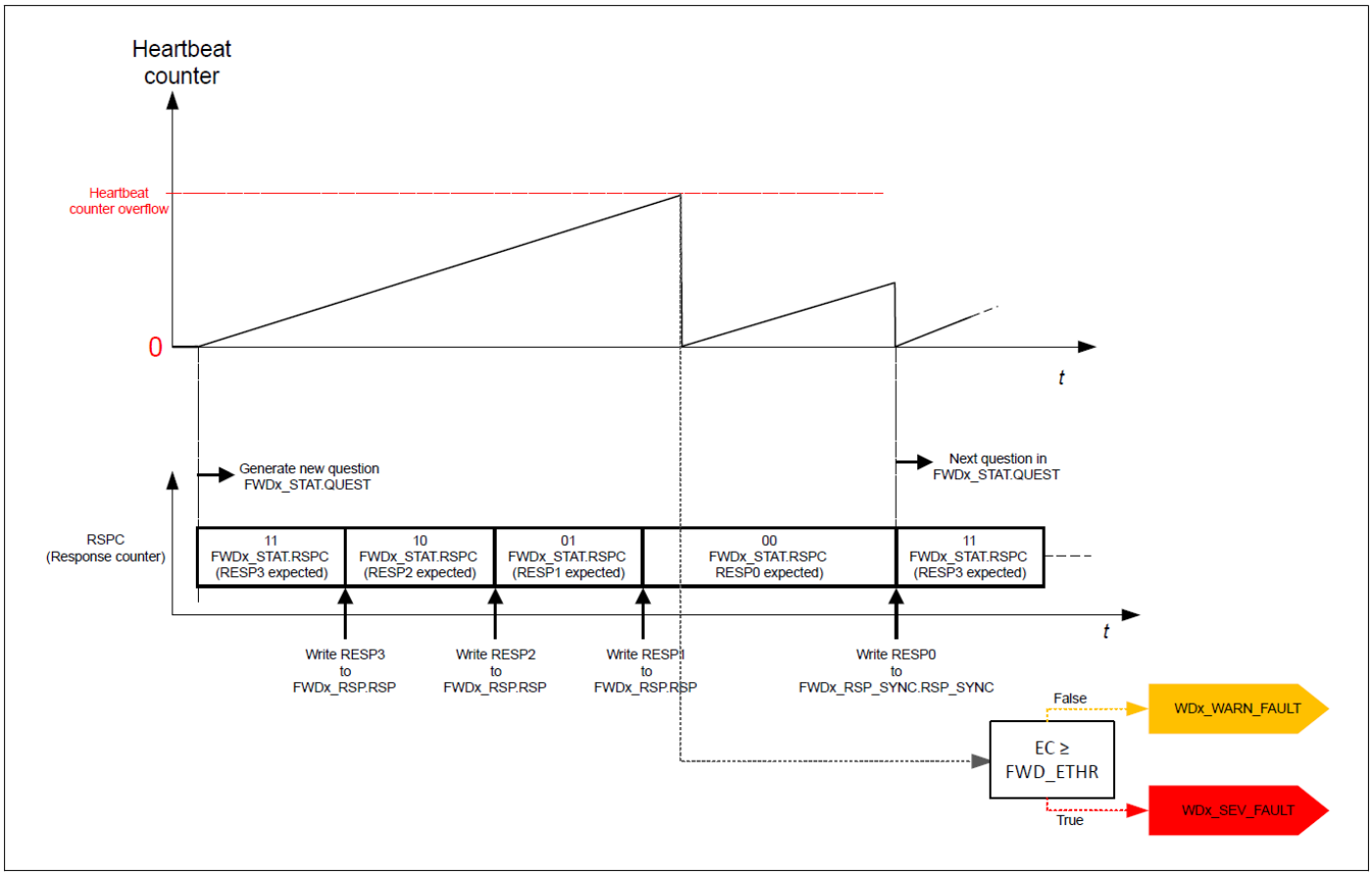


图 45　　心跳计数器溢出

(x = 1, 2)

10.1.3.1.2　　功能看门狗错误计数器溢出

如果器件检测到有效 FWDx 触发，则当 **FWDx_STAT** 寄存器中 ECNT 位字段值大于 0 时会减 1。
如果器件检测到无效 FWDx 触发，则会将 **FWDx_STAT** 寄存器中的 ECNT 位字段值加 2。
如果 ECNT 位字段的值达到或超过配置的 FWD 错误计数器阈值 **WDx_PW_CFG1.FWD_ETHR** 的值，器件将执行以下操作（请参阅故障反应）：

- 生成看门狗严重故障 WDx_SEV_FAULT，参见章节 9
- 设置对应的错误位（寄存器 **INIT_ERR_APPx.FWDy_EC**），该错误位可通过 SPI 清零
- 清除 FWD 错误计数器

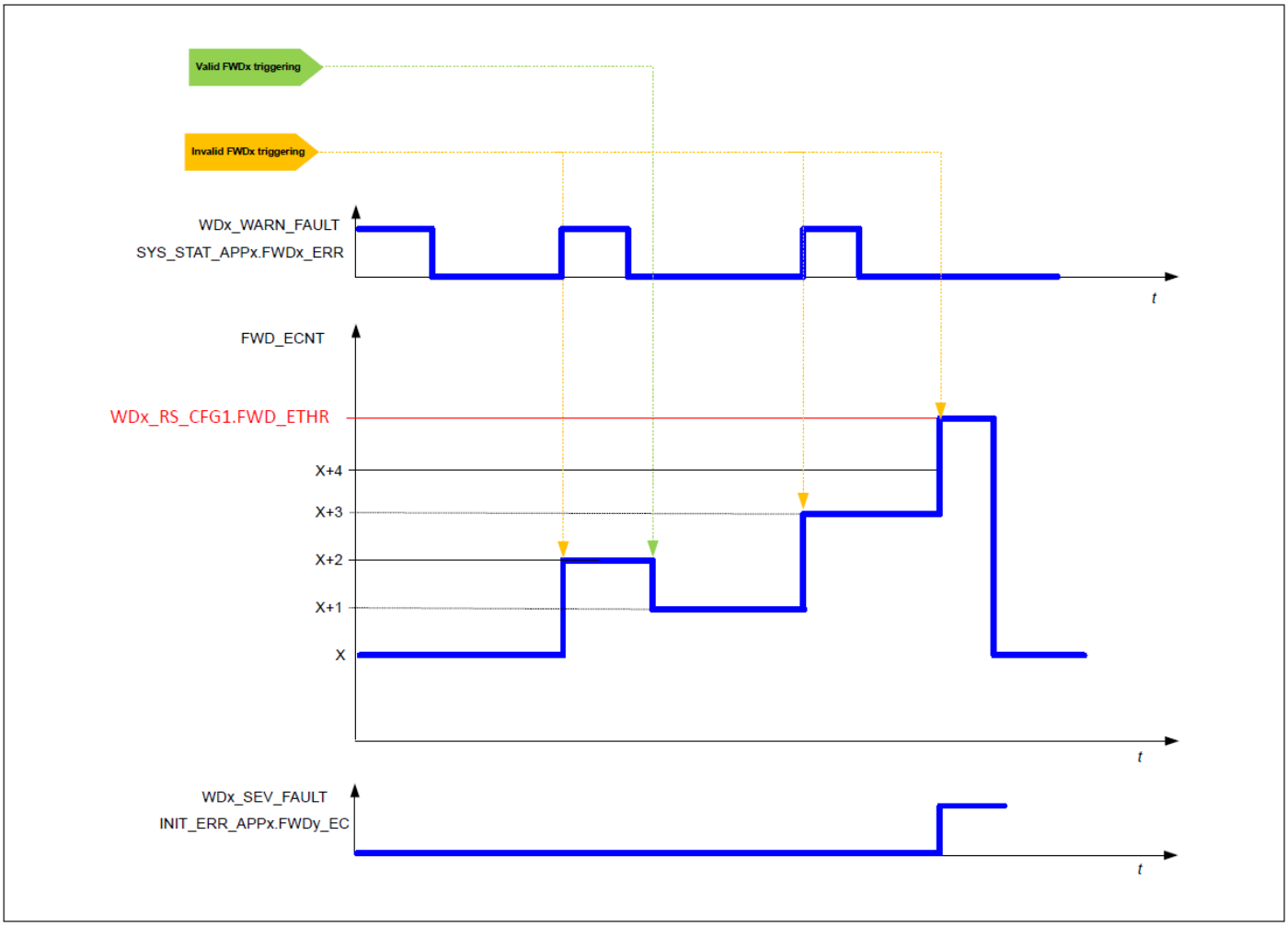


图 46　　错误计数器（ECNT）溢出时序图

(x = 1, 2)

(y = 1, 2)

10.2　　错误监测（ERR MON）

10.2.1　　介绍

错误监测（ERR MON）功能是一种安全机制，用于监控应用微控制器的安全管理单元（SMU）。它有三个独立的 ERRx 输入。如果其中一个错误监测器检测到其输入信号频率超出有效频率范围，则器件会做出相应的反应（参见故障反应）。

(x=0, 1, 2)

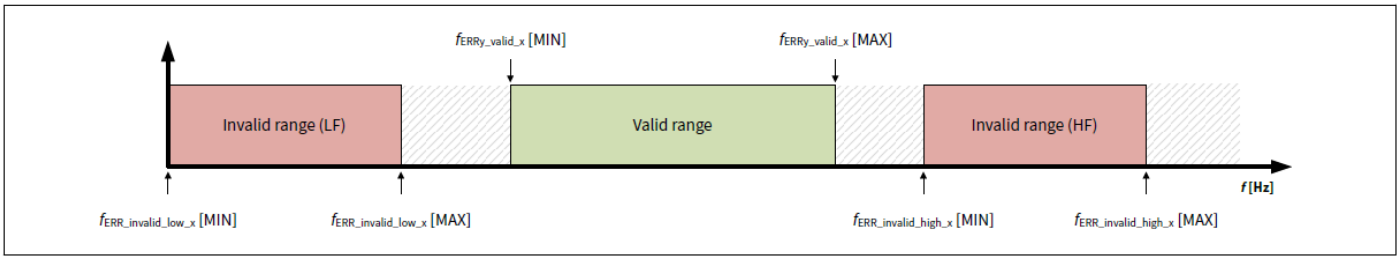


图 47　　施加于 ERRy 监测输入端的切换频率信号

(x = LF; HF)

(y = 0; 1; 2)

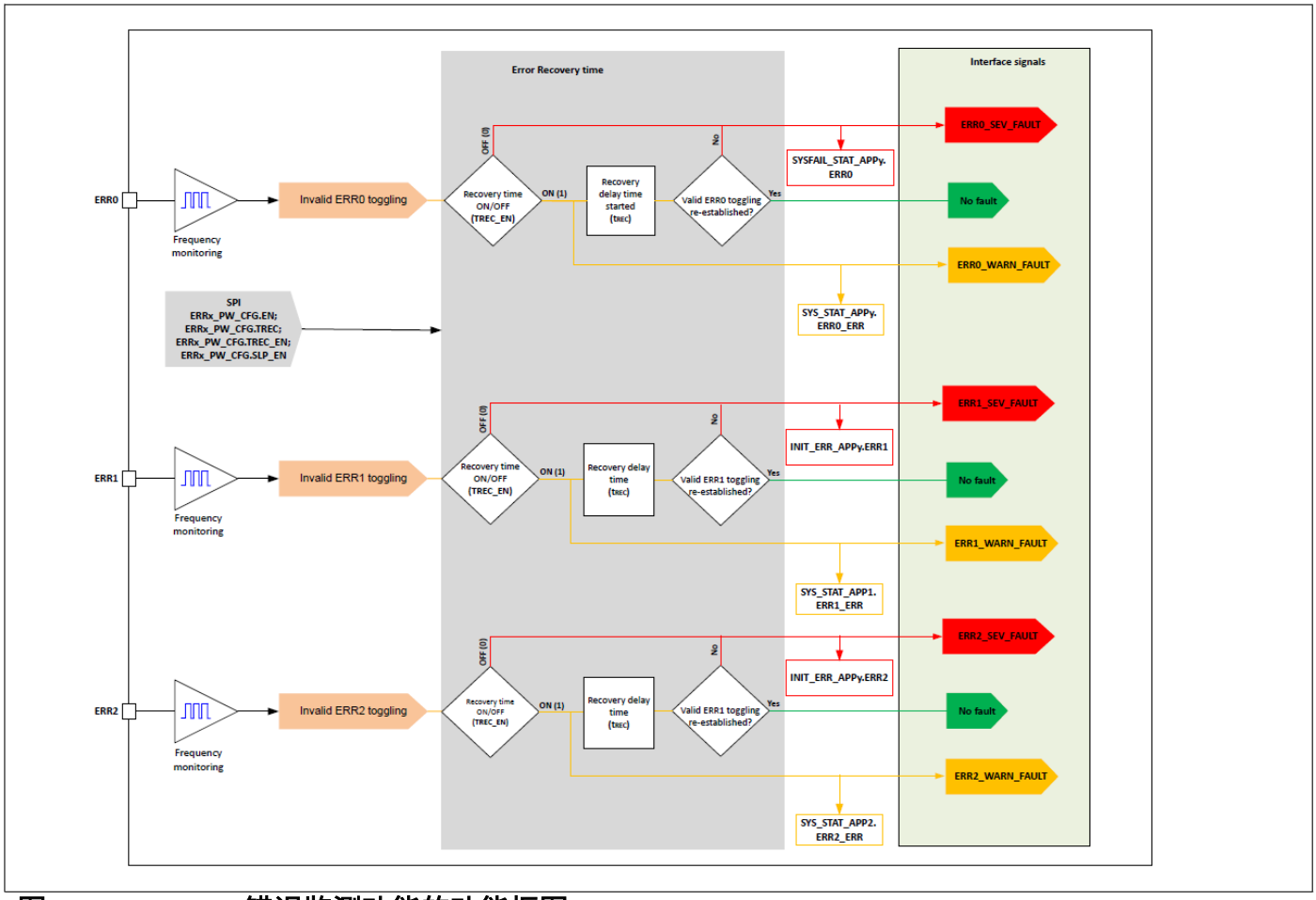


图 48　　错误监测功能的功能框图

(x = 1, 2, 3; y = 1, 2)

器件提供以下错误监测通道：

- ERR0 引脚的 ERR MON0
- ERR1 引脚的 ERR MON1
- ERR2 引脚的 ERR MON2

10.2.2　　功能描述：错误监测（ERR MON）

10.2.2.1　　错误监测初始化

错误监测模块可以使用低频率或高频率正确触发：

- 有效输入信号频率低（$f_{ERRx\_valid\_LOW}$）
- 有效输入信号频率高（$f_{ERRx\_valid\_HIGH}$）

当在 ERRx 施加错误监测信号时，器件会忽略信号的前六个边沿，以使外部信号稳定。接下来，器件会自动检测频率范围是否在允许的范围内。如果无法检测到正确的频率范围，器件会做出相应的反应（参见故障反应）。运行时，ERRx 模块持续监控施加的信号。每当 ERRx 模块遇到复位条件并且需要重新初始化时，总是执行此过程。复位条件是：

- RESOUT 显示复位
- 从 POWERDOWN 开始
- 禁用 QUC 或 BUCKCORE 后从 FAILSAFE、STANDBY 或 SLEEP 恢复
- 在 **ERRx_RS_CFG.EN** = 1 和 **ERRx_RS_CFG.SLP_EN** = 0 时退出 SLEEP

(x = 0; 1; 2)

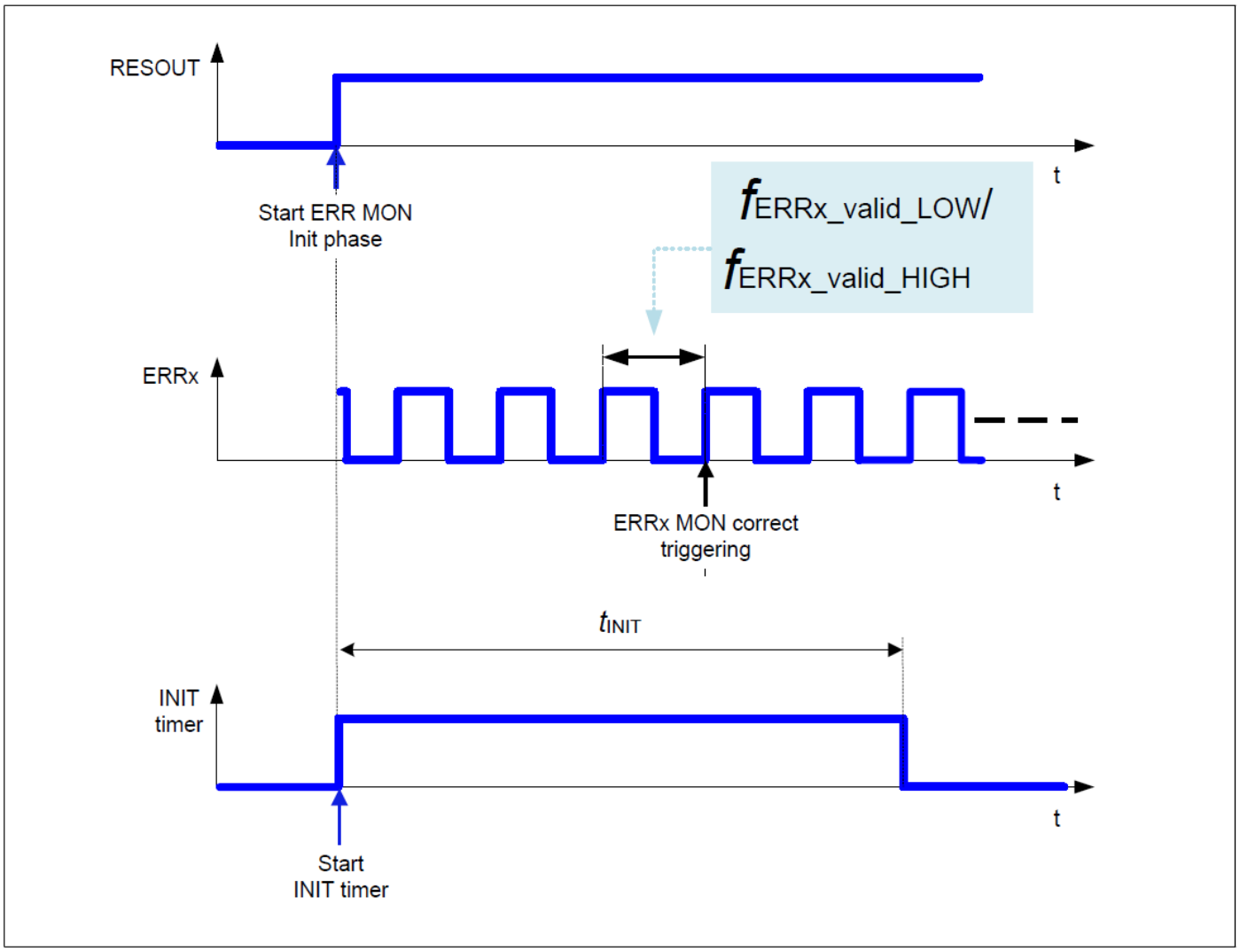


图 49　　错误监测正确触发

(x = 0; 1; 2)

10.2.2.2　　错误监测配置

每个错误监测通道可以在寄存器位 **ERRx_PW_CFG.EN** 中独立激活或关闭。

通过 SPI 重新激活错误监测通道后，器件在重新启用 $t_{ERR\_to\_ren}$ 后开始执行重新激活超时。当器件检测到 ERRx 引脚上的边沿时，它会停止 $t_{ERR\_to\_ren}$。如果 $t_{ERR\_to\_ren}$ 超时而未检测到边沿，则会抛出严重故障。

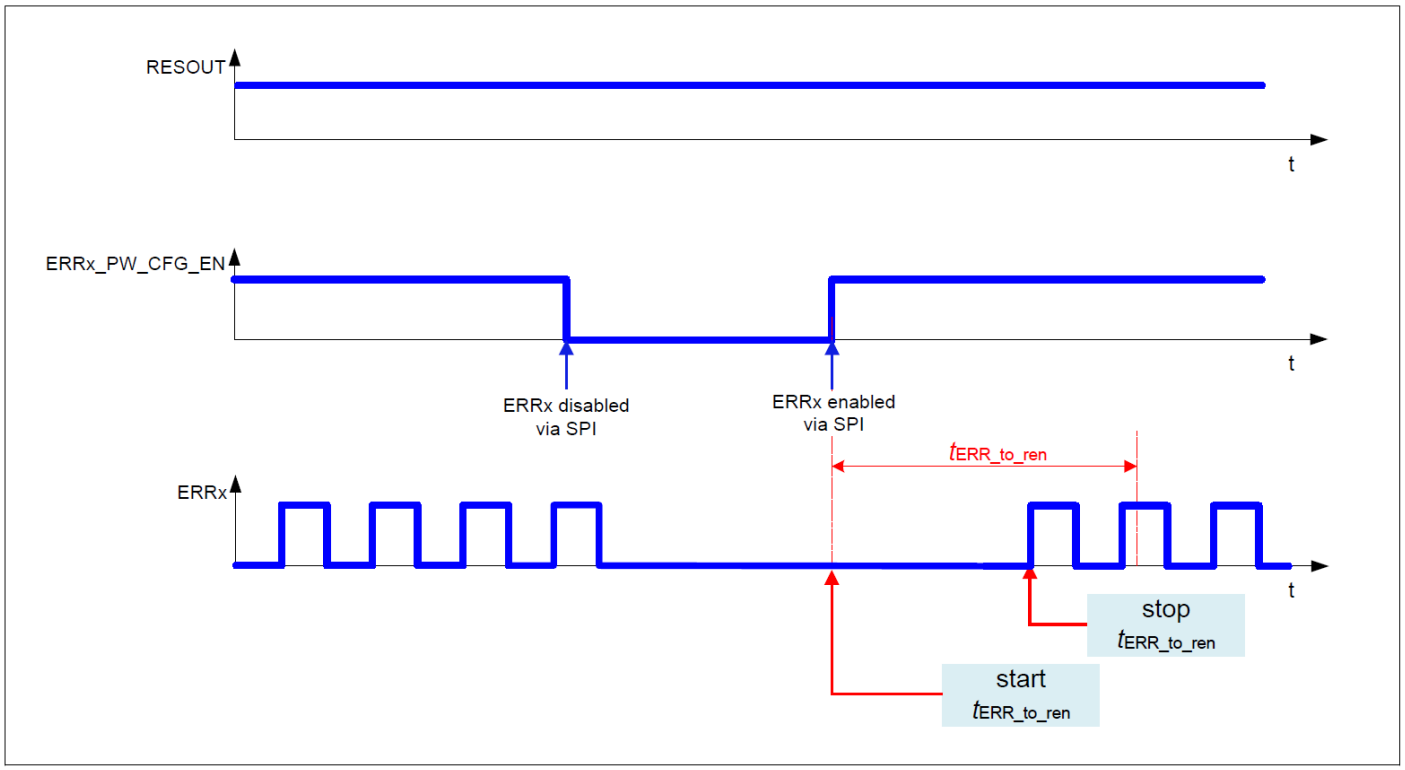


图 50　　ERRx 重新激活超时

(x = 0; 1; 2)

可以通过写入相应的 **ERRx_PW_CFG.EN** 位来独立启用和禁用错误监测通道。此外，每个错误监测通道都可以通过相应的 **ERRx_PW_CFG.SLP_EN** 位配置为在 SLEEP 状态下保持激活状态。如果错误监测通道未配置为在 SLEEP 状态下保持激活状态，并且在进入 SLEEP 状态之前已经运行，则该功能将在恢复到 WAKE 状态时重新启用，并启动重新激活超时时间 t_{ERR_to}。

这提供了额外的时间预算，用于再次应用错误监测信号或禁用该功能。如果在 t_{ERR_to} 时间内未应用错误监测，则会发出 ERRx_SEV_FAULT（参见中断功能（INT）和复位功能（RESOUT））。ERR 超时是一个全局计时器，仅当所有 ERRx 通道都被禁用，或者所有启用的 ERRx 通道在 t_{ERR_to} 内得到正确服务时才会停止。

注释： *ERR2 仅在启用 REDUCED OPERATION 时才能使用 (**REDOP_RS_CFG1.EN = 1**)。*

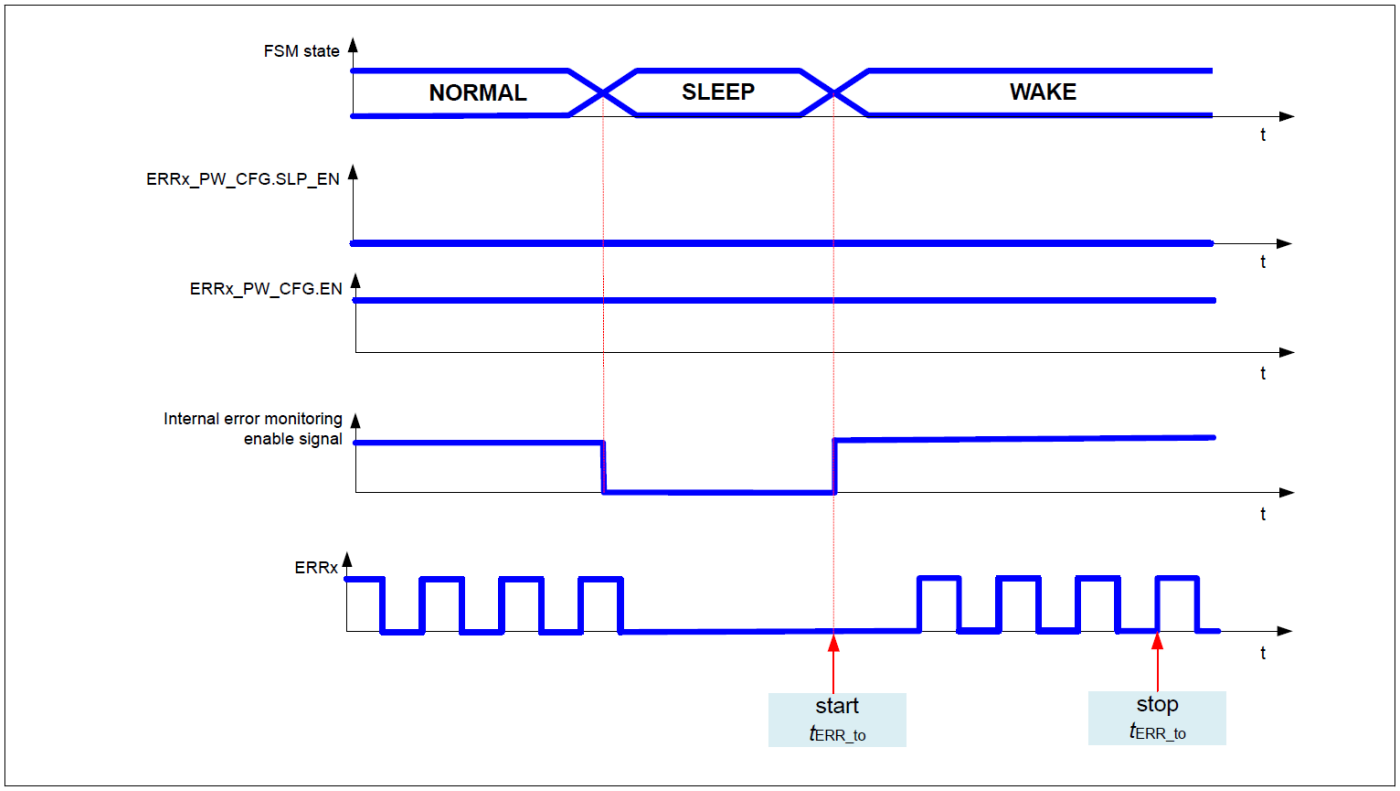


图 51　　ERRx 从 SLEEP 状态重新激活超时

(x = 0; 1; 2;
y = 1; 2)

10.2.2.3　　错误监测恢复计时器

每个错误监测通道都提供一个恢复计时器。当检测到无效的 ERRx 切换信号周期时，相应的恢复计时器会给应用一些时间来恢复并重新生成有效的错误频率。

每个错误监测通道的恢复计时器可以在寄存器位 **ERRx_PW_CFG.TREC_EN** 中独立激活或关闭。

对于已激活的恢复计时器，恢复时间 t_{REC} 的持续时间可以在位字段 **ERRx_PW_CFG.TREC** 中配置。

10.2.2.4　　无效错误切换

如果满足以下任一条件，则器件检测到“**无效 ERRx 切换**”：

- ERR信号停止切换，保持"低电平"或"高电平"
- ERR 信号开始以过高的频率切换（$f_{ERR\_invalid\_high\_x}$）
- ERR 信号开始以过低的频率切换（$f_{ERR\_invalid\_low\_x}$）　（x = LF；HF）

恢复时间禁用

当检测到无效 ERRx 触发时，器件执行以下操作：

- 生成错误监测严重故障 ERRx_SEV_FAULT，请参阅故障反应
- 设置相应的故障位（**SYSFAIL_STAT_APPy.ERR0, INIT_ERR_APPy.ERRx**）

恢复时间启用

当检测到无效 ERRx 触发时，器件执行以下操作：

- 生成错误监测警告故障 ERRx_WARN_FAULT，请参阅故障反应
- 设置相应的故障位（**SYS_STAT_APPy.ERRx_ERR**），该故障位可通过 SPI 清除

- 启动恢复计时器
- 如果在 t_{REC} 过期之前已重新建立正确信号，则计时器停止运行，不再执行任何操作。
- 如果在恢复时间 t_{REC} 过期后，且未及时重新建立有效的错误信号，则生成错误监测严重故障 ERRx_SEV_FAULT，请参阅故障反应
- 设置相应的故障位（**SYSFAIL_STAT_APPy.ERR0, INIT_ERR_APPy.ERRx**），该故障位可通过 SPI 清除

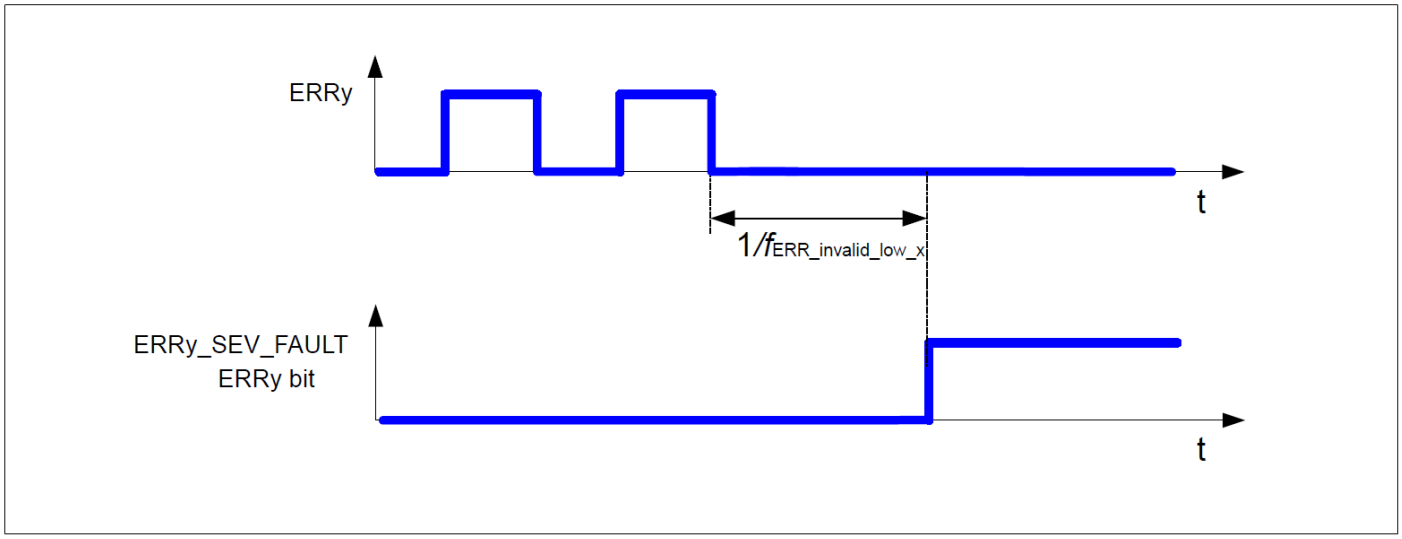


图 52　　ERRy 捕获频率过低或停止切换（恢复时间禁用）

(x = LF; HF)
(y = 0; 1; 2)

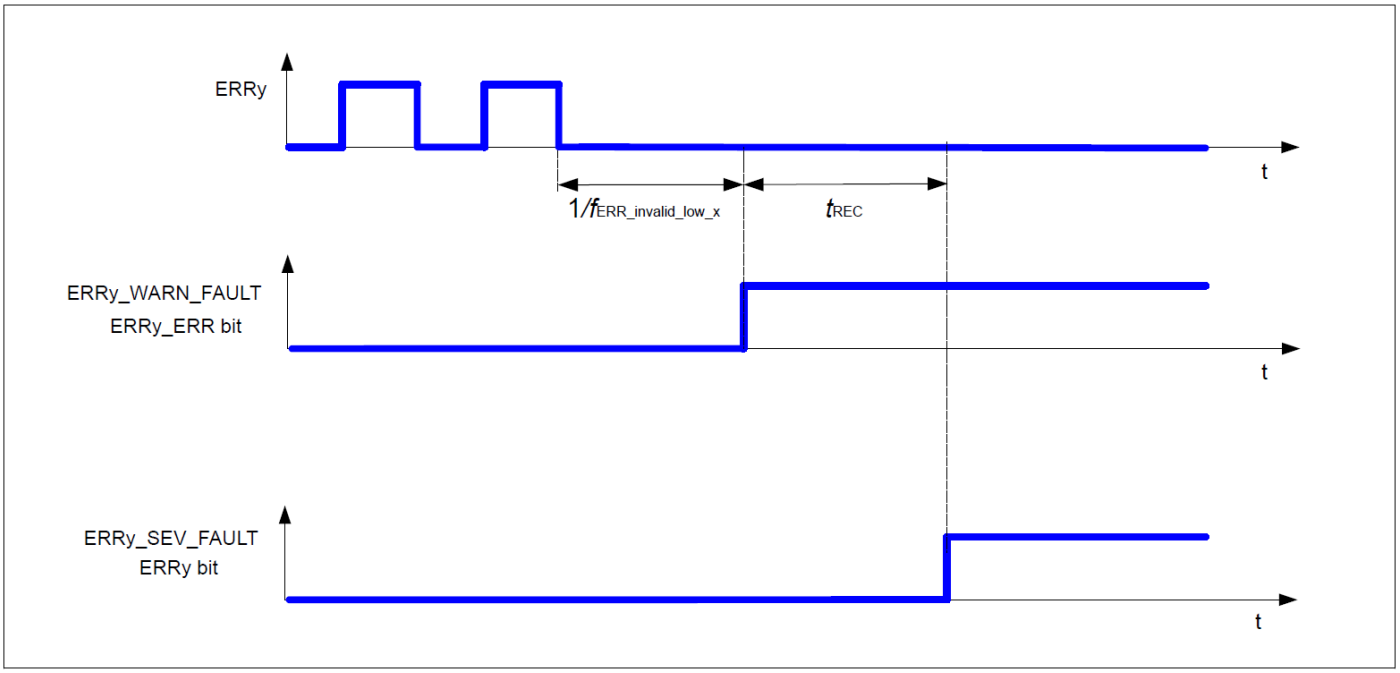


图 53　　ERRy 捕获频率过低或停止切换（恢复时间启用）

(x = LF; HF)
(y = 0; 1; 2)

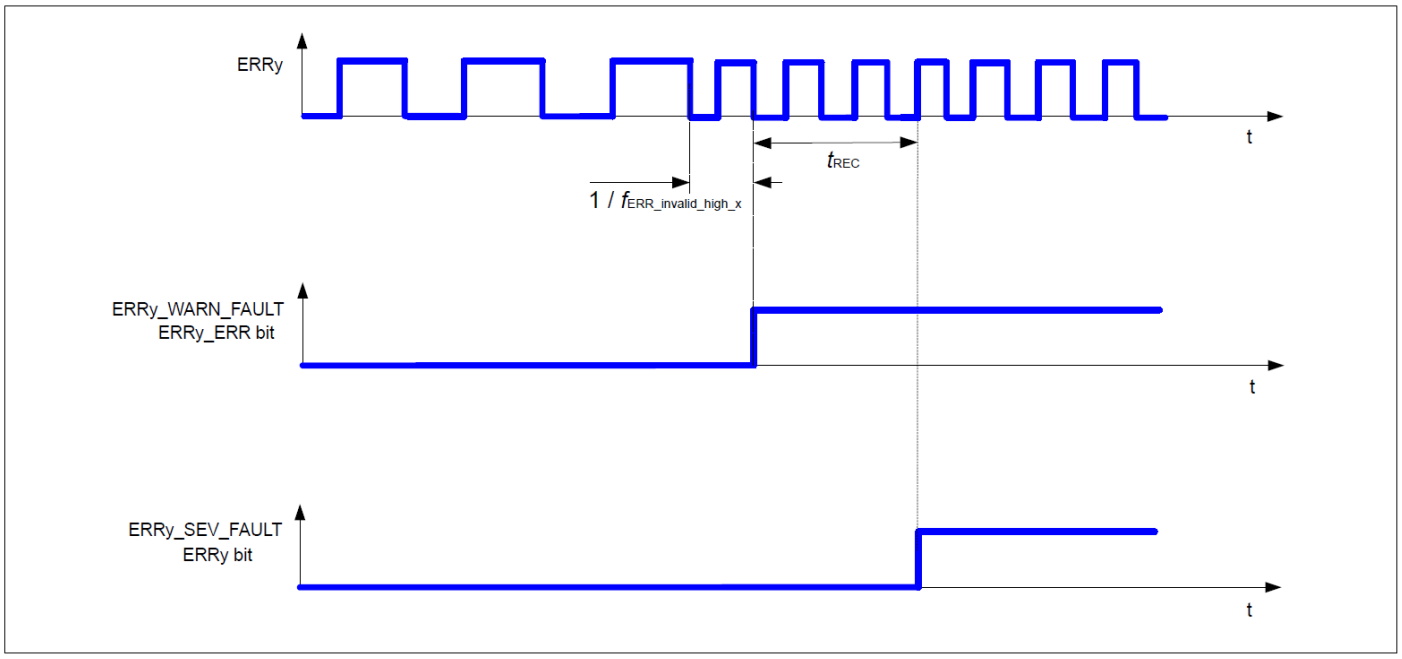


图 54　　ERRy 捕获频率过高（恢复时间启用）

(x = LF; HF)
(y = 0; 1; 2)

10.2.3　电气特性：错误监测（ERR MON）

表 36　　电气特性：错误监测（ERR MON）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRx pin valid "high" voltage	V_{ERRx_HIGH}	2	–	V_{QUC}	V	V_{ERRx} increasing; $V_{QUC} \geq V_{QUC}$[Min.]	DS-1624
ERRx pin valid "low" voltage	V_{ERRx_LOW}	0	–	0.8	V	V_{ERRx} decreasing	DS-1625
ERRx pin hysteresis	V_{ERRx_HYST}	–	200	–	mV	$V_{QUC} = V_{QUC}$[Typ.]	DS-1627
ERRx pin pull-down current	I_{ERRx}	–	135	330	µA	$V_{ERRx} = V_{QUC}$	DS-1628
ERRx pin input capacitance	C_{ERRx}	–	4	15	pF	1)	DS-1629
Valid ERRx input signal frequency low	$f_{ERRx\_valid\_LOW}$	10	–	45	kHz	–	DS-1630
Valid ERRx input signal frequency high	$f_{ERRx\_valid\_HIGH}$	1000	–	2000	kHz	–	DS-1631
ERRx invalid input signal - too low frequency LF	$f_{ERR\_invalid\_low\_LF}$	0	–	5	kHz	1)	DS-1632
ERRx invalid input signal - too high frequency LF	$f_{ERR\_invalid\_high\_LF}$	96.2	–	10000	kHz	1)	DS-1633

（表格续下页……）

表 36　（续）电气特性：错误监测（ERR MON）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRx invalid input signal - too low frequency HF	$f_{ERR\_invalid\_low\_HF}$	0	–	0.5	MHz	1)	DS-1634
ERRx invalid input signal - too high frequency HF	$f_{ERR\_invalid\_high\_HF}$	4	–	10	MHz	1)	DS-1635
Reactivation timeout	t_{ERR_to}	9	–	11	ms	After SLEEP with RESOUT=1 and ERRx_RS_CFG.EN=1 and ERRx_RS_CFG.SLP_EN=0 1)	DS-1636
Reactivation timeout after reenabling	$t_{ERR\_to\_ren}$	90	100	110	µs	After reenabling via SPI 1)	DS-1637
ERRx recovery time	t_{REC}	0.9 · t	t	1.1 · t	ms	t configurable to be 1 ms, 2.5 ms, 5 ms, 10 ms; Configuration done via SPI 1)	DS-1998

1)　未经过生产测试，由设计指定

10.3　电压监测

10.3.1　介绍

电压监测（VMON）功能是一种安全机制，用于监控内部和外部电源轨。如果监测电压轨超出规定的工作范围，则器件会做出相应的反应。

电压监测模块提供以下电压监测通道：

- 电池电压监测
- 每个内部调节器或电源轨的内部电压监测
- 两个外部电压监测通道

每当调节器启用时，相应电压轨的电压监测就会被激活。

仅当调节器逐渐升高时，欠压才会被忽略，直到输出电压处于其欠压和过压阈值定义的监测范围内。

接地短路检测在升压过程中仍然保持激活。

该器件还集成了操作所有功能所需的内部电压源和偏置电流，包括调节器、监测和数字逻辑。对这些内部电源进行监控，以确保器件正常运行。

器件中受监控的内部电源包括：

- 内部电源电压
- 偏置电流
- 带隙到带隙变化

注释：这些电压和电流源不能直接从器件外部获得

10.3.2 电池电压监测

Vs 引脚上的电压受到监控，以保护器件免受意外过压的影响。
如果 Vs 引脚上的电压 (V_{VS}) 超过过压阈值 V_{VS_OV}，则器件执行以下操作：

- 生成 VBAT 监测严重故障 VBAT_SEV_FAULT，请参阅章节 9
- 设置相应的故障位 INTSUP_STAT_APPx.VBAT_OV，该故障位可通过 SPI 清除。

10.3.3 内部电压监测

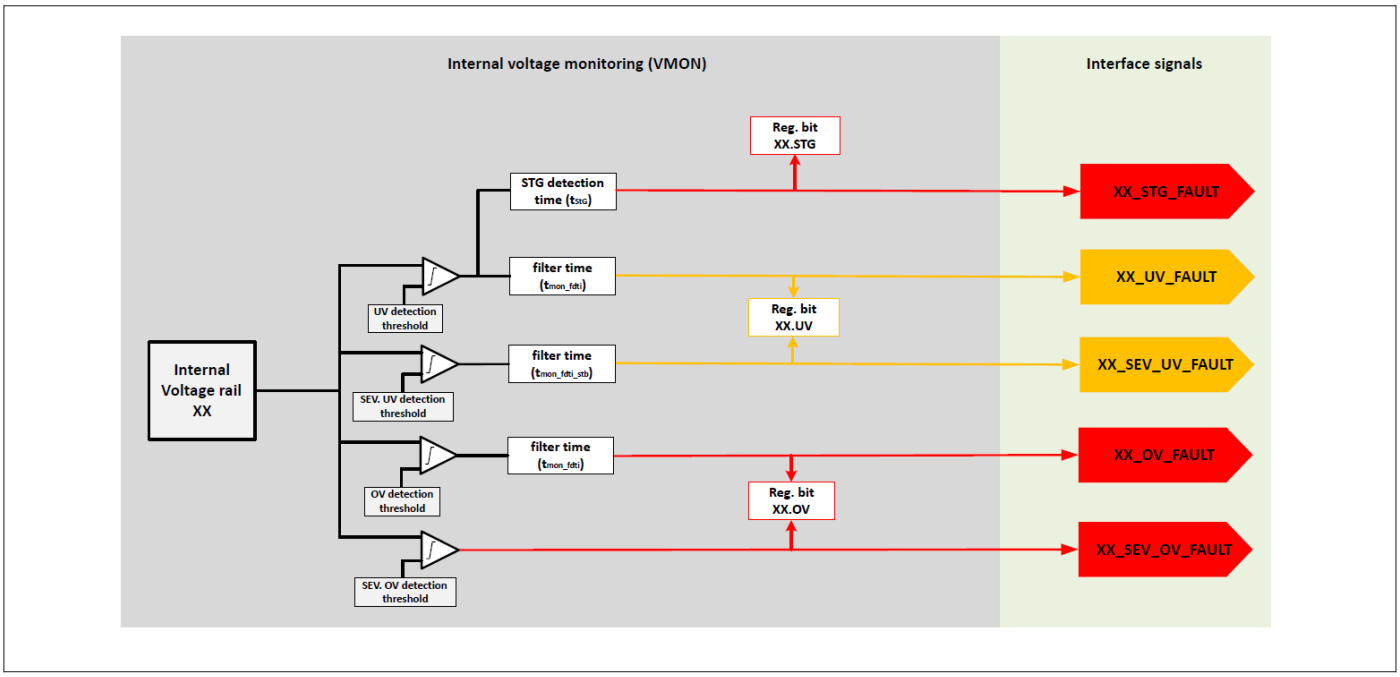


图 55 内部电压监测功能框图

下表显示了每个调节器轨对应的监测类型（XX）

Monitoring rail (XX)	severe OV detection	OV detection	UV detection	severe UV Detection	Short to Ground
BUCK PREREG	x	x	x	x (BOOST not used) *	x
BUCKIF	x	x	x		x
BUCKCORE	x	x	x		x
BOOST		x	x	x (BOOST used) *	x
QUC		x	x		x
QCO		x	x		x
QVR		x	x		x
QST	x	x	x		x
QST (STANDBY)	x			x	x
Int. Supply	x	x	x		x
BG12		x	x		

*在以下情况下，会对BSTFB 引脚进行严重欠压监测：

- *如果BOOST 已安装并且已开启，它被视为BOOST 严重欠压，并在SPI 位字段STG_STAT_APPx.BOOST 中指示*
- *如果BOOST 未安装或在睡眠状态下关闭，则视为BUCK PREREG 严重欠压，并在SPI 位字段 STG_STAT_APPx.PREREG 中指示*

过压检测：

如果内部电源轨 XX 的输出电压超过定义的过压阈值 V_{XX_OV}，且持续时间长于监测反应时间 t_{mon_fdti}，则器件将执行以下操作：

- 生成内部过压故障 XX_OV_FAULT（请参阅检测到故障时的反应）
- 设置相应的故障位（寄存器 **OV_STAT_APPx.XX**），这些故障位只能在电压恢复到正常工作范围后通过 SPI 清除。

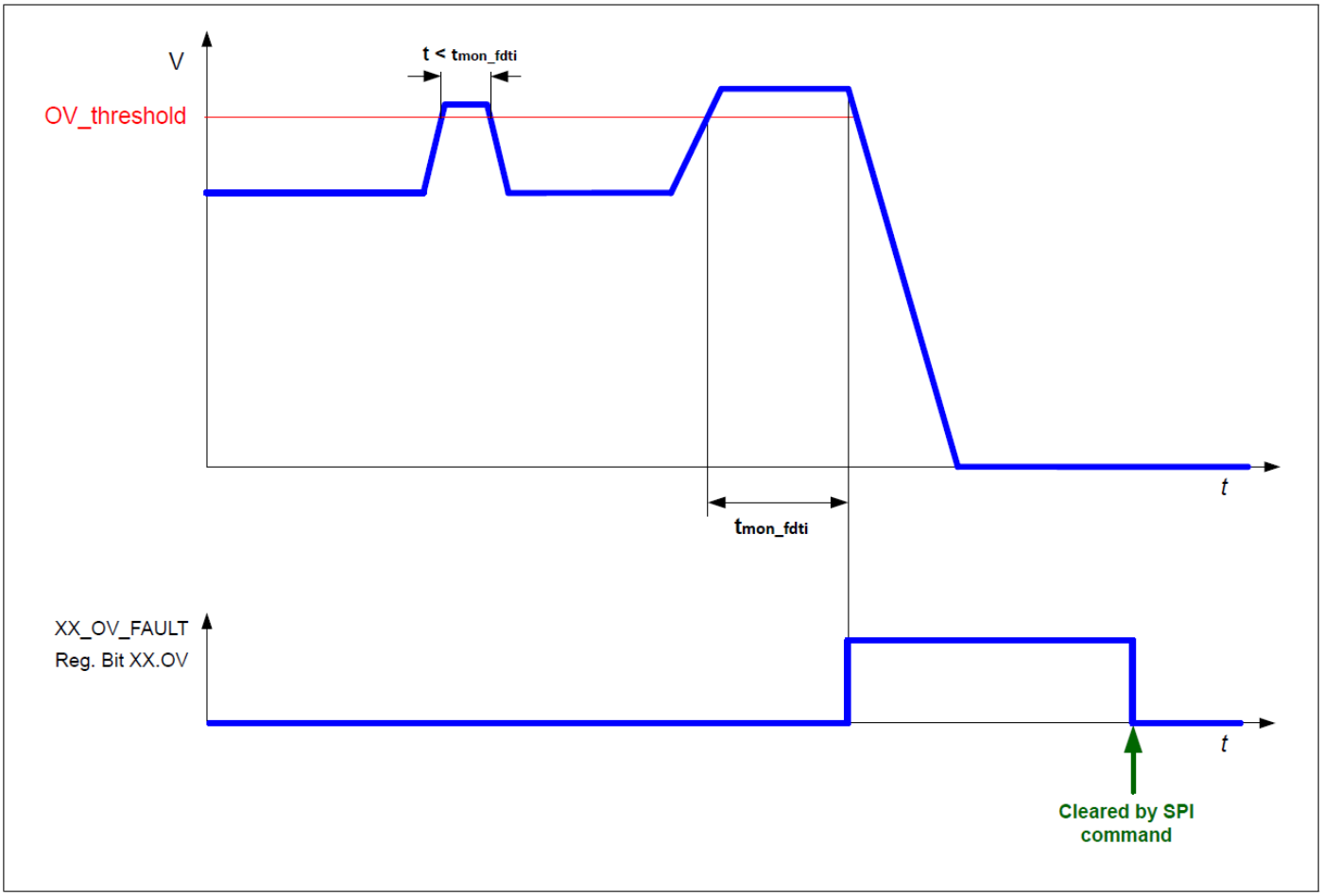


图 56　　过压检测时序图

严重过压检测：

如果内部电源轨 XX 的输出电压迅速升高并达到严重过压阈值 $V_{XX\_SEV\_OV}$，

该器件立即关闭相应的调节器。一般来说，严重的过压反应与过压检测相同，不同之处在于，与过压相比，阈值设置较高，并且不应用滤波时间。

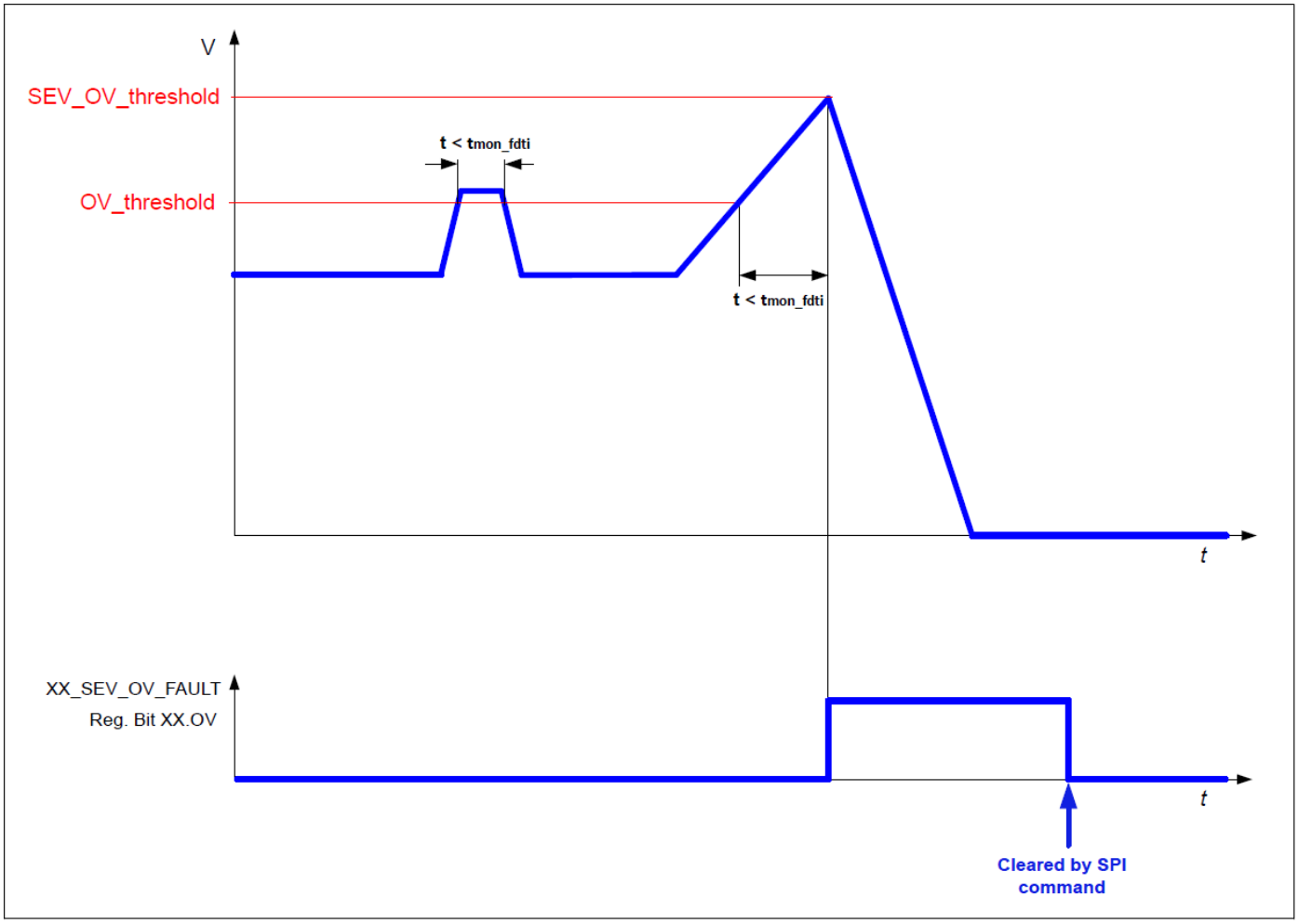


图 57　　严重过压检测时序图

如果器件进入 STANDBY 状态，并且备用调节器 (QST) 的输出电压下降到低于严重欠压阈值 $V_{QST_SEV_UV}$的时间长于备用监测反应时间$t_{mon_fdti_stb}$，
器件执行以下操作：

- 生成内部欠压故障 QST_SEV_UV_FAULT（请参阅检测到故障时的反应）
- 设置相应的故障位（寄存器 **UV_STAT_APPx.XX**），这些故障位只能在电压恢复到正常工作范围后通过 SPI 清除。

接地短路检测：

如果内部电源轨 XX 的输出电压下降到低于定义的欠压阈值 V_{XX_UV} 的时间长于接地短路检测时间 t_{STG}，
器件执行以下操作：

- 产生接地内部短路故障 XX_STG_FAULT，参见章节 9
- 设置相应的故障位（寄存器 **STG_STAT_APPx.XX**），该故障位只能在电压恢复到正常工作范围后通过 SPI 清除。

如果在开关周期之间引脚 VBSTI 处的电压没有恢复到阈值 VBSTI_UV 以上，则器件会检测到 BOOST 调节器开关节点接地短路 (StG)。

如果电压 V_{QST} 下降到低于欠压阈值 V_{QST_UV} 的时间长于 QST 接地短路检测时间 t_{StG_QST}，则器件检测到引脚 QST 处存在接地短路 (StG)。

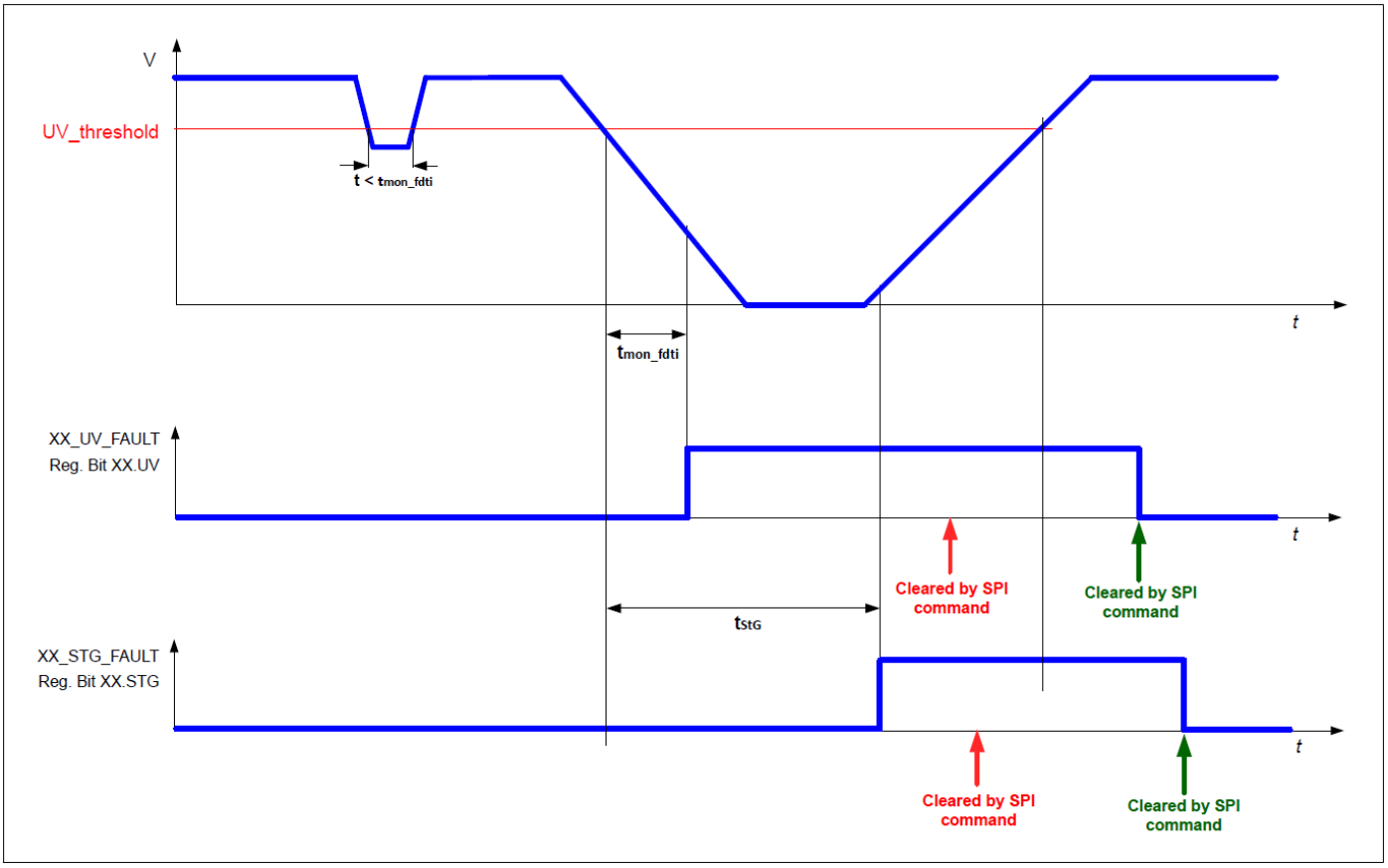


图 58　　UV 和 STG 检测时序图

10.3.4　　电气特性：监测功能

表 37　　电气特性：监测功能

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage monitoring							
Vbat overvoltage shutdown threshold	V_{VS_OV}	49	52	55	V	–	DS-1355
Severe overvoltage threshold Pre-reg	$V_{R1FB\_SEV\_OV}$	6.66	6.8	6.94	V	–	DS-1356
5V5 overvoltage threshold Pre-reg	$V_{R1FB\_5V5\_OV}$	6.15	6.3	6.43	V	–	DS-1357
4V0 overvoltage threshold Pre-reg	$V_{R1FB\_4V0\_OV}$	5.10	5.2	5.3	V	–	DS-1358

（表格续下页……）

表 37　　（续）电气特性：监测功能

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Severe overvoltage threshold BUCK CORE	$V_{R3FB\_sev\_OV}$	y * 1.19	–	y * 1.56	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value); y = 1.15 V for x = 33	DS-2043
Overvoltage threshold BUCK CORE	V_{R3FBH_OV}	y * 1.068	y * 1.09	y * 1.112	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value BUCK_CORE_PW_VSEL); y = 1.15 V for x = 33	DS-1359
Overvoltage hysterese BUCK CORE	$V_{R3FBH\_OV\_HYS}$	5	15	25	mV	–	DS-1360
Severe overvoltage threshold BUCK IF	$V_{R4FB\_SEV\_OV}$	2.15	2.2	2.25	V	–	DS-1362
Overvoltage threshold BUCK IF	V_{R4FB_OV}	1.908	1.94	1.98	V	–	DS-1364
Overvoltage threshold BOOST	V_{BSTFB_OV}	6.37	6.5	6.63	V	–	DS-1365
Overvoltage hysteresis BOOST	$V_{BSTFB\_OV\_HYS}$	35	–	115	mV	–	DS-1366
Overvoltage threshold QUC	V_{QUC_OV}	3.49	3.56	3.63	V	–	DS-1369
Overvoltage hysteresis QUC	$V_{QUC\_OV\_HYS}$	20	–	70	mV	–	DS-1370
Overvoltage threshold QCO	V_{QCO_OV}	5.3	5.4	5.5	V	–	DS-1371
Overvoltage hysteresis QCO	$V_{QCO\_OV\_HYS}$	25	–	102	mV	–	DS-2153
Severe overvoltage threshold QST	$V_{QST\_SEV\_OV}$	5.95	6.25	6.5	V	–	DS-1373
Overvoltage threshold QST	V_{QST_OV}	3.49	3.56	3.63	V	–	DS-1375
Overvoltage hysteresis QST	$V_{QST\_OV\_HYS}$	20	–	70	mV	–	DS-1376
Overvoltage threshold QVR	V_{QVR_OV}	5.24	5.35	5.46	V	–	DS-1378
Overvoltage hysterese QVR	$V_{QVR\_OV\_HYS}$	30	–	100	mV	–	DS-1379

（表格续下页.....）

表 37　　（续）电气特性：监测功能

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage monitoring							
Undervoltage threshold Pre-reg	V_{R1FB_UV}	2.59	2.65	2.71	V	–	DS-1380
Undervoltage hysteresis Pre-reg	$V_{R1FB\_UV\_HYS}$	15	–	50	mV	–	DS-1381
Undervoltage threshold BUCK CORE	V_{R3FBH_UV}	y * 0.891	y * 0.91	y * 0.929	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value BUCK_CORE_PW_VSEL); y = 1.15 V for x = 33	DS-1382
Undervoltage hysterese BUCK CORE	$V_{R3FBH\_UV\_HYS}$	3	15	25	mV	–	DS-1383
Undervoltage threshold BUCK IF	V_{R4FB_UV}	1.58	1.62	1.66	V	–	DS-1384
Undervoltage hysteresis BUCK IF	$V_{R4FB\_UV\_HYS}$	9	–	30	mV	–	DS-1386
Undervoltage threshold BOOST	V_{BSTFB_UV}	4.9	5	5.10	V	–	DS-1388
Severe undervoltage threshold BOOST	$V_{BSTFB\_SEV\_UV}$	1.96	2	2.04	V	If BOOST is not used, it is interpreted as BUCK PREREG severe undervoltage threshold	DS-2161
Undervoltage hysteresis BOOST	$V_{BSTFB\_UV\_HYS}$	30	–	90	mV	–	DS-1389
Boost short to ground threshold	V_{BSTI_UV}	1.84	2.0	2.16	V	V_{BSTI} decreasing	DS-1955
Boost short to ground threshold hysteresis	$V_{BSTI\_UV\_HYS}$	13[1)]	25	37	mV	V_{BSTI} increasing	DS-1956
Undervoltage threshold QCO	V_{QCO_UV}	4.5	4.6	4.7	V	–	DS-1390
Undervoltage hysteresis QCO	$V_{QCO\_UV\_HYS}$	25	–	80	mV	–	DS-1391
Undervoltage threshold QUC	V_{QUC_UV}	2.9	2.97	3.036	V	–	DS-1394

（表格续下页……）

表 37 （续）电气特性：监测功能

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage hysteresis QUC	$V_{QUC\_UV\_HYS}$	15	–	55	mV	–	DS-1395
Undervoltage threshold QVR	V_{QVR_UV}	4.5	4.6	4.7	V	–	DS-1396
Undervoltage hysterese QVR	$V_{QVR\_UV\_HYS}$	25	–	80	mV	–	DS-1397
Undervoltage threshold QST	V_{QST_UV}	2.83	2.9	2.97	V	–	DS-1399
Undervoltage hysteresis QST	$V_{QST\_UV\_HYS}$	15	–	55	mV	–	DS-1401
Severe undervoltage threshold QST	$V_{QST\_SEV\_UV}$	2.6	2.72	2.78	V	–	DS-2007
Internal Supply undervoltage threshold	$V_{int\_sup\_UV}$	4.4	4.5	4.6	V	V_{QIS} decreasing	DS-1966
Internal Supply overvoltage threshold	$V_{int\_sup\_OV}$	6.37	6.5	6.63	V	V_{QIS} increasing	DS-2008
Voltage monitoring fault detection time	t_{mon_fdti}	6		12	µs	–	DS-2001
Voltage monitoring fault detection time standby	$t_{mon\_fdti\_stb}$	8		50	µs	–	DS-2002

1) 未经过生产测试，由设计指定

10.3.5 外部监测通道（VMON）

10.3.5.1 功能描述：外部监测通道（VMON）

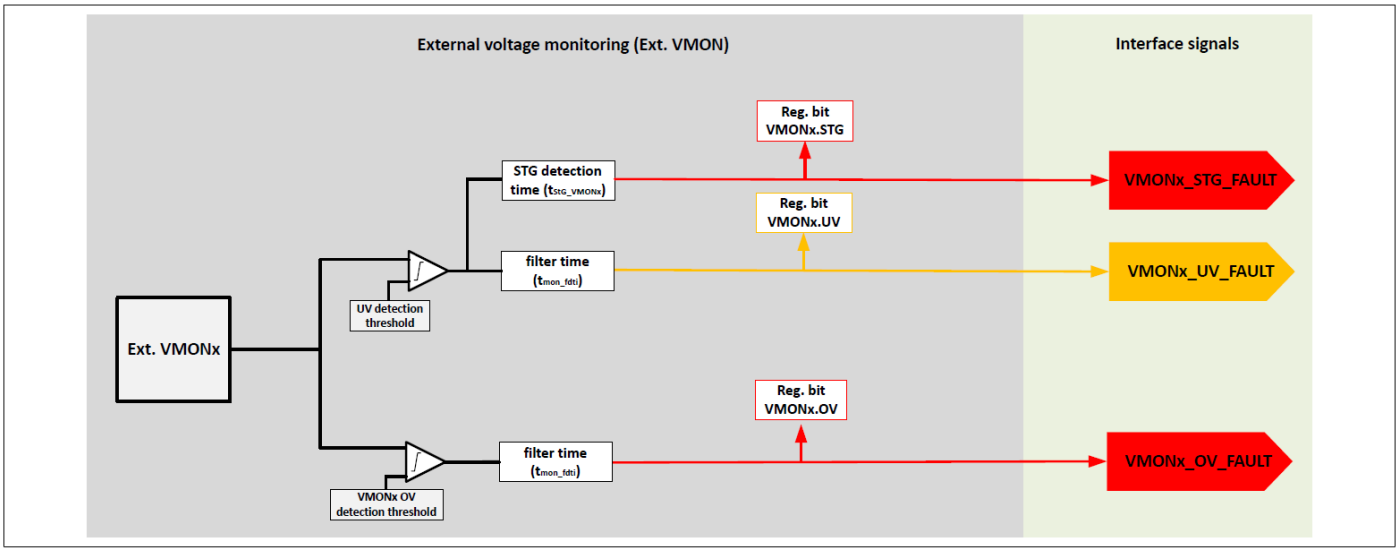


图 59 外部电压监测功能框图

器件包含双通道（VMON1 或 VMON2），每个通道由两个引脚 VMxFB 和 VMxEN 组成。外部电压轨与引脚 VM1FB 和 VM2FB 上的预定义阈值进行比较。必须使用外部电阻分压器将待监测电压缩放到监测窗口的中点（典型值：0.8 V）。引脚 VM1EN 和 VM2EN 的输出分别连接到相应的监测输入 VM1FB 和 VM2FB。如果自动使用检测在启动期间检测到通道正在使用，或者之后通过 SPI 禁用并重新启用通道，则它们会提供高电平 V_{VMxEN_Ho}。它可用于在器件的启动和关闭序列中启用和嵌入外部稳压器。

当信号超过阈值且持续时间超过故障检测时间t_{mon_fdti} 时，就会产生欠压或过压事件。

启动期间，器件检测应用中是否使用外部监测通道 VMON1 或 VMON2。如果应用中不使用相应的外部电压监测器，则必须将 VMxEN 引脚接地，以使器件能够可靠地确定是否使用电压监测器。在这种情况下，VMxFB 可以保持开放。如果使用外部电压监测通道，VMxEN 必须连接到外部调节器的使能引脚。这样就将电压轨的启动正确地整合到了启动序列中。

注释： *如果不使用，VMON1 和VMON2 将被排除在电源序列之外。*

如果引脚 V_{VMxFB} 处的输出电压低于欠压阈值 V_{MONx_UV} 的时间长于对地短路检测时间 t_{StG_VMONx}，则器件检测到外部监测通道之一存在接地短路 (StG)。

每个外部监测通道的接地短路检测时间 t_{STG_VMONx}可通过 SPI 寄存器位字段 **DEV_PW_CFG2.VMONx_STG_TIME** 进行编程

(x = 1; 2)

10.3.5.2 电气特性：外部监测通道（VMON）

表 38 电气特性：外部监测通道（VMON）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage high level (x=1 or 2)	V_{VMxEN_H}	2	–	–	V	$V_{QUC} \geq V_{QUC}$[Min]; I_{VMxEN} = -7 mA	DS-1656
Output voltage low level (X = 1 or 2)	V_{VMxEN_L}	–	–	0.7	V	I_{VMxEN} = 5 mA	DS-1657
Short to ground detection time for VMON1	t_{STG_VMON1}	1		6	ms	t_{STG_VMON1} is programmable between 1ms, 2ms, 4ms and 6ms via SPI with a default value of 6ms	DS-1942
accuracy of the short to ground detection time for VMON1	$t_{STG\_VMON1\_acc}$	t_{STG_VMON1} - (10 %*t_{STG_VMON1})	t_{STG_VMON1}	t_{STG_VMON1} + (10 %*t_{STG_VMON1})	ms		DS-1943
Short to ground detection time for VMON2	t_{STG_VMON2}	1		6	ms	t_{STG_VMON2} is programmable between 1 ms, 2 ms, 4 ms and 6 ms via SPI with a default value of 6 ms	DS-1939
Accuracy of the short to ground detection time for VMON2	$t_{STG\_VMON2\_acc}$	t_{STG_VMON2} - (10 %*t_{STG_VMON2})	t_{STG_VMON2}	t_{STG_VMON2} + (10 %*t_{STG_VMON2})	ms		DS-1938
VMON1 overvoltage threshold	$V_{mon\_MON1\_OV}$	858	872	886	mV	V_{VM1FB} increasing	DS-1957
VMON1 overvoltage hysteresis	$V_{mon\_MON1\_OV\_HYS}$	5[1)]		15	mV	V_{VM1FB} decreasing	DS-1958
VMON1 undervoltage threshold	$V_{mon\_MON1\_UV}$	716	728	740	mV	V_{VM1FB} decreasing	DS-1959
VMON1 undervoltage hysteresis	$V_{mon\_MON1\_UV\_HYS}$	5[1)]		15	mV	V_{VM1FB} increasing	DS-1960

（表格续下页……）

表 38 (续) 电气特性：外部监测通道（VMON）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VMON2 overvoltage threshold	$V_{mon\_MON2\_OV}$	858	872	895	mV	V_{VM2FB} increasing	DS-1961
VMON2 overvoltage hysteresis	$V_{mon\_MON2\_OV\_HYS}$	5[1)]		15	mV	V_{VM2FB} decreasing	DS-2009
VMON2 undervoltage threshold	$V_{mon\_MON2\_UV}$	716	728	750	mV	V_{VM2FB} decreasing	DS-2010
VMON2 undervoltage hysteresis	$V_{mon\_MON2\_UV\_HYS}$	5[1)]		15	mV	V_{VM2FB} increasing	DS-2011

1) 未经过生产测试，由设计指定

10.4 过流和过温监测

10.4.1 介绍

过温或过流监测功能可保护器件免受瞬态过温影响（例如：负载突降或短路）。

过温监测

该器件为安全区域和除备用 (QST) 和基准 (QVR) 调节器之外的所有后置稳压器提供过温监测传感器。

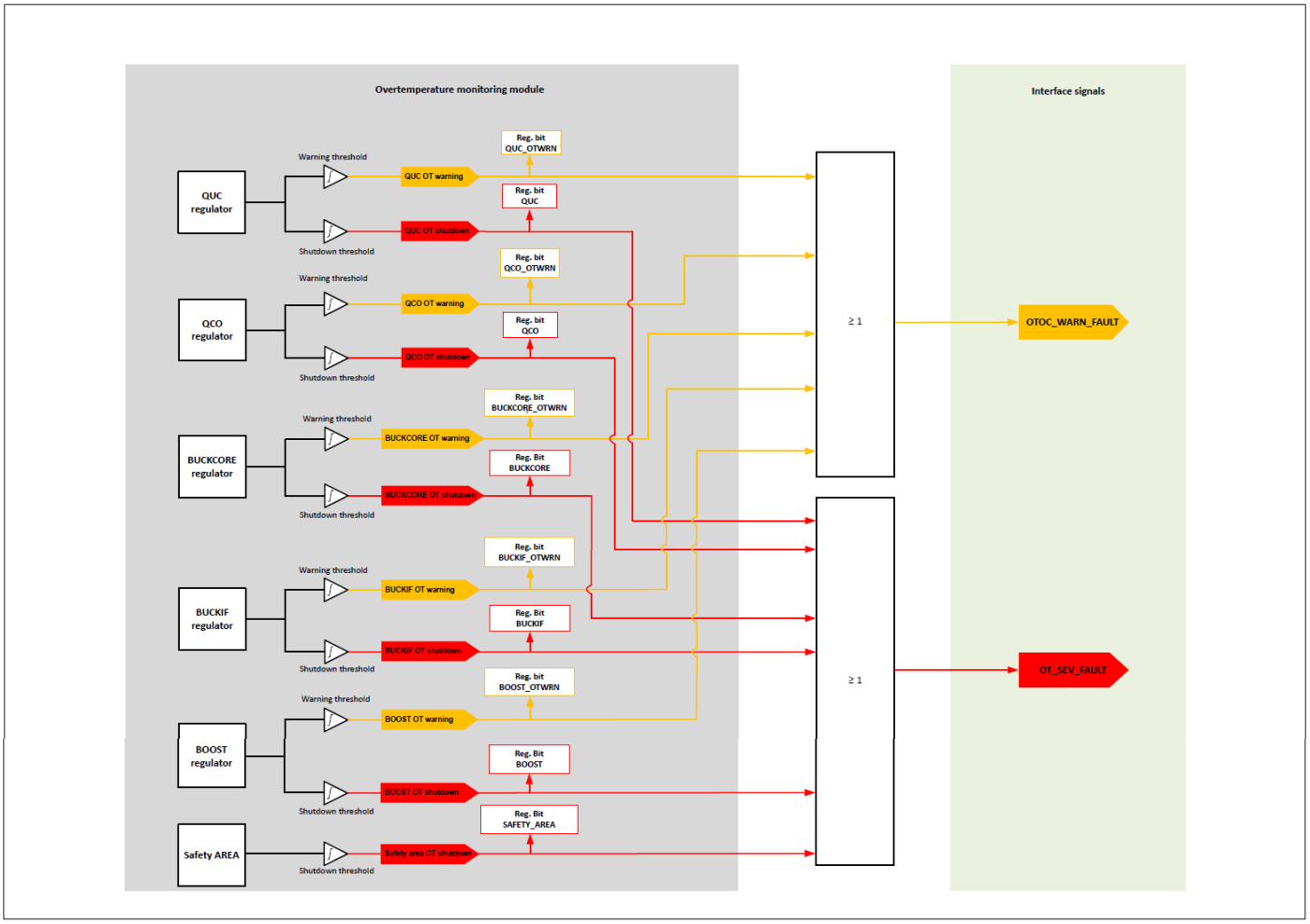


图 60　　过温监测功能的功能框图

过流监测

该器件为升压调节器、备用调节器 (QST)、内部电源 (IVCC) 和基准稳压器 (QVR) 提供过流监测传感器。

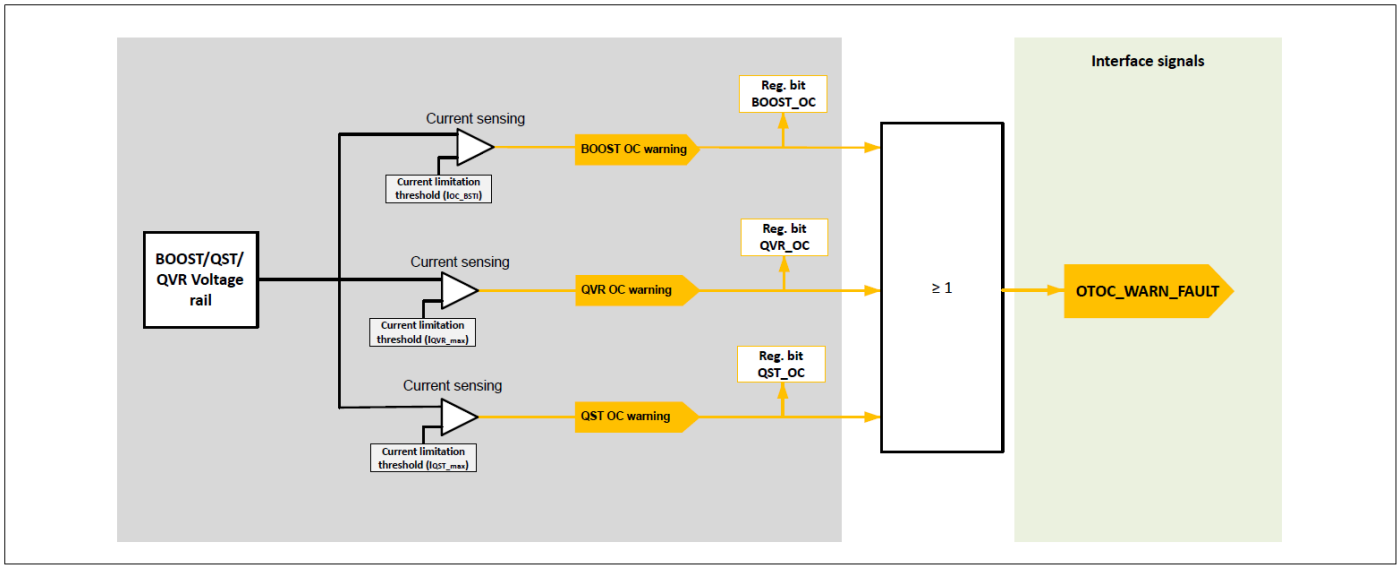


图 61　　过流监测功能框图

10.4.2 功能描述：过温监测

采用了两种过温检测阈值：

过热警告

如果监测功能块的温度超过第一阈值（过温警告阈值（t_{PRE}）），则器件：

- 设置相应的过温警告位，如果温度降至警告阈值以下，则可通过 SPI 清除该位
- 生成过温警告故障 OTOC_WARN_FAULT，请参阅章节 9

过温关断

如果监测功能块的温度持续上升并超过第二阈值（过温关断阈值（t_{OT}）），则器件：

- 设置相应的过温关断位，如果温度降至关断阈值以下，则可通过 SPI 清除该位
- 产生过温严重故障 OT_SEV_FAULT，请参阅章节 9

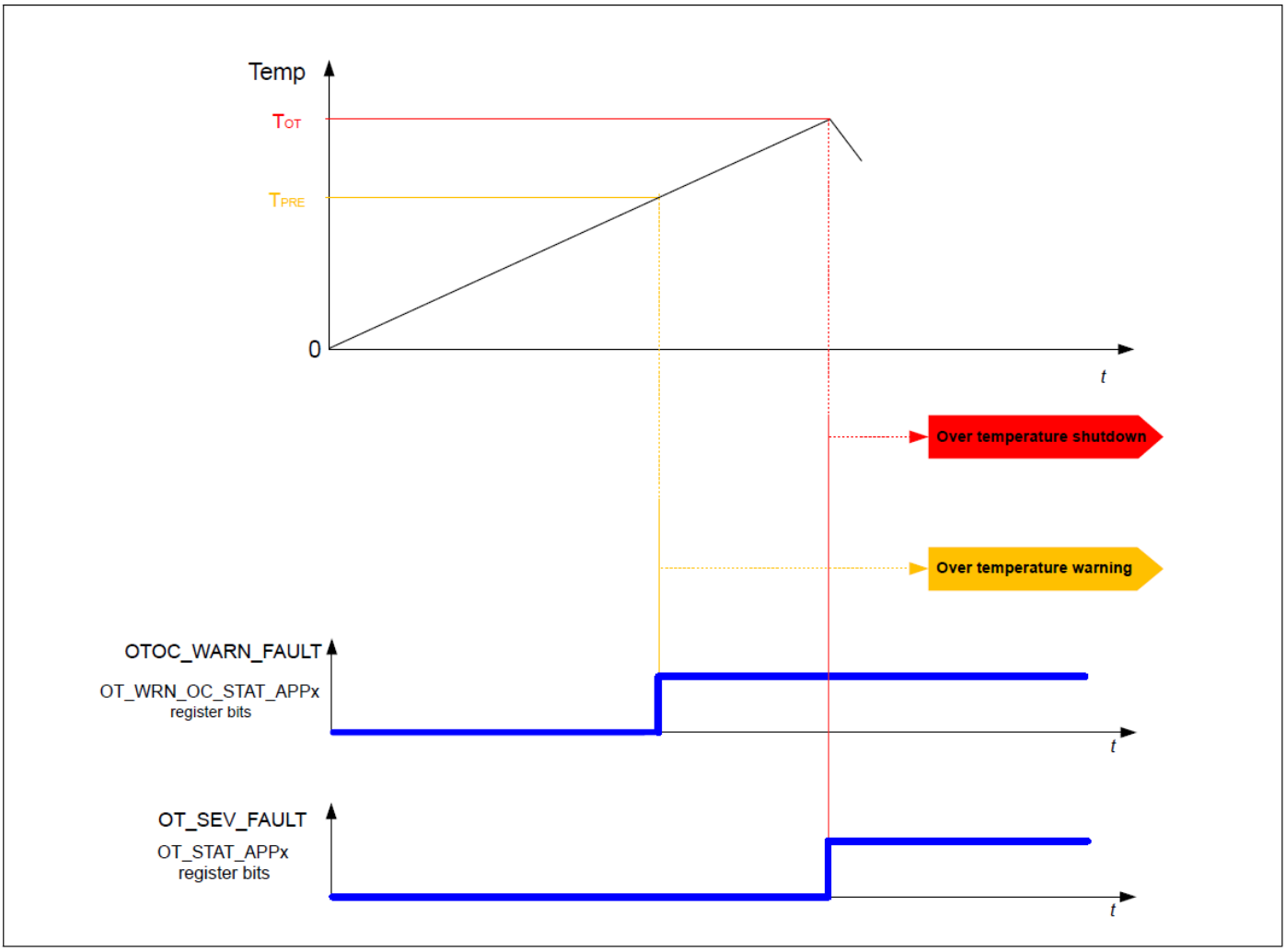


图 62 过温监测信号图

10.4.3 功能描述：电流监测

如果监测调节器的输出电流达到过流限制阈值，则器件：

- 设置相应的过流警告位，当电流降至警告阈值以下时，可通过 SPI 清除该位
- 生成过流警告故障 OTOC_WARN_FAULT，请参阅章节 9
- 因此，相应调节器的输出电压立即开始下降

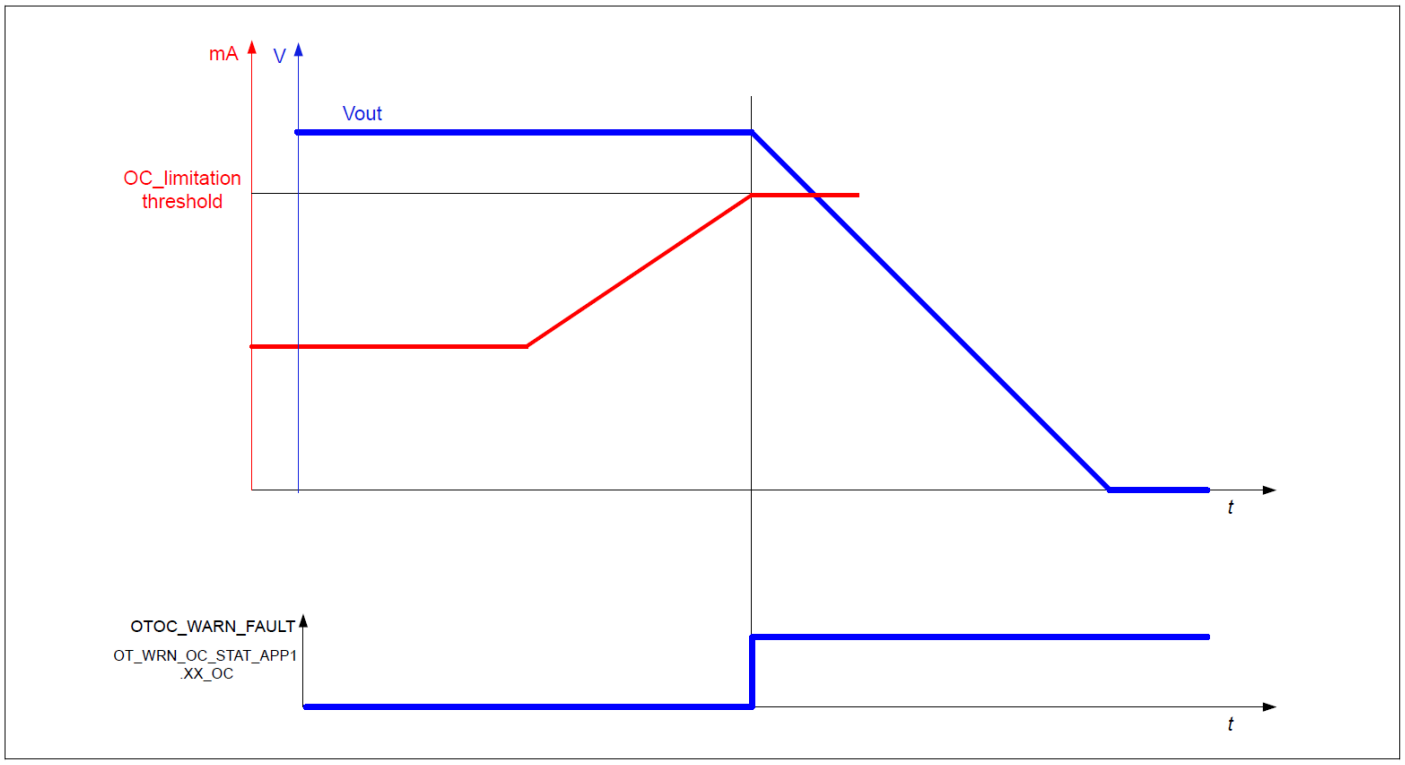


图 63　过流监测信号图

10.4.4　电气特性：过温监测

表 39　电气特性：过温监测

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overtemperature pre-warning threshold	T_{PRE}	136	146	156	°C	T_j increasing[1)]	DS-1402
Overtemperature threshold	T_{OT}	177	187	197	°C	T_j increasing[1)]	DS-1403

1)　未经过生产测试，由设计指定

10.5　安全状态控制（SSOx）

10.5.1　介绍

安全状态控制模块监控安全相关信号并控制安全状态输出。以下说明总结了对安全状态控制功能的各个贡献项，以及可对其进行调整的方式。

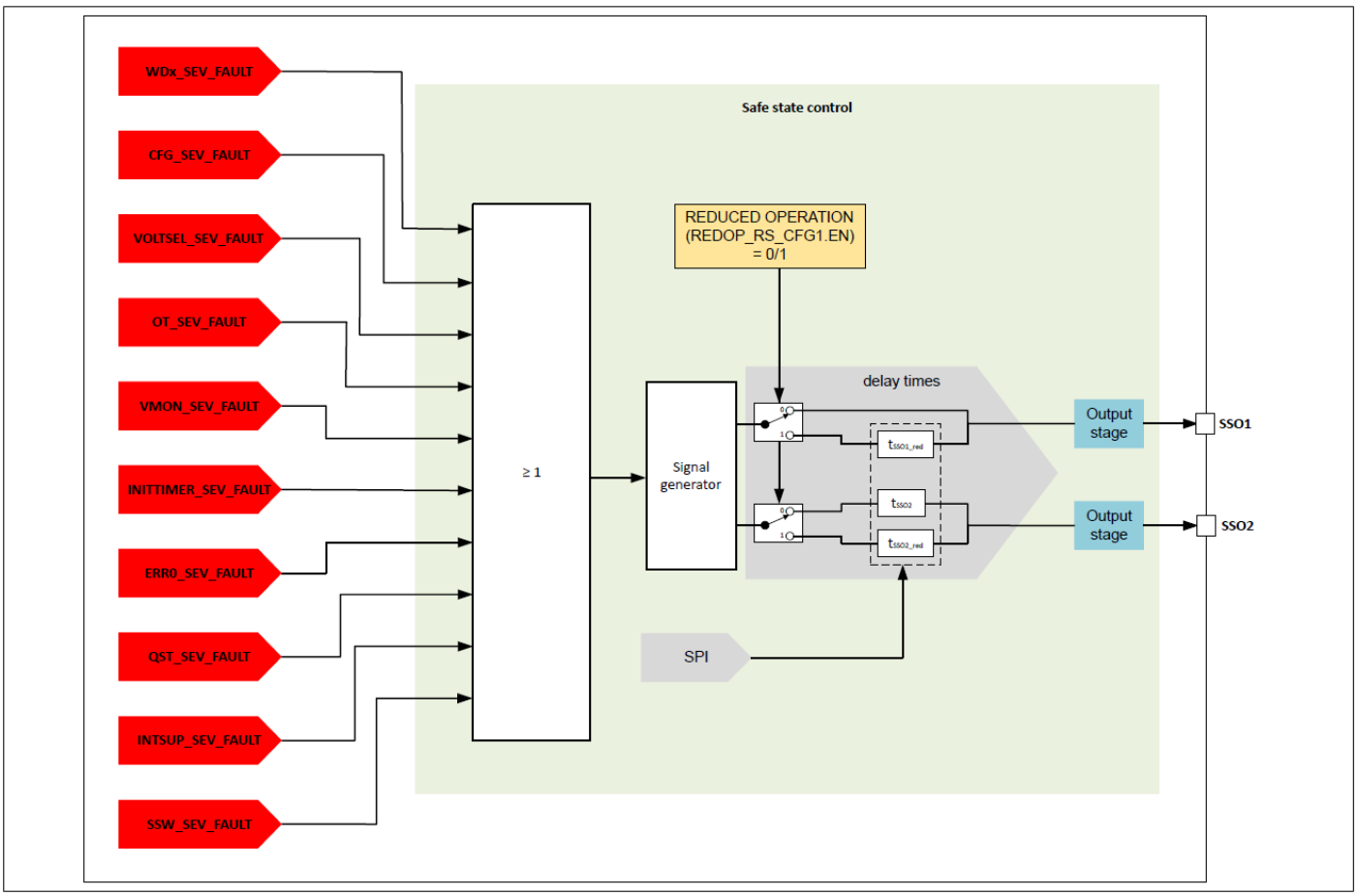


图 64　　安全状态控制功能框图

安全状态控制模块提供两个安全状态输出控制通道：

- 安全状态控制通道 1 在引脚 SSO1 上生成安全状态输出信号
- 安全状态控制通道 2 在引脚 SSO2 上生成安全状态输出信号

安全状态控制模块在电路、信号和布局上设计成独立于器件电源部分。

10.5.2　　功能描述：关断路径（SSOx）

器件会在除 NORMAL 之外的任何状态下激活关断路径（SSOx 输出低电平）。任何导致器件离开 NORMAL 状态的故障或状态转移指令都会导致 SSO1 或 SSO2 或两者都被拉低，具体取决于故障。另请参阅检测到故障时的反应。

10.5.2.1　　检测到错误时的延迟时间和反应

安全状态控制通过可选的延迟时间来实现。这些功能使应用能够根据应用的使用情况生成两个独立的安全状态输出信号：

单一应用案例：

通过将寄存器位 **REDOP_PW_CFG1.EN** 设置为 0 来激活单个应用。

在检测到任何严重故障后，器件立即将 SSO1 引脚上的输出信号设置为“低”，而 SSO2 引脚上的输出信号在延迟时间（t_{SSO2}）后拉为“低”。

延迟时间（t_{SSO2}）可以在寄存器位字段 **REDOP_PW_CFG1.SSO1TOSSO2_DEL** 中配置。

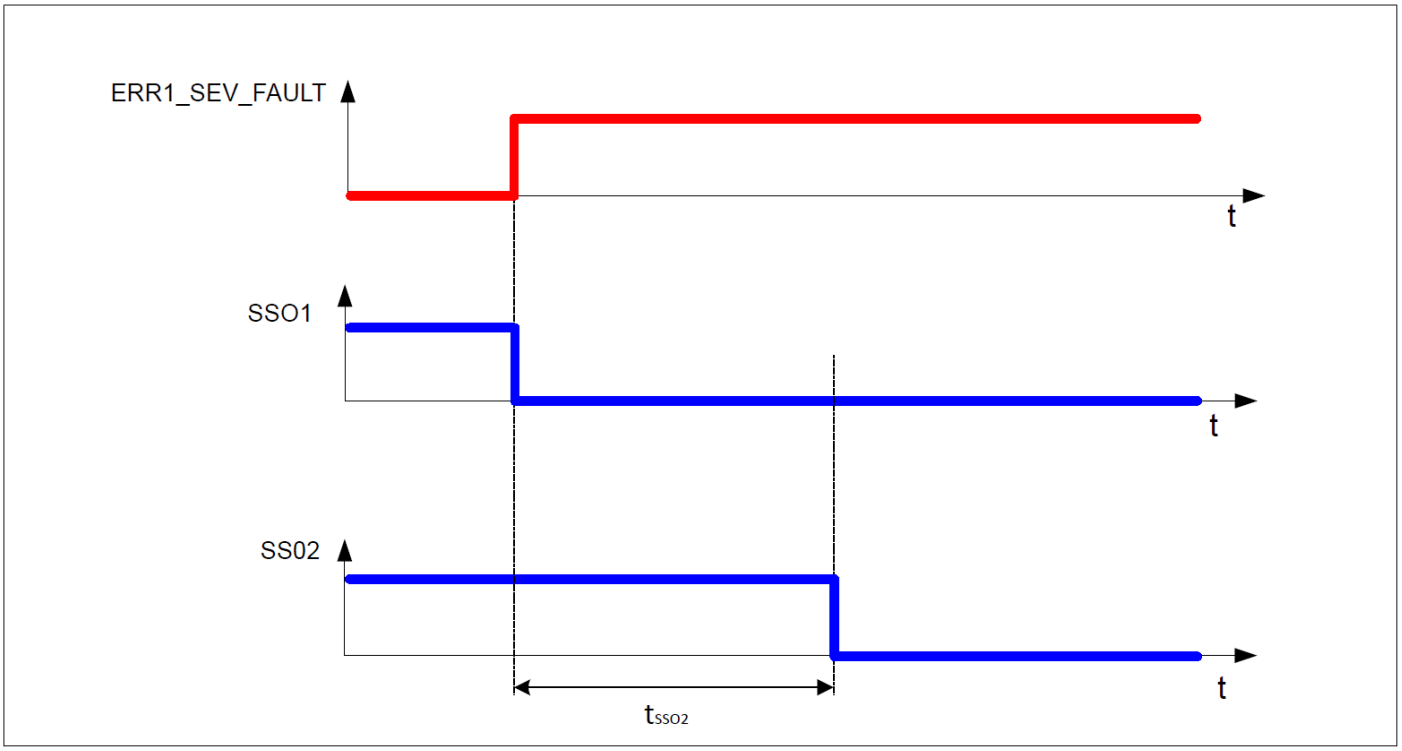


图 65　　单个应用案例的 SSOx 生成流程图（如果 ERR1 是错误源）

(x = 1, 2)

双重应用案例：

通过将寄存器位 **REDOP_PW_CFG1.EN** 设置为 1 来激活双重应用。

一旦检测到任何严重故障，器件就会将引脚 SSO1 或 SSO2 上的输出信号设置为“低”。如果严重故障仅源自两个应用之一，则相关的 SSOx 引脚置位为低电平。可以通过配置寄存器位字段 **REDOP_PW_CFG1.SSOx_DEL** 中的延迟时间 (t_{SSOx_red}) 来延迟此激活。

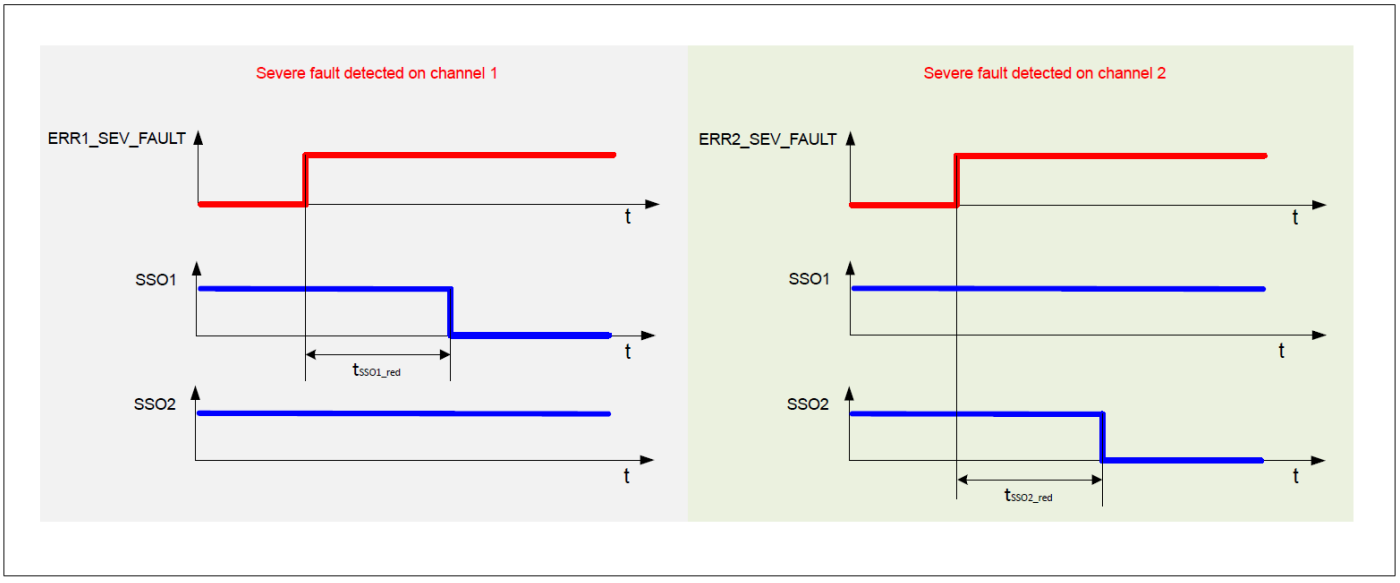


图 66　　双应用案例的 SSOx 生成流程图 (REDOP_PW_CFG1.EN = 1)

注释： *上述段落中描述的延迟时间仅适用于未进入 FAILSAFE 的故障类型。换句话说，如果进入 FAILSAFE 状态，则 SSO1/2 的延迟时间不适用。*

10.5.3 电气特性：关断路径（SSOx）

表 40 电气特性：关断路径（SSOx）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output high level 1 mA	V_{SSOx_HIGH}	2.9	3.2	V_{QUC}	V	I_{SSOx} ≥ -1 mA; V_{QUC} = V_{QUC} [Min]	DS-1613
Output high level 5 mA	V_{SSOx_HIGH}	2.0	2.8	V_{QUC}	V	I_{SSOx} ≥ -5 mA; V_{QUC} = V_{QUC} [Min]	DS-1615
Pull-down resistor	R_{SSOx}	70	100	130	kΩ	–	DS-1616
Output low level	V_{SSOx_LO}	–	0	0.3	V	$R_{SSOx\_PD\_EXT}$ ≤ 100 kΩ; I_{SSOx} <= 1.2 mA; QUC active; V_{QUC} ≥ 2.9 V; -40°C ≤ Tj ≤ 150°C	DS-2081
SSO2 reaction delay time	t_{SSO2}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1618
SSO1 reaction delay time for REDUCED OPERATION	t_{SSO1_red}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1619
SSO2 reaction delay time for REDUCED OPERATION	t_{SSO2_red}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1620
Timebase accuracy	t_{SSC}	-10	-	10	%		DS-1999

10.6 故障反应

10.6.1 检测到故障时的反应

表 41 调节器检测事件的反应

Module	Event description	REDUCED OPERATION ON/OFF	State transition	IO reaction	Register name	Bitfield name
Battery Monitoring	VS OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	VBAT_OV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	VBAT_OV
BOOST	BOOST OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BOOST

（表格续下页……）

表 41 （续）调节器检测事件的反应

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	BOOST
	BOOST overcurrent	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BOOST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BOOST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BOOST_OC
	BOOST overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BOOST_OT WRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BOOST_OT WRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BOOST_OT WRN
	BOOST short to ground or Severe undervoltage or undervoltage at BSTI pin	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_A P P1	BOOST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_A P P2	BOOST
	BOOST thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	BOOST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	BOOST
	Undervoltage at BOOST	off	No transition	INT1	UV_STAT_APP 1	BOOST
		on	No transition	INT1, INT2	UV_STAT_APP 1	BOOST
		on	No transition	INT1, INT2	UV_STAT_APP 2	BOOST
BUCKCORE	BUCKCORE overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BUCKCORE_ OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BUCKCORE_ OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BUCKCORE_ OTWRN
	BUCKCORE short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_A P P1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_A P P2	BUCKCORE

（表格续下页……）

表 41 （续）调节器检测事件的反应

	BUCKCORE thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	BUCKCORE
	BUCKCORE undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP1	BUCKCORE
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP1	BUCKCORE
	Feedback open	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BUCKCORE_FB_OPEN
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	BUCKCORE_FB_OPEN
	Severe overvoltage at BUCKCORE or BUCKCORE OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	BUCKCORE
	Static voltage scaling completed successfully.	off	No transition	INT1	SYS_STAT_AP P1	BUCKCORE_SVS_OK
		on	No transition	INT1, INT2	SYS_STAT_AP P1	BUCKCORE_SVS_OK
		on	No transition	INT1, INT2	SYS_STAT_AP P2	BUCKCORE_SVS_OK
	Static voltage scaling not performed due to: - Device being not in INIT or NORMAL - BUCKCORE voltage set to 1.15 V - Invalid SPI value	off	No transition	INT1	SYS_STAT_AP P1	BUCKCORE_SVS_NOK
		on	No transition	INT1, INT2	SYS_STAT_AP P1	BUCKCORE_SVS_NOK
		on	No transition	INT1, INT2	SYS_STAT_AP P2	SBUCKCORE_SVS_NOK
	Voltage selection error. Core voltage might be corrupt.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	BUCK_CORE_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	BUCK_CORE_VOLTSEL
BUCKIF	BUCKIF overtemperature warning	off	No transition	INT1	OT_WRN_OC_STAT_APP1	BUCKIF_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	BUCKIF_OTWRN

(table continues...)

10 Monitoring functions

表 41 （续）调节器检测事件的反应

		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	BUCKIF_OTWRN
	BUCKIF thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	BUCKIF
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	BUCKIF
	Severe overvoltage at BUCKIF or BUCKIF OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BUCKIF
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	BUCKIF
	Undervoltage at BUCKIF	off	No transition	INT1	UV_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	UV_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	UV_STAT_APP2	BUCKIF
	Voltage selection error. 1.8 or 3.3 V might be corrupt and not correctly selected.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	BUCKIF_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	BUCKIF_VOLTSEL
	Short to ground at BUCKIF	off	No transition	INT1	STG_STAT_AP P1	BUCKIF
		on	No transition	INT1, INT2	STG_STAT_AP P1	BUCKIF
		on	No transition	INT1, INT2	STG_STAT_AP P2	BUCKIF
PREREG	PREREG short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P1	PREREG
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P2	PREREG
	Severe overvoltage at PREREG & PREREG OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	PREREG
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	PREREG
	Undervoltage at PREREG	off	No transition	INT1	UV_STAT_APP1	PREREG
		on	No transition	INT1, INT2	UV_STAT_APP1	PREREG
		on	No transition	INT1, INT2	UV_STAT_APP2	PREREG

(table continues...)

表 41 （续）调节器检测事件的反应

QCO	QCO OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QCO
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QCO
	QCO overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	QCO_OTWR N
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	QCO_OTWR N
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	QCO_OTWR N
	QCO thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	QCO
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	QCO
	Undervoltage at QCO	off	No transition	INT1	UV_STAT_APP 1	QCO
		on	No transition	INT1, INT2	UV_STAT_APP 1	QCO
		on	No transition	INT1, INT2	UV_STAT_APP 2	QCO
	Short to ground at QCO	off	No transition	INT1	STG_STAT_A P P1	QCO
		on	No transition	INT1, INT2	STG_STAT_A P P1	QCO
		on	No transition	INT1, INT2	STG_STAT_A P P2	QCO
QST	QST OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QST
	QST overcurrent	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	QST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	QST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	QST_OC
	QST undervoltage or Severe undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QST
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QST

（表格续下页……）

表 41 （续）调节器检测事件的反应

	QST short to ground	on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P2	QST
	QST BIST errors, severe overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	QST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	QST
	QST short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P1	QST
QST/QUC	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	QST_QUC_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	QST_QUC_VOLTSEL
QUC	QUC OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QUC
	QUC overtemperature warning	off	No transition	INT1	OT_WRN_OC_STAT_APP1	QUC_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	QUC_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	QUC_OTWRN
	QUC short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P2	QUC
	QUC thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	QUC
	QUC undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QUC
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QUC
QVR	QVR OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QVR
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QVR
	QVR overcurrent	off	No transition	INT1	OT_WRN_OC_STAT_APP1	QVR_OC

（表格续下页……）

表 41 （续）调节器检测事件的反应

		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	QVR_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	QVR_OC
	Undervoltage at QVR	off	No transition	INT1	UV_STAT_APP1	QVRUV
		on	No transition	INT1, INT2	UV_STAT_APP1	QVRUV
		on	No transition	INT1, INT2	UV_STAT_APP2	QVR
	QVR short to ground	off	No transition	INT1	STG_STAT_AP P1	QVR
		on	No transition	INT1, INT2	STG_STAT_AP P1	QVR
		on	No transition	INT1, INT2	STG_STAT_AP P2	QVR
VMON1	Undervoltage at VMON1	off	No transition	INT1	UV_STAT_APP1	VMON1
		on	No transition	INT1, INT2	UV_STAT_APP1	VMON1
		on	No transition	INT1, INT2	UV_STAT_APP2	VMON1
	VMON1 OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	VMON1
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	VMON1
	Short to ground at VMON1	off	No transition	INT1	STG_STAT_AP P1	VMON1
		on	No transition	INT1, INT2	STG_STAT_AP P1	VMON1
		on	No transition	INT1, INT2	STG_STAT_AP P2	VMON1
VMON2	Undervoltage at VMON2	off	No transition	INT1	UV_STAT_APP1	VMON2
		on	No transition	INT1, INT2	UV_STAT_APP1	VMON2
		on	No transition	INT1, INT2	UV_STAT_APP2	VMON2
	VMON2 OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	VMON2

（表格续下页……）

表 41 （续）调节器检测事件的反应

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	VMON2
	Short to ground at VMON2	off	No transition	INT1	STG_STAT_AP P1	VMON2
		on	No transition	INT1, INT2	STG_STAT_AP P1	VMON2
		on	No transition	INT1, INT2	STG_STAT_AP P2	VMON2

1) 仅用于转入 INIT

2) 由于转入 FAILSAFE，INTx 也将变为低电平（QUC 在 FAILSAFE 关闭）（x = 1; 2）

表 42 系统检测事件的反应

Module	Event description	REDUCED OPERATION ON/OFF	State transition	IO reaction	Register name	Bitfield name
SSW	Major error detected during SSW BIST or SSW was activated during normal operation	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	PREREG_COSW
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	PREREG_COSW
ENA	ENA signal detected (only when waking up form FAILSAFE, STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP1	ENA
		on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP2	ENA

（表格续下页……）

表 42 （续）系统检测事件的反应

		off	Move into WAKE or INIT if device is in STANDBY or SLEEP or within the transition into those states. Else no transition takes place.	INT1[3)]	WAKE_STAT_APP1	ENA
WAK	WAK signal detected (only when waking up form FAILSAFE, STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP2	WAK
		on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP1	WAK
		off	Move into WAKE or INIT if device is in STANDBY or SLEEP or within the transition into those states. Else no transition takes place.	INT1[3)]	WAKE_STAT_APP1	WAK
WUT	Wake-up timer (WUT) expired and woke up the device (only when waking up form STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT2	WAKE_STAT_APP2	WUT
		on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP1	WUT

（表格续下页……）

表 42 （续）系统检测事件的反应

		off	Move into WAKE or INIT if device is in STANDBY or SLEEP. Else no transition takes place.	INT1	WAKE_STAT_APP1	WUT
ERR0	ERR0 monitoring error AND ERR0 recovery is enabled	on	No transition	INT1, INT2	SYS_STAT_APP2	ERR0_ERR
		on	No transition	INT1, INT2	SYS_STAT_APP1	ERR0_ERR
		off	No transition	INT1	SYS_STAT_APP1	ERR0_ERR
	FAILSAFE was entered after ERR0 reported invalid frequency (No recovery enabled or recovery expired)	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	ERR0
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	ERR0
ERR1	ERR1 monitoring error AND ERR1 recovery is enabled (less than t_{REC})	any	No transition	INT1	SYS_STAT_APP1	ERR1_ERR
	ERR1 signal is outside of of valid frequencies (if recovery enabled: longer than t_{REC} before being set)	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	ERR1
		on	Move to REDUCED OPERATION	INT2[4)]	INIT_ERR_APP2	ERR1
		on	Move to REDUCED OPERATION	INT1[6)], SSO1	INIT_ERR_APP1	ERR1
ERR2	ERR2 monitoring error AND ERR2 recovery is enabled (less than t_{REC})	on	No transition	INT2	SYS_STAT_APP2	ERR2_ERR
	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than t_{REC} before being set)	on	Move to REDUCED OPERATION	INT2[6)], SSO2	INIT_ERR_APP2	ERR2
		on	Move to REDUCED OPERATION	INT1[4)]	INIT_ERR_APP1	ERR2

（表格续下页……）

表 42 （续）系统检测事件的反应

FSM	FAILSAFE was entered because INIT timer expired a 3rd time in a row without successful initialization.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	FSM_INITTIMER
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	FSM_INITTIMER
	INIT timer expires 1st time Soft reset issued	off/on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	SOFTRES
		on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP2	SOFTRES
	INIT timer expires 2nd time in a row Hard reset issued	off/on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	HARDRES
		on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP2	HARDRES
	State transition into low power state (STANDBY or SLEEP) failed/ interrupted (e.g. by WAK or ENA)	off	Move into WAKE or INIT (depending on the transition)	INT1, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP1	FSM_TRFAIL
	State transition into low power state (STANDBY or SLEEP) failed/ interrupted (e.g. by WAK or ENA)	on	Move into WAKE or INIT (depending on the transition)	INT1, INT2, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP1	FSM_TRFAIL
		on	Move into WAKE or INIT (depending on the transition)	INT1, INT2, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP2	FSM_TRFAIL
	State transition not existing or transition conditions not fulfilled.	off	No transition	INT1	SYS_STAT_APP1	FSM_NOOP
		on	No transition	INT1, INT2	SYS_STAT_APP1	FSM_NOOP
		on	No transition	INT1, INT2	SYS_STAT_APP2	FSM_NOOP
WWD1	WWD1 incorrectly triggered and error counter reaches or exceeds threshold	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	WWD1_EC
		on	Move to REDUCED OPERATION	INT2[4)]	INIT_ERR_APP2	WWD1_EC
		on	Move to REDUCED OPERATION	INT1[6)], SSO1	INIT_ERR_APP1	WWD1_EC

（表格续下页……）

表 42 （续）系统检测事件的反应

	WWD1 missed or incorrect service (error counter below threshold)	any	No transition	INT1	SYS_STAT_APP1	WWD1_ERR
WWD2	WWD2 incorrectly triggered and error counter reaches threshold	on	Move to REDUCED OPERATION	INT2[6], SSO2	INIT_ERR_APP2	WWD2_EC
		on	Move to REDUCED OPERATION	INT1[4]	INIT_ERR_APP1	WWD2_EC
	WWD2 missed or incorrect service (error counter below threshold)	on	No transition	INT2	SYS_STAT_APP2	WWD2_ERR
FWD1	FWD1 incorrectly triggered and error counter reaches threshold	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	FWD1_EC
		on	Move to REDUCED OPERATION	INT2[4]	INIT_ERR_APP2	FWD1_EC
		on	Move to REDUCED OPERATION	INT1[6], SSO1	INIT_ERR_APP1	FWD1_EC
	FWD1 response missed or incorrectly triggered (error counter below threshold)	any	No transition	INT1	SYS_STAT_APP1	FWD1_ERR
FWD2	FWD2 response missed or incorrectly triggered (error counter below threshold)	on	No transition	INT2	SYS_STAT_APP2	FWD2_ERR
	FWD2 incorrectly triggered and error counter reaches threshold	on	Move to REDUCED OPERATION	INT2[6], SSO2	INIT_ERR_APP2	FWD2_EC
		on	Move to REDUCED OPERATION	INT1[4]	INIT_ERR_APP1	FWD2_EC
INT	Interrupt flags not cleared after t_{INTx_to}	any	No transition	-	IF1	INTMISS
		on	No transition	-	IF2	INTMISS

（表格续下页……）

表 42 （续）系统检测事件的反应

Internal Element	Internal 2V5 rail overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	INTSUP_VDD2V5
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	INTSUP_VDD2V5
	Internal 2V5 rail undervoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP1	INTSUP_VDD2V5_UV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP2	INTSUP_VDD2V5_UV
	Internal bias current too high	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	BIAS_HI
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	BIAS_HI
	Internal bias current too low	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	BIAS_LOW
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	BIAS_LOW
	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx can be set)	off	No transition	INT1	INTSUP_STAT_APP1	BG12_OV
		off	No transition	INT1	INTSUP_STAT_APP1	BG12_UV
		off	No transition	INT1	INTSUP_STAT_APP1	PMU_MAIN
		off	No transition	INT1	INTSUP_STAT_APP1	PMU_RED
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	BG12_OV
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	BG12_UV
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	PMU_MAIN
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	PMU_RED
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	BG12_OV

（表格续下页……）

表 42 （续）系统检测事件的反应

		on	No transition	INT1, INT2	INTSUP_STAT_APP2	BG12_UV
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	PMU_MAIN
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	PMU_RED
	Internal IVCC overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	INTSUP_IVCC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	INTSUP_IVCC
	Internal IVCC undervoltage or short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP1	INTSUP_IVCC_UV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP2	INTSUP_IVCC_UV
	Internal IVCC overcurrent	off	No transition	INT1	OT_WRN_OC_STAT_APP1	IVCC_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	IVCC_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	IVCC_OC
	Interval IVCC BIST errors, severe overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	INTSUP_IVCC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	INTSUP_IVCC
	Double Error detected on a protected register	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	CFGE
	Double Error detected on a protected register	on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	CFGE
Safety Area	Overtemperature of safety area	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	SAFETY_AREA

（表格续下页……）

表 42 （续）系统检测事件的反应

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	SAFETY_AREA
SPI	CRC wrong	off	No transition	INT1	SPI_FAIL_STAT_APP1	CRC
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	CRC
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	CRC
	CSN timeout after 2 ms	off	No transition	INT1	SPI_FAIL_STAT_APP1	CS_TO
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	CS_TO
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	CS_TO
	Frame length wrong	off	No transition	INT1	SPI_FAIL_STAT_APP1	FR_LEN
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	FR_LEN
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	FR_LEN
	Invalid address	off	No transition	INT1	SPI_FAIL_STAT_APP1	ADR
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	ADR
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	ADR
	Lock of protected registers was unsuccessful (will cause the registers to be locked again and made changes are ignored)	off	No transition	INT1	SPI_FAIL_STAT_APP1	LOCK
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	LOCK
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	LOCK
	SPI command woke up the device while in sleep	on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP2	SPI

（表格续下页……）

表 42 （续）系统检测事件的反应

		on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP1	SPI
		off	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1	WAKE_STAT_APP1	SPI
ABIST	ABIST finished execution	off	No transition	INT1	IF1	ABIST
		on	No transition	INT1, INT2	IF1	ABIST
		on	No transition	INT1, INT2	IF2	ABIST
	Any error that moves the device to FAILSAFE or INIT during an ABIST execution aborts the on-going ABIST and sets this bit.	any	No transition	RESOUT, SSO1, SSO2	SYSFAIL_STAT_APP1	ABIST
		on	No transition	RESOUT, SSO1, SSO2	SYSFAIL_STAT_APP2	ABIST
Application1	Application 1 was reason for entering REDUCED OPERATION	on	Move to REDUCED OPERATION	INT2[4)]	SYS_STAT_APP2	APP1_FAIL
	INIT timer expired a second time in RED. OP. due to application 1 not being able to reinitialize	on	Move to INIT	RESOUT, SSO2	INIT_ERR_APP1	REDOP_RES2
	INIT timer expired the first time in RED. OP. due to application 1 not being able to reinitialize	on	Move to REDUCED OPERATION	INT1	INIT_ERR_APP1	REDOP_RES1
Application2	Application 2 was reason for entering REDUCED OPERATION	on	Move to REDUCED OPERATION	INT1[4)]	SYS_STAT_APP1	APP2_FAIL

（表格续下页……）

表 42 （续）系统检测事件的反应

	INIT timer expired a second time in RED. OP. due to application 2 not being able to reinitialize	on	Move to INIT	RESOUT , SSO1	INIT_ERR_APP2	REDOP_RES2
	INIT timer expired the first time in RED. OP. due to application 2 not being able to reinitialize	on	Move to REDUCED OPERATION	INT2	INIT_ERR_APP2	REDOP_RES1

1) 仅用于转入 INIT
2) 由于转入 FAILSAFE，INTx 也将变为低电平（在 FAILSAFE 状态下 QUC 已关闭）
3) 仅当 BUCKCORE 和 QUC 处于开启状态时
4) 可通过 SPI 配置
5) 仅当 REDUCED OPERATION 启用
6) 应用复位
(x = 1; 2)

10.7 模拟内置自测试 (ABIST)

10.7.1 模拟内置自测试 (ABIST) - 概述

该器件包含一个模拟内置自测试功能，可由微控制器触发。它用于测试外部和内部电压轨的过压和欠压比较器，以及相应的安全逻辑。通过执行这些测试，可以确保监测功能正常工作，并且系统中的警告和安全路径完好无损。该器件区分以下几种 ABIST 主要配置：

- 仅比较器（无去毛刺）
- 包含去毛刺逻辑和中断生成（INTx）的完整路径
- 包含去毛刺逻辑和次级关断路径 (SSOx) 的完整路径

(x = 1;2)

上述测试的配置在以下寄存器中完成：

- ABIST_CTRL0
- ABIST_SELECT0
- ABIST_SELECT1
- ABIST_SELECT2

此外，器件还允许进行特定的模拟测试，这些测试会直接影响安全逻辑。为此，寄存器

- ABIST_CTRL1

必须据此编写。

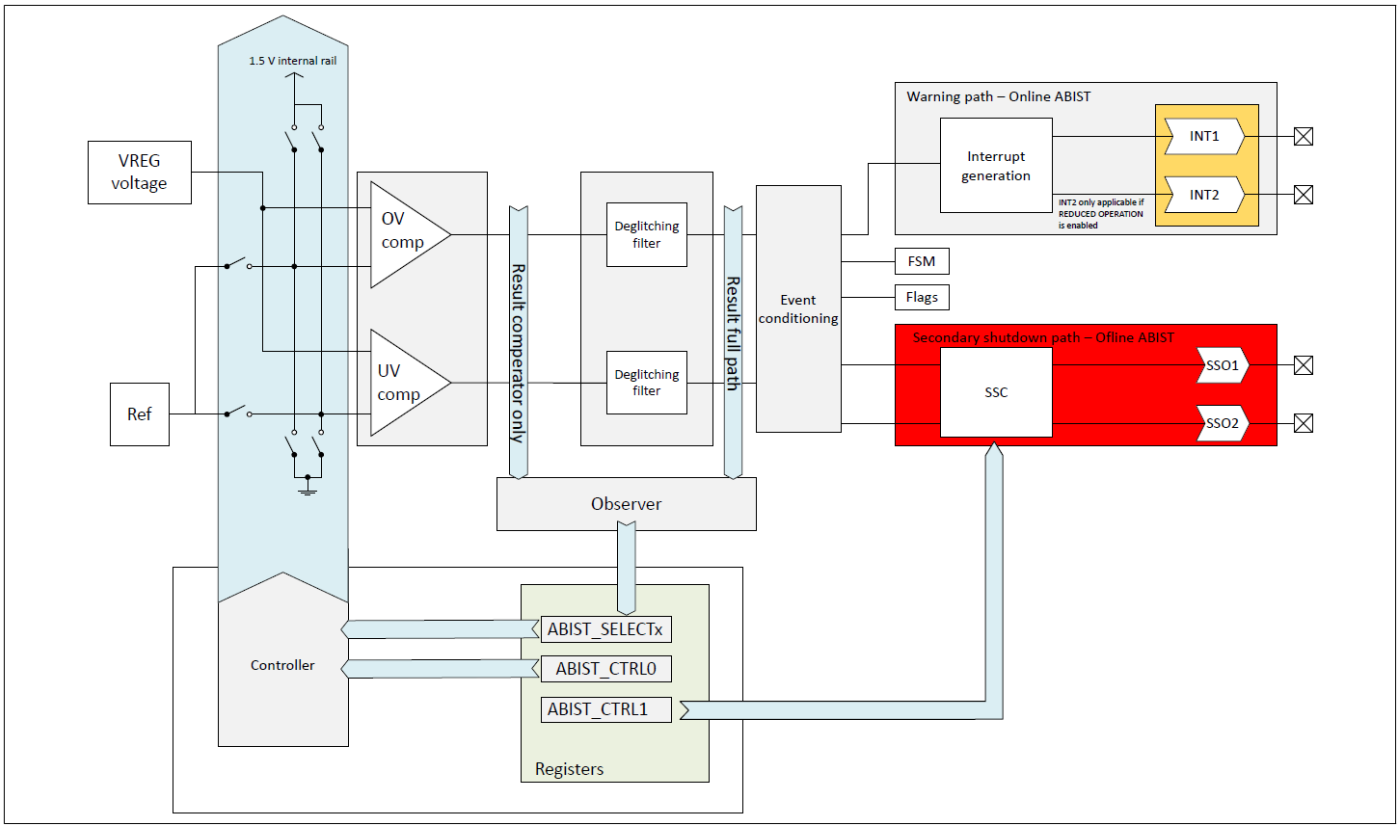


图 67　　ABIST 框图

10.7.2　　ABIST - 仅用于比较器

该器件提供仅测试比较器而不进行去毛刺逻辑的功能。在测试过程中，通过将参考输入连接到地或内部 1.5 V，使过压和欠压比较器被迫进入错误状态。该条件仅适用一段时间，且不超过去毛刺逻辑滤波时间。因此，剩余路径（警告路径，次级关断路径）不再进行进一步测试。

10.7.3　　ABIST - 完整路径

该器件提供测试内部过压和欠压比较器的功能，包括相应的去毛刺逻辑。因此，也会发出相应的完整路径（警告路径、次级关断路径）。当启动对 SSO1/2 进行完整测试的路径时，器件必须处于 NORMAL 状态。对于所有其他完整路径测试执行，也可以在 INIT 或 WAKE 模式下启动器件。接下来，比较器将被迫进入错误状态，该状态会持续足够长的时间，以触发去毛刺逻辑。这将导致剩余路径出现相应的事件。如果测试在 NORMAL 模式下启动，也会发生状态转移到 WAKE（仅适用于次级关断路径比较器，否则不会发生转换）。是否发出 INT1/2 的中断或 SSO1/2 的二次关断路径，取决于在测试开始之前已经做出的比较器选择。相应比较器属性的概述如下表所示：

表 43　　ABIST - 比较器属性到次级关断路径或警告路径

Comparator	Secondary shutdown path	Interrupt
PREREG OV	x	
QST OV	x	
QUC OV	x	

（表格续下页……）

表 43 （续） ABIST - 比较器属性到次级关断路径或警告路径

BUCKCORE OV	x	
QCO OV	x	
QVR OV	x	
BUCKIF OV	x	
BOOST OV	x	
VMON1 OV	x	
VMON2 OV	x	
IVCC OV	x	
VDD2V5 OV	*	
PREREG SEVOV	*	
BUCKCORE SEVOV	*	
BUCKIF SEVOV	*	
R3FBL_OPEN	*	
PREREG UV		x
QST UV	x	
QUC UV	x	
BUCKCORE UV	x	
QCO UV		x
QVR UV		x
BUCKIF UV		x
BOOST UV		x
VMON1 UV		x
VMON2 UV		x
IVCC UV	x	
VDD2V5 UV	*	
BSTI UV	*	
BST_DEEP_UV	x	
VBAT OV	x	
BG12 UV		x
BG12 OV		x
BIASLOW	x	
BIASHI	x	
VDD1V5 UV	*	
VDD1V5 OV	*	

（表格续下页……）

表 43 （续） ABIST - 比较器属性到次级关断路径或警告路径

VDD5V0 UV	*	
VDD5V0 OV	*	

*) 比较器有助于次级关断路径，但无法通过 ABIST 在完整路径中进行测试。

注释： *单次测试执行（仅测试一个比较器）的中断将在设备上显示两个中断。一个用于比较器测试，另一个用于测试执行完成。如果测试多个比较器，则只会发出一个测试完成的中断。SSO1/2 事件以及从 NORMAL 转入 WAKE 的状态转换，每次测试执行仅发生一次。*
这意味着，如果针对完整路径运行测试序列，则只有第一个比较器将触发状态转移及其相应的完整路径反应（次级关断路径）。其他所有比较器都将测试去毛刺逻辑并放置相应的标志。

注释： *要查看完整路径的整个反应链，其中包括 INT 引脚或 SSO1/2 引脚（取决于所选比较器）的触发，以及相应错误或状态位的标记，集成商必须确保所有需测试的受影响调节器也已启用。*

10.7.4 ABIST - 配置和执行

要执行 ABIST，必须进行以下选择和配置：

- ABIST_CTRL0：
  - START： 启动 ABIST
  - PATH：确定是测试整个路径还是只测试比较器
  - SINGLE：确定是仅执行单个比较器还是执行整个序列（仅执行 ABIST_SELECT0/1/2 中选定的比较器）
  - INT：必须配置为选择警告路径（中断相关比较器）或次级关断路径（SSO1/2 相关比较器）的测试
  - STATUS：指示 ABIST 是否已完成，有无错误
  - ALL：如果置位，则自动选择 ABIST_SELECT0/1/2 中的所有比较器，并以 PATH = 0 和 SINGLE = 0 执行测试，但 BSTI UV比较器除外
- ABIST_SELECT0/1/2：确定执行过程中应测试哪些比较器

注释： 集成商必须确保位 ABIST_SELECT1.BSTIUV 设置为 0，特别是在开始任何 ABIST 操作之前，以防报告 BSTI UV 错误

ABIST 执行结束后：

1. 发出中断
2. 检查 ABIST_CTRL0.START 是否 = 0
3. ABIST 无错误：ABIST_CTRL0.STATUS = 0x5
4. ABIST 有错误：ABIST_CTRL0.STATUS = 0xA
5. 读取 ABIST_SELECT0/1/2：
   - 0：比较器完好无损
   - 1：比较器测试失败

10.7.5 ABIST - 测试次级关断路径逻辑

除了上述描述的比较器测试外，该设备还提供直接触发并由此测试次级关断路径激活的选项。这可以分别针对每个 SSO1/2 执行，并在写入寄存器 ABIST_CTRL1 后立即应用。

可通过写入 ABIST_CTRL1 应用以下测试：

- OV_1V5_TRIG：在次级关断路径逻辑的内部 1.5 V 电源上强制施加过压
  - 预期结果：SSO1/2 必须激活（拉低）
- ABIST_CLK_EN：启用 SSOx 反应的内部时钟信号
  - 必须与 ABIST_CTRL1 中的其他位结合使用。更多信息请参考《安全手册》。
- SS1_EN_BIST：仅中断 SS1 的安全时钟信号
  - 预期结果：SSO1 必须激活（拉低）
- SS2_EN_BIST：仅为 SS2 中断安全时钟信号
  - 预期结果：SSO2 必须激活（拉低）

11 中断功能（INT）

11.1 介绍

中断模块用于通知微控制器，器件已检测到系统事件。这是向微控制器发出的对器件进行诊断的请求。

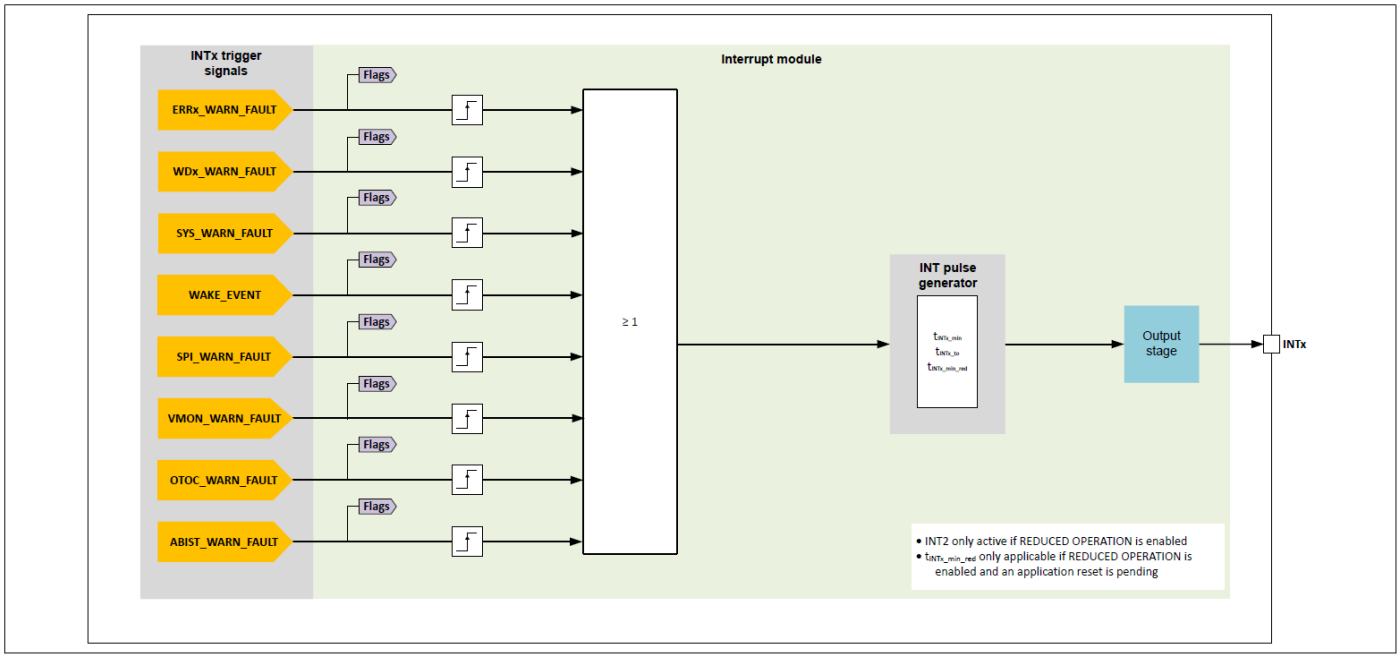


图 68 中断功能的功能框图

中断模块提供两个中断通道。

一般事件报告在 INT1 上。如果启用 REDUCED OPERATION，则 INT1 和 INT2 还会针对其特定于应用程的错误情况进行额外激活（参见故障反应） 。

每个中断引脚 INTx（x = 1 或 2）都是一个推挽级。

该器件可配置用于单一应用或双应用场景。

单一应用案例（默认配置）：

在这种情况下，任何中断触发信号检测都会激活输出引脚 INT1 上的中断。

双应用案例：

双应用案例可通过 SPI 激活，方法是将 **REDOP_PW_CFG1.EN** 位设置为 1。

在这种情况下（参见故障反应）：

- 检测到应用 1 上的中断触发信号后，会激活输出引脚 INT1 上的中断
- 检测到应用 2 上的中断触发信号后，会激活输出引脚 INT2 上的中断
- 一般事件的检测结果会同时报告给中断线 INT1 和 INT2
- 如果 SPI 位 **REDOP_RS_CFG1.INT2_DIS** 设置为 0（条件：器件必须处于 NORMAL 或 REDUCED OPERATION 状态），则在应用 1 上检测到严重故障（**WD1_SEV_FAULT 或 ERR1_SEV_FAULT**） 在应用 2 上激活中断
- 如果 SPI 位 **REDOP_RS_CFG1.INT1_DIS** 设置为 0（条件：器件必须处于 NORMAL 或 REDUCED OPERATION 状态），则在应用 2 上检测到严重故障 （**WD2_SEV_FAULT 或 ERR2_SEV_FAULT**） 在应用 1 上激活中断

11.2 中断激活

中断引脚默认输出值为逻辑高电平（无中断挂起）。器件通过将相关中断引脚设置为“低”来激活中断。

中断引脚变为非激活（中断信号从“低”转变为“高”）后，必须经过最小激活时间 t_{INTx_to}，然后新的中断请求才能重新激活引脚。t_{INTx_to} 时间从中断引脚的下一个上升沿开始。

中断的发生会被锁存到状态寄存器中，在排除故障后，可以通过 SPI 的写入命令读取和清除该状态寄存器。

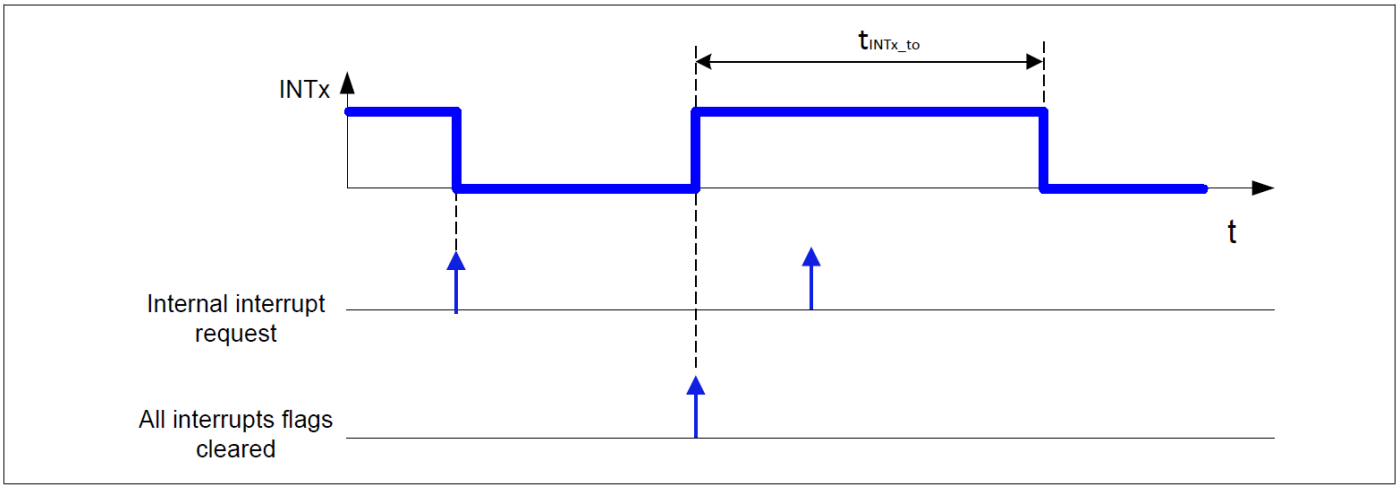


图 69 中断引脚 INTx 的激活（置位中断引脚为逻辑低）

11.3 中断停用

在下列情况下，中断将被停用，置位将被置为逻辑“高”：

- 如果在最小中断脉冲宽度 t_{INTx_min} 之后且在 t_{INTx_to} 过期之前清除所有专用中断标志（参见图“通过清理所有专用中断标志来停用中断”）。
- 如果 t_{INTx_min} 超时，并且所有中断标志都已及时清除（参见图“如果中断标志被过早清除，则中断通过最小脉冲宽度停用”）
- 如果 $t_{INTx\_min\_red}$ 过期并且在应用复位待处理时启用了 REDUCED OPERATION
- 如果 t_{INTx_to}超时且并非所有中断标志都已及时清除（参见图“如果中断标志清除过晚，则通过 t_{INTx_to} 停用中断”）。在这种情况下，检测到缺失的中断，位 **IFx.INTMISS** 被置位，可通过 SPI 清除

(x=1,2)

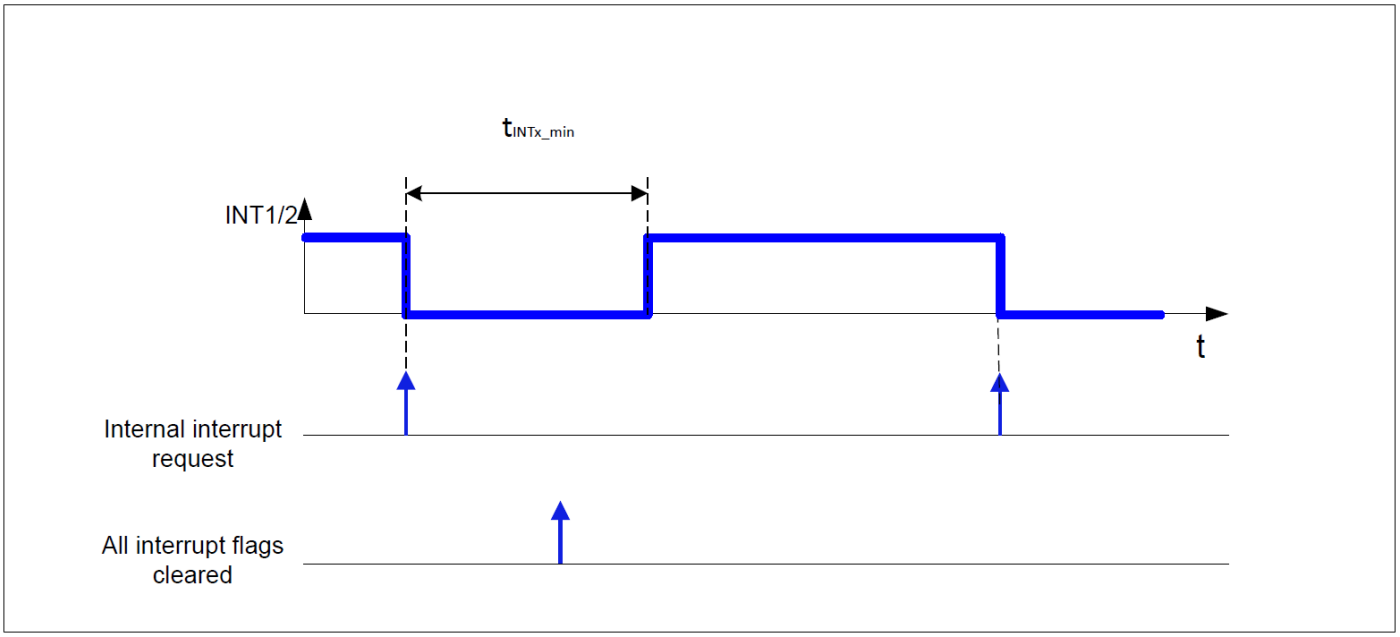


图 70 如果中断标志在 t_{INTx_min} 过期之前被清除，则中断将按最小脉冲宽度停用

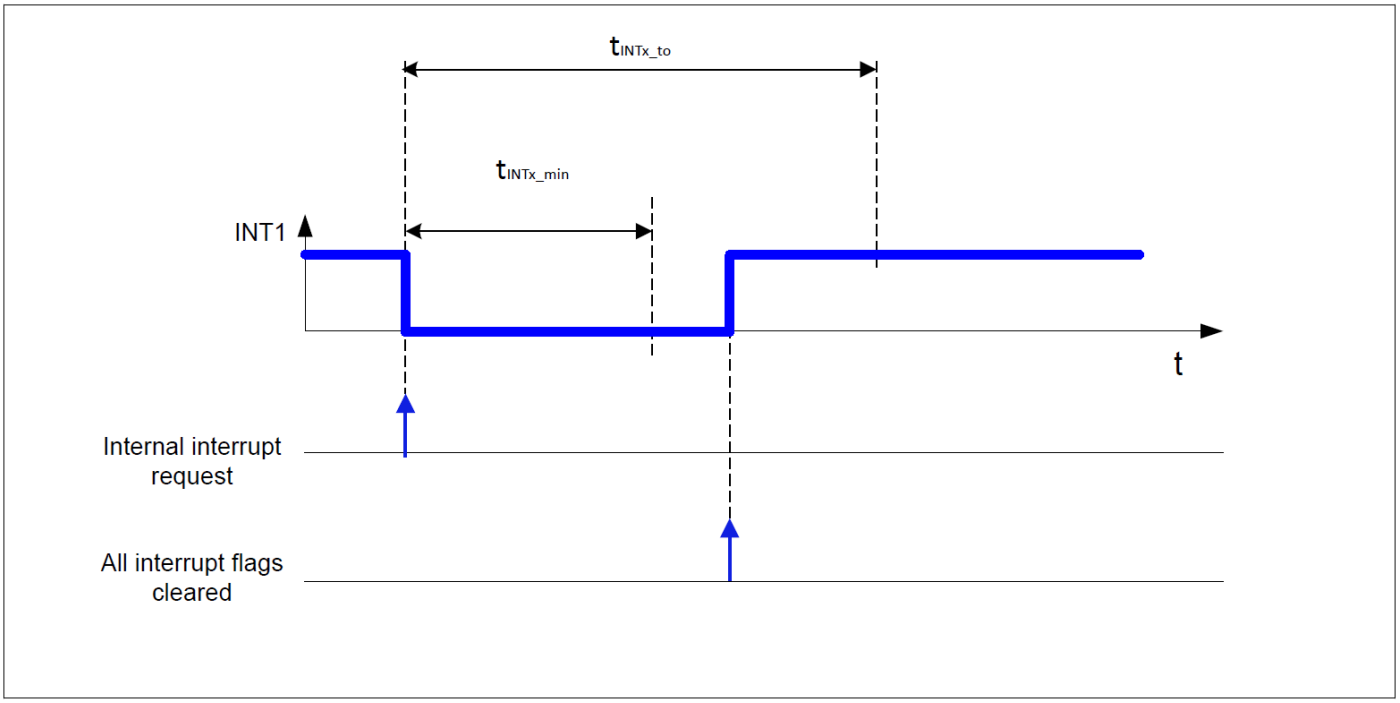


图 71 通过清除所有专用中断标志来停用中断

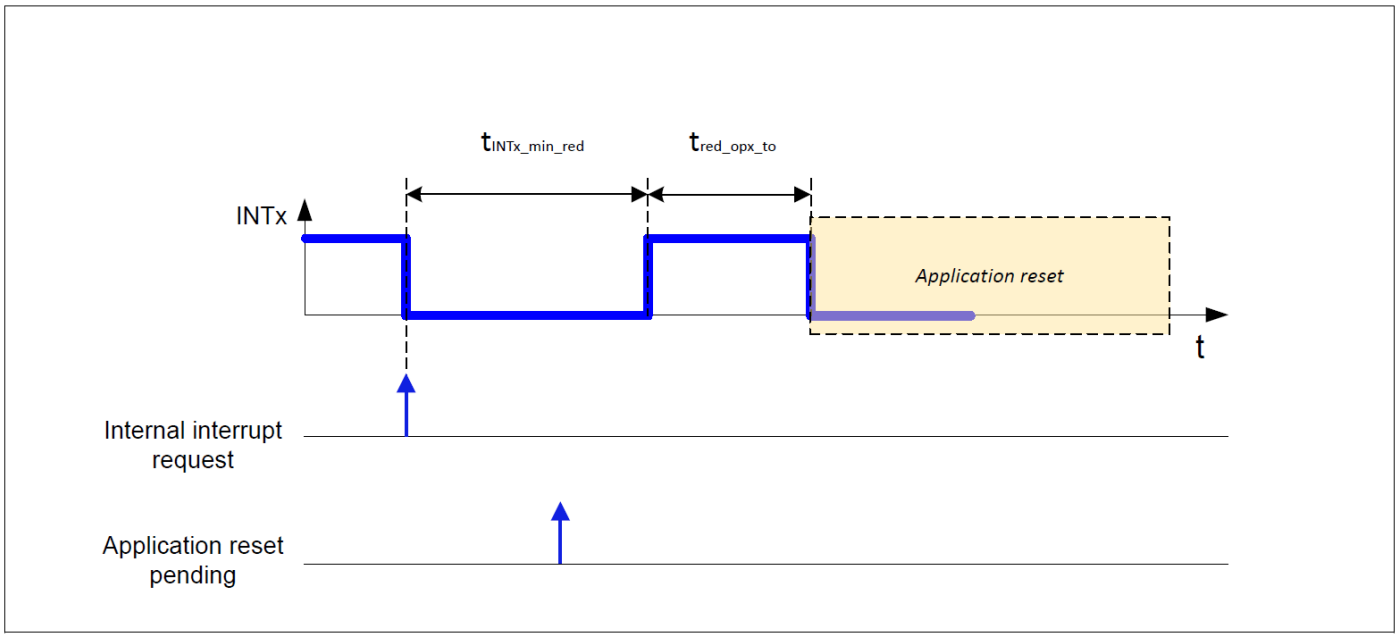


图 72 由于待处理的应用复位而停用中断

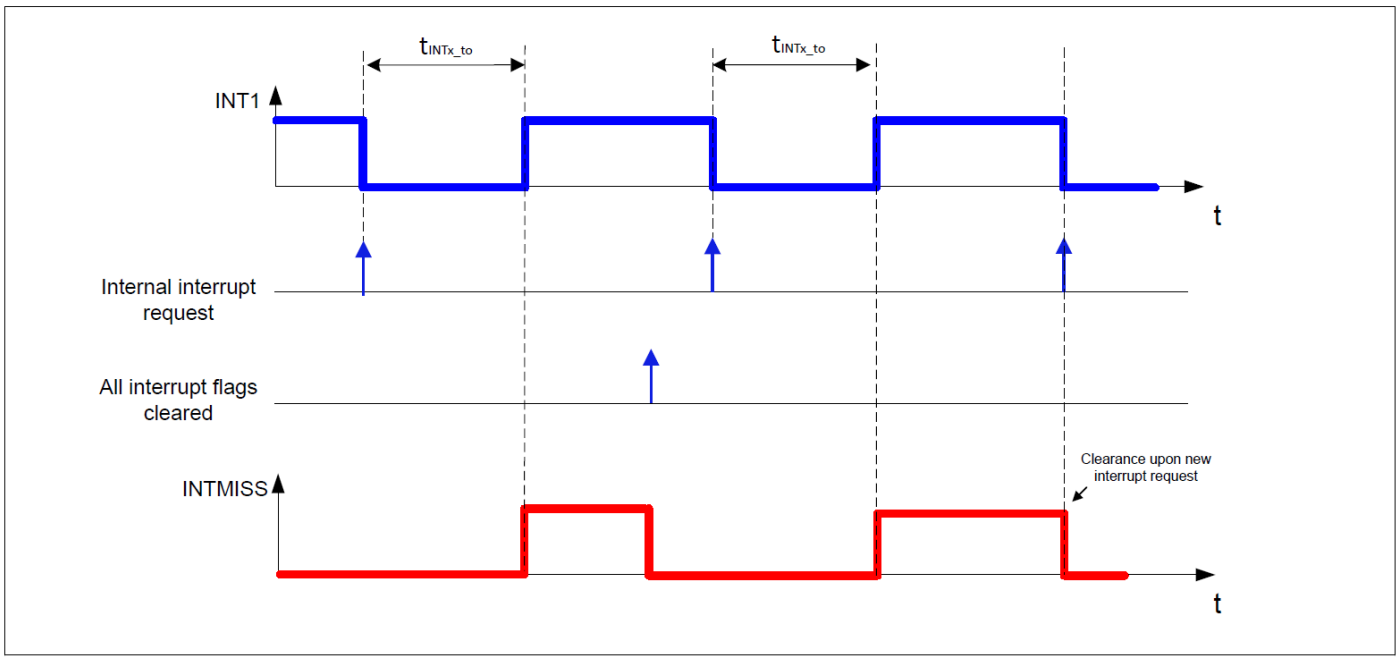


图 73 丢失中断（如果中断标志清除过晚，则通过超时 (t_{INTx_to}) 停用中断）

11.4 电气特性：中断（INT）

表 44 电气特性：中断（INT）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage high level	V_{INT_H}	2	–	–	V	$V_{QUC} \geq V_{QUC}$[Min]; I_{INT} = -7 mA; Parameter applicable to INT1 and SYNC_IN/INT2	DS-1642
Output voltage low level	V_{INT_L}	–	–	0.7	V	I_{INT} = 5.5 mA; Parameter applicable to INT1 and SYNC_IN/INT2	DS-1643
Pin output rise time	t_{INT_RISE}	–	–	25	ns	$C_{INT,load}$ = 50 pF[1)]	DS-1644
Pin output fall time	t_{INT_FALL}	–	–	25	ns	$C_{INT,load}$ = 50 pF[1)]	DS-1645
Minimum interrupt pulse width for single application use case	t_{INTx_min}	90	100	150	µs	[1)]	DS-1646
Interrupt pulse timeout	t_{INTx_to}	270	300	350	µs	[1)]	DS-1647
Minimum interrupt pulse width for dual application used case - application reset pending	$t_{INTx\_min\_red}$	50	55	60	µs	[1)]	DS-1649

1) 未经过生产测试，由设计指定

12 复位功能（RESOUT）

12.1 功能描述：复位功能（RESOUT）

12.1.1 介绍

复位模块用于根据配置和复位来源对一组应用（应用复位）或整个系统（系统复位）进行复位。仅当 REDUCED OPERATION 启用时，应用复位才是激活的。

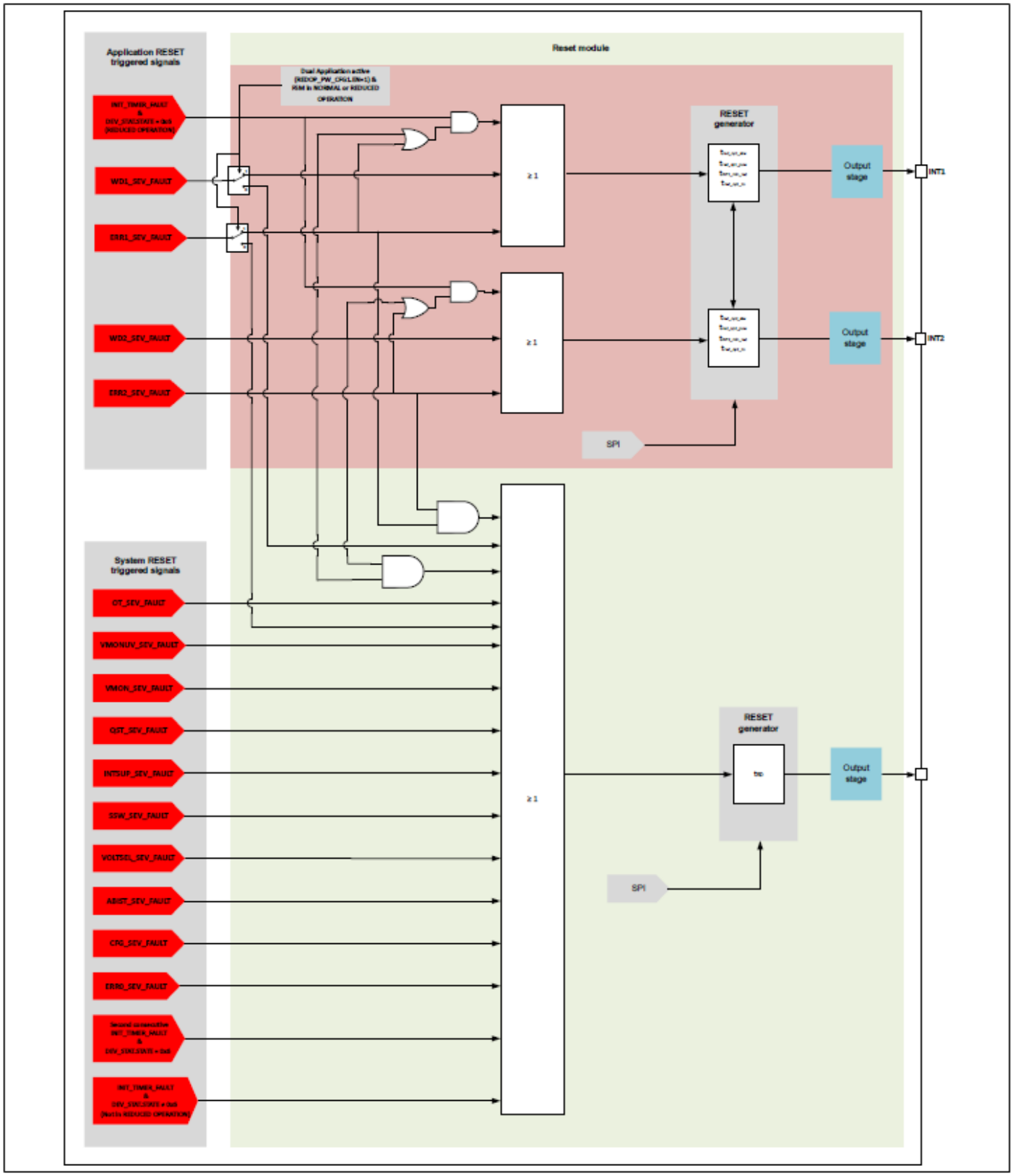


图 74 复位功能的功能框图

复位模块提供以下复位通道：

- 应用复位有两个通道。如果在相关应用上检测到应用复位触发信号，则在输出引脚 INTx（x = 1 或 2）上激活应用复位（仅适用于双应用场景（位 **REDOP_PW_CFG1.EN** = 1））
- 单通道用于系统复位。如果满足以下条件，则在输出引脚 RESOUT 上激活系统复位：
  - 检测到系统复位触发信号
  - 在两个应用上都检测到应用复位触发信号（仅对双应用案例 **REDOP_PW_CFG1.EN** = 1 有效）

12.1.2 应用复位（REDUCED OPERATION ENABLE）

12.1.2.1 激活

如果在相应的应用上检测到以下应用复位触发信号之一，则器件通过在相关中断引脚（INTx）上生成“低”脉冲来激活应用复位：

- WD 或 ERRx 监测严重故障（WDx_SEV_FAULT 或 ERRx_SEV_FAULT），请参阅应用复位激活
- 当器件处于 REDUCED OPERATION 状态 (SPI 位字段 **DEV_STAT.STATE = 0x6**) 时，INIT 计时器一旦过期(INIT_TIMER_FAULT)，请参阅 INIT 计时器故障应用复位激活。

脉冲长度（$t_{red\_opx\_puw}$）的持续时间可通过 SPI 进行配置，并可使用以下公式计算：

	Calculation	$t_{red\_opx\_stw}$	STEP
Pulse type 1 (default):	$t_{red\_opx\_puw}$ = STEP × $t_{red\_opx\_stw}$	10 µs (TYP)	1 ... 8
Pulse type 2:	$t_{red\_opx\_puw}$ = STEP × $t_{red\_opx\_stw}$;	100 µs (TYP)	1 ... 8

$t_{red\_opx\_stw}$ 可以通过 SPI 位 **REDOP_RS_CFG2.REDOP_RESOUT_APP_TB** 配置，默认值为 10 µs，STEP 可以通过 SPI 位 **REDOP_RS_CFG2.REDOP_RESOUT_APPx_DUR** 设置。

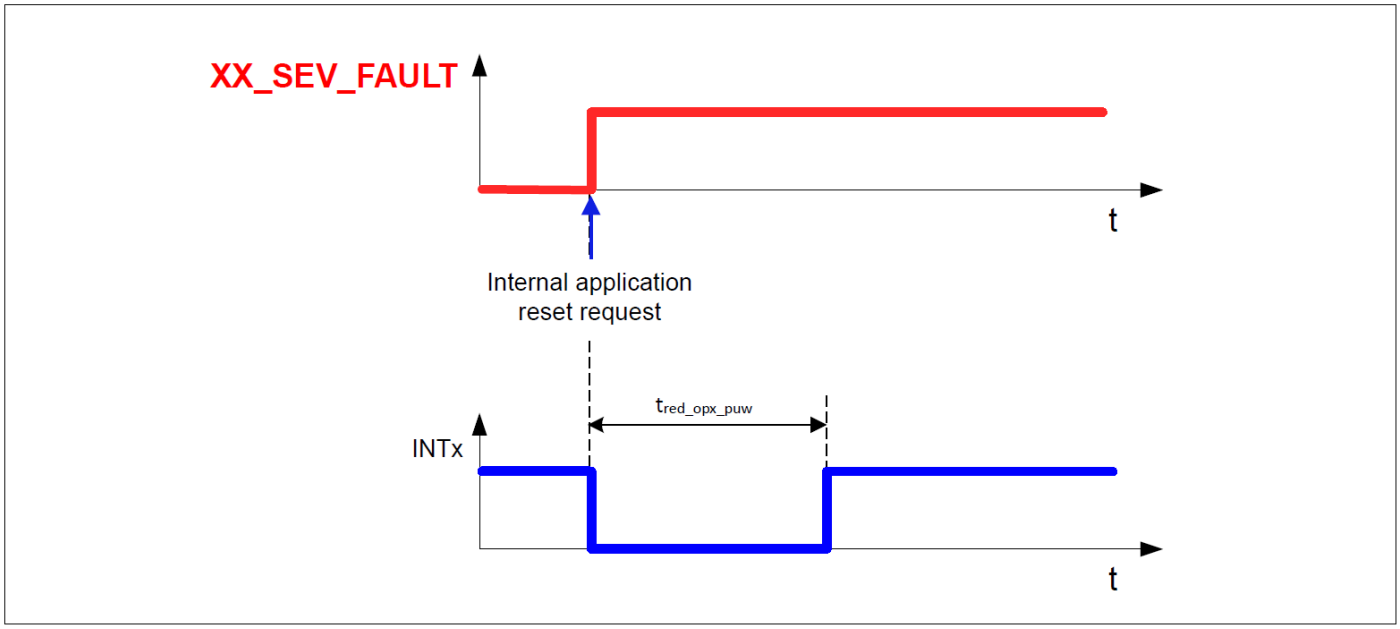


图 75 由于严重故障导致应用复位激活
（xx：ERR1/2 或 WD1/2 或 INIT 计时器超时，并伴有模块 ERR1/2 或 WD1/2 之一）

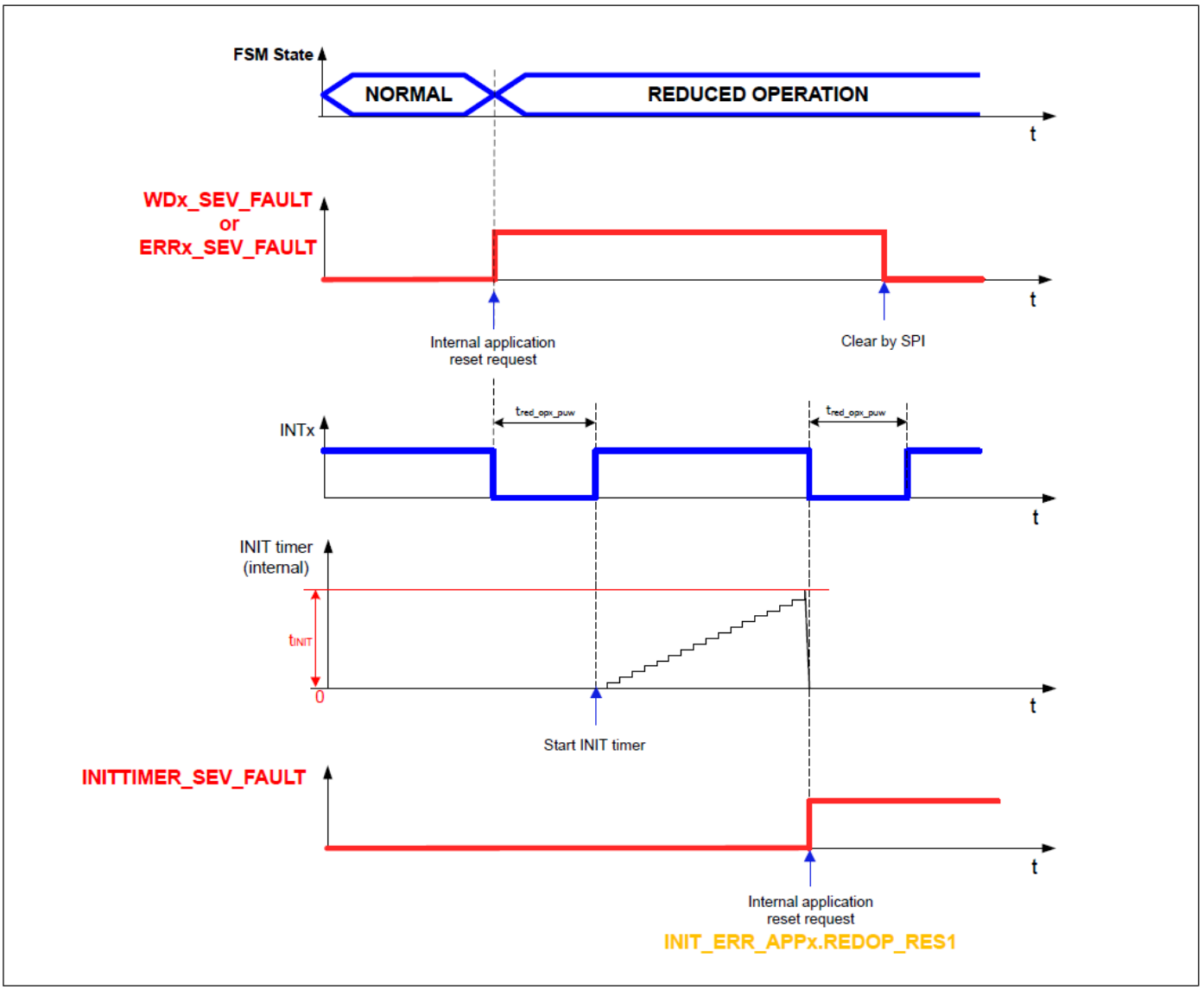


图 76　　由于 INIT_TIMER_FAULT 导致应用复位激活

(x = 1; 2)

如果在中断激活时应用复位被激活，则器件将依次执行以下操作：

1. 等待最小中断脉冲宽度 $t_{INTx\_min\_red}$
2. 释放中断线并等待 $t_{red\_opx\_to}$
3. 生成具有可配置宽度 $t_{red\_opx\_puw}$ 的中断脉冲

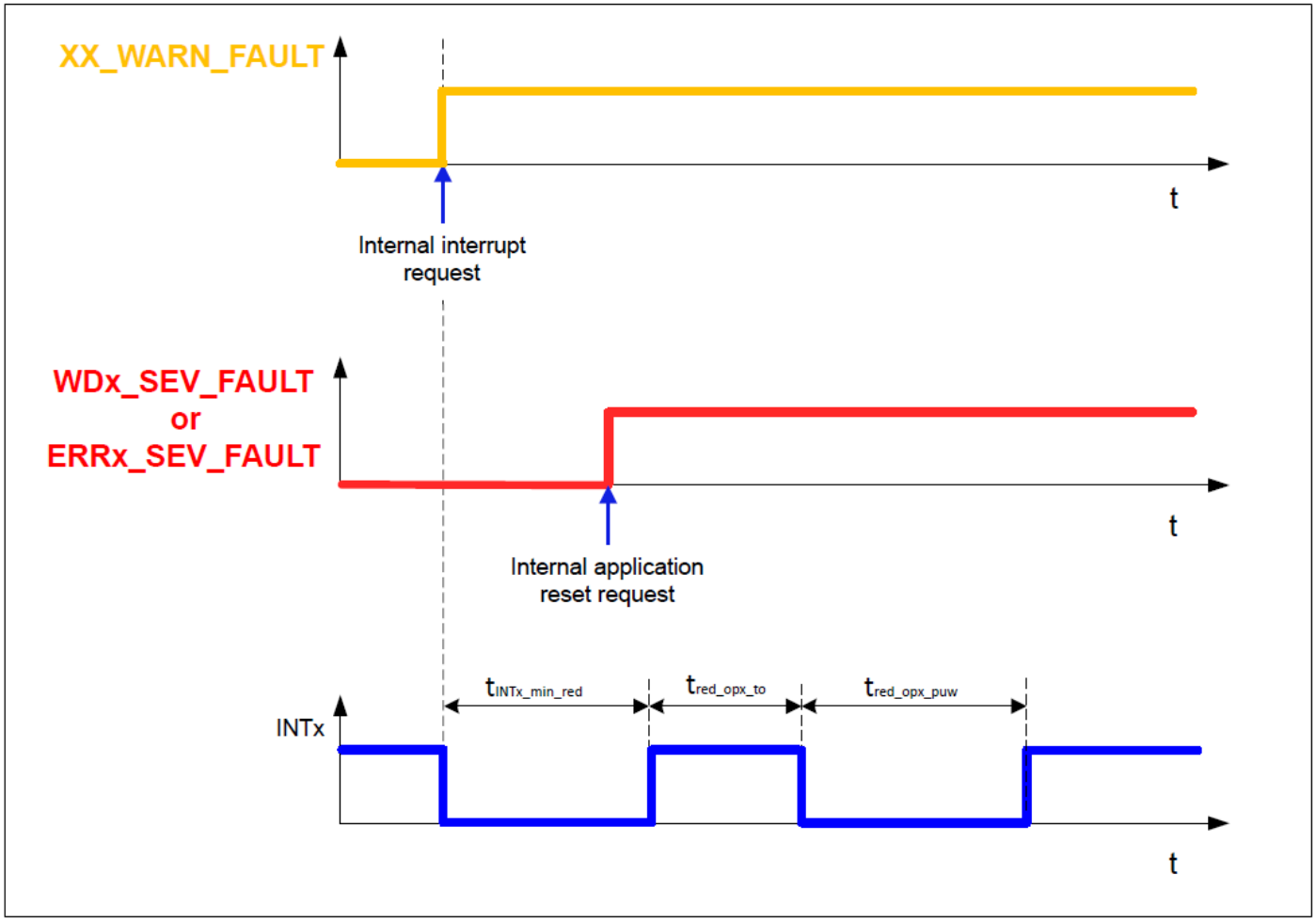


图 77　　中断激活时的应用复位激活

如果 INIT 计时器在 REDUCED OPERATION 状态下过期**一次**，则器件：

- 生成 INIT_TIMER_FAULT，
- 激活一个新的应用复位，
- 设置位 **INIT_ERR_APPx.REDOP_RES1**；故障消除后可通过 SPI 清除该位。
- 仍处于 REDUCED OPERATION

如果在 REDUCED OPERATION 状态下 INIT 计时器过期**两次**，则器件

- 生成一个 INIT_TIMER_FAULT
- 激活系统复位
- 设置错误位 **INIT_ERR_APP1.REDOP_RES2** 和 **INIT_ERR_APP2.REDOP_RES2**；故障消除后可通过 SPI 清除这些错误位。
- 进入 INIT 状态，请参见第 9 章。

12.1.3　　系统复位

12.1.3.1　　激活

复位输出引脚 RESOUT 为开漏结构。内部上拉电流 (I_{RESOUT_PU}) 将输出拉向 V_{QUC}。一旦发生系统复位条件，器件就会通过将引脚 RESOUT 拉至低于 V_{RESOUT_LOW} 来触发复位。

可以在 RESOUT 和 V_{QUC} 引脚之间连接一个额外的外部上拉电阻， 以加快低电平到高电平的转换速度。

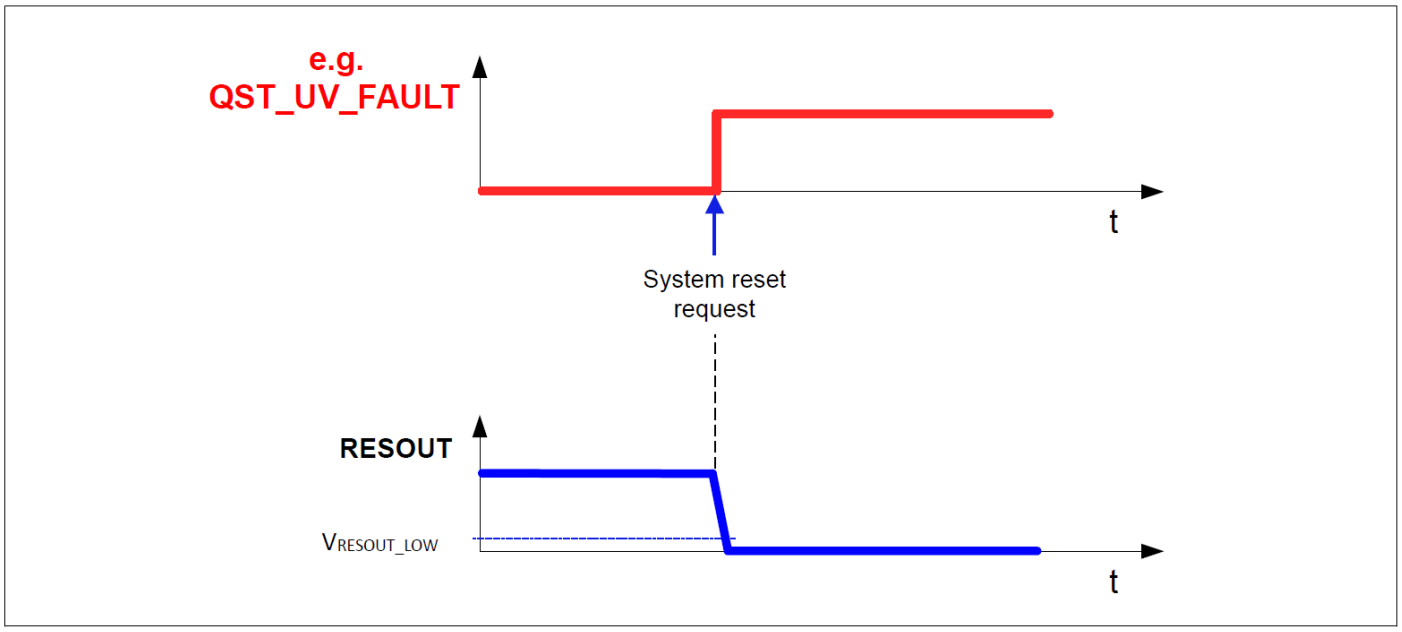


图 78 系统复位激活

12.1.3.2 硬复位和软复位

定义

根据检测到的系统故障，器件在进入 INIT 状态后生成**“软复位”（WARM RESET）**或**“硬复位”（COLD RESET）**，请参见第 9 章。

- 如果引脚 RESOUT 低于 V_{RESOUT_LOW}，但调节器输出电压（包括前置和后置调节器输出电压）没有关闭，则称为**“软复位”**。
- 如果引脚 RESOUT 低于 V_{RESOUT_LOW} 且所有调节器输出电压均关闭，则称为**“硬复位”**。

如果 INIT 计时器在 INIT 或 WAKE 状态下过期**一次**，则器件：

- 激活软复位
- 生成一个 INIT_TIMER_FAULT
- 设置位 **INIT_ERR_APPx.SOFTRES**；该位可通过 SPI 清除
- 进入 INIT 状态，参见第 9 章

如果 INIT 计时器在 INIT 状态下连续过期**第二次**，则器件

- 激活硬复位，所有调节器输出电压均关闭
- 生成 INIT_TIMER_FAULT
- 设置故障位 **INIT_ERR_APPx.HARDRES**；排除故障后可通过 SPI 清除
- 进入 INIT 状态，参见第 9 章

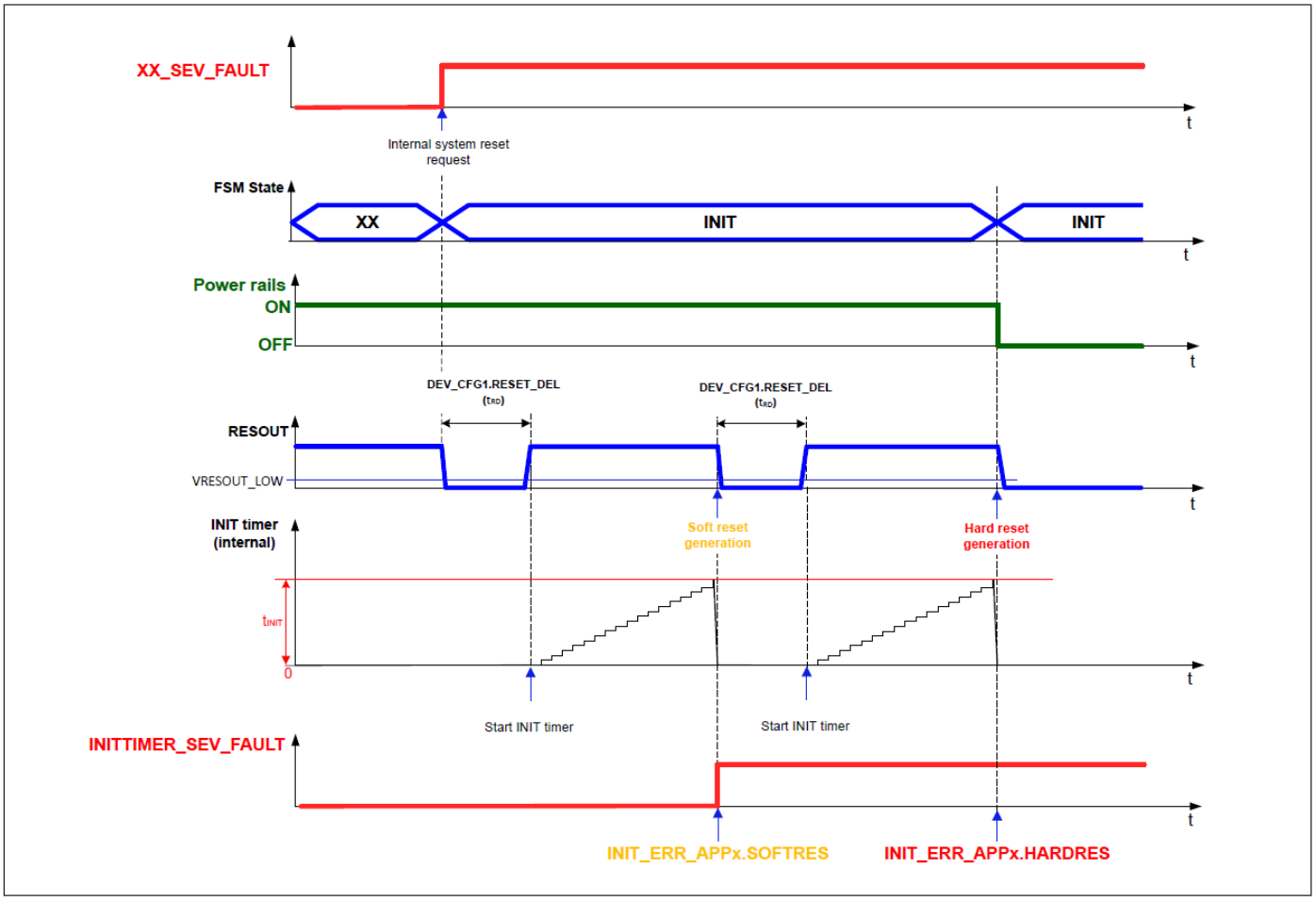


图 79　　软、硬复位激活信号图

复位释放

生成软复位后，器件会在复位延迟时间 (t_{RD}) 后通过将输出引脚 RESOUT 设置为“高”来释放复位。

硬复位生成后，器件会等待 QST、QUC 和 BUCKCORE 在上电序列方案 A 或上电序列方案 B 中达到其欠压阈值。只有当此成功时，器件：

1. 等待复位延迟时间 t_{RD}
2. 将输出引脚 RESOUT 设置为“高”

复位延迟时间配置

当从 POWERDOWN 或 STANDBY 启动且 WUT 和 QST 禁用时，复位延迟时间的默认值可由硬件设置，请参见 HWCFG。

复位延迟时间 t_{RD} 可在运行时在寄存器 **DEV_CFG1.RESET_DEL** 中配置。

12.2 电气特性：复位功能（RESOUT）

表 45 电气特性：复位功能（RESOUT）

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RESOUT start up delay time 2ms	t_{RD_2ms}	1.8	2	2.2	ms	RESOUT start up delay time is set to 2ms by HWCFG 1)	DS-1539
RESOUT start up delay time 10ms	t_{RD_10ms}	9	10	11	ms	RESOUT start up delay time is set to 10ms by HWCFG 1)	DS-1540
Pull-up current	I_{RESOUT_PU}	-180	-55	-15	µA	$V_{RESOUT} \leq 2.0$ V	DS-2131
Low level	V_{RESOUT_LOW}	–	–	0.4	V	$V_{QUC} = V_{QUC}$ [Typ]; I_{RESOUT} = 3.5 mA	DS-1558
REDUCED OPERATION configurable reset step (default)	$t_{red\_opx\_stw}$	9	10	11	µs	Default configuration 1)	DS-1648
REDUCED OPERATION reset timeout	$t_{red\_opx\_to}$	9	10	11	µs	1)	DS-1650
Output fall time	t_{RESOUT_FALL}	–	–	25	ns	$C_{RESOUT,load}$ = 50 pF 1)	DS-1559

1) 未经过生产测试，由设计指定

13 微控制器编程支持（MPS）

该器件包含微控制器编程支持（MPS）功能，在该功能期间，以下事件将被屏蔽：

- 由于 ERR1/2 引脚监测反应而导致的 MCU 复位事件（RESOUT）
- 由于看门狗反应而导致的 MCU 复位事件（RESOUT）
- 由于所有 INIT 计时器（包括 REDUCED OPERATION）过期反应（INIT 计时器停止或未启动）而导致的 MCU 复位事件（RESOUT）
- 由于 ERR0 引脚监测反应而转变为 FAILSAFE。如果触发了 ERR0，器件将进入 INIT 状态，而不会产生任何触发事件。

例如，这样就可以不间断地对 µC 进行编程。

注释： *所有其他故障都会生成各自的响应，并且器件的其他行为保持不变。*

可以配置 MPS 模式：

- 通过硬件，按照 HWCFG 表中的描述设置相应的电阻值。
  - MPS 模式选择仅在完成一次功率循环后才会刷新。
- 通过 SPI 指令
  - MPS 模式可以在所有 FSM 模式下启用或禁用（**DEV_CFG1.MPS_EN**）。

14 SPI

串行外设接口（SPI）是器件和微控制器之间的通信链路，支持全双工模式下的多从机操作，具有 32 位数据访问。数据传输以 MSB 开始。时钟极性（CPOL）为 0，时钟相位（CPHA）为 1。

SPI 使用 4 个接口信号进行同步和数据传输：

- CSN：SPI 片选（低电平有效）
- SCK：SPI 时钟
- SDI：SPI 数据输入
- SDO：SPI 数据输出

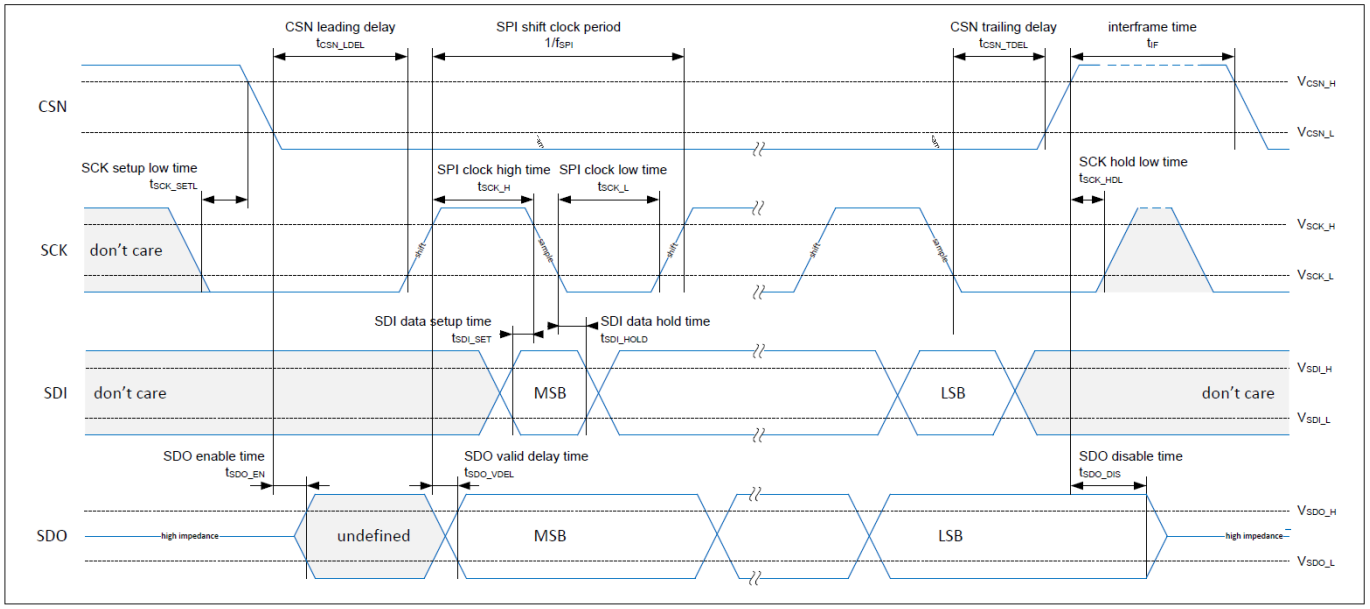


图 80 SPI 信号

14.1 功能描述：SPI

14.1.1 SPI 数据传输

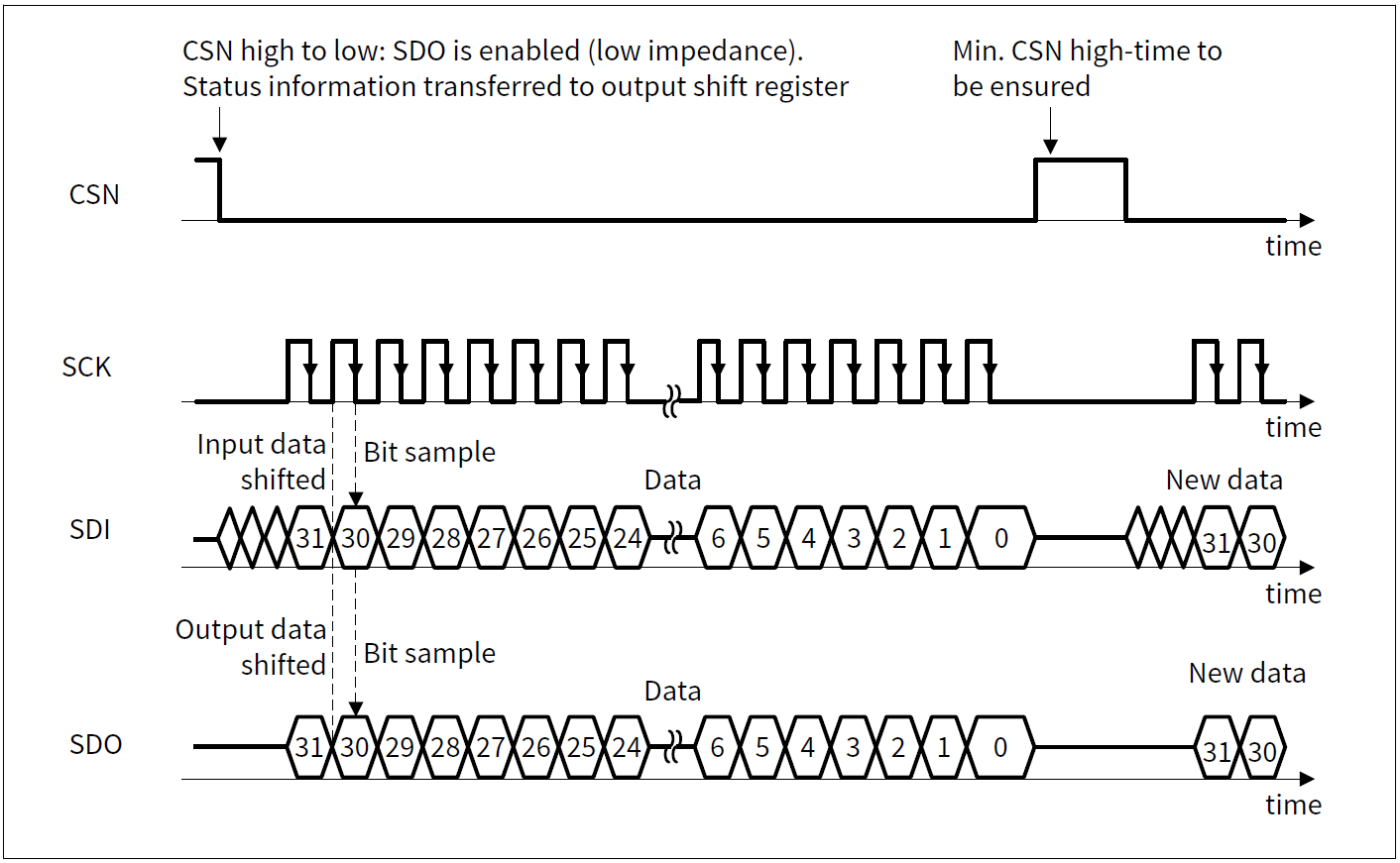


图 81 SPI 数据传输

当通过将 CSN 引脚设置为“低”来选择器件时， SPI 传输开始。在每个 SCK 上升沿上，数据先移入 SDI（MSB 优先），然后分别移出 SDO（MSB 优先）。SDI 上的数据在 SCK 的每个下降沿进行采样。SPI 传输通过检测 CSN 处的“高”信号而终止。当 CSN 处于“高”电平时，SDO 处于高阻态。

SPI 不支持菊花链连接。

14.1.2 SPI 帧格式

以下部分定义了 SPI 帧格式并定义了 SPI 服务。

14.1.2.1 SPI 传输

SPI 传输由以下帧组成：

- SDI 帧
- SDO 帧

经过 32 个移位时钟周期后，器件已接收到 SDI 帧，主机（微控制器）已接收到 SDO 帧。图 82 展示了 SPI 传输的结构。

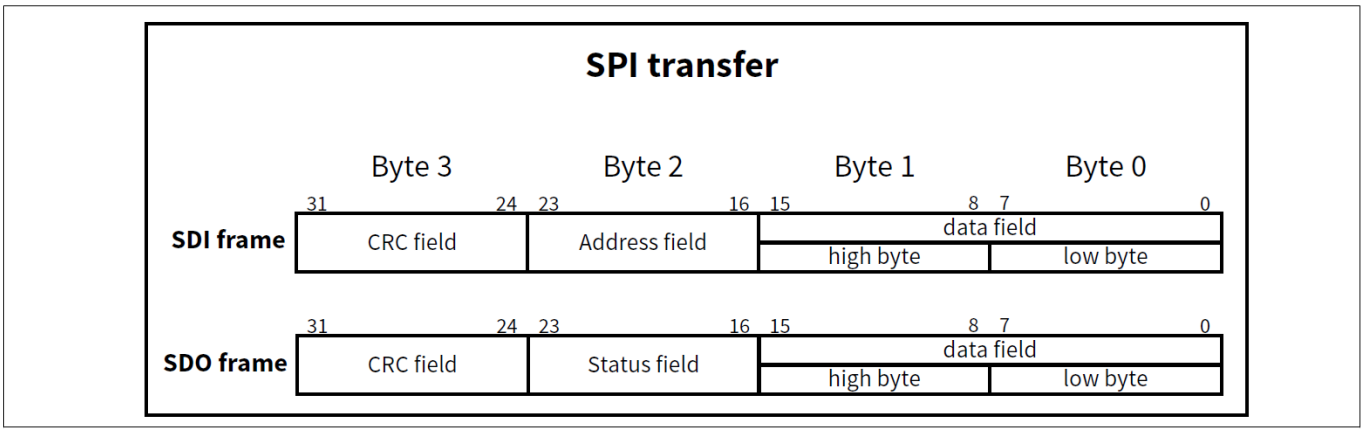


图 82　　SPI 传输结构

14.1.2.2　SPI 服务

SPI 服务可以是写入服务或读取服务，由两次 SPI 传输组成。第一次 SPI 传输（请求）包含主机（微控制器）发送给器件的 SDI 帧中的请求信息。第一次 SPI 传输（请求）的 SDO 帧包含前一次服务的响应信息，与目前服务无关。第二次 SPI 传输（响应）包含 SDO 帧中的响应信息。SDI 帧包含下一次服务的请求信息，与目前的服务无关。图 83 展示了 SPI 服务的结构。

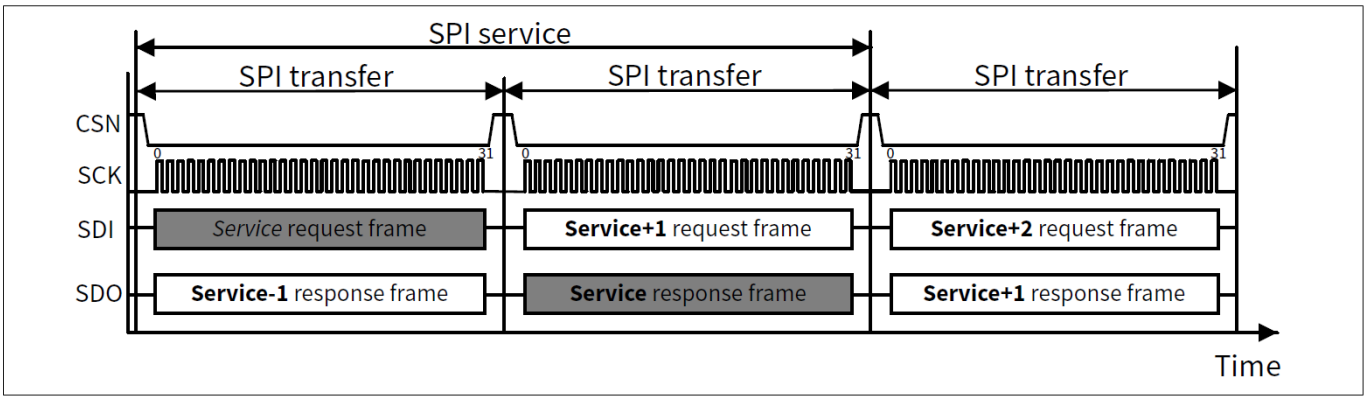


图 83　　SPI 服务和传输定义

14.1.2.3　SPI 读取服务

读取服务包含两次 SPI 传输（请求 SPI 传输和响应 SPI 传输）。图 84 展示了读取服务的结构。

请求 SPI 传输 SDI 帧

- CRC 字段：CRC 值的计算过程详见章节 14.1.2.5
- 地址字段：地址字段的值必须为 FF_H，该值定义为一个读取服务。
- 数据字段：数据字段包含要读取的寄存器的地址。

响应 SPI 传输 SDO 帧

- CRC 字段：CRC 值的计算过程详见章节 14.1.2.5
- 状态字段：状态字段说明详见章节 14.1.2.6
- 数据字段：数据字段包含在请求 SPI 传输 SDI 帧中寻址的寄存器的值

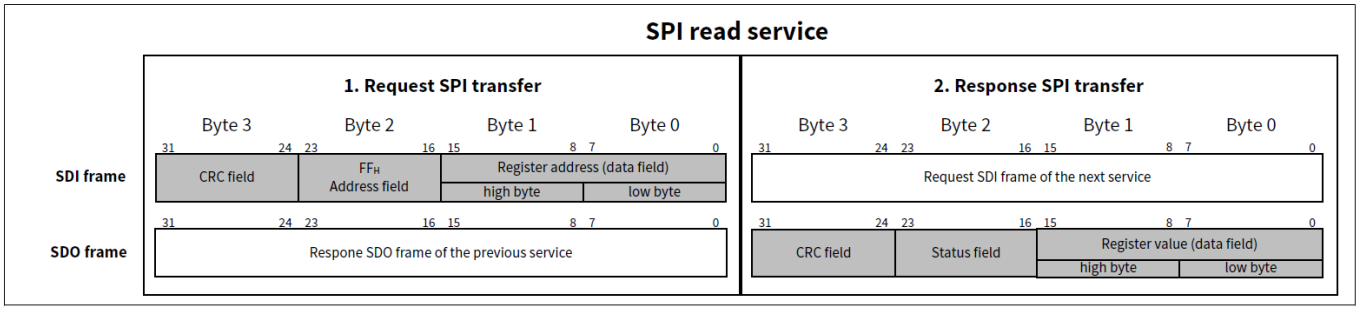


图 84　　读取服务的结构

14.1.2.4　SPI 写入服务

写入服务包含两次 SPI 传输（请求 SPI 传输和响应 SPI 传输）。图 85 展示了读取服务的结构。

请求 SPI 传输 SDI 帧

- CRC 字段：CRC 值的计算过程详见章节 14.1.2.5
- 地址字段：地址字段包含应写入的寄存器的地址
- 数据字段：数据字段包含应写入寄存器的值。

响应 SPI 传输 SDO 帧

- CRC 字段：CRC 值的计算过程详见章节 14.1.2.5
- 状态字段：状态字段说明详见章节 14.1.2.6
- 数据字段：数据字段包含寄存器写入后的新值。

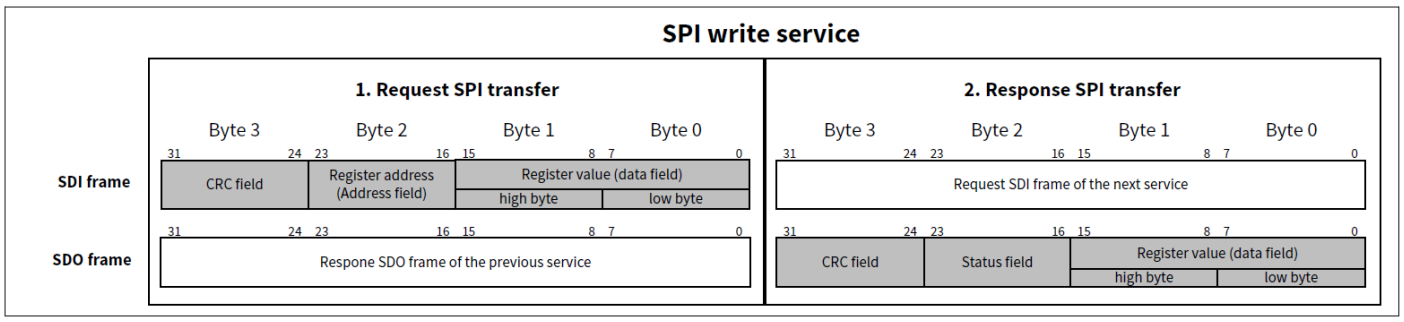


图 85　　SPI 写入服务的结构

14.1.2.5　CRC 字段

本章从微控制器和器件的角度描述了 CRC 计算。CRC 计算采用 SAE J1850 标准的 CRC8。

CRC8 计算和算法的数学背景在 CRC AUTOSAR 规范版本 4.3.1 中有所描述。以下 C# 示例代码解释了计算 CRC8 的算法。

```
Byte crc8(Byte[] data ,uint length) {
    Byte crc;
    uint i,bit;

    //Inital value must be 0xFF
    crc = 0xFF;
    for ( i=0 ; i<length ; i++ ) {
        crc ^= data[i];
        for ( bit=0 ; bit<8 ; bit++ ) {
            if ( (crc & 0x80)!=0 ) {
                crc <<= 1;
                crc ^= 0x1D;  //Polynomial is 0x1D
            }
            else {
                crc <<= 1;
            }
        }
    }

    return (Byte)~crc;
}
```

微控制器计算 SDI 帧中的 CRC（参见章节），并且必须检查 SDO 帧中的 CRC（参见章节）。

器件计算 SDO 帧中的 CRC（参见章节），并且必须检查 SDI 帧中的 CRC（参见章节）。

14.1.2.5.1 CRC 微控制器处理

CRC 计算

CRC 计算包括以下 SDI 帧元素（图 86）：

- 数据字段低位字节
- 数据字段高位字节
- 地址字段

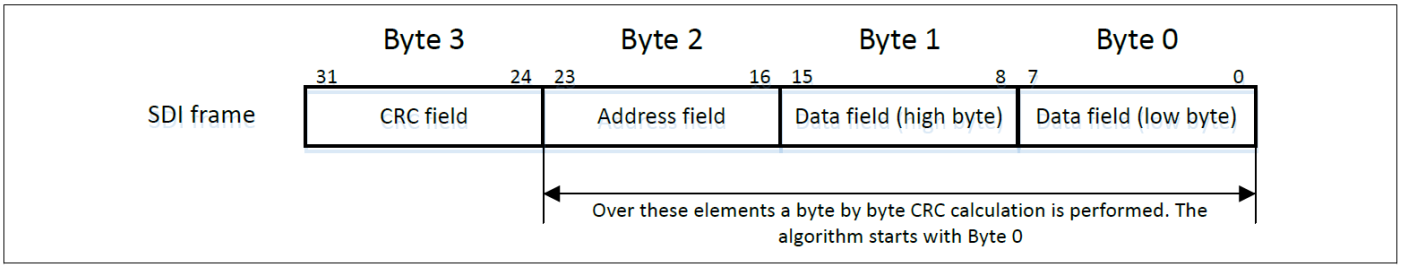


图 86 字节 SAE J1850 CRC 计算的字节顺序

为了将寄存器值 $01F2_H$ 写入寄存器地址 83_H，CRC 算法（参见第 14.1.2.5 章）需要以下输入参数：

14 SPI

- 输入字节域参数数据：{$F2_H$, 01_H, 83_H}
- 输入参数长度：3

CRC 计算的结果是 37_H。必须从微控制器发送的 SDI 帧如图 87 所示。

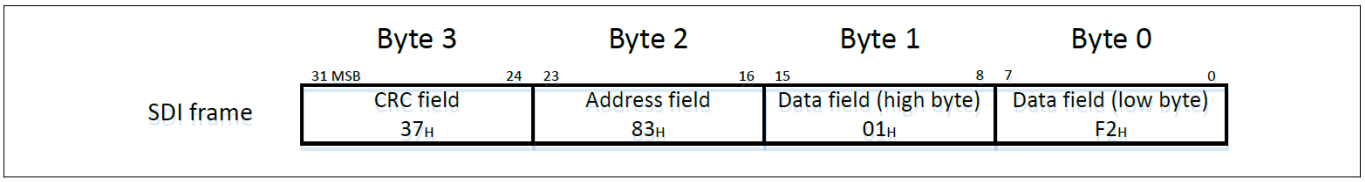


图 87　　SDI 帧示例

CRC 检查

CRC 检查包括以下 SDO 帧元素（图 88）：

- 数据字段低位字节
- 数据字段高位字节
- 状态字段
- CRC 字段

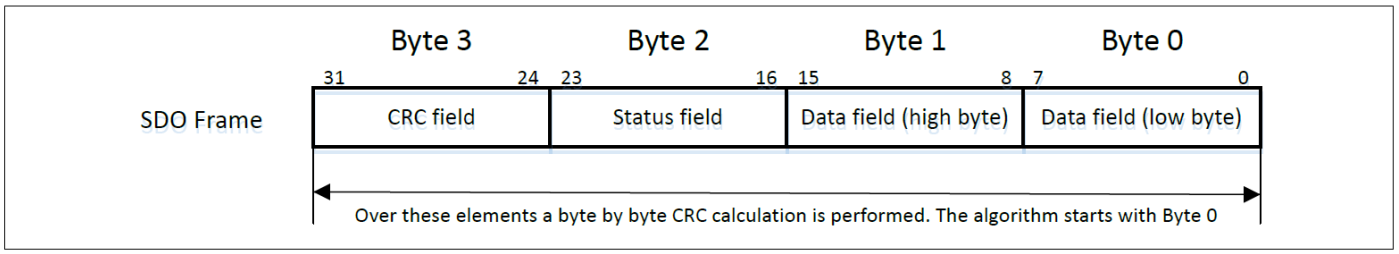


图 88　　SAE J1850 CRC 检查的字节顺序

示例：

如果微控制器接收到图 89 中的帧，则 CRC 算法（参见第 14.1.2.5 章）需要以下输入参数：

- 输入字节域参数数据：{$F2_H$, 01_H, 83_H, 37_H}
- 输入参数长度：4

CRC 检查的结果必须始终为 $3B_H$。任何其他值都意味着帧已损坏。值 $3B_H$ 在AUTOSAR CRC 规范中被称为魔力数。

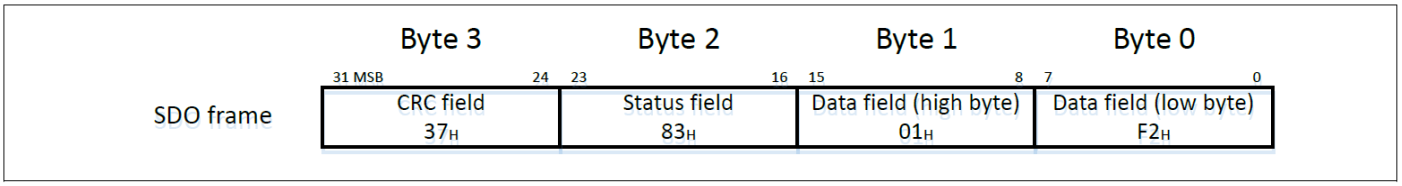


图 89　　SDO 框架示例

14.1.2.5.2　CRC 器件处理

CRC 计算

CRC 计算包括以下 SDO 帧元素（图 90）：

- 数据字段低位字节
- 数据字段高位字节
- 状态字段

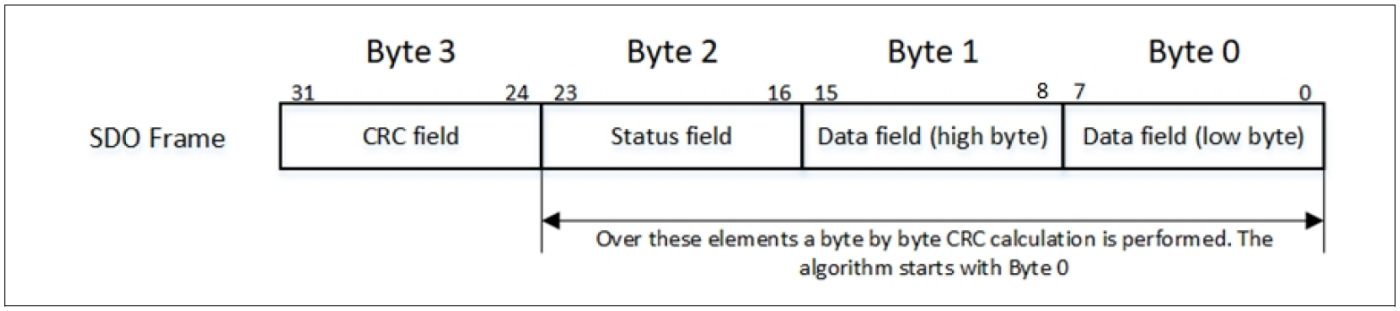


图 90　　SAE J1850 CRC 计算的字节顺序

如果状态字段的值为 83_H 并且数据字段的值为 $01F2_H$，则 CRC 算法（请参阅章节 14.1.2.5）需要以下输入参数：

- 输入字节域参数数据：{$F2_H$, 01_H, 83_H}
- 输入参数长度：3

CRC 计算的结果是 37_H。

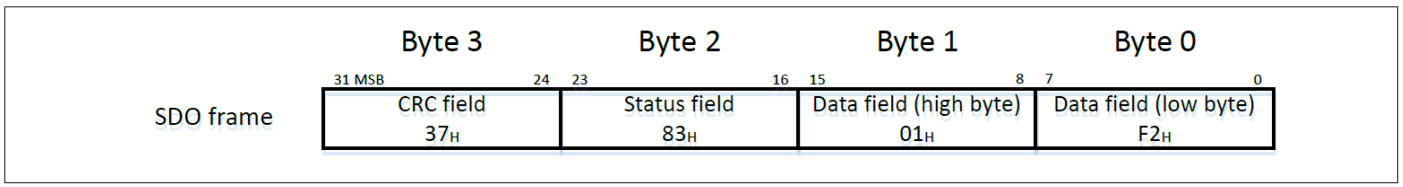


图 91　　SDO 框架示例

CRC 检查

CRC 检查包括以下 SDI 帧元素（图 92）：

- 数据字段低位字节
- 数据字段高位字节
- 地址字段
- CRC 字段

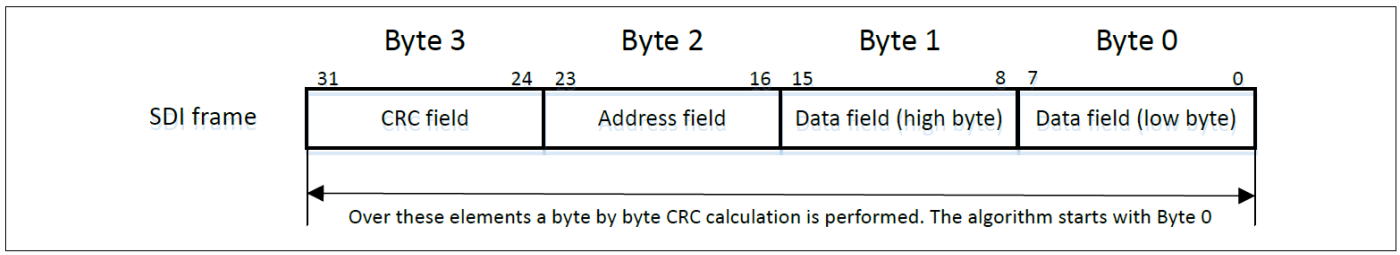


图 92　　SAE J1850 CRC 计算的字节顺序

示例：

如果器件接收到图 93 中的帧，则 CRC 算法（参见第 14.1.2.5 章）需要以下输入参数：

- 输入字节域参数数据：{$F2_H$, 01_H, 83_H, 37_H}
- 输入参数长度：4

CRC 检查的结果始终为 $3B_H$。不同的值意味着帧已损坏。值 $3B_H$在 AUTOSAR CRC 规范中被称为魔力数。

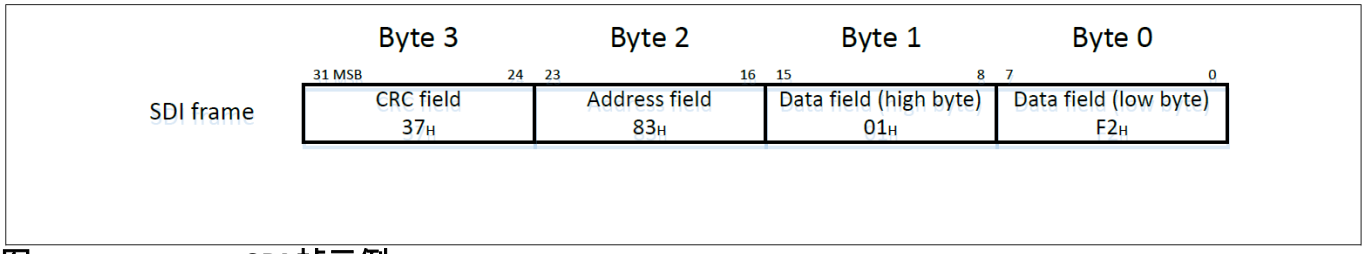


图 93　　SDI 帧示例

14.1.2.6　状态字段

图 94 展示了状态字段的结构。接下来的章节将详细定义状态字段位的功能。

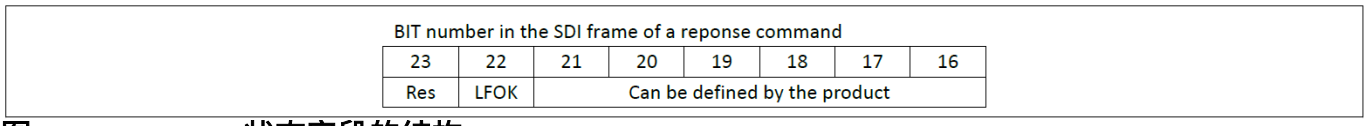


图 94　　状态字段的结构

该设备在 SDO 帧状态字段的第 21 位到第 16 位中实现了以下位字段：

表 46　　设备特定状态字段

Bit number referred to SDO frame	Bit number referred to status field	Function
[21]	[5]	**INTMISS:** Flag for interrupt not serviced in time t_{INTx_to}
[20]	[4]	**MON:** Flag for monitor interrupt (IF1.MON)
[19]	[3]	**OTW:** Flag for overtemperature warning interrupt (IF1.OTW)
[18]	[2]	**CL2ERR:** Flag for fault detected on WWD2, FWD2 or ERR2
[17]	[1]	**CL1ERR:** Flag for fault detected on WWD1, FWD1 or ERR1
[16]	[0]	**ERRMISS:** Flag for fault detected on any ERR[x]

注释：

状态标志仅在最后一帧到达/请求时更新。

14.1.2.6.1　最后一帧 OK (LFOK)

表 47　　最后一帧 OK

Encoding	Description
0_b	Error encountered in the SDI frame of last request frame
1_b	Read service or write service successfully executed

第 14.1.2.7 章介绍了错误处理和 LFOK = 0 的原因。

注释：
建议在处理 SPI 帧之前检查 LFOK 的状态，这与 INT 无关

14.1.2.7 错误机制

如果 SPI 通信发生故障（参见表 48), LFOK 位置位为“0”(参见表 47）。在这种情况下，响应 SPI 传输包含错误代码。图 95 展示了响应 SPI 传输的结构。

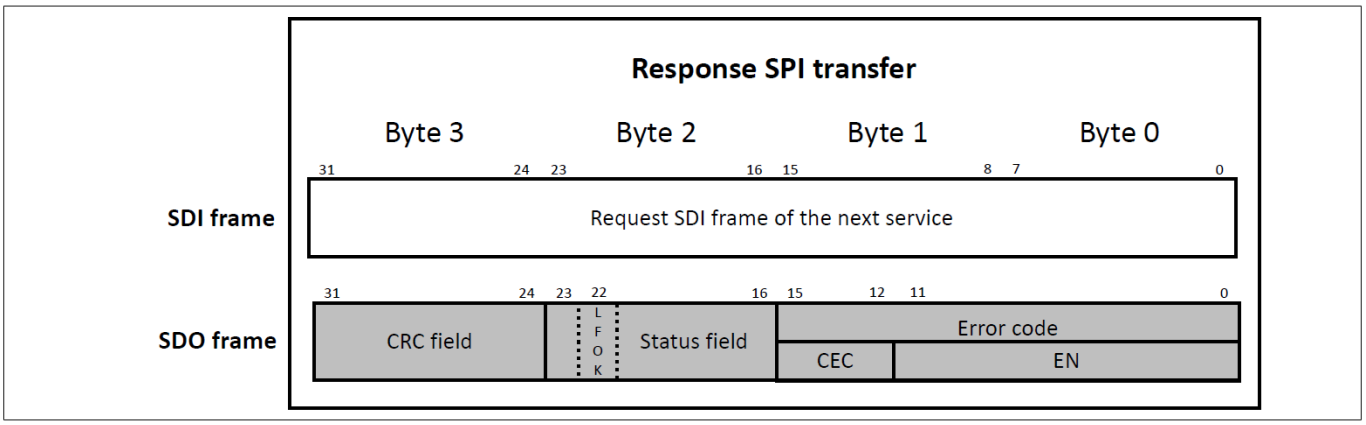


图 95　　错误响应 SPI 传输

错误代码由以下部分组成：

- 通信错误代码（CEC）
- 错误编号（EN，仅供内部使用）

表 48　　SPI 通信故障

CEC	Description
0x0	reserved
0x1	Frame error detected - frame frame length invalid of previous SPI communication - frame ignored
0x2	CRC error detected - frame ignored
0x3	reserved
0x4	Access to none existing register (if SPI interframe is >5.2 us) If SPI interframe is <5.2 us an error frame of 0xF1000000 can be responded instead
0x5	reserved
0x6	reserved
0x7	Internal error while accessing a register

***注释：**　　如果收到未列出的通信错误代码，请联系客户支持。*

14.1.2.8 MPS ON 时的 SPI 响应

如果 MPS 已启用，并且 MCU 无法处理 ERR/WD，则器件将进入 INIT 状态，并以 RESOUT 为高电平执行初始化序列。

由于移动到 INIT 事件后需要进行初始化活动，因此存在一个最多 75µs 的窗口期，在此期间 SDO 响应需要更长的时间（2.5 µs）才能可用。如果 SPI 帧间间隔较短，即使请求已执行，当传输下一个 SPI 帧时，SDO 上的响应也会有 0xF1000000 错误帧（“没有可用数据”）。软件可以实施以下任一对策来避免错误帧条件：

- 将帧间距增至 2.5 µs（典型值）

- 使 SPI 处理程序在接收到错误帧时具有鲁棒性
- 如果对 ERR 和 WD 进行故障注入测试，建议从故障注入点开始，直到 SSO1 下降后 75µs 内避免 SPI 通信。由于模拟延迟，SSO1 在实际移动到 INIT 事件后最多下降 30 µs。

14.2 电气特性：SPI

表 49 电气特性：SPI

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI timing							
SPI frequency	f_{SPI}	–	–	10	MHz	1)	DS-1577
CSN leading delay	t_{CSN_LDEL}	200	–	–	ns	1)	DS-2075
CSN trailing delay	t_{CSN_TDEL}	100	–	–	ns	1)	DS-1579
Interframe time	t_{IF}	1	–	–	µs	CSN rising to CSN falling edge 1)	DS-1580
SCK setup low time	t_{SCK_SETL}	100	–	–	ns	1)	DS-1581
SCK clock high time	t_{SCK_H}	45	–	–	ns	1)	DS-1582
SCK clock low time	t_{SCK_L}	45	–	–	ns	1)	DS-1583
SCK hold low time	t_{SCK_HDL}	100	–	–	ns	1)	DS-1584
SDI data setup time	t_{SDI_SET}	10	–	–	ns	1)	DS-1585
SDI data hold time	t_{SDI_HOLD}	10	–	–	ns	1)	DS-1586
SDO enable time	t_{SDO_EN}	–	–	50	ns	1)	DS-1587
SDO valid delay time (high frequency)	t_{SDO_VDEL}	–	–	136	ns	$C_{SDO,load}$ = 50 pF; f_{SPI} < 1 MHz 1)	DS-1588
SDO valid delay time (high frequency)	t_{SDO_VDEL}	–	–	36 + 0.1/ f_{SPI}	ns	$C_{SDO,load}$ = 50 pF; 1 MHz ≤ f_{SPI} ≤ 10 MHz 1)	DS-1589
SDO disable time	t_{SDO_DIS}	–	–	100	ns	1)	DS-1590
SPI input signal rise time (SDI, SCK, CSN)	$t_{SPI,r}$	–	–	100	ns	f_{SPI} < 1 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1591
SPI input signal rise time (SDI, SCK, CSN)	$t_{SPI,r}$	–	–	0.1/ f_{SPI}	ns	1 MHz ≤ f_{SPI} ≤ 10 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1592
SPI input signal fall time (SDI, SCK, CSN)	$t_{SPI,f}$	–	–	100	ns	f_{SPI} < 1 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1593

（表格续下页……）

表 49　　（续）电气特性：SPI

V_{VS}= 6.0 V 至 36 V；T_j = -40°C 至 +150°C，所有电压均相对于接地，正向电流流入引脚（除非另有说明）

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI input signal fall time (SDI, SCK, CSN)	$t_{SPI,f}$	–	–	0.1/ f_{SPI}	ns	1 MHz ≤ f_{SPI} ≤ 10 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1594
SPI microcontroller interface							
SPI input voltage high level	V_{SPI_H}	2	–	V_{QUC}	V	V_{SPI} increasing, V_{QUC} ≥ V_{QUC} [Min]; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1596
SPI input voltage low level	V_{SPI_L}	0	–	0.8	V	V_{SPI} decreasing; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1597
SPI input voltage hysteresis	V_{SPI_HYS}	–	200	–	mV	V_{QUC} = V_{QUC} [Typ]; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1599
SPI input capacitance	C_{SPI}	–	4	15	pF	Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1600
CSN pull-up current	I_{CSN}	-180	-55	–	µA	V_{CSN} ≤ V_{QUC}[Typ] 1)	DS-1601
SCK pull-down current	I_{SCK}	–	135	330	µA	V_{SCK} ≤ V_{QUC}[Typ] 1)	DS-1602
SDI pull-down current	I_{SDI}	–	135	330	µA	V_{SDI} = V_{QUC} 1)	DS-1603
SDO output voltage high level	V_{SDO_H}	2	–	–	V	V_{QUC} ≥ V_{QUC}[Min]; I_{SDO} = -7 mA 1)	DS-1605
SDO output voltage low level	V_{SDO_L}	–	–	0.7	V	I_{SDO} = 5.5 mA 1)	DS-1606
SDO tristate capacitance	C_{SDO}	–	4	15	pF	1)	DS-1607
SDO tristate leakage current	I_{SDO_leak}	-10	–	10	µA	1)	DS-1608

1)　未经过生产测试，由设计指定

15 复位级别

总共有 6 个复位级别。每个位字段被分配给这六个复位级别之一，并在发生复位级别中列出的事件时相应地复位为其复位值。复位级别以某种方式置位，以便下一个较高的复位级别完全包含较低的复位级别（例如：R3 包含 R2，R2 包含 R1，...）。

15.1 R0 - 复位级别

发生以下事件时，分配给复位级别 R0 的位字段将复位为其复位值：
- POR（上电复位，断开电池）
- STANDBY no WUT AND no QST 激活（进入 STANDBY 状态，不激活唤醒计时器，也不使用备用稳压器 QST）

15.2 R1 - 复位级别

发生以下事件时，分配给复位级别 R1 的位字段将复位为其复位值：
- POR
- STANDBY no WUT AND no QST 激活
- STANDBY

15.3 R2 - 复位级别

发生以下事件时，分配给复位级别 R2 的位字段将复位为其复位值：
- POR
- STANDBY no WUT AND no QST 激活
- STANDBY
- FAILSAFE

15.4 R3 - 复位级别

发生以下事件时，分配给复位级别 R3 的位字段将复位为其复位值：
- POR
- STANDBY no WUT AND no QST 激活
- STANDBY
- FAILSAFE
- RESOUT 拉低
- INIT（进入 INIT 状态）

15.5 R3_C1 - 复位级别

发生以下事件时，分配给复位级别 R3_C1 的位字段将复位为其复位值：
- POR
- STANDBY no WUT AND no QST 激活
- STANDBY
- FAILSAFE
- RESOUT 拉低
- INIT
- REDUCED OPERATION（由应用 1 故障引起的进入REDUCED OPERATION）

属于此复位级别的寄存器和位字段包括：
- ERR1_RS_CFG

- WD1_RS_CFG0
- WD1_RS_CFG1
- FWD1_RS_HBTP_CFG
- WWD1_RS_CW_CFG
- WWD1_RS_OW_CFG
- FWD1_STAT
- WWD1_ECNT_STAT

15.6 R3_C2 - 复位级别

发生以下事件时，分配给复位级别 R3_C2 的位字段将复位为其复位值：

- POR
- STANDBY no WUT AND no QST 激活
- STANDBY
- FAILSAFE
- RESOUT 拉低
- INIT
- REDUCED OPERATION（由应用 2 故障引起的进入 REDUCED OPERATION）

属于此复位级别的寄存器和位字段为：

- ERR2_RS_CFG
- WD2_RS_CFG0
- WD2_RS_CFG1
- FWD2_RS_HBTP_CFG
- WWD2_RS_CW_CFG
- WWD2_RS_OW_CFG
- FWD2_STAT
- WWD2_ECNT_STAT

16 集合寄存器、错误报告和位字段清除

如果发生相应的错误事件，器件会提供错误寄存器（请参阅故障反应）。为了简化诊断程序，集合寄存器实现了将一组错误寄存器捆绑在一起，并且集合寄存器中仅放置一个位。通过提供这条信息，它允许集成商在第一步中仅读取集合寄存器并遵循错误报告的路径，而不是总是读取所有错误寄存器。如果 REDUCED OPERATION 是启用的并且两个应用线程访问该信息，则整个配置可在双倍结构中使用。如果不使用 REDUCED OPERATION，这些双倍的寄存器是非激活的，不会反馈任何可靠的结果。

通过将相应的位写入“1”来清除故障位和错误位。其他任何读写访问均无效。

此外，错误报告概述提供了所用错误类别的赋值。一般来说，严重故障（xx_SEV_FAULT）和警告故障（xx_WARN_FAULT）是有区别的。

严重故障：

严重故障是指器件或器件监控的系统参数中发生的严重事件，该事件可能导致应用变得不可靠，并且已经变得不可靠，因此绝不能允许其进入正常运行状态。根据故障情况，将进行多次恢复尝试，例如软复位、硬复位或转入 FAILSAFE。在任何情况下，都会发出 SSO1/2 信号，表示不能认为应用已完全正常运行，必须将其转入安全状态。

故障警告：

警告与设备或设备监控的系统参数中的事件相关，但这些事件不会直接危及应用的正常功能。发出中断表示出现故障警告。但应用仍处于正常功能状态，SSO1/2 不会显示安全状态。

16.1 错误报告生成中断

触发中断 (INT) 的错误会被收集到 IFx 寄存器中。在此寄存器中捆绑的事件列在下表中。

表 50 错误生成中断 - 收集寄存器：IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
SYSFAIL_ERR	SYS_STAT_APP1	ERRx_WARN_FAULT	ERR0_ERR	ERR0 monitoring error AND ERR0 recovery is enabled
			ERR1_ERR	ERR1 monitoring error AND ERR1 recovery is enabled
		WDx_WARN_FAULT	WWD1_ERR	WWD1 missed or incorrect service (error counter below threshold)
			FWD1_ERR	FWD1 response missed or incorrectly triggered (error counter below threshold)
		SYS_WARN_FAULT		

（表格续下页……）

表 50 （续）错误生成中断 - 收集寄存器：IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			FSM_NOOP	State transition not existing or transition conditions not fulfilled.
			FSM_TRFAIL	State transition into low power state (STANDBY or SLEEP) failed/interrupted (e.g. by WAK or ENA)
			BUCKCORE_SVS_NOK	Static voltage scaling not performed due to: - Device being no in INIT or NORMAL - BUCKCORE voltage set to 1.15 V
			BUCKCORE_SVS_OK	Static voltage scaling completed successfully.
			APP2_FAIL	Application 2 was reason for entering REDUCED OPERATION
WUT_EVT	WAKE_STAT_APP1	WAKE_EVENT	ENA	ENA signal detected
			WAK	WAK signal detected
			WUT	Wake-up timer (WUT) expired and woke up the device
			SPI	SPI command woke up the device
SPI_FAIL	SPI_FAIL_STAT_APP 1	SPI_WARN_FAULT	LOCK	Lock of protected registers was unsuccessful
			CRC	CRC wrong
			FR_LEN	Frame length wrong
			ADR	Invalid address
			CS_TO	CSN timeout after 2 ms
MON	STG_STAT_APP1	VMON_WARN_FAULT	BUCKIF	Short to ground at BUCKIF BUCKIF is switched off

（表格续下页……）

表 50 （续）错误生成中断 - 收集寄存器：IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			QCO	Short to ground at QCO QCO is switched off
			QVR	Short to ground at QVR QVR is switched off
			VMON1	Short to ground at VMON1 VMON1 rail is disabled
			VMON2	Short to ground at VMON2 VMON2 rail is disabled
	UV_STAT_APP1		PREREG	Undervoltage at PREREG
			BOOST	Undervoltage at BOOST
			QCO	Undervoltage at QCO
			BUCKIF	Undervoltage at BUCKIF
			QVRUV	Undervoltage at QVR
			VMON1	Undervoltage at VMON1
			VMON2	Undervoltage at VMON2
	INTSUP_STAT_APP1		PMU_RED	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			PMU_MAIN	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)

（表格续下页……）

表 50 （续）错误生成中断 - 收集寄存器：IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			BG12_OV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_UV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
OT_WRN_OC_ERR	OT_WRN_OC_STAT_APP1	OTOC_WARN_FAULT	IVCC_OC	Internal error
			QST_OC	QST overcurrent
			BUCKCORE_OTWRN	BUCKCORE overtemperature warning
			BUCKIF_OTWRN	BUCKIF overtemperature warning
			BOOST_OTWRN	BOOST overtemperature warning
			BOOST_OC	BOOST overcurrent
			QUC_OTWRN	QUC overtemperature warning
			QCO_OTWRN	QCO overtemperature warning
			QVR_OC	QVR overcurrent
ABIST	-	ABIST_WARN_FAULT	-	ABIST finished execution
INTMISS	-	-	-	Interrupt flags not cleared after tINTx_to

(x = 1; 2)

如果启用 REDUCED OPERATION，还会设置以下位：

表 51 错误生成中断 - 有限操作 - 收集寄存器：IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
SYSFAIL_ERR	SYS_STAT_APP2	ERRx_WARN_FAULT	ERR0_ERR	ERR0 monitoring error
			ERR2_ERR	ERR2 monitoring error AND ERR2 recovery is enabled
		WDx_WARN_FAULT	WWD2_ERR	WWD2 missed or incorrect service (error counter below threshold)
			FWD2_ERR	FWD2 response missed or incorrectly triggered (error counter below threshold)
		SYS_WARN_FAULT	FSM_NOOP	State transition not existing or transition conditions not fulfilled.
			FSM_TRFAIL	State transition into low power state (STANDBY or SLEEP) failed/interrupted (e.g. by WAK or ENA)
			BUCKCORE_SVS_NOK	Static voltage scaling not performed due to: - Device being not in INIT or NORMAL - BUCKCORE voltage set to 1.15 V
			BUCKCORE_SVS_OK	Static voltage scaling completed successfully.
			APP1_FAIL	Cluster 1 was reason for entering REDUCED OPERATION
WUT_EVT	WAKE_STAT_APP2	WAKE_EVENT	ENA	ENA signal detected
			WAK	WAK signal detected
			WUT	Wake-up timer (WUT) expired and woke up the device

（表格续下页……）

表 51 （续）错误生成中断 - 有限操作 - 收集寄存器： IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
			SPI	SPI command woke up the device
SPI_FAIL	SPI_FAIL_STAT_APP 2	SPI_WARN_FAULT	LOCK	Lock of protected registers was unsuccessful
			CRC	CRC wrong
			FR_LEN	Frame length wrong
			ADR	Invalid address
			CS_TO	CSN timeout after 2 ms
MON	STG_STAT_APP2	VMON_WARN_FAULT	BUCKIF	Short to ground at BUCKIF BUCKIF is switched off
			QCO	Short to ground at QCO QCO is switched off
			QVR	Short to ground at QVR QVR is switched off
			VMON1	Short to ground at VMON1 VMON1 rail is disabled
			VMON2	Short to ground at VMON2 VMON2 rail is disabled
	UV_STAT_APP2		PREREG	Undervoltage at PREREG
			BOOST	Undervoltage at BOOST
			QCO	Undervoltage at QCO
			BUCKIF	Undervoltage at BUCKIF
			QVR	Undervoltage at QVR
			VMON1	Undervoltage at VMON1
			VMON2	Undervoltage at VMON2

（表格续下页……）

表 51 （续）错误生成中断 - 有限操作 - 收集寄存器： IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
	INTSUP_STAT_APP2		PMU_RED	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			PMU_MAIN	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_OV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_UV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
OT_WRN_OC_ERR	OT_WRN_OC_STAT_APP2	OTOC_WARN_FAULT	IVCC_OC	Internal error
			QST_OC	QST overcurrent
			BUCKCORE_OTWRN	BUCKCORE overtemperature warning
			BUCKIF_OTWRN	BUCKIF overtemperature warning
			BOOST_OTWRN	BOOST overtemperature warning

（表格续下页……）

表 51 （续）错误生成中断 - 有限操作 - 收集寄存器：IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
			BOOST_OC	BOOST overcurrent
			QUC_OTWRN	QUC overtemperature warning
			QCO_OTWRN	QCO overtemperature warning
			QVR_OTWRN	QVR overcurrent
ABIST	-	ABIST_WARN_FAULT	-	ABIST finished execution
INTMISS	-	-	-	Interrupt flags not cleared after tINTx_to

(x = 1; 2)

16.2 错误报告导致移至 INIT 或 REDUCED OPERATION

触发进入 INIT 状态的错误通常也会触发一个复位（RESOUT），并收集在 INIT_ERR_APPx 寄存器中。此寄存器中包含的事件列于下表中。在 MPS（参见微控制器编程支持（MPS））启用的情况下，某些到 INIT 的转移不会发出复位。

表 52 导致移至 INIT 的错误 - 收集寄存器：INIT_ERR_APP1

INIT_ERR_APP1 bitfield	Error class	Error register	Error bitfield	Description
VMONF	VMONUV_SEV_FAULT	UV_STAT_APP1	BUCKCORE	BUCKCORE undervoltage
			QUC	QUC undervoltage
			QST	QST undervoltage
WWD1_EC	WDx_SEV_FAULT	-	-	WWD1 incorrectly triggered and error counter reaches threshold
WWD2_EC		-	-	WWD2 incorrectly triggered and error counter reaches threshold
FWD1_EC		-	-	FWD1 incorrectly triggered and error counter reaches threshold

（表格续下页……）

表 52 （续）导致移至 INIT 的错误 - 收集寄存器：INIT_ERR_APP1

INIT_ERR_APP1 bitfield	Error class	Error register	Error bitfield	Description
FWD2_EC		-	-	FWD2 incorrectly triggered and error counter reaches threshold
ERR1	ERRx_SEV_FAULT	-	-	ERR1 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
ERR2		-	-	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
REDOP_RES1	INITTIMER_SEV_FAULT	-	-	INIT timer expired the first time in RED. OP. due to application 1 not being able to reinitialize
REDOP_RES2		-	-	INIT timer expired a second time in RED. OP.
SOFTRES		-	-	INIT timer expires 1st time → Soft reset issued
HARDRES		-	-	INIT timer expires 2nd time consecutively → Hard reset issued

(x = 1; 2)

如果启用 REDUCED OPERATION，还会设置以下位：

表 53 导致移至 INIT的错误 - 有限操作 - 收集寄存器：INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
VMONF	VMONUV_SEV_FAULT	UV_STAT_APP1	BUCKCORE	BUCKCORE undervoltage
			QUC	QUC undervoltage

（表格续下页……）

表 53 （续）导致移至 INIT 的错误 - 有限操作 - 收集寄存器：INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
			QST	QST undervoltage
WWD1_EC	WDx_SEV_FAULT	—	—	WWD1 incorrectly triggered and error counter reaches threshold
WWD2_EC		—	—	WWD2 incorrectly triggered and error counter reaches threshold
FWD1_EC		—	—	FWD1 incorrectly triggered and error counter reaches threshold
FWD2_EC		—	—	FWD2 incorrectly triggered and error counter reaches threshold
ERR1	ERRx_SEV_FAULT	—	—	ERR1 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
ERR2		—	—	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
REDOP_RES1	INITTIMER_SEV_FAULT	—	—	INIT timer expired the first time in RED. OP. due to application 2 not being able to reinitialize
REDOP_RES2		—	—	INIT timer expired a second time in RED. OP.
SOFTRES		—	—	INIT timer expires 1st time → Soft reset issued

（表格续下页……）

表 53 （续）导致移至 INIT 的错误 - 有限操作 - 收集寄存器：INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
HARDRES		—	—	INIT timer expires 2nd time consecutively → Hard reset issued

(x = 1; 2)

16.3 错误报告导致移至 FAILSAFE

触发移至 FAILSAFE 的错误会被记录在寄存器中。唯一例外是 ABIST 位。仅当 ABIST 执行期间发生错误导致器件移至 INIT 或 FAILSAFE 时，才会将其置位，而这本身并不会触发状态转移。

表 54 导致移至 FAILSAFE 的错误 - 收集寄存器：SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
QST_QUC_VOLTSEL	VOLTSEL_SEV_FAULT	-	-	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.
BUCKIF_VOLTSEL		-	-	Voltage selection error. 1.8 or 3.3 V might be corrupt and not correctly selected.
BUCK_CORE_VOLTSEL		-	-	Voltage selection error. Core voltage might be corrupt.
OT	OT_SEV_FAULT	OT_STAT_APP1	BUCKCORE	BUCKCORE thermal shutdown
			BUCKIF	BUCKIF thermal shutdown
			BOOST	BOOST thermal shutdown
			QUC	QUC thermal shutdown
			QCO	QCO thermal shutdown
			SAFETY_AREA	Overtemperature of safety area

（表格续下页……）

表 54 （续）导致移至 FAILSAFE 的错误 - 收集寄存器：SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
VMON	VMON_SEV_FAULT	STG_STAT_APP1	BUCKCORE	BUCKCORE short to ground
			BOOST	BOOST short to ground & Severe undervoltage
			QUC	QUC short to ground
			QST	QST short to ground
			PREREG	PREREG short to ground & Severe undervoltage
		OV_STAT_APP1	BUCKCORE	Severe overvoltage at BUCKCORE & BUCKCORE OV
			BUCKCORE_FB_OPEN	Feedback open
			PREREG	Severe overvoltage at PREREG & PREREG OV
			BUCKIF	Severe overvoltage at BUCKIF & BUCKIF OV
			BOOST	BOOST OV
			QUC	QUC OV
			QCO	QCO OV
			QVR	QVR OV
			QST	QST OV
			VMON1	VMON1 OV
			VMON2	VMON2 OV
			INTSUP_VDD2V5	Internal 2V5 rail overvoltage
			INTSUP_IVCC	Internal IVCC overvoltage
		UV_STAT_APP1	INTSUP_VDD2V5_UV	Internal 2V5 rail undervoltage
			INTSUP_IVCC_UV	Internal IVCC undervoltage

（表格续下页……）

表 54 （续）导致移至 FAILSAFE 的错误 - 收集寄存器：SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
		INTSUP_STAT_APP1	BIAS_HI	Internal bias current too high
			BIAS_LOW	Internal bias current too low
			VBAT_OV	VS OV
FSM_INITTIMER	INITTIMER_SEV_FAU LT	-	-	FAILSAFE was entered because INIT timer expired a 3rd time without successful initialization.
ERR0	ERR0_SEV_FAULT	-	-	FAILSAFE was entered after ERR0 reported invalid frequency.
QST	QST_SEV_FAULT	-	-	Set for: QST BIST errors, severe overvoltage
INTSUP_IVCC	INTSUP_SEV_FAULT	-	-	Set for: QIS BIST errors, severe overvoltage
PREREG_COSW	SSW_SEV_FAULT	-	-	BIST major error SSC or SSW was activated during normal operation
CFGE	CFG_SEV_FAULT	-	-	Double Error detected on a protected register
ABIST	ABIST_SEV_FAULT	-	-	Any error that moves the device to FAILSAFE or INIT and is not part of the ABIST routine will abort the on-going ABIST and set this bit.

(x = 1; 2)

如果启用 REDUCED OPERATION，还会设置以下位：

表 55 导致移至 FAILSAFE 的错误 - 有限操作 - 收集寄存器：SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
QST_QUC_VOLTSEL	VOLTSEL_SEV_FAULT	-	-	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.
BUCKIF_VOLTSEL		-	-	Voltage selection error. 1.8 V or 3.3 V might be corrupt and not correctly selected.
BUCK_CORE_VOLTSEL		-	-	Voltage selection error. Core voltage might be corrupt.
OT	OT_SEV_FAULT	OT_STAT_APP2	BUCKCORE	BUCKCORE thermal shutdown
			BUCKIF	BUCKIF thermal shutdown
			BOOST	BOOST thermal shutdown
			QUC	QUC thermal shutdown
			QCO	QCO thermal shutdown
			SAFETY_AREA	Overtemperature of safety area
VMON	VMON_SEV_FAULT	STG_STAT_APP2	BUCKCORE	BUCKCORE short to ground
			BOOST	BOOST short to ground & severe undervoltage
			QUC	QUC short to ground
			QST	QST short to ground
			PREREG	PREREG short to ground & severe undervoltage
		OV_STAT_APP2	BUCKCORE	Severe overvoltage at BUCKCORE & BUCKCORE OV

（表格续下页……）

表 55 （续）导致移至 FAILSAFE 的错误 - 有限操作 - 收集寄存器：SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
			BUCKCORE_FB_OPE N	Feedback open
			PREREG	Severe overvoltage at PREREG & PREREG OV
			BUCKIF	Severe overvoltage at BUCKIF & BUCKIF OV
			BOOST	BOOST OV
			QUC	QUC OV
			QCO	QCO OV
			QVR	QVR OV
			QST	QST OV
			VMON1	VMON1 OV
			VMON2	VMON2 OV
			INTSUP_VDD2V5	Internal 2V5 rail overvoltage
			INTSUP_IVCC	Internal IVCC overvoltage
		UV_STAT_APP2	INTSUP_VDD2V5_UV	Internal 2V5 rail undervoltage
			INTSUP_IVCC_UV	Internal IVCC undervoltage
		INTSUP_STAT_APP2	BIAS_HI	Internal bias current too high
			BIAS_LOW	Internal bias current too low
			VBAT_OV	VS OV
FSM_INITTIMER	INITTIMER_SEV_FAU LT	-	-	FAILSAFE was entered because INIT timer expired a 3rd time without successful initialization.
ERR0	ERR0_SEV_FAULT	-	-	FAILSAFE was entered after ERR0 reported invalid frequency.

（表格续下页……）

表 55 （续）导致移至 FAILSAFE 的错误 - 有限操作 - 收集寄存器：SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
QST	QST_SEV_FAULT	-	-	Set for: QST BIST errors, severe overvoltage
INTSUP_IVCC	INTSUP_SEV_FAULT	-	-	Set for: QIS BIST errors, severe overvoltage
PREREG_COSW	SSW_SEV_FAULT	-	-	BIST major error SSC or SSW was activated during normal operation
CFGE	CFG_SEV_FAULT	-	-	Double error detected on a protected register
ABIST	ABIST_SEV_FAULT	-	-	Any error that moves the device to FAILSAFE or INIT and is not part of the ABIST routine will abort the on-going ABIST and set this bit.

(x = 1; 2)

16.4 状态报告 - 杂项寄存器

设备状态信息被收集在 VMON_STAT 和 DEV_STAT 中。

	Status bitfield	Description
VMON_STAT	all	Indicates whether voltage regulators are within range or outside of it. If a regulator is switched off the bits read as 0.
DEV_STAT	all	Provides an overview of the devices general state (e.g. Enabled regulators, State, Autodetection)

17 受保护寄存器 - 受保护的写入寄存器和反映状态寄存器

该设备包含受保护寄存器以避免对与安全相关的参数的无意访问。一个受保护寄存器总是由一对可配置的“受保护写入”寄存器及其对应的“反映状态”影子寄存器组成。必须先解锁这些寄存器，才能写入新内容。新内容必须始终写入受保护的写寄存器。为了使新的更改生效，必须再次锁定寄存器。通过锁定序列，新内容被传输到反映状态寄存器。

属于受保护寄存器类别的寄存器，其名称中会按如下方式标记：

Protected write	*<registername>*_PW_*<registername>*
Reflected status	*<registername>* _RS_*<registername>*

17.1 解锁/锁定序列

要解锁和锁定受保护的寄存器，必须执行以下步骤：

1. 解锁寄存器：将 0xB5CA 写入寄存器**PROT_CFG.KEY**
2. 向受保护的写寄存器写入更改
3. 锁定寄存器：向寄存器 **PROT_CFG.KEY** 写入 0xD396。

在向受保护的写寄存器写入更改之前，并通过读取反映的状态寄存器检查这些更改是否生效，可以在 **PROT_STAT.LOCK** 中读取受保护寄存器的当前锁定状态。此外，如果在解锁/上锁序列过程中出现问题，错误位 SPI_FAIL_STAT_APP1.LOCK 将被设置。在这种情况下，写入的值不会生效，RS 寄存器也不会更新。如果启用了 REDUCED OPERATION，SPI_FAIL_STAT_APP2.LOCK 也会被设置。

18 寄存器描述

18.1 寄存器概述 - OTHERSR2（升序偏移地址）

表56 寄存器概述 - OTHERSR2（升序偏移地址）

Short name	Long name	Offset address	See
DEV_CFG4	Device configuration 4 *R2)	000_H	210
REDOP_RS_CFG2	Reduced operation reflected status configuration 2 register - *R2)	001_H	212
PROT_CFG	Protection configuration register - *R2)	002_H	213
DEV_RS_CFG3	Device reflected status configuration Register *R2)	003_H	214
WUT_CFG0	Wake up timer LSB Value (*R2)	004_H	216
WUP_CFG1	Wake up timer MSB Value (*R2)	005_H	217
WAKE_STAT_APP1	Wakeup status flags for Application 1 *R2)	006_H	218
WAKE_STAT_APP2	Wakeup status flags for Application 2 *R2)	007_H	219
INIT_ERR_APP1	INIT and REDUCED OPERATION Error Status flags for Application 1 *R2)	008_H	220
INIT_ERR_APP2	INIT and REDUCED OPERATION Error Status flags for Application 2 *R2)	009_H	222
IF1	Interrupt flags for Application 1 that trigger INT1 *R2)	$00A_H$	224
IF2	Interrupt flags for Application 2 that trigger INT2 *R2)	$00B_H$	226
SYS_STAT_APP1	System status flags for Application 1 that trigger INT1 *R2)	$00C_H$	228
SYS_STAT_APP2	System status flags for Application 2 that trigger INT2 *R2)	$00D_H$	230
SPI_FAIL_STAT_APP1	SPI failure status flags that triggers INT1 *R2)	$00E_H$	232
SPI_FAIL_STAT_APP2	SPI status flags for Application 2 that trigger INT2 *R2)	$00F_H$	233
UV_STAT_APP1	Monitor status flags register 2 for Application 1 *R2)	010_H	234
UV_STAT_APP2	Monitor status flags register 2 for Application 2 *R2)	011_H	236
OT_WRN_OC_STAT_APP1	Over temperature warning and over current status flags *R2)	012_H	238
OT_WRN_OC_STAT_APP2	Over temperature warning /Over current status flags for Application 2 *R2)	013_H	240
VMON_STAT	Voltage monitor status *R2)	014_H	242
DEV_STAT	Device status register *R2)	015_H	244
DCDC_FREQ_SYNC	DC-DC switching frequency change *R2)	016_H	246
FREQ_SPREAD	DC-DC Frequency spread-spectrum control register *R2)	017_H	248
ABIST_CTRL0	ABIST control 0 *R2)	018_H	250
ABIST_CTRL1	ABIST control 1 *R2)	019_H	251
ABIST_SELECT0	ABIST select 0 *R2)	$01A_H$	252
ABIST_SELECT1	ABIST select 1 *R2)	$01B_H$	254
ABIST_SELECT2	ABIST select 2 *R2)	$01C_H$	256

（表格续下页.....）

表56 寄存器概述 - SOTP（升序偏移地址）

Short name	Long name	Offset address	See
GTM	Global testmode *R2)	$01D_H$	258
REDOP_RS_CFG1	Reduced operation reflected status configuration 1 register - *R2)	$01E_H$	259

18.2 寄存器概述 - ERR（升序偏移地址）

表57 寄存器概述 -ERR（升序偏移地址）

Short name	Long name	Offset address	See
ERR0_PW_CFG	ERR0 protection write configuration register *R2)	$01F_H$	261
ERR0_RS_CFG	ERR0 reflected status configuration register *R3)	020_H	262
ERR1_PW_CFG	ERR1 protection write configuration register *R2)	021_H	263
ERR1_RS_CFG	ERR1 reflected status configuration register *R3_C1)	022_H	264
ERR2_PW_CFG	ERR2 protection write configuration register *R2)	023_H	265
ERR2_RS_CFG	ERR2 reflected status configuration register *R3_C2)	024_H	266

18.3 寄存器概述 - OTHERSR0（升序偏移地址）

表 58 寄存器概述 - OTHERSR0 （升序偏移地址）

Short name	Long name	Offset address	See
DEV_CFG1	Device configuration 1 register *R0)	025_H	267
DEV_PW_CFG2	Device protected write configuration 2 register *R0)	026_H	269
DEV_RS_CFG2	Device reflected status configuration 2 register *R0)	027_H	270

18.4 寄存器概述 - OTHERSR1 （升序偏移地址）

表59 寄存器概述 - OTHERSR1 （升序偏移地址）

Short name	Long name	Offset address	See
SYSFAIL_STAT_APP1	System failure status register for application 1 *R1)	029_H	271
SYSFAIL_STAT_APP2	System failure status flags for application 2 *R1)	$02A_H$	273
STG_STAT_APP1	Short to ground status register for application 1 *R1)	$02B_H$	275
STG_STAT_APP2	Short to ground status register for application 2 *R1)	$02C_H$	277
OV_STAT_APP1	Overvoltage status register for application 1 *R1)	$02D_H$	279
OV_STAT_APP2	Overvoltage status register for application 2 *R1)	$02E_H$	281
INTSUP_STAT_APP1	Internal supply status register for application 1 *R1)	$02F_H$	283
INTSUP_STAT_APP2	Internal supply status register for application 2 *R1)	030_H	284

（表格续下页.....）

18 Registers description

表59 （续）寄存器概述 - OTHERSR1 （升序偏移地址）

Short name	Long name	Offset address	See
OT_STAT_APP1	Over temperature status register for application 1 *R1)	031_H	285
OT_STAT_APP2	Over temperature status register for application 2 *R1)	032_H	286
PROT_STAT	Protection status *R1)	033_H	287
REDOP_PW_CFG1	Reduced operation protected write configuration 1 register - *R1)	034_H	288
REDOP_PW_CFG2	Reduced operation protected write configuration 2 register - *R1)	035_H	290
DEV_PW_CFG3	Device protected write configuration 3 register *R1)	036_H	291

18.5 寄存器概述 - WATCHDOG （升序偏移地址）

表60 寄存器概述 - WATCHDOG （升序偏移地址）

Short name	Long name	Offset address	See
WD1_PW_CFG0	Watchdog 1 protected write configuration 0 register *R2)	037_H	293
WD1_RS_CFG0	Watchdog 1 reflected status configuration 0 register - *R3_C1	038_H	294
WD1_PW_CFG1	Watchdog 1 protected write configuration 1 register *R2)	039_H	295
WD1_RS_CFG1	Watchdog 1 reflected status configuration 1 register- *R3_C1	$03A_H$	296
FWD1_PW_HBTP_CFG	Functional watchdog 1 protected write heart beat timer period configuration register - *R2)	$03B_H$	297
FWD1_RS_HBTP_CFG	Functional watchdog 1 reflected status heart beat timer period configuration register *R3_C1	$03C_H$	298
WWD1_PW_CW_CFG	Window watchdog 1 protected write closed window configuration register - *R2)	$03D_H$	299
WWD1_RS_CW_CFG	Window watchdog 1 reflected status closed window configuration register *R3_C1)	$03E_H$	300
WWD1_PW_OW_CFG	Window watchdog 1 protected write open window configuration register - *R2)	$03F_H$	301
WWD1_RS_OW_CFG	Window watchdog 1 reflected status open window configuration register - *R3_C1)	040_H	302
WWD1_TRIG	Window watchdog 1 trigger- *R2)	041_H	303
FWD1_RSP	Functional watchdog 1 response register - *R2)	042_H	304
FWD1_RSP_SYNC	Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2)	043_H	305
FWD1_STAT	Functional watchdog 1 status register - *R3_C1)	044_H	306
WWD1_ECNT_STAT	Window watchdog 1 error counter status register - *R3_C1)	045_H	307
WD2_PW_CFG0	Watchdog 2 protected write configuration 0 register - *R2)	046_H	308
WD2_RS_CFG0	Watchdog 2 reflected status configuration 0 register- *R3_C2)	047_H	309

（表格续下页.....）

表 60 （续）寄存器概述 - WATCHDOG （升序偏移地址）

Short name	Long name	Offset address	See
WD2_PW_CFG1	Watchdog 2 protected write configuration 1 - *R2)	048_H	310
WD2_RS_CFG1	Watchdog 2 reflected status configuration 1 register - *R3_C2)	049_H	311
FWD2_PW_HBTP_CFG	Functional watchdog 2 protected write heart beat timer period configuration register - *R2)	$04A_H$	312
FWD2_RS_HBTP_CFG	Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2)	$04B_H$	313
WWD2_PW_CW_CFG	Window watchdog 2 protected write closed window configuration register - *R2)	$04C_H$	314
WWD2_RS_CW_CFG	Window watchdog 2 reflected status closed window configuration register *R3_C2)	$04D_H$	315
WWD2_PW_OW_CFG	Window watchdog 2 protected write open window configuration register - *R2)	$04E_H$	316
WWD2_RS_OW_CFG	Window watchdog 2 reflected status open window configuration register *R3_C2)	$04F_H$	317
WWD2_TRIG	Window watchdog 2 service - *R2)	050_H	318
FWD2_RSP	Functional watchdog 2 response register - *R2)	051_H	319
FWD2_RSP_SYNC	Functional watchdog 2 response register with synchronization - *R2)	052_H	320
FWD2_STAT	Functional watchdog 2 status register - *R3_C2)	053_H	321
WWD2_ECNT_STAT	Window watchdog 2 status register - *R3_C2)	054_H	322

18.6 寄存器概述 - MISC（升序偏移地址）

表 61 寄存器概述 - MISC（升序偏移地址）

Short name	Long name	Offset address	See
SSW_DIAG	Safety switch diagnostics, *R1)	055_H	323
BUCK_CORE_PW_VSEL	BUCK CORE protected write voltage selection register *R1)	056_H	324
BUCK_CORE_RS_VSE L	BUCK CORE reflected status voltage selection register *R2)	057_H	325
VCORESTAT	Buck core voltage selection stat, *R2)	058_H	326
VCOREMONSTAT	Buck core voltage selection monitors stat, *R2)	059_H	327
WUT_STAT0	Wake Up Timer value after exiting from STANDBY or SLEEP (lower 16 bits)	$05A_H$	328
WUT_STAT1	Wake Up Timer value after exiting from STANDBY or SLEEP (upper 8 bits)	$05B_H$	329

18.7 寄存器概述 - DEVICEID（升序偏移地址）

表 62 寄存器概述 - DEVICEID（升序偏移地址）

Short name	Long name	Offset address	See
CHPID	Chip product identifier	$1F0_H$	330
CHREV	Chip product version and revision	$1F1_H$	331
MANID	Manufacturer ID	$1F2_H$	332

18.8 器件配置 4 *R2)

DEV_CFG4 Offset address: 000_H

Device configuration 4 *R2) Reset values see: Table 63

15	14	13	12	11	10	9	8
FSM_SDT_VMON12		Res				DCDC_SYNC_IN_EN	WUT_EN
rw		r				rw	rw

7	6	5	4	3	2	1	0
WUT_CYC	WUT_PRESC	FSM_SDT_TMR		FSM_TRDEL			
rw	rw	rw		rw			

Field	Bits	Type	Description
FSM_TRDEL	3:0	rw	**Transition delay (TRDEL) into low power states (STANDBY, SLEEP)** 0_H 100 µs 1_H 200 µs 2_H 300 µs 3_H 400 µs 4_H 500 µs 5_H 600 µs 6_H 700 µs 7_H 800 µs 8_H 900 µs 9_H 1000 µs A_H 1100 µs B_H 1200 µs C_H 1300 µs D_H 1400 µs E_H 1500 µs F_H 1600 µs
FSM_SDT_TMR	5:4	rw	**Shut down timer (tSDT_TMR) for internal regulators of power down sequencing** 00_B 0 01_B 500 µs 10_B 1000 µs 11_B 1500 µs
WUT_PRESC	6	rw	**Wake up timer cycle period pre-scaler** 0_B Disabled 1_B Enabled
WUT_CYC	7	rw	**Wake timer cycle period** 0_B 10 µs 1_B 10 ms

（表格续下页……）

（续）

Field	Bits	Type	Description
WUT_EN	8	rw	**Wake timer enable** 0_B Disabled 1_B Enabled
DCDC_SYNC_IN_EN	9	rw	**Enable synchronization input (only applicable when REDUCED OPERATION is disabled, since it uses SYNC_IN pin shared with INT2)** 0_B Disable 1_B Enable
FSM_SDT_VMON12	15:14	rw	**Shut down timer for VMON1 and VMON2 of power down sequencing** 00_B 0 µs 01_B 500 µs 10_B 1 ms 11_B 1.5 ms

表 63 DEV_CFG4 的复位值

Reset	Reset value	Note
	$C038_H$	Reset class R2)

18.9 有限操作反映状态配置 2 寄存器 - *R2)

REDOP_RS_CFG2 Offset address: 001_H

Reduced operation reflected status configuration 2 register - *R2) Reset values see: Table 64

15	14	13	12	11	10	9	8
REDOP_RESOUT_APP2_DUR			REDOP_RESOUT_APP1_DUR			REDOP_RESOUT_APP_TB	Res
r			r			r	r

7	6	5	4	3	2	1	0
Res							
r							

Field	Bits	Type	Description
REDOP_RESOUT_APP_TB	9	r	**Partial reset timer step, selectable between 10 µs or 100 µs** 0_B 10 µs 1_B 100 µs
REDOP_RESOUT_APP1_DUR	12:10	r	**Application reset pulse duration duration for INT1** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 ... 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1
REDOP_RESOUT_APP2_DUR	15:13	r	**Application reset pulse duration duration for INT2** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 ... 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1

表 64 REDOP_RS_CFG2 的复位值

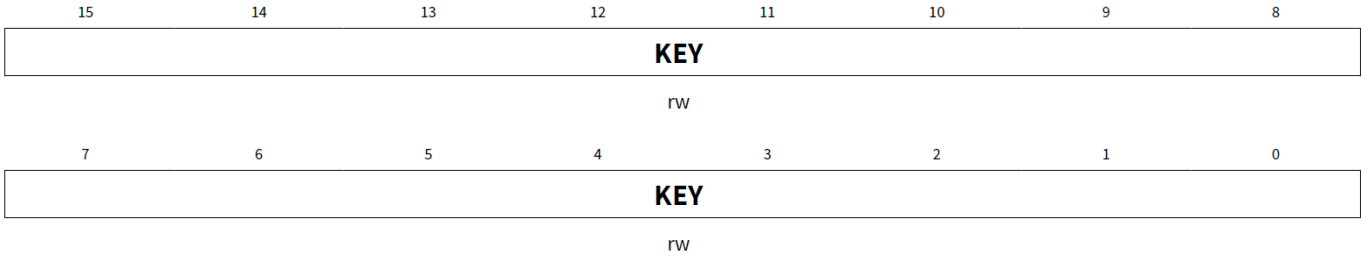
Reset	Reset value	Note
	0000_H	Reset class R2)

18.10 受保护配置寄存器 - *R2)

控制受密码保护寄存器的 UNLOCK/LOCK 机制。UNLOCK 允许编程寄存器，LOCK 更新已编程寄存器的实际内容。任何其他值都会导致 LOCKED 状态，并丢弃任何挂起更改。

PROT_CFG Offset address: 002_H

Protection configuration register - *R2) Reset values see: Table 65



Field	Bits	Type	Description
KEY	15:0	rw	**KEY value** $B5CA_H$ Registers unlocked $D396_H$ Registers locked

表 65 PROT_CFG 的复位值

Reset	Reset value	Note
	$D396_H$	Reset class R2)

18.11 器件反映状态配置寄存器 *R2)

DEV_RS_CFG3 Offset address: 003_H

Device reflected status configuration Register *R2) Reset values see: Table 66

15	14	13	12	11	10	9	8
Res					VMON2_EN	VMON1_EN	BOOST_EN
r					r	r	r

7	6	5	4	3	2	1	0
BUCKINT_EN	QUC_EN	BUCKCORE_EN	QCO_EN	QVR_EN	FSM_STATEREQ		
r	r	r	r	r	r		

Field	Bits	Type	Description
FSM_STATEREQ	2:0	r	**Request for device state transition.** 000_B NONE 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B NONE 111_B NONE
QVR_EN	3	r	**Enable request for reference voltage.** 0_B Disabled 1_B Enabled
QCO_EN	4	r	**Enable request for communication LDO.** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	r	**Enable request for BUCKCORE** 0_B Disabled 1_B Enabled
QUC_EN	6	r	**Enable request for QUC** 0_B Disabled 1_B Enabled
BUCKINT_EN	7	r	**Enable request for BUCK interface** 0_B Disabled 1_B Enabled
BOOST_EN	8	r	**Enable request for Boost** 0_B Disabled 1_B Enabled

（表格续下页……）

（续）

Field	Bits	Type	Description
VMON1_EN	9	r	**Enable request for External Monitoring1** 0_B Disabled 1_B Enabled
VMON2_EN	10	r	**Enable request for External Monitoring2** 0_B Disabled 1_B Enabled

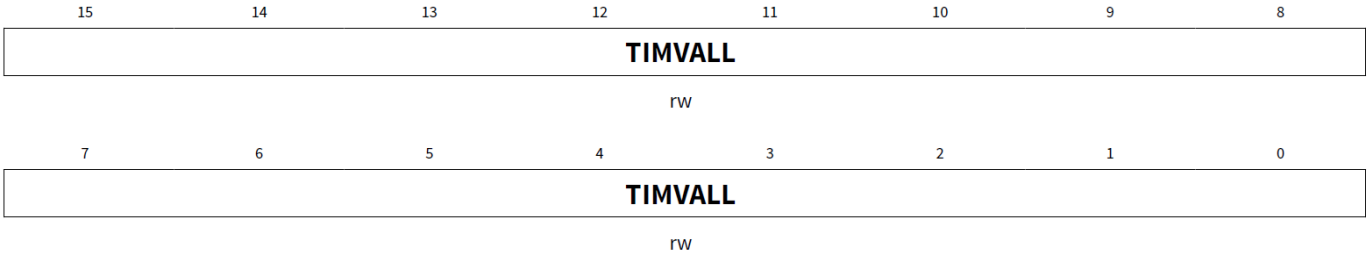
表 66 DEV_RS_CFG3 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.12 唤醒计时器 LSB 值 (*R2)

WUT_CFG0 Offset address: 004_H

Wake up timer LSB Value [*R2) Reset values see: Table 67



Field	Bits	Type	Description
TIMVALL	15:0	rw	**Wake timer compare value, 16bit lsb**

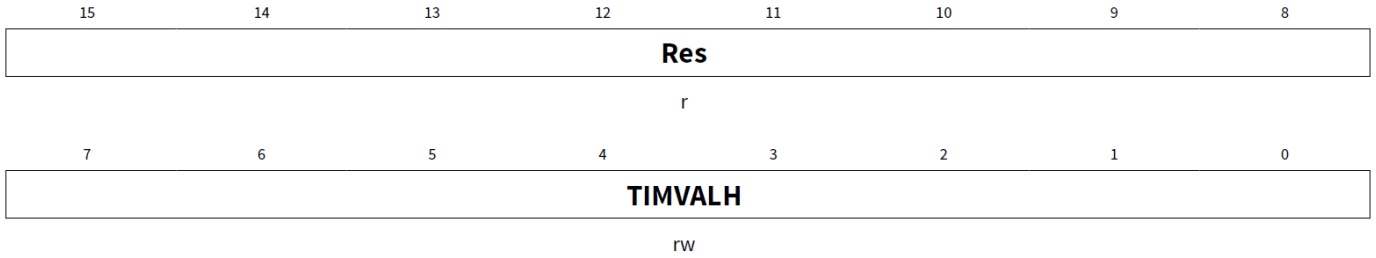
表 67 WUT_CFG0 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.13 唤醒计时器 MSB 值 (*R2)

WUP_CFG1 Offset address: 005_H

Wake up timer MSB Value [*R2) Reset values see: Table 68



Field	Bits	Type	Description
TIMVALH	7:0	rw	**Wake timer compare value (23:16) (msb)**

表 68 WUP_CFG1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.14 应用 1 的唤醒状态标志 *R2)

WAKE_STAT_APP1 Offset address: 006_H

Wakeup status flags for Application 1 *R2) Reset values see: Table 69

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SPI	WUT	Res	ENA	WAK
r			rw1c	rw1c	r	rw1c	rw1c

Field	Bits	Type	Description
WAK	0	rw1c	**Wakeup by WAK signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of WAK** 0_B No event detected 1_B Event detected
ENA	1	rw1c	**Wake by ENA signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of ENA** 0_B No event detected 1_B Event detected
WUT	3	rw1c	**Wakeup by wake timer** 0_B No event detected 1_B Event detected
SPI	4	rw1c	**Wakeup by SPI** 0_B No event detected 1_B Event detected

表 69 WAKE_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.15 应用 2 的唤醒状态标志 *R2)

WAKE_STAT_APP2 Offset address: 007_H

Wakeup status flags for Application 2 *R2) Reset values see: Table 70

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SPI	WUT	Res	ENA	WAK
r			rw1c	rw1c	r	rw1c	rw1c

Field	Bits	Type	Description
WAK	0	rw1c	**Wakeup by WAK signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of WAK** 0_B No event detected 1_B Event detected
ENA	1	rw1c	**Wake by ENA signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of ENA** 0_B No event detected 1_B Event detected
WUT	3	rw1c	**Wakeup by wake timer, bit will also be set if device leaves STANDBY state because of wakeup timer expired** 0_B No event detected 1_B Event detected
SPI	4	rw1c	**Wakeup by SPI from SLEEP state** 0_B No event detected 1_B Event detected

表 70 WAKE_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.16 应用 1 的 INIT 和 REDUCED OPERATION 错误状态标志 *R2)

INIT_ERR_APP1

Offset address: 008_H

INIT and REDUCED OPERATION Error Status flags for Application 1 *R2)

Reset values see: Table 71

15	14	13	12	11	10	9	8
HARDRES	SOFTRES	Res		REDOP_RES2	REDOP_RES1	Res	
rw1c	rw1c	r		rw1c	rw1c	r	

7	6	5	4	3	2	1	0
ERR2	ERR1	Res	FWD2_EC	FWD1_EC	WWD2_EC	WWD1_EC	VMONF
rw1c	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VMONF	0	rw1c	**Voltage monitor failure which lead to INIT (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
WWD1_EC	1	rw1c	**Window watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
WWD2_EC	2	rw1c	**Window watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD1_EC	3	rw1c	**Functional watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD2_EC	4	rw1c	**Functional watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
ERR1	6	rw1c	**ERR1 failure** 0_B No fault 1_B Fault occurred
ERR2	7	rw1c	**ERR2 failure** 0_B No fault 1_B Fault occurred
REDOP_RES1	10	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired once (same timer as INIT timer)** 0_B No fault 1_B Fault occurred

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Field	Bits	Type	Description
REDOP_RES2	11	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired twice (same timer as INIT timer); Move to INIT is triggered** 0_B No fault 1_B Fault occurred
SOFTRES	14	rw1c	**Soft reset generated** 0_B No soft reset occurred 1_B Soft reset occurred
HARDRES	15	rw1c	**Hard reset generated because INIT timer expired twice** 0_B No hard reset occurred 1_B Hard reset occurred

表 71　　INIT_ERR_APP1的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.17 应用 2 的 INIT 和 REDUCED OPERATION 错误状态标志 *R2)

INIT_ERR_APP2

Offset address: 009_H

INIT and REDUCED OPERATION Error Status flags for Application 2 *R2)

Reset values see: Table 72

15	14	13	12	11	10	9	8
HARDRES	SOFTRES	Res		REDOP_RES2	REDOP_RES1	Res	
rw1c	rw1c	r		rw1c	rw1c	r	

7	6	5	4	3	2	1	0
ERR2	ERR1	Res	FWD2_EC	FWD1_EC	WWD2_EC	WWD1_EC	VMONF
rw1c	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VMONF	0	rw1c	**Voltage monitor failure which lead to INIT (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
WWD1_EC	1	rw1c	**Window watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
WWD2_EC	2	rw1c	**Window watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD1_EC	3	rw1c	**Functional watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD2_EC	4	rw1c	**Functional watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
ERR1	6	rw1c	**error1 monitor failure** 0_B No fault 1_B Fault occurred
ERR2	7	rw1c	**error2 monitor failure** 0_B No fault 1_B Fault occurred
REDOP_RES1	10	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired once** 0_B No fault 1_B Fault occurred

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Field	Bits	Type	Description
REDOP_RES2	11	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired twice** 0_B No fault 1_B Fault occurred
SOFTRES	14	rw1c	**Soft reset generated because the Init timer expired once** 0_B No soft reset occurred 1_B Soft reset occurred
HARDRES	15	rw1c	**Hard reset generated because Init timer expired twice** 0_B No hard reset occurred 1_B Hard reset occurred

表 72　　INIT_ERR_APP2的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.18 触发 INT1 的应用 1 中断标志 *R2)

IF1 Offset address: $00A_H$

Interrupt flags for Application 1 that trigger INT1 *R2) Reset values see: Table 73

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
INTMISS	ABIST	Res	OT_WRN_OC_ERR	MON	SPI_FAIL	WUT_EVT	SYSFAIL_ERR
r	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
SYSFAIL_ERR	0	rw1c	**INT1 is triggered, because a system event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occured
WUT_EVT	1	rw1c	**INT1 is triggered, because a wake up event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
SPI_FAIL	2	rw1c	**INT1 is triggered, because a SPI_FAIL has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
MON	3	rw1c	**INT1 is triggered, because a monitoring event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
OT_WRN_OC_ERR	4	rw1c	**INT1 is triggered, because a overtemperature warning or overcurrent has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
ABIST	6	rw1c	**Requested ABIST operation performed or interrupted. ABIST is not continued automatically.** 0_B No interrupt 1_B Interrupt occurred
INTMISS	7	r	**Interrupt INT1 has not been serviced within tINTTO time** 0_B No interrupt 1_B Interrupt occurred

表 73 IF1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.19 触发 INT2 的应用 2 中断标志 *R2) *R2)

IF2 Offset address: $00B_H$

Interrupt flags for Application 2 that trigger INT2 *R2) Reset values see: Table 74

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
INTMISS	ABIST	Res	OT_WRN_OC_ERR	MON	SPI_FAIL	WUT_EVT	SYSFAIL_ERR
r	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
SYSFAIL_ERR	0	rw1c	**INT2 is triggered, because a system event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
WUT_EVT	1	rw1c	**INT2 is triggered, because a wake up event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
SPI_FAIL	2	rw1c	**INT2 is triggered, because a SPI_FAIL has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
MON	3	rw1c	**INT2 is triggered, because a monitoring event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
OT_WRN_OC_ERR	4	rw1c	**INT2 is triggered, because a overtemperature warning or overcurrent has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
ABIST	6	rw1c	**Requested ABIST operation performed or interrupted. ABIST is not continued automatically.** 0_B No interrupt 1_B Interrupt occurred
INTMISS	7	r	**Interrupt INT2 has not been serviced within tINTTO time** 0_B No interrupt 1_B Interrupt occurred

表 74 IF2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.20 触发 INT1 的应用 1 系统状态标志 *R2)

SYS_STAT_APP1

Offset address: $00C_H$

System status flags for Application 1 that trigger INT1 *R2)

Reset values see: Table 75

15	14	13	12	11	10	9	8
Res						BUCKCORE_SVS_NOK	BUCKCORE_SVS_OK
r						rw1c	rw1c

7	6	5	4	3	2	1	0
APP2_FAIL	ERR1_ERR	ERR0_ERR	FSM_NOOP	FSM_TRFAIL	FWD1_ERR	WWD1_ERR	Res
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	r

Field	Bits	Type	Description
WWD1_ERR	1	rw1c	**Window watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event occurred 1_B Event detected
FWD1_ERR	2	rw1c	**Functional watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event occured 1_B Event occured
FSM_TRFAIL	3	rw1c	**Transition to low power state (STANDBY/SLEEP) failed** 0_B No occurrence 1_B Transition unscuccessful
FSM_NOOP	4	rw1c	**Requested state transition via DEVCTRL could not be performed because either path between current state and requested state does not exist (eg. INIT to SLEEP), or paths exists but pre-conditions are not satisfied (e.g. INIT to NORMAL, but WWD enabled and not serviced).** 0_B No occurrence 1_B Transition was not executed
ERR0_ERR	5	rw1c	**ERR0 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
ERR1_ERR	6	rw1c	**ERR1 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
APP2_FAIL	7	rw1c	**Application 2 entered REDUCED OPERATION** 0_B No occurrence 1_B Application 2 fault occurred

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Field	Bits	Type	Description
BUCKCORE_SVS_OK	8	rw1c	**BUCK CORE static voltage scaling procedure completed successfully.** 0_B Not completed 1_B Completed successfully
BUCKCORE_SVS_NOK	9	rw1c	**BUCK CORE static voltage scaling procedure was unsuccessful, because the device is not in state NORMAL or INIT or BUCKCORE output voltage is set to 1.15 V.** 0_B No occurrence 1_B BUCK CORE voltage scaling was unsuccessful

表 75 SYS_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.21 触发 INT2 的应用 2 系统状态标志 *R2)

SYS_STAT_APP2
System status flags for Application 2 that trigger INT2 *R2)

Offset address: $00D_H$
Reset values see Table 76

15	14	13	12	11	10	9	8
Res						BUCKCORE_SVS_NOK	BUCKCORE_SVS_OK
r						rw1c	rw1c

7	6	5	4	3	2	1	0
APP1_FAIL	ERR2_ERR	ERR0_ERR	FSM_NOOP	FSM_TRFAIL	FWD2_ERR	WWD2_ERR	Res
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	r

Field	Bits	Type	Description
WWD2_ERR	1	rw1c	**Window watchdog 2 error interrupt flag. Service was incorrect or missed.** 0_B No event occurred 1_B Event detected
FWD2_ERR	2	rw1c	**Functional watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event detected 1_B Event detected
FSM_TRFAIL	3	rw1c	**Transition to low power state (STANDBY/SLEEP) failed** 0_B No occurrence 1_B Transition unsuccessful
FSM_NOOP	4	rw1c	**Requested state transition via DEVCTRL could not be performed because either path between current state and requested state does not exist (eg. INIT to SLEEP), or paths exists but pre-conditions are not satisfied (e.g. INIT to NORMAL, but WWD enabled and not serviced).** 0_B No occurrence 1_B Transition was not executed
ERR0_ERR	5	rw1c	**ERR0 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
ERR2_ERR	6	rw1c	**ERR2 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
APP1_FAIL	7	rw1c	**Application 1 entered REDUCED OPERATION** 0_B No occurrence 1_B Application 1 fault occurred

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Field	Bits	Type	Description
BUCKCORE_SVS_OK	8	rw1c	**BUCK CORE static voltage scaling procedure completed successfully.** 0_B Not completed 1_B Completed successfully
BUCKCORE_SVS_NOK	9	rw1c	**BUCK CORE static voltage scaling procedure was unsuccessful, because the device is not in state NORMAL or INIT or BUCKCORE output voltage is set to 1.15 V.** 0_B No occurrence 1_B BUCK CORE voltage scaling was unsuccessful

表 76 SYS_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.22 触发 INT1 的 SPI 故障状态标志 *R2)

SPI_FAIL_STAT_APP1 Offset address: $00E_H$

SPI failure status flags that triggers INT1 *R2) Reset values see: Table 77

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			LOCK	CS_TO	ADR	FR_LEN	CRC
r			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
CRC	0	rw1c	**CRC error in SPI frame** 0_B No error 1_B CRC wrong
FR_LEN	1	rw1c	**Invalid frame length, number of detected SPI clock cycles different than 32** 0_B Frame length ok 1_B Frame length incorrect
ADR	2	rw1c	**Invalid address in SPI frame** 0_B No occurrence 1_B Address not existing
CS_TO	3	rw1c	**Error in duration of SPI transaction, nCS low for more than 2 ms** 0_B No occurrence 1_B CSN timeout
LOCK	4	rw1c	**Error during LOCK/UNLOCK procedure or write attempts to locked registers** 0_B No occurrence 1_B LOCK/UNLOCK sequence failed

表 77 SPI_FAIL_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.23 触发 INT2 的应用 2 SPI 状态标志 *R2)

SPI_FAIL_STAT_APP2 Offset address: $00F_H$

SPI status flags for Application 2 that trigger INT2 *R2) Reset values see: Table 78

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			LOCK	CS_TO	ADR	FR_LEN	CRC
r			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
CRC	0	rw1c	**CRC error in SPI frame** 0_B No error 1_B CRC wrong
FR_LEN	1	rw1c	**Invalid frame length, number of detected SPI clock cycles different than 32** 0_B Frame length ok 1_B Frame length incorrect
ADR	2	rw1c	**Invalid address in SPI frame** 0_B No occurrence 1_B Address not existing
CS_TO	3	rw1c	**Error in duration of SPI transaction, nCS low for more than 2 ms** 0_B No occurrence 1_B CSN timeout
LOCK	4	rw1c	**Error during LOCK/UNLOCK procedure or write attempts to locked registers** 0_B No occurrence 1_B LOCK/UNLOCK sequence failed

表 78 SPI_FAIL_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.24 应用 1 的监测状态标志寄存器 2 *R2)

UV_STAT_APP1 Offset address: 010_H

Monitor status flags register 2 for Application 1 *R2) Reset values see: Table 79

15	14	13	12	11	10	9	8
Res				INTSUP_VDD2V5_UV	INTSUP_IVCC_UV	BUCKIF	VMON2
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QUC	1	rw1c	**QUC under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QST	2	rw1c	**QST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BUCKCORE	3	rw1c	**BUCKCORE under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QCO	4	rw1c	**QCO under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QVR	5	rw1c	**QVR under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BOOST	6	rw1c	**BOOST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON1	7	rw1c	**VMON1 under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON2	8	rw1c	**VMON2 under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred

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Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_IVCC_UV	10	rw1c	**Internal supply IVCC under voltage status flag, *R1)** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_VDD2V5_UV	11	rw1c	**Internal supply VDD 2.5 V under voltage status flag, *R1)** 0_B No occurrence 1_B Undervoltage occurred

表 79　　UV_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.25 应用 2 的监测状态标志寄存器 2 *R2)

UV_STAT_APP2 Offset address: 011_H

Monitor status flags register 2 for Application 2 *R2) Reset values see: Table 80

15	14	13	12	11	10	9	8
Res				INTSUP_2V5_UV	INTSUP_IVCC_UV	BUCKIF	VMON2
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QUC	1	rw1c	**QUC under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QST	2	rw1c	**QST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BUCKCORE	3	rw1c	**BUCKCORE under voltage status flag** 0_B No occurrence 1_B Undervolage occurred
QCO	4	rw1c	**QCO under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QVR	5	rw1c	**QVR under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BOOST	6	rw1c	**Boost voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON1	7	rw1c	**VMON1 voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurrence
VMON2	8	rw1c	**Mon2 voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred

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Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_IVCC_UV	10	rw1c	**IVCC voltage under voltage status flag *R1)** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_2V5_UV	11	rw1c	**2V5 voltage under voltage status flag *R1)** 0_B No occurrence 1_B Undervoltage occurred

表 80　　UV_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.26 过温警告和过流状态标志 *R2)

OT_WRN_OC_STAT_APP1

Over temperature warning and over current status flags *R2)

Offset address: 012_H

Reset values see: Table 81

15	14	13	12	11	10	9	8
Res							BOOST_OC
r							rw1c

7	6	5	4	3	2	1	0
IVCC_OC	QUC_OTWRN	BOOST_OTWRN	BUCKIF_OTWRN	BUCKCORE_OTWRN	QVR_OC	QCO_OTWRN	QST_OC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_OC	0	rw1c	**QST over current** 0_B No occurrence 1_B Over current occurred
QCO_OTWRN	1	rw1c	**QCO over temperature warning** 0_B No occurrence 1_B Overtemperature warning
QVR_OC	2	rw1c	**QVR over current** 0_B No occurrence 1_B Over current occurred
BUCKCORE_OTWRN	3	rw1c	**BUCKCORE overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BUCKIF_OTWRN	4	rw1c	**BUCKIF overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BOOST_OTWRN	5	rw1c	**BOOST overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
QUC_OTWRN	6	rw1c	**QUC over temperature warning** 0_B No occurrence 1_B Overtemperature warning
IVCC_OC	7	rw1c	**IVCC over current warning** 0_B No occurrence 1_B Over current occurred
BOOST_OC	8	rw1c	**BOOST over current** 0_B No occurrence 1_B Over current occurred

表 81 OT_WRN_OC_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.27 应用 2 的过温警告/过流状态标志 *R2)

OT_WRN_OC_STAT_APP2

Over temperature warning /Over current status flags for Application 2 *R2)

Offset address: 013_H

Reset values see: Table 82

15	14	13	12	11	10	9	8
Res							BOOST_OC
r							rw1c

7	6	5	4	3	2	1	0
IVCC_OC	QUC_OTWRN	BOOST_OTWRN	BUCKIF_OTWRN	BUCKCORE_OTWRN	QVR_OC	QCO_OTWRN	QST_OC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_OC	0	rw1c	**QST over current** 0_B No occurrence 1_B Over current occurred
QCO_OTWRN	1	rw1c	**QCO over temperature warning** 0_B No occurrence 1_B Overtemperature warning
QVR_OC	2	rw1c	**QVR over current** 0_B No occurrence 1_B Over current occurred
BUCKCORE_OTWRN	3	rw1c	**BUCKCORE overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BUCKIF_OTWRN	4	rw1c	**BUCKIF overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BOOST_OTWRN	5	rw1c	**BOOST overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
QUC_OTWRN	6	rw1c	**QUC over temperature warning** 0_B No occurrence 1_B Overtemperature warning
IVCC_OC	7	rw1c	**IVCC over current warning** 0_B No occurrence 1_B Over current occurred
BOOST_OC	8	rw1c	**BOOST over current** 0_B No occurrence 1_B Over current occurred

表 82 OT_WRN_OC_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.28 电压监测状态 *R2)

VMON_STAT

Offset address: 014_H

Voltage monitor status *R2)

Reset values see: Table 83

15	14	13	12	11	10	9	8
Res					VMON2_ST	VMON1_ST	IVCC_ST
r					r	r	r

7	6	5	4	3	2	1	0
QUC_ST	PREREG_ST	BOOST_ST	BUCKINT_ST	QVR_ST	QCO_ST	BUCKCORE_ST	QST_ST
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
QST_ST	0	r	**Standby LDO voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BUCKCORE_ST	1	r	**Core voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QCO_ST	2	r	**Communication voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QVR_ST	3	r	**Reference voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BUCKINT_ST	4	r	**Buckint voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BOOST_ST	5	r	**Boost voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
PREREG_ST	6	r	**Prereg voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QUC_ST	7	r	**QUC voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
IVCC_ST	8	r	**IVCC voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK

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Field	Bits	Type	Description
VMON1_ST	9	r	**MON1 voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
VMON2_ST	10	r	**MON2 voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK

表 83 VMON_STAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.29 器件状态寄存器 *R2)

DEV_STAT Offset address: 015H

Device status register *R2) Reset values see: Table 84

15	14	13	12	11	10	9	8
VMON2_AUTO_DET	VMON1_AUTO_DET	BOOST_AUTO_DET	BUCKINT_AUTO_DET	SSW_AUTO_DET	VMON2_EN	VMON1_EN	BOOST_EN
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
BUCKIF_EN	QUC_EN	BUCKCORE_EN	QCO_EN	QVR_EN	STATE		
r	r	r	r	r	r		

Field	Bits	Type	Description
STATE	2:0	r	**Current device state** 000_B reserved 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B REDUCED_OPERATION 111_B reserved
QVR_EN	3	r	**QVR status** 0_B Disabled 1_B Enabled
QCO_EN	4	r	**QCO status** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	r	**BUCKCORE status** 0_B Disabled 1_B Enabled
QUC_EN	6	r	**QUC status** 0_B Disabled 1_B Enabled
BUCKIF_EN	7	r	**BUCKIF status** 0_B Disabled 1_B Enabled
BOOST_EN	8	r	**BOOST status** 0_B Disabled 1_B Enabled

（表格续下页……）

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Field	Bits	Type	Description
VMON1_EN	9	r	**External voltage monitor channel 1 status** 0_B Disabled 1_B Enabled
VMON2_EN	10	r	**External voltage monitor channel 2 status** 0_B Disabled 1_B Enabled
SSW_AUTO_DET	11	r	**Safety switch auto detect** 0_B not detected 1_B detected
BUCKINT_AUTO_DET	12	r	**BUCKINT autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
BOOST_AUTO_DET	13	r	**BOOST autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
VMON1_AUTO_DET	14	r	**VMON1 autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
VMON2_AUTO_DET	15	r	**VMON2 autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected

表 84　　DEV_STAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.30 DC-DC 开关频率变化 *R2)

DCDC_FREQ_SYNC Offset address: 016_H

DC-DC switching frequency change *R2) Reset values see: Table 85

15	14	13	12	11	10	9	8
PREREG_BOOST_PHSHFT	BOOST_BUCKIF_PHSHFT	Res			BOOST_DRIVER_CONFIG		BUCKIF_DRIVER_CONFIG
rw	rw	r			rw		rw

7	6	5	4	3	2	1	0
BUCKIF_DRIVER_CONFIG	BUCKCORE_DRIVER_CONFIG		PREREG_DRIVER_CONFIG		DCDC_FREQSEL		
rw	rw		rw		rw		

Field	Bits	Type	Description
DCDC_FREQSE L	2:0	rw	**DC-DC switching frequency (fDCDC) change** 000_B 1.8 MHz 001_B 1.9 MHz 010_B 2.0 MHz 011_B 2.1 MHz 100_B 2.2 MHz - default/center value 101_B 2.3 MHz 110_B 2.4 MHz 111_B 2.4 MHz
PREREG_DRIVER_CONFIG	4:3	rw	**Drive strength configuration for BUCK PREREG** 00_B Full strenght 01_B 66% of full strength 10_B 33% of full strength 11_B **RESERVED**: Do not use, currently selects 33% strength
BUCKCORE_DRIVER_CONFIG	6:5	rw	**Drive strength configuration for BUCK CORE** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B Do not use, currently selects 25% strength
BUCKIF_DRIVER_CONFIG	8:7	rw	**Drive strength configuration for BUCK IF** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B **RESERVED**: Do not use, currently selects 25% strength

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Field	Bits	Type	Description
BOOST_DRIVER_CONFIG	10:9	rw	**Drive strength configuration for BOOST** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B **RESERVED**: Do not use, currently selects 25% strength
BOOST_BUCKIF_PHSHFT	14	rw	**180 degree phase shift between BOOST and BUCKIF** 0_B Disable phase shift 1_B Enable phase shift
PREREG_BOOST_PHSHFT	15	rw	**180 degree phase shift between BOOST and PREREG** 0_B Disable Phase Shift 1_B Enable Phase Shift

表 85　　DCDC_FREQ_SYNC 的复位值

Reset	Reset value	Note
	0004_H	Reset class R2)

18.31 DC-DC 频率展频控制寄存器 *R2)

FREQ_SPREAD
DC-DC Frequency spread-spectrum control register *R2)

Offset address: 017_H
Reset values see: Table 86

15	14	13	12	11	10	9	8
Res		FRE_SP_AMPLITUDE				FRE_SP_FSTEP	
r		rw				rw	

7	6	5	4	3	2	1	0
FRE_SP_TIMEBASE			FRE_SP_METH			FRE_SP_BUCK_IF_EN	FRE_SP_EN
rw			rw			rw	rw

Field	Bits	Type	Description
FRE_SP_EN	0	rw	**Enable spread spectrum** 0_B Disabled 1_B Enabled
FRE_SP_BUCK_IF_EN	1	rw	**Enable spread spectrum for BUCKIF (ignored when FRE_SP_EN is 0)** 0_B Disabled 1_B Enabled
FRE_SP_METH	4:2	rw	**These bits define the method for vary the frequency spectrum** 000_B Triangle 001_B Triangle with dithering 010_B Triangle with pseudorandom period 011_B Triangle with pseudorandom period and dithering 100_B Triangle with pseudorandom half-period 101_B Triangle with pseudorandom half-period and dithering 110_B Triangle with pseudorandom ramp 111_B Triangle with pseudorandom ramp and dithering
FRE_SP_TIMEBASE	7:5	rw	**These bits define the timings for varying the frequency spectrum** 000_B Frequency changes every 3.5 us 001_B Frequency changes every 7 us 010_B Frequency changes every 10.5 us 011_B Frequency changes every 14 us 100_B Frequency changes every 17.5 us 101_B Frequency changes every 21 us 110_B Frequency changes every 24.5 us 111_B Frequency changes every 28 us
FRE_SP_FSTEP	9:8	rw	**These bits define the frequency step for varying the frequency spectrum** 00_B 0.625% variation 01_B 1.25% variation 10_B 2.5% variation 11_B **RESERVED**: Do not use. Currently maps to 2.5% variation

（表格续下页……）

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Field	Bits	Type	Description
FRE_SP_AMPLITUDE	13:10	rw	**Defines the maximum width of the triangular ramp with respect to the center value** 0_H 12 frequency steps 1_H 1 frequency step 2_H 2 frequency steps 3_H 3 frequency steps 4_H 4 frequency steps 5_H 5 frequency steps 6_H 6 frequency steps 7_H 7 frequency steps 8_H 8 frequency steps 9_H 9 frequency steps A_H 10 frequency steps B_H 11 frequency steps C_H 12 frequency steps D_H 13 frequency steps E_H 14 frequency steps F_H 15 frequency steps

表 86 FREQ_SPREAD 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.32 ABIST control 0 *R2)

ABIST_CTRL0 Offset address: 018_H

ABIST control 0 *R2) Reset values see: Table 87

15	14	13	12	11	10	9	8
Res							ALL
r							rwh

7	6	5	4	3	2	1	0
STATUS				INT	SINGLE	PATH	START
r				rw	rw	rwh	rwh

Field	Bits	Type	Description
START	0	rwh	**Start ABIST operation, the operation itself will be started. This bit is cleared after ABIST operation has been performed** 0_B Operation done or not started 1_B Start operation
PATH	1	rwh	**Select the path which should be covered by ABIST operation** 0_B Comparator only 1_B Comparator and correspondig deglitching logic
SINGLE	2	rw	**Select whether a single comparator shall be tested or all comparators in predefined sequence** 0_B Predefined sequence 1_B Single comparator test
INT	3	rw	**Selection for safe state related comparators or interrupt related comparators** 0_B Safe state related comparators 1_B Interrupt related comparators
STATUS	7:4	r	**ABIST global status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared** 5_H Selected ABIST operation performed without errors A_H Selected ABIST operation performed with errors, check respective ABIST_SELECTx registers
ALL	8	rwh	**When set to '1' all comparators are automatically selected.** 0_B Comparators executed as selected in ABIST_CTRL0 and ABIST_SELECT0/1/2 1_B All comparators are tested with PATH = 0 and SINGLE = 0

表 87 ABIST_CTRL0 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.33 ABIST control 1 *R2)

ABIST_CTRL1 Offset address: 019_H

ABIST control 1 *R2) Reset values see: Table 88

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SS2_EN_BIST	SS1_EN_BIST	ABIST_CLK_EN	Res	OV_1V5_TRIG
r			rw	rw	rw	r	rw

Field	Bits	Type	Description
OV_1V5_TRIG	0	rw	**Enable overvoltage trigger for protected 1.5 V comparator for analog safe state control** 0_B Disabled 1_B Enabled
ABIST_CLK_EN	2	rw	**Select ABIST clock to generate local 2 MHz clock** 0_B Disable 1_B Enable
SS1_EN_BIST	3	rw	**Enables ABIST for SSO1. Requires ABIST_CTRL1.ABIST_CLK_EN=1 and ABIST_CTRL1.OV_1V5_TRIG=1** 0_B Disable 1_B Enable
SS2_EN_BIST	4	rw	**Enables ABIST for SSO2. Requires ABIST_CTRL1.ABIST_CLK_EN=1 and ABIST_CTRL1.OV_1V5_TRIG=1** 0_B Disable 1_B Enable

表 88 ABIST_CTRL1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.34 ABIST select 0 *R2)

ABIST_SELECT0 Offset address: $01A_H$

ABIST select 0 *R2) Reset values see: Table 89

15	14	13	12	11	10	9	8
R3FBL_OPEN	BUCKIF_SEVOV	BUCKCORE_SEVOV	PREREG_SEVOV	VDD2V5OV	IVCCOV	VMON2OV	VMON1OV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
7	6	5	4	3	2	1	0
BOOSTOV	BUCKIFOV	QVROV	QCOOV	BUCKCOREOV	QSTOV	QUCOV	PREREGOV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PREREGOV	0	rwh	**Select Pre-regulator OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QUCOV	1	rwh	**Select uC LDO OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QSTOV	2	rwh	**Select Standby LDO OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCOREOV	3	rwh	**Select Core voltage OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QCOOV	4	rwh	**Select COM OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QVROV	5	rwh	**Select VREF OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKIFOV	6	rwh	**Buck_int OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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Field	Bits	Type	Description
BOOSTOV	7	rwh	**BOOST OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON1OV	8	rwh	**VMON1 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON2OV	9	rwh	**VMON2 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
IVCCOV	10	rwh	**IVCCOV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD2V5OV	11	rwh	**VDD2V5 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
PREREG_SEVOV	12	rwh	**Select Pre-regulator Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCORE_SEVOV	13	rwh	**Select BUCKCORE Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKIF_SEVOV	14	rwh	**Select BUCKINT Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
R3FBL_OPEN	15	rwh	**Select R3FBL comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

表 89　　ABIST_SELECT0 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.35 ABIST select 1 *R2)

ABIST_SELECT1

ABIST select 1 *R2)

Offset address: $01B_H$

Reset values see: Table 90

15	14	13	12	11	10	9	8
Res		BST_DEEP_UV	BSTIUV	VDD2V5UV	IVCCUV	VMON2UV	VMON1UV
r		rwh	rwh	rwh	rwh	rwh	rwh

7	6	5	4	3	2	1	0
BOOSTUV	BUCKINTUV	QVRUV	QCOUV	BUCKCOREUV	QSTUV	QUCUV	PREREGUV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PREREGUV	0	rwh	**Select pre regulator UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QUCUV	1	rwh	**Select uC UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QSTUV	2	rwh	**Select STBY UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCOREUV	3	rwh	**Select VCORE UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QCOUV	4	rwh	**Select COM UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QVRUV	5	rwh	**Select VREF UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKINTUV	6	rwh	**Select Buck_int UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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Field	Bits	Type	Description
BOOSTUV	7	rwh	**Select Boost UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON1UV	8	rwh	**Select VMON1 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON2UV	9	rwh	**Select VMON2 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
IVCCUV	10	rwh	**Select IVCC UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD2V5UV	11	rwh	**Select VDD2V5 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BSTIUV	12	rwh	**BSTI UV comparator for ABIST operation** 0_B No error detected 1_B Error detected (during internal checks)
BST_DEEP_UV	13	rwh	**Select BST_DEEP_UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

表 90　　ABIST_SELECT1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.36 ABIST select 2 *R2)

ABIST_SELECT2
ABIST select 2 *R2)

Offset address: $01C_H$
Reset values see: Table 91

15	14	13	12	11	10	9	8
Res							VDD5V0OV
r							rwh

7	6	5	4	3	2	1	0
VDD5V0UV	VDD1V5OV	VDD1V5UV	BIASHI	BIASLOW	BG12OV	BG12UV	VBATOV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VBATOV	0	rwh	**Supply voltage VS1/2 is too high** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BG12UV	1	rwh	**Bandgap comparator UV condition** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BG12OV	2	rwh	**Bandgap comparator OV condition** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BIASLOW	3	rwh	**Bias current too low** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BIASHI	4	rwh	**Bias current too high** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD1V5UV	5	rwh	**Select internal 1.5 V domain undervoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected
VDD1V5OV	6	rwh	**Select internal 1.5 V domain overvoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected
VDD5V0UV	7	rwh	**Select internal 2.5 V domain undervoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected

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Field	Bits	Type	Description
VDD5V0OV	8	rwh	**Select internal 2.5 V domain overvoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected

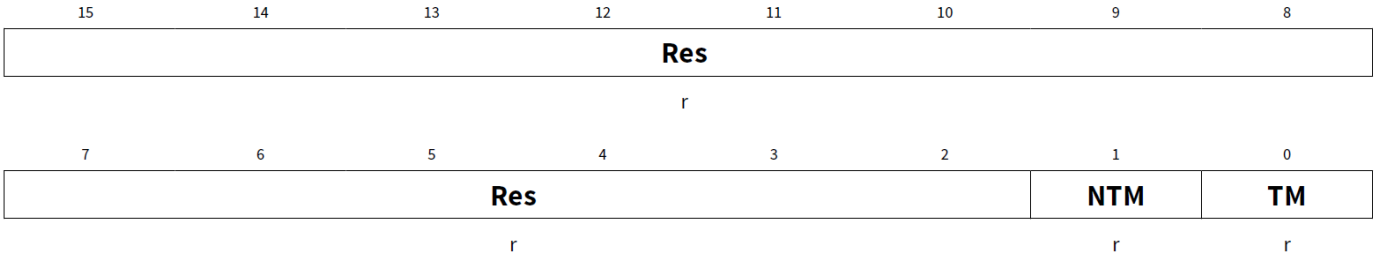
表 91 ABIST_SELECT2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.37 Global testmode *R2)

GTM Offset address: $01D_H$

Global testmode *R2) Reset values see: Table 92



Field	Bits	Type	Description
TM	0	r	**Test mode status** 0_B Device is in normal mode 1_B Device is in test mode
NTM	1	r	**Test mode status inverted** 0_B Device is in test mode 1_B Device is in normal mode

表 92 GTM 的复位值

Reset	Reset value	Note
	0002_H	Reset class R2)

18.38 有限操作反映状态配置 1 寄存器 - *R2)

REDOP_RS_CFG1

Reduced operation reflected status configuration 1 register - *R2)

Offset address: $01E_H$

Reset values see: Table 93

15	14	13	12	11	10	9	8
Res	SSO1TOSSO2_DEL			Res		INT2_DIS	INT1_DIS
r	r			r		r	r

7	6	5	4	3	2	1	0
SSO2_DEL			SSO1_DEL			Res	EN
r			r			r	r

Field	Bits	Type	Description
EN	0	r	**Enable reduced operation - *R3)** 0_B Disable 1_B Enable
SSO1_DEL	4:2	r	**Safe state output 1 delay (tSSO1_red) - only active if REDUCED OPERATION is enabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms
SSO2_DEL	7:5	r	**Safe state output 2 delay (tSSO2_red) - only active if REDUCED OPERATION is enabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms
INT1_DIS	8	r	**Disable generation of INT1 due to Cluster 2 entering REDUCED OPERATION** 0_B Allow generation of INT1 when application 2 enters REDUCED OPERATION 1_B Disable generation of INT1 related to application 2 entering REDUCED OPERATION

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Field	Bits	Type	Description
INT2_DIS	9	r	**Disable generation of INT2 due to Cluster 1 entering REDUCED OPERATION** 0_B Allow generation of INT2 when application 1 enters REDUCED OPERATION 1_B Disable generation of INT2 related to application 1 entering REDUCED OPERATION
SSO1TOSSO2_DEL	14:12	r	**Safe state output 2 delay to Safe state output 1 (tSSO2) when REDUCED OPERATION is disabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms

表 93　　REDOP_RS_CFG1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.39 ERR0 保护写入配置寄存器 *R2)

ERR0_PW_CFG Offset address: $01F_H$

ERR0 protection write configuration register *R2) Reset values see: Table 94

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR0 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR0 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR0 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR0 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 94 ERR0_PW_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R2)

18.40 ERR0 反映状态配置寄存器 *R3)

ERR0_RS_CFG Offset address: 020_H

ERR0 reflected status configuration register *R3) Reset values see: Table 95

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR0 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR0 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR0 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR0 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 95 ERR0_RS_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R3) C1

18.41 ERR1 保护写入配置寄存器 *R2)

ERR1_PW_CFG Offset address: 021_H

ERR1 protection write configuration register *R2) Reset values see: Table 96

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR1 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR1 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR1 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR1 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 96 ERR1_PW_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R2)

18.42 ERR1 反映状态配置寄存器 *R3_C1)

ERR1_RS_CFG Offset address: 022_H

ERR1 reflected status configuration register *R3_C1) Reset values see: Table 97

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR1 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR1 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR1 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR1 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 97 ERR1_RS_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R3) C1

18.43 ERR2 保护写入配置寄存器 *R2)

ERR2_PW_CFG Offset address: 023_H

ERR2 protection write configuration register *R2) Reset values see: Table 98

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR2 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR2 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR2 pin monitor** This bit has only an effect if REDOP_RS_CFG1.EN is 1 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR2 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 98 ERR2_PW_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R2)

18.44 ERR2 反映状态配置寄存器 *R3_C2)

ERR2_RS_CFG Offset address: 024_H

ERR2 reflected status configuration register *R3_C2) Reset values see: Table 99

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR2 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR2 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR2 pin monitor** This bit has only an effect if REDOP_RS_CFG1.EN is 1 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR2 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

表 99 ERR2_RS_CFG 的复位值

Reset	Reset value	Note
	0008_H	Reset class R3) C2

18.45 器件配置 1 寄存器 *R0)

DEV_CFG1 Offset address: 025_H

Device configuration 1 register *R0) value: 0206_H

15	14	13	12	11	10	9	8
Res						ABIST_EN	Res
r						rw	r

7	6	5	4	3	2	1	0
HWCFG_STAT				MPS_EN	RESET_DEL		
r				rwh	rwh		

Field	Bits	Type	Description
RESET_DEL	2:0	rwh	**Reset delay time (tRD); Starts upon QST, QUC and BUCKCORE are above their UV thresholds.** 000_B 200 µs 001_B 400 µs 010_B 800 µs 011_B 1 ms 100_B 2 ms 101_B 4 ms 110_B 10 ms 111_B 20 ms
MPS_EN	3	rwh	**Microcontroller programming support enable** 0_B Disabled 1_B Enabled
HWCFG_STAT	7:4	r	**This bit reflects the status of the hardware configuration pin** 0_H 1 kOhm 1_H 2.2 kOhm 2_H 3.3 kOhm 3_H 4.7 kOhm 4_H 6.8 kOhm 5_H 10 kOhm 6_H 15 kOhm 7_H Reserved value 8_H Reserved value 9_H 22 kOhm A_H 33 kOhm B_H 47 kOhm C_H 68 kOhm D_H 100 kOhm E_H 150 kOhm F_H 200 kOhm

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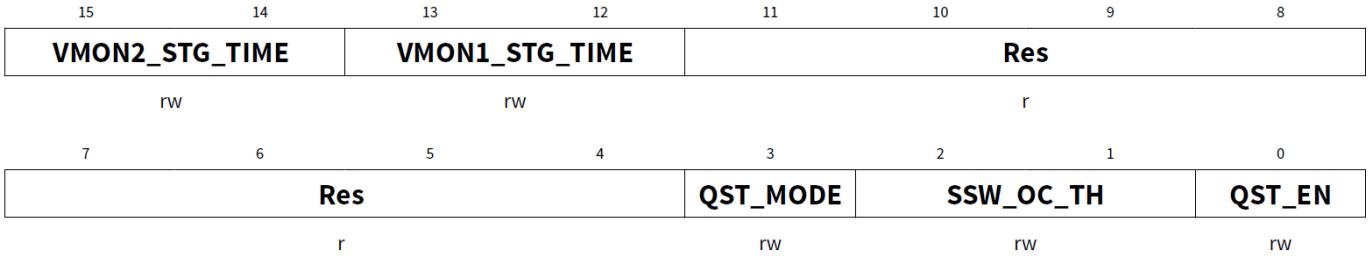
Field	Bits	Type	Description
ABIST_EN	9	rw	**Autostart of analog built in self test for voltage monitoring when waking up from FAILSAFE, STANDBY and POWERDOWN.** 0_B ABIST only executed when waking up from STANDBY (if WUT and QST are both OFF) or from POWERDOWN 1_B ABIST executed when waking up from STANDBY or from POWERDOWN or from FAILSAFE

18.46 器件受保护写入配置 2 寄存器 *R0)

DEV_PW_CFG2 Offset address: 026_H

Device protected write configuration 2 register *R0) Value: $F001_H$



Field	Bits	Type	Description
QST_EN	0	rw	**Activation of standby LDO** 0_B Disabled 1_B Enabled
SSW_OC_TH	2:1	rw	**Safety switch overcurrent detection threshold.** 00_B 0.755 V 01_B 0.944 V 10_B 1.04 V 11_B 1.22 V
QST_MODE	3	rw	**Selects between 2 different modes of controlling standby LDO via QSTEN** 0_B **PMIC_MODE**: QST is selectable only when the device is moving to STANDBY. QST is on in all other states, independently of QST_EN. 1_B **USER_MODE**: QST supply on or off,can be configured by QST_EN
VMON1_STG_TIME	13:12	rw	**Filter time to detect a short-to-ground on external voltage monitor channel 1** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms
VMON2_STG_TIME	15:14	rw	**Filter t ime to detect a short-to-ground on external voltage monitor channel 2** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms

18.47 器件反映状态配置 2 寄存器 *R0)

DEV_RS_CFG2 Offset address: 027_H

Device reflected status configuration 2 register *R0) value: $F001_H$

15	14	13	12	11	10	9	8
VMON2_STG_TIME		VMON1_STG_TIME		Res			
r		r		r			

7	6	5	4	3	2	1	0
Res				QST_MODE	SSW_OC_TH		QST_EN
r				r	r		r

Field	Bits	Type	Description
QST_EN	0	r	**Activation of standby LDO** 0_B Disabled 1_B Enabled
SSW_OC_TH	2:1	r	**Safety switch overcurrent detection threshold.** 00_B 0.755 V 01_B 0.944 V 10_B 1.04 V 11_B 1.22 V
QST_MODE	3	r	**Selects between 2 different modes of controlling standby LDO via QSTEN** 0_B **PMIC_MODE**: QST is selectable only when the device is moving to STANDBY. QST is on in all other states, independently of QST_EN. 1_B **USER_MODE**: QST supply on or off,can be configured by QST_EN
VMON1_STG_TIME	13:12	r	**Time to detect a short-to-ground on external voltage monitor channel 1** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms
VMON2_STG_TIME	15:14	r	**Time to detect a short-to-ground on external voltage monitor channel 2** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms

18.48 应用 1 的系统故障状态寄存器 *R1)

SYSFAIL_STAT_APP1 Offset address: 029_H

System failure status register for application 1 *R1) Reset values see: Table 100

15	14	13	12	11	10	9	8
Res				ABIST	CFGE	PREREG_COSW	INTSUP_IVCC
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
QST	ERR0	FSM_INITTIMER	VMON	OT	BUCK_CORE_VOLTSEL	BUCKIF_VOLTSEL	QST_QUC_VOLTSEL
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_QUC_VOLTSEL	0	rw1c	**QST and QUC voltage selection error. Nominal voltage of QST and QUC might be corrupt (3.3 V or 5 V).** 0_B No occurrence 1_B Fault occurred
BUCKIF_VOLTSEL	1	rw1c	**BUCK IF voltage selection error. Nominal voltage of BUCKIF might be corrupt (1.8 V or 3.3 V).** 0_B No occurrence 1_B Fault occurred
BUCK_CORE_VOLTSEL	2	rw1c	**BUCK CORE voltage selection error. Nominal voltage of BUCKCORE might be corrupt.** 0_B No occurrence 1_B Fault occurred
OT	3	rw1c	**Over temperature failure. (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
VMON	4	rw1c	**Voltage monitor failure (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
FSM_INITTIMER	5	rw1c	**Init timer failure due to the third INIT failure in row. The device moved to FAILSAFE state.** 0_B No fault 1_B Fault occurred
ERR0	6	rw1c	**ERR0 failure** 0_B No fault 1_B Fault occurred
QST	7	rw1c	**Standby LDO (QST) failure; Also set if BIST of QST retunred an error** 0_B No fault 1_B Fault occurred

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Field	Bits	Type	Description
INTSUP_IVCC	8	rw1c	**Internal supply IVCC failure; Also set if BIST of QIS retunred an error** 0_B No fault 1_B Fault occurred
PREREG_COSW	9	rw1c	**Reports major faults detected during SSW BIST and overcurrent on SSW** 0_B No fault 1_B Fault occurred
CFGE	10	rw1c	**DED for Cluster1 config registers** 0_B Write 0 - no action 1_B Event detected, write 1 to clear the flag
ABIST	11	rw1c	**ABIST operation interrupted by move to INIT or move to FAILSAFE fault** 0_B No fault 1_B Fault occurred

表 100　　SYSFAIL_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.49 应用 2 的系统故障状态寄存器 *R1)

SYSFAIL_STAT_APP2 Offset address: 02A$_H$

System failure status flags for application 2 *R1) Reset values see: Table 101

15	14	13	12	11	10	9	8
Res				ABIST	CFGE	PREREG_COSW	INTSUP_IVCC
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
QST	ERR0	FSM_INITTIMER	VMON	OT	BUCK_CORE_VOLTSEL	BUCKIF_VOLTSEL	QST_QUC_VOLTSEL
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_QUC_VOLTSEL	0	rw1c	**QST and QUC voltage selection error. Nominal voltage of QST and QUC might be corrupt (3.3 V or 5 V).** 0_B No occurrence 1_B Fault occurred
BUCKIF_VOLTSEL	1	rw1c	**BUCK IF voltage selection error. Nominal voltage of BUCKIF might be corrupt (1.8 V or 3.3 V).** 0_B No occurrence 1_B Fault occurred
BUCK_CORE_VOLTSEL	2	rw1c	**BUCK CORE voltage selection error. Nominal voltage of BUCKCORE might be corrupt.** 0_B No occurrence 1_B Fault occurred
OT	3	rw1c	**Over temperature failure (see chapter: Collection registers)** 0_B No occurrence 1_B Fault occurred
VMON	4	rw1c	**Voltage monitor failure (see chapter: Collection registers)** 0_B No occurrence 1_B Fault occurred
FSM_INITTIMER	5	rw1c	**Init timer failure due to the third INIT failure in row. The device moved to FAILSAFE state.** 0_B No occurrence 1_B Fault occurred
ERR0	6	rw1c	**ERR0 failure** 0_B No occurrence 1_B Fault occurred
QST	7	rw1c	**Standby LDO (QST) failure** 0_B No occurrence 1_B Fault occurred

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Field	Bits	Type	Description
INTSUP_IVCC	8	rw1c	**Internal supply IVCC failure** 0_B No occurrence 1_B Fault occurred
PREREG_COSW	9	rw1c	**Reports severe faults detected during SSW BIST** 0_B No occurrence 1_B Fault occurred
CFGE	10	rw1c	**DED for Cluster 2 config registers** 0_B Write 0 - no action 1_B Event detected, write 1 to clear the flag
ABIST	11	rw1c	**ABIST operation interrupted by move to INIT or move to FAILSAFE fault** 0_B No occurrence 1_B Fault occurred

表 101　　SYSFAIL_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.50 应用 1 的短路到地状态寄存器 *R1)

STG_STAT_APP1 Offset address: $02B_H$

Short to ground status register for application 1 *R1) Reset values see: Table 102

15	14	13	12	11	10	9	8
Res						VMON2	VMON1
r						rw1c	rw1c

7	6	5	4	3	2	1	0
BOOST	BUCKIF	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QUC	1	rw1c	**MCU LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QST	2	rw1c	**Standby LDO short to ground status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QCO	4	rw1c	**Communication LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QVR	5	rw1c	**Reference LDO short to groung status flag** 0_B No fault 1_B Fault occurred
BUCKIF	6	rw1c	**Buck interface short to ground status flag** 0_B No fault 1_B Fault occurred
BOOST	7	rw1c	**Boost short to ground status flag** 0_B No fault 1_B Event detected
VMON1	8	rw1c	**VMON1 short to ground status flag** 0_B No fault 1_B Fault occurred
VMON2	9	rw1c	**VMON2 short to ground status flag** 0_B No fault 1_B Fault occurred

表 102 STG_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.51 应用 2 的短路到地状态寄存器 *R1)

STG_STAT_APP2 Offset address: $02C_H$

Short to ground status register for application 2 *R1) Reset values see: Table 103

15	14	13	12	11	10	9	8
Res						VMON2	VMON1
r						rw1c	rw1c

7	6	5	4	3	2	1	0
BOOST	BUCKIF	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QUC	1	rw1c	**MCU LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QST	2	rw1c	**Standby LDO short to ground status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QCO	4	rw1c	**Communication LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QVR	5	rw1c	**Voltage reference short to groung status flag** 0_B No fault 1_B Fault occurred
BUCKIF	6	rw1c	**Buckint short to ground status flag** 0_B No fault 1_B Fault occurred
BOOST	7	rw1c	**Boost short to ground status flag** 0_B No fault 1_B Fault occurred
VMON1	8	rw1c	**VMON1 short to ground status flag** 0_B No fault 1_B Fault occurred
VMON2	9	rw1c	**VMON2 short to ground status flag** 0_B No fault 1_B Fault occurred

表 103 STG_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.52 应用 1 的过压状态寄存器 *R1)

OV_STAT_APP1

Offset address: $02D_H$

Overvoltage status register for application 1 *R1)

Reset values see: Table 104

15	14	13	12	11	10	9	8
Res			BUCKCORE_FB_OPEN	INTSUP_VDD2V5	INTSUP_IVCC	BUCKIF	PREREG
	r		rw1c	rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON2	VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over voltage status flag** 0_B No fault 1_B Fault occurred
QST	1	rw1c	**Standby LDO QST over voltage status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	2	rw1c	**BUCKCORE over voltage status flag** 0_B No fault 1_B Fault occurred
QCO	3	rw1c	**QCO over voltage status flag** 0_B No fault 1_B Fault occurred
QVR	4	rw1c	**QVR over voltage status flag** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over voltage status flag** 0_B No fault 1_B Fault occurred
VMON1	6	rw1c	**External volatage monitor channel 1 over voltage status flag** 0_B No fault 1_B Fault occurred
VMON2	7	rw1c	**External volatage monitor channel 2 over voltage status flag** 0_B No fault 1_B Fault occurred
PREREG	8	rw1c	**Pre-regulator over voltage status flag** 0_B No fault 1_B Fault occurred

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Field	Bits	Type	Description
BUCKIF	9	rw1c	**Buck interface over voltage status flag** 0_B No fault 1_B Fault occurred
INTSUP_IVCC	10	rw1c	**Internal supply IVCC LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
INTSUP_VDD2V5	11	rw1c	**Internal supply VDD 2V5 LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
BUCKCORE_FB_OPEN	12	rw1c	**BUCKCORE feedback open status flag** 0_B No fault 1_B Fault occurred

表 104　　OV_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.53 应用 2 的过压状态寄存器 *R1)

OV_STAT_APP2 Offset address: $02E_H$

Overvoltage status register for application 2 *R1) Reset values see: Table 105

15	14	13	12	11	10	9	8
Res			BUCKCORE_GND_OPEN	VDD2V5OV	INTSUP_IVCC	BUCKIF	PREREG
r			rw1c	rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON2	VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**MCU LDO over voltage status flag** 0_B No fault 1_B Fault occurred
QST	1	rw1c	**Standby LDO QST over voltage status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	2	rw1c	**BUCKCORE over voltage status flag** 0_B No fault 1_B Fault occurred
QCO	3	rw1c	**QCO over voltage status flag** 0_B No fault 1_B Fault occurred
QVR	4	rw1c	**QVR over voltage status flag** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over voltage status flag** 0_B No fault 1_B Fault occurred
VMON1	6	rw1c	**External volatage monitor channel 1 over voltage status flag** 0_B No fault 1_B Fault occurred
VMON2	7	rw1c	**External volatage monitor channel 2 over voltage status flag** 0_B No fault 1_B Fault occurred
PREREG	8	rw1c	**Pre-regulator over voltage status flag** 0_B No fault 1_B Fault occurred

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Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF over voltage status flag** 0_B No fault 1_B Fault occurred
INTSUP_IVCC	10	rw1c	**Internal supply IVCC LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
VDD2V5OV	11	rw1c	**Internal supply VDD 2V5 LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
BUCKCORE_GND_OPEN	12	rw1c	**Buckcore ground open status flag** 0_B No fault 1_B Fault occurred

表 105　　OV_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.54 应用 1 的内部电源状态寄存器 *R1)

INTSUP_STAT_APP1 Offset address: $02F_H$

Internal supply status register for application 1 *R1) Reset values see: Table 106

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res	PMU_RED	PMU_MAIN	BIAS_HI	BIAS_LOW	BG12_OV	BG12_UV	VBAT_OV
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VBAT_OV	0	rw1c	**Battery voltage supply (VS) over voltage** 0_B No fault 1_B Fault occurred
BG12_UV	1	rw1c	**Internal bandgap comparator detected UV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BG12_OV	2	rw1c	**Internal bandgap comparator detected OV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_LOW	3	rw1c	**Internal bias current too low (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_HI	4	rw1c	**Internal bias current too high (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_MAIN	5	rw1c	**PMU main pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_RED	6	rw1c	**PMU redundant pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred

表 106 INTSUP_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.55 应用 2 的内部电源状态寄存器 *R1)

INTSUP_STAT_APP2 Offset address: 030_H

Internal supply status register for application 2 *R1) Reset values see: Table 107

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res	PMU_RED	PMU_MAIN	BIAS_HI	BIAS_LOW	BG12_OV	BG12_UV	VBAT_OV
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VBAT_OV	0	rw1c	**Battery voltage supply (VS) over voltage** 0_B No fault 1_B Fault occurred
BG12_UV	1	rw1c	**Internal bandgap comparator detected UV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BG12_OV	2	rw1c	**Internal bandgap comparator detected OV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_LOW	3	rw1c	**Internal bias current too low (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_HI	4	rw1c	**Internal bias current too high (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_MAIN	5	rw1c	**PMU main pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_RED	6	rw1c	**PMU redundant pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred

表 107 INTSUP_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.56 应用 1 的过温状态寄存器 *R1)

OT_STAT_APP1 Offset address: 031_H

Over temperature status register for application 1 *R1) Reset values see: Table 108

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		BOOST	BUCKIF	BUCKCORE	SAFETY_AREA	QCO	QUC
r		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over temperature** 0_B No fault 1_B Fault occurred
QCO	1	rw1c	**QCO over temperature** 0_B No fault 1_B Fault occurred
SAFETY_AREA	2	rw1c	**Over temperature of Safety area temperature sensor** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore over temperature** 0_B No fault 1_B Fault occurred
BUCKIF	4	rw1c	**BUCKIF over temperature** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over temperature** 0_B No fault 1_B Fault occurred

表 108 OT_STAT_APP1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.57 应用 2 的过温状态寄存器 *R1)

OT_STAT_APP2 Offset address: 032_H

Over temperature status register for application 2 *R1) Reset values see: Table 109

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		BOOST	BUCKIF	BUCKCORE	SAFETY_AREA	QCO	QUC
r		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over temperature** 0_B No fault 1_B Fault occurred
QCO	1	rw1c	**QCO over temperature** 0_B No fault 1_B Fault occurred
SAFETY_AREA	2	rw1c	**Over temperature of Safety area temperature sensor** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**BUCKCORE over temperature** 0_B No fault 1_B Fault occurred
BUCKIF	4	rw1c	**BUCKIF over temperature** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over temperature** 0_B No fault 1_B Fault occurred

表 109 OT_STAT_APP2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.58 保护状态 *R1)

PROT_STAT Offset address: 033_H

Protection status *R1) Reset values see: Table 110

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res							**LOCK**
r							r

Field	Bits	Type	Description
LOCK	0	r	**Protected register password status** 0_B Registers unlocked 1_B Registers locked

表 110 PROT_STAT 的复位值

Reset	Reset value	Note
	0001_H	Reset class R1)

18.59 有限操作受保护写入配置 1 寄存器 - *R1)

该寄存器包含与有限操作模式相关的配置。如果有限操作模式启用（EN = 1），则所有设置将被应用。

REDOP_PW_CFG1
Reduced operation protected write configuration 1 register - *R1)

Offset address: 034_H
Reset values see: Table 111

15	14	13	12	11	10	9	8
Res	**SSO1TOSSO2_DEL**			**Res**		**INT2_DIS**	**INT1_DIS**
r	rw			r		rw	rw

7	6	5	4	3	2	1	0
SSO2_DEL			**SSO1_DEL**			**Res**	**EN**
rw			rw			r	rw

Field	Bits	Type	Description
EN	0	rw	**Enable reduced operation *R2)** 0_B Disabled 1_B Enabled
SSO1_DEL	4:2	rw	**Safe state output 1 delay (tSSO1_red)** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms
SSO2_DEL	7:5	rw	**Safe state output 2 delay (tSSO2_red)** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms
INT1_DIS	8	rw	**Disable generation of INT1 due to Cluster 2 entering REDUCED OPERATION** 0_B Allow generation of INT1 when Cluster 2 enters REDUCED OPERATION 1_B Disable generation of INT1 related to Cluster 2 entering REDUCED OPERATION

（表格续下页.....）

（续）

Field	Bits	Type	Description
INT2_DIS	9	rw	**Disable generation of INT2 due to Cluster 1 entering REDUCED OPERATION** 0_B Allow generation of INT2 when Cluster 1 enters REDUCED OPERATION 1_B Disable generation of INT2 related to Cluster 1 entering REDUCED OPERATION
SSO1TOSSO2_DEL	14:12	rw	**Safe state output 2 delay to Safe state output 1 (tSSO2) when REDUCED OPERATION is disabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms ... 111_B Do not use. Maps to 0 ms

表 111 REDOP_PW_CFG1 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.60 有限操作受保护写入配置 2 寄存器 - *R1)

该寄存器包含与有限操作模式相关的配置。如果有限操作模式启用（EN = 1），则所有设置将被应用。

REDOP_PW_CFG2 Offset address: 035_H

Reduced operation protected write configuration 2 register - *R1) Reset values see: Table 112

15	14	13	12	11	10	9	8
REDOP_RESOUT_APP2_DUR			REDOP_RESOUT_APP1_DUR			REDOP_RESOUT_APP_TB	Res
rw			rw			rw	r
7	6	5	4	3	2	1	0
Res							
r							

Field	Bits	Type	Description
REDOP_RESOUT_APP_TB	9	rw	**Reset timer time base for application reset pulse** 0_B 10 µs 1_B 100 µs
REDOP_RESOUT_APP1_DUR	12:10	rw	**Application reset pulse duration for INT1** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 ... 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1
REDOP_RESOUT_APP2_DUR	15:13	rw	**Application reset pulse duration for INT2** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 ... 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1

表 112 REDOP_PW_CFG2 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.61 器件受保护写入配置 3 寄存器 *R1)

DEV_PW_CFG3 Offset address: 036_H

Device protected write configuration 3 register *R1) Reset values see: Table 113

15	14	13	12	11	10	9	8
Res					VMON2_EN	VMON1_EN	BOOST_EN
r					rw	rw	rw

7	6	5	4	3	2	1	0
BUCKIF_EN	QUCEN	BUCKCORE_EN	QCO_EN	QVR_EN	FSM_STATEREQ		
rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
FSM_STATEREQ	2:0	rw	**Request for device state transition.** 000_B NONE 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B NONE 111_B NONE
QVR_EN	3	rw	**Enable request for reference voltage.** 0_B Disabled 1_B Enabled
QCO_EN	4	rw	**Enable request for communication LDO.** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	rw	**Enable request for BUCKCORE.** 0_B Disabled 1_B Enabled
QUCEN	6	rw	**Enable request for QUC.** 0_B Disabled 1_B Enabled
BUCKIF_EN	7	rw	**Enable request for Buck interface.** 0_B Disabled 1_B Enabled
BOOST_EN	8	rw	**Enable request for Boost.** 0_B Disabled 1_B Enabled

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Field	Bits	Type	Description
VMON1_EN	9	rw	**Enable request for external voltage monitoring channel 1.** 0_B Disabled 1_B Enabled
VMON2_EN	10	rw	**Enable request for external voltage monitoring channel 2.** 0_B Disabled 1_B Enabled

表 113　　DEV_PW_CFG3 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.62 看门狗 1 受保护写入配置 0 寄存器 *R2)

WD1_PW_CFG0
Watchdog 1 protected write configuration 0 register *R2)

Offset address: 037_H
Reset values see Table 114

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
WWD_ETHR				WWD_EN	FWD_EN	WWD_TSEL	CYC
rw				rw	rw	rw	rw

Field	Bits	Type	Description
CYC	0	rw	**Watchdog 1 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	rw	**Window watchdog (WWD1) trigger selection** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	rw	**Functional watchdog (FWD1) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	rw	**Window watchdog (WWD1) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	rw	**Window watchdog error counter threshold.**

表 114 WD1_PW_CFG0 的复位值

Reset	Reset value	Note
	$009B_H$	Reset class R2)

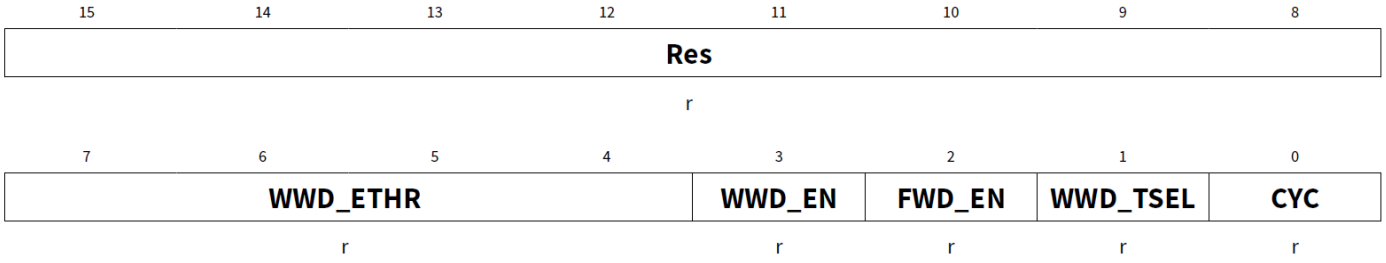
18.63 看门狗 1 反映状态配置 0 寄存器 - *R3_C1

WD1_RS_CFG0

Watchdog 1 reflected status configuration 0 register - *R3_C1

Offset address: 038_H

Reset values see: Table 115



Field	Bits	Type	Description
CYC	0	r	**Watchdog 1 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	r	**Window watchdog (WWD1) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	r	**Functional watchdog enable (FWD1)** 0_B Disabled 1_B Enabled
WWD_EN	3	r	**Window watchdog enable (WWD1)** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	r	**Window watchdog error threshold.**

表 115 WD1_RS_CFG0 的复位值

Reset	Reset value	Note
	$009B_H$	Reset class R3) C1

18.64 看门狗 1 受保护写入配置 1 寄存器 *R2)

WD1_PW_CFG1

看门狗 1 受保护的写入配置 1 寄存器 *R2)

Offset address: 039_H

Reset values see: Table 116

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLP_EN	FWD_ETHR			
r		rw	rw	rw			

Field	Bits	Type	Description
FWD_ETHR	3:0	rw	**Functional watchdog error threshold.**
SLP_EN	4	rw	**Watchdog1 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	rw	**Apply an additional divider of 10 to the cycle time** 0_B Disabled 1_B Enabled

表 116 WD1_PW_CFG1 的复位值

Reset	Reset value	Note
	0009_H	Reset class R2)

18.65 看门狗 1 反映状态配置 1 寄存器- *R3_C1

WD1_RS_CFG1

Watchdog 1 reflected status configuration 1 register- *R3_C1

Offset address: $03A_H$

Reset values see Table 117

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLPEN	FWD_ETHR			
r		r	r	r			

Field	Bits	Type	Description
FWD_ETHR	3:0	r	**Functional watchdog error threshold.**
SLPEN	4	r	**Watchdog1 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	r	**Additional divider of 10 to the cycle time is applied** 0_B Disabled 1_B Enabled

表 117 WD1_RS_CFG1 的复位值

Reset	Reset value	Note
	0009_H	Reset class R3) C1

18.66 功能看门狗 1 受保护写入心跳计时器周期配置寄存器 - *R2)

FWD1_PW_HBTP_CFG

Functional watchdog 1 protected write heart beat timer period configuration register- *R2)

Offset address: $03B_H$

Reset values see: Table 118

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			HBTP				
r			rw				

Field	Bits	Type	Description
HBTP	4:0	rw	**Functional watchdog 1 heartbeat timer period** 00_H (0 * 50 + 50) * time base ... $1F_H$ (31 * 50 + 50) * time base

表 118 FWD1_PW_HBTP_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R2)

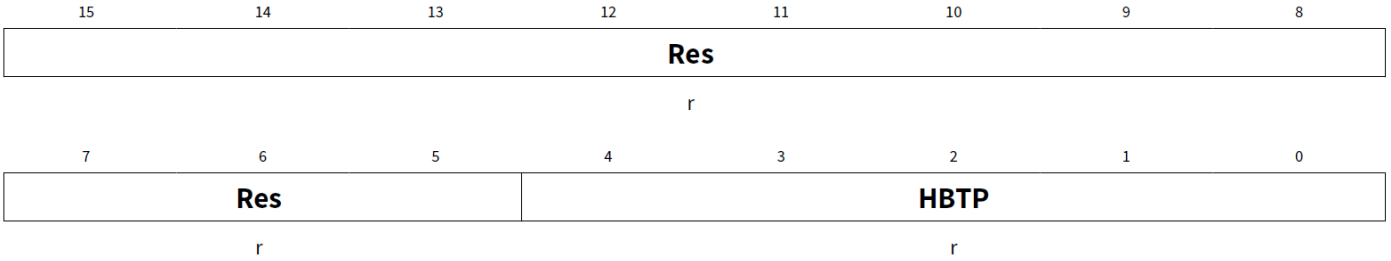
18.67 功能看门狗 1 反映状态心跳计时器周期配置寄存器 *R3_C1

FWD1_RS_HBTP_CFG

Offset address: $03C_H$

Functional watchdog 1 reflected status heart beat timer period configuration register*R3_C1

Reset values see: Table 119



Field	Bits	Type	Description
HBTP	4:0	r	**Functional watchdog 1 heartbeat timer period** 00_H (0 * 50 + 50) * time base ... $1F_H$ (31 * 50 + 50) * time base

表 119 FWD1_RS_HBTP_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R3) C1

18.68 窗口看门狗 1 受保护写入关闭窗口配置寄存器 - *R2)

WWD1_PW_CW_CFG

Window watchdog 1 protected write closed window configuration register - *R2)

Offset address: $03D_H$

Reset values see: Table 120

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
rw	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			rw				

Field	Bits	Type	Description
CW	4:0	rw	**Closed window time** 00_H (0 * 50 + 50) * time base ... $1F_H$ (31 * 50 + 50) * time base
CW_DIS	15	rw	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

表 120 WWD1_PW_CW_CFG 的复位值

Reset	Reset value	Note
	0006_H	Reset class R2)

18.69 窗口看门狗 1 反映状态关闭窗口配置寄存器 *R3_C1)

WWD1_RS_CW_CFG

Offset address: $03E_H$

Window watchdog 1 reflected status closed window configuration register*R3_C1)

Reset values see: Table 121

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			r				

Field	Bits	Type	Description
CW	4:0	r	**Closed window time** 00_H (0 * 50 + 50) * time base ... $1F_H$ (31 * 50 + 50) * time base
CW_DIS	15	r	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

表 121 WWD1_RS_CW_CFG 的复位值

Reset	Reset value	Note
	0006_H	Reset class R3) C1

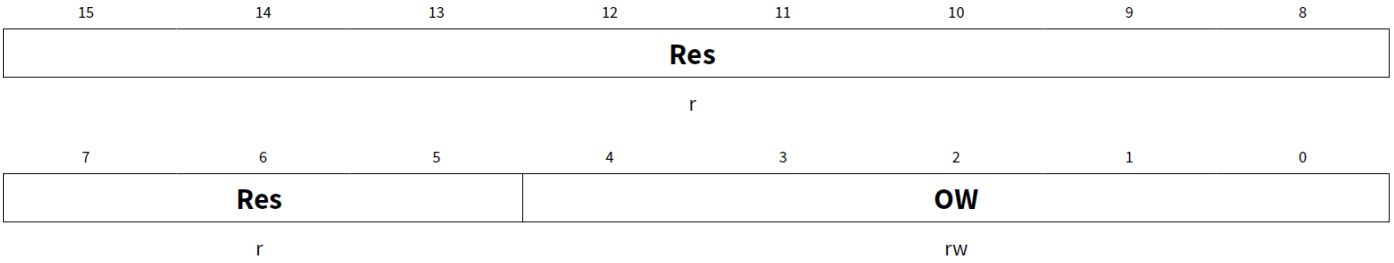
18.70 窗口看门狗 1 受保护写入打开窗口配置寄存器 - *R2)

WWD1_PW_OW_CFG

Offset address: 03F $_H$

Window watchdog 1 protected write open window configuration register - *R2)

Reset values see: Table 122



Field	Bits	Type	Description
OW	4:0	rw	**Open window time** 00_H (0 * 50 + 50) * time base ... $1F_H$ (31 * 50 + 50) * time base

表 122 WWD1_PW_OW_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R2)

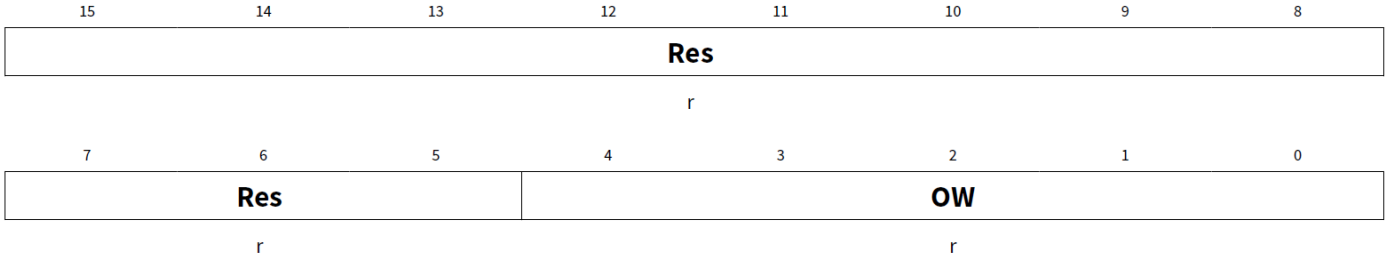
18.71 窗口看门狗 1 反映状态打开窗口配置寄存器 - *R3_C1)

WWD1_RS_OW_CFG

Offset address: 040_H

Window watchdog 1 reflected status open window configuration register - *R3_C1)

Reset values see: Table 123



Field	Bits	Type	Description
OW	4:0	r	**Open window time** 00_H (0 * 50 + 50) * time base . . . $1F_H$ (31 * 50 + 50) * time base

表 123 WWD1_RS_OW_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R3) C1

18.72 窗口看门狗 1 触发 - *R2)

WWD1_TRIG Offset address: 041_H

Window watchdog 1 trigger- *R2) Reset values see: Table 124

15	14	13	12	11	10	9	8
TRIG_STAT	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res							**TRIG**
r							rw

Field	Bits	Type	Description
TRIG	0	rw	**This bit triggers the window watchdog 1. For successful trigger, inverted value must be written.**
TRIG_STAT	15	r	**Last internal trigger value (TRIG bit) received via SPI.**

表 124 WWD1_TRIG 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.73 功能看门狗 1 响应寄存器 - *R2)

FWD1_RSP Offset address: 042_H

Functional watchdog 1 response register - *R2) Reset values see: Table 125

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
RSP							
rw							

Field	Bits	Type	Description
RSP	7:0	rw	**Response byte**

表 125 FWD1_RSP 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

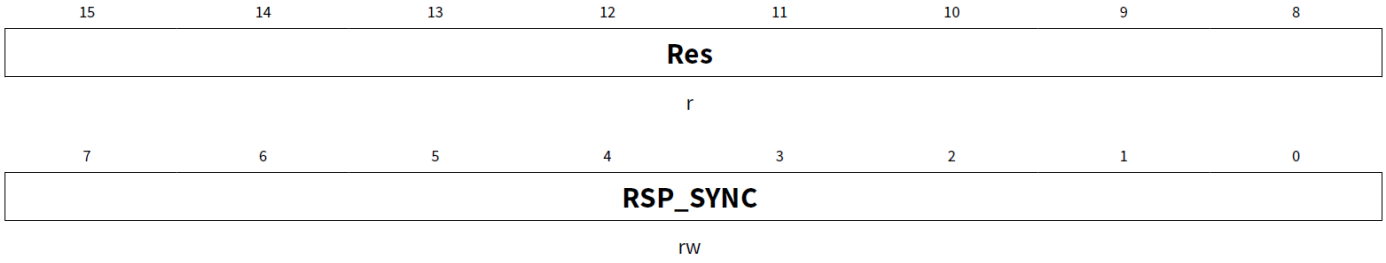
18.74 功能看门狗 1 响应寄存器与心跳计时器同步 - *R2)

FWD1_RSP_SYNC

Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2)

Offset address: 043_H

Reset values see: Table 126



Field	Bits	Type	Description
RSP_SYNC	7:0	rw	**Functional watchdog response byte and heartbeat timer synchronization**

表 126 FWD1_RSP_SYNC 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.75 功能看门狗 1 状态寄存器 - *R3_C1)

FWD1_STAT Offset address: 044_H

Functional watchdog 1 status register - *R3_C1) Reset values see: Table 127

15	14	13	12	11	10	9	8
Res					ECNT		
r					r		

7	6	5	4	3	2	1	0
ECNT	RSP_OK	RSPC		QUEST			
r	r	r		r			

Field	Bits	Type	Description
QUEST	3:0	r	**Functional watchdog question. Represents the value of the question, that is currently being asked.**
RSPC	5:4	r	**Functional watchdog response counter value. Represents the response which is currently expected (RESP3/2/1/0).**
RSP_OK	6	r	**Functional watchdog response status** 0_B Response message is wrong 1_B All received bytes in response message are correct
ECNT	10:7	r	**Functional watchdog error counter value**

表 127 FWD1_STAT 的复位值

Reset	Reset value	Note
	0030_H	Reset class R3) C1

18.76 窗口看门狗 1 错误计数器状态寄存器 - *R3_C1)

WWD1_ECNT_STAT

Window watchdog 1 error counter status register - *R3_C1)

Offset address: 045_H

Reset values see: Table 128

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res				ECNT			
r				r			

Field	Bits	Type	Description
ECNT	3:0	r	**Error counter value**

表 128 WWD1_ECNT_STAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R3) C1

18.77 看门狗 2 受保护写入配置 0 寄存器 - *R2)

WD2_PW_CFG0

Watchdog 2 protected write configuration 0 register - *R2)

Offset address: 046_H

Reset values see: Table 129

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
WWD_ETHR				WWD_EN	FWD_EN	WWD_TSEL	CYC
rw				rw	rw	rw	rw

Field	Bits	Type	Description
CYC	0	rw	**Watchdog 2 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	rw	**Window watchdog (WWD2) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	rw	**Functional watchdog (FWD2) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	rw	**Window watchdog (WWD2) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	rw	**Window watchdog error threshold.**

表 129 WD2_PW_CFG0 的复位值

Reset	Reset value	Note
	$009B_H$	Reset class R2)

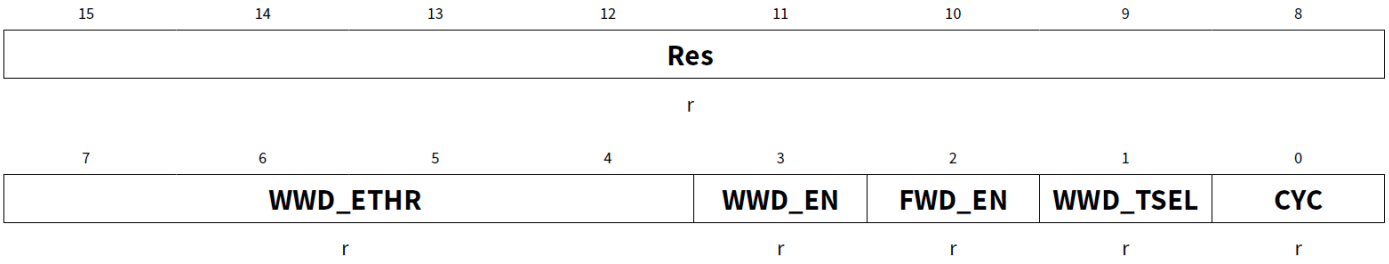
18.78 看门狗 2 反映状态配置 0 寄存器 - *R3_C2)

WD2_RS_CFG0

Watchdog 2 reflected status configuration 0 register-*R3_C2)

Offset address: 047_H

Reset values see: Table 130



Field	Bits	Type	Description
CYC	0	r	**Watchdog 2 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	r	**Window watchdog (WWD2) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI write to WWDSCMD register
FWD_EN	2	r	**Functional watchdog (FWD2) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	r	**Window watchdog (WWD2) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	r	**Window watchdog error threshold.**

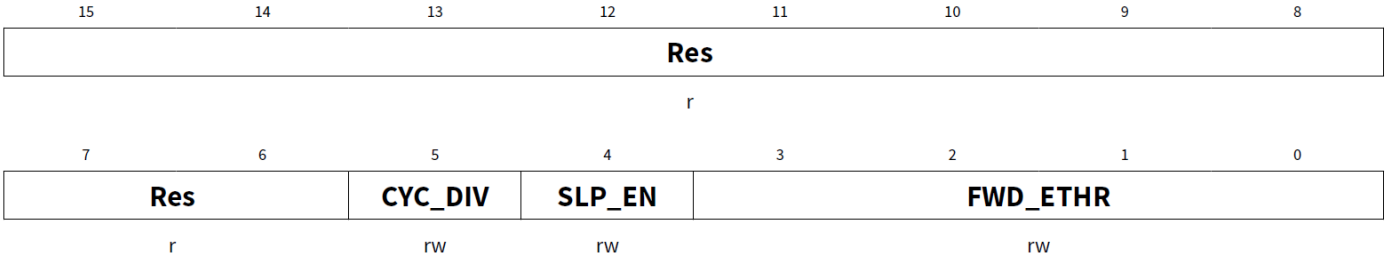
表 130 WD2_RS_CFG0 的复位值

Reset	Reset value	Note
	$009B_H$	Reset class R3) C2

18.79 看门狗 2 保护写入配置 1 - *R2)

WD2_PW_CFG1 Offset address: 048_H

Watchdog 2 protected write configuration 1 - *R2) Reset values see: Table 131



Field	Bits	Type	Description
FWD_ETHR	3:0	rw	**Functional watchdog error threshold.**
SLP_EN	4	rw	**Watchdog 2 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	rw	**Apply an additional divider of 10 to the cycle time** 0_B Disabled 1_B Enabled, additional divider

表 131 WD2_PW_CFG1 的复位值

Reset	Reset value	Note
	0009_H	Reset class R2)

18.80 看门狗 2 反映状态配置 1 寄存器 - *R3_C2)

WD2_RS_CFG1

Watchdog 2 reflected status configuration 1 register - *R3_C2)

Offset address: 049_H

Reset values see Table 132

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLP_EN	FWD_ETHR			
r		r	r	r			

Field	Bits	Type	Description
FWD_ETHR	3:0	r	**Functional watchdog error threshold.**
SLP_EN	4	r	**Watchdog 2 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	r	**Additional divider of 10 to the cycle time is applied** 0_B Disabled 1_B Enabled

表 132 WD2_RS_CFG1 的复位值

Reset	Reset value	Note
	0009_H	Reset class R3) C2

18.81 功能看门狗 2 受保护写入心跳计时器周期配置寄存器 - *R2)

FWD2_PW_HBTP_CFG

Functional watchdog 2 protected write heart beat timer period configuration register - *R2)

Offset address: $04A_H$

Reset values see: Table 133

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			HBTP				
r			rw				

Field	Bits	Type	Description
HBTP	4:0	rw	**Functional watchdog 2 heartbeat timer period** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base

表 133 FWD2_PW_HBTP_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R2)

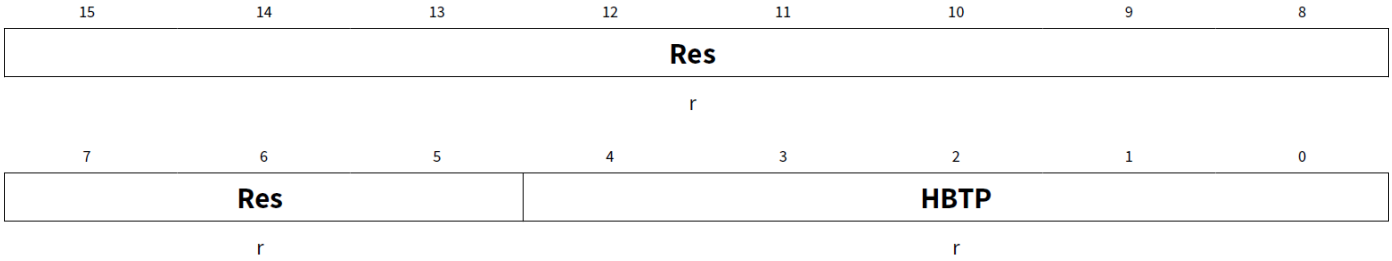
18.82 功能看门狗 2 反映状态心跳计时器周期配置寄存器 *R3_C2)

FWD2_RS_HBTP_CFG

Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2)

Offset address: $04B_H$

Reset values see: Table 134



Field	Bits	Type	Description
HBTP	4:0	r	**Functional watchdog 2 heartbeat timer period** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base

表 134 FWD2_RS_HBTP_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R3) C2

18.83 窗口看门狗 2 受保护写入关闭窗口配置寄存器 - *R2)

WWD2_PW_CW_CFG

Window watchdog 2 protected write closed window configuration register - *R2)

Offset address: $04C_H$

Reset values see: Table 135

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
rw	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			rw				

Field	Bits	Type	Description
CW	4:0	rw	**Closed window time** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base
CW_DIS	15	rw	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

表 135 WWD2_PW_CW_CFG 的复位值

Reset	Reset value	Note
	0006_H	Reset class R2)

18.84 窗口看门狗 2 反映状态关闭窗口配置寄存器 *R3_C2)

WWD2_RS_CW_CFG

Offset address: $04D_H$

Window watchdog 2 reflected status closed window configuration register *R3_C2)

Reset values see: Table 136

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			r				

Field	Bits	Type	Description
CW	4:0	r	**Closed window time** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base
CW_DIS	15	r	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

表 136 WWD2_RS_CW_CFG 的复位值

Reset	Reset value	Note
	0006_H	Reset class R3) C2

18.85 窗口看门狗 2 受保护写入打开窗口配置寄存器 - *R2)

WWD2_PW_OW_CFG

Window watchdog 2 protected write open window configuration register - *R2)

Offset address: $04E_H$

Reset values see: Table 137

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			OW				
r			rw				

Field	Bits	Type	Description
OW	4:0	rw	**Open window time** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base

表 137 WWD2_PW_OW_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R2)

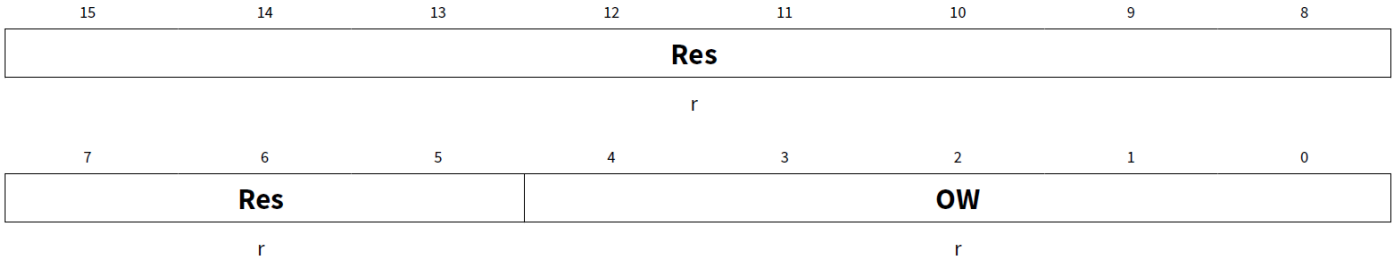
18.86 窗口看门狗 2 反映状态打开窗口配置寄存器 *R3_C2)

WWD2_RS_OW_CFG

Window watchdog 2 reflected status open window configuration register *R3_C2)

Offset address: $04F_H$

Reset values see: Table 138



Field	Bits	Type	Description
OW	4:0	r	**Open window time** 00_H (0 * 50 + 50) wd time base ... $1F_H$ (31 * 50 + 50) wd time base

表 138 WWD2_RS_OW_CFG 的复位值

Reset	Reset value	Note
	$000B_H$	Reset class R3) C2

18.87 窗口看门狗 2 服务 - *R2)

WWD2_TRIG Offset address: 050_H

Window watchdog 2 service - *R2) Reset values see: Table 139

15	14	13	12	11	10	9	8
TRIG_STAT	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res							**TRIG**
r							rw

Field	Bits	Type	Description
TRIG	0	rw	**This bit triggers the window watchdog 2. For successful trigger, inverted value must be written.**
TRIG_STAT	15	r	**Last internal service value (TRIG bit) received via SPI.**

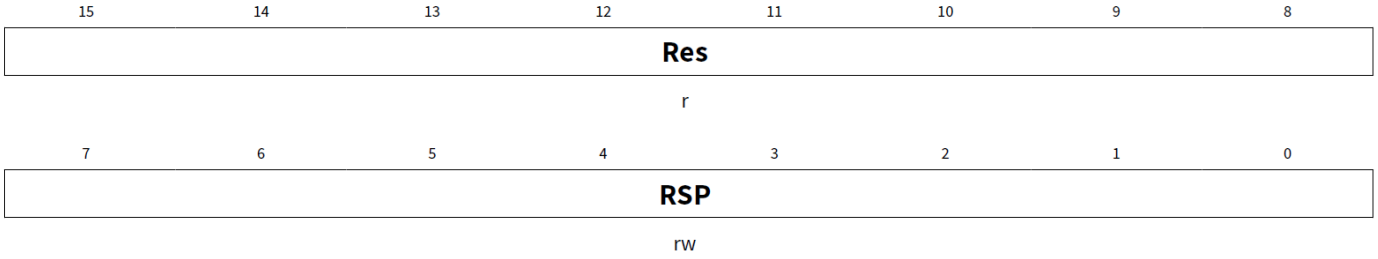
表 139 WWD2_TRIG 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.88 功能看门狗 2 响应寄存器 - *R2)

FWD2_RSP Offset address: 051_H

Functional watchdog 2 response register - *R2) Reset values see: Table 140



Field	Bits	Type	Description
RSP	7:0	rw	**Response byte**

表 140 FWD2_RSP 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

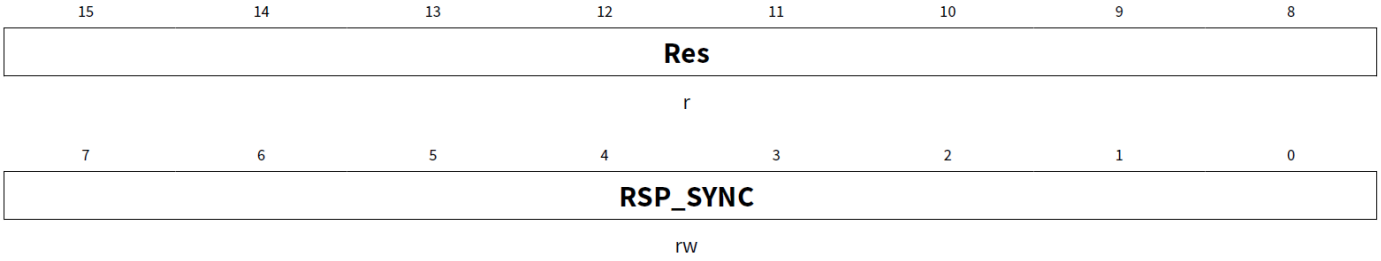
18.89 带同步的功能看门狗 2 响应寄存器 - *R2)

FWD2_RSP_SYNC

Functional watchdog 2 response register with synchronization - *R2)

Offset address: 052_H

Reset values see: Table 141



Field	Bits	Type	Description
RSP_SYNC	7:0	rw	**Functional watchdog response byte and heartbeat timer synchronization**

表 141 FWD2_RSP_SYNC 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.90 功能看门狗 2 状态寄存器 - *R3_C2)

FWD2_STAT Offset address: 053_H

Functional watchdog 2 status register - *R3_C2) Reset values see: Table 142

15	14	13	12	11	10	9	8
Res					ECNT		
r					r		

7	6	5	4	3	2	1	0
ECNT	RSP_OK	RSPC		QUEST			
r	r	r		r			

Field	Bits	Type	Description
QUEST	3:0	r	**Functional watchdog question**
RSPC	5:4	r	**Functional watchdog response counter value**
RSP_OK	6	r	**Functional watchdog response status** 0_B Response message is wrong 1_B All received bytes in response message are correct
ECNT	10:7	r	**Functional watchdog error counter value**

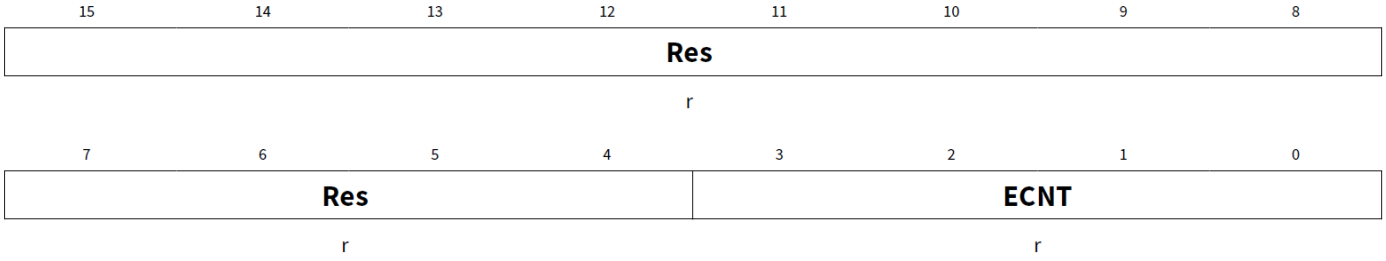
表 142 FB_STAT 的复位值

Reset	Reset value	Note
	0030_H	Reset class R3) C2

18.91 窗口看门狗 2 状态寄存器 - *R3_C2)

WWD2_ECNT_STAT Offset address: 054_H

Window watchdog 2 status register - *R3_C2) Reset values see: Table 143



Field	Bits	Type	Description
ECNT	3:0	r	**Error counter value**

表 143 WWD2_ECNT_STAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R3) C2

18.92 安全开关诊断，*R1)

SSW_DIAG

Safety switch diagnostics, *R1)

Offset address: 055_H

Reset values see: Table 144

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			EBIST4	EBIST3	EBIST2	EBIST1	EBIST0
r			r	r	r	r	r

Field	Bits	Type	Description
EBIST0	0	r	**Indicates if SSW is intact** 0_B No fault 1_B SSW check not passed
EBIST1	1	r	**Indicates if high side switch at PREREG is intact** 0_B No fault 1_B HS switch of PREREG defect
EBIST2	2	r	**Indicates if SSW gate can be discharged** 0_B No fault 1_B SSW gate could not be discharged
EBIST3	3	r	**Indicates if low side switch of PREREG is intact** 0_B No fault 1_B LS switch of PREREG defect
EBIST4	4	r	**Sanity check on SSW charge pump chain** 0_B No fault 1_B Sanity check unsuccessful

表 144 SSW_DIAG 的复位值

Reset	Reset value	Note
	0000_H	Reset class R1)

18.93 BUCK CORE 受保护写入电压选择寄存器 *R1)

BUCK_CORE_PW_VSEL
BUCK CORE protected write voltage selection register *R1)

Offset address: 056_H
Reset values see: Table 145

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		VSEL					
r		rw					

Field	Bits	Type	Description
VSEL	5:0	rw	**Voltage selection (0.7 V to 1.1 V; 12.5 mV steps)** 00_H BUCKCORE output voltage: 0.7 V + 0*12.5 mV ... 20_H BUCKCORE output voltage: 0.7 V + 32*12.5 mV **others,** reserved

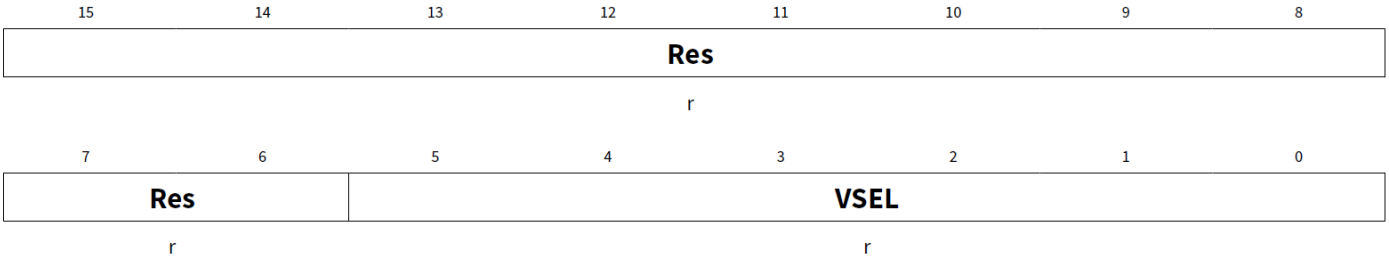
表 145 BUCK_CORE_PW_VSEL 的复位值

Reset	Reset value	Note
	0000_H	

18.94 BUCK CORE 反映状态电压选择寄存器 *R2)

BUCK_CORE_RS_VSEL
BUCK CORE reflected status voltage selection register *R2)

Offset address: 057_H
Reset values see: Table 146



Field	Bits	Type	Description
VSEL	5:0	r	**Voltage selection status register (0.7 V to 1.1 V; 12.5 mV steps)** 00_H BUCKCORE output voltage: 0.7 V + 0*12.5 mV ... 20_H BUCKCORE output voltage: 0.7 V + 32*12.5 mV **others,** reserved

表 146 BUCK_CORE_RS_VSEL 的复位值

Reset	Reset value	Note
	$001A_H$	Reset class R2)

18.95 BUCK CORE 电压选择状态，*R2)

VCORESTAT Offset address: 058_H

Buck core voltage selection stat, *R2) Reset values see: Table 147

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		VOUT					
r		r					

Field	Bits	Type	Description
VOUT	5:0	r	**Current voltage out for buckcore, *R2)** 00_H BUCKCORE output voltage set to 0.7 V + 0*12.5 mV ... 20_H BUCKCORE output voltage set to 0.7 V + 32*12.5 mV 21_H BUCKCORE output voltage set to 1.15 V; Not allowed to be used for static voltage scaling! **others,** reserved

表 147 VCORESTAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.96 BUCK CORE 电压选择监测状态，*R2)

VCOREMONSTAT Offset address: 059_H

Buck core voltage selection monitors stat, *R2) Reset values see: Table 148

15	14	13	12	11	10	9	8
Res		**OVTH**					
r		r					

7	6	5	4	3	2	1	0
Res		**UVTH**					
r		r					

Field	Bits	Type	Description
UVTH	5:0	r	**Under voltage thresholds for buckcore voltage selection, *R2)** 00_H BUCKCORE undervoltage threshold for VOUT = 0.7 V + 0*12.5 mV ... 20_H BUCKCORE undervoltage threshold for VOUT = 0.7 V + 32*12.5 mV 21_H BUCKCORE undervoltage threshold for VOUT = 1.15 V **others,** reserved
OVTH	13:8	r	**Over voltage thresholds for buckcore voltage selection, *R2)** 00_H BUCKCORE overvoltage threshold for VOUT = 0.7 V + 0*12.5 mV ... 20_H BUCKCORE overvoltage threshold for VOUT = 0.7 V + 32*12.5 mV 21_H BUCKCORE overvoltage threshold for VOUT = 1.15 V **others,** reserved

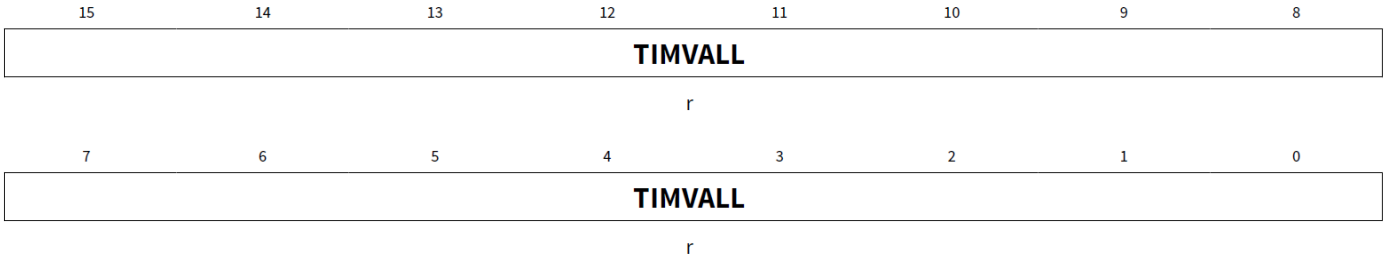
表 148 VCOREMONSTAT 的复位值

Reset	Reset value	Note
	0000_H	Reset class R2)

18.97 从 STANDBY 或 SLEEP 退出后唤醒计时器值（低 16 位）

WUT_STAT0 Offset address: $05A_H$

Wake Up Timer value after exiting from STANDBY or SLEEP [lower 16 bits) value: 0000_H



Field	Bits	Type	Description
TIMVALL	15:0	r	**Lower 16 bit of wake-up timer value: LSB bit 0; MSB bit15**

18.98 从 STANDBY 或 SLEEP 退出后唤醒计时器值（高 8 位）

WUT_STAT1 Offset address: $05B_H$

Wake Up Timer value after exiting from STANDBY or SLEEP [upper 8 bits) value: 0000_H

15	14	13	12	11	10	9	8
CYC	**PRESC**	**Res**					
r	r	r					

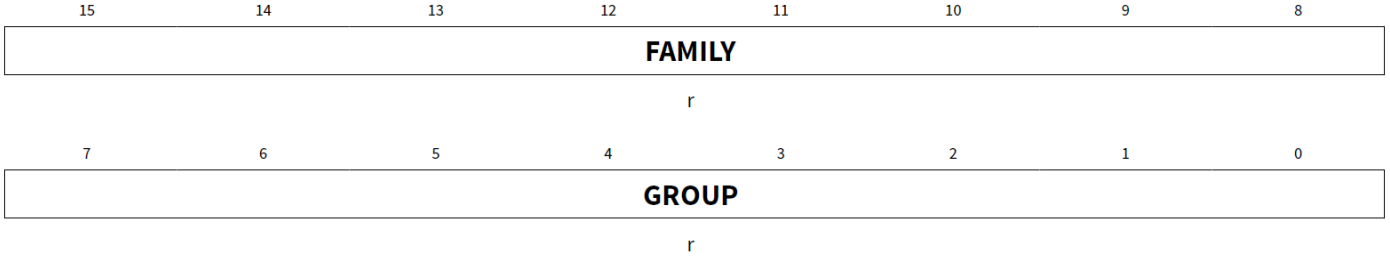
7	6	5	4	3	2	1	0
TIMVALH							
r							

Field	Bits	Type	Description
TIMVALH	7:0	r	**Higher 8 bits of wake-up timer value: LSB bit0; MSB bit 7**
PRESC	14	r	0_B Disabled 1_B Enabled
CYC	15	r	0_B 10 µs 1_B 10 ms

18.99 芯片产品标识符

CHPID Offset address: $1F0_H$

Chip product identifier value: 0201_H



Field	Bits	Type	Description
GROUP	7:0	r	**Chip product group** 01_H GP_PMIC
FAMILY	15:8	r	**Chip family** 02_H CLF4D985

18.100 芯片产品版本和修订

CHREV

Chip product version and revision

Offset address: $1F1_H$

value: 0003_H

15	14	13	12	11	10	9	8
VERSION							
r							

7	6	5	4	3	2	1	0
REVISION							
r							

Field	Bits	Type	Description
REVISION	7:0	r	**Chip revision** 03_H A31 (CLF4D985QxV0xR1)
VERSION	15:8	r	**Chip product version** 01_H CLF4D985QxV01 02_H CLF4D985QxV02 03_H CLF4D985QxV03

18.101 制造商 ID

MANID Offset address: $1F2_H$

Manufacturer ID value: $00C1_H$

15	14	13	12	11	10	9	8
RESERVED							
r							

7	6	5	4	3	2	1	0
MANUFACTURER							
r							

Field	Bits	Type	Description
MANUFACTURER	7:0	r	**MANUFACTURER** $C1_H$ Infineon technologies AG
RESERVED	15:8	r	**RESERVED**

19 应用信息

19.1 应用图

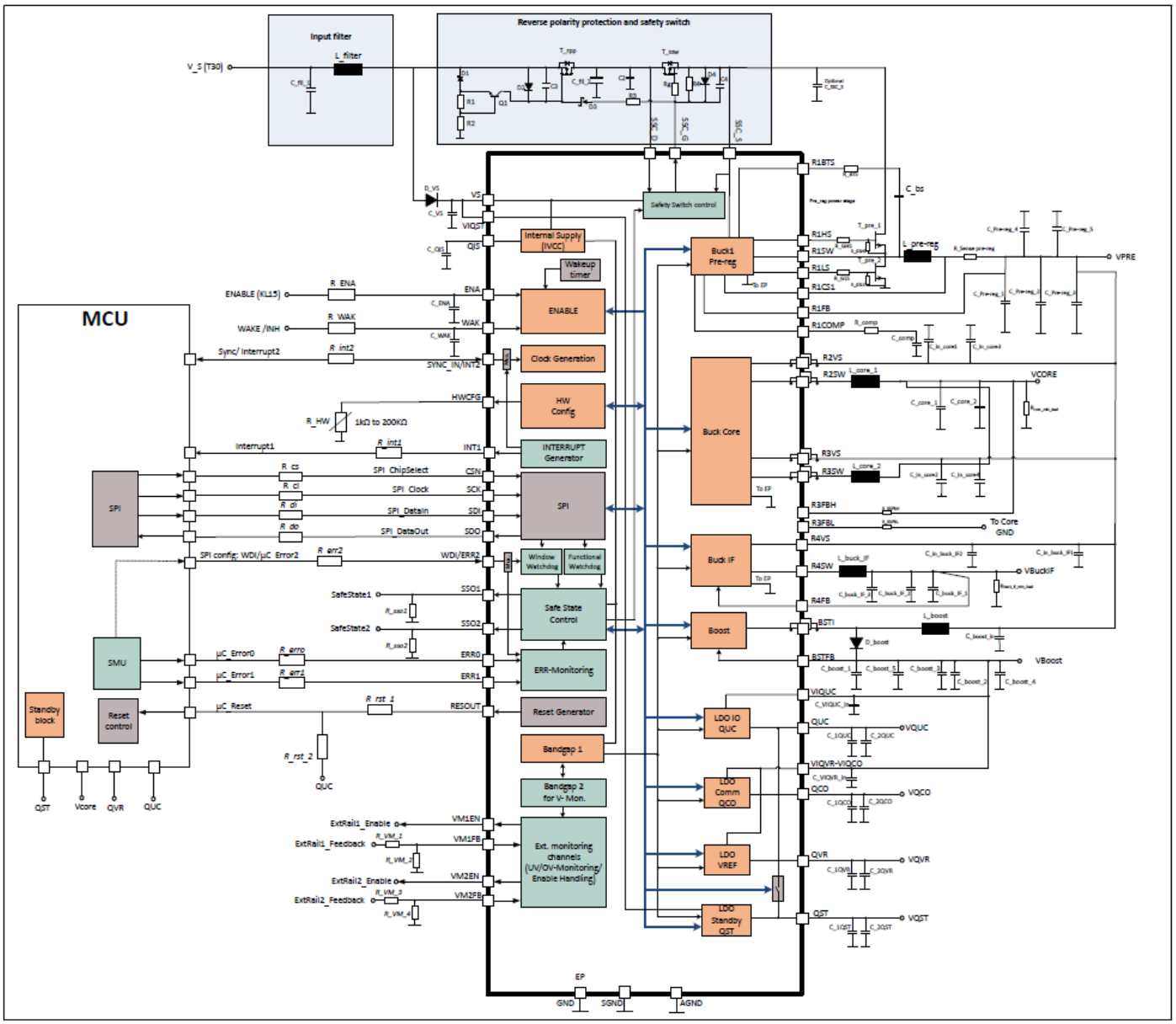


图 96 应用图

19.2 BOM 建议

表 149 BOM 建议

Block	Symbol	Value	Description	Note
Input Filter	C_fil_1	10 µF	Surface mount ceramic capacitor	Max voltage depending on application (50 V for 12 V application and 100 V for 24 V application)
	C_fil_2	220 µF	Electrolytic capacitor	Max voltage depending on application (50 V for 12 V application and 100 V for 24 V application)
	L_filter	4.7 µH	Shielded filter Power Inductor	Inductor selection depending on EMC requirement
QIS & Input voltage	C_QIS	1 µF	Surface mount ceramic capacitor	–
	C_VS	4.7 µF	Surface mount ceramic capacitors	–
	D_VS	d_schottky	reverse polarity protection diode for low current path	–
Reverse battery protection (RPP) and safety switch (SSC)	C2	10 µF	Surface mount capacitor	Max voltage ceramic depending on application (50 V for 12 V application and 100 V for 24 V application)
	C3	1 nF	Surface mount ceramic capacitor	–
	C4	1 nF	Surface mount ceramic capacitor	–
	T_rpp	RPP + SSC MOSFET	N-Channel MOSFETs (logic level)	IPG20N06S2L-35A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	T_ssw			
	D1	VBD = 60 V	Schottky diode to prevent current flowing via R1 and R2 in normal supply condition	–

（表格续下页……）

表 149 （续）BOM 建议

Block	Symbol	Value	Description	Note
	D2	VZ = 10 V	Zener diode to protect gate of RPP MOSFET	–
	D3	VBD = 60 V	Schottky diode to prevent current bypassing RPP and SSW via R4 and R5 in normal supply condition	RB558VYM150FH
	D4	VZ = 6.2 V	Zener diode to protect the PMIC VGS driver	–
	Q1	npn	Low leakage npn transistor, to discharge the RPP MOSFET when the battery voltage is below ground	Recommended low leakage at VCB = 40 V at hot
	R1	47 kΩ	Standard thick film chip resistor	–
	R2	47 kΩ	Standard thick film chip resistor	–
	R3	300 kΩ	Standard thick film chip resistor	–
	R4	300 kΩ	Standard thick film chip resistor	–
	Rg	10 Ω	Gate resistor for the control of the external safety switch	–
	C_SSC_S	1 µF (Max)	Surface mount ceramic capacitors	optional: To improve EMC performance. However dimension the capacitance to meet safety goals as it might have an effect on system's response to fault conditions.
PREREG	C_Pre_reg_1 C_Pre_reg_2	3 × 22 µF	Surface mount ceramic capacitors	Nominal values of capacitances are recommended taking into account

（表格续下页……）

表 149 （续）BOM 建议

Block	Symbol	Value	Description	Note
	C_Pre_reg_3			all derating factors (voltage, temperature and aging)
	C_Pre_reg_4	1 µF	Surface mount ceramic capacitor	–
	C_Pre_reg_5	100 nF	Surface mount ceramic capacitor	–
	L_pre_reg	6.8 µH	Shielded power inductor	Select inductor according to the over current limitation
	T_pre_1	External MOSFETs	N-Channel MOSFETs (logic level)	IPG20N06S4L-26A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	T_pre_2			IPG20N06S4L-26A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	R_COMP	12 kΩ	Standard thick film chip resistor	For 10 A current capability
		25 kΩ	Standard thick film chip resistor	For 5 A current capability
	C_COMP	1.5 nF	Surface mount ceramic capacitor	For 5 A current capability
		2.7 nF	Surface mount ceramic capacitor	For 10 A current capability
	R_Sense_pre-reg	10 mΩ	Standard thick film chip resistor, tol. ±1%	For 10 A current capability
		20 mΩ	Standard thick film chip resistor, tol. ±1%	For 5 A current capability
	C_bs	100 nF	Surface mount ceramic capacitor	–
	R_BTS	–	Boot strap line resistance for limiting inrush currents	If EMC does not require it, set it to 0 Ω

（表格续下页……）

表 149 （续）BOM 建议

Block	Symbol	Value	Description	Note
	R_GHS	–	Gate resistor for limiting gate currents	If EMC does not require it, set it to 0 Ω
	R_GSHS	–	–	optional: Only if use case assumption requires it for safety reasons
	R_GSLS	–	–	optional Only if use case assumption requires it for safety reasons
	R_GLS	–	Gate resistor for limiting gate currents	If EMC does not require it, set it to 0 Ω
BOOST	C_boost_in	100 nF	Surface mount ceramic capacitor	–
	C_boost_1	100 nF	Surface mount ceramic capacitor	–
	C_boost_2	1 µF	Surface mount ceramic capacitor	–
	C_boost_3	10 µF	Surface mount ceramic capacitor	–
	C_boost_4	100 nF	Surface mount ceramic capacitor	–
	C_boost_5	47 nF	Surface mount ceramic capacitor	–
	D_boost	d_schottky	Schottky Rectifier	MSS2P3 or similar
	L_boost	3.3 µH	Shielded Power Inductor	Select inductance according to the over current limitation
BUCK CORE	C_in_core1	2 × 4.7 µF	Surface mount ceramic capacitors	–
	C_in_core2			
	C_in_core3	2 × 100 nF	Surface mount ceramic capacitors	–
	C_in_core4			
	C_core_1	2 × 47 µF	Surface mount ceramic capacitors	consider to use additional capacitance in case it is necessary.
	C_core_2			

（表格续下页……）

表 149 （续）BOM 建议

Block	Symbol	Value	Description	Note
	L_core_1	1 µH	Shielded power inductor	Select inductor according to the over current limitation
	L_core_2	1 µH	Shielded power inductor	Select inductor according to the over current limitation
	R_core_min_load	–	–	Pick accordingly to fulfill Minimum output current - BUCK CORE
	R_R3FBH	10 - 100 Ω	–	optional: Only required if use case assumption requires it for safety reasons
	R_R3FBL	10 - 100 Ω	–	optional: Only required if use case assumption requires it for safety reasons
BUCK IF	C_in_buck_IF1	1 µF	Surface mount ceramic capacitors	–
	C_in_buck_IF2	100 nF	Surface mount ceramic capacitors	–
	C_buck_IF_1	47 µF	Surface mount ceramic capacitors	–
	C_buck_IF_2	1 µF	Surface mount ceramic capacitor	–
	C_buck_IF_3	100 nF	Surface mount ceramic capacitor	–
	L_buck_IF	2.2 µH	Shielded power inductor	Select inductor according to the over current limitation
	R_buck_if_min_load	–	–	Pick accordingly to fulfill Minimum output current - BUCK IF
LDO_Capacitors	C_1QCO	4.7 µF	Surface mount ceramic capacitor	–

（表格续下页……）

表 149 （续）BOM 建议

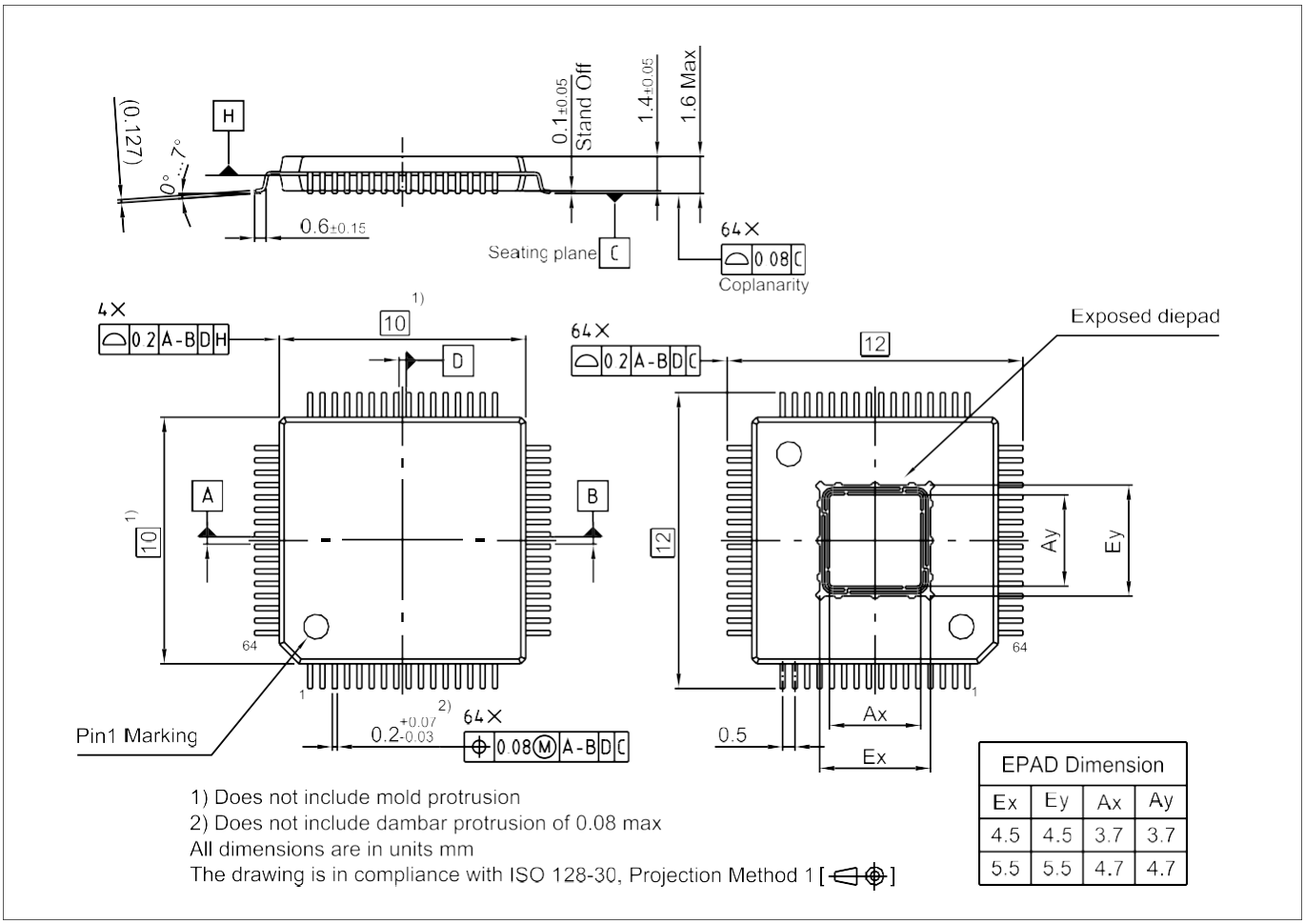
Block	Symbol	Value	Description	Note
	C_2QCO	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QCO.
	C_1QST	4.7 µF	Surface mount ceramic capacitor	–
	C_2QST	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QST.
	C_1QUC	4.7 µF	Surface mount ceramic capacitor	–
	C_2QUC	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QUC.
	C_1QVR	4.7 µF	Surface mount ceramic capacitor	–
	C_2QVR	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QVR.
	C_IQUC_in	100 nF	Surface mount ceramic capacitor	optional
	C_IQVR_in	100 nF	Surface mount ceramic capacitor	optional
ENA/WAK	C_ENA	10 nF	Surface mount ceramic capacitor	optional
	C_WAK	10 nF	Surface mount ceramic capacitor	optional
	R_ENA	10 kΩ	Standard thick film chip resistor	optional
	R_WAK	10 kΩ	Standard thick film chip resistor	optional

表 150　　开关模式电源输出电容的 BOM 偏差

SMPS	Effective capacitance	Deviation
PREREG	$C_{PR}[typ]$	-40%
BUCKCORE	$C_{buck\_core\_1/2}[typ]$	-30%
BUCKIF	$C_{BUCK\_IF}[typ]$	-40%
BOOST	$C_{bst}[typ]$	-40%

注释： *当偏离上述表中所示的开关模式调节器的输出电容值时，数据手册中指定的动态性能可能会受到影响，并且需要在应用上下文中对其行为进行专门评估。*

20 封装信息



EPAD Dimension			
Ex	Ey	Ax	Ay
4.5	4.5	3.7	3.7
5.5	5.5	4.7	4.7

图 97 PG-LQFP-64[1)]

绿色产品（符合 RoHS 标准）

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封装信息

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1 本产品裸露的散热焊盘尺寸 [mm]： E_x: 5.5, E_y: 5.5, A_x: 4.7, A_y: 4.7

修订记录

Revision	Date	Changes
1.00	2026-01-09	Datasheet created

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