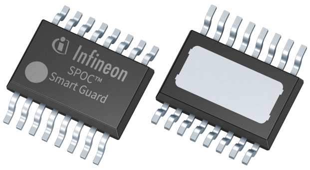
BTS81000-SSGI-6ET

Datasheet

SPOC™ Smart Guard



AEC Qualified

RoHS

ISO 26262 compliant

Features

- High-side switch with diagnosis and embedded protection
- 8-bit SPI, daisy chain capable
- Low operating current (idle) for active supply during parking
- ISO 26262 Safety Element out of Context for requirements up to ASIL-D
- Digital load current sense
- Open load detection
- Short circuit to ground and short circuit to battery protection
- Temperature warning indication
- Overvoltage protection
- Undervoltage protection
- Selectable overcurrent limitation thresholds
- Temperature protection with unlimited restarts

Potential applications

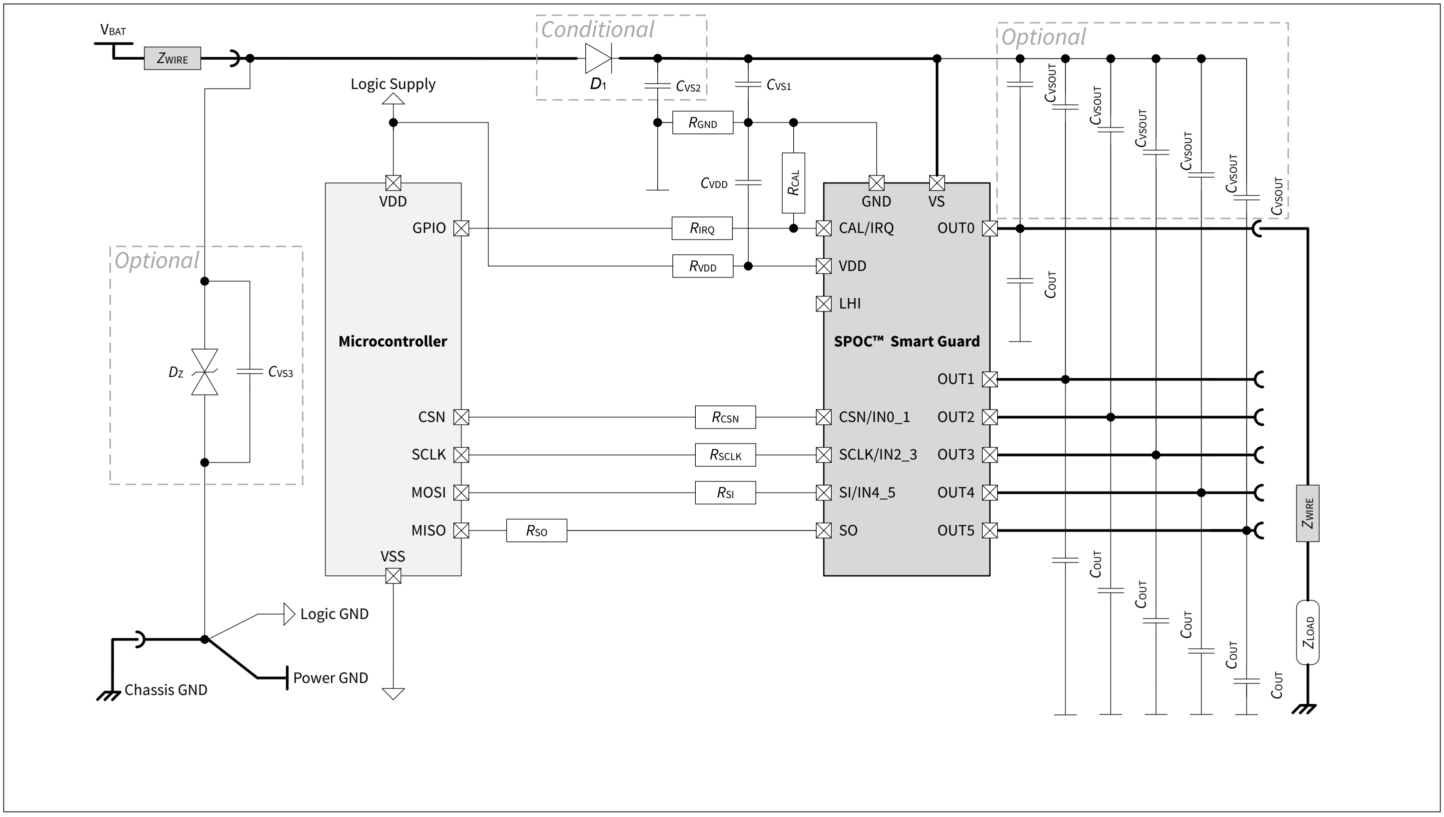
- Replaces electromechanical relays, fuses and discrete circuits
- Power supply switch for sensors and ECUs
- Suitable for driving resistive, inductive and capacitive loads

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The SPOC™ Smart Guard is a multichannel smart high-side power switch, providing protection functions and diagnosis.



Product type	Package	Marking
BTS81000-SSGI-6ET	PG-TFDSO-16	810

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1 Product description

Table 1 **Product summary**

Parameter	**Symbol**	**Values**
Minimum operating voltage	$V_{S(OP)}$	4.1 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	3.5 V
Maximum power supply voltage	V_S	28 V
Digital supply voltage	V_{DD}	3.3 V or 5 V
Minimum overvoltage protection	$V_{DS(CLAMP)}$	37 V
Maximum source to ground clamping voltage	$V_{OUT(CLAMP)}$	-18 V
Typical ON-state resistance (T_J = 25°C)	$R_{DS(ON)\_25}$	133 mΩ
Maximum ON-state resistance (T_J = 150°C)	$R_{DS(ON)\_150}$	230 mΩ
Nominal load current (T_A = 85°C)	$I_{L(NOM)\_85}$	1 A
Typical highest overcurrent limitation threshold	$I_{L(HOCT)}$	1.85 A
Typical lowest overcurrent limitation threshold	$I_{L(LOCT)}$	0.136 A
Maximum operating current	$I_{GND(ACTIVE)}$	3.2 mA
Maximum operating current without diagnosis	$I_{GND(ACTIVE\_WOD)85}$	128 µA

2 Block diagram and terms

2.1 Block diagram

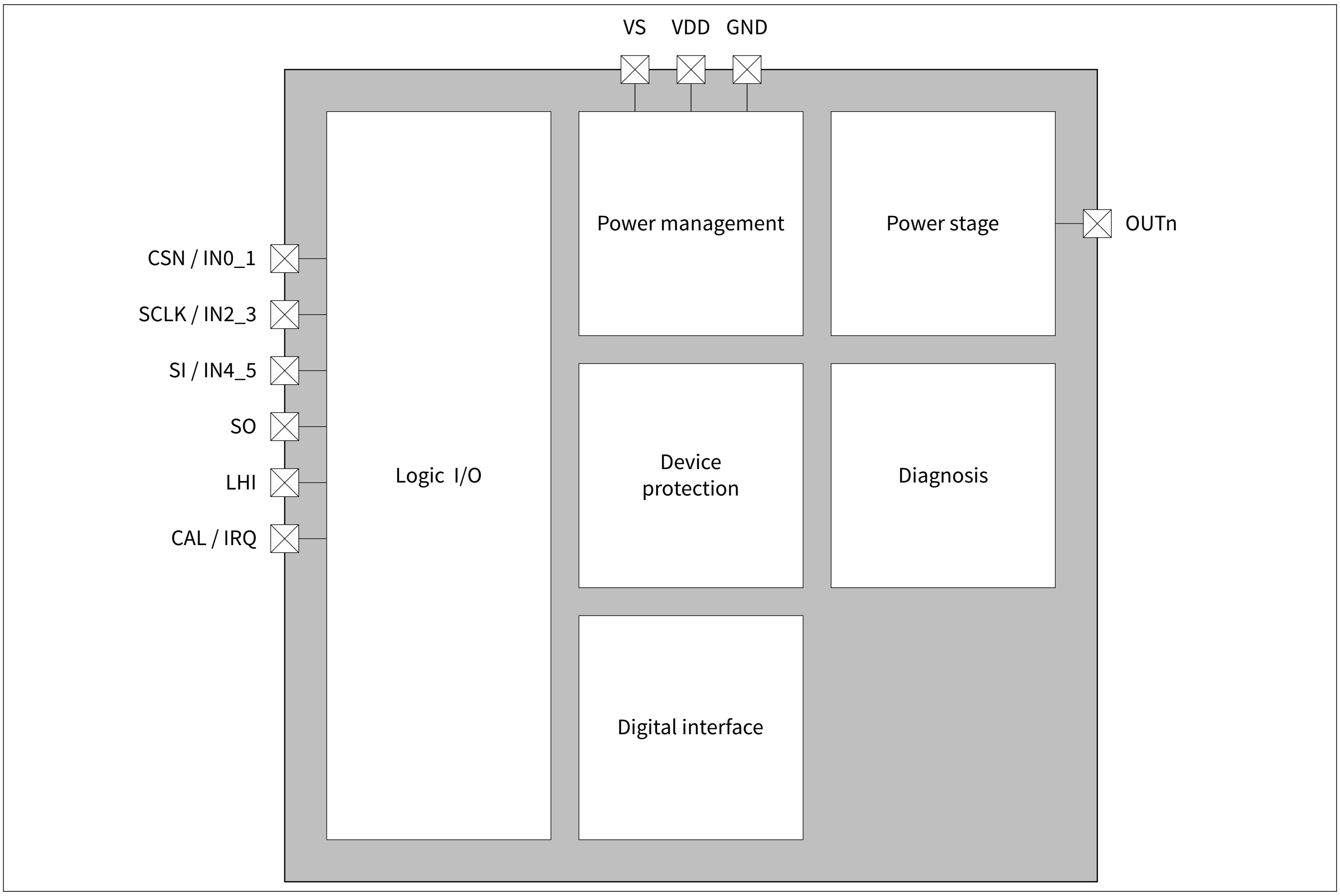


Figure 1 Block diagram

2.2 Terms

The figure below shows all terms used in this datasheet, with associated convention for positive values. Voltages and currents are defined accordingly.

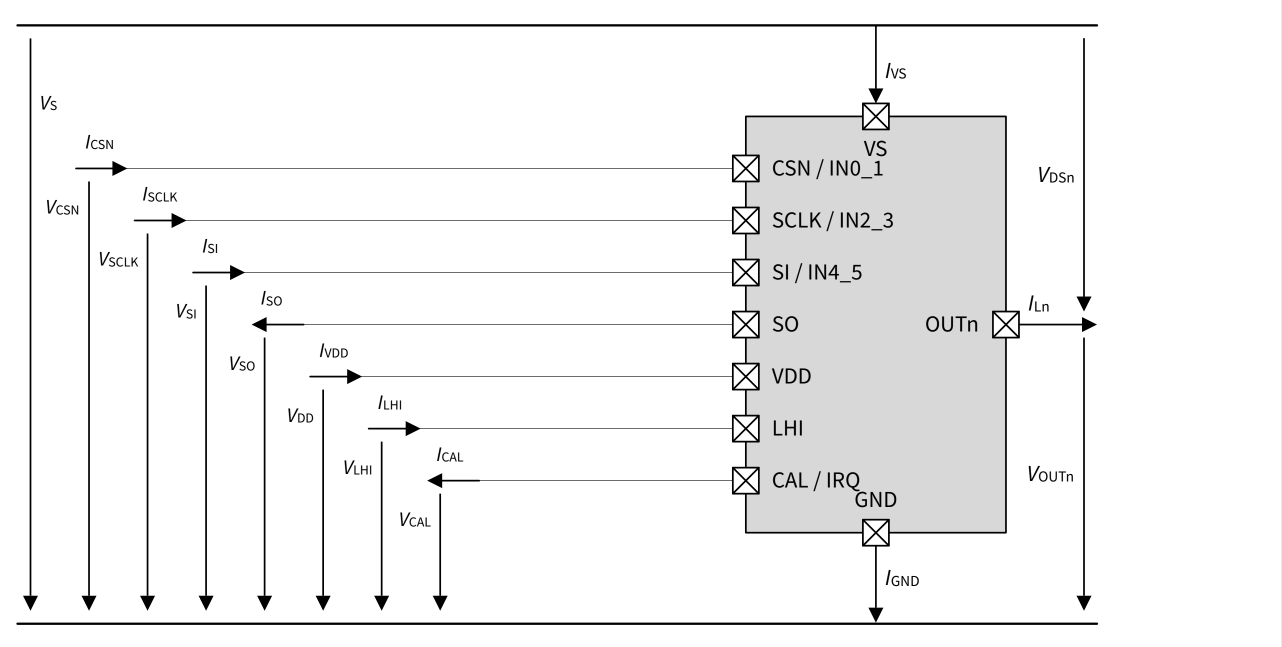


Figure 2 Voltage and current convention

3 Pin configuration

3.1 Pin assignment

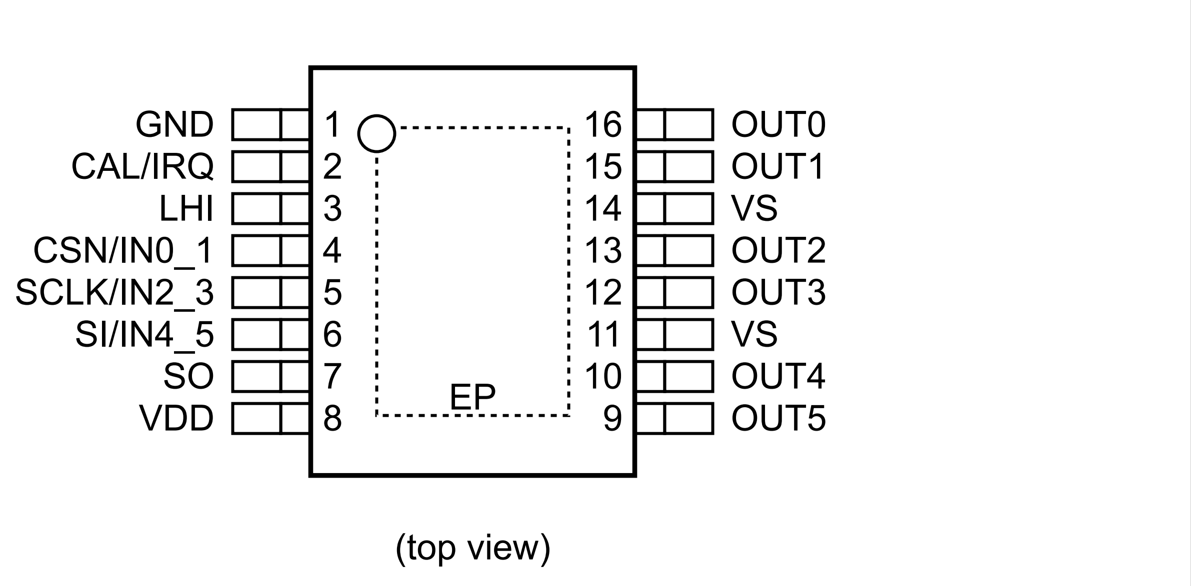


Figure 3 Pin configuration

3.2 Pin definitions and functions

Table 2 Pin definition

Pin	Symbol	I/O	Function
EP	GND	–	**Ground** Connect to IC ground - not used as electrical GND pin
1	GND	–	**Ground** Ground connection for internal logic
2	CAL / IRQ	I / O	**Calibration for internal current reference** A resistor R_{CAL} needs to be connected between CAL pin and GND pin to calibrate the ADC reference current. "Z" (tri-state) when no protection-based interrupt is present and not in calibration mode **Interruption request** ("HIGH" active)
3	LHI	I	**Limp home input** ("HIGH" active) If not used: Connect with a 10 kΩ resistor either to GND pin or to module ground
4	CSN / IN0_1	I	**Chip select of SPI interface** ("LOW" active) **Input power stage 0_1** ("HIGH" active)
5	SCLK / IN2_3	I	**Serial clock of SPI interface** ("HIGH" active) **Input power stage 2_3** ("HIGH" active)
6	SI / IN4_5	I	**Serial input of SPI interface** ("HIGH" active) **Input power stage 4_5** ("HIGH" active)

(table continues...)

Table 2 (continued) Pin definition

Pin	Symbol	I/O	Function
7	SO	O	**Serial output of SPI interface** "Z" (tri-state) when CSN = "HIGH"
8	VDD	–	**Digital supply voltage**
9,10,12, 13,15,16	OUTn	O	**Output n** Protected high-side power output channel n
11, 14	VS	–	**Power supply voltage** Battery voltage

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

$T_J = T_{J(NOR)}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	28	V	–	PRQ-106
Digital supply voltage	V_{DD}	-0.3	–	5.5	V	–	PRQ-108
Load dump voltage	$V_{BAT(LD)}$	–	–	35	V	Suppressed load dump acc. to ISO16750-2 (2023); $R_i = 2\ \Omega$	PRQ-109
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	20	V	Setup acc. to AEC-Q100-012 (2006), single channel configuration	PRQ-113
Reverse polarity voltage	$V_{BAT(REV)}$	-18	–	–	V	$t_{REV} \leq 5$ min, $T_A = 25°C$; Setup as described in Application information	PRQ-115
Current through GND pin	I_{GND}	-160	–	50	mA	–	PRQ-118
Current through VDD pin	I_{VDD}	-160	–	30	mA	$t_{REV} \leq 5$ min	PRQ-120
Digital input (DI) pins: CSN / IN0_1, SCLK / IN2_3, SI / IN4_5, LHI							
Voltage at DI pin	V_{DI}	-0.3	–	5.5	V	1)	PRQ-838
Current through DI pin - reverse battery condition	$I_{DI(REV)}$	-1	–	16	mA	t_{REV} <= 5 min 1)	PRQ-125
Digital output (DO) pins: SO, CAL / IRQ							
Voltage at DO pin	V_{DO}	-0.3	–	V_{DD} + 0.3	V	2)	PRQ-126
Current through DO pin - reverse battery condition	$I_{DO(REV)}$	-16	–	6	mA	t_{REV} <= 5 min2)	PRQ-129
Analog output (AO) pin: CAL / IRQ							
Voltage at AO pin	V_{AO}	-0.3	–	V_{DD} + 0.3	V	3)	PRQ-839
Current through AO pin - reverse battery condition	$I_{AO(REV)}$	-16	–	6	mA	t_{REV} <= 5min 3)	PRQ-837

(table continues...)

Table 3 **(continued) Absolute maximum ratings**

$T_J = T_{J(NOR)}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-799
Junction temperature for safety mechanisms	T_J	-40	–	200	°C	Protection functions operational $t < 10$ hours	PRQ-886
Storage temperature	T_{STG}	-55	–	150	°C	–	PRQ-136
ESD robustness							
ESD robustness all pins (HBM)	V_{ESD_HBM1}	-2	–	2	kV	4)	PRQ-137
ESD robustness OUTn vs GND and VS connected (HBM)	V_{ESD_HBM2}	-4	–	4	kV	4)	PRQ-138
ESD robustness all pins (CDM)	V_{ESD_CDM1}	-500	–	500	V	5)	PRQ-139
ESD robustness corner pins (CDM)	V_{ESD_CDM2}	-750	–	750	V	5)	PRQ-140
Power stage							
Maximum energy dissipation - single pulse	E_{AS}	–	–	12	mJ	$I_{Ln} = 2 \cdot I_{L(NOM)\_85}$, $T_{J(0)} = 150°C$, $V_S = 28$ V	PRQ-142
Maximum energy dissipation - repetitive pulse	E_{AR}	–	–	3.5	mJ	$I_{Ln} = I_{L(NOM)\_85}$, $T_{J(0)} = 85°C$, $V_S = 13.5$ V, 1M cycles	PRQ-143
Maximum energy dissipation - repetitive pulse (relay)	$E_{AR(RELAY)}$	–	–	10	mJ	$I_{Ln} = 220$ mA, $T_{J(0)} = 85°C$, $V_S = 13.5$ V, 1M cycles	PRQ-981
Current through output pins	I_{OUTn}	$-I_{L(HOCT),Max}$	–	$I_{L(HOCT),Max}$	A	$T_J < T_{J(ABS)}$, $(T_J - T_{J(0)}) < 60$ K	PRQ-144

1) Maximum V_{DI} to be considered for latch-up tests: 5.5 V
2) Maximum V_{DO} to be considered for latch-up tests: 5.5 V
3) Maximum V_{AO} to be considered for latch-up tests: 5.5 V
4) Human body model (HBM) robustness according to AEC - Q100-002
5) Charged device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply voltage range for normal operation	$V_{S(NOR)}$	5	13.5	18	V	–	PRQ-145
Lower extended power supply voltage range for operation	$V_{S(EXT,LOW)}$	3.5	–	5	V	(Parameter deviations possible) 1) 2)	PRQ-147
Upper extended power supply voltage range for operation	$V_{S(EXT,UP)}$	18	–	28	V	$t < 1$ h (parameter deviations possible) 2)	PRQ-149
Digital supply voltage range for normal operation	$V_{DD(NOR)}$	3.0	–	5.5	V	–	PRQ-151
Junction temperature range for normal operation	$T_{J(NOR)}$	-40	25	150	°C	–	PRQ-152

1) In case of V_S voltage decreasing, $V_{S(EXT,LOW),MIN} = V_{S(UV),MAX}$. In case of V_S voltage increasing, $V_{S(EXT,LOW),MIN} = V_{S(OP),MAX}$

2) Device protection functions still operative

Note: *Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the Electrical Characteristics tables.*

4.3 Thermal resistance

Table 5 Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-top	Ψ_{JTOP}	–	6.4	10.3	K/W	1)	PRQ-488

(table continues...)

Table 5 (continued) Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction-to-case	R_{thJC}	–	1.7	2.7	K/W	Simulated at exposed pad [1]	PRQ-489
Thermal resistance junction-to-ambient	R_{thJA}	–	34	–	K/W	[1]	PRQ-490

1) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W

4.3.1 PCB setup

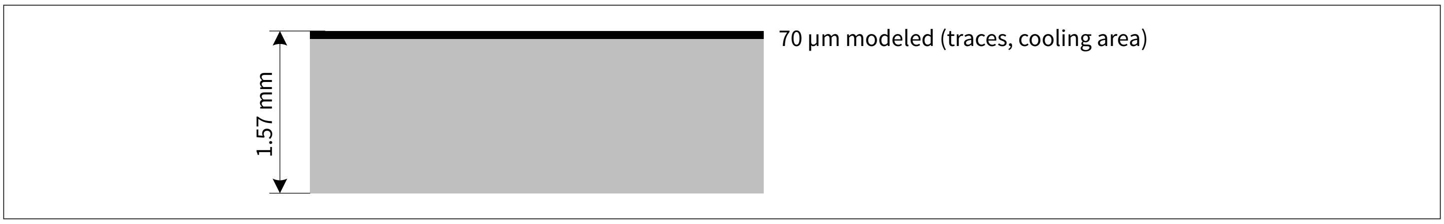


Figure 4 **1s0p PCB cross section**

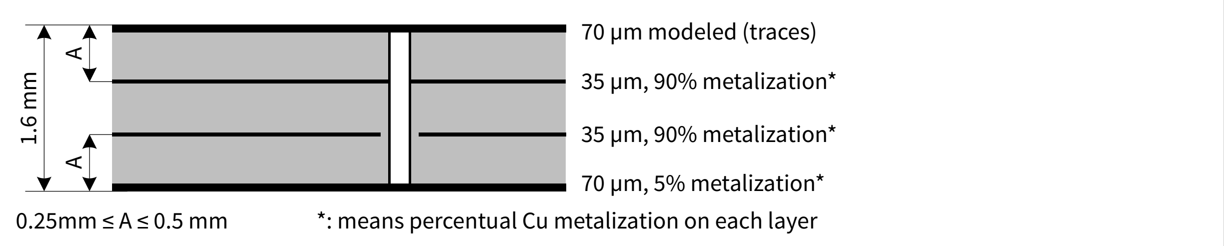


Figure 5 **2s2p PCB cross section**

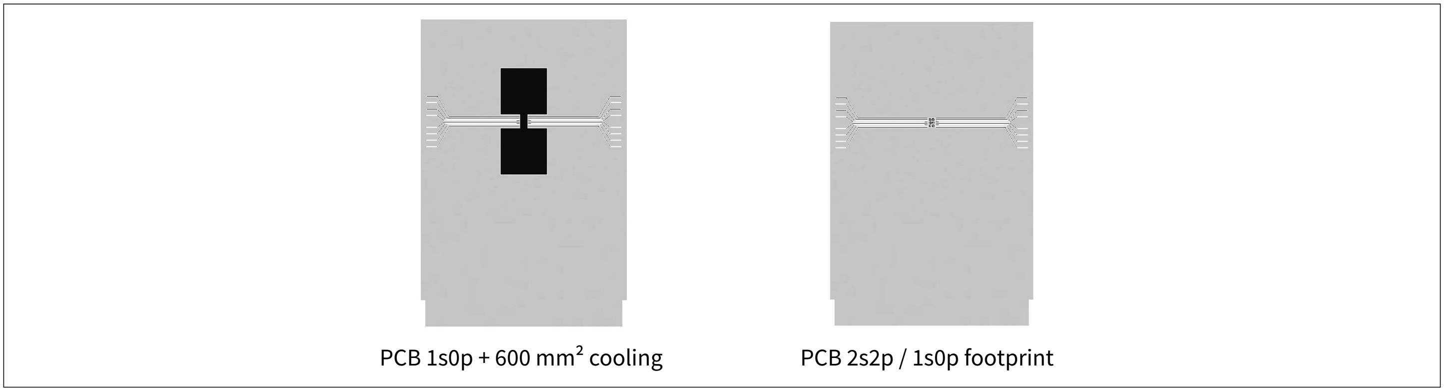


Figure 6 **PCB setup for thermal simulations**

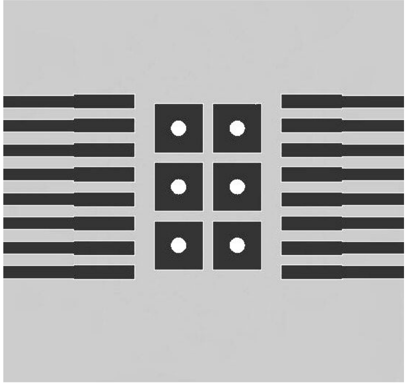


Figure 7 Thermal vias on PCB for 2s2p PCB setup

4.3.2 Thermal impedance

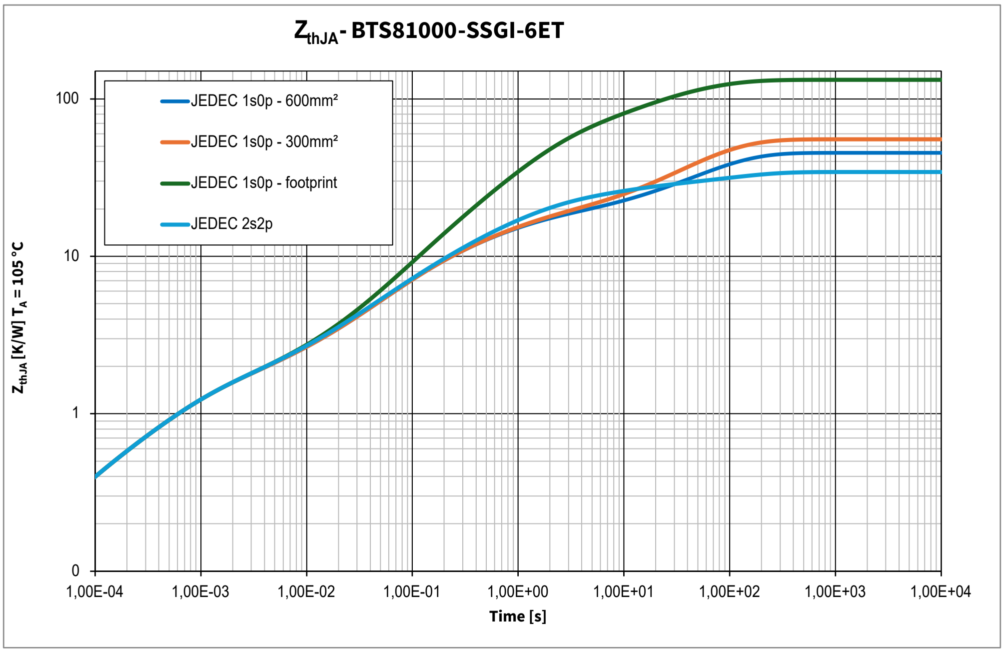


Figure 8 Typical thermal impedance

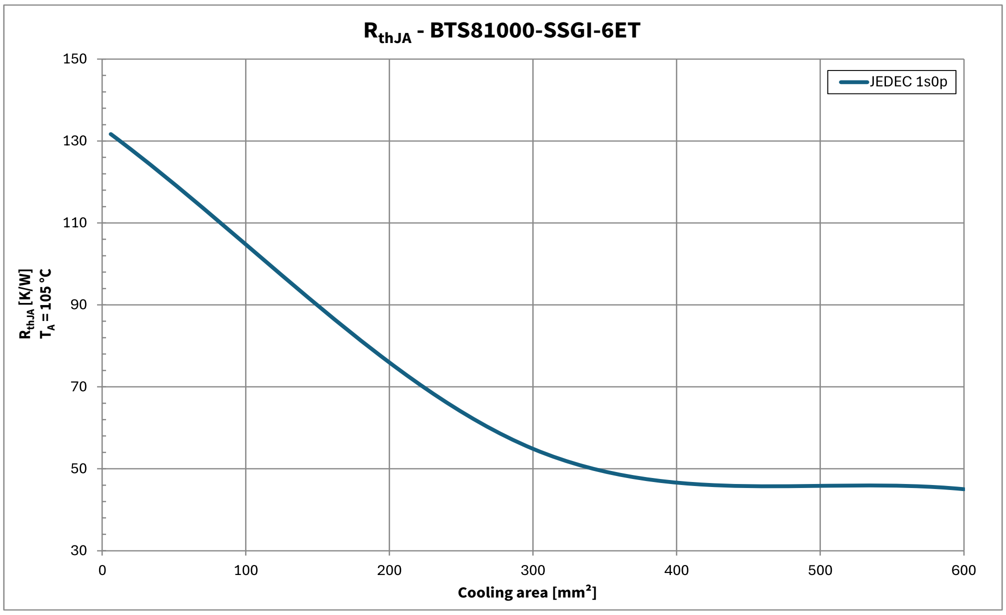


Figure 9 Typical thermal resistance on 1s0p PCB with various cooling surfaces

5 Logic I/O

5.1 Digital I/O pins

The device has five digital input (DI) pins: CSN / IN0_1, SCLK / IN2_3, SI / IN4_5, LHI

The digital input circuitry is compatible with 3.3 V and 5 V microcontrollers. The logic thresholds for “LOW” and “HIGH” states are defined by the parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in the figure below. The voltage V_{DI} needed to ensure a “HIGH” state is always higher than the voltage needed to ensure a “LOW” state.

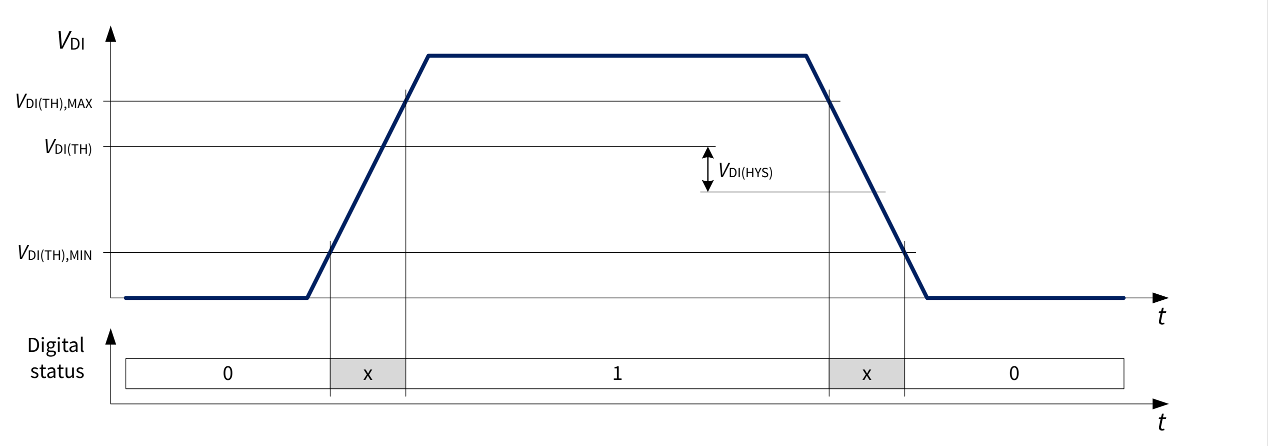


Figure 10 **Digital input threshold voltages and hysteresis**

In case a digital input pin is not used, it has be connected by a 10 kΩ resistor either to GND pin or to module ground.

The device has two digital output (DO) pins: SO, CAL / IRQ

5.1.1 Input pin

In case of $V_{LHI} > V_{DI(TH)}$ the SPI pins CSN, SCLK and SI are configured as input pins to control the power stages. CSN / IN0_1 is mapped to control OUT0_1, SCLK / IN2_3 is mapped to control OUT2_3 and SI / IN4_5 is mapped to control OUT4_5.

The electrical equivalent of the input circuitry is shown below.

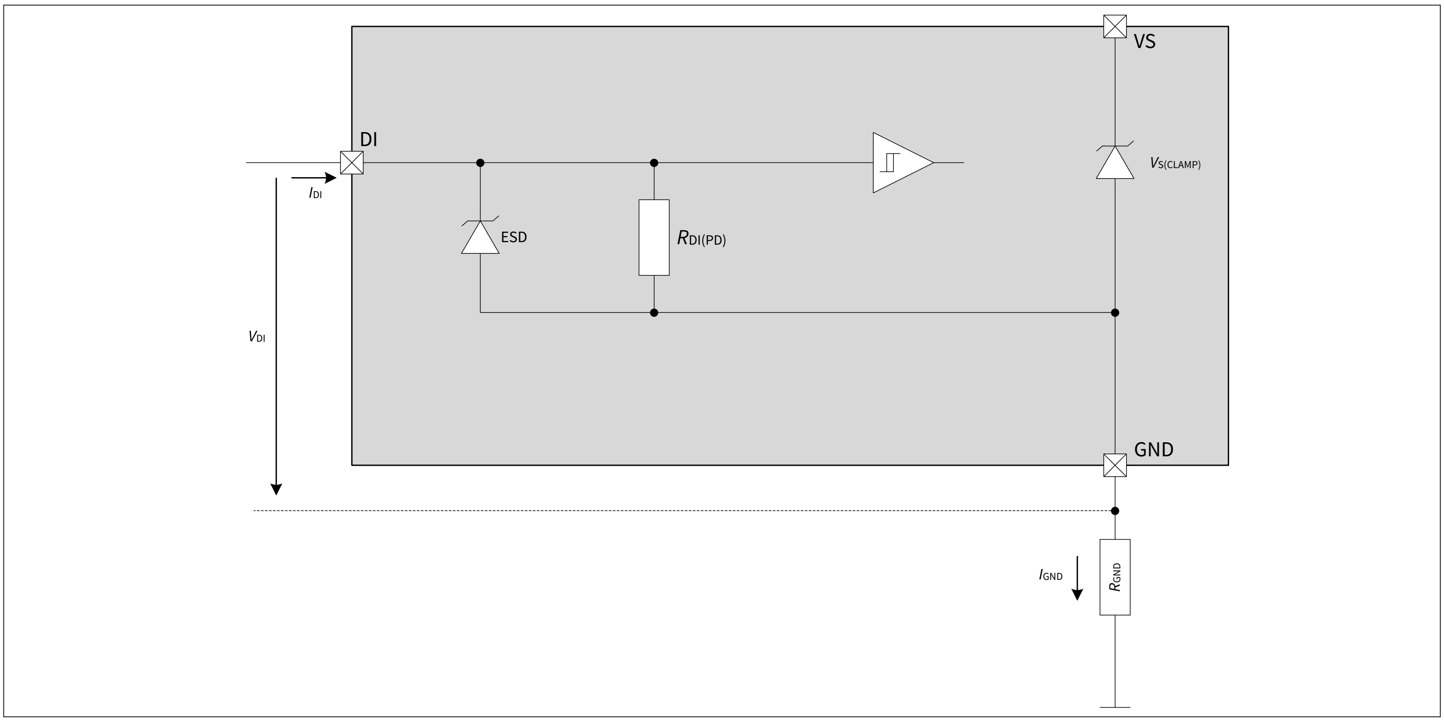


Figure 11 Input circuitry

5.1.2 SPI pins

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN.

The electrical equivalent of the CSN circuitry is shown below.

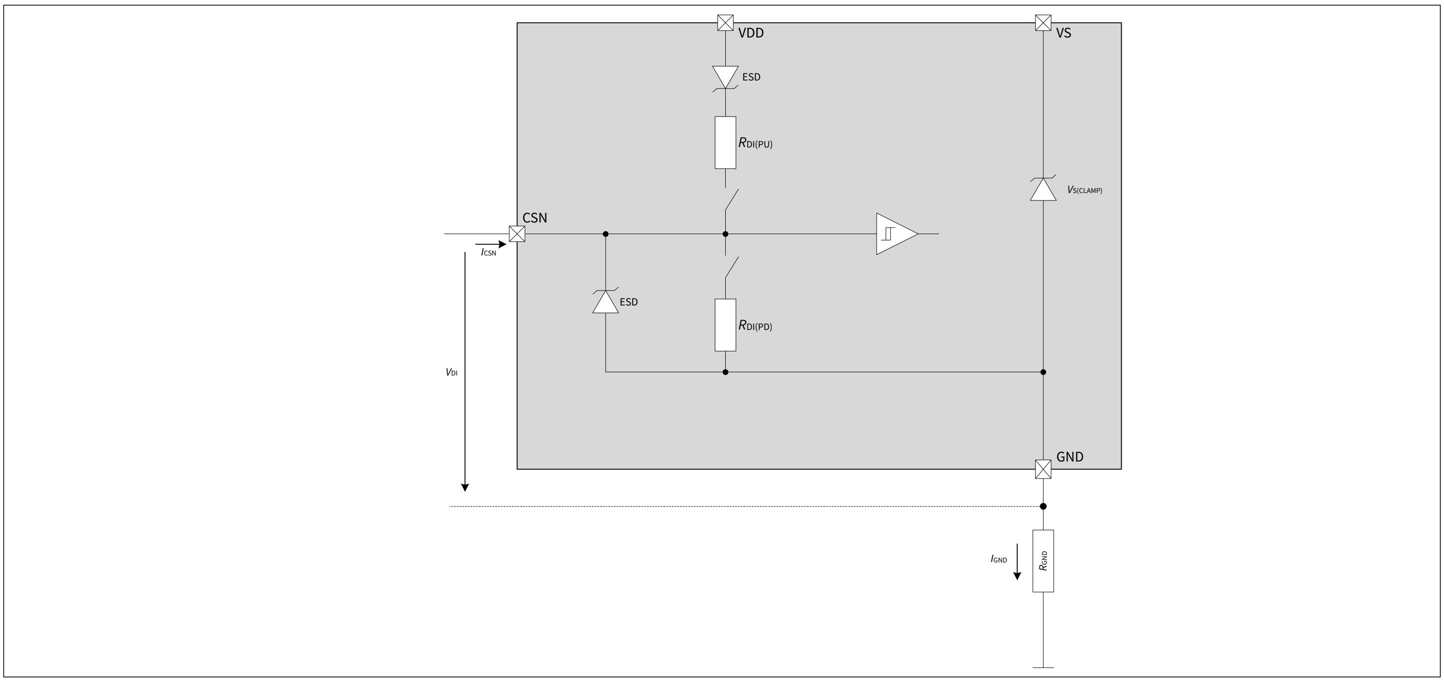


Figure 12 CSN circuitry

The electrical equivalent of the SO circuitry is shown below.

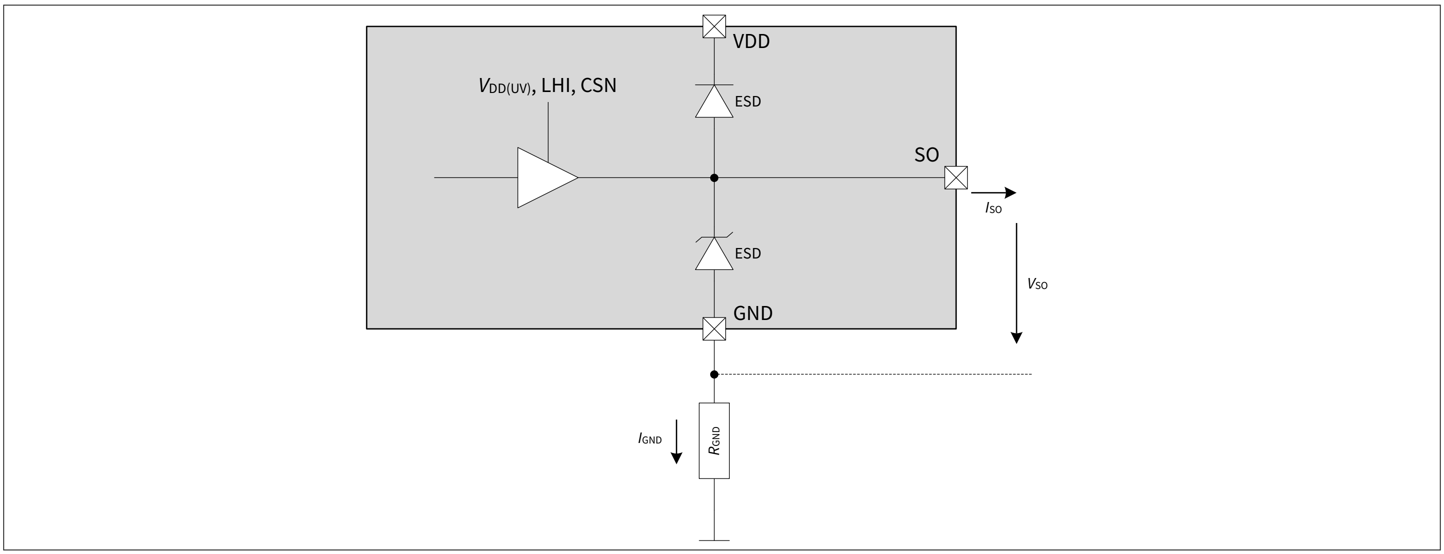


Figure 13 SO circuitry

5.1.3 Limp home input pin

For activating the limp home mode, the device features a limp home input pin. The electrical equivalent of the limp home circuitry is shown below.

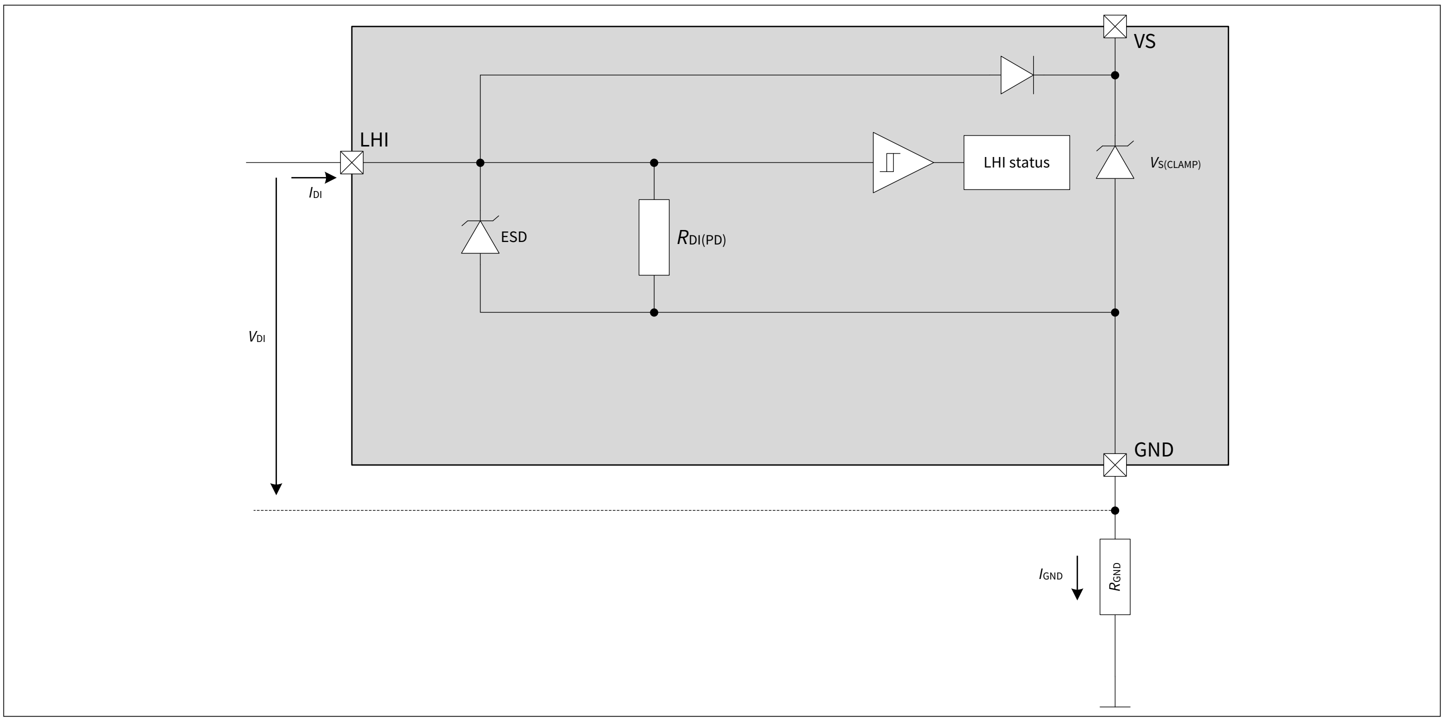


Figure 14 LHI circuitry

5.2 Analog I/O pins

Analog output (AO) pin: CAL / IRQ

5.2.1 Calibration / Interrupt Request pin

The CAL / IRQ pin is used to trim the internal reference current and adjust the gain of the digital current measurement. Additionally, if a protection mechanism is triggered the device reports via this pin an interrupt request to the host controller.

The electrical equivalent of the input circuitry is shown below.

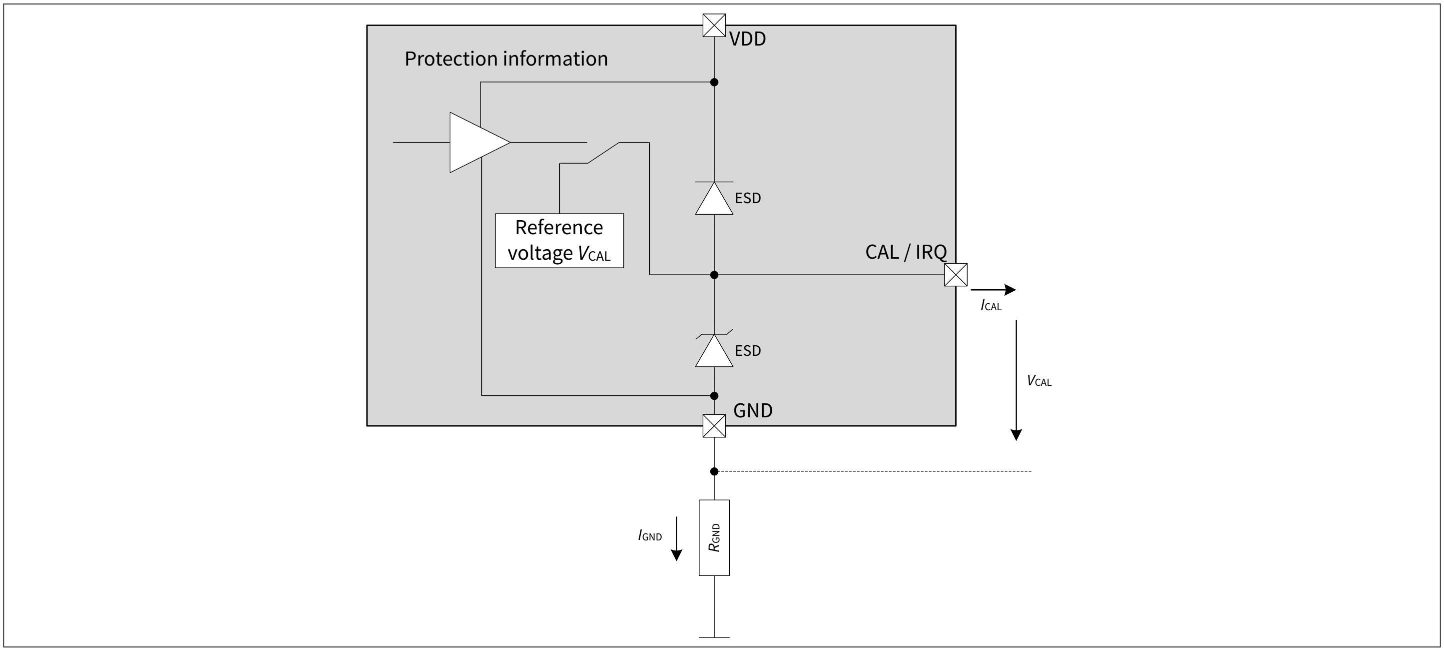


Figure 15 **CAL / IRQ circuitry**

5.3 Electrical characteristics logic I/O pins

Table 6 **Electrical characteristics logic I/O pins**

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital input (DI) pins: CSN / IN0_1, SCLK / IN2_3, SI / IN4_5, LHI							
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	2	V	–	PRQ-157
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	–	PRQ-161
Digital input pull-down resistor	$R_{DI(PD)}$	35	50	65	kΩ	–	PRQ-833
Digital input pull-up resistor	$R_{DI(PU)}$	35	50	65	kΩ	–	PRQ-834

(table continues...)

Table 6 (continued) Electrical characteristics logic I/O pins

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital output (DO) pins: SO, CAL / IRQ							
Digital output voltage ("HIGH") of pin IRQ	$V_{IRQ(H)}$	V_{DD} - 0.5	–	V_{DD}	V	R_{CAL} = 1 kΩ	PRQ-802
Output tristate leakage current of pin IRQ	$I_{IRQ(OFF)}$	-1	–	1	µA	No protection-based interrupt at CAL / IRQ pin and not in calibration mode $0\ V \leq V_{IRQ} \leq V_{DD(NOR)}$	PRQ-803
Digital output voltage ("LOW") of pin SO	$V_{SO(L)}$	–	–	0.5	V	$I_{SO} \geq -0.5$ mA	PRQ-169
Digital output voltage ("HIGH") of pin SO	$V_{SO(H)}$	V_{DD} - 0.5	–	V_{DD}	V	$I_{SO} \leq 0.5$ mA	PRQ-168
Output tristate leakage current of pin SO	$I_{SO(OFF)}$	-1	–	1	µA	$V_{CSN} \geq V_{DI(TH),MAX}$ $0\ V \leq V_{SO} \leq V_{DD(NOR)}$	PRQ-170
Analog output (AO) pins: CAL / IRQ							
CAL pin reference voltage	V_{CAL}	–	1	–	V	No protection-based interrupt at CAL / IRQ pin and CAL bit set	PRQ-809

6 Power management

The device is supplied by two supply voltages:

- Power supply voltage (V_S)
- Digital supply voltage (V_{DD})

The supply line of the V_S is connected to a battery feed and used for the driving circuitry of the power stage, while V_{DD} is used for the digital interface. Both supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the respective undervoltage threshold. More in detail:

- An undervoltage on V_{DD} prevents digital interface communication.
- An undervoltage on V_S switches OFF the power stage, even in limp home mode. The power stage is enabled again as soon as $V_S \geq V_{S(OP)}$.

6.1 Device capability as function of VS and VDD

	$V_{DD} \leq V_{DD(UV)}$	$V_{DD} > V_{DD(OP)}$
$V_S \leq V_{S(UV)}$	Channels are OFF	Channels are OFF
	SPI register reset	SPI registers available
	SPI communication not available	SPI communication available
	Limp home mode not available	Limp home mode not available
$V_S > V_{S(UV)}$	Channels cannot be controlled by SPI	Channels can be controlled by SPI
	SPI register protected	SPI registers available
	SPI communication not available	SPI communication available
	Limp home mode available	Limp home mode available

6.2 Operation modes and transitions

6.2.1 Operation modes

The device has the following operation modes:

- Unsupplied
- Power up
- Inactive
- Active
- Limp home

The transition between operation modes is determined according to these variables:

- Power supply voltage (V_S)
- Digital supply voltage (V_{DD})
- Output control register
- Logic level at SPI pins in case $V_{LHI} > V_{DI(TH)}$ for $t > t_{LHI(AC)}$
- Logic level at LHI pin

The state diagram including the possible transitions is shown below. The behavior of device as well as some parameters may change independent from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S power supply voltage and VDD digital supply voltage, some changes within the same operation mode can be observed.

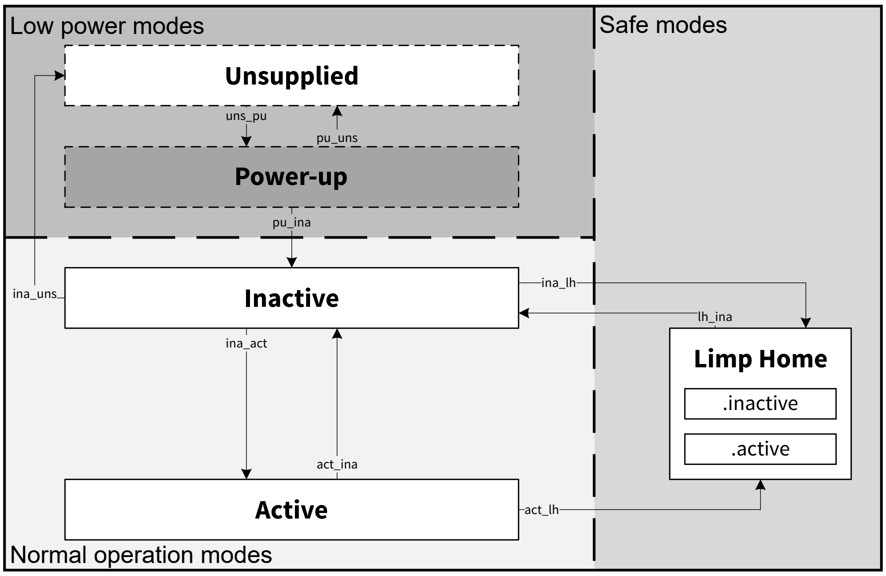


Figure 16 Operation mode state diagram

The table below shows the correlation between operation modes, V_S power supply voltage, V_{DD} digital supply voltage, and the states of the most important functions.

6.2.1.1 Device function in relation to operation modes, VS and VDD voltages

Operation mode	Function	$V_S \leq V_{S(UV)}$	$V_S > V_{S(UV)}$
Inactive mode	Channels	OFF	OFF
	SPI register	available (1)	available (1)
	SPI communication	available (1)	available (1)
Active mode	Power stage	OFF	controlled by SPI
	SPI register	available (1)	available (1)
	SPI communication	available (1)	available (1)
Limp home mode	Channels	OFF	Channels ON if V_{SCN}, V_{SCLK}, $V_{SI} > V_{DI(TH)}$
	SPI register	protected (1)	protected
	SPI communication	all commands rejected (1)	all commands rejected (1)

1) In case $V_{DD} > V_{DD(OP)}$ otherwise not available or in reset

6.2.1.2 Unsupplied

In this mode the device supply voltage is below the undervoltage threshold $V_{S(UV)}$ and $V_{DD(UV)}$.

6.2.1.3 Power-up

The power-up will be performed when the power supply voltage (V_S) or digital supply voltage (V_{DD}) is applied to the device and increases above the power supply minimum operating voltage $V_S > V_{S(OP)}$ or digital supply minimum operating voltage $V_{DD} > V_{DD(OP)}$. The power-up time is t_{PU}.

6.2.1.4 Inactive mode

The device is in inactive mode in case one of the supply voltages is above its normal operating voltage ($V_S > V_{S(OP)}$ or $V_{DD} > V_{DD(OP)}$) and all power stages are disabled.

In inactive mode, the power stage is OFF with limited diagnosis and protection mechanisms available.

In case $V_{DD} > V_{DD(OP)}$ the device can be configured and controlled via intended registers.

In inactive mode and active mode VMON, CAL and ADC are disabled per default and can be enabled via the digital interface.

6.2.1.5 Active mode

The active mode is that operation mode where the power stage is enabled via the power stage control and all diagnosis and protection mechanisms are functional.

The active mode with digital current sense disabled is the low current consumption mode (idle) where the power stage is enabled via the power stage control, and protection mechanisms are functional.

6.2.1.6 Limp home mode

The device enters limp home mode when the LHI pin is set to "HIGH" for $t > t_{LHI(AC)}$.

When the limp home mode is entered, the control and configuration registers are reset to their default values and the overcurrent protection is set to the highest value.

Furthermore all registers are protected.

The device can be configured via the digital interface to not reset the output configuration and current limitation settings when limp home mode is entered. These settings are used by the device when limp home mode is left.

The corresponding register bit will be set once the LHI pin is set to "HIGH" and can be read via the digital interface.

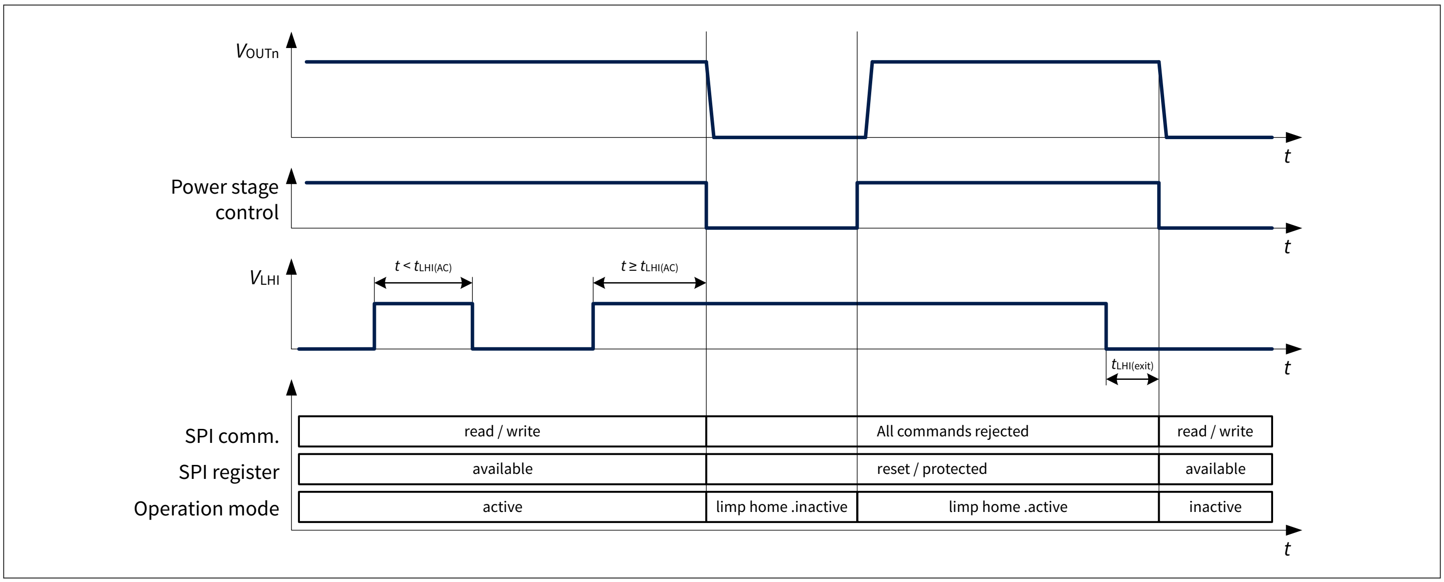


Figure 17 **Limp home mode activation diagram**

Depending of $V_{DI(TH)}$ on CSN, SCLK, and SI pins, the device changes between two different limp home sub-modes:

- Limp home inactive: this sub-mode is entered when the power stage control = LOW.
- Limp home active: this sub-mode is entered when the power stage control = HIGH.

6.2.2 Transitions

Table 7 **Operating transition conditions**

Name	Start mode	End mode	Transition condition
uns_pu	Unsupplied	Power up	$V_S > V_{S(UV)}$ or $V_{DD} > V_{DD(UV)}$
pu_uns	Power up	Unsupplied	$V_S \leq V_{S(UV)}$ and $V_{DD} \leq V_{DD(UV)}$

(table continues...)

Table 7 (continued) Operating transition conditions

Name	Start mode	End mode	Transition condition
pu_ina	Power up	Inactive	$t > t_{PU}$
ina_uns	Inactive	Unsupplied	$V_S \leq V_{S(UV)}$ and $V_{DD} \leq V_{DD(UV)}$
ina_act	Inactive	Active	Power stage control = "HIGH"
act_ina	Active	Inactive	Power stage control = "LOW"
act_lh	Active	Limp home	$V_{LHI} > V_{DI(TH)}$ for $t > t_{LHI(AC)}$
ina_lh	Inactive	Limp home	$V_{LHI} > V_{DI(TH)}$ for $t > t_{LHI(AC)}$
lh_ina	Limp home	Inactive	$V_{LHI} < V_{DI(TH)}$ for $t_{LHI(exit)}$

6.2.3 Availability of protection and diagnosis functions

The availability of protection mechanisms and diagnosis functions of the device depends on the operation mode in which the device is. A detailed overview is shown in the tables below.

Table 8 Mode vs. protection overview

Mode	Sub-mode	Overvoltage protection	Overcurrent protection	Overtemperature protection
Unsupplied	**n.a.**	Available	Not available	Not available
Power-up	**n.a.**	Available	Not available	Not available
Inactive	**n.a.**	Available	Not available	Not available
Active	**ADC enabled**	Available	Available	Available
Active	**ADC disabled**	Available	Available	Available
Limp home	**Inactive**	Available	Not available	Not available
Limp home	**Active**	Available	Available (max)	Available

Table 9 Mode vs. diagnosis overview

Mode	Sub-mode	Digital current sense	Voltage monitoring	Overtemperature warning
Unsupplied	**n.a.**	Not available	Not available	Not available
Power-up	**n.a.**	Not available	Not available	Not available
Inactive	**n.a.**	Not available	Available	Not available
Active	**n.a.**	Available	Available	Available
Limp home	**Inactive**	Not available	Not available	Not available
Limp home	**Active**	Not available	Not available	Not available

6.3 Undervoltage on VS

The power output stage follows the input state as long as $V_S > V_{S(OP)}$.

In case the power output stage of the device is switched ON and the supply voltage drops below or equal to $V_{S(UV)}$, the internal logic switches OFF the power output stage.

In case of an undervoltage event on V_S an indication via the digital interface is performed.

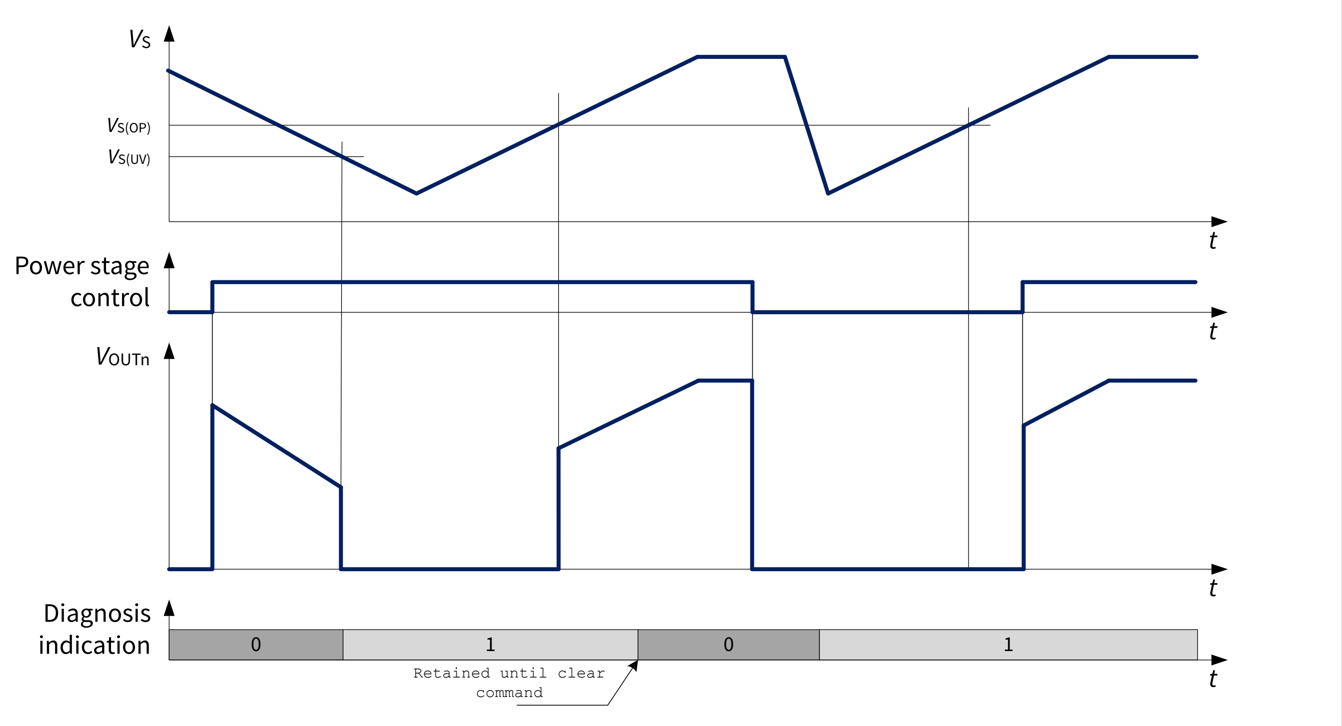


Figure 18 V_S undervoltage behavior

6.4 Undervoltage on VDD

The undervoltage mechanism of the digital supply voltage is triggered when $V_{DD} \leq V_{DD(UV)}$.

In case of an undervoltage event on V_{DD} an indication via the digital interface is performed.

As soon as the digital supply voltage recovers and the condition $V_{DD} > V_{DD(OP)}$ is fulfilled, the digital interface communication is enabled after $t_{WU(SPI)}$ and the digital supply undervoltage bit is set and can be read via the digital interface.

6.5 Electrical characteristics power management

Table 10 **Electrical characteristics power management**

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Power supply undervoltage shutdown	$V_{S(UV)}$	1.8	3.3	3.5	V	V_S decreasing	PRQ-218

(table continues...)

Table 10 (continued) Electrical characteristics power management

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply minimum operating voltage	$V_{S(OP)}$	2	3	4.1	V	V_S increasing	PRQ-220
Power supply overvoltage detection	$V_{S(OV)}$	33	35	37	V	–	PRQ-859
Digital supply undervoltage shutdown	$V_{DD(UV)}$	1.3	2.2	2.4	V	V_{DD} decreasing	PRQ-225
Digital supply minimum operating voltage	$V_{DD(OP)}$	1.4	2.7	2.8	V	V_{DD} increasing	PRQ-226
Digital supply clamping voltage	$V_{DD(CLAMP2)}$	6	6.2	8	V	$I_{VDD} \leq 20$ mA	PRQ-811
Current consumptions							
Digital supply current consumption in normal operation (average)	$I_{VDD(NORMAL)}$	–	–	1.9	mA	Device in a normal operation mode, 0 Hz < $f_{SCLK} \leq 5$ MHz, $C_{L(SO)} = 50$ pF	PRQ-812
Operating current in active mode (all power stages ON)	$I_{GND(ACTIVE)}$	–	–	3.2	mA	Device in active mode, ADC and VMON enabled	PRQ-790
Operating current in active mode without diagnosis (all power stages ON, TJ < 85°C)	$I_{GND(ACTIVE\_WOD)85}$	–	–	128	µA	Device in active mode, diagnosis disabled, no SPI communication, $T_J < 85°C$, $I_{Ln} = 0$ A	PRQ-791
Operating current in active mode without diagnosis (all power stages ON)	$I_{GND(ACTIVE\_WOD)}$	–	–	800	µA	Device in active mode with $I_{Ln} = 1$A, diagnosis disabled	PRQ-927
Operating current in inactive mode	$I_{GND(INACTIVE)}$	–	7	25	µA	$T_J < 85°C$, Device in inactive mode, diagnosis disabled	PRQ-792
Operating current in limp home mode, all channels ON	$I_{GND(LH)}$	–	–	2.4	mA	Device in limp home mode, $T_J \leq 85°C$	PRQ-793
Operating current in case voltage monitor enabled	$I_{GND(INACTIVE\_WD)}$	–	145	–	µA	–	PRQ-826
Timings							
Digital interface wake-up time	$t_{WU(SPI)}$	–	–	1	µs	–	PRQ-795
Power-up time	t_{PU}	–	–	100	µs	–	PRQ-823

(table continues...)

Table 10 **(continued) Electrical characteristics power management**

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Limp home acknowledgement time	$t_{LHI(AC)}$	10	20	40	µs	–	PRQ-709
Limp home exit filter time	$t_{LHI(exit)}$	1	4.5	6	µs	–	PRQ-883
Transition time inactive to active	$t_{T(INA\_ACT)}$	3	–	50	µs	–	PRQ-784
Transition time active to inactive	$t_{T(ACT\_INA)}$	1	–	70	µs	–	PRQ-785
Transition time inactive to unsupplied	$t_{T(INA\_UNS)}$	–	–	10	µs	–	PRQ-825
Transition time inactive to limp home	$t_{T(INA\_LH)}$	10	–	50	µs	–	PRQ-786
Transition time limp home to inactive	$t_{T(LH\_INA)}$	5	–	70	µs	–	PRQ-824
Transition time active to limp home	$t_{T(ACT\_LH)}$	10	–	40	µs	–	PRQ-787

7 Power stage

The high-side power stages are built using a n-channel lateral power MOSFET with a charge pump, controlled via the power stage control.

7.1 Power stage control

The power stage control signal enables or disables the corresponding power stage and is sensitive to two input parameters:

- Output control bit
- Input control logic in case $V_{LHI} > V_{DI(TH)}$ (SPI pins CSN, SCLK and SI are configured as input pins)

7.2 Power stage ON-state resistance

As shown below, the ON-state resistance $R_{DS(ON)}$ mainly depends on the junction temperature T_J. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150°C.

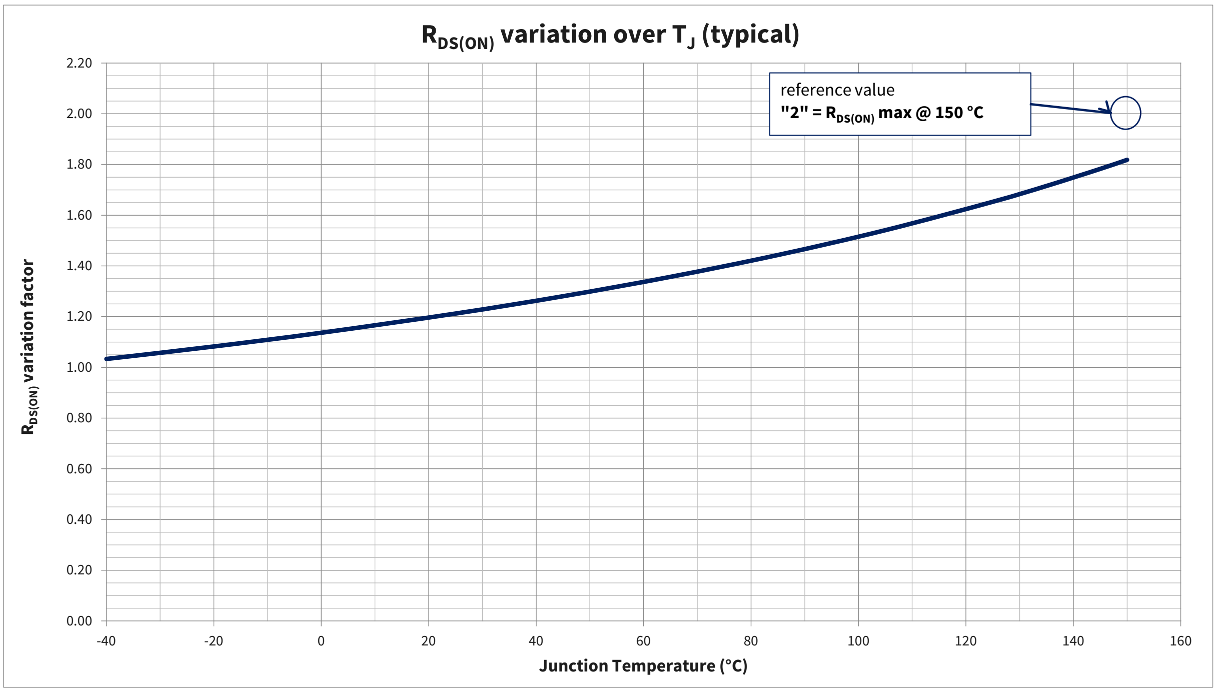


Figure 19 **$R_{DS(ON)}$ variation factor**

7.3 Switching loads

7.3.1 Switching resistive loads

When switching resistive loads, the switch energy values E_{ON} and E_{OFF} are proportional to load resistance and times t_{ON} and t_{OFF}.

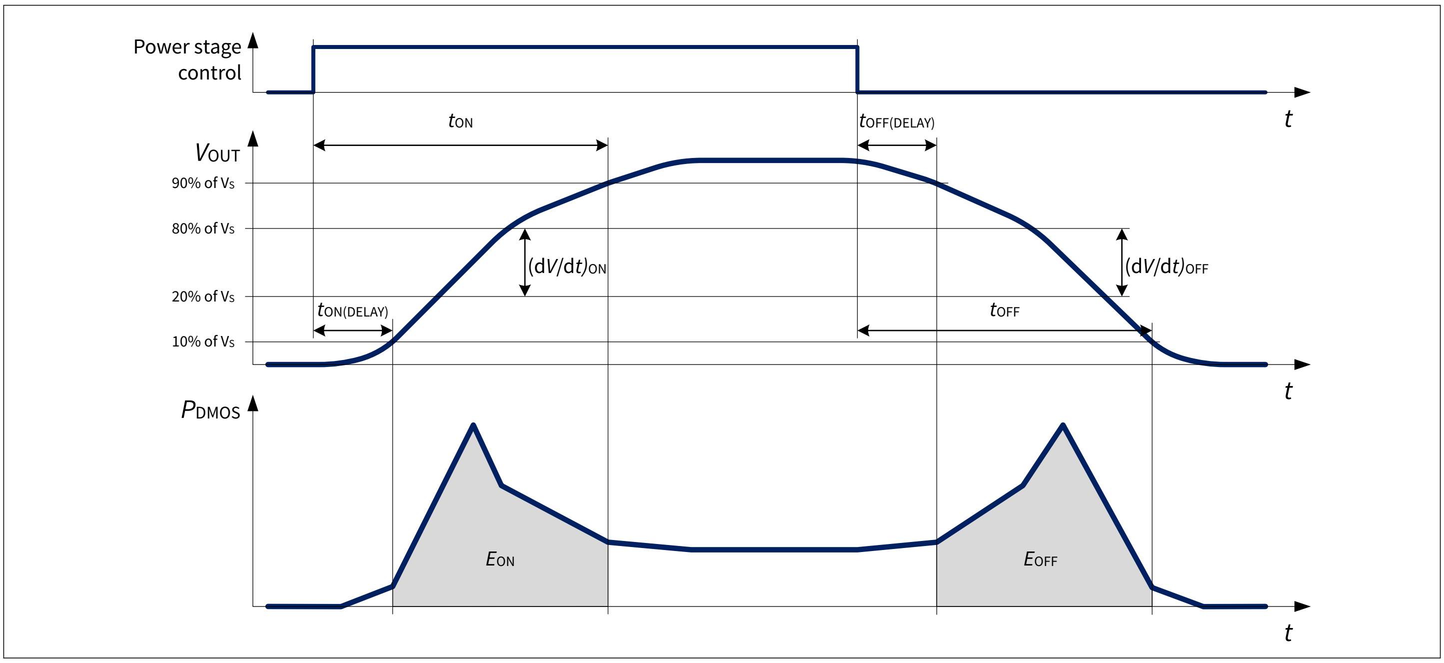


Figure 20 **Switching a resistive load**

7.3.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUTn} drops below the ground potential, as a consequence of the fact that the inductance continues driving the load current.

To prevent the destruction of the device due to overvoltage, a voltage clamping mechanism between the VS pin and the OUTn pin is available. The clamping structure limits the negative output voltage so that $V_{DSn} = V_{DS(CLAMP)}$.

The energy resulting from the demagnetization of inductive loads has to be dissipated in the power stage of the device. The energy can be calculated with:

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_{Ln}}{V_S - V_{DS(CLAMP)}}\right) + I_{Ln} \right] \cdot \frac{L}{R_L} \tag{1}$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Please refer to the maximum allowed values of E_{AS} (single pulse energy) and E_{AR} (repetitive energy).

***Note**:* *The device is not developed to be used as high-side switch in an H-bridge configuration paired with external low-side switches.*

7.3.3 Switching capacitive loads

When switching capacitive loads, the load current increases due to the inrush behavior of the load. Due to the high load current and V_{DS}, the power dissipation is increased during the charging phase of the capacitor. Therefore, the load driving capability is energy limited. To enable higher load driving performance the overtemperature protection restart strategy can be set to unlimited restarts.

The overcurrent limitation mechanism allows charging or re-charging of the capacitive load following battery transients (e.g., ISO pulses, micro interruptions, and load dump), with the maximum capacitive load limited by the thermal behavior of the device.

7.4 Advanced switching characteristics

The device supports switching of two neighbor power stages in parallel to a single load.

When two power stages are used in parallel, the total current capability $I_{L(NOM)}$ is doubled.

Since the current sense of the power stages used in parallel is not synchronized, the total current has to be calculated out of the current sense reading of each single power stage.

7.4.1 Inverse current behavior

When $V_{OUTn} > V_S$, a current $I_{L(INV)}$ flows into the power output transistor. This condition is known as "Inverse Current".

If the power stage is in OFF state, the current flows through the intrinsic body diode generating high power losses, causing an increase of overall device temperature. This can lead to a switch OFF of unaffected channels due to overtemperature.

If the power stage is switched ON during inverse current, the power dissipation is comparable to the one during normal operation, as the ON-state resistance is given by $R_{DS(INV)}$.

The feature of inverse ON allows to switch ON the channel during inverse current condition as long as $|I_{Ln}| < |I_{L(INV)}|$.

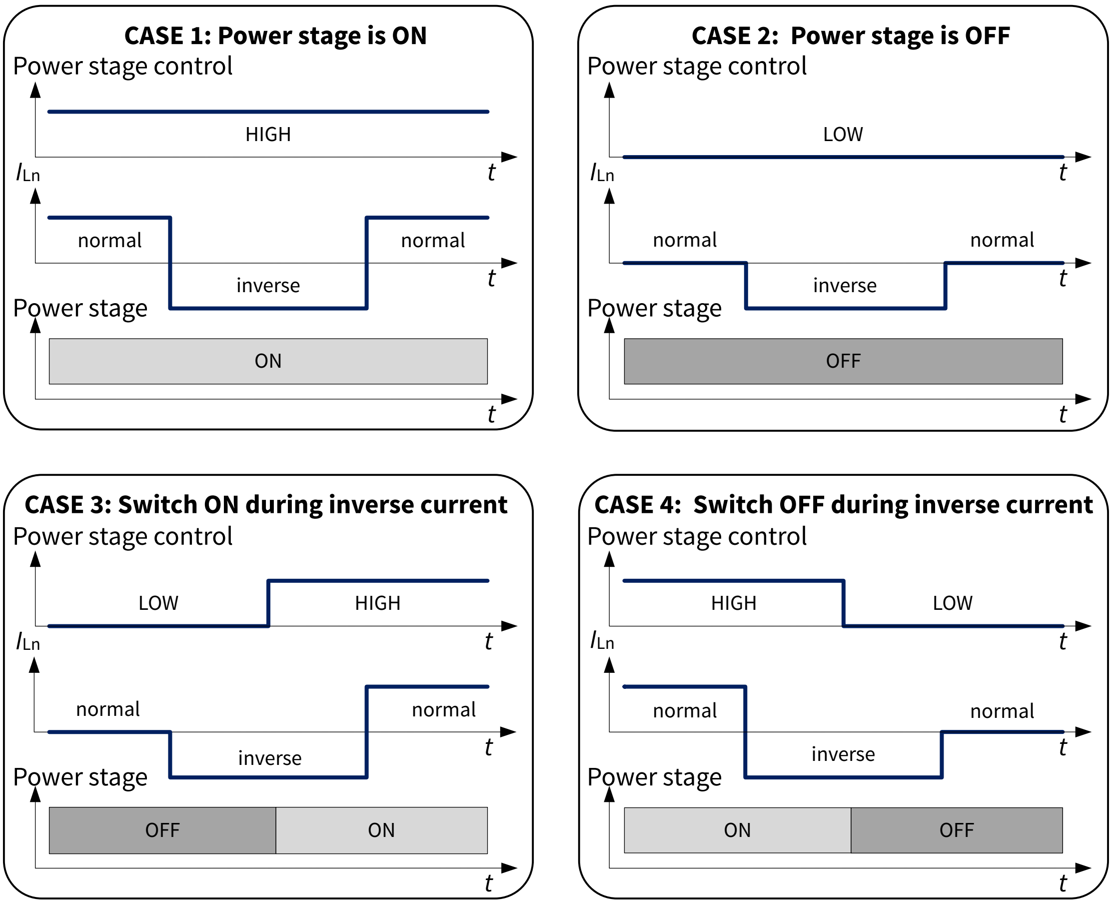


Figure 21 Inverse ON - power stage behavior in the case of applied inverse current

7.5 Electrical characteristics power stage

Table 11 **Electrical characteristics power stage**

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Drain to source clamping voltage	$V_{DS(CLAMP)}$	37	41	45	V	–	PRQ-247
Source to ground clamping voltage	$V_{OUT(CLAMP)}$	-24	-21	-18	V	–	PRQ-665
Drain source diode voltage	$\|V_{DS(DIODE)}\|$	–	600	800	mV	T_J = 150°C	PRQ-249
Switching characteristics							
Switch-ON delay	$t_{ON(DELAY)}$	4	16	27	µs	From power stage control = "HIGH" to V_{OUTn} = 20% V_S Highest current limitation setting, R_{LOAD} = 180 Ω	PRQ-657
Switch-ON delay	$t_{ON(DELAY)}$	14	60	90	µs	From power stage control = "HIGH" to V_{OUTn} = 20% V_S Lowest current limitation setting, R_{LOAD} = 180 Ω	PRQ-954
Switch-OFF delay	$t_{OFF(DELAY)}$	4	13	20	µs	From power stage control = "LOW" to V_{OUTn} = 80% V_S R_{LOAD} = 180 Ω	PRQ-658
Switch-ON time	t_{ON}	6	25	40	µs	From power stage control = "HIGH" to V_{OUTn} = 80% $V_{S,}$ Highest current limitation setting, R_{LOAD} = 180 Ω	PRQ-659
Switch-ON time	t_{ON}	35	135	180	µs	From power stage control = "HIGH" to V_{OUTn} = 80% $V_{S,}$ Lowest current limitation setting, R_{LOAD} = 180 Ω	PRQ-888
Switch-OFF time	t_{OFF}	8	30	40	µs	From power stage control = "LOW" to V_{OUTn} = 20% V_S R_{LOAD} = 180 Ω	PRQ-660

(table continues...)

Table 11 (continued) Electrical characteristics power stage

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch-ON slew rate	$(dV/dt)_{ON}$	0.25	0.45	1.6	V/µs	V_S = 13.5 V, V_{OUTn} = 20% to 80% of V_S, setup acc. to AEC-Q100-012 (2006) Highest current limitation setting, R_{LOAD} = 180 Ω	PRQ-889
Switch-ON slew rate	$(dV/dt)_{ON}$	0.07	0.12	0.48	V/µs	V_S = 13.5 V, V_{OUTn} = 20% to 80% of V_S, setup acc. to AEC-Q100-012 (2006) Lowest current limitation setting, R_{LOAD} = 180 Ω	PRQ-662
Switch-OFF slew rate	$(dV/dt)_{OFF}$	-2.4	-0.55	-0.2	V/µs	V_S = 13.5 V, V_{OUTn} = 80% to 20% of V_S, setup acc. to AEC-Q100-012 (2006) R_{LOAD} = 180 Ω	PRQ-663
Switch-ON energy	E_{ON}	–	0.016	–	mJ	$V_S = V_{S(NOR),MAX}$, R_{LOAD} = 180 Ω	PRQ-260
Switch-OFF energy	E_{OFF}	–	0.034	–	mJ	$V_S = V_{S(NOR),MAX}$, R_{LOAD} = 180 Ω	PRQ-261
Capacitive load switching with overcurrent limitation and overtemperature protection							
Maximum time in CLS	t_{CLS1}	–	–	100	ms	–	PRQ-894
Maximum number of CLS activations	n_{CLS_ACT1}	–	–	50	kcycles	$t = t_{CLS1}$	PRQ-895
Power stage characteristics							
ON-state resistance at TJ = 25°C	$R_{DS(ON)\_25}$	–	133	–	mΩ	T_J = 25°C	PRQ-283
ON-state resistance at TJ = 150°C	$R_{DS(ON)\_150}$	–	–	230	mΩ	T_J = 150°C	PRQ-284
ON-state resistance in cranking at TJ = 150°C	$R_{DS(ON)\_CRANK\_150}$	–	–	230	mΩ	$V_S = V_{S(UV),MAX}$, T_J = 150°C	PRQ-285
ON-state resistance in inverse current at TJ = 25°C	$R_{DS(INV)\_25}$	–	133	–	mΩ	T_J = 25°C	PRQ-743

(table continues...)

Table 11 (continued) Electrical characteristics power stage

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ON-state resistance in inverse current at TJ = 150°C	$R_{DS(INV)\_150}$	–	–	230	mΩ	T_J = 150°C	PRQ-744
Nominal load current per channel (all channels active) at TA = 85°C	$I_{L(NOM)\_85}$	–	1	–	A	T_A = 85°C, $T_J \leq$ 150°C	PRQ-290
Inverse current per channel	$I_{L(INV)}$	–	$-I_{L(NOM)\_85}$	–	A	Power stage control = "HIGH", $V_S < V_{OUTn}$	PRQ-293
Output leakage current at TJ ≤ 85°C per channel	$I_{L(OFF)\_85}$	–	0.01	0.25	µA	Power stage control = "LOW", V_{OUTn} = 0 V, $T_J \leq$ 85°C	PRQ-788
Output leakage current at TJ = 150°C per channel	$I_{L(OFF)\_150}$	–	–	5	µA	Power stage control = "LOW", V_{OUTn} = 0 V, T_J = 150°C	PRQ-789

8 Device protection

The device is protected against overtemperature, overcurrent and overvoltage.

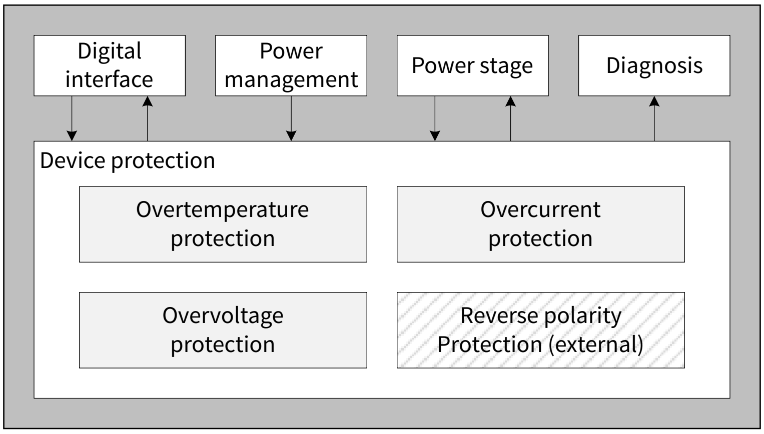


Figure 22 Device protection block diagram

Overtemperature and overcurrent protection are operational in all operation modes, except when in inactive mode.

Overvoltage protection is active in all operation modes.

Overtemperature and overcurrent protection during inverse current is inactive on the channel which is in inverse condition.

8.1 Overtemperature protection

The device incorporates both an absolute ($T_{J(ABS)}$) and a dynamic ($T_{J(DYN)}$) temperature protection circuitry for each channel.

An increase in junction temperature T_J above either one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated channel.

The power stage remains switched OFF until the junction temperature T_J fulfills the reactivation condition. Besides this, the restart strategy has to be considered as described in device protection restart strategy chapter.

Table 12 Overtemperature protection reactivation condition

Fault condition	Switch OFF event	Reactivation condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)

$T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

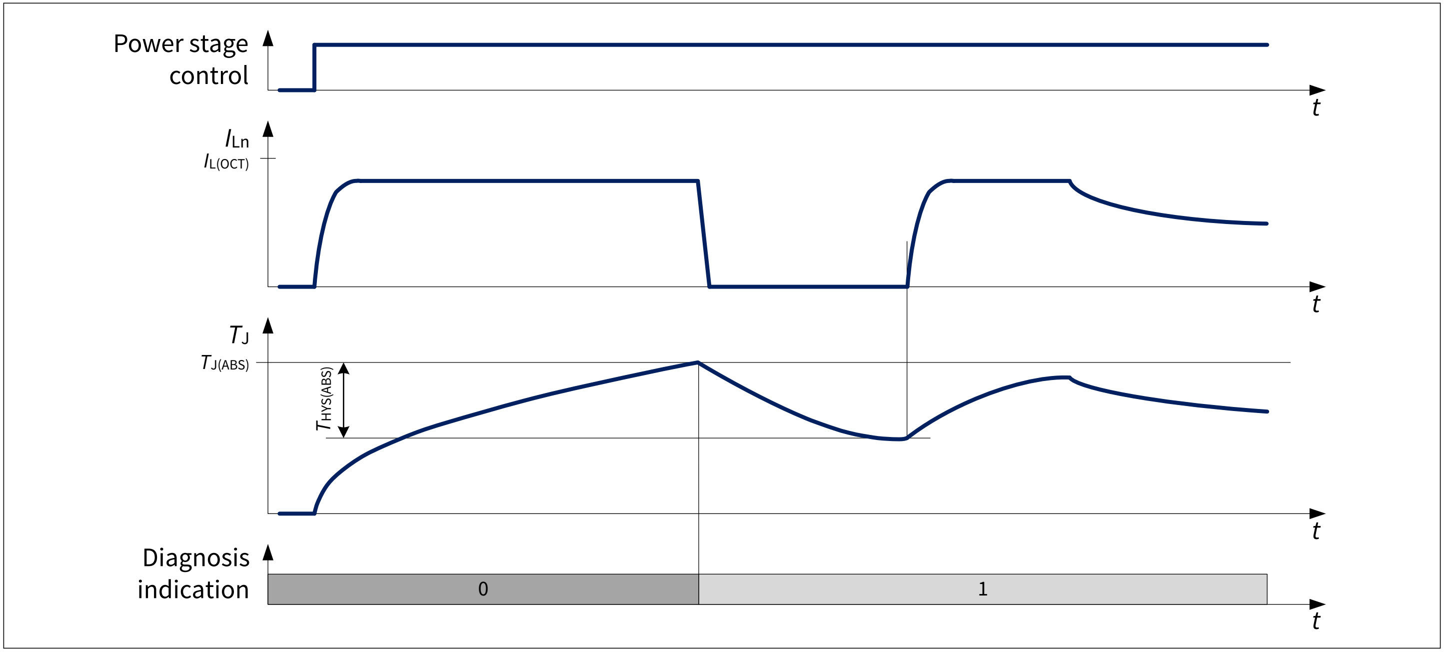


Figure 23 **Overtemperature protection (absolute) - unlimited restarts**

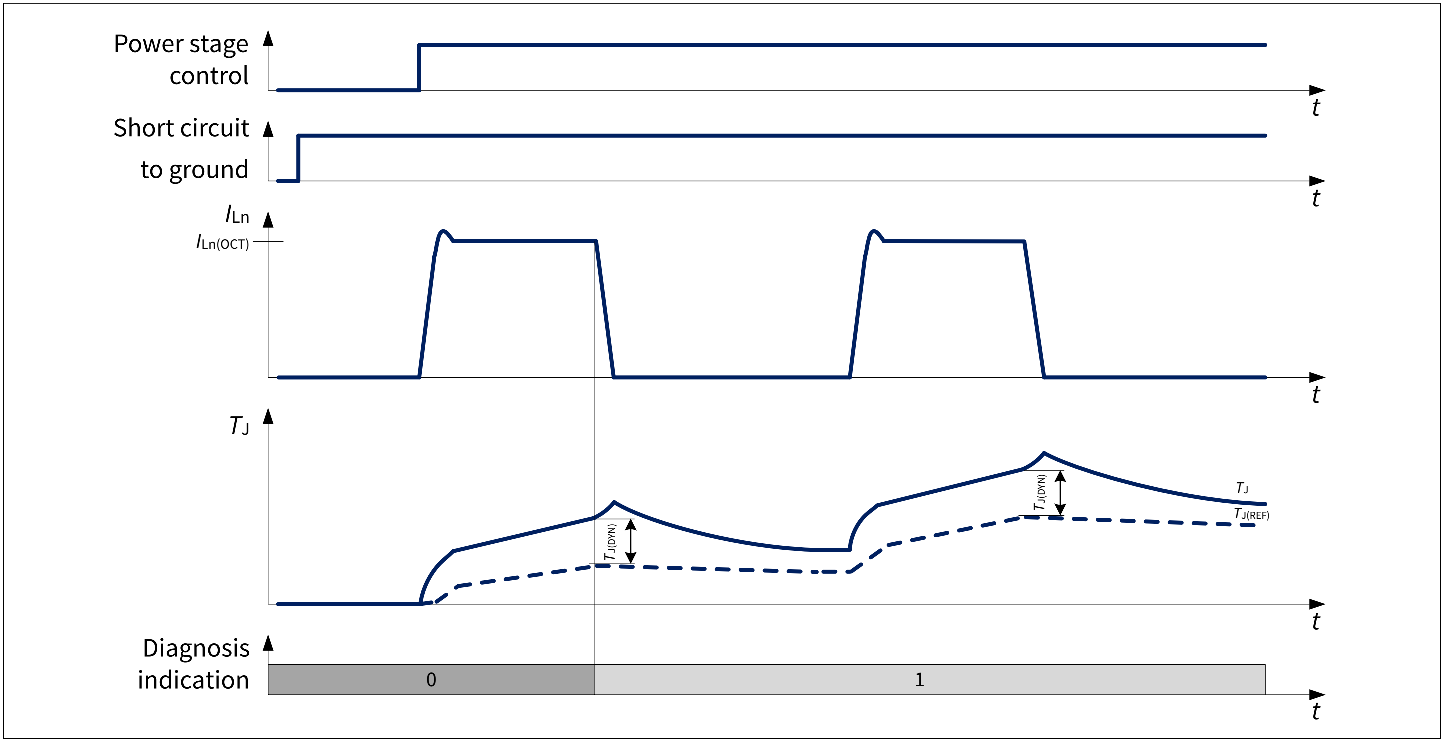


Figure 24 **Overtemperature protection (dynamic) - unlimited restarts**

8.2 Overcurrent protection

To protect the load as well as the power stage against an overload condition, the device offers an overcurrent limitation mechanism.

The device limits the load current to a configurable current $I_{L(OCT)}$.

The overcurrent limitation threshold $I_{L(OCT)}$ can be selected with 16 steps via the digital interface. The selection can be done for each channel individually.

The range for the selection is defined by the lowest and the highest configurable overcurrent limitation threshold $I_{L(LOCT)}$ and $I_{L(HOCT)}$.

For the selection of the overcurrent limitation threshold, the following equation can be considered:

$$I_{\mathrm{L(OCT)}} = I_{\mathrm{L(OCT\_LSB),\,TYP}} \cdot \mathrm{OCTn}_{\mathrm{decimal}} + I_{\mathrm{L(LOCT),\,TYP}} \tag{2}$$

In case of an SPI reset the minimum overcurrent limitation threshold $I_{L(LOCT)}$ is selected.

In case of limp home activation the maximum overcurrent limitation threshold $I_{L(HOCT)}$ is selected to provide maximum load driving capability.

The overcurrent limitation mechanism is active in case $V_{DS} \geq V_{DS(OC\_PROT)}$.

An activation of the overcurrent limitation mechanism is indicated via diagnosis.

8.3 Device protection restart strategy

The absolute overtemperature protection restart strategy can be configured to either single latch or unlimited restart via the digital interface.

The overheated channel performs automatic restart attempts until the host controller switches OFF the output channel.

If an overtemperature protection mechanism is triggered and the device protection restart strategy is configured to single latch, the protection latch is set and the power stage is latched OFF.

8.3.1 Latch reset options

- Using SPI command in one of the normal operation modes: by sending a clear latch command on the digital interface, the device resets the protection latch the affected power stages.
- Using the LHI pin: when the limp home mode is entered, the protection latch is cleared for all power stages.

8.4 Device protection and diagnosis in case of fault

An event that triggers a protection mechanism causes a report in the corresponding diagnosis registers.

The channel can be switched ON again if all the protection mechanisms fulfill the reactivation conditions.

8.4.1 Restart strategy

During fault condition, the device applies automatic restarts and either return to normal operation or it has to be switched OFF from the host controller.

To reset the power stage and its fault condition it is necessary to send a clear latch command over the digital interface.

The restart strategy is shown below.

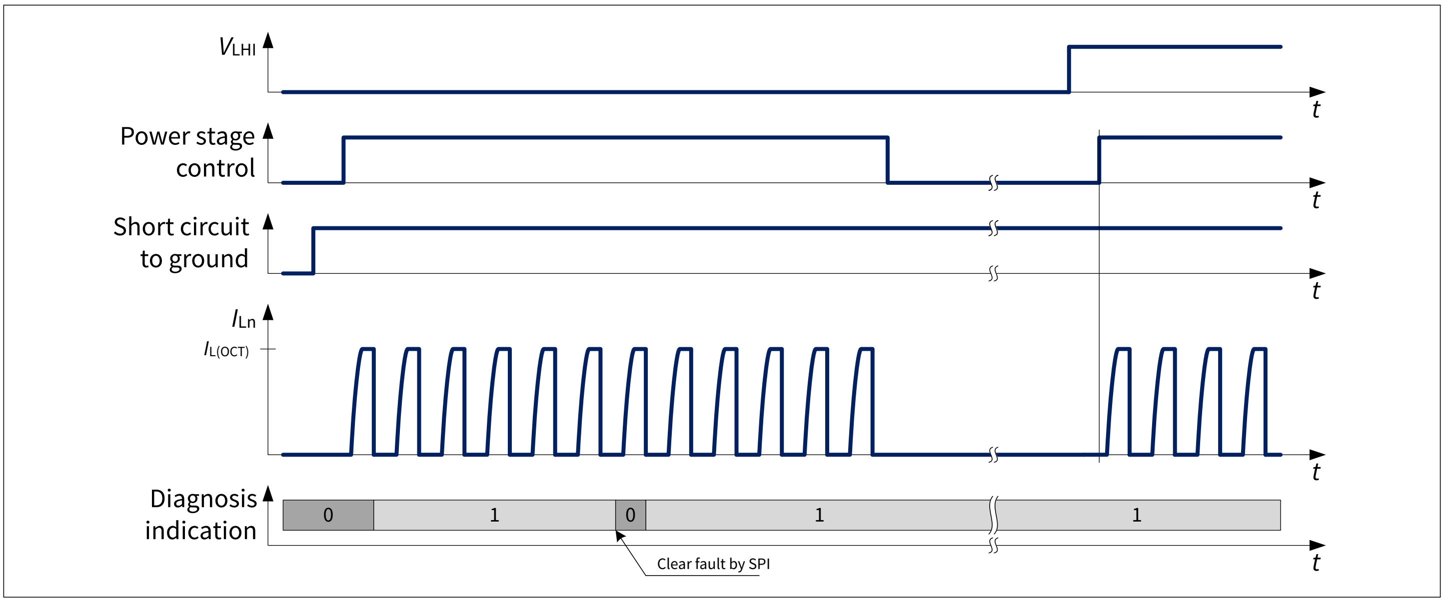


Figure 25 Restart strategy timing diagram

8.5 Additional protection

8.5.1 Reverse polarity protection

In reverse polarity condition (also known as reverse battery), power dissipation is caused by the intrinsic body diode of the DMOS channel. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the power stages has to be limited by the connected loads. The current through digital I/O and supply pins and ground pins has to be limited by an external resistor (please refer to the absolute maximum ratings and the application information).

8.5.2 Overvoltage protection

In case the power supply voltage is between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the power stage is still operational and follows the power stage control command.

In case the power supply voltage is above $V_{BAT(LD)}$ the device provides the following overvoltage protection mechanisms:

- $V_{S(CLAMP)}$ limits the voltage between VS and GND to protect the logic circuits
- $V_{DS(CLAMP)}$ limits the voltage between VS and OUTn to protect the output stage
- $V_{OUT(CLAMP)}$ limits the voltage between VOUTn and GND to protect the output stage

Below figure shows a concept drawing of the implementation. The clamping structure is available in all operation modes.

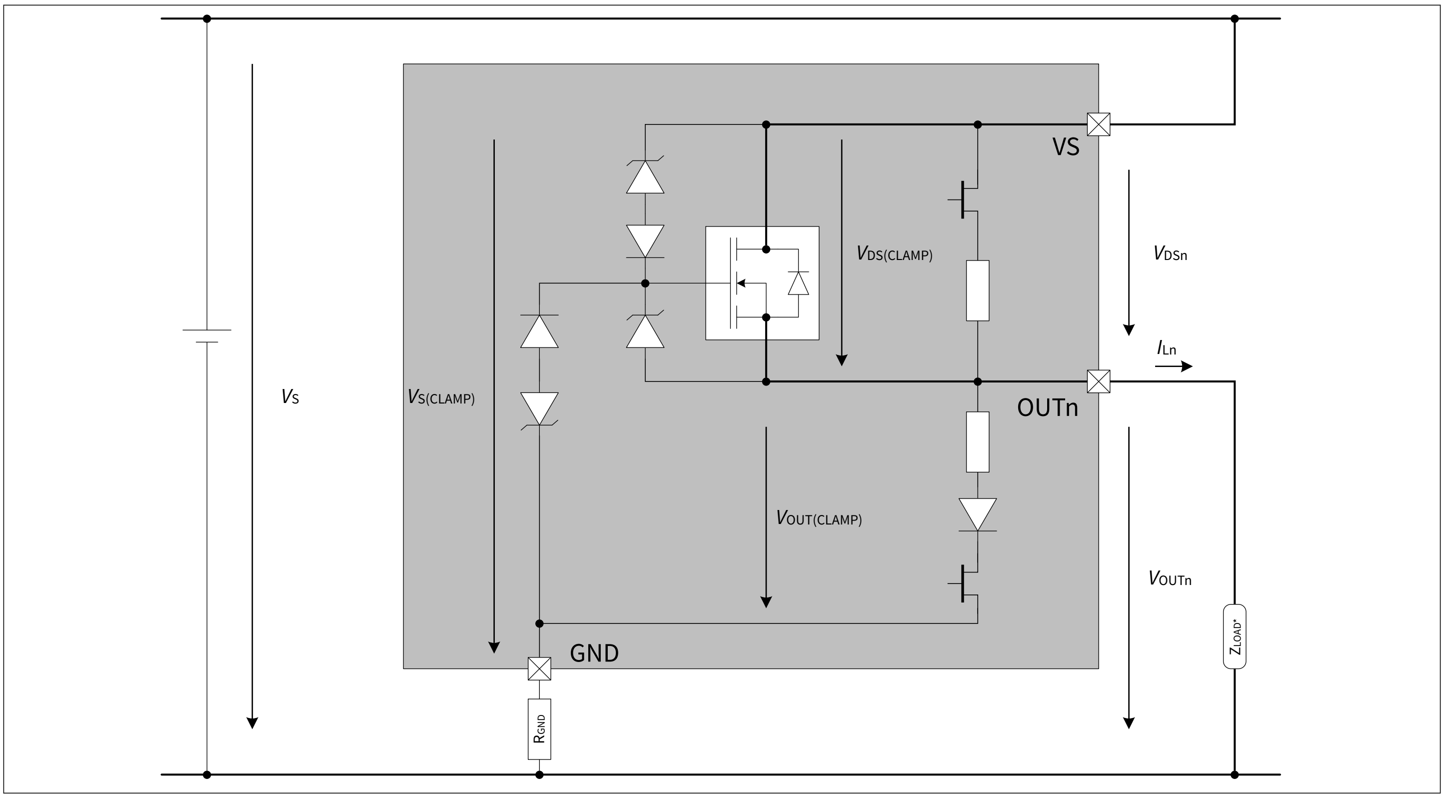


Figure 26 **Clamping concept**

8.5.3 Loss of battery and loss of load

The loss of connection to either the battery or to the load has no influence on the device robustness in case of purely resistive loads. In this case only the energy stored in the parasitic inductance of the wire harness needs to be handled. When driving an inductive load, the energy stored in the load and the wire harness has to be handled. In this case an external suppressor diode is recommended to handle the energy and to provide a well-defined path for the load current.

8.5.4 Loss of ground

In case the device is losing the connection to the ground potential the power stage can enter an undefined state. To avoid this undefined state:

The device switches OFF the power stage in case of loss of logic ground on module level

It is recommended to have a resistor connected between a digital input pin and the microcontroller, in order to ensure a deactivation of the power stage.

***Note**: In case a digital input pin is pulled to ground (either by a resistor or active), a parasitic ground path is available, which can keep the device operational during a loss of device ground.*

8.6 Electrical characteristics device protection

Table 13 Electrical characteristics device protection

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal							
Thermal shutdown temperature (absolute)	$T_{J(ABS)}$	180	190	200	°C	–	PRQ-333
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$	–	4	–	K	–	PRQ-334
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$	–	70	–	K	–	PRQ-335
Thermal shutdown hysteresis (dynamic)	$T_{HYS(DYN)}$	–	20	–	K	–	PRQ-336
Voltages							
Power supply clamping voltage	$V_{S(CLAMP)}$	42	45	52	V	–	PRQ-340
Overcurrent limitation threshold							
Lowest configurable overcurrent limitation	$I_{L(LOCT)}$	40	136	270	mA	–	PRQ-347
Lowest configurable overcurrent limitation	$I_{L(LOCT)}$	40	136	270	mA	After calibration	PRQ-348
Highest configurable overcurrent limitation	$I_{L(HOCT)}$	1.3	1.85	2.5	A	–	PRQ-354
Highest configurable overcurrent limitation	$I_{L(HOCT)}$	1.4	1.85	2.5	A	After calibration	PRQ-355
Configurable overcurrent limitation LSB value	$I_{L(OCT\_LSB)}$	65	115	205	mA	–	PRQ-720

9 Diagnosis

The device offers enhanced diagnosis features, which are realized by digital diagnosis information. The digital diagnosis is available via SPI in combination with the IRQ pin.

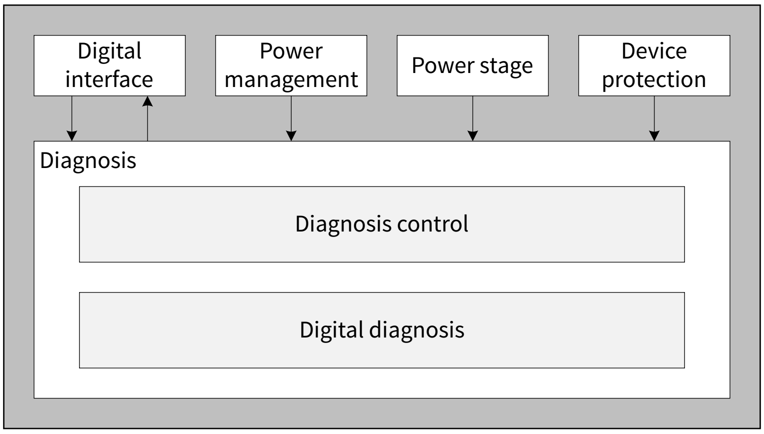


Figure 27 Diagnosis block diagram

9.1 Diagnosis control

The diagnosis control is responsible to coordinate which diagnosis is executed and reported, either digital via digital interface or via IRQ pin. Therefore, the device owns control registers to enable, disable and select the dedicated diagnosis features.

- With the power stage selection, the power stage and its corresponding multiplexer can be selected

9.2 Digital diagnosis

The digital diagnosis provides detailed information about the device status, separated into the following areas:

- Protection information
- Warning information
- Communication information
- Digital current sense
- Status reporting
- Self check information

9.2.1 Protection information

A protection bit is set, when at least one of the following protection mechanisms is triggered:

- Overtemperature protection
- Power stage warning
- Power supply undervoltage protection
- Power supply overvoltage protection

Protection information, except power stage warning, is stored in the protection diagnosis register until a clear latch command is performed by the host controller.

The power stage warning is a combination of the following device functions:

- Overcurrent limitation triggered $I_{L(OCT)}$
- Overcurrent wake up threshold triggered $I_{L(WU)}$
- Drain-source voltage for ON-state detection (by overcurrent limitation)
- Output voltage for ON-state detection
- Output voltage for OFF-state detection

The table below shows the relationship between the power stage warning information and the related diagnosis information.

Voltage monitoring	Power stage control	Power stage warning	Application condition
0	0	0	Normal operation - inactive
0	0	1	not applicable
0	1	0	Normal operation - active
0	1	1	Overcurrent limitation triggered
1	0	0	Normal operation - inactive
1	0	1	Short circuit to VS
1	1	0	Normal operation - active
1	1	1	Short circuit to ground
1	0	1	Open load in OFF-state - output pull-up resistor enabled

Additionally, the device provides a protection-based interrupt on the CAL / IRQ pin, by setting the pin to high impedance. The protection flags are clustered and can be linked to the CAL / IRQ pin via the digital interface as follows:

- Power supply overvoltage detection triggered $V_{S(OV)}$
- Power supply undervoltage shutdown triggered $V_{S(UV)}$
- Digital supply undervoltage shutdown triggered $V_{DD(UV)}$
- Power stage warning triggered
  - Drain-source voltage for ON-state detection
  - Output voltage for ON-state detection
  - Output voltage for OFF-state detection
  - Overcurrent limitation triggered $I_{L(OCT)}$
  - Overcurrent wake up threshold triggered $I_{L(WU)}$
- Temperature protection triggered
  - Absolute overtemperature protection
  - Dynamic overtemperature protection
- Modulo counter error triggered

The device provides the protection diagnosis information for each channel individually. First, the power stage select register has to be set to the proper channel, before reading.

A protection bit is set, when at least one of the following protection mechanisms for a channel is triggered:

- Absolute temperature protection
- Dynamic temperature protection
- Power stage warning

9.2.2 Warning information

The device offers several warning flags to inform the microcontroller about a potential issue in the application.

Warning flags for the following quantities are available:

- Overtemperature warning threshold
- Overcurrent wake up threshold
- Overcurrent limitation threshold

- ON-status reporting VHI
- OFF-status reporting VLO

Warning information is stored in the warning diagnosis register until a clear command is performed by the host controller.

The device is indicating a temperature warning threshold via digital interface in case the $T_J > T_{J(WRN)}$.

The device provides an indication in the power stage warning register and on the IRQ pin in case the load current exceeds a configured overcurrent wake up threshold $I_{L(WU)}$ and exits the low current consumption mode.

The overcurrent wake up threshold ($I_{L(WU)}$) is set in relation to the selected overcurrent limitation threshold (between $I_{L(LWU)}$ and $I_{L(HWU)}$).

$$I_{L(WU)} = \frac{I_{L(OCT)}}{10} \tag{3}$$

The overcurrent wake up function can be enabled via the digital interface in the normal operating modes.

The device indicates a warning information if the overcurrent limitation threshold is triggered. This is signaled at typically 75% of the selected overcurrent limitation threshold.

The device provides the warning diagnosis information for each channel individually. First, the power stage select register has to be set to the proper channel, before reading. Same information per channel can be read as in the global warning diagnosis register.

9.2.3 Communication information

The device offers several communication bits to inform the microcontroller about a potential issue in the communication path.

Communication bits for the following quantities are available:

- Modulo counter error
- Limp home input monitor
- Digital supply undervoltage
- Power ON reset

Communication information is stored in the communication diagnosis register until a clear command is performed by the host controller.

9.2.4 Digital current sense

The digital current sense is provided in the dedicated diagnosis register, in case the following conditions are fulfilled:

- The power stage is switched ON via the output control register
- The multiplexer is set to a power stage via the power stage select register
- The power stage in not in inverse condition
- No protection mechanism is active
- The power stage is not latched OFF

The device is capable to measure the load current up to $I_{L(HOCT)}$. This can be read via the digital interface.

To calculate the corresponding load current from the digital current sense, the following equation has to be used:

$$I_{\mathrm{Ln}} = I_{\mathrm{DCS(LSB)}} \cdot \mathrm{DCSn,}_{\mathrm{decimal}} \tag{4}$$

The device features an 8 bit ADC for load current measurement.

***Note**:* *After digital current sense activation, a valid readout will be available after 20 µs.*

9.2.5 Status reporting

The device offers the possibility to read the following status information via the digital interface:

- ON-state status
- OFF-state status

The power stage status is evaluated by the device and results in the following two status reports:

- The ON-state status reporting indicates that the power stage is switched ON, in case $V_{OUT} > V_{OUT(ON)}$. The result of the comparison can be read via the digital interface.
- The ON-state status reporting indicates that the power stage is switched ON, in case $V_{OUTn} > V_{OUT(ON)}$. The result of the comparison can be read via the digital interface.
- The OFF-state status reporting indicates that the power stage is switched OFF, in case $V_{OUTn} \leq V_{OUT(OFF)}$. The result of the comparison can be read via the digital interface.

9.2.6 Self check information

The device offers the possibility to perform dedicated self checks, which can be activated via digital interface.

The ON-to-OFF switchability check can be performed while the device is in active mode. The host controller can command the power stage to switch OFF. In case $V_{OUTn} < V_{OUT(ON)}$ a status will be indicated via the digital interface for the selected channel. After reading the status the host controller can switch ON the power stage again.

9.2.7 Open load in OFF-state

The device features an open load detection capability in OFF-state (OUTn set 0_B). This function involves the voltage monitor and the output pull-up resistor for the selected power stage to be enabled. Enable these by setting the DCR0.VMON to 1_B and the ICL_TRM.OCT_TRM to 0001_B, respectively. With these settings, if the V_{DS} comparator check results in WDIAGn.VHIn being LOW, it indicates an open load condition, which is then reported at PROTDIAGn.PSWn, set to 1_B. Additionally, the fault is indicated on the IRQ pin.

***Note**: A valid register readout is available once the output is polarized. The required time depends on the variation of the pull-up current and the effective capacitance present at the output.*

9.3 Electrical characteristics diagnosis

Table 14 Electrical characteristics diagnosis

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage for OFF-state detection	$V_{OUT(OFF)}$	1.6	2	2.4	V	–	PRQ-722
Output voltage for ON-state detection	$V_{OUT(ON)}$	V_S - 1.6	V_S - 2	V_S - 2.4	V	–	PRQ-830
Output pull-down resistor for OFF state diagnosis	$R_{OUT(PD)}$	45	59	90	kΩ	OUTx = OFF and current limitation of OUTx set to 0x0 Diode placed in series to output pull-down resistor, see Figure 26	PRQ-952

(table continues...)

Table 14 (continued) Electrical characteristics diagnosis

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output pull-up resistor for OFF state diagnosis	$R_{OUT(PU)}$	80	100	350	kΩ	OUTx = OFF and current limitation of OUTx set to 0x1	PRQ-953
Temperature warning threshold	$T_{J(WRN)}$	150	160	170	°C	–	PRQ-723
Digital current sense range	$I_{DCS(RANGE)}$	0	–	$I_{L(HOCT)}$	A	–	PRQ-748
Digital current sense LSB value	$I_{DCS(LSB)}$	–	7.4	–	mA	–	PRQ-683
Accuracy of digital current sense #05	ACC_{DCS05}	-8.5	–	+8.5	LSB	100mA ≤ I_{Ln} < $I_{L(OCT)}$	PRQ-760
Accuracy of digital current sense #05	ACC_{DCS05}	-8.3	–	+8	LSB	100mA ≤ I_{Ln} < $I_{L(OCT)}$, After calibration	PRQ-761
Accuracy of digital current sense #08	ACC_{DCS08}	-26	–	+28	%	250mA ≤ I_{Ln} < $I_{L(OCT)}$	PRQ-766
Accuracy of digital current sense #08	ACC_{DCS08}	-24	–	+23	%	250mA ≤ I_{Ln} < $I_{L(OCT)}$, After calibration	PRQ-767
Accuracy of digital current sense #11	ACC_{DCS11}	-11	–	+13.5	%	1A ≤ I_{Ln} < $I_{L(OCT)}$	PRQ-772
Accuracy of digital current sense #11	ACC_{DCS11}	-7.5	–	+7.5	%	1A ≤ I_{Ln} < $I_{L(OCT)}$, After calibration	PRQ-773
Accuracy of digital current sense #12	ACC_{DCS12}	-10	–	+12	%	1.5 A ≤ I_{Ln} < $I_{L(OCT)}$	PRQ-776
Accuracy of digital current sense #12	ACC_{DCS13}	-6	–	+6	%	1.5A ≤ I_{Ln} < $I_{L(OCT)}$, After calibration	PRQ-777
Lowest configurable overcurrent wake up threshold	$I_{L(LWU)}$	8.5	44.5	91.5	mA	$I_{L(OCT)}$ set to 3 * $I_{L(LOCT)}$	PRQ-936
Lowest configurable overcurrent wake up threshold	$I_{L(LWU)}$	10	51	90	mA	$I_{L(OCT)}$ set to 3 * $I_{L(LOCT)}$, After calibration	PRQ-940
Highest configurable overcurrent wake up threshold	$I_{L(HWU)}$	107	162	258	mA	$I_{L(OCT)}$ set to $I_{L(HOCT)}$	PRQ-938
Highest configurable overcurrent wake up threshold	$I_{L(HWU)}$	115	183	250	mA	$I_{L(OCT)}$ set to $I_{L(HOCT)}$, After calibration	PRQ-942

10 Digital interface

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four signal lines: SO, SI, SCLK and CSN. While on the SI and SO the data is transferred at the data rate set by SCLK, the signal on CSN defines if the device is listening to the communication.

The falling edge of CSN indicates the beginning of an access frame. Data is sampled-in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access frame is terminated on a rising edge of CSN.

A modulo 8 counter ensures that a command is accepted only when a multiple of 8 bit has been transferred, with a minimum of 8 bits.

Starting from the most significant bit (MSB), these 8 bits consist of 4 bit address, and 4 bit data as shown in belows figure.

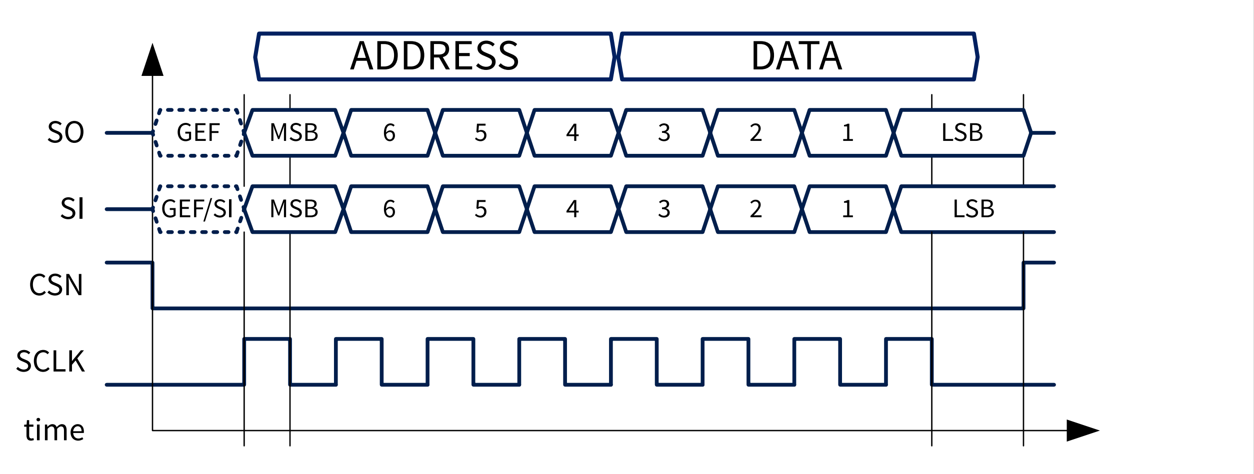


Figure 28 **Serial peripheral interface**

10.1 SPI signal description

CSN - Chip Select Negated

The system microcontroller selects the device by means of the CSN pin. Whenever the pin is in a “LOW” state, data can be transmitted. When CSN is in a “HIGH” state, any signal at the SCLK and SI pins are ignored and the SO pin is driven to a “high impedance” state.

- **CSN “HIGH” to “LOW” transition**
  - The previously requested information is transferred into the shift register.
  - The SO pin changes from a “high impedance” state to a “LOW” state.
- **CSN “LOW” to “HIGH” transition**
  - Command decoding is only done when, after the falling edge of CSN, an exact multiple (1, 2, 3, …) of 8 SCLK signals have been detected.
  - Data from the shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. It is essential that the SCLK pin is in a “LOW” state whenever the chip select CSN makes any transition, otherwise, the command may not be accepted.

SI - Serial Input

Serial input data bits are shifted in at this pin, the most significant bit first. The information at the SI pin is read on the falling edge of SCLK.

SO - Serial Output

During transmission, the response data is serially shifted out at this pin, with the most significant bit first. The SO pin is in high impedance until the CSN pin goes to “LOW”. New data will be shifted out at the SO pin at every rising edge of the SCLK.

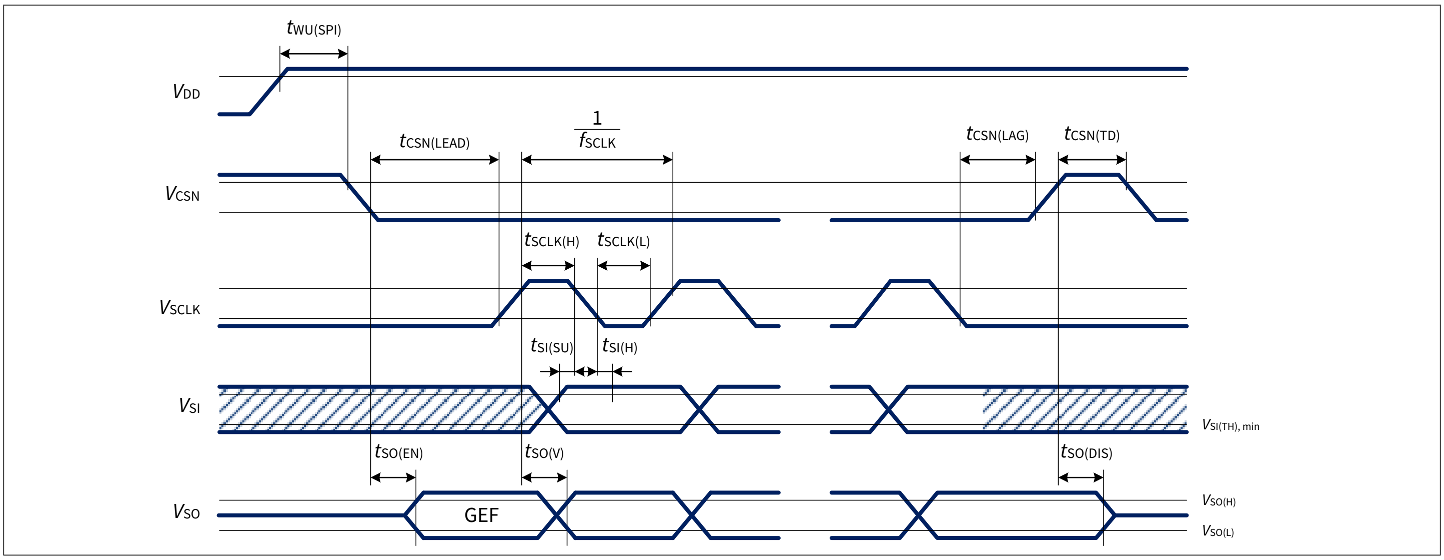


Figure 29 Timing diagram SPI access

10.1.1 SPI protocol

The global error flag (GEF) bit is reported on SO between the CSN falling edge and the first SCLK rising edge.

With the global error flag, the device can provide quick diagnosis feedback without any SPI clock pulse. All status information are logically OR combined and reported by the global error flag. Visualized in the figure below.

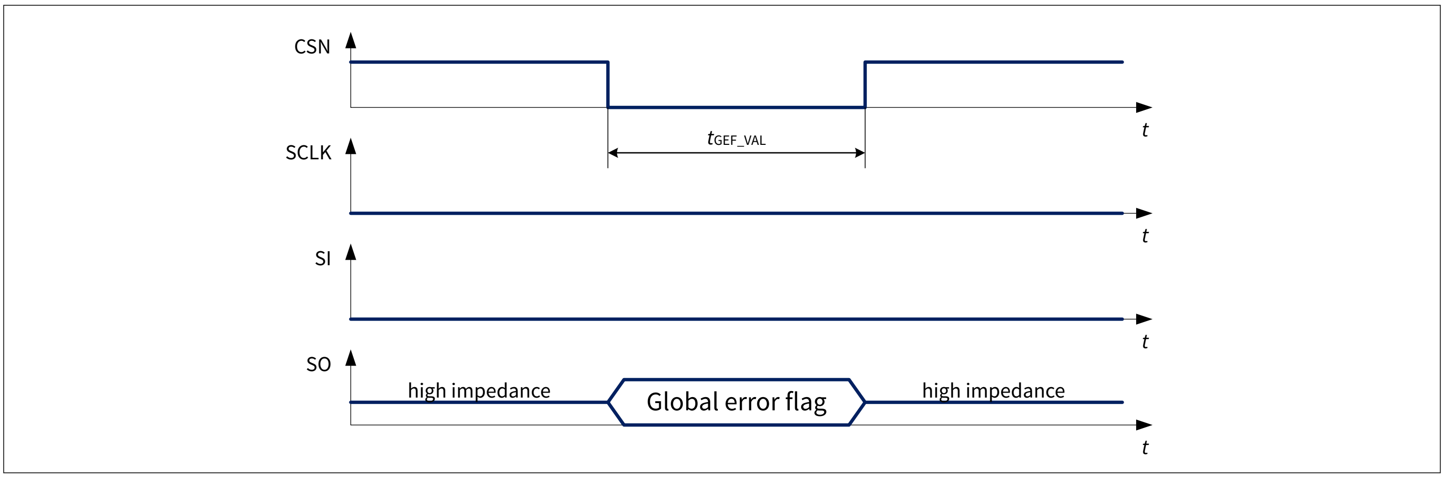


Figure 30 Global error flag - diagnosis without clock cycle

The following status information are or combined into the global error flag:

- Power supply overvoltage detection triggered $V_{S(OV)}$
- Power supply undervoltage shutdown triggered $V_{S(UV)}$
- Digital supply undervoltage shutdown triggered $V_{DD(UV)}$
- Power stage warning triggered
- Temperature protection triggered
  - Absolute overtemperature protection
  - Dynamic overtemperature protection
- Modulo counter error triggered

The relationship between SI and SO content during SPI communication is shown in the figure below. SI line represents the frame sent from the µC and the SO line is the answer provided by the device. The “previous response” means that the frame sent back depends on the command frame received before frame A.

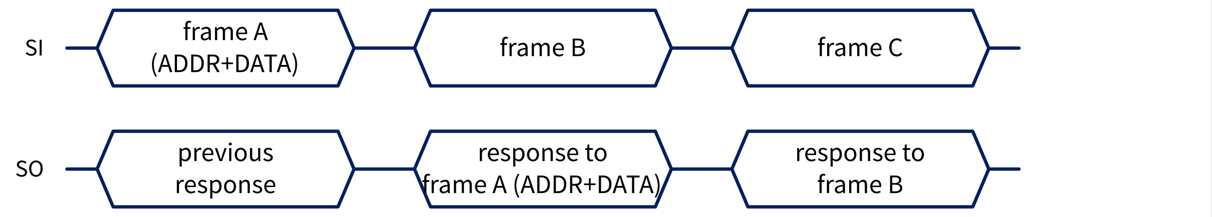


Figure 31 **Relationship between SI and SO during SPI communication**

In below situations the content of the frame sent back to the µC does not depend on the previously received frame:

- When the digital supply voltage leaves the undervoltage reset condition, as shown in the figure below.
- In case a communication error happened during the previously sent read or write command (for instance, the clock pulses were not multiple of 8), the device indicates it via the digital interface.

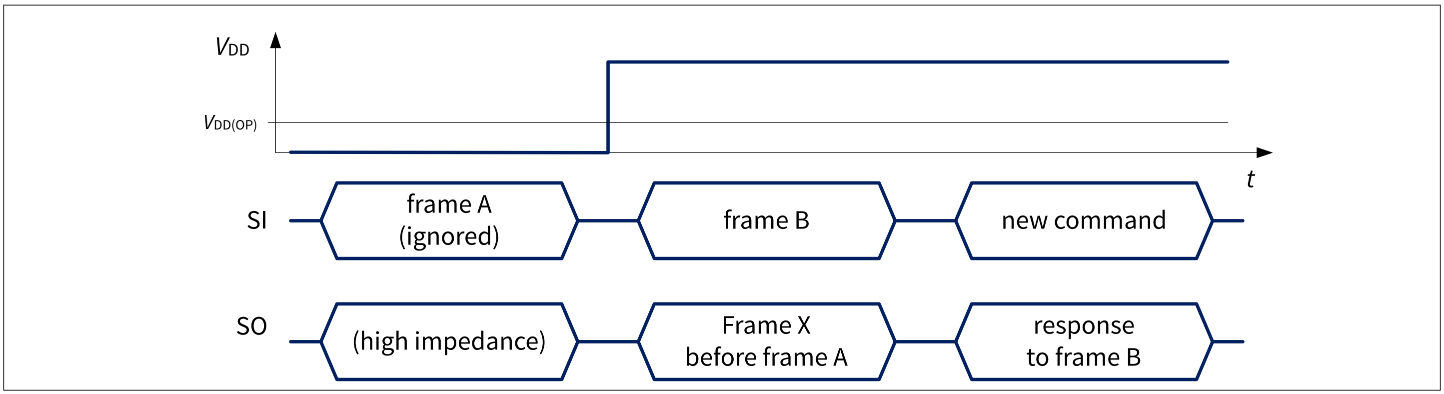


Figure 32 **SPI response after leaving undervoltage at VDD pin**

10.2 SPI register set to default conditions

The below described conditions have an impact on the SPI register content:

When the limp home mode is entered:

- Configuration and control registers will be either
  - reset to their default values (except current limitation) (default behavior)
  - kept at last state if configured accordingly via the digital interface
- Error, protection and warning flags will be reset

When a power on reset command is received via the digital interface:

- Register content will be reset to the default values

10.3 Daisy chain capability

The interface provides daisy chain capability with modulo 8 bit SPI devices.

In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device see belows figure, in order to build a chain. The two ends of the chain are connected to the output and input of the master device, MOSI and MISO respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

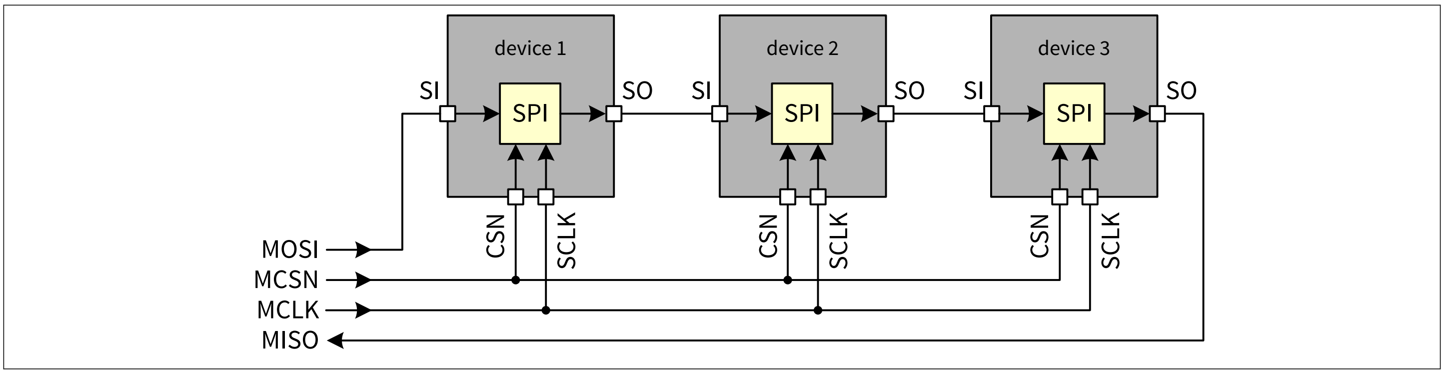


Figure 33 **Daisy chain configuration**

In the SPI block of each device, there is one shift register where each bit from the SI line is shifted in every SCLK cycle. The bit is shifted out on the SO pin. After 8 SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line must turn “HIGH” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in at device 2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCSN line must turn “HIGH”, see belows figure.

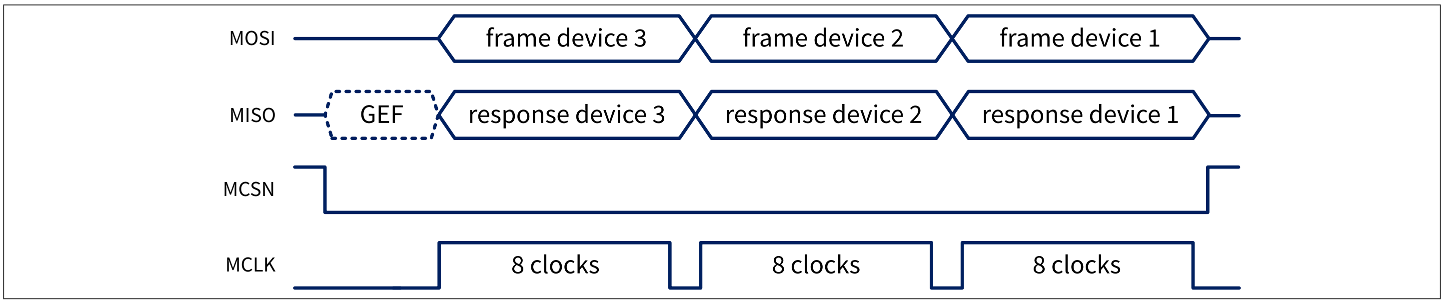


Figure 34 **Data transfer in daisy chain configuration**

A logic OR combination of the global error flags (GEF) of all the devices in the daisy chain is integrated at the beginning of the SPI frame, between the CS rising edge and the first SCLK rising edge.

10.4 SPI register description

10.4.1 Register address overview

The table below provides an overview of the available diagnosis and configuration registers including their address. Write-registers are configured by sending the corresponding address together with the data bits. For detailed information on the data bits, refer to the dedicated register description.

Table 15 **Register overview**

Name	Type	Address	Description
RC	r	0_H	Read command
PROTDIAG	r or r/wclr	1_H	Protection diagnosis
WDIAG	r/wclr	2_H	Warning diagnosis
COMDIAG	r/wclr	3_H	Communication diagnosis
PROTDIAGn	r	4_H	Protection diagnosis per channel

(table continues...)

Table 15 (continued) Register overview

Name	Type	Address	Description
WDIAGn	r	5_H	Warning diagnosis per channel
DCSR_MSBn	r	6_H	Digital current sense register 4bit MSB per channel
DCSR_LSBn	r	7_H	Digital current sense register 4bit LSB per channel
DCR0	r/w	8_H	Device control register 0
OCR0	r/w	9_H	Output control register 0
OCR1	r/w	A_H	Output control register 1
PS_SEL	r/w	B_H	Power stage select register
ICL_TRM	r/w	C_H	Selectable current limitation threshold per channel / trim code
DCR1	r/w	D_H	Device control register 1
DCR2	r/w	E_H	Device control register 2

10.4.2 SPI register description

10.4.2.1 Read command

Name	Address	D3	D2	D1	D0	Default
RC	0_H	A3	A2	A1	A0	0_H

10.4.2.2 Protection diagnosis

Name	Address	D3	D2	D1	D0	Default
PROTDIAG	1_H	VSOV	VSUV	PSW	OT_PROT	0_H

Table 16 **Protection diagnosis bit descriptions**

Field	Bits	Type	Description
VSOV	3	r/wclr	**VS overvoltage detection** 0_B (default) No VS overvoltage detected 1_B VS overvoltage detected
VSUV	2	r/wclr	**VS undervoltage detection** 0_B (default) No VS undervoltage detected 1_B VS undervoltage detected
PSW	1	r	**Power stage warning** 0_B (default) No power stage warning indication triggered 1_B Power stage warning indication triggered for at least one output
OT_PROT	0	r/wclr	**Temperature shutdown** 0_B (default) No temperature protection triggered ($T_{J(ABS)}$ or $T_{J(DYN)}$) 1_B Temperature protection triggered ($T_{J(ABS)}$ or $T_{J(DYN)}$)

10.4.2.3 Warning diagnosis

Name	Address	D3	D2	D1	D0	Default
WDIAG	2_H	VHI	VLO	OC_PROT / OC_WU	OTW	0_H

Table 17 **Warning diagnosis bit descriptions**

Field	Bits	Type	Description
VHI	3	r/wclr	**Status of V_{DS} comparator** 0_B (default) $V_{OUT} > V_{OUT(ON)}$ 1_B $V_{OUT} \leq V_{OUT(ON)}$
VLO	2	r/wclr	**Status of V_{OUT} comparator** 0_B (default) $V_{OUT} > V_{OUT(OFF)}$ 1_B $V_{OUT} \leq V_{OUT(OFF)}$
OC_PROT / OC_WU	1	r/wclr	**Current limitation threshold protection indication** 0_B (default) No current limitation triggered and overcurrent wake up threshold reached 1_B current limitation triggered ($I_L > I_{L(OCT)}$) (in case OCR1.OCWUEN = 0_B) 1_B current limitation triggered ($I_L > I_{L(OCT)}$) or overcurrent wake up threshold reached ($I_L > I_{L(WU)}$) (in case OCR1.OCWUEN = 1_B)
OTW	0	r/wclr	**Temperature warning** 0_B (default) No temperature warning triggered 1_B Temperature warning triggered

10.4.2.4 Communication diagnosis

Name	Address	D3	D2	D1	D0	Default
COMDIAG	3_H	POR	VDDUV	LHI	CER	8_H

Table 18 **Communication diagnosis bit descriptions**

Field	Bits	Type	Description
POR	3	r/wclr	**Power ON reset indication** 0_B No power ON reset occurred 1_B (default) Power ON reset (POR) occurred
VDDUV	2	r/wclr	**VDD undervoltage detection** 0_B (default) No VDD undervoltage detected 1_B VDD undervoltage detected
LHI	1	r/wclr	**Limp home input pin monitor** 0_B (default) no HIGH signal on LHI pin detected 1_B HIGH signal on LHI pin detected
CER	0	r/wclr	**Communication error** 0_B (default) Previous transmission was successful (module 8 clocks received) 1_B Previous transmission failed

10.4.2.5 Protection diagnosis per channel

Name	Address	D3	D2	D1	D0	Default
PROTDIAGn	4_H	res	PSWn	DT_PROTn	OT_PROTn	0_H

Table 19 Error diagnosis bit descriptions

Field	Bits	Type	Description
res	3	r	**reserved** should be written with 0_B
PSWn	2	r	**Power stage warning** 0_B (default) No power stage warning indication triggered for selected power stage 1_B Power stage warning indication triggered for selected power stage if • OC_PROTn = 1_B AND OUTn = 1_B if DCR0.VMON = 0_B • VHIn = 0_B & OUTn = 0_B OR VLO = 1B & OUTn = 1_B if DCR0.VMON = 1_B
DT_PROTn	1	r	**Dynamic overtemperature protection** 0_B (default) No dT protection triggered for selected power stage 1_B dT protection triggered for selected power stage
OT_PROTn	0	r	**Absolute overtemperature protection** 0_B (default) No OT protection triggered for selected power stage 1_B OT protection triggered for selected power stage

10.4.2.6 Warning diagnosis per channel

Name	Address	D3	D2	D1	D0	Default
WDIAGn	5_H	VHIn	VLOn	OC_PROTn / OC_WUn	OTWn	0_H

Table 20 Warning diagnosis bit descriptions

Field	Bits	Type	Description
VHIn	3	r	**Status of V_{DS} comparator of selected power stage** 0_B $V_{OUT} > V_{OUT(ON)}$ 1_B (default) $V_{OUT} \leq V_{OUT(ON)}$
VLOn	2	r	**Status of V_{OUT} comparator of selected power stage** 0_B (default) $V_{OUT} > V_{OUT(OFF)}$ 1_B $V_{OUT} \leq V_{OUT(OFF)}$

(table continues...)

Table 20 (continued) Warning diagnosis bit descriptions

Field	Bits	Type	Description
OC_PROTn	1	r	**Current limitation threshold protection indication of selected power stage** 0_B (default) No current limitation triggered and overcurrent wake up threshold reached 1_B current limitation triggered ($I_L > I_{L(OCT)}$) (in case the bit OCR1.OCWUEN is set to 0_B) 1_B current limitation triggered ($I_L > I_{L(OCT)}$) or overcurrent wake up threshold reached ($I_L > I_{L(WU)}$) (in case OCR1.OCWUEN = 1_B) For the BTS81000-SSGI-6ET, the overcurrent limitation indication is not available for OCT_TRM settings 0_H - 3_H. The overcurrent protection is functional at all settings.
OTWn	0	r	**Temperature warning** 0_B (default) No temperature warning threshold triggered on selected power stage 1_B Temperature warning threshold triggered on selected power stage

10.4.2.7 Digital current sense register 4 bit MSB per channel

Name	Address	D3	D2	D1	D0	Default
DCSR_MSBn	6_H	DCS7	DCS6	DCS5	DCS4	0_H

Table 21 Digital current sense MSB register descriptions

Field	Bits	Type	Description
DCS	3:0	r	**Digital current sense register 4 most significant bits (MSBs) of 8 bit digital current sense value** triggers current measurement and returns digital current sense 4 most significant bits after $t_{CSN(TD\_DCS)}$ when another register read command is received.

10.4.2.8 Digital current sense register 4 bit LSB per channel

Name	Address	D3	D2	D1	D0	Default
DCSR_LSBn	7_H	DCS3	DCS2	DCS1	DCS0	0_H

Table 22 Digital current sense LSB register descriptions

Field	Bits	Type	Description
DCS	3:0	r	**Digital current sense register 4 least significant bits (LSBs) of 8 bit digital current sense value** returns 4 least significant bits

10.4.2.9 Device control register 0

Name	Address	D3	D2	D1	D0	Default
DCR0	8_H	VMON	CAL	ADC	FPOR	0_H

Table 23 **Device control register 0 bit descriptions**

Field	Bits	Type	Description
VMON	3	r/w	**Voltage monitor enable** 0_B (default) Voltage monitor disabled 1_B Voltage monitor enabled
CAL	2	r/w	**Calibration mode enable** 0_B (default) Calibration disabled 1_B Calibration enabled
ADC	1	r/w	**Digital current sense enable** 0_B (default) Digital current sense disabled 1_B Digital current sense enabled
FPOR	0	r/w	**Force power ON reset** Write 1_B to force power ON reset when all outputs, VMON and current sense are OFF.

10.4.2.10 Output control register 0

Name	Address	D3	D2	D1	D0	Default
OCR0	9_H	OUT3	OUT2	OUT1	OUT0	0_H

Table 24 **Output control register 0 bit descriptions**

Field	Bits	Type	Description
OUT3	3	r/w	**Output control power stage OUT3** 0_B (default) power stage OUT3 OFF 1_B power stage OUT3 ON
OUT2	2	r/w	**Output control power stage OUT2** 0_B (default) power stage OUT2 OFF 1_B power stage OUT2 ON
OUT1	1	r/w	**Output control power stage OUT1** 0_B (default) power stage OUT1 OFF 1_B power stage OUT1 ON

(table continues...)

Table 24 **(continued) Output control register 0 bit descriptions**

Field	Bits	Type	Description
OUT0	0	r/w	**Output control power stage OUT0** 0_B (default) power stage OUT0 OFF 1_B power stage OUT0 ON

10.4.2.11 Output control register 1

Name	Address	D3	D2	D1	D0	Default
OCR1	A_H	res	OCWUEN	OUT5	OUT4	0_H

Table 25 **Output control register 1 bit descriptions**

Field	Bits	Type	Description
res	3	r/w	**reserved** should be written with 0
OCWUEN	2	r/w	**Overcurrent wake up threshold function** 0_B (default) overcurrent wake up threshold function disabled 1_B overcurrent wake up threshold function and notification via wake up signal on IRQ pin enabled
OUT5	1	r/w	**Output control power stage OUT5** 0_B (default) power stage OUT5 OFF 1_B power stage OUT5 ON
OUT4	0	r/w	**Output control power stage OUT4** 0_B (default) power stage OUT4 OFF 1_B power stage OUT4 ON

10.4.2.12 Power stage select

Name	Address	D3	D2	D1	D0	Default
PS_SEL	B_H	res	S2	S1	S0	7_H

Table 26 **Power stage select register bit descriptions**

Field	Bits	Type	Description
res	3	r/w	**reserved** should be written with 0

(table continues...)

Table 26 (continued) Power stage select register bit descriptions

Field	Bits	Type	Description
S	2:0	r/w	**Power stage select** 000_B power stage OUT0 selected 001_B power stage OUT1 selected 010_B power stage OUT2 selected 011_B power stage OUT3 selected 100_B power stage OUT4 selected 101_B power stage OUT5 selected 110_B calibration bits 0-3 selected $_{111B}$ calibration bits 4-7 selected

10.4.2.13 Selectable current limitation threshold per channel and calibration code

Name	Address	D3	D2	D1	D0	Default
ICL_TRM	C_H	OCT3_TRM3	OCT2_TRM2	OCT1_TRM1	OCT0_TRM0	0_H

Table 27

Field	Bits	Type	Description
OCT_TRM	3:0	r/w	**Overcurrent limitation threshold selection for selected power stage** Select power stage using PS_SEL and select current limitation threshold $I_{L(OCT)} = I_{L(LOCT)} + I_{L(OCT\_LSB)}$ * ICL_TRM.OCT_TRM **Output pull-down resistor enable for for selected power stage in OFF state** 0000_B and selected power stage control = LOW: output pull-down resistor $R_{OUT(PD)}$ enabled (disabled for all other settings of OCT_TRM) **Output pull-up resistor enable for for selected power stage in OFF state** 0001_B and selected power stage control = LOW: output pull-up resistor $R_{OUT(PU)}$ enabled (disabled for all other settings of OCT_TRM) **Calibration register (when PS_SEL.S = 6_H or 7_H)** PS_SEL.S = 6_H Calibration bits 0-3 can be written PS_SEL.S = 7_H Calibration bits 4-7 can be written

10.4.2.14 Device control register 1

Name	Address	D3	D2	D1	D0	Default
DCR1	D_H	OTRD3	OTRD2	OTRD1	OTRD0	0_H

Table 28 Error diagnosis bit descriptions

Field	Bits	Type	Description
OTRD3	3	r/w	**Absolute overtemperature protection restart disable OUT3** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior
OTRD2	2	r/w	**Absolute overtemperature protection restart disable OUT2** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior
OTRD1	1	r/w	**Absolute overtemperature protection restart disable OUT1** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior
OTRD0	0	r/w	**Absolute overtemperature protection restart disable OUT0** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior

10.4.2.15 Device control register 2

Name	Address	D3	D2	D1	D0	Default
DCR2	E_H	res	LHCFG	OTRD5	OTRD4	0_H

Table 29 Error diagnosis bit descriptions

Field	Bits	Type	Description
res	3	r/w	**reserved** should be written with 0
LHCFG	2	r/w	**Limp home reset configuration** 0_B (default) Registers reset to default values during limp home 1_B Registers not reset to default values during limp home
OTRD5	1	r/w	**Absolute overtemperature protection restart disable OUT5** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior

(table continues...)

Table 29 (continued) Error diagnosis bit descriptions

Field	Bits	Type	Description
OTRD4	0	r/w	**Absolute overtemperature protection restart disable OUT4** 0_B (default) overtemperature protection set to automatic restart 1_B overtemperature protection set to latched behavior

10.5 Electrical characteristics digital interface

Table 30 Electrical characteristics digital interface

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI signal timings							
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(LEAD)}$	200	–	–	ns	–	PRQ-641
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(LAG)}$	200	–	–	ns	–	PRQ-642
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(TD)}$	500	–	–	ns	–	PRQ-643
Transfer delay time in case of digital current sense readout (rising CSN to falling CSN)	$t_{CSN(TD\_DCS)}$	5	–	–	µs	–	PRQ-873
Output enable time (falling CSN to SO valid)	$t_{SO(EN)}$	–	30	100	ns	$C_{L(SO)}$ = 50 pF	PRQ-644
Output disable time (rising CSN to SO tristate)	$t_{SO(DIS)}$	–	30	100	ns	$C_{L(SO)}$ = 50 pF	PRQ-645
Serial clock frequency	f_{SCLK}	0	–	5	MHz	–	PRQ-646
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	–	PRQ-647
Serial clock "HIGH" time	$t_{SCLK(H)}$	90	–	–	ns	–	PRQ-648
Serial clock “LOW” time	$t_{SCLK(L)}$	90	–	–	ns	–	PRQ-649
Data setup time (required time SI to falling SCLK)	$t_{SI(SU)}$	20	–	–	ns	–	PRQ-650
Data hold time (falling SCLK to SI)	$t_{SI(H)}$	20	–	–	ns	–	PRQ-651
Output data valid time with capacitive load	$t_{SO(V)}$	–	–	60	ns	$C_{L(SO)}$ = 50 pF	PRQ-652

(table continues...)

Table 30 (continued) Electrical characteristics digital interface

$V_{DD} = V_{DD(NOR)}$, $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$
Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Global error flag valid time	t_{GEF_VAL}	–	–	250	ns	–	PRQ-746

11 Application information

Note: *The information provided in this chapter is a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device. The function must be verified in the real application. For sizing and dimensioning of external components, refer to the additional technical documentation or contact our technical support team for assistance.*

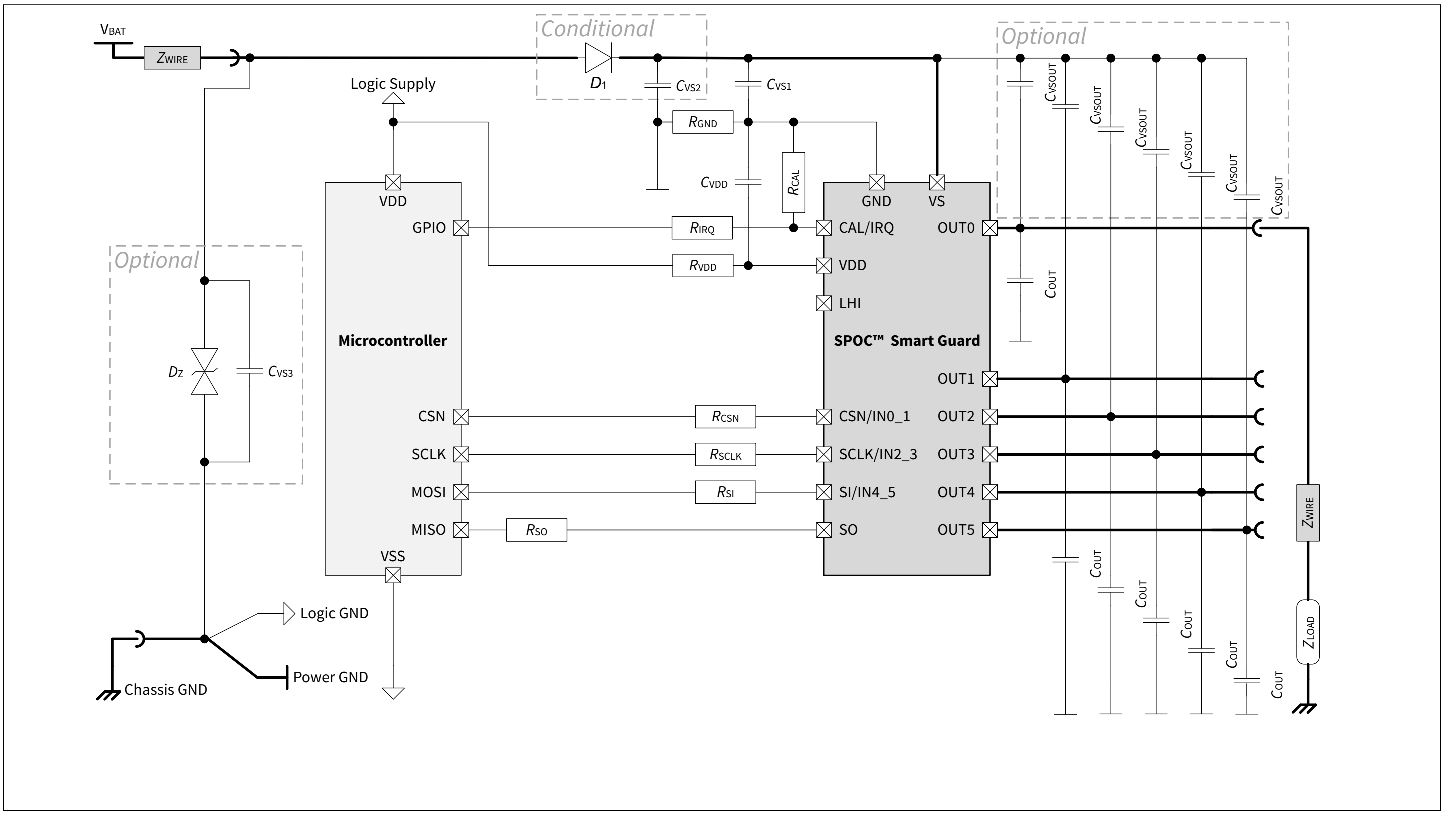


Figure 35 Application diagram

Table 31 Suggested component values

Reference	Value	Purpose
R_{GND}	100 Ω	Reverse battery protection and ground voltage spikes filtering for improved robustness against battery voltage transients
R_{VDD}	60 Ω	Device logic protection
R_{LHI}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{CAL}	1 kΩ	Calibration for internal current reference
R_{IRQ}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{CSN}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SCLK}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SI}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SO}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
C_{VDD}	470 nF	Digital supply voltage spikes filtering and for improved robustness against battery voltage transients

(table continues...)

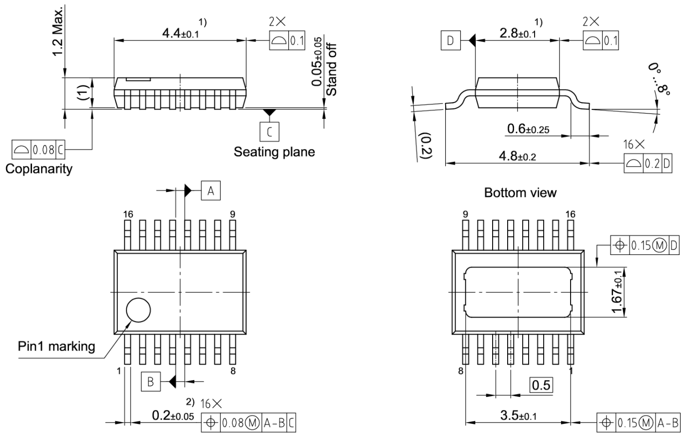
Table 31 **(continued) Suggested component values**

Reference	**Value**	**Purpose**
C_{VS1}	100 nF	Battery voltage spikes filtering
C_{VS2}	100 nF	Battery voltage spikes filtering
C_{OUT}	33 nF	For improved electromagnetic compatibility (EMC)
C_{VSOUT}	0.5 nF	For improved electromagnetic compatibility (EMC)
C_{VS3}	–	Filtering / buffer capacitor located at VBAT connector
D_1	–	Reverse blocking diode and protection against inverse currents from capacitive loads
D_{Z1}	–	Protection of microcontroller during overvoltage
D_{Z2}	–	Transient Voltage Suppressor diode Protection during overvoltage and in case of loss of battery while driving an inductive load
T1	–	Switch the fail-safe control voltage to enable the output channels
T2	–	Switch the fail-safe control voltage to disable the output channels

- Please contact us for information regarding the pin behaviour assessment
- For further information you may contact http://www.infineon.com

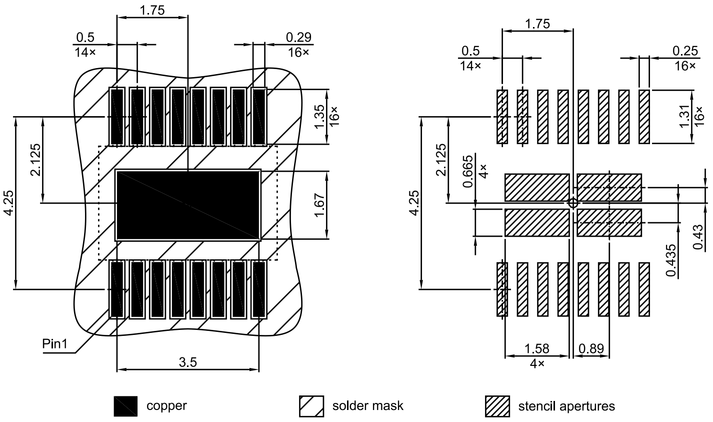
12 Package information

12.1 Package outline drawing



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊏◁⊕]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 36 PG-TFDSO-16 dual small outline package dimensions



All dimensions are in units mm
All pads are non-solder mask defined

Figure 37 PG-TFDSO-16 dual small outline footprint dimensions

***Note**: To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).*

Further information on packages https://www.infineon.com/packages

13 Revision history

Revision number	Date of release	Description of changes
1.00	2026-03-17	Initial datasheet

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