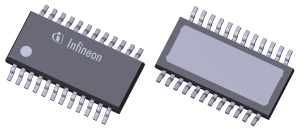
SPOC™ Wire Guard

Features

- High-side power switch with diagnosis and embedded protection
- Daisy chain capable 24 bit SPI with CRC
- Embedded I^2t wire and system protection
- Capacitive load switching mode
- ISO 26262 safety element out of context for safety requirements up to ASIL D



AEC Qualified

RoHS

ISO 26262 compliant

Potential applications

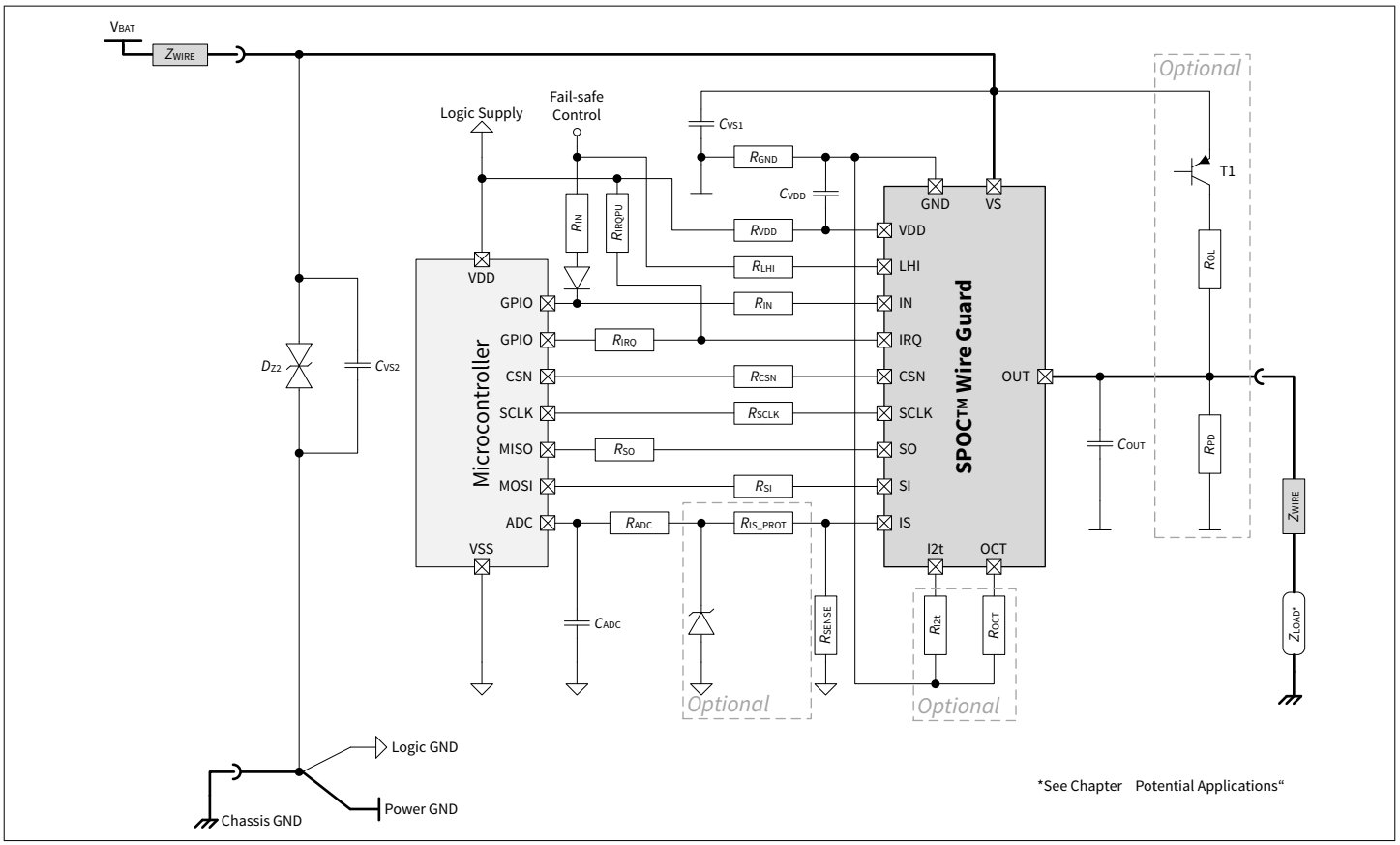
- Fail operational power supply
- Fuse and relay replacement in 12 V power distribution
- ECU main switch

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The SPOC™ Wire Guard is a smart high-side power switch with SPI as digital interface. The device is suitable for applications driving loads up to a nominal current of 15.3 A and supporting inrush currents. In addition to standard protection and standard diagnosis functions, the device offers selectable overcurrent protection, selectable I2t protection, fail safe mode, limp home mode, and enhanced diagnosis via the digital interface.



Package	Marking
PG-TSDSO-24	S0045SWPA1

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1 Product description

Basic features

- High-side power switch with diagnosis and embedded protection
- Daisy chain capable 24 bit SPI with CRC
- 3.3 V and 5 V compatible logic pins
- Capacitive load switching mode
- Reverse ON for low power dissipation in reverse polarity
- Switch-ON capability while inverse current condition (Inverse ON)
- Optimized for high immunity against electromagnetic interference (EMI)
- Green product (RoHS compliant)

Protection features

- Configurable restart control
- Absolute and dynamic temperature limitation
- Overcurrent protection with selectable overcurrent threshold
- Undervoltage shutdown
- Configurable integrated I2t function for system protection
- Overvoltage protection with external components

Diagnosis features

- Proportional load current sense
- Proportional chip temperature measurement
- Open load in ON and OFF state
- Short circuit to ground and battery
- Enhanced diagnosis feedback via digital interface

Functional safety features

- ISO 26262 safety element out of context for safety requirements up to ASIL D
- SPI interface with error detection (CRC, invalid read/write address, and SCLK count error detection)
- Communication watchdog
- Limp home mode and fail safe mode
- Monitoring of input pin status (IN and LHI)
- Current sense verification mode

Table 1 Product summary

Parameter	Symbol	Values
Power supply voltage range for normal operation	$V_{S(NOR)}$	5 V to 20 V
Extended power supply voltage range for operation	$V_{S(EXT)}$	2.8 V to 28 V
Digital supply voltage range for normal operation	$V_{DD(NOR)}$	2.4 V to 5.5 V
Maximum digital supply current consumption in normal operation	$I_{VDD(NORMAL)}$	2.6 mA
Typical operating current in active mode (all power stages ON)	$I_{GND(ACTIVE)}$	7.2 mA
Junction temperature range for normal operation	$T_{J(NOR)}$	-40°C to 150°C
Load dump voltage	$V_{BAT(LD)}$	35 V
Typical thermal resistance junction-to-ambient	$R_{th(JA)}$	24 K/W
Maximum ON-state resistance (T_J = 150°C)	$R_{DS(ON)\_150}$	9.0 mΩ

(table continues...)

Table 1 (continued) Product summary

Parameter	Symbol	Values
Nominal load current (T_A = 85°C)	$I_{L(NOM)\_85}$	15.3 A
Typical overcurrent detection threshold range	$I_{L(OCT)}$	27.2 A to 75.8 A

2 Block diagram and terms

2.1 Block diagram

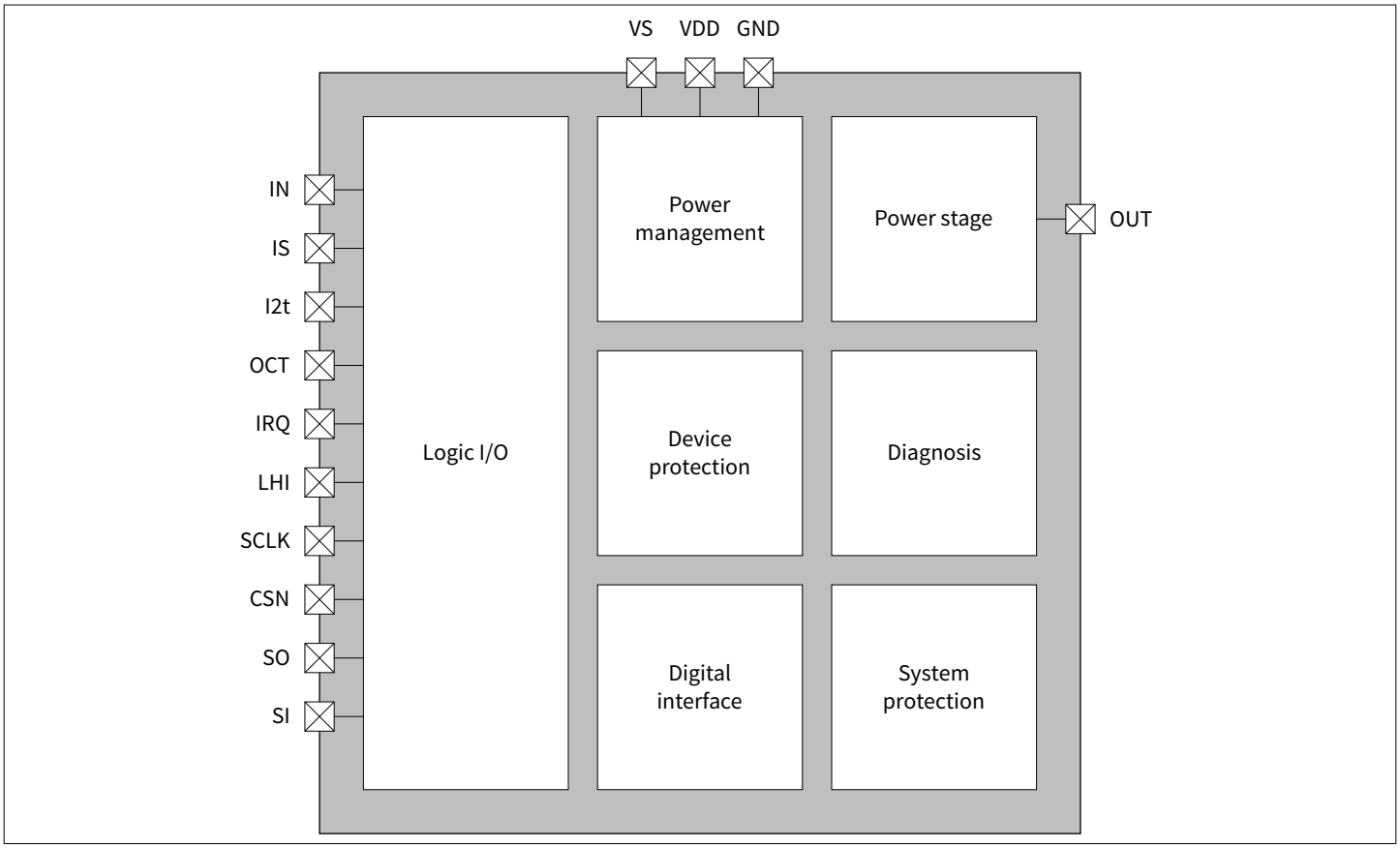


Figure 1 Block diagram

2.2 Terms

The figure below shows all the terms used in this datasheet, with their associated conventions for positive values. Voltages and currents are defined accordingly.

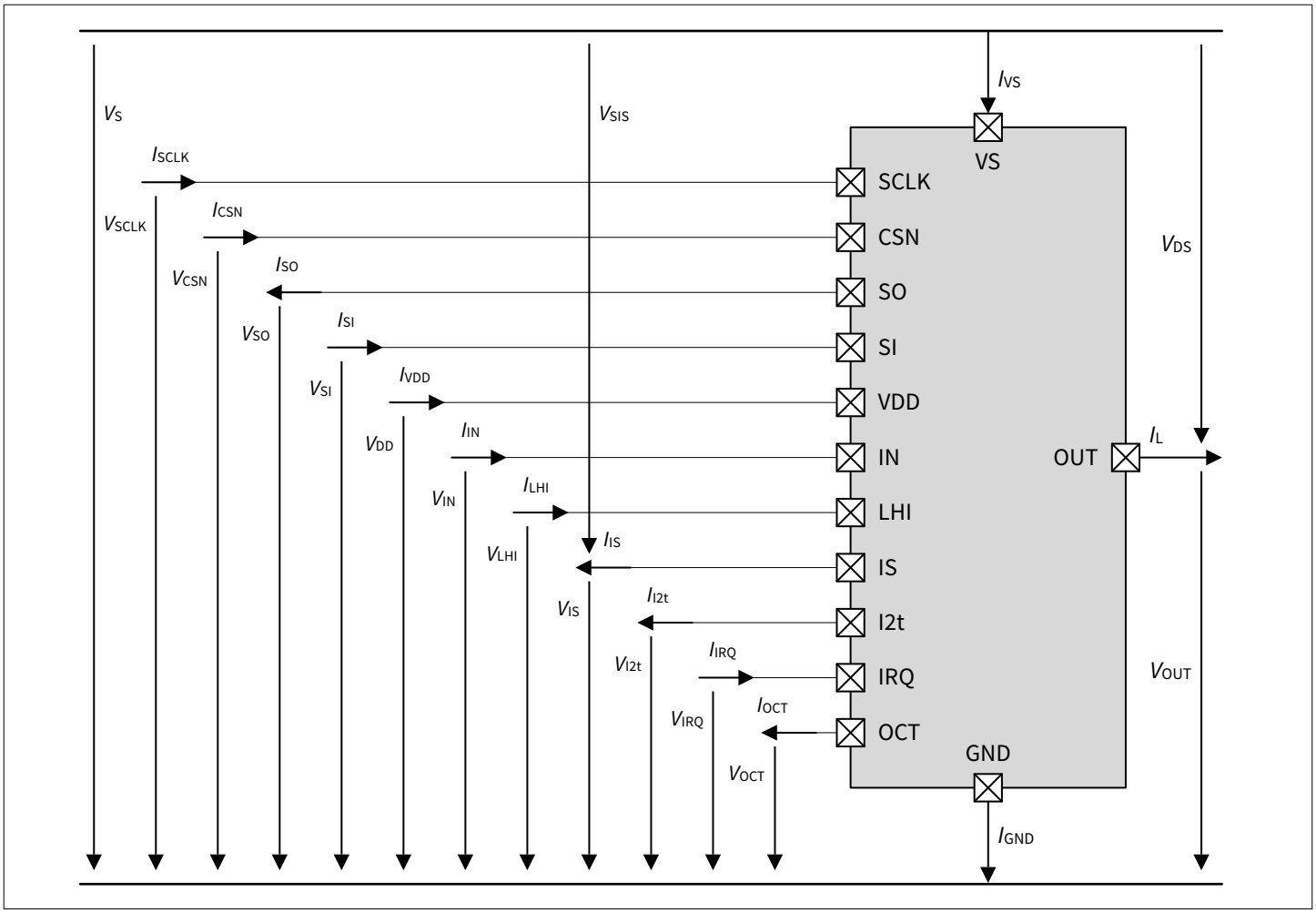


Figure 2 Voltage and current conventions

3 Pin configuration

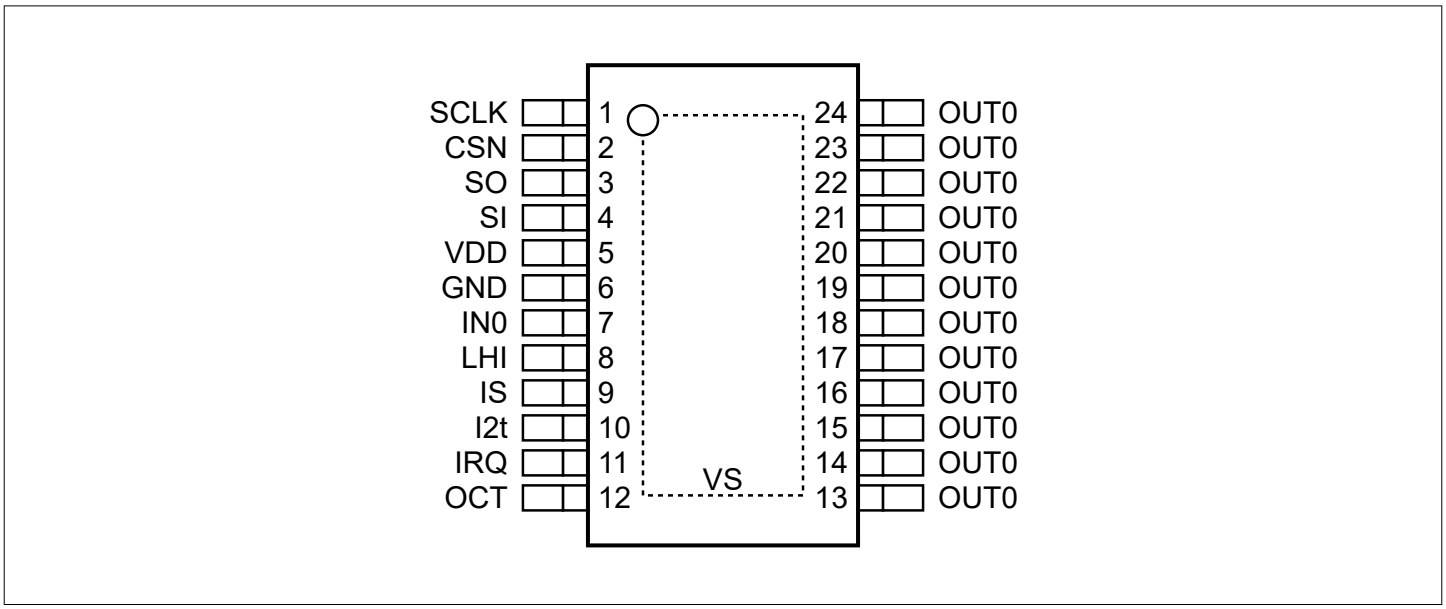


Figure 3 Pin configuration

Table 2 Pin definition

Pin	Symbol	I/O	Function
EP	VS (exposed pad)	–	**Power supply voltage** Battery voltage
1	SCLK	I	**Serial clock** Serial clock of SPI interface (active HIGH)
2	CSN	I	**Chip select** Chip select of SPI interface (active LOW); integrated pull up to VDD
3	SO	O	**Serial output** Serial output of SPI interface
4	SI	I	**Serial input** Serial input of SPI interface
5	VDD	–	**Digital supply voltage**
6	GND	–	**Ground** Ground connection for internal logic
7	IN0	I	**Input** Digital signal to switch ON the power stage (active HIGH) If not used: connect with R_{IN} = 4.7 kΩ resistor either to GND pin or to logic GND of the module

(table continues...)

Table 2 (continued) Pin definition

Pin	Symbol	I/O	Function
8	LHI	I	**Limp home input** Digital signal to enter limp home mode (active HIGH) If not used: connect with R_{LHI} = 4.7 kΩ resistor either to GND pin or to logic GND of the module
9	IS	O	**SENSE current output** Analog signal for diagnosis If not used: leave open
10	I2t	I	**Selectable I2t protection curve** A resistor R_{I2t} needs to be connected between I2t pin and GND pin to select one of the available I2t protection curves If not used: leave open. I2t protection curve selection as described in the I2t protection chapter
11	IRQ	O	**Interruption request open drain output** Digital signal to inform the microcontroller of warning, error or watchdog overflow (active HIGH) If not used: connect with a 10 kΩ resistor either to GND pin or to logic GND of the module
12	OCT	I	**Selectable overcurrent threshold** A resistor R_{OCT} needs to be connected between OCT pin and GND pin to select one of the available overcurrent thresholds If not used: leave open. Threshold selection as described in the overcurrent protection chapter
13-24	OUT0	O	**Output** Protected high-side power stage output 0[1)]

1) All output pins of the power stage have to be connected together on the PCB. All pins of the output are connected together internally. PCB traces have to be designed to withstand the maximum current that can flow.

4 Application information

***Note**: The information provided in this chapter is a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device. The function must be verified in the real application. For sizing and dimensioning of external components, refer to the additional technical documentation or contact our technical support team for assistance.*

4.1 Application setup

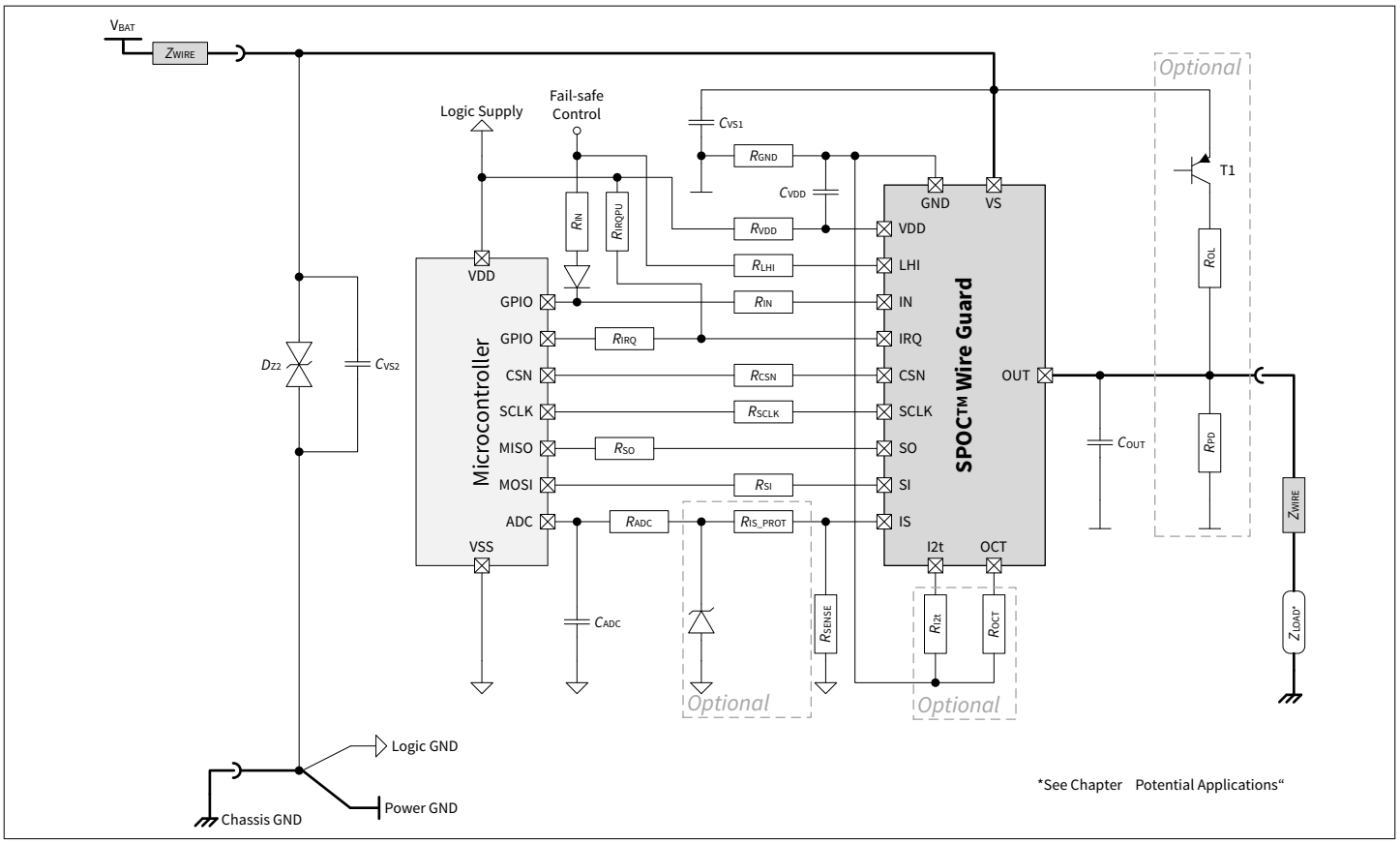


Figure 4 Application diagram

4.2 External components

Table 3 Suggested component values

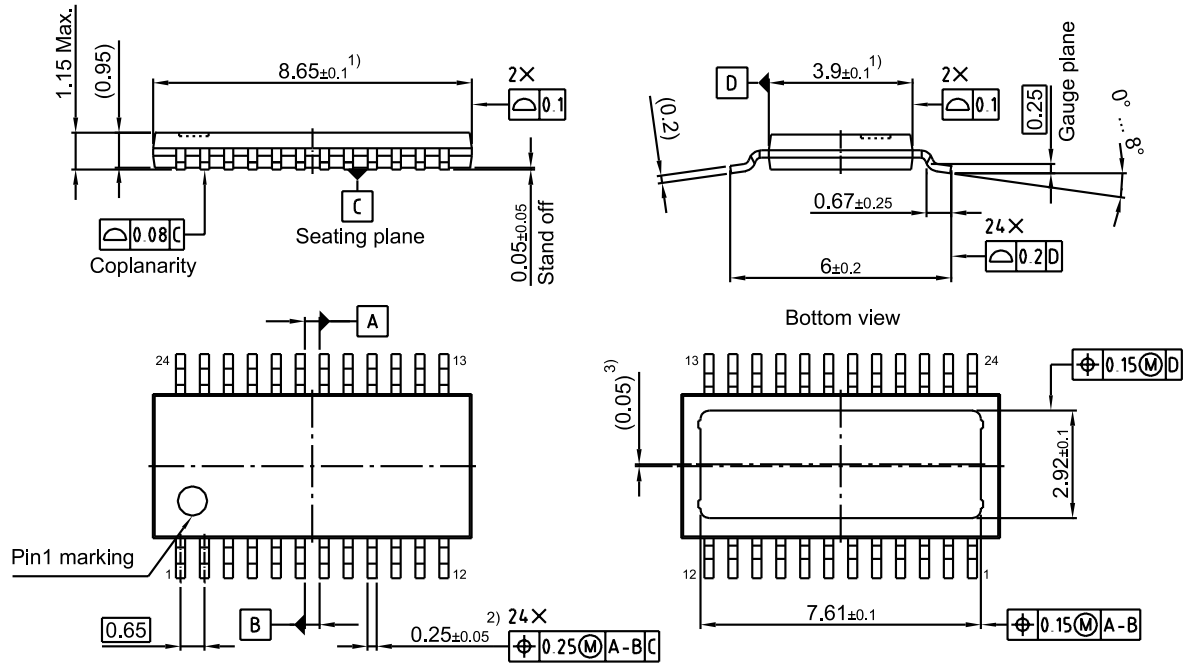
Reference	Value	Purpose
R_{GND}	40.2 Ω	Ground voltage spikes filtering for improved robustness against battery voltage transients
R_{VDD}	150 Ω for VDD = 3.3 V 750 Ω for VDD = 5 V	Device logic protection
R_{LHI}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{IN}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity Necessary to switch OFF the power stage during loss of ground

(table continues...)

Table 3 (continued) Suggested component values

Reference	Value	Purpose
R_{IRQ}	4.7 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{IRQPU}	10 kΩ	Interrupt request polarization (pull-up) Ensure the polarization of the open drain IRQ pin for interrupt request at the microcontroller
R_{CSN}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SCLK}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SO}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{SI}	1.2 kΩ	Protection of the microcontroller during overvoltage and reverse polarity
R_{IS_PROT}	4.7 kΩ	Protection resistor for overvoltage, reverse polarity, and loss of ground Value to be tuned with microcontroller specification
R_{SENSE}	1.2 kΩ	Sense resistor
R_{ADC}	4.7 kΩ	Microcontroller ADC voltage spikes filtering
R_{I2t}	R_{I2t_SHORT} to R_{I2t_OPEN}	Selection of the default I2t protection curve during power-up mode Protection of the device during overvoltage and reverse polarity
R_{OCT}	R_{OCT_SHORT} to R_{OCT_OPEN}	Selection of the default overcurrent threshold high during power-up mode Protection of the device during overvoltage and reverse polarity
R_{OL}	1.5 kΩ	Output polarization (pull-up) Ensure polarization of power stage during open load in OFF diagnosis
R_{PD}	47 kΩ	Output polarization (pull-down) Ensure polarization of power stage to distinguish between open load and short to V_S in OFF diagnosis
C_{ADC}	220 pF	Microcontroller ADC voltage spikes filtering A time constant ((R_{IS_PROT} + R_{ADC}) * C_{ADC}) longer than 1 µs is recommended
C_{VDD}	680 nF	Digital supply voltage spikes filtering and for improved robustness against battery voltage transients
C_{VS1}	100 nF	Battery voltage spikes filtering
C_{VS2}	–	Conditional buffer capacitor to support battery voltage spikes filtering in dependency of application setup (EMC)
C_{OUT}	10 nF	For improved electromagnetic compatibility (EMC)
D_{Z1}	–	Protection of microcontroller during overvoltage
D_{Z2}	–	Transient voltage suppressor diode Protection against overvoltage, loss of battery while driving an inductive load, and voltage spikes caused by fast load disconnection
T_1	–	Switch the battery voltage for open load in OFF diagnosis

5 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
3) Distance from centerline exposed pad to package centerline
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇿]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 5 PG-TSDSO-24 package outlines

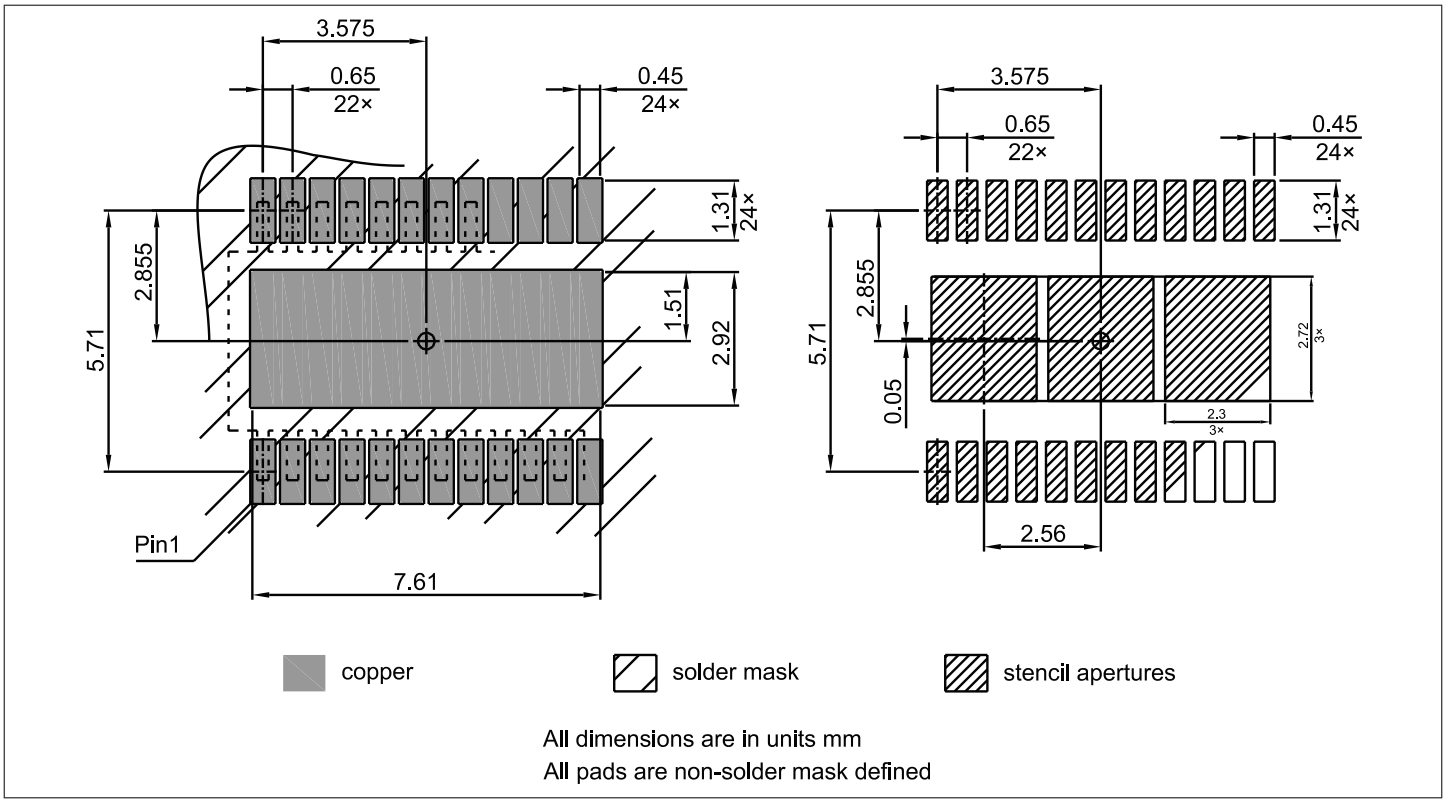


Figure 6 PG-TSDSO-24 footprint

***Note**: For minimum environmental impact and compliance with government regulations, the package of the device fulfills the requirements of a green product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). For further information, please refer to* https://www.infineon.com/packages.

Revision history

Revision	Date of release	Description of changes
Rev. 1.00	2026-03-03	Table 1 updated Table 2 updated Table 3 updated
Rev. 0.10	2025-10-01	Product overview available

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