

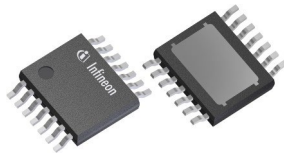


PROFET™ +2 12V

英飞凌智能高边功率开关

特性

- 具有诊断和保护功能的高边开关
- PROFET™ +2 12V 系列产品之一
- 逆向电流条件下的开启功能 (InverseON)
- 电容负载开关模式
- 绿色产品：符合 RoHS 标准



潜在应用

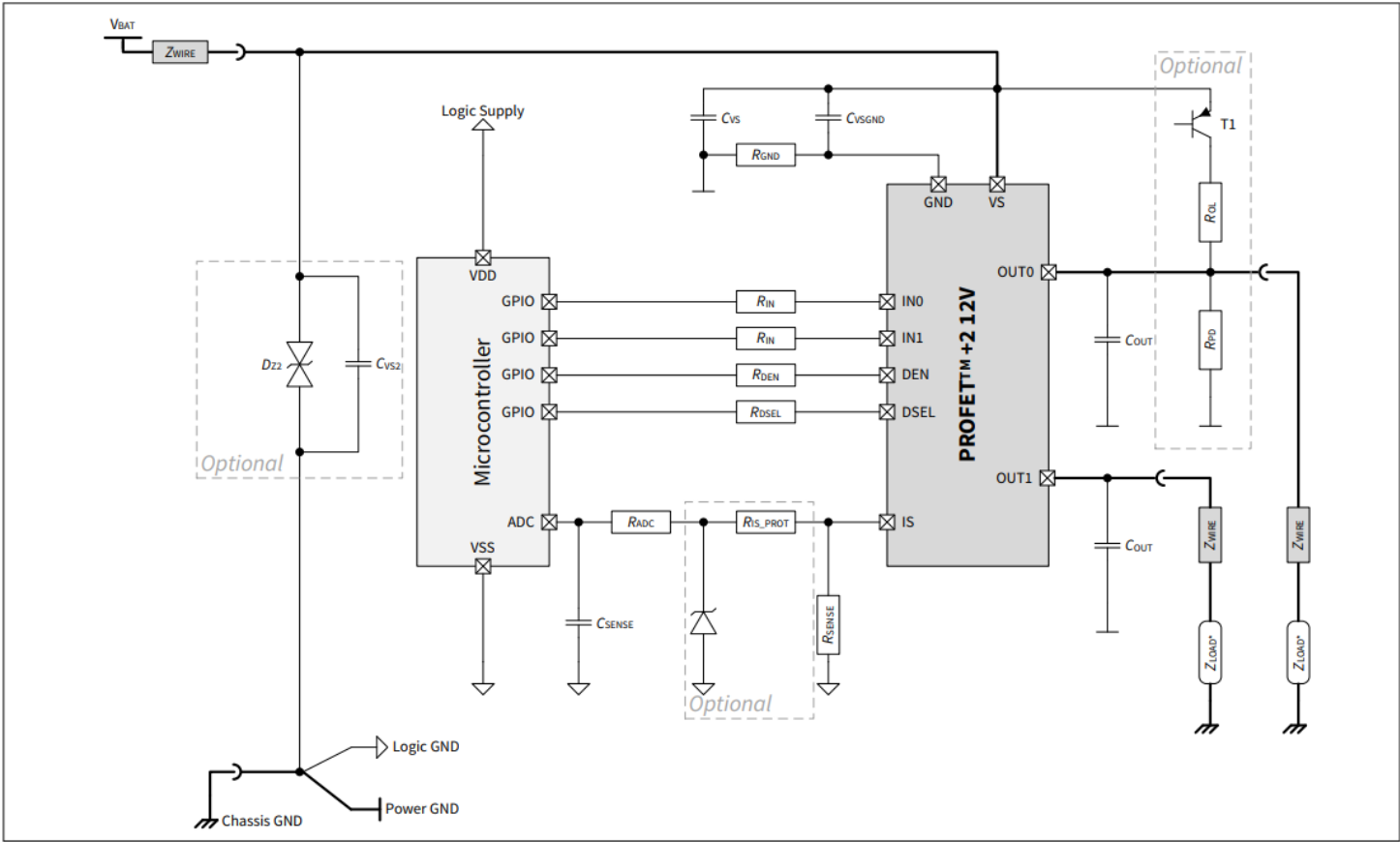
- 取代继电器、保险丝和分立电路
- 系统供电保护
- 电子控制单元电源主开关
- 适用于驱动阻性、感性和容性负载
- 适用于驱动热元件

产品验证

汽车应用认证。
产品依据AEC-Q100 Grade1进行验证。

描述

BTS7090-2EPL 是一款智能高边开关，提供保护功能和诊断功能。该器件提供电流钳位并具有容性负载开关模式对电容充电。采用SMART7技术。



Further information in [Chapter 9](#)

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性请务必访问 infineon.com 参考最新的英文版本（控制文档）。

描述

Parameter	Symbol	Values
Minimum operating voltage	$V_{S(OP)}$	3 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	2.7 V
Maximum operating voltage	V_S	28 V
Minimum overvoltage protection ($T_J \geq 25^\circ\text{C}$)	$V_{DS(CLAMP)_25}$	35 V
Maximum current in sleep mode ($T_J \leq 85^\circ\text{C}$)	$I_{VS(SLEEP)_85}$	0.5 μA
Maximum operative current	$I_{GND(ACTIVE)}$	4.5 mA
Typical ON-state resistance ($T_J = 25^\circ\text{C}$)	$R_{DS(ON)_25}$	90 m Ω
Maximum ON-state resistance ($T_J = 150^\circ\text{C}$)	$R_{DS(ON)_150}$	180 m Ω
Nominal load current ($T_A = 85^\circ\text{C}$)	$I_{L(NOM)}$	2 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	k_{ILIS}	1000
Overcurrent limitation	I_{LIM}	4.7 A

诊断特征

- 比例负载电流采样
- 在打开和关闭情况下负载开路检测
- 短路到地和短路到电源检测

保护功能

- 带重启控制的绝对过温保护和动态过温保护
- 过流钳位
- 过压保护

Type	Package	Marking
BTS7090-2EPL	PG-TSDSO-14	7090-2AL

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1 框图和terms

1.1 框图

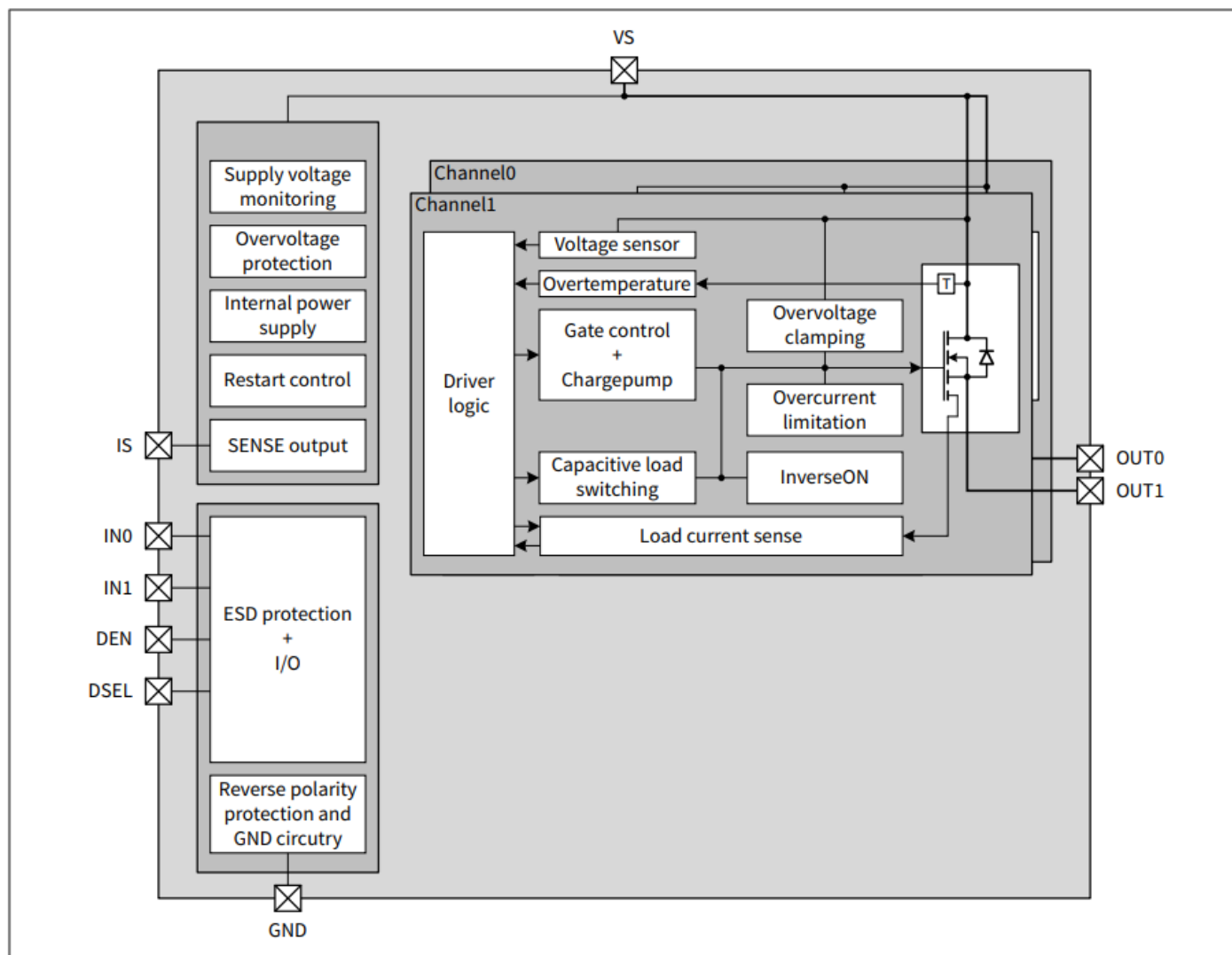


Figure 2 **Block diagram of BTS7090-2EPL**

1.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

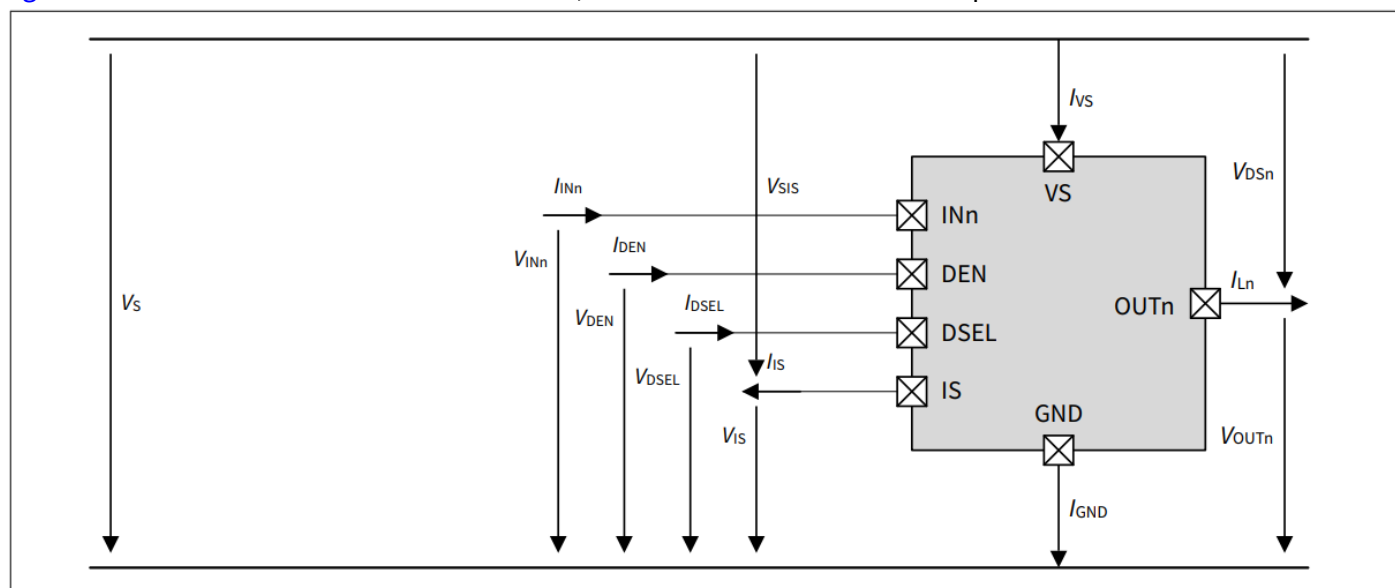


Figure 3 Voltage and current convention

2 引脚配置

2 引脚配置

2.1 引脚分配

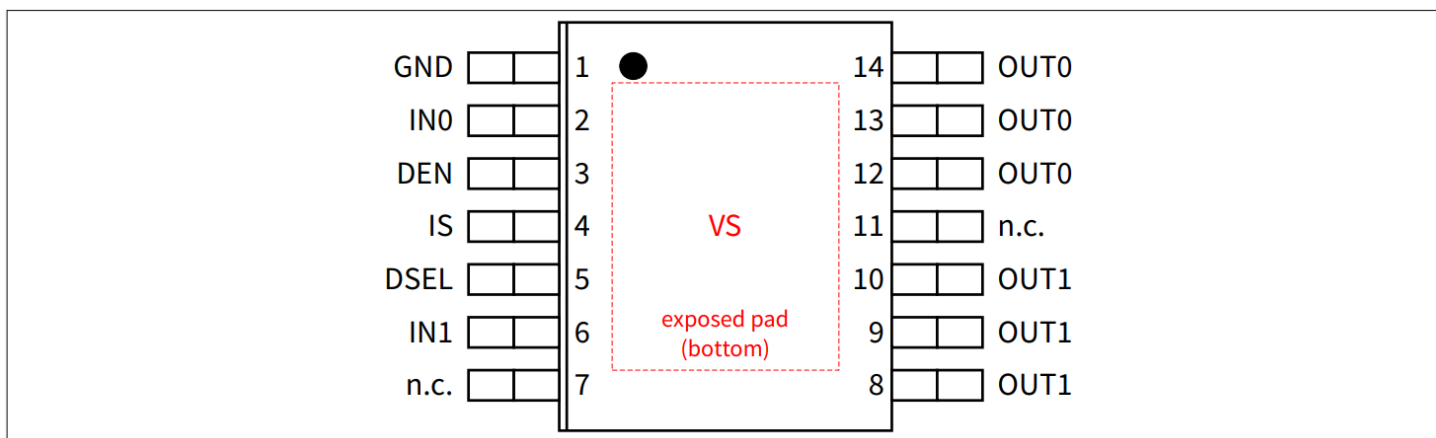


Figure 4 Pin configuration

2.2 引脚定义和功能

Table 1 Pin definition

Pin	Symbol	Function
EP	VS (exposed pad)	Supply Voltage Battery voltage
1	GND	Ground Ground connection for the internal logic
2, 6	INn	Input Channel n Digital signal to switch ON channel n ("high" active) If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
3	DEN	Diagnostic Enable Digital signal to enable device diagnosis ("high" active) and to clear the protection counter of channel selected with DSEL pin. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
4	IS	SENSE current output Analog/digital signal for diagnosis If not used: Left open
5	DSEL	Diagnosis Selection Digital signal to toggle between the channels. If not used: Connect with a 10kΩ resistor either to GND pin or to module ground
7, 11	n.c.	Not connected, internally not bonded
8-10, 12-14	OUTn	Output n Protected high-side power output channel n ¹⁾

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

3 产品基本特性

3 产品基本特性

3.1 绝对最大额定值

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	28	V	²⁾ -	PRQ-34
Load dump voltage	$V_{\text{BAT(LD)}}$	–	–	35	V	²⁾ suppressed load dump acc. to ISO16750-2 (2010). $R_i = 2\ \Omega$	PRQ-36
Supply voltage for short circuit protection	$V_{\text{BAT(SC)}}$	0	–	24	V	²⁾ Setup acc. to AEC- Q100-012	PRQ-38
Reverse polarity voltage	$-V_{\text{BAT(REV)}}$	–	–	16	V	²⁾ $t \leq 2\text{min}$ $T_A = +25^\circ\text{C}$ Setup as described in Chapter 9	PRQ-40
Current through GND pin	I_{GND}	-50	–	50	mA	²⁾ R_{GND} according to Chapter 9	PRQ-44

Logic & control pins (Digital Input = DI)**DI = INN, DEN, DSEL**

Current through DI pin	I_{DI}	-1	–	2	mA	²⁾ ¹⁾	PRQ-47
Current through DI pin - Reverse battery condition	$I_{\text{DI(REV)}}$	-1	–	10	mA	²⁾ ¹⁾ $t \leq 2\text{ min}$	PRQ-48

IS pin

Voltage at IS pin	V_{IS}	-1.5	–	V_S	V	²⁾ $I_{\text{IS}} = 10\ \mu\text{A}$	PRQ-50
Current through IS Pin	I_{IS}	-25	–	$I_{\text{IS(SAT),M AX}}$	mA	²⁾ –	PRQ-52

温度

Junction temperature	T_J	-40	–	+150	$^{\circ}\text{C}$	²⁾ –	PRQ-53
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(表格续下页.....)

Table 2 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Storage temperature	T_{STG}	-55	–	+150	°C	²⁾ –	PRQ-54

ESD 承受能力

ESD Susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	²⁾ HBM ³⁾	PRQ-55
ESD Susceptibility OUTn vs GND and VS connected (HBM)	$V_{ESD(HBM)_{OUT}}$	-4	–	4	kV	²⁾ HBM ³⁾	PRQ-56
ESD Susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	²⁾ CDM ⁴⁾	PRQ-57
ESD Susceptibility corner pins (CDM) - (pins 1, 7, 8, 14)	$V_{ESD(CDM)_{CRN}}$	-750	–	750	V	²⁾ CDM ⁴⁾	PRQ-58

Power stage

Maximum energy dissipation - single pulse	E_{AS}	–	–	6.5	mJ	²⁾ $I_L = 2 \cdot I_{L(NOM)}$ $T_{J(0)} = 150^\circ\text{C}$ $V_S = 28\text{ V}$	PRQ-63
Maximum energy dissipation - repetitive pulse	E_{AR}	–	–	1.5	mJ	²⁾ $I_L = I_{L(NOM)}$ $T_{J(0)} = 85^\circ\text{C}$ $V_S = 13.5\text{ V}$ 1M cycles	PRQ-64
Load current	$ I_L $	–	–	$I_{LIM,MAX}$	A	²⁾ –	PRQ-65

- 1) Maximum V_{DI} to be considered for Latch-Up tests: 5.5 V
 2) Not subject to production test - specified by design
 3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002
 4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011

注:

- Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 工作范围

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(NOR)}$	4	13.5	20	V	¹⁾ –	PRQ-66
Lower extended supply voltage range for operation (normal)	$V_{S(EXT,LOW)}$	2.7	–	4	V	¹⁾ ²⁾ ³⁾ (parameter deviations possible)	PRQ-67
Upper extended supply voltage range for operation	$V_{S(EXT,UP)}$	20	–	28	V	¹⁾ ³⁾ (parameter deviations possible)	PRQ-68
Junction temperature	T_J	–40	–	+150	°C	¹⁾ –	PRQ-69

1) Not subject to production test - specified by design

2) In case of V_S voltage decreasing refer to the maximum voltage of $V_{S(UV)}$, in case of V_S voltage increasing refer to the maximum voltage of $V_{S(OP)}$

3) Protection functions still operative

注:

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the Electrical Characteristics tables.

3.3 热阻抗

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-top	Ψ_{JTOP}	–	7	11.8	K/W	¹⁾ ²⁾	PRQ-74
Thermal resistance junction-to-case	R_{thJC}	–	7.6	12.9	K/W	¹⁾ ²⁾ simulated at exposed pad	PRQ-71
Thermal resistance junction-to-ambient	R_{thJA}	–	38	–	K/W	¹⁾ ²⁾	PRQ-72

1) Not subject to production test - specified by design

3 产品基本特性

- 2) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a $76.2 \times 114.3 \times 1.5$ mm board with 2 inner copper layers ($2 \times 70 \mu\text{m Cu}$, $2 \times 35 \mu\text{m Cu}$). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at $T_A = 105^\circ\text{C}$, $P_{\text{DISSIPATION}} = 1 \text{ W}$

注:

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

3.3.1 PCB 设置

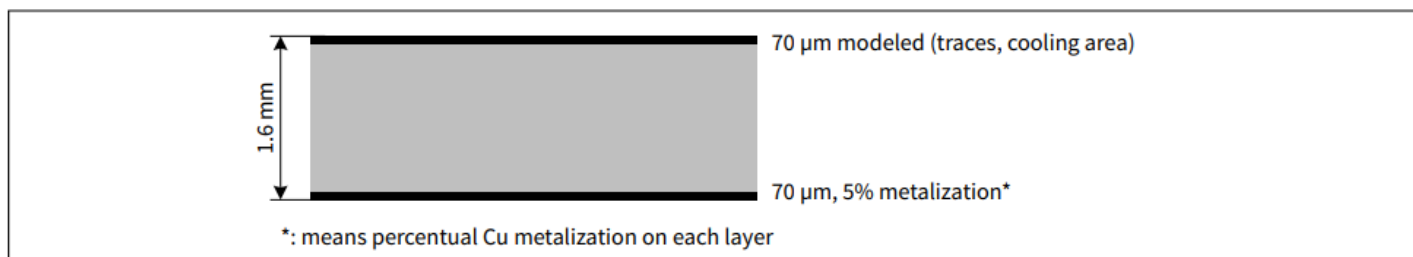


Figure 5 1s0p PCB cross section

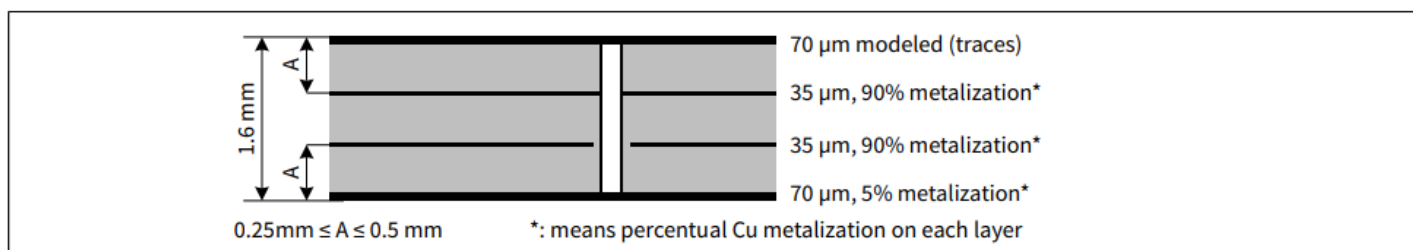


Figure 6 2s2p PCB cross section

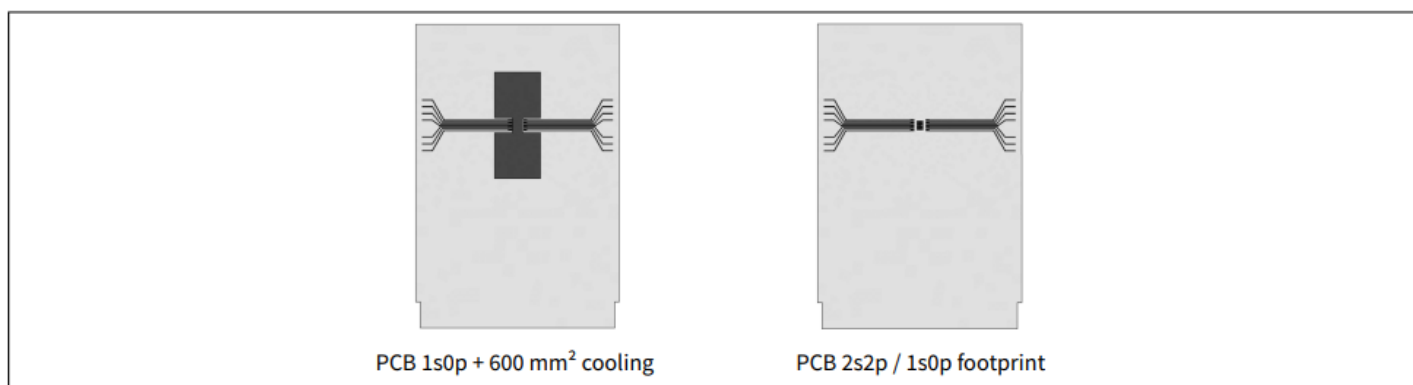


Figure 7 PCB setup for thermal simulations

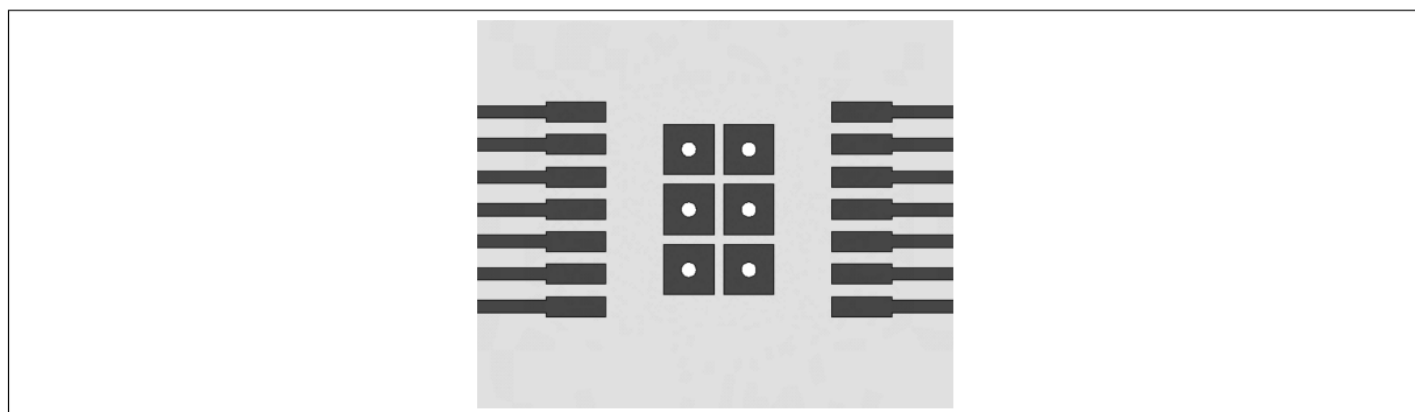


Figure 8 Thermal vias on PCB for 2s2p PCB setup

3.3.2 热阻抗

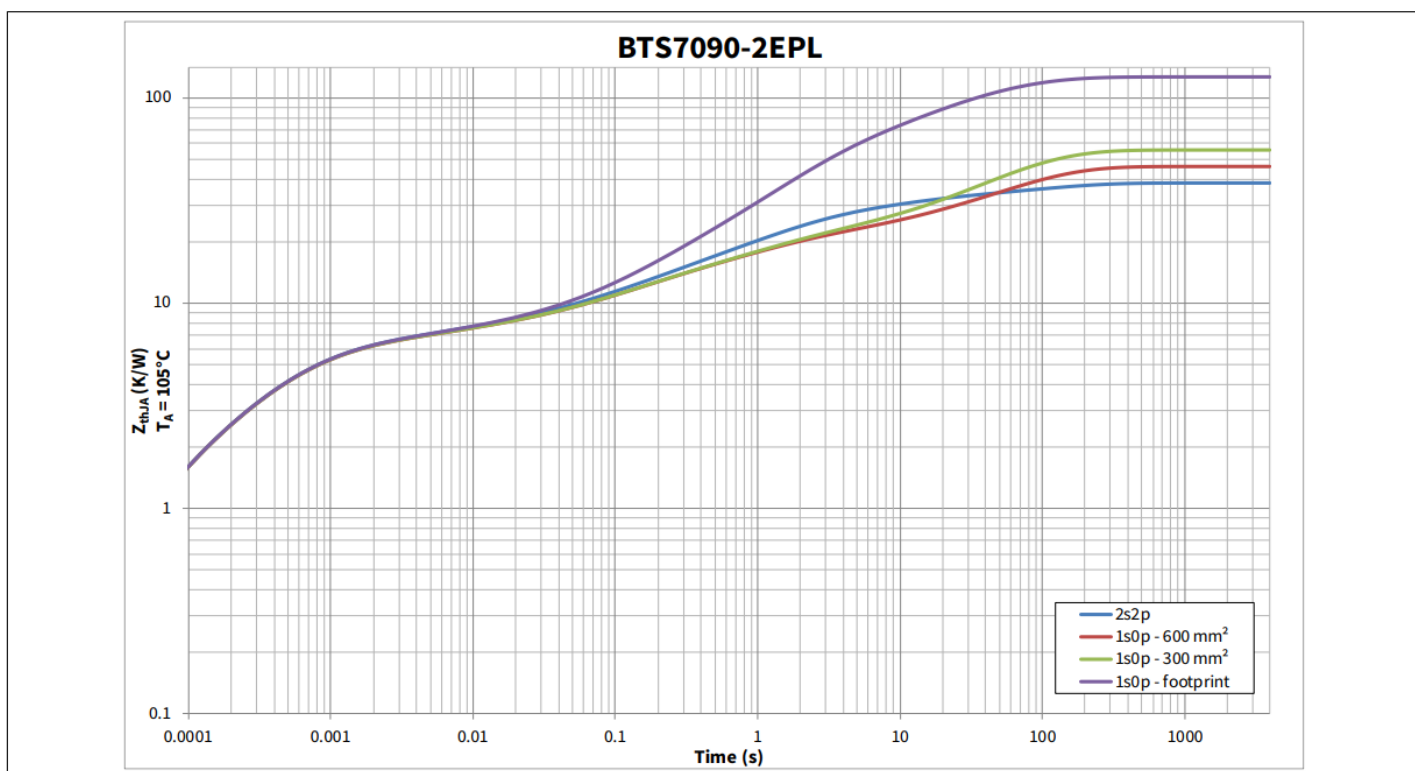


Figure 9 Typical thermal impedance. PCB setup according to PCB setup

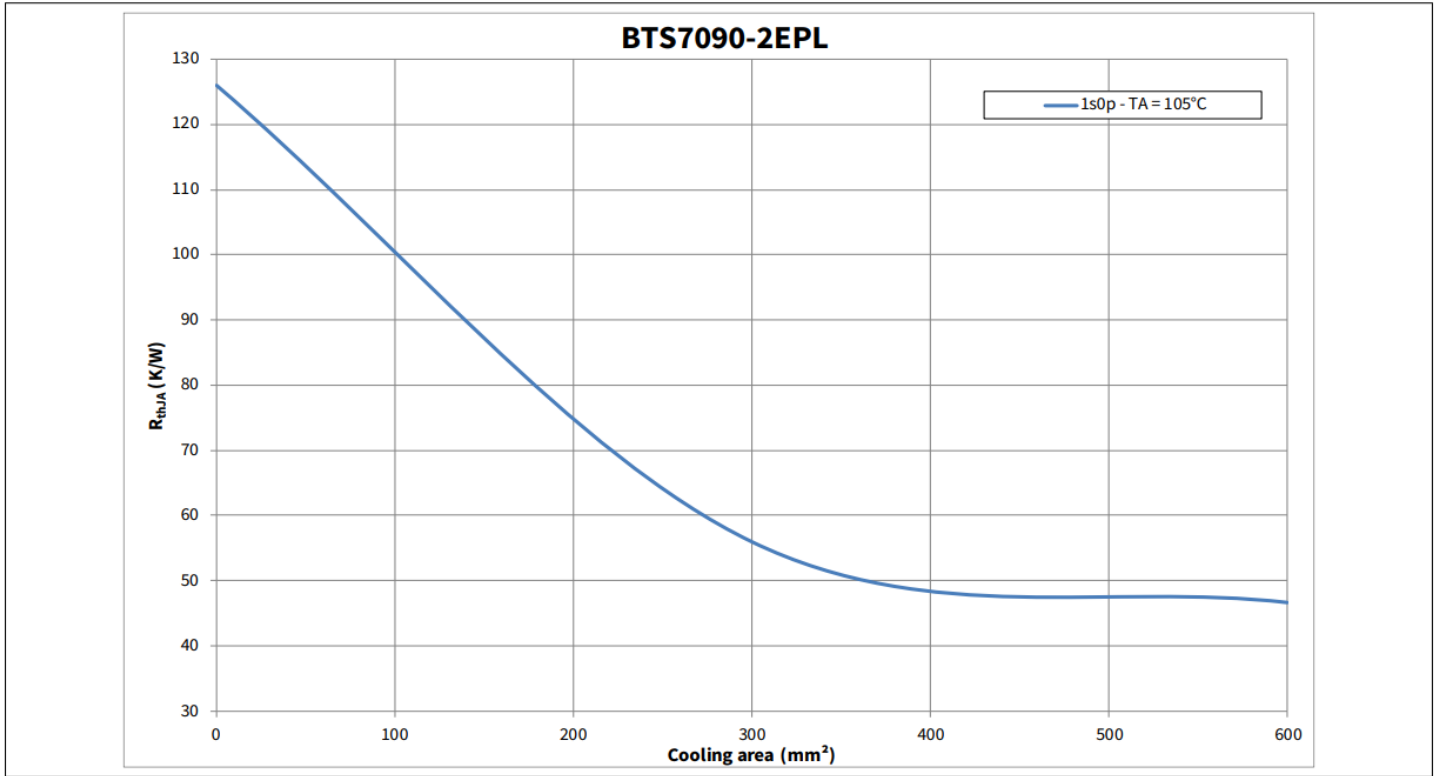


Figure 10 Thermal resistance on 1s0p PCB with various cooling surfaces

4 I/O 引脚

该器件有四个数字引脚用于直接控制。

4.1 数字 I/O 引脚

数字输入 (DI) 引脚是 INn、DEN、DSEL

4.1.1 输入引脚

输入引脚 IN0 和 IN1 激活相应的输出通道。输入电路可兼容 3.3 V 和 5 V。输入电路的等效电路如图 11 所示。未使用引脚，则必须通过 10 k Ω 电阻将其连接至 GND 引脚或模块接地。

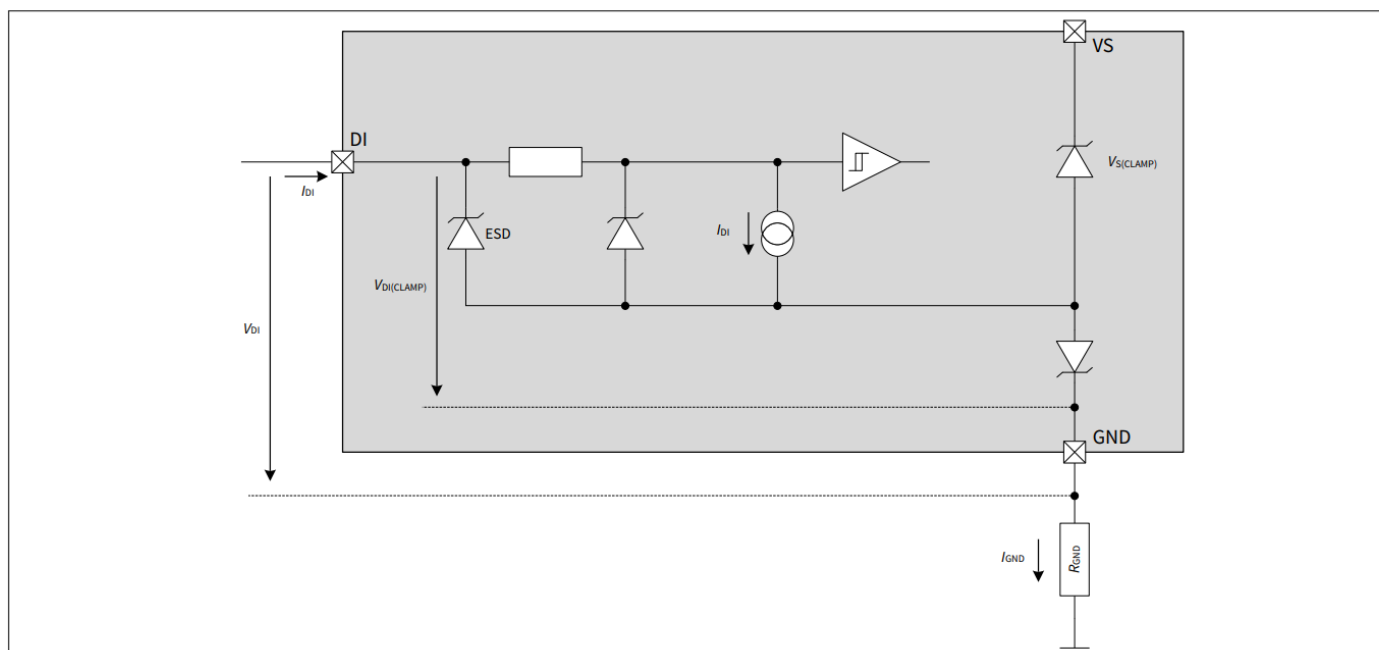


Figure 11 **Input circuitry**

逻辑电平“低电平”和“高电平”的阈值由参数 $V_{DI(TH)}$ 和 $V_{DI(HYS)}$ 定义。这两个值之间的关系如图12所示。

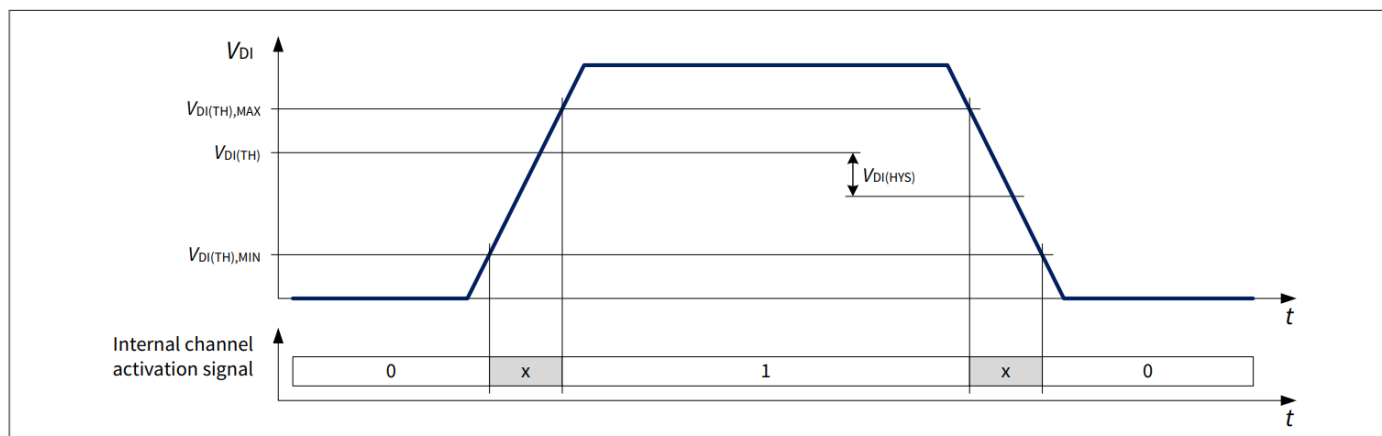


Figure 12 Input threshold voltages and hysteresis

4.1.2 诊断引脚

诊断使能 (DEN) 引脚控制诊断电路和保护电路。当 DEN 引脚置位为“高”时，诊断是启用的（参见[章节 8.2](#) 了解更多详情）。当置位为“低电平”时，诊断禁用（IS 引脚置位为高阻态）。诊断选择 (DSEL) 引脚选择执行诊断的通道（见表 12）。见图 12 了解更多详情。

DEN 引脚从“高”电平到“低电平”的转变将清除 DSEL 引脚所选择通道的保护锁存器，具体取决于输入引脚的逻辑状态和 DEN 脉冲长度（参见[章节 7.3](#) 了解更多详细信息）。

4.2 电气特性 I/O 引脚

$V_S = 4\text{ V}$ 至 20 V , $T_J = -40^\circ\text{C}$ 至 $+150^\circ\text{C}$

Unless otherwise specified typical values: $V_S = 13.5\text{ V}$, $T_J = 25^\circ\text{C}$

Digital input (DI) pins = INN, DEN, DSEL

Table 5 Electrical characteristics I/O pins

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See Figure 11 and Figure 12	PRQ-76
Digital input clamping voltage	$V_{DI(CLAMP1)}$	–	7	–	V	¹⁾ $I_{DI} = 1\text{ mA}$ See Figure 11 and Figure 12	PRQ-77
Digital input clamping voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2\text{ mA}$ See Figure 11 and Figure 12	PRQ-78
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	¹⁾ See Figure 11 and Figure 12	PRQ-80
Digital input current ("high")	$I_{DI(H)}$	2	10	25	μA	$V_{DI} = 2\text{ V}$ See Figure 11 and Figure 12	PRQ-81
Digital input current ("low")	$I_{DI(L)}$	2	10	25	μA	$V_{DI} = 0.8\text{ V}$ See Figure 11 and Figure 12	PRQ-82

¹⁾ Not subject to production test - specified by design

5 电源

该器件由VS供电，VS用于为内部逻辑电路以及功率输出级供电。在欠压条件下，器件具有检测电路，可防止功率输出级的激活以及诊断。

5.1 操作模式和转换

5.1.1 操作模式

该器件有以下工作模式：

- Sleep
- Inactive with diagnosis
- Active with diagnosis
- Active without diagnosis
- Capacitive load switching mode with diagnosis
- Capacitive load switching mode without diagnosis

操作模式之间的转换根据以下变量确定：

- INn 引脚的逻辑电平
- INn 引脚上的 PWM 信号
- DEN 引脚的逻辑电平

包含工作状态转换图如图13所示.器件的行为以及某些参数可能会独立于器件的操作模式而变化。此外，由于欠电压检测电路监控 VS 供电电压，因此可以看到在同一个模式下一些参数和状态的变化。

Table 6 shows the correlation between operation modes, VS supply voltage, and the state of the most important functions (channel status).

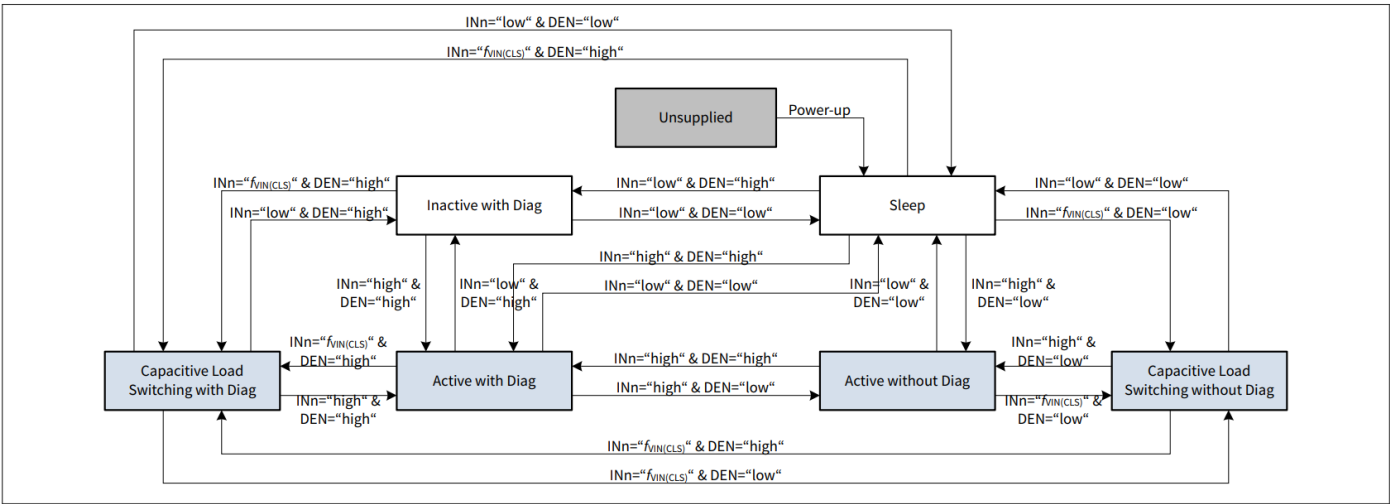


Figure 13 Operation mode state diagram

Table 6 Operation mode, device function and VS voltage

Operation mode	Function	VS > VS(OP)	VS < VS(OP)
Sleep	Channels	OFF	OFF
	Diagnosis	OFF	OFF

(表格续下页.....)

5 电源

Table 6 (continued) Operation mode, device function and V_S voltage

Operation mode	Function	$V_S > V_{S(OP)}$	$V_S < V_{S(OP)}$
Inactive with diagnosis	Channels	OFF	OFF
	Diagnosis	ON	OFF
Active with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Active without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF
Capacitive load switching mode with diagnosis	Channels	ON	OFF
	Diagnosis	ON	OFF
Capacitive load switching mode without diagnosis	Channels	ON	OFF
	Diagnosis	OFF	OFF

5.1.1.1 Unsupplied

在此状态下，器件供电电压低于欠压阈值 $V_{S(UV)}$ 。

5.1.1.2 上电

当供电电压 (V_S) 加到器件上时，器件进入上电阶段，电源电压上升直至超过欠压阈值 $V_{S(OP)}$ 。

5.1.1.3 休眠p

当数字输入 (DI) 引脚设置为“低电平”时，器件处于休眠模式。在休眠模式下，电流功耗为 $I_{VS(SLEEP)}$ 。过温保护、过载保护和欠压保护机制被禁用。该器件仅处于休眠模式，如果保护没有激活 ($n_{RESTART(CR)} = 0$, $T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)), see [Chapter 7.3](#).

5.1.1.4 Inactive with diagnosis

当 DEN 引脚置位为“高”且输入引脚置位为“低电平”时，器件处于 Inactive with diagnosis 模式。通道处于关闭状态，可进行关断状态下负载开路诊断。根据负载工况，IS 引脚可能出现故障电流 $I_{IS(FAULT)}$ 或负载开路电流 $I_{IS(OLOFF)}$ 状态。在 Inactive with diagnosis 模式下，器件的消耗电流增加。

5.1.1.5 Active with diagnosis

Active with diagnosis 是正常工作模式之一。当 INn = “高”且 DEN = “高”时，器件进入 active with diagnosis 模式，在此模式下，一个或多个打开，并具有诊断功能。芯片电流功耗参数 $I_{GND(ACTIVE)}$ 定义。

5.1.1.6 Active without diagnosis

当 INn = “高”且 DEN = “低电平”时，器件处于 active without diagnosis 模式，在此模式下，一个或多个输出打开，但不具有诊断功能。

5.1.1.7 Capacitive load switching mode with diagnosis

该器件具有 capacitive load switching with diagnosis 模式，用于驱动容性负载。当 INn = “ $f_{VIN(CLS)}$ ”和 DEN 设置为高电平时，器件进入 capacitive load switching mode with diagnosis 模式，在此模式下，一个或多个输出打开，并具有诊断功能。芯片电流参数 $I_{GND(ACTIVE)}$ 定义。

5电源

5.1.1.8 Capacitive load switching mode without diagnosis

当 INn = “fVIN(CLS)” 且 DEN 设置为“低电平”时，器件处于capative load switching mode without diagnosis模式，在此条件下，一个或多个输出无需诊断即可打开。

5.2 VS 欠压

电源电压在 VS(OP) 和 VS(UV) 之间，触发欠压保护机制。
只要 VS > VS(OP)，功率输出级状态跟随输入逻辑指令。
如果器件处于active模式，或者Capacitive Load Switching模式，或者带诊断模式，或者不带诊断模式，且供电电压VsVs低于欠压阈值VS(UV)以下，内部逻辑将关闭输出通道。

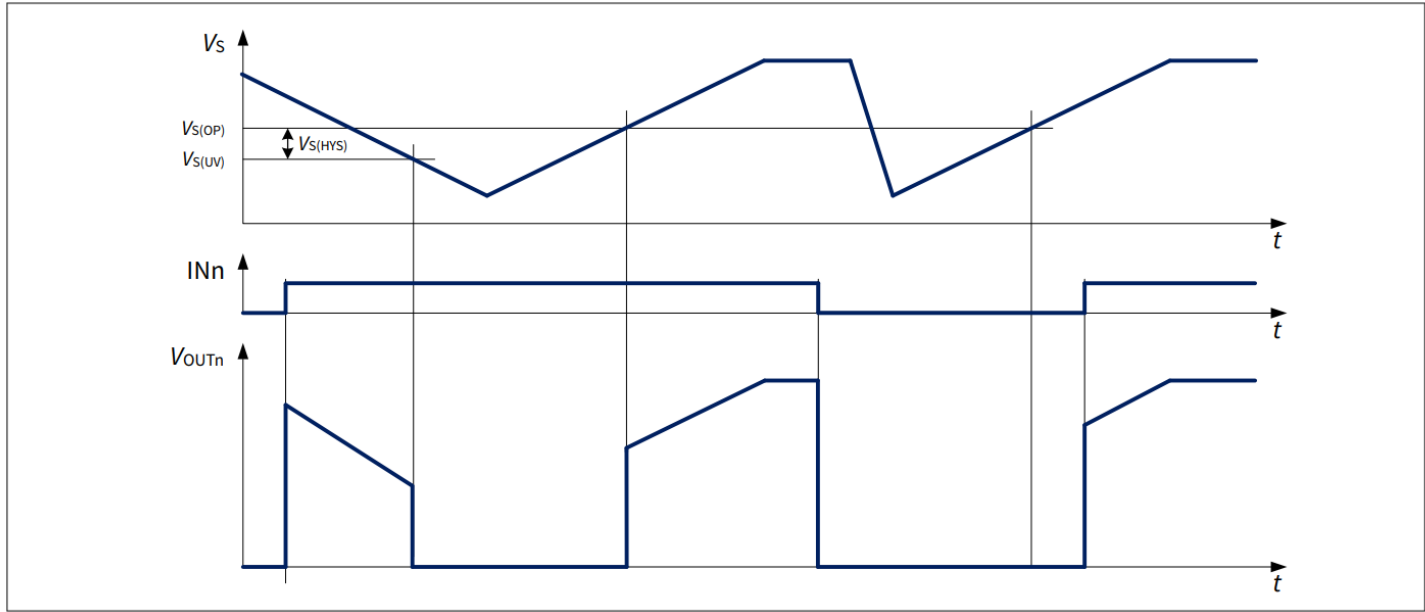


Figure 14 VS undervoltage behavior

5.3 电源电气特性参数

VS = 4 V to 20 V, TJ = -40°C to +150°C
Unless otherwise specified typical values: VS = 13.5 V, TJ = 25°C
Typical resistive loads connected to the outputs for testing (unless otherwise specified):
BTS7090-2EPL: RL = 6.8 Ω

Table 7 Electrical characteristics power supply

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS pin							
Power supply undervoltage shutdown	V _{S(UV)}	1.8	2.2	2.7	V	V _S decreasing INn = “high” From 0 ≤ V _{DS} ≤ 0.5 V to V _{DS} ~ V _S See Figure 14	PRQ-98

(表格续下页.....)

5电源

Table 7 (continued) Electrical characteristics power supply

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply minimum operating voltage	$V_{S(OP)}$	2.1	2.5	3	V	V_S increasing INn = "high" From $V_{DS} \sim V_S$ to $0 \leq V_{DS} \leq 0.5 \text{ V}$ See Figure 14	PRQ-99
Power supply undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	0.3	–	V	¹⁾ $V_{S(OP)} - V_{S(UV)}$ See Figure 14	PRQ-100
Breakdown voltage between GND and VS pins in reverse battery	$-V_{S(REV)}$	16	–	30	V	¹⁾ $I_{GND(REV)} = 7 \text{ mA}$ $T_J = 150^\circ\text{C}$	PRQ-101
Power supply current consumption in sleep mode with Loads at $T_J \leq 85^\circ\text{C}$	$I_{VS(SLEEP)_85}$	–	0.01	0.5	μA	¹⁾ $V_S = 20 \text{ V}$ $V_{OUT} = 0 \text{ V}$ INn = DEN = DSEL = "low" $T_J \leq 85^\circ\text{C}$	PRQ-821
Power supply current consumption in sleep mode with loads at $T_J = 150^\circ\text{C}$	$I_{VS(SLEEP)_150}$	–	1	8	μA	$V_S = 20 \text{ V}$ $V_{OUT} = 0 \text{ V}$ INn = DEN = DSEL = "low" $T_J = 150^\circ\text{C}$	PRQ-822
Operating current in active with diagnosis mode	$I_{GND(ACTIVE)}$	–	3.7	4.5	mA	$V_S = 20 \text{ V}$ INn = DEN = DSEL = "high"	PRQ-823
Operating current in inactive with diagnosis mode	$I_{GND(INACTIVE)}$	–	1.8	2.2	mA	$V_S = 20 \text{ V}$ INn = "low" DEN = DSEL = "high"	PRQ-824

1) Not subject to production test - specified by design

6 功率级

高边开关采用的是集成电荷泵方式的N-Channel MOSFET.

6.1 输出导通电阻

导通电阻 $R_{DS(ON)}$ 主要取决于结温 T_J 。图 15 显示导通电阻在 T_J 温度范围内的变化
在 $T_J = 150^\circ\text{C}$ 时测得的最大 $R_{DS(ON)}$ 是两倍的关系。

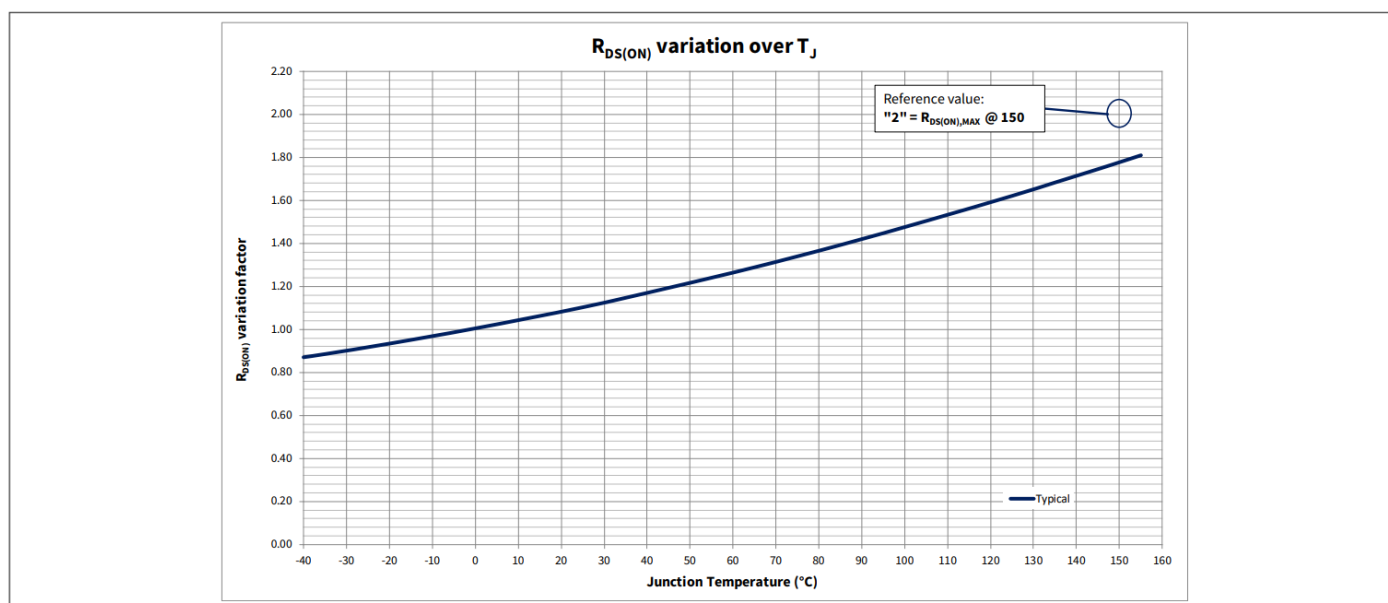


Figure 15 $R_{DS(ON)}$ variation factor

反接的具体表现见 第7.4.1章中描述

6.2 驱动负载

6.2.1 驱动阻性负载

驱动电阻负载时，图 16 中所示的开关时间和转换速率需要考虑。开关能量值 E_{ON} 和 E_{OFF} 与负载阻抗和开关时间 t_{ON} 和 t_{OFF} 成正比。

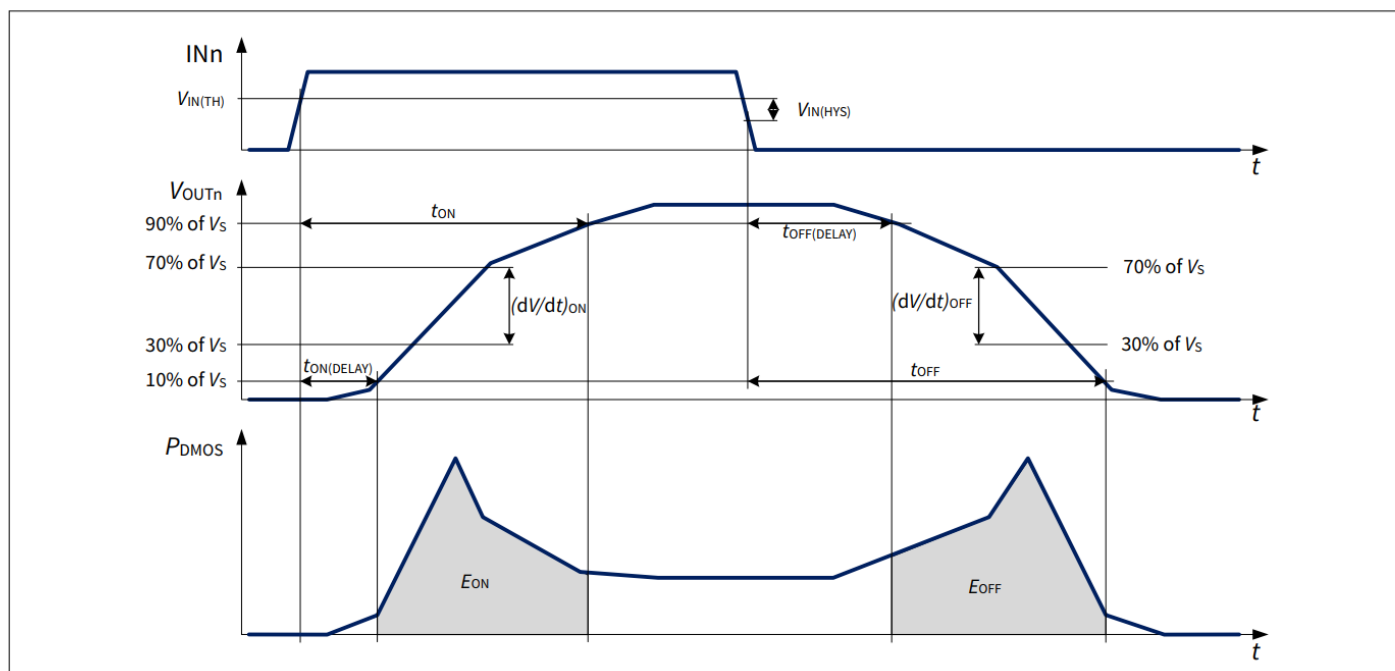


Figure 16 Switching a resistive load

6.2.2 驱动感性负载

当用高边开关关闭感性负载时，电压 V_{OUT} 会降至地电位以下，因为通过电感的电流不能瞬间变化。为了防止器件因过压而损坏，采用了电压钳位机制。钳位机制将限制输出电压，使得 $V_{DS} \leq V_{DS(CLAMP)}$ 。第6.2.2为钳位结构示意图。

在所有工作模式下5.1，钳位结构都起作用。

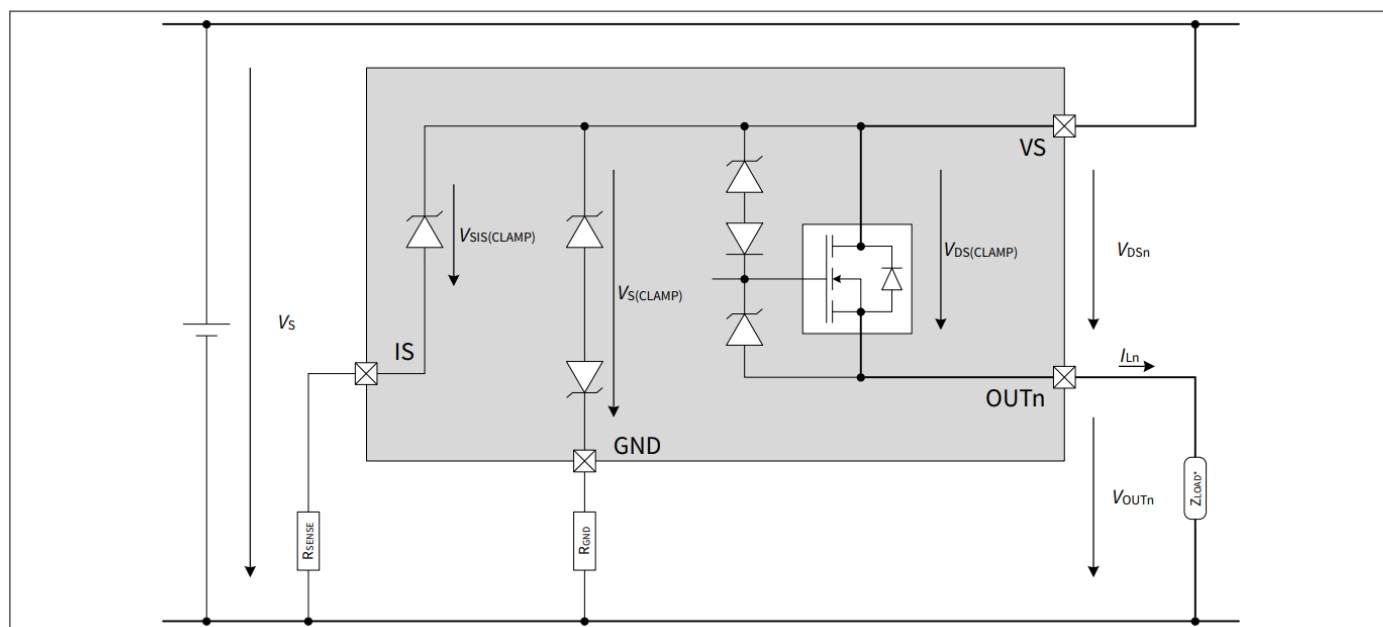


Figure 17 Output clamping concept

在感性负载退磁过程中，热量在器件中耗散。热量计算公式如下：

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln \left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

器件能承受的最大能量受热限制，请参考表2 最大允许值为 E_{AS} （单脉冲能量）和 E_{AR} （重复的能量）。

6.2.3 驱动容性负载

当 IN 控制信号频率为 $f_{VIN(CLS)}$ 时，器件在 $t_{ON_CLS(DELAY)}$ 之后进入 CLS 模式，如图 18 所示。当过流保护触发，容性负载进入 Pumping 模式充电，如图 19 所示。在 CLS 模式下，保护和诊断功能仍是激活的。

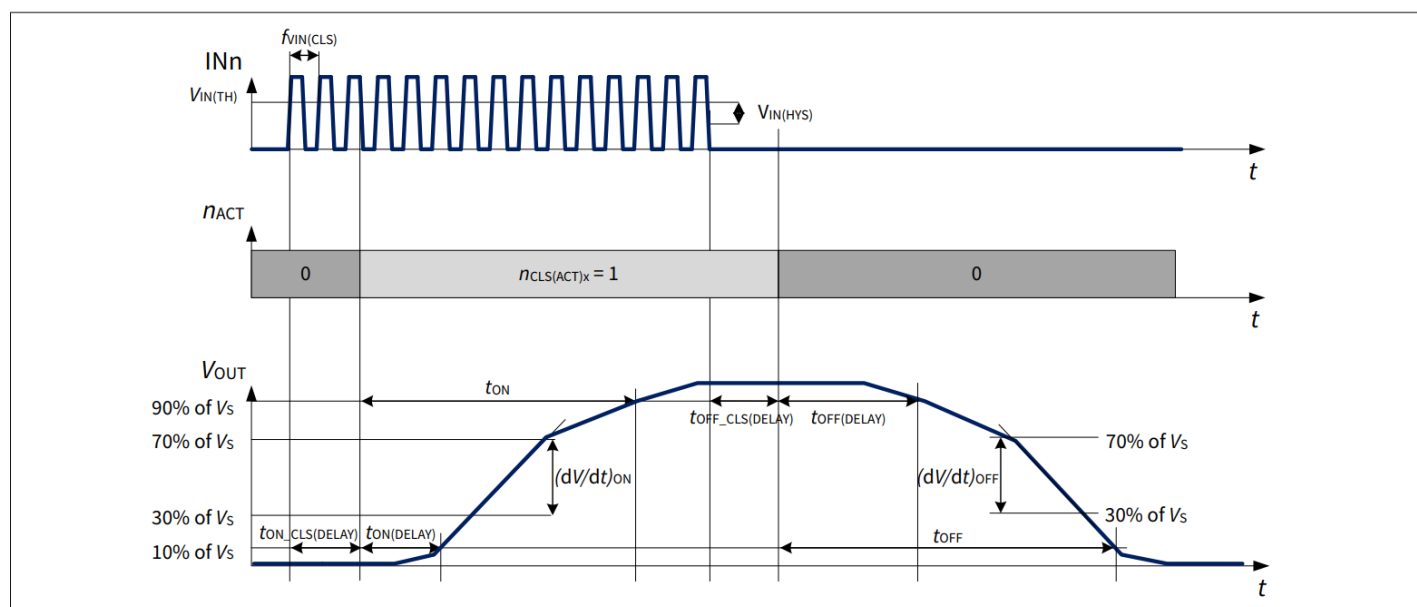


Figure 18 Switching a capacitive load

当器件处于 CLS 模式时，动态过温保护阈值降低至 $T_{J(DYN_CLS)}$ 并支持自动重启。

当 $V_{DS} \leq V_{DS(OLOFF)}$ 时，自动从 CLS 模式切换到 Active 模式。

当 $V_{DS} > V_{DS(OLOFF)}$ 时，并且芯片进入 CLS 模式超过 t_{CLSx} 时间，需要设置输出为“低电平”或“高电平”，使得芯片退出 CLS 模式。

仅当输出无短路时，才能执行从 capacitive load switching 模式切换到 active 模式。为了区分短路和正常连接，在退出 Capacitive load switching 模式前，需要进行负载电流采样。如果负载电流采样正常，则可以从 Capacitive load switching 模式切换到 Active 模式。如果负载电流采样为无负载电流，则输出可能是开路或者短路。此外，也可以通过检测输出电压确定输出是否短路。

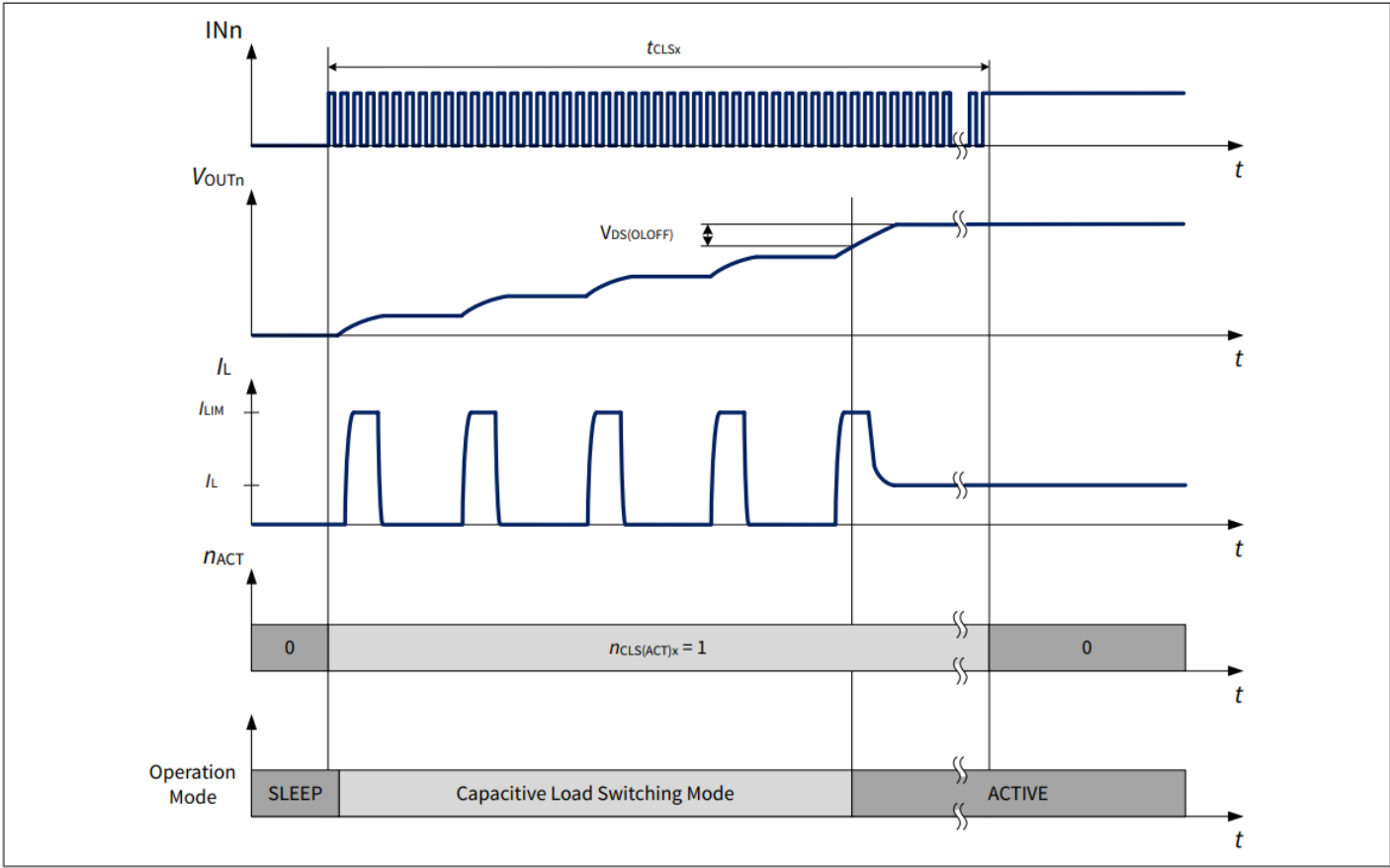


Figure 19 Capacitive load switching activations

6.3 开关特性

6.3.1 Inverse current特性

当 $V_{OUT} > V_S$ 时，电流 $I_{L(INV)}$ 流入功率输出管（见图 20）。这种条件被称为“inverse current”。
如果通道处于关闭状态，电流流入芯片体二极管，将产生能量耗散，因此，器件温度升高。由于过温，可能导致另外的通道关闭。如果通道处于打开状态，则导通阻抗为 $R_{DS(INV)}$ ，在芯片的耗散功率和 $R_{DS(ON)}$ 的耗散功率类似。

在inverse current条件下，只要 $|-I_L| < |-I_{L(INV)}|$ ，通道就会保持打开或关闭状态。

只要 $|-I_L| < |-I_{L(INV)}|$ 条件下，InverseON的功能允许通道打开参见图 21。

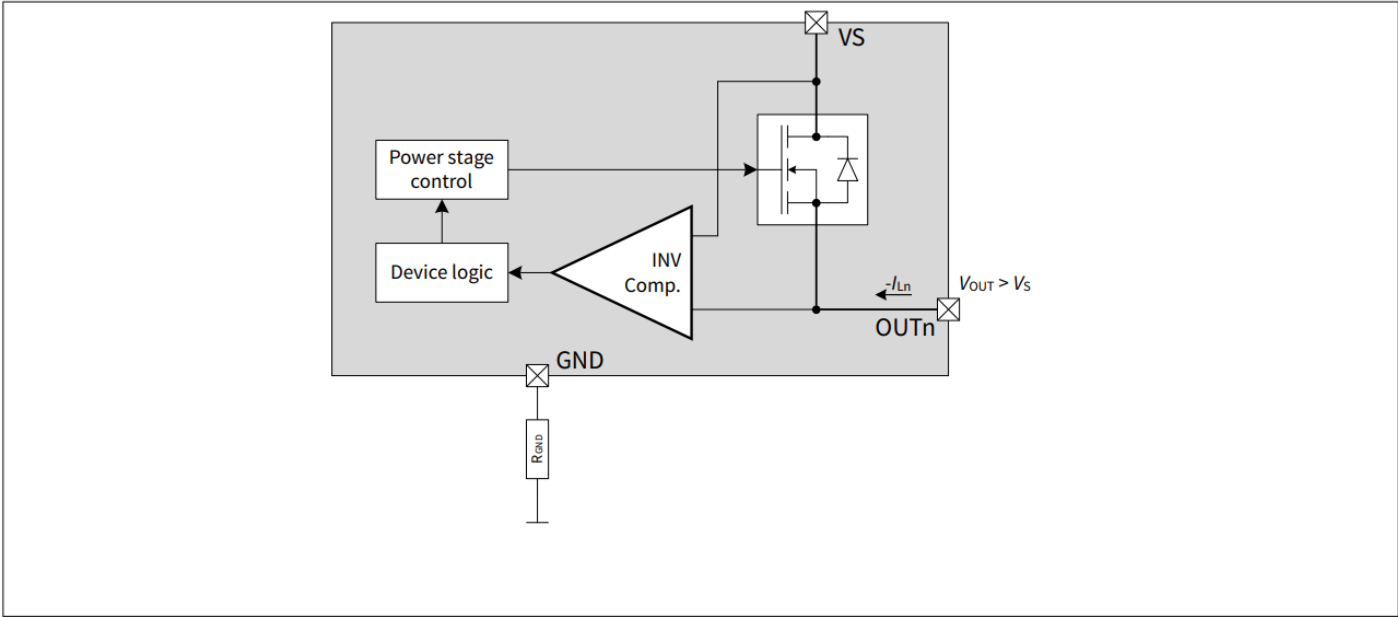


Figure 20 Inverse current circuitry

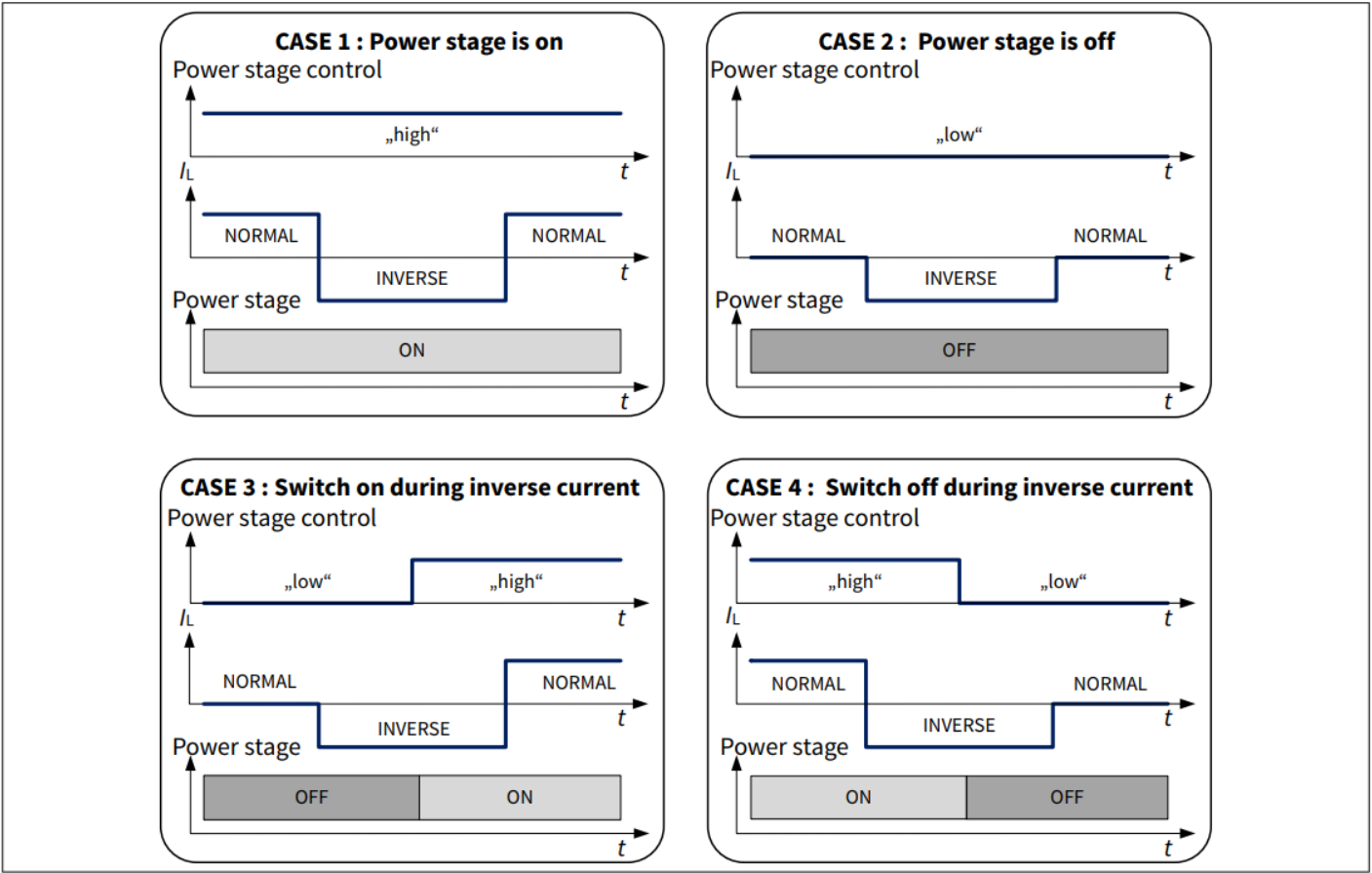


Figure 21 InverseON - Channel behavior in case of applied inverse current

6.4 功率开关电气特性

$V_S = 4\text{ V to }20\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$
Unless otherwise specified typical values: $V_S = 13.5\text{ V}$, $T_J = 25^\circ\text{C}$

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Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL: $R_L = 6.8 \Omega$

Table 8 Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

Voltages

Drain to source clamping voltage at $T_J = -40^\circ\text{C}$	$V_{DS(\text{CLAMP})_{-40}}$	33	36.5	42	V	$I_L = 5 \text{ mA}$ $T_J = -40^\circ\text{C}$ See Chapter 6.2.2	PRQ-110
Drain to source clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{DS(\text{CLAMP})_{25}}$	35	38	44	V	¹⁾ $I_L = 5 \text{ mA}$ $T_J \geq 25^\circ\text{C}$ See Chapter 6.2.2	PRQ-111

Timings

Switch-ON delay	$t_{\text{ON}(\text{DELAY})}$	10	70	130	μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 10\% V_S$ See Figure 16	PRQ-834
Switch-OFF delay	$t_{\text{OFF}(\text{DELAY})}$	10	50	160	μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 90\% V_S$ See Figure 16	PRQ-835
Switch-ON time	t_{ON}	50	130	210	μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 90\% V_S$ See Figure 16	PRQ-836
Switch-OFF time	t_{OFF}	30	100	220	μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 10\% V_S$ See Figure 16	PRQ-837
CLS activation delay	$t_{\text{ON_CLS}(\text{DELAY})}$	10	70	200	μs	$V_S = 13.5 \text{ V}$ See Figure 18	PRQ-838
CLS de-activation delay	$t_{\text{OFF_CLS}(\text{DELAY})}$	20	40	90	μs	$V_S = 13.5 \text{ V}$ See Figure 18	PRQ-839
Switch-ON/OFF Matching - $t_{\text{ON}} - t_{\text{OFF}}$	Δt_{SW}	-60	25	90	μs	$V_S = 13.5 \text{ V}$	PRQ-840

Voltage slope

Switch-ON slew rate	$(dV/dt)_{\text{ON}}$	0.16	0.27	0.39	V/ μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 30\% \text{ to } 70\% \text{ of } V_S$	PRQ-841
Switch-OFF slew rate	$(dV/dt)_{\text{OFF}}$	-0.39	-0.27	-0.16	V/ μs	$V_S = 13.5 \text{ V}$ $V_{\text{OUT}} = 70\% \text{ to } 30\% \text{ of } V_S$	PRQ-842
Slew rate matching - $(dV/dt)_{\text{ON}} + (dV/dt)_{\text{OFF}}$	$\Delta(dV/dt)_{\text{SW}}$	-0.15	0	0.15	V/ μs	$V_S = 13.5 \text{ V}$	PRQ-843

(表格续下页.....)

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Table 8 (continued) Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CLS mode							
Input frequency for capacitive load switching mode activation	$f_{\text{VIN(CLS)}}$	22	30	38	kHz	²⁾ $DC_{\text{VIN(CLS)}} = 50\%$	PRQ-353
Duty cycle for capacitive load switching mode activation	$DC_{\text{VIN(CLS)}}$	30%	50%	70%	–	²⁾ $f_{\text{VIN(CLS)}} = 30 \text{ kHz}$	PRQ-354
Maximum time in CLS mode	t_{CLS1}	–	–	25	ms	²⁾ See Chapter 6.2.3	PRQ-355
Maximum time in CLS mode	t_{CLS2}	–	–	90	ms	²⁾ See Chapter 6.2.3	PRQ-813
Maximum number of CLS mode activations	$n_{\text{CLS_ACT1}}$	–	–	500	kcycles	²⁾ See Chapter 6.2.3	PRQ-812
Maximum number of CLS mode activations	$n_{\text{CLS_ACT2}}$	–	–	50	kcycles	²⁾ See Chapter 6.2.3	PRQ-814
输出特性							
ON-state resistance at $T_{\text{J}} = 25^{\circ}\text{C}$	$R_{\text{DS(ON)_{25}}}$	–	90	–	mΩ	²⁾ $T_{\text{J}} = 25^{\circ}\text{C}$	PRQ-121
ON-state resistance at $T_{\text{J}} = 150^{\circ}\text{C}$	$R_{\text{DS(ON)_{150}}}$	–	–	180	mΩ	$T_{\text{J}} = 150^{\circ}\text{C}$ $I_{\text{L}} = 1 \text{ A}$	PRQ-122
ON-state resistance in cranking at $T_{\text{J}} = 150^{\circ}\text{C}$	$R_{\text{DS(ON)_{CRANK_{150}}}}$	–	–	200	mΩ	$T_{\text{J}} = 150^{\circ}\text{C}$ $V_{\text{S}} = 3.1 \text{ V}$ $I_{\text{L}} = 0.5 \text{ A}$	PRQ-124
ON-state resistance in inverse current at $T_{\text{J}} = 25^{\circ}\text{C}$	$R_{\text{DS(INV)_{25}}}$	–	90	–	mΩ	²⁾ $T_{\text{J}} = 25^{\circ}\text{C}$ $V_{\text{S}} = 13.5 \text{ V}$ $I_{\text{L}} = -1 \text{ A}$ See Figure 20	PRQ-131
ON-state resistance in inverse current at $T_{\text{J}} = 150^{\circ}\text{C}$	$R_{\text{DS(INV)_{150}}}$	–	–	200	mΩ	$T_{\text{J}} = 150^{\circ}\text{C}$ $V_{\text{S}} = 13.5 \text{ V}$ $I_{\text{L}} = -1 \text{ A}$ See Figure 20	PRQ-132
Nominal load current per channel (all channels active) at $T_{\text{A}} = 85^{\circ}\text{C}$	$I_{\text{L(NOM)_{85}}}$	–	2	–	A	²⁾ $T_{\text{A}} = 85^{\circ}\text{C}$ $T_{\text{J}} \leq 150^{\circ}\text{C}$	PRQ-134

(表格续下页.....)

Table 8 (continued) Electrical characteristics power stage

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output leakage current at $T_J \leq 85^\circ\text{C}$	$I_{L(\text{OFF})_85}$	–	0.01	0.5	μA	2) $V_{\text{OUT}} = 0\text{ V}$ $I_{\text{Nn}} = \text{"low"}$ $T_A \leq 85^\circ\text{C}$	PRQ-136
Output leakage current at $T_J = 150^\circ\text{C}$	$I_{L(\text{OFF})_150}$	–	1.2	4	μA	$V_{\text{OUT}} = 0\text{ V}$ $I_{\text{Nn}} = \text{"low"}$ $T_A = 150^\circ\text{C}$	PRQ-137
Inverse current capability	$I_{L(\text{INV})}$	–	2	–	A	2) $V_S < V_{\text{OUT}}$ $I_{\text{Nn}} = \text{"high"}$ see Figure 20	PRQ-139

Voltages

Drain source diode voltage	$ V_{\text{DS(DIODE)}} $	–	550	700	mV	$I_L = -190\text{ mA}$ $T_J = 150^\circ\text{C}$	PRQ-141
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Switching energy

Switch-ON energy	E_{ON}	–	0.75	–	mJ	2) $V_S = 20\text{ V}$ See Chapter 6.2.1	PRQ-142
Switch-OFF energy	E_{OFF}	–	0.85	–	mJ	2) $V_S = 20\text{ V}$ See Chapter 6.2.1	PRQ-144

1) Tested at $T_J = 150^\circ\text{C}$

2) Not subject to production test - specified by design

7 保护措施

该器件具有过流保护、过温保护和过压保护。

除睡眠模式外，过温保护和过流保护在所有操作模式下均可运行。在Inverse current工况下，过流保护不激活。

通道发生Inverse current工况下，相应通道的过温保护和过流保护不激活。

过压保护在所有操作模式下都激活。

7.1 过流保护

7.1.1 过流保护阈值

当发生过流或者短路到地时，芯片具有保护功能。

器件提电流钳位功能，该功能保护防止芯片过应力。第一步，通过将电流限制为开关中允许的最大电流（ I_{LIM} ），则将高边开关的瞬时功率维持在安全值。电流钳位独立于 V_{DS} 和 T_J 无关。当高边温升超过器件安全工作环境时，绝对过温和动态过温保护被激活，如图22和图23所示。

7.2 过温保护

该器件为每个通道都集成了绝对过温保护（ $T_{J(ABS)}$ ）和动态过温保护（ $T_{J(DYN)}$ ）。

当温度 T_J 超过绝对过温阈值或者动态过温阈值（ $T_{J(ABS)}$ 或 $T_{J(DYN)}$ ）芯片会关闭过温通道。受影响的通道将尝试自动重启。通道保持关闭状态，直到温度达到表9中所述的重启条件根据

章 7.3.1. 如果自动重启尝试次数超过 $n_{RESTART(CR),TYP}$ ，则受影响的通道将关断以防止损坏。参考如图22和图23所示。

$T_{J(REF)}$ 是动态过温保护的参考温度。

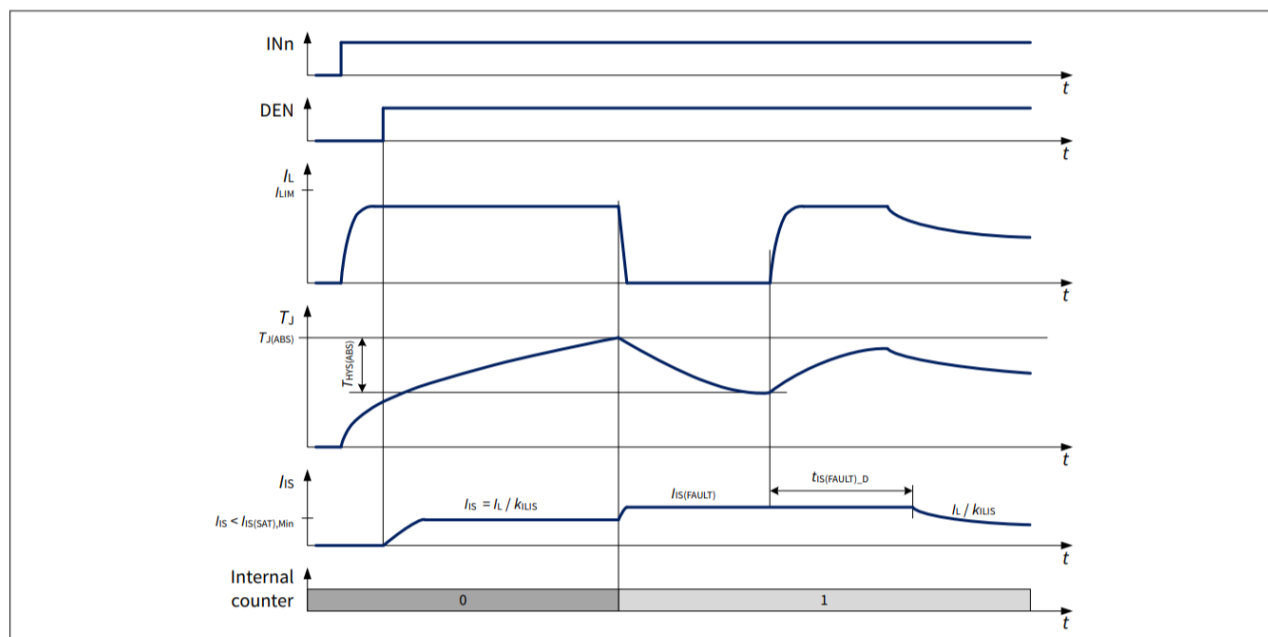


Figure 22 Overtemperature protection (absolute)

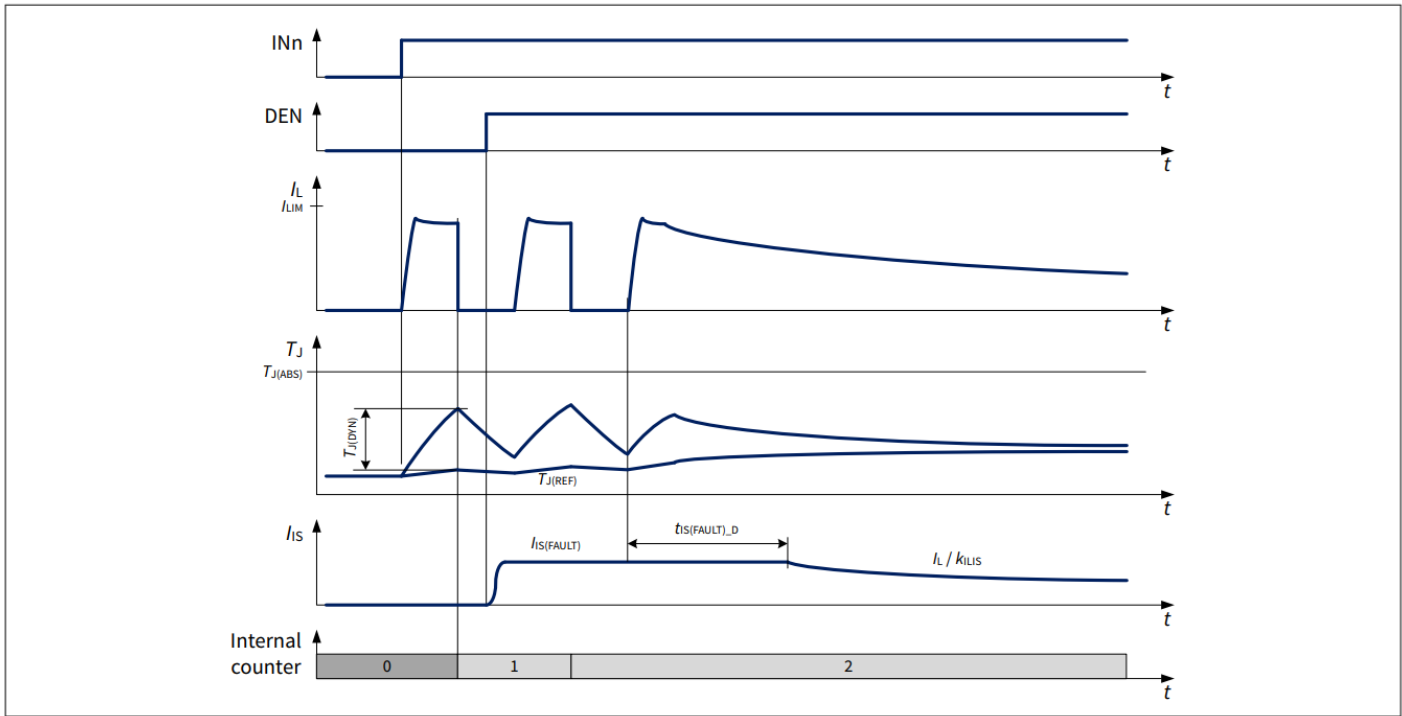


Figure 23 Overtemperature protection (dynamic)

当过温保护电路允许通道再次开启时，重启策略参考Chapter 7.3。

7.3 故障保护与诊断

当发生过温保护后，芯片会进入下面状态：

- 根据 章节7.3.1受影响的通道会关闭
- 如果受影响的通道，诊断是激活的，则 IS 引脚会提供电流 $I_{IS(FAULT)}$ （请参阅 章节 8.2.2 了解更多详细信息）。

如果所有条件满足表 9 中描述的“重启”条件并且 $n_{RESTART(CR)} < n_{RESTART(CR),typ}$ ，则对应通道可再次打开。

Table 9 Protection "restart" condition

Fault condition	Switch OFF event	"Restart" condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)

7.3.1 重启策略

当 INn 置位为“高”时，相关输出通道开启。如果检测到故障，相关输出通道关闭。芯片根据重启策略，相关通道会再次打开，如果故障在 $n_{RESTART(CR),TYP}$ 之后仍然存在，相应通道将关闭锁住。

该器件有一个内部重启计数器 $n_{RESTART(CR)}$ （每个通道一个），以最大限度地提高芯片故障时的鲁棒性。

在关闭之前，允许通道打开 $n_{RESTART(CR)}$ 次。在 $n_{RESTART(CR),TYP}$ 重启次数后，相应通道锁存为 OFF。为了解除输出锁存并清除内部计数器，需要将输入引脚设置为“低电平”，持续时间长于 $t_{DELAY(CR)}$ 。

如果故障不再存在，并且观察到 $t_{DELAY(CR)}$ ，则器件可以正常运行。如果故障仍然存在，则器件将再次触发重启策略。

重启策略如图24所示。

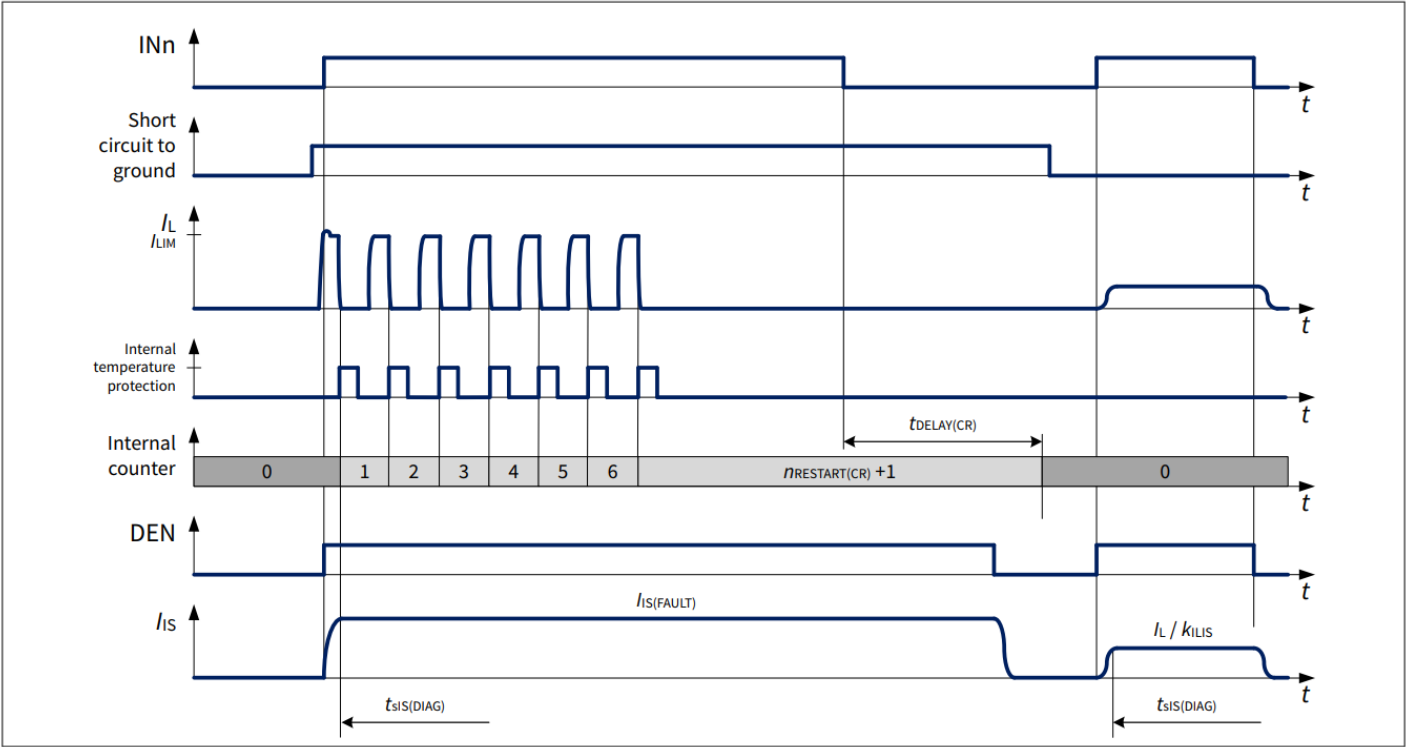


Figure 24 Retry strategy timing diagram

还有一种强制复位，可实现清除内部计数器，并且不需要等待 $t_{\text{DELAY(CR)}}$ 。当IN引脚设置为低电平，施加到DEN引脚的脉冲(能够识别到DEN的上升沿和下降沿)持续时间必须长于 $t_{\text{DEN(CR)}}$ ，以确保内部计数器复位。DSEL引脚必须选择需要解锁的通道，并确保DSEL电平稳定的状态下DEN引脚切换两次（DEN上升沿和下降沿）。

The timings are shown in [Figure 25](#).

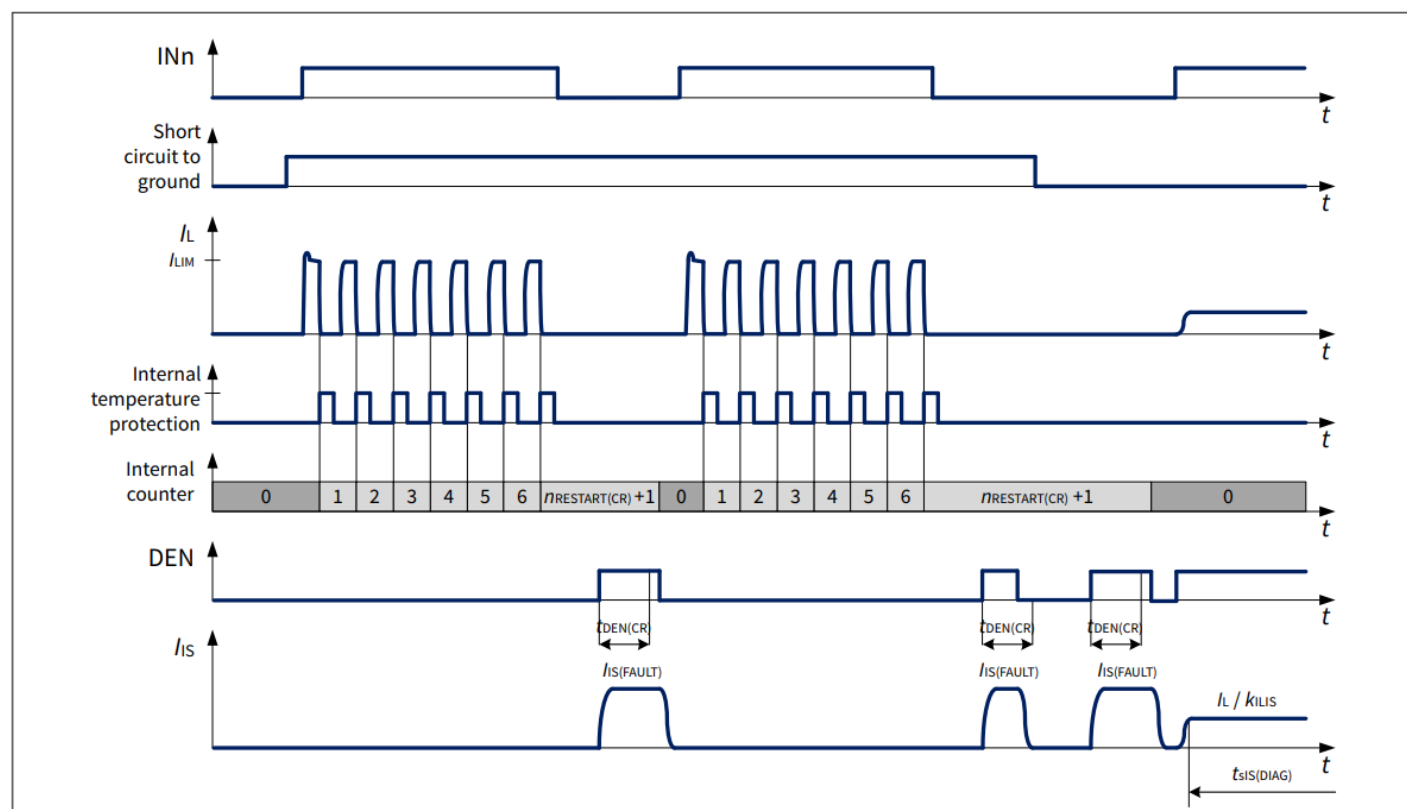


Figure 25 Retry strategy timing diagram with forced reset

7.4 其他保护

7.4.1 反极性保护

在反接条件（也称为反接电池）中，功率耗散主要是有DMOS内部的体二极管引起的。逻辑域的ESD二极管在反接电池的情况下也会产生功率耗散。通过DMOS的反接电流受到所连接负载的限制。通过数字输入引脚的电流受到外接串联电阻的限制（请参阅 表2中列出的绝对最大额定值以及 第9章中的应用信息）。

7.4.2 过压保护

当电源电压介于 $V_{S(EXT,UP)}$ 和 $V_{BAT(LD)}$ 之间时，高边输出仍可运行并跟随输入引脚的指令。

除了 第6.2.2章 中描述针对感性负载的输出钳位之外，还有一个针对逻辑域和输出的过压钳位保护，监控 V_S 和GND引脚之间的电压($V_{S(CLAMP)}$)。

7.4.3 掉电和负载连接断开

只要负载和线束是纯电阻的，掉电或负载连接断开是不会影响器件的鲁棒性。如果驱动感性负载，掉电或者负载连接断开时，感抗中的能量需要处理。

芯片可以承受住负载电流为($I_{L(NOM)_85}$)，上并且线束感抗小于 $10\mu H$ 。

如果应用中负载电流和/或感抗值超过上述定义，则外部的抑制二极管（比如第9章中所示的二极管 D_{Z2} ）需要增加，并且需要注意定义合适的负载电流路径。

7 保护措施

7.4.4 地线丢失

建议在数字输入引脚和MCU控制器件之间连接一个电阻，以确保当地线丢失时，输出通道仍然时关闭状态（如[章节9](#)中所述）。

注：

如果数字输入引脚被拉至地（通过电阻或低电平），当器件地丢失时，有一个寄生回地路径，使得芯片仍可以操作。

7.5 电气特性保护参数

$V_S = 4\text{ V to }20\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values: $V_S = 13.5\text{ V}$, $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL: $R_L = 6.8\ \Omega$

Table 10 Electrical characteristics protection

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown temperature (absolute)	$T_{J(ABS)}$	150	175	200	$^\circ\text{C}$	^{1) 2)} See Figure 22	PRQ-174
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$	–	30	–	K	³⁾ See Figure 22	PRQ-356
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$	–	80	–	K	³⁾ See Figure 22	PRQ-357
Thermal shutdown temperature (dynamic) in capacitive load switching mode	$T_{J(DYN_CLS)}$	–	40	–	K	³⁾	PRQ-177
Power supply clamping voltage at $T_J = -40^\circ\text{C}$	$V_{S(CLAMP)_-40}$	33	36.5	42	V	$I_{VS} = 5\text{ mA}$ $T_J = -40^\circ\text{C}$ See Chapter 6.2.2	PRQ-179
Power supply clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{S(CLAMP)_25}$	35	38	44	V	²⁾ $I_{VS} = 5\text{ mA}$ $T_J \geq 25^\circ\text{C}$ See Chapter 6.2.2	PRQ-184
Automatic restarts in case of fault after counter reset	$n_{RESTART(CR)}$	–	6	–	–	¹⁾ See Figure 24	PRQ-186
Counter reset delay time after fault condition	$t_{DELAY(CR)}$	40	70	100	ms	¹⁾ See Figure 24	PRQ-188
Minimum DEN pulse duration for counter reset	$t_{DEN(CR)}$	50	100	150	μs	³⁾ See Figure 25	PRQ-190

(表格续下页.....)

Table 10 (continued) Electrical characteristics protection

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

过流钳位保护

Overcurrent limitation	I_{LIM}	3.7	4.7	5.7	A	⁴⁾ $V_{DS} = 3\text{ V}$	PRQ-831
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1) Functional test only

2) Tested at $T_J = 150^\circ\text{C}$ only

3) Not subject to production test - specified by design

4) Tested at $T_J = -40^\circ\text{C}$ only

8 诊断

基于诊断需求，芯片在引脚 IS 提供比例检测电流信号 (I_{IS})。如果关闭诊断功能（DEN 引脚置位为“低电平”），IS 引脚为高阻态。

如果使能电流采样诊断功能，则需要在 IS 引脚和模块接地之间连接 检测电阻 R_{SENSE} 。

R_{SENSE} 电阻值必须高于 $820\ \Omega$ （或 如果在总电源上有反接保护，则电阻值必须高于 $400\ \Omega$ ），来限制电流检测电路中的功率耗散。

R_{SENSE} 典型值为 $1.2\text{k}\Omega$ 。

由于 IS 引脚和 V_S 供电之间芯片存在内部连接，如果其他芯片由不同的电池供电，则不建议将 IS 引脚连接到其他芯片的检测电流输出。

See Figure 26 for details as an overview.

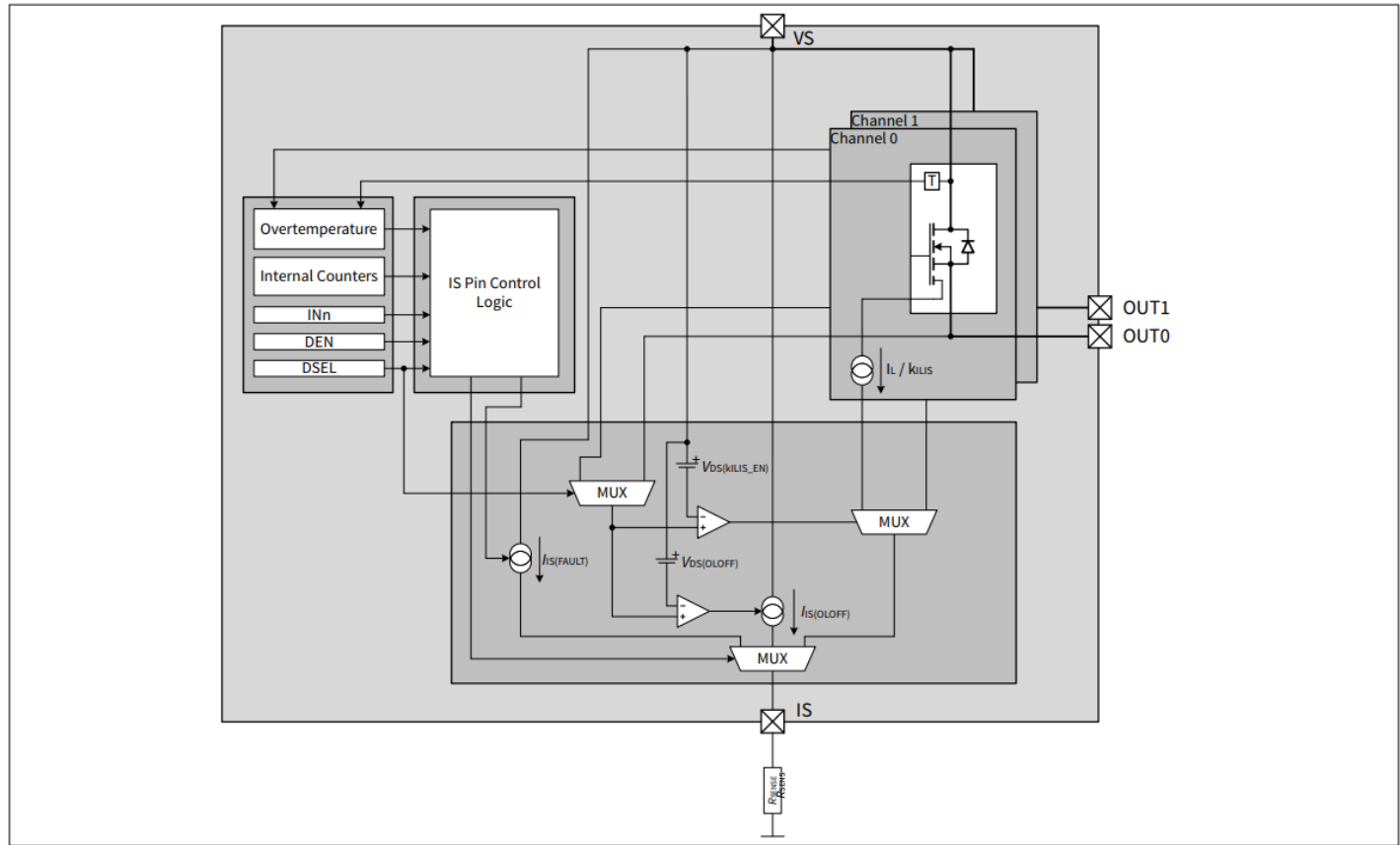


Figure 26 Diagnosis block diagram

8.1 概述

Table 11 gives a quick reference to the state of the IS pin during the device operation.

Table 11 SENSE signal as a function of application condition

Operation mode	Input level	DEN level	V_{OUT}	Diagnostic output
Normal operation	LOW/OFF	HIGH	$\sim$ GND	Z $I_{IS(Fault)}$ if $n_{RESTART(CR)} > 0$
Short circuit to GND			$\sim$ GND	Z $I_{IS(Fault)}$ if $n_{RESTART(CR)} > 0$

(表格续下页.....)

Table 11 (continued) SENSE signal as a function of application condition

Operation mode	Input level	DEN level	V_{OUT}	Diagnostic output
Thermal shutdown temperature (absolute)			Z	$I_{IS(FAULT)}$
Thermal shutdown temperature (dynamic)			Z	$I_{IS(FAULT)}$
Short circuit to V_S			$= V_S$	$I_{IS(OLOFF)}$ $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Open load			$< V_S - V_{DS(OLOFF)}$ $> V_S - V_{DS(OLOFF)}^{1)}$	Z $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$ for both cases
Inverse current	HIGH/ON or CLS		$\sim V_{INV} = V_{OUT} > V_S$	$I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$
Normal operation			$< V_S - V_{DS(KILIS_EN)}$	$I_{IS} = I_L / k_{ILIS}$
Short circuit to GND			$\sim GND$	$I_{IS(FAULT)}$
Thermal shutdown temperature (absolute)			Z	$I_{IS(FAULT)}$
Thermal shutdown temperature (dynamic)			Z	$I_{IS(FAULT)}$
Short circuit to V_S			$= V_S$	$I_{IS} < I_L / k_{ILIS}$
Open load			$\sim V_S^{2)}$	$I_{IS} = I_{IS(EN)}$
Inverse current			$\sim V_{INV} = V_{OUT} > V_S$	$I_{IS} = I_{IS(EN)}$
Current limitation			$< V_S$	$I_{IS(FAULT)}$
Underload			$\sim V_S^{3)}$	$I_{IS(EN)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$
All conditions	n.a.	LOW	n.a.	Z

1) With additional pull up resistor

2) The output current has to be smaller than $I_{L(OL)}$ 3) The output current has to be higher than $I_{L(OL)}$

8.1.1 SENSE 信号真值表

诊断功能可通过 DEN 引脚使能或关闭。通道选择通过 DSEL 引脚根据 表 12 进行。

Table 12 Diagnostic truth table

DEN	DSEL	IS
"low"	not relevant	Z
"high"	"low"	SENSE output 0
"high"	"high"	SENSE output 1

8.2 通道打开时诊断

当以下条件均满足时，IS引脚可提供与负载电流成比例的电流 ($I_{IS} = I_L / k_{ILIS}$)：

- 高边输出打开，并且 $V_{DS} < V_{DS(kILIS_EN)}$
- 通道的诊断是使能的
- 没有故障（如第7.3章所述）或没有故障未清除（请参阅第8.2.2章）了解更多详情）

只要有故障或者故障未清除，IS引脚上电流为 $I_{IS(FAULT)}$ 。

8.2.1 电流采样 (kILIS)

I_{IS} 随 I_L 输出电流线性增加，直至达到饱和电流 $I_{IS(SAT)}$ 。如果高边为负载开路 (I_L 接近 0 A)，则最大检测电流为 $I_{IS(EN)}$ （空载、诊断使能）

如图27所示蓝色为理想的 k_{ILIS} 曲线，另外灰色的曲线为芯片的典型曲线。建议在IS引脚和ADC输入引脚之间增加RC滤波电路，以减少信号纹波和振荡（建议RC滤波电路的最小时间常数为 1 μ s）。 k_{ILIS} 系数的参数特性受到温度、供电电压和制造工艺的影响。

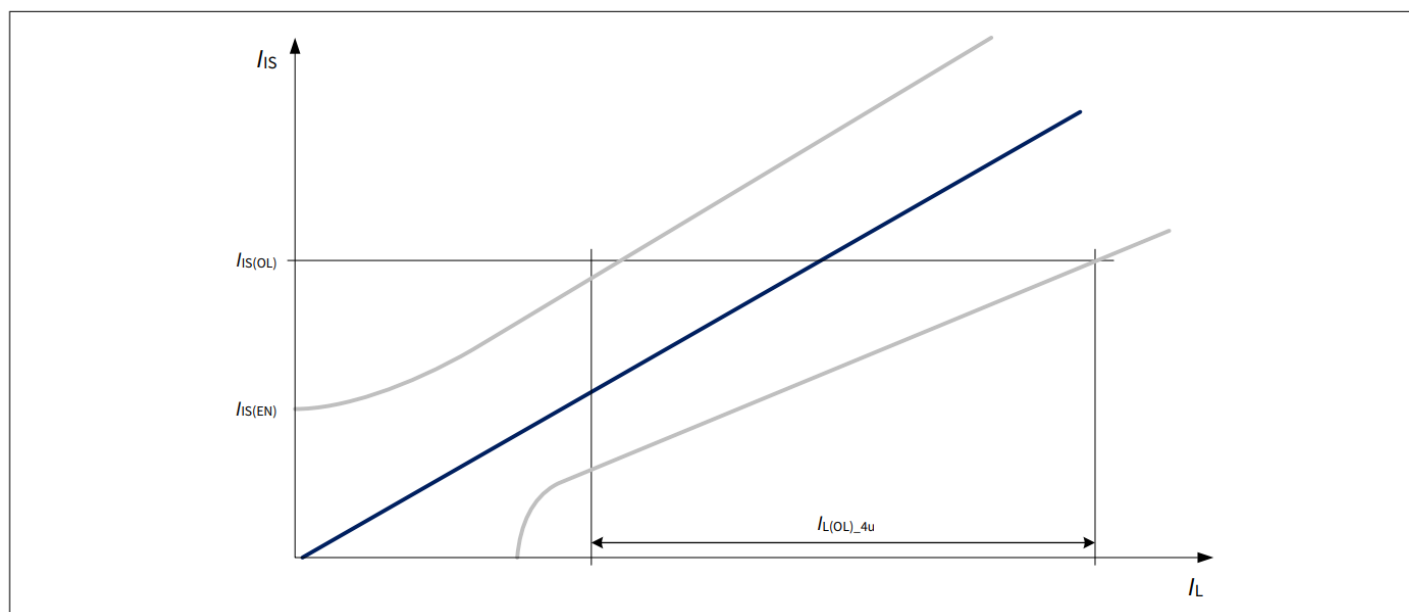


Figure 27 Current sense ratio in open load at ON condition

8.2.2 故障电流($I_{IS(FAULT)}$)

如果出现故障，且DEN置位为“高”，并且受影响的通道由DSEL选定，则IS引脚上电流为 $I_{IS(FAULT)}$ 。可能出现以下情况：

- 如果通道打开，且重启次数小于“ $n_{RESTART(CR),TYP}$ ”，通道允许重启后，IS管脚上电流维持在 $I_{IS(FAULT)}$ ，在时间 $t_{IS(FAULT)_D}$ 时间之后， $I_{IS} = I_L / k_{ILIS}$ （如图28所示）。在重启过程中，每次检测通道诊断时，IS管脚上电流为 $I_{IS(FAULT)}$ 。
- 如果通道打开，且重启次数等于“ $n_{RESTART(CR),TYP}$ ”，通则IS管脚电流 $I_{IS(FAULT)}$ ，为直到内部计数器清零。内部计数器可以通过INn设置为“低电平”并持续 $t_{DELAY(CR)}$ 或通过INn设置为“低电平”和DEN引脚为脉冲，并且脉冲持续 $t_{DEN(CR)}$ 来清零，如第7.3.1章所述。
- 如果通道关闭，内部计数器值未清零时，IS管脚电流为 $I_{IS(FAULT)}$ 。

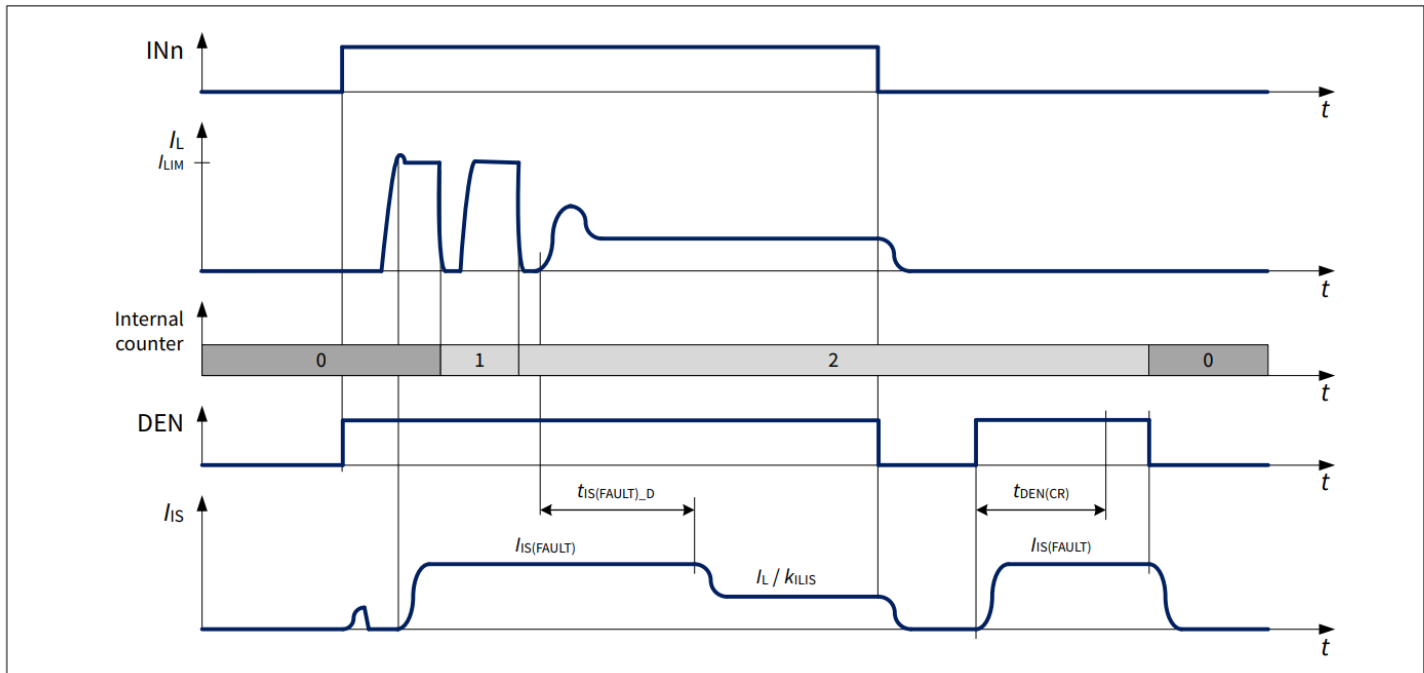


Figure 28 $I_{IS(FAULT)}$ at load switching

Figure 29 adds the behavior of SENSE signal to the timing diagram seen in Figure 24, while Figure 30 shows the relation between $I_{IS} = I_L / k_{ILIS}$, $I_{IS(SAT)}$ and $I_{IS(FAULT)}$.

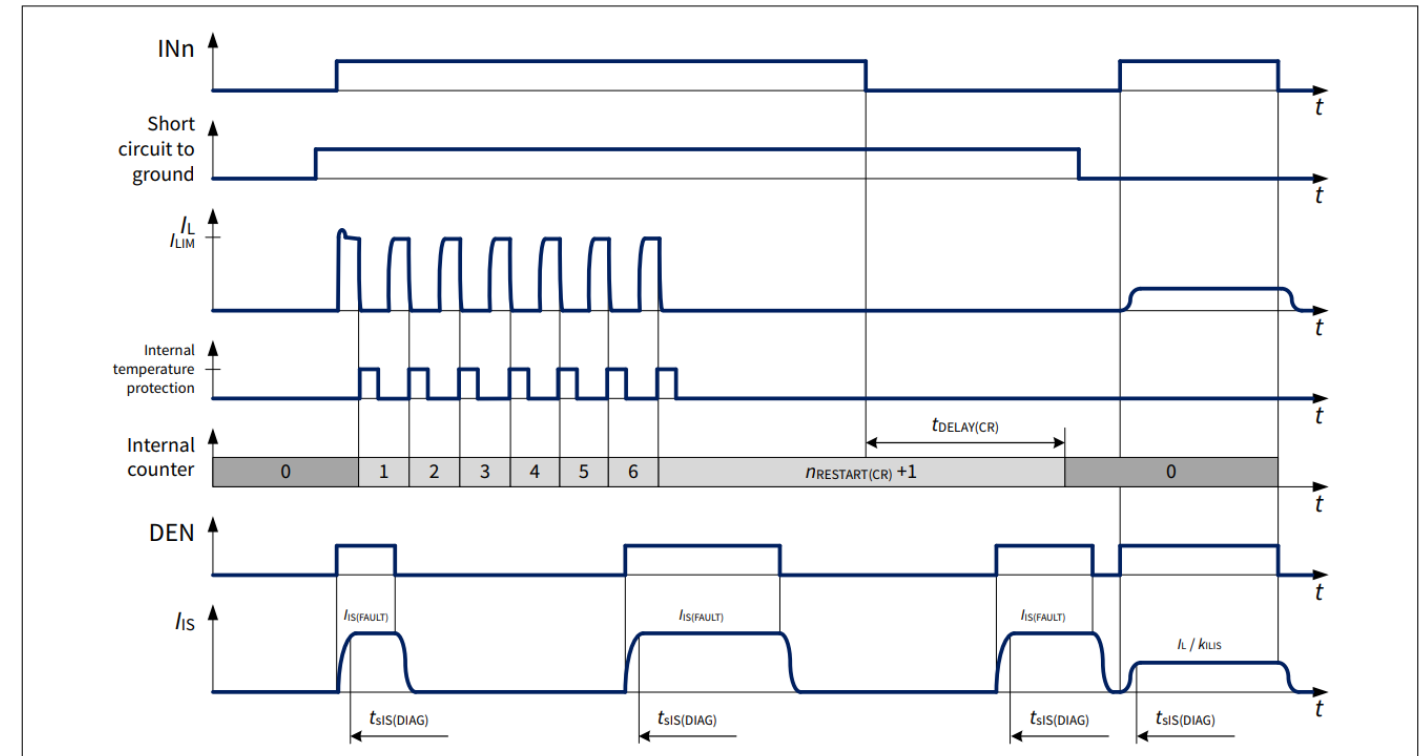


Figure 29 SENSE behavior in fault condition

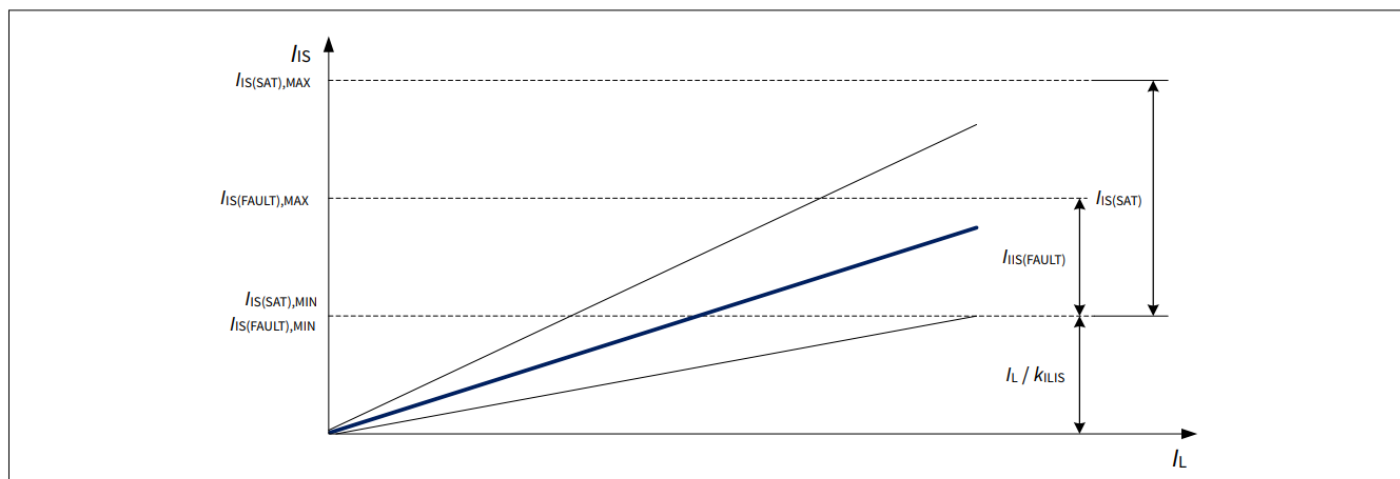
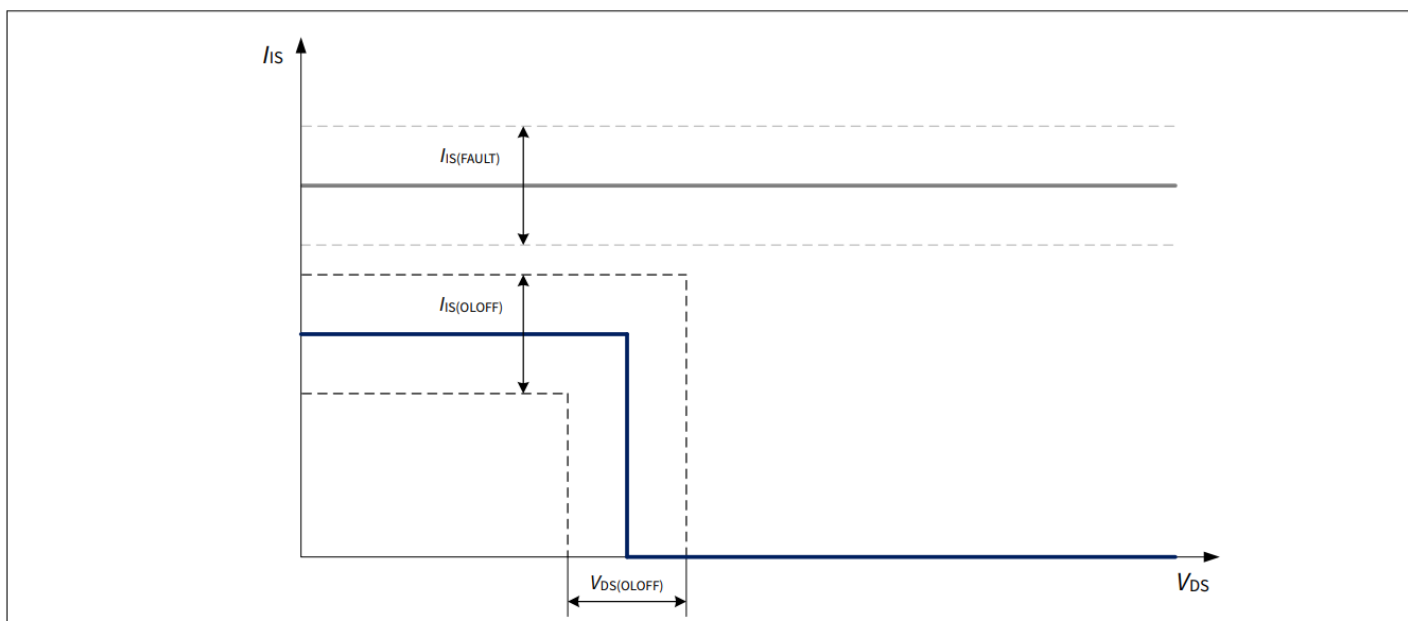


Figure 30 SENSE behavior - overview

8.3 通道关闭时诊断

当通道处于关闭状态，芯片监测输出电压并和内部电压阈值进行比较。基于电压比较器，使用一些外部元件（下拉电阻和可切换的上拉电流源），可检测负载是否丢失或是输出对电源短路。如果芯片检测到故障条件（内部计数器的值与复位值不同，如 [章节8.2.2](#)所述 在重启过程中，通道关闭时，每次检测通道诊断时，IS管脚上电流为 $I_{IS(FAULT)}$ 。

[图 31](#) 显示了在不同 V_{DS} 时， $I_{IS(OLOFF)}$ 和 $I_{IS(FAULT)}$ 的关系。这两个电流不重叠，因此始终可以区分通道关闭情况下负载开路 and 故障状态。

Figure 31 I_{IS} in OFF state

8.3.1 开路负载电流

在通道关闭状态下，当DEN引脚设置为“高”并且使用DSEL引脚对应通道选定时， V_{DS} 电压与阈值电压 $V_{DS(OLOFF)}$ 进行比较。当诊断使能并且 $V_{DS} \leq V_{DS(OLOFF)}$ 时，IS 引脚电流 $I_{IS(OLOFF)}$ 。如果负载正常连接且输出没有对电源短路， V_{DS} 接近 V_S ，因此， $V_{DS} > V_{DS(OLOFF)}$ IS 引脚置位为高阻态。

通道关闭状态下的开路检测，需要在输入引脚的下降沿之后 等待 $t_{IS(OLOFF_D)}$ 时间，IS管脚上才能反馈正确的状态，这段时间主要进行内部比较器的建立。图32 显示负载始终开路，芯片开路检测时序。

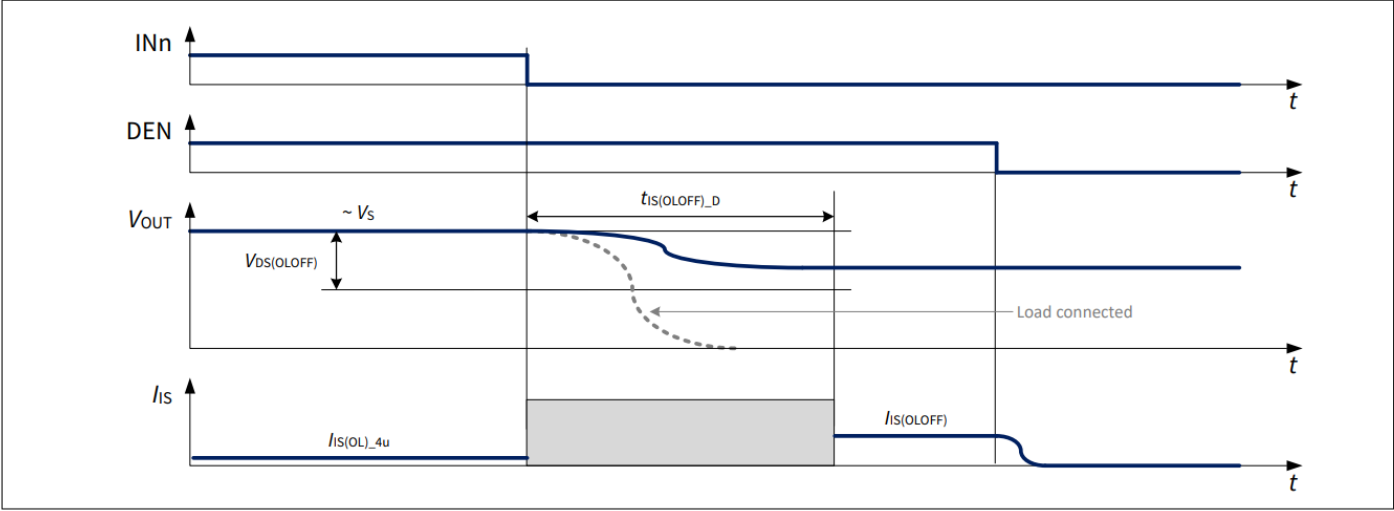


Figure 32 Open load in OFF timings - load disconnection

8.4 诊断时序

图33 和图34表示SENSE的建立 $t_{sIS(ON)}$ 和诊断关掉 $t_{sIS(OFF)}$ 的时序(包括负载变化的情况)。在负载电流稳定之前 (t_{ON} 之前) 无法建立正确的信号，

$$t_{sIS(DIAG)} = t_{sIS(ON)} + t_{ON} \tag{2}$$

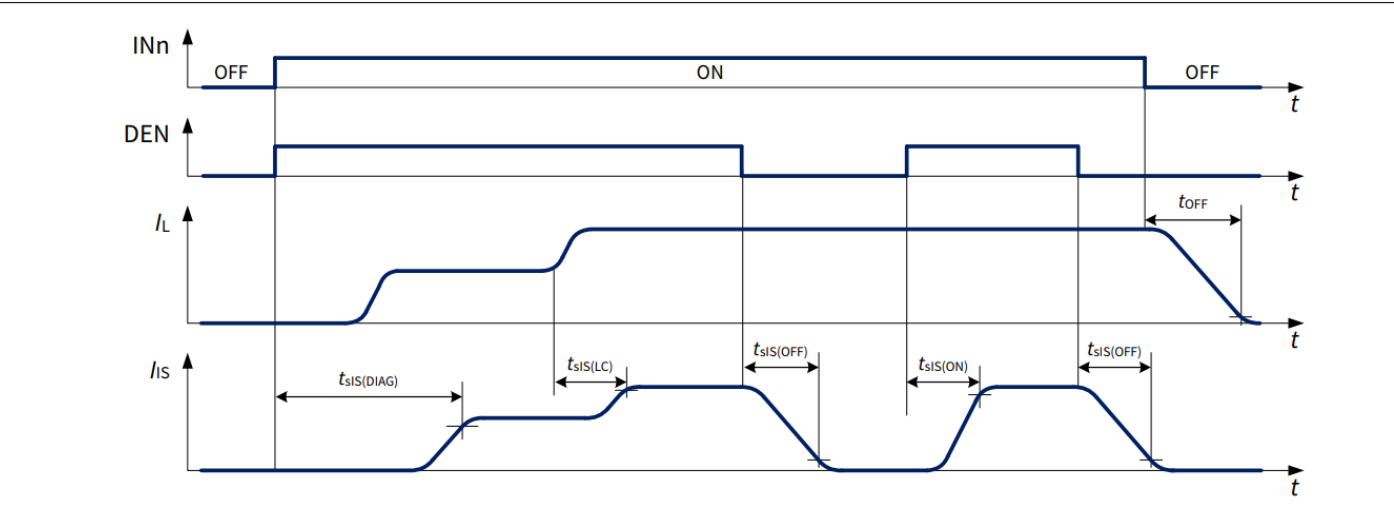


Figure 33 SENSE settling/disabling timing

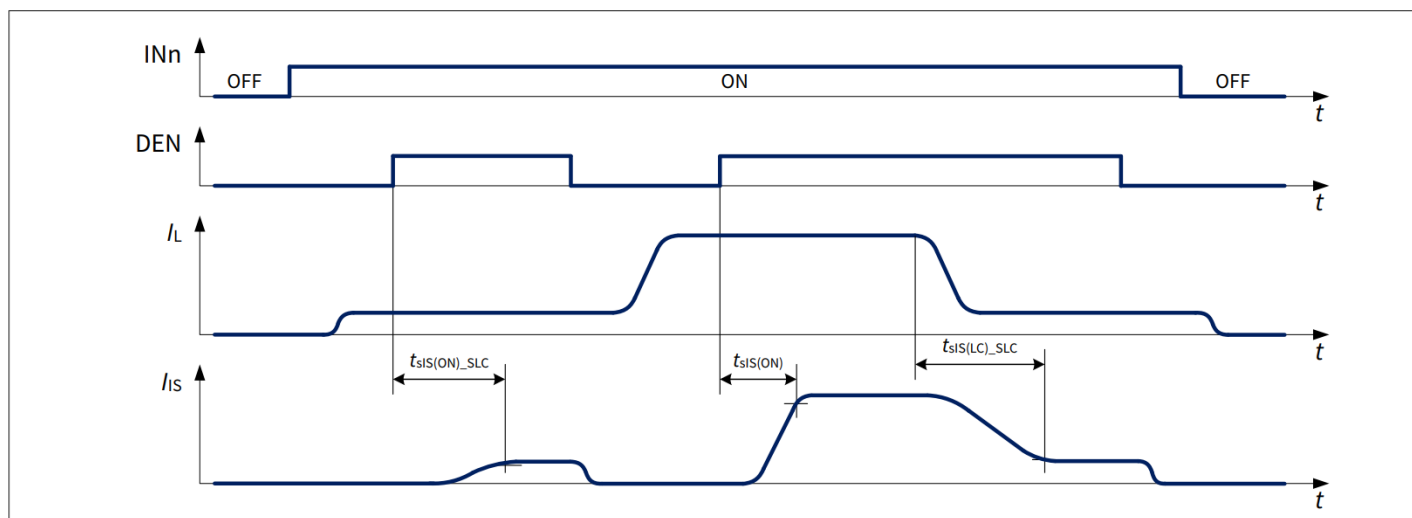


Figure 34 SENSE timing with small load current

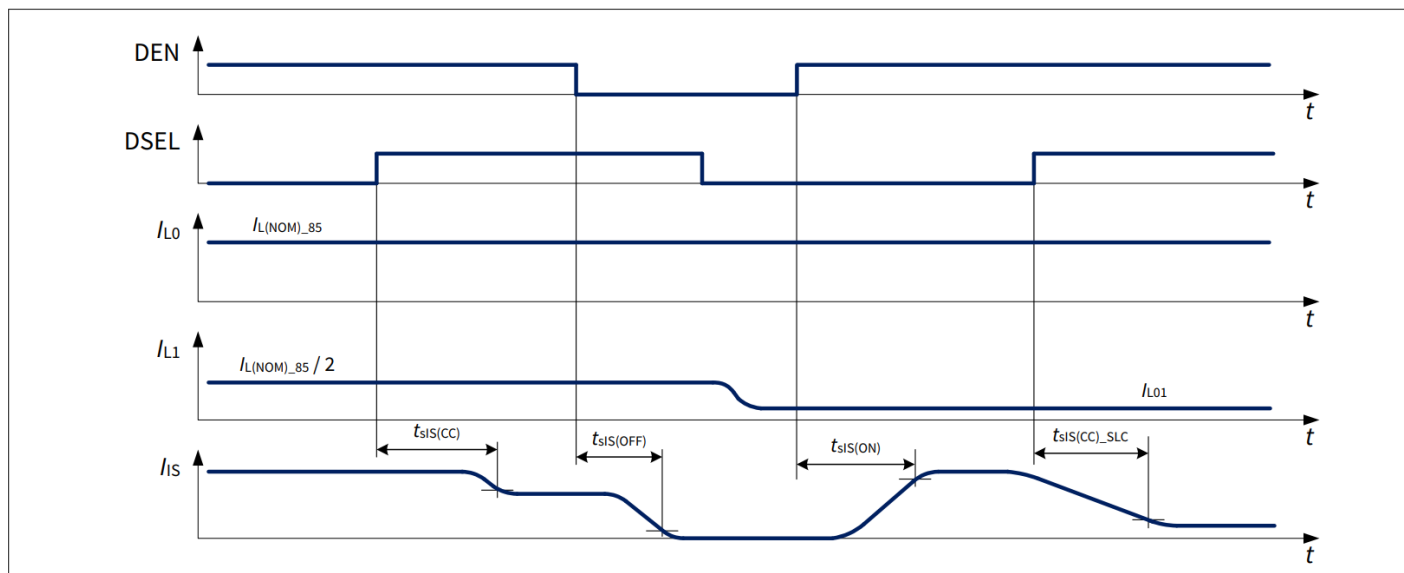


Figure 35 SENSE settling timing - channel change

8.5 诊断电气特性参数

$V_S = 4\text{ V to }20\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values: $V_S = 13.5\text{ V}$, $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTS7090-2EPL: $R_L = 6.8\ \Omega$

Table 13 Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE saturation current	$I_{IS(SAT)}$	4.4	–	15	mA	1) $V_S = 6\text{ V to }20\text{ V}$ $R_{SENSE} = 1.2\text{ k}\Omega$ See Figure 30	PRQ-215
SENSE leakage current when disabled	$I_{IS(OFF)}$	–	0.01	0.5	μA	DEN = "low" $I_L \geq I_{L(NOM)}$ $V_{IS} = 0\text{ V}$	PRQ-219
SENSE leakage current when enabled at $T_J \leq 85^\circ\text{C}$	$I_{IS(EN)_85}$	–	0.2	2	μA	1) $T_J \leq 85^\circ\text{C}$ DEN = "high" $I_L = 0\text{ A}$ See Figure 27	PRQ-221
SENSE leakage current when enabled at $T_J = 150^\circ\text{C}$	$I_{IS(EN)_150}$	–	0.2	2	μA	$T_J = 150^\circ\text{C}$ DEN = "high" $I_L = 0\text{ A}$ See Figure 27	PRQ-223
Saturation voltage in kILIS operation (VS-VIS)	V_{SIS_k}	–	0.5	1	V	1) $V_S = 5\text{ V}$ IN = DEN = "high"	PRQ-226
Saturation voltage in open load at OFF diagnosis (VS-VIS)	V_{SIS_OL}	–	0.5	1	V	1) $V_S = 5\text{ V}$ IN = "low" DEN = "high"	PRQ-682
Saturation voltage in fault diagnosis (VS-VIS)	V_{SIS_F}	–	0.5	1	V	1) $V_S = 5\text{ V}$ IN = "low" DEN = "high" counter > 0	PRQ-684
Power supply to IS pin clamping voltage at $T_J = -40^\circ\text{C}$	$V_{SIS(CLAMP)_-40}$	33	36.5	42	V	$I_{IS} = 1\text{ mA}$ $T_J = -40^\circ\text{C}$ See Chapter 6.2.2	PRQ-294
Power supply to IS pin clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{SIS(CLAMP)_25}$	35	38	44	V	2) $I_{IS} = 1\text{ mA}$ $T_J \geq 25^\circ\text{C}$ See Chapter 6.2.2	PRQ-296
SENSE fault current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	See Chapter 8	PRQ-298

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8 诊断

Table 13 (continued) Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE open load in OFF current	$I_{IS(OLOFF)}$	1.9	2.5	3.5	mA	See Chapter 8	PRQ-306
SENSE delay time at channel switch ON after last fault condition	$t_{IS(FAULT)_D}$	–	500	–	μs	¹⁾ See Figure 28	PRQ-308
SENSE open load in OFF delay time	$t_{IS(OLOFF)_D}$	70	185	300	μs	$V_{DS} < V_{DS(OLOFF)}$ from INn falling edge to $I_{IS} = I_{IS(OLOFF),MIN} \cdot 0.9$ DEN = "high" $n_{RESTART(CR)} = 0$ See Figure 32	PRQ-310
VDS threshold for kILIS enable	$V_{DS(kILIS_EN)}$	0.8	1.2	1.4	V	¹⁾	PRQ-809
Open load VDS detection threshold in OFF state	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	See Chapter 8.3	PRQ-313
SENSE settling time with nominal load current stable	$t_{SIS(ON)}$	–	5	20	μs	$I_L = I_{L(NOM)}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$ See Figure 33	PRQ-315
SENSE settling time with small load current stable	$t_{SIS(ON)_SLC}$	–	–	60	μs	¹⁾ $I_L = I_{L01}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$ See Figure 34	PRQ-317
SENSE disable time	$t_{SIS(OFF)}$	–	5	20	μs	¹⁾ $I_L = I_{L(NOM)}$ From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See Figure 33	PRQ-319
SENSE settling time after load change	$t_{SIS(LC)}$	–	5	20	μs	¹⁾ from $I_L = I_{L(NOM)}/2$ to $I_L = I_{L(NOM)}$ See Figure 33	PRQ-321
SENSE settling time after load change with small load current	$t_{SIS(LC)_SLC}$	–	250	400	μs	¹⁾ DEN = "high" from load change to $I_{IS} = I_L / (k_{ILIS} @ I_L)$ from $I_{L(NOM)}$ to I_{L01} See Figure 34	PRQ-323

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8诊断

Table 13 (continued) Electrical characteristics diagnosis

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE settling time after channel change	$t_{\text{SIS(CC)}}$	–	5	20	μs	1) Start channel: $I_L = I_{L(\text{NOM})}$ End channel: $I_L = I_{L(\text{NOM})}/2$ See Figure 35	PRQ-326
SENSE settling time after channel change with small load current	$t_{\text{SIS(CC)_SLC}}$	–	–	60	μs	1) DEN = “high” from DSEL toggling to $I_{\text{IS}} = I_L / (k_{\text{ILIS,MIN}} @ I_L) \cdot 1.1$ Start channel: $I_L = I_{L(\text{NOM})}$ End Channel: $I_L = I_{L01}$ See Figure 35	PRQ-327
Open load output current at $I_{\text{IS}} = 4 \mu\text{A}$	$I_{L(\text{OL})_4\mu}$	1	4	8	mA	$I_{\text{IS}} = I_{\text{IS(OL)}} = 4 \mu\text{A}$	PRQ-329
Current sense ratio at $I_L = I_{L01}$	k_{ILIS01}	-27%	1100	+27%	–	$I_{L01} = 10 \text{ mA}$	PRQ-333
Current sense ratio at $I_L = I_{L02}$	k_{ILIS02}	-25%	1000	+25%	–	$I_{L02} = 20 \text{ mA}$	PRQ-335
Current sense ratio at $I_L = I_{L04}$	k_{ILIS04}	-24%	1000	+24%	–	$I_{L04} = 50 \text{ mA}$	PRQ-337
Current sense ratio at $I_L = I_{L08}$	k_{ILIS08}	-10%	1000	+10%	–	$I_{L08} = 250 \text{ mA}$	PRQ-341
Current sense ratio at $I_L = I_{L09}$	k_{ILIS09}	-8.8%	1000	+8.8%	–	$I_{L09} = 450 \text{ mA}$	PRQ-342
Current sense ratio at $I_L = I_{L11}$	k_{ILIS11}	-6%	1000	+6%	–	$I_{L11} = 1 \text{ A}$	PRQ-344
Current sense ratio at $I_L = I_{L13}$	k_{ILIS13}	-5%	1000	+5%	–	$I_{L13} = 2 \text{ A}$	PRQ-346

1) Not subject to production test - specified by design

2) Tested at $T_J = 150^\circ\text{C}$

9 应用信息

注： 以下信息仅作为执行器件的提示，不应被视为对器件某种功能、条件或质量的描述或担保。

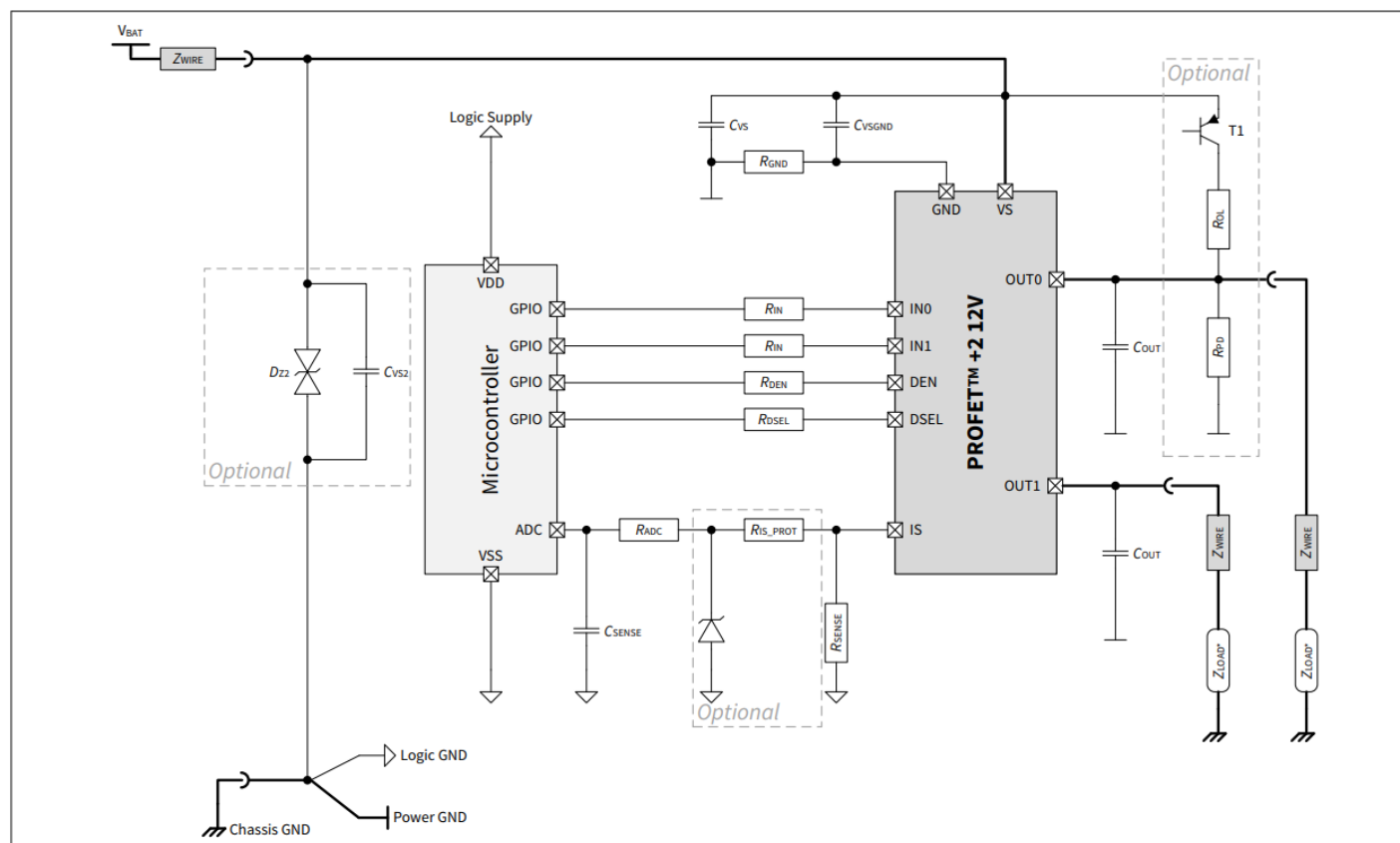


Figure 36 Application diagram

Table 14 Suggested component values

Reference	Value	Purpose
R_{IN}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{DEN}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{DSEL}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground
R_{PD}	47 k Ω	Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis
R_{OL}	1.5 k Ω	Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis
C_{OUT}	10 nF	Protection of the output during ESD events and BCI
T_1	BC 807	Switch the battery voltage for open load in OFF diagnosis
C_{VS}	100 nF	Filtering of voltage spikes on the battery line
C_{VSGND}	47 nF	Buffer capacitor for fast transient

(表格续下页.....)

Table 14 (continued) Suggested component values

Reference	Value	Purpose
D_{Z2}	33V TVS Diode	Transient voltage suppressor diode. Protection during overvoltage and in case of loss of battery while driving an inductive load
C_{VS2}	–	Filtering/buffer capacitor located at VBAT connector
R_{SENSE}	1.2 k Ω	SENSE resistor
R_{IS_PROT}	4.7 k Ω	Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
D_{Z1}	7V Z-Diode	Protection of microcontroller during overvoltage
R_{ADC}	4.7 k Ω	Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications
C_{SENSE}	220 pF	Sense signal filtering. A time constant ($R_{ADC} \cdot C_{SENSE}$) longer than 1 μ s is recommended
R_{GND}	47 Ω	Protection in case of overvoltage and loss of battery while driving inductive loads

- Please contact us for information regarding the pin behavior assessment
- For further information you may contact <http://www.infineon.com>

10 封装外形

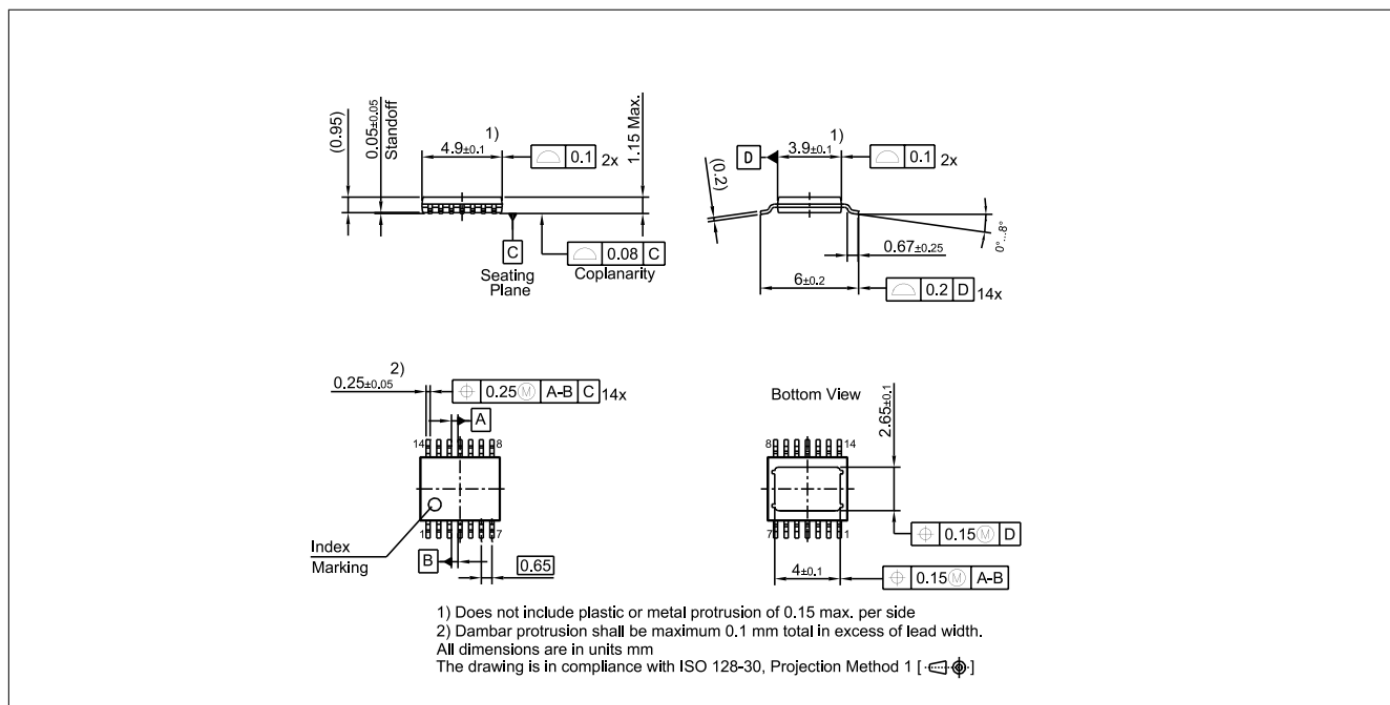


Figure 37 PG-TSDSO-14 dual small outline package dimensions

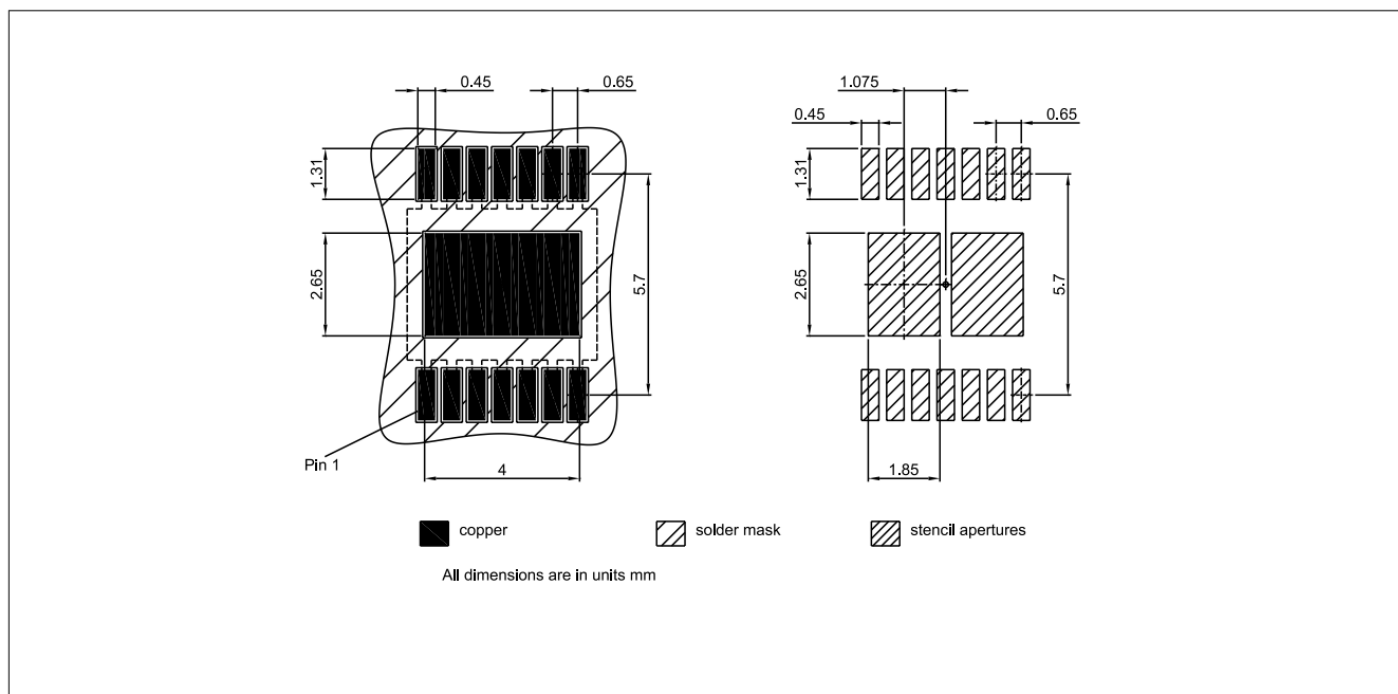


Figure 38 PG-TSDSO-14 dual small outline footprint dimensions

Note: To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages <https://www.infineon.com/packages>

11 修订记录

Table 15 **Revision history**

Document version	Date of release	Description of changes
Rev.1.00	2022-09-20	Initial Datasheet

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