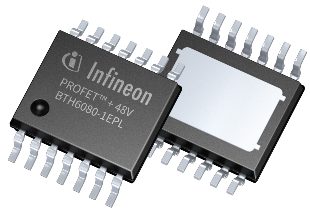
PROFET™ + 48V

Features

- Single channel device
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)



RoHS

AEC Qualified

ISO 26262 ready

Potential applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Suitable for 48 V systems

Product validation

Product validation according to AEC-Q100, Grade 1. Qualified for automotive applications.

Description

The BTH6080-1EPL is a 80 mΩ single channel smart high-side power switch, embedded in a PG-TSDSO-14, exposed pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device offers an adjustable current limitation to offer higher reliability for protecting the system.

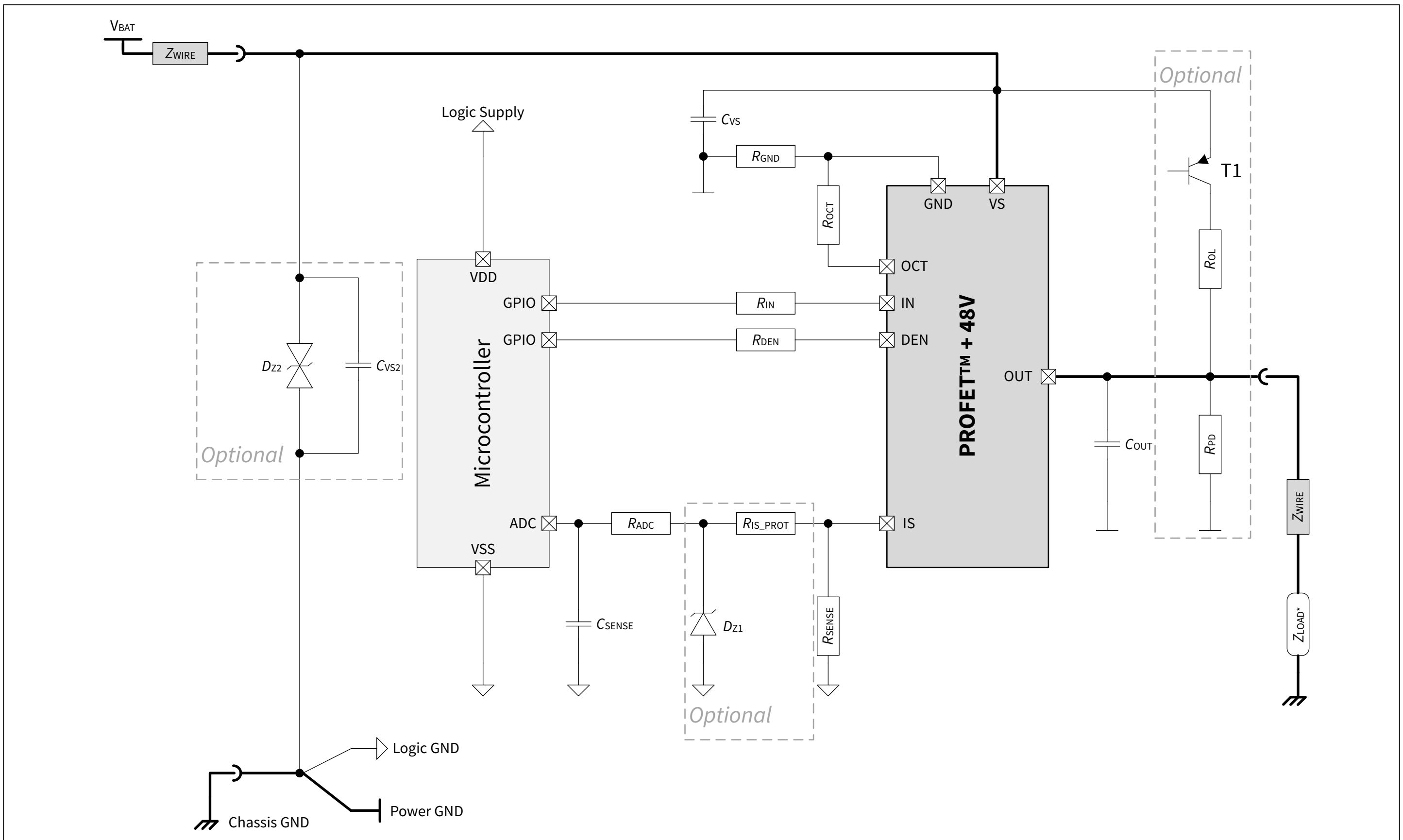


Table 1 **Ordering Information**

Product Name	Package	Marking
BTH6080-1EPL	PG-TSDSO-14	H6080-1P

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1 Product description

Basic features

- High-side power switch with diagnosis and embedded protection
- Adjustable current limitation with OCT pin
- 3.3 V and 5 V compatible logic inputs
- Very low power DMOS leakage current in OFF state
- Logic ground independent from load ground
- Electrostatic discharge protection (ESD)
- Optimized for high immunity against electromagnetic interference (EMI)
- Green product (RoHS compliant)

Protection features

- Stable behavior during undervoltage
- Overtemperature protection with latch
- Overcurrent protection with adjustable overcurrent threshold
- Overvoltage protection with external components
- Secure load turn-OFF during loss of logic ground with external components

Diagnosis features

- Proportional load current sense
- Open load in ON and OFF state
- Short circuit to ground and battery

Table 2 Product summary

Parameter	Symbol	Values
Power supply minimum operating voltage (at switch ON)	$V_{S(OP)}$	5 V
Power supply minimum operating voltage (cranking)	$V_{S(UV)}$	4.1 V
Maximum supply voltage	V_S	60 V
Minimum overvoltage protection ($T_J \geq 25°C$)	$V_{DS(CLAMP)\_25}$	65 V
Typical ON-state resistance ($T_J = 25°C$)	$R_{DS(ON)\_25}$	75 mΩ
Maximum ON-state resistance ($T_J = 150°C$)	$R_{DS(ON)\_150}$	150 mΩ
Nominal load current ($T_A = 85°C$)	$I_{L(NOM)\_85}$	2.5 A
Typical current sense ratio	k_{ILIS}	1250
Adjustable current limitation	I_{LIM}	0.81 A to 5.56 A
Maximum operating current	I_{GND}	3.5 mA

2 Functional block diagram

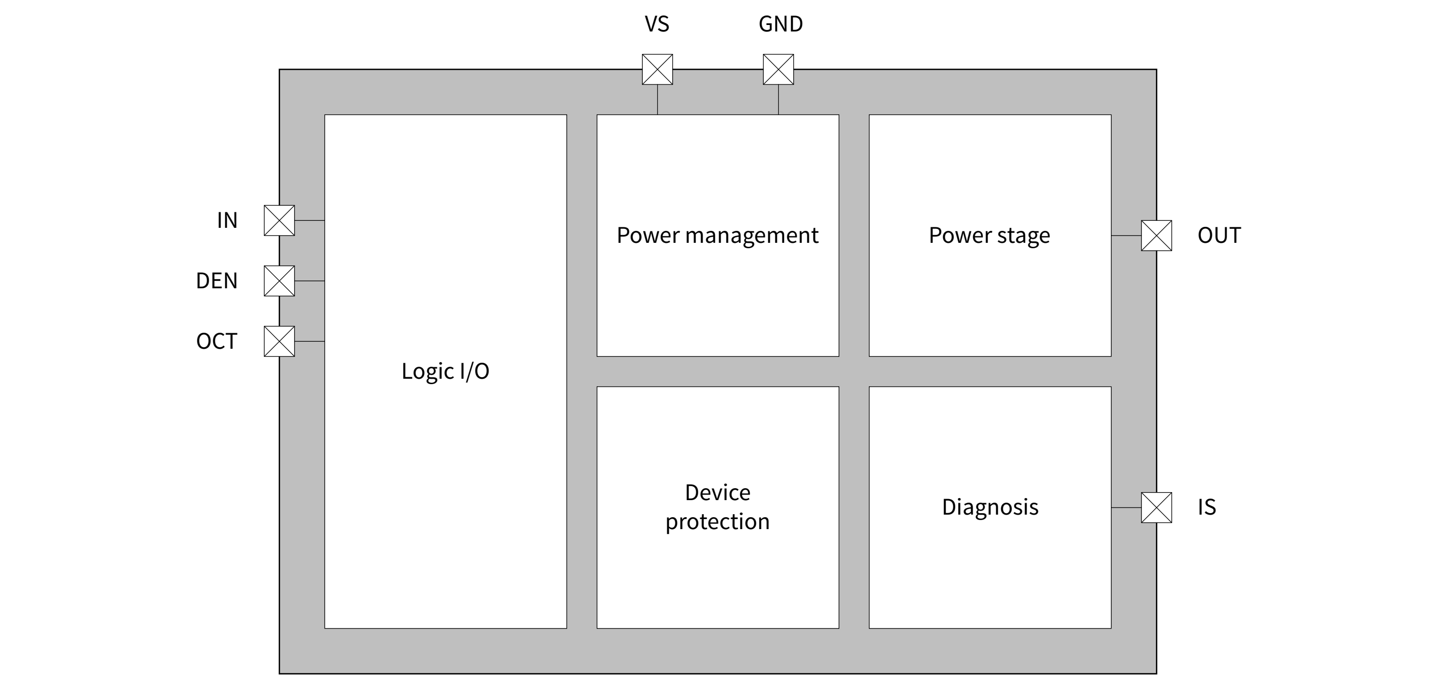


Figure 1 Block diagram

3 Pin configuration

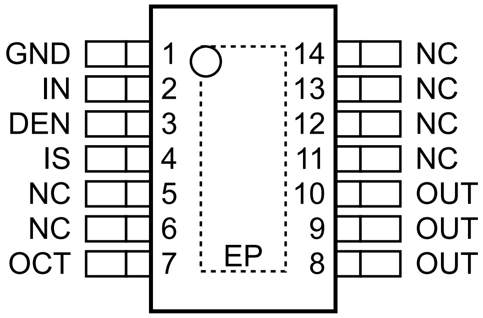


Figure 2 Pin assignment

Table 3 Pin definition and functions

Pin	Symbol	I/O	Function
EP	VS	–	**Voltage supply** Battery voltage
1	GND	–	**Ground** Ground connection
2	IN	I	**Input channel 0** Input signal for channel 0 activation
3	DEN	I	**Diagnostic enable** Digital signal to enable/disable the diagnosis of the device
4	IS	O	**Sense** Sense current of the selected channel
5, 6, 11, 12 13, 14	NC	–	Not connected, internally not bonded
7	OCT	I	**Adjustable overcurrent threshold** A resistor R_{OCT} needs to be connected between OCT pin and GND pin to adjust the overcurrent threshold and must be placed close to the OCT pin
8, 9, 10	OUT	O	**Output** Protected high-side power output channel

The figure below shows all terms used in this datasheet, with associated convention for positive values.

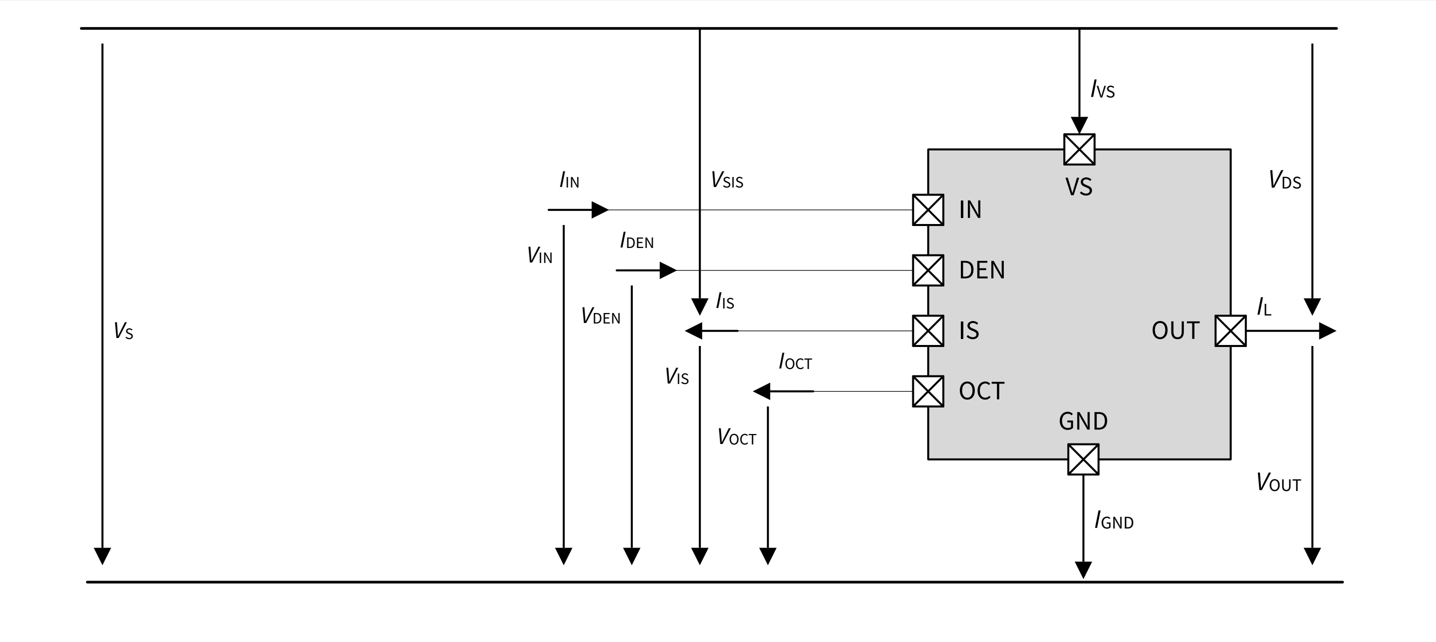


Figure 3 **Voltage and current convention**

4 General product characteristics

4.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

T_J = -40°C to +150°C (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltages							
Supply voltage	V_S	-0.3	–	54	V	–	PRQ-54
Supply voltage - extended	$V_{S(EXT)}$	-0.3	–	60	V	$T_J \leq 125$°C	PRQ-398
Supply voltage - short transients	$V_{S(ST)}$	-0.3	–	81	V	t < 100 µs R_{GND} = 50 Ω R_{LOAD} = 100 Ω	PRQ-378
Supply voltage - moderate transients	$V_{S(MT)}$	-0.3	–	70	V	t < 1 ms R_{GND} = 50 Ω R_{LOAD} = 100 Ω	PRQ-379
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	54	V	Setup acc. to AEC-Q100-012	PRQ-56
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	65	V	Setup acc. to ISO 7637-1 R_I = 2 Ω	PRQ-57
Input pins							
Voltage at INPUT pins	V_{IN}	-0.3	–	6	V	–	PRQ-62
Current through INPUT pins	I_{IN}	-2	–	2	mA	–	PRQ-63
Voltage at DEN pin	V_{DEN}	-0.3	–	6	V	–	PRQ-64
Current through DEN pin	I_{DEN}	-2	–	2	mA	–	PRQ-65
Voltage at DSEL pin	V_{DSEL}	-0.3	–	6	V	–	PRQ-66
Current through DSEL pin	I_{DSEL}	-2	–	2	mA	–	PRQ-67
Sense pin							
Voltage at IS pin	V_{IS}	-0.3	–	–	V	–	PRQ-69
Current through IS pin	I_{IS}	-25	–	50	mA	–	PRQ-70
Power stage							
Maximum energy dissipation single pulse	E_{AS}	–	–	60	mJ	$I_{L(0)} = I_{L(NOM)}$ $T_{J(0)}$ = 150°C V_S = 54 V	PRQ-404
Voltage at power transistor	V_{DS}	–	–	65	V	–	PRQ-75

(table continues...)

Table 4 (continued) Absolute maximum ratings

T_J = -40°C to +150°C (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Currents							
Current through ground pin	I_{GND}	-20	–	20	mA	–	PRQ-77
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-79
Storage temperature	T_{STG}	-55	–	150	°C	–	PRQ-80
ESD susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	[1] HBM	PRQ-164
ESD susceptibility OUT pins vs. GND and VS connected	V_{ESD}	-4	–	4	kV	[1] HBM	PRQ-165
ESD susceptibility	V_{ESD}	-500	–	500	V	[2] CDM	PRQ-166
ESD susceptibility (corner pins)	V_{ESD}	-750	–	750	V	[2] CDM	PRQ-167

1) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002
2) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

T_J = -40°C to 150°C unless otherwise specified.

Table 5 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(NOM)}$	8	48	54	V	–	PRQ-86
Extended upper operating voltage	$V_{S(EXT,UP)}$	54	–	60	V	$T_J \leq 125°C$	PRQ-399
Minimum functional supply voltage	$V_{S(OP)\_MIN}$	3.8	4.3	5	V	1) IN = HIGH From I_{OUT} = 0 A to V_{DS} < 0.5 V	PRQ-88
Undervoltage shutdown	$V_{S(UV)}$	3.0	3.5	4.1	V	1) IN = HIGH DEN = LOW From V_{DS} < 1 V to I_{OUT} = 0 A	PRQ-89
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	–	PRQ-90

1) Test at T_J = -40°C only

Table 6 Current consumption

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operating current channel active	I_{GND}	–	2.5	3.5	mA	IN = HIGH DEN = HIGH Device in $R_{DS(ON)}$ V_S = 54 V	PRQ-248
Standby current for whole device with load (ambient)	$I_{S(OFF)}$	–	0.1	2	µA	1) V_S = 54 V V_{OUT} = 0 V IN = DEN = floating $T_J \leq 85°C$	PRQ-249
Maximum standby current for whole device with load	$I_{S(OFF)\_150}$	–	–	10	µA	V_S = 54 V V_{OUT} = 0 V IN = DEN = floating T_J = 150°C	PRQ-250

(table continues...)

Table 6 (continued) Current consumption

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Maximum standby current for whole device with load	$I_{S(OFF)\_150}$	–	–	50	µA	V_S = 60 V V_{OUT} = 0 V IN = DEN = floating T_J = 150°C	PRQ-251
Standby current for whole device with load, diagnostic active	$I_{S(OFF\_DEN)}$	–	1.3	–	mA	V_S = 54 V V_{OUT} = 0 V IN = floating DEN = HIGH	PRQ-252

1) Test at T_J = -40°C only

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the electrical characteristics tables.*

4.3 Thermal resistance

Table 7 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-top	Ψ_{JTOP}	–	3.7	4.6	K/W	[1]	PRQ-412
Thermal resistance junction-to-case	R_{thJC}	–	4	4.9	K/W	[1] Simulated at exposed pad	PRQ-413
Thermal resistance junction-to-ambient	R_{thJA}	–	37.3	–	K/W	[1]	PRQ-414

1) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W

4.3.1 PCB set-up

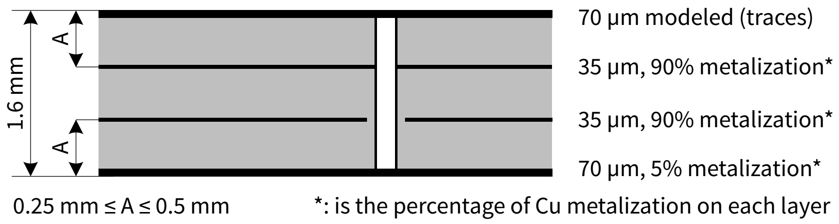


Figure 4 **PCB 2s2p setup**

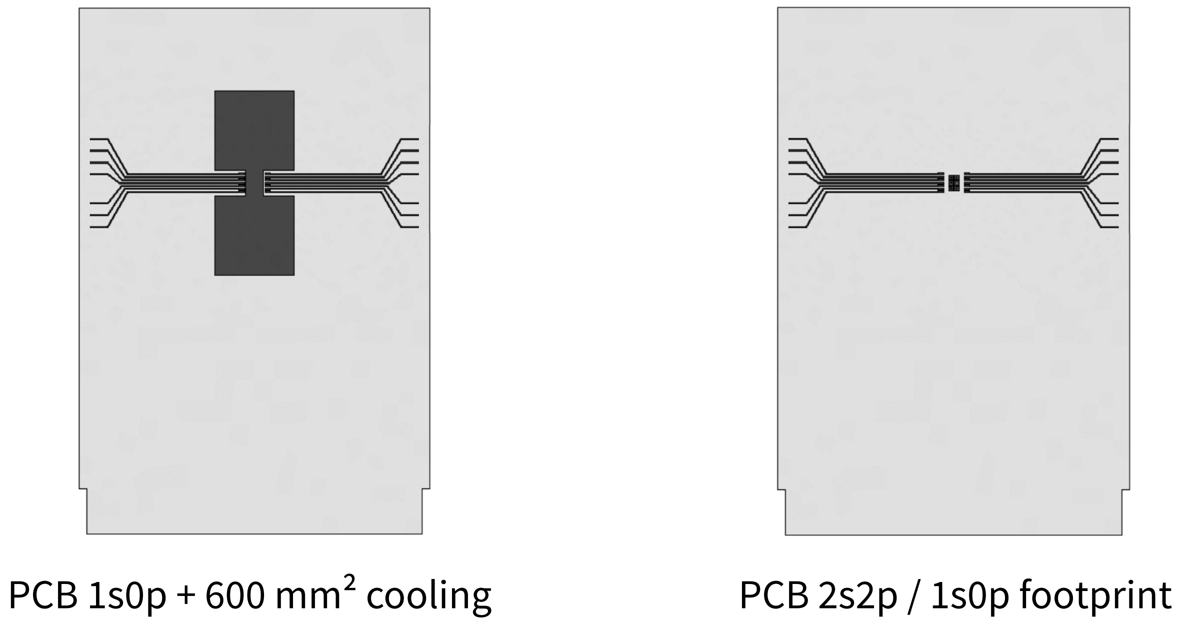


Figure 5 **PCB setup for thermal simulations**

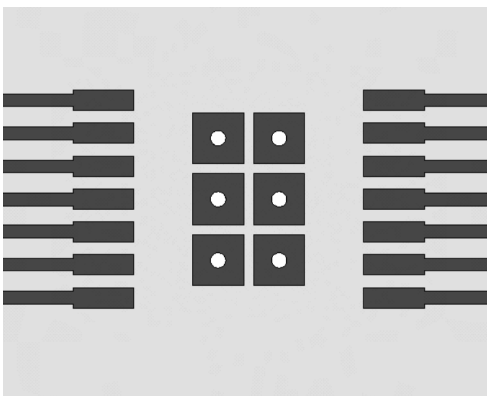


Figure 6 **Thermal vias on PCB for 2s2p PCB setup**

4.3.2 Thermal impedance

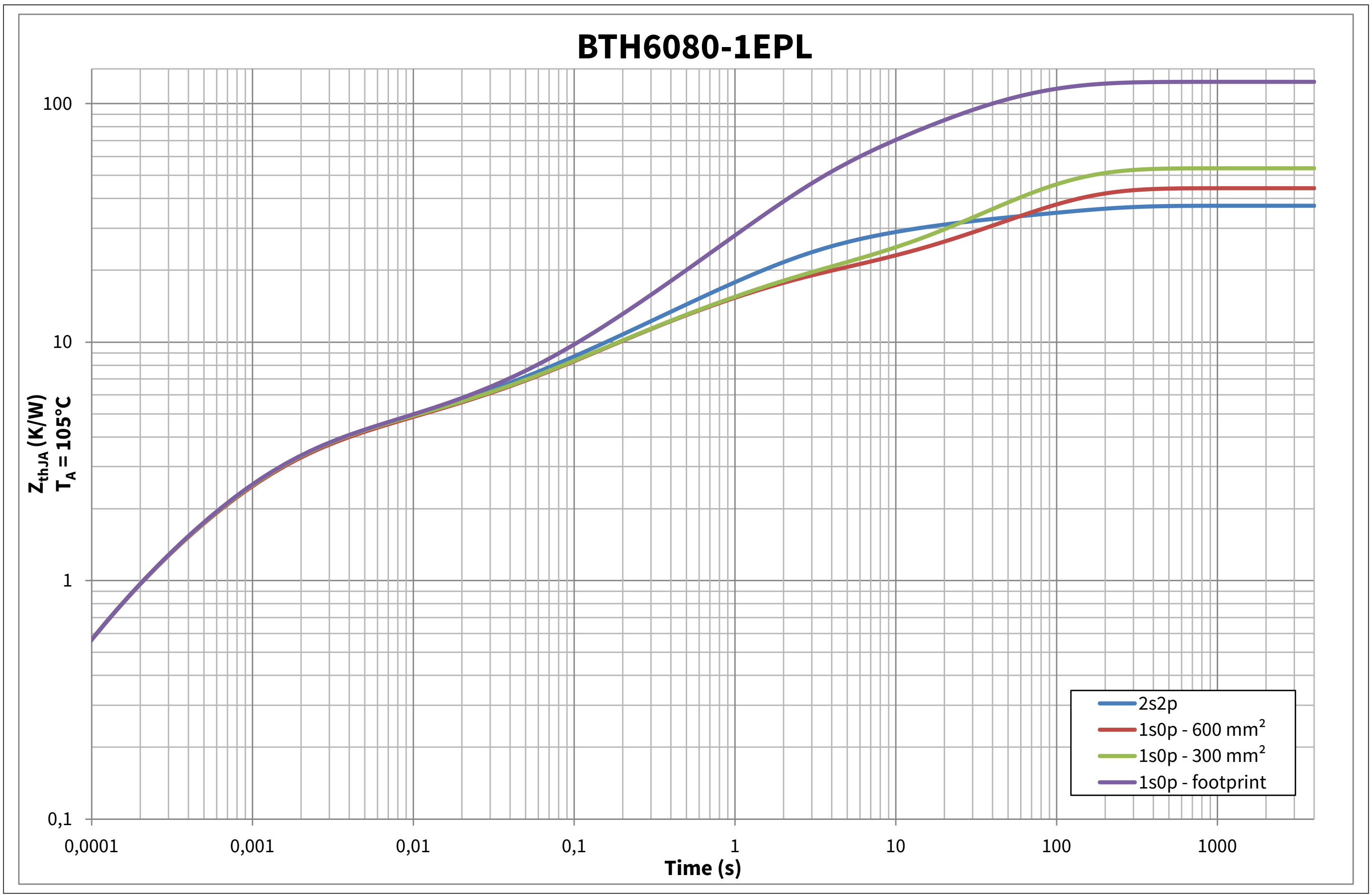


Figure 7 **Typical thermal impedance with different PCB setups**

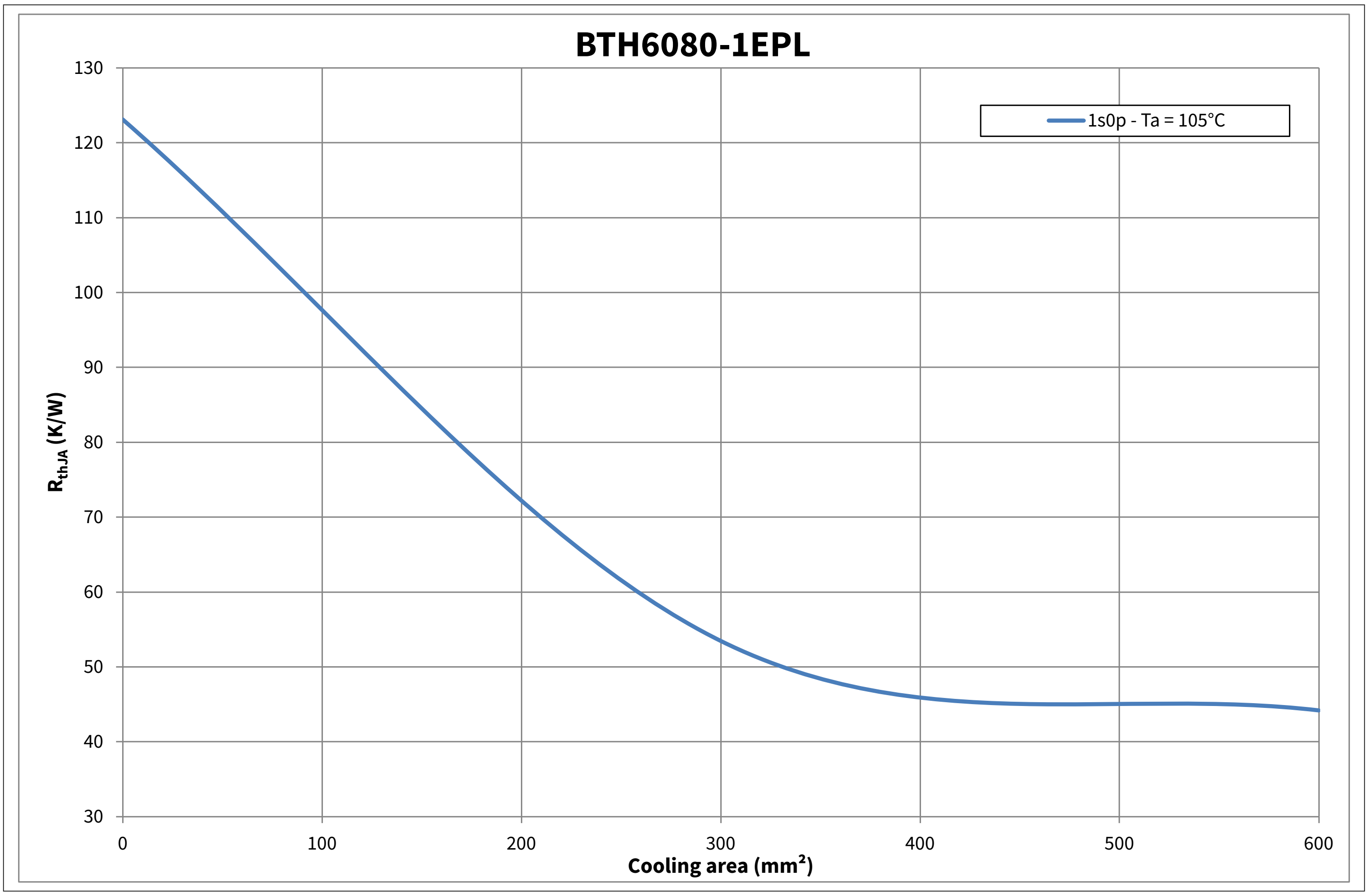


Figure 8 Typical thermal resistance with PCB 1s0p setup and different cooling surfaces

5 Power stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-state resistance

As shown below, the ON-state resistance $R_{DS(ON)}$ mainly depends on the junction temperature T_J.

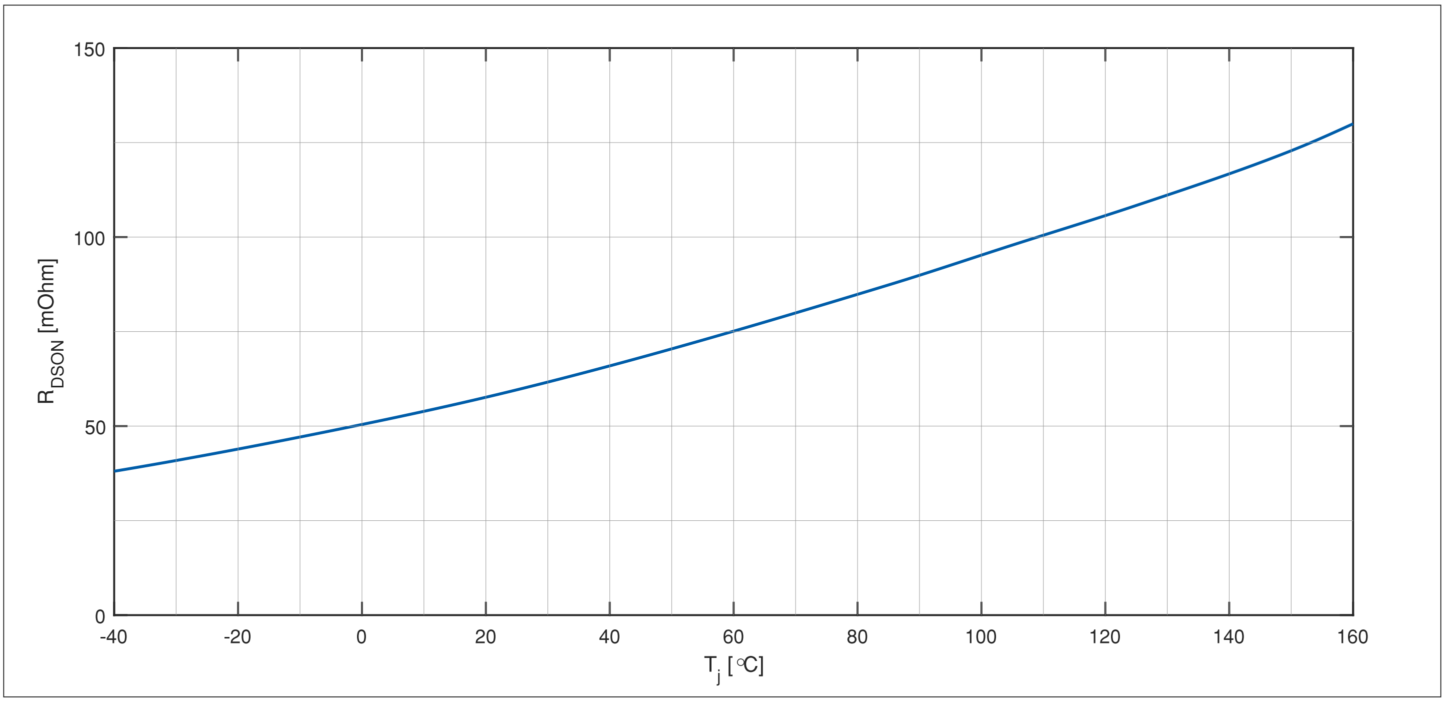


Figure 9 Typical ON-state resistance

A high signal at the input pin (see Input Pins) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn on/off characteristics with resistive load

The figure below shows the typical timing when switching a resistive load.

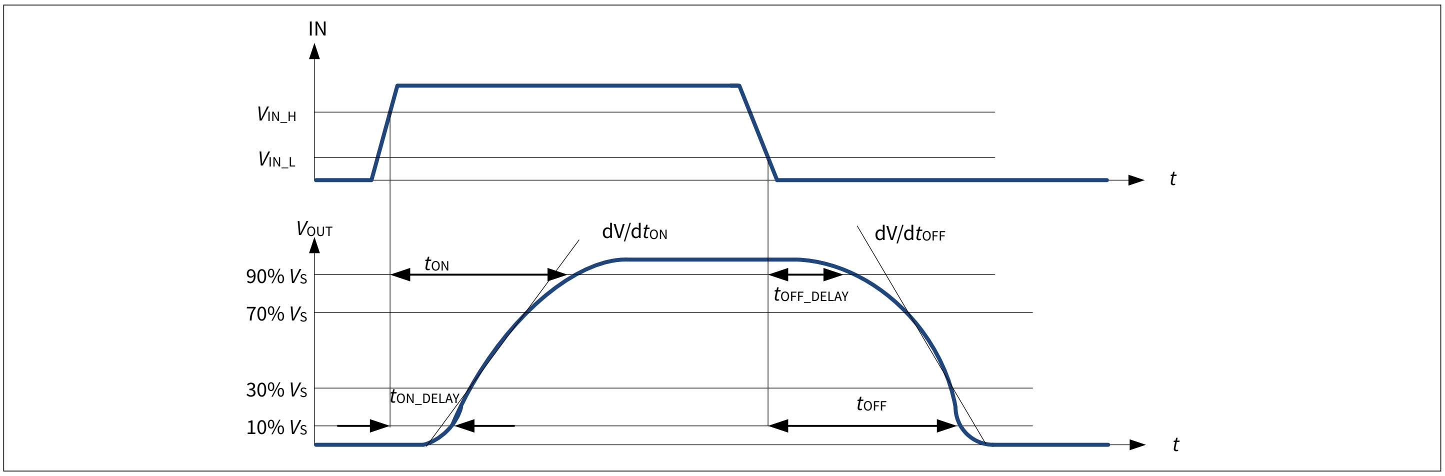


Figure 10 Switching a resistive load - timings

5.3 Inductive load

5.3.1 Output clamping

When switching off inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current.

To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(CLAMP)}$ implemented that limits negative output voltage to a certain level (V_S - $V_{DS(CLAMP)}$).

Refer to the figures below for details. Nevertheless, the maximum allowed load inductance is limited.

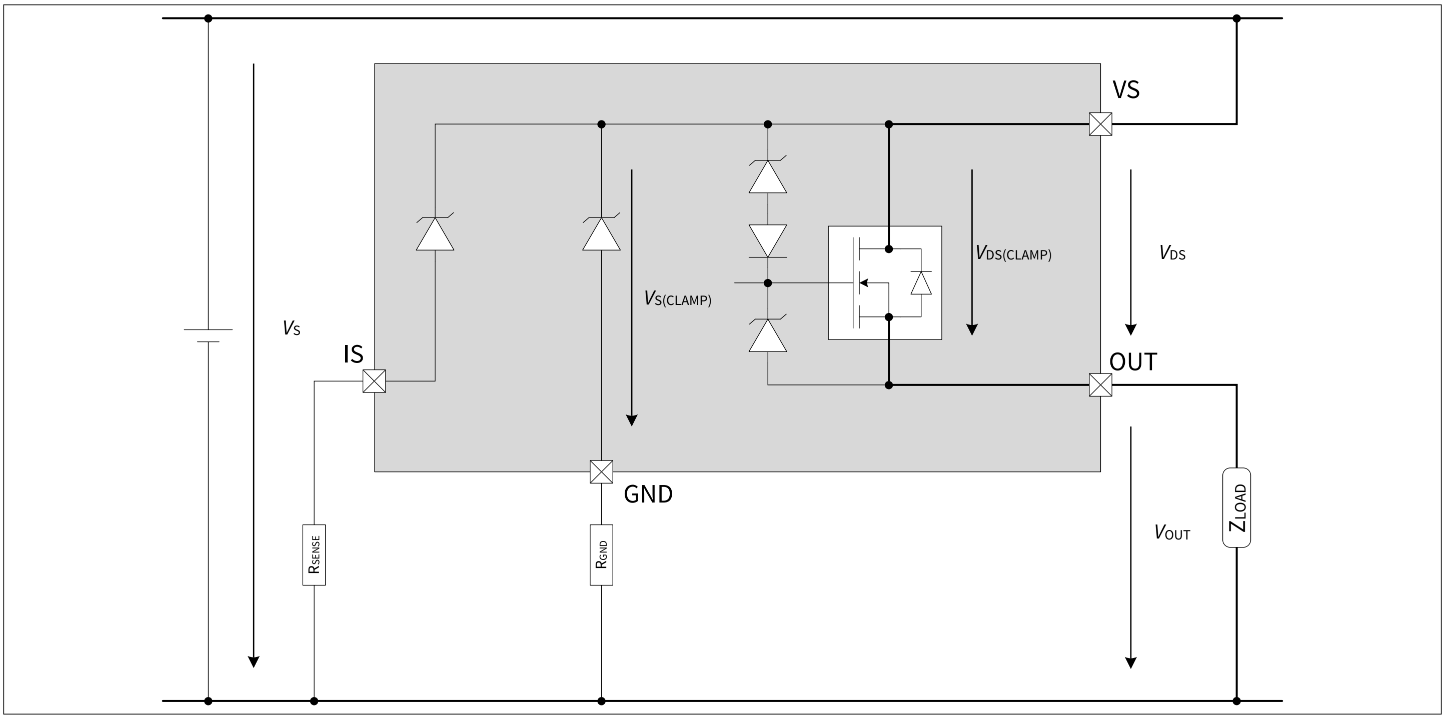


Figure 11 **Output clamp**

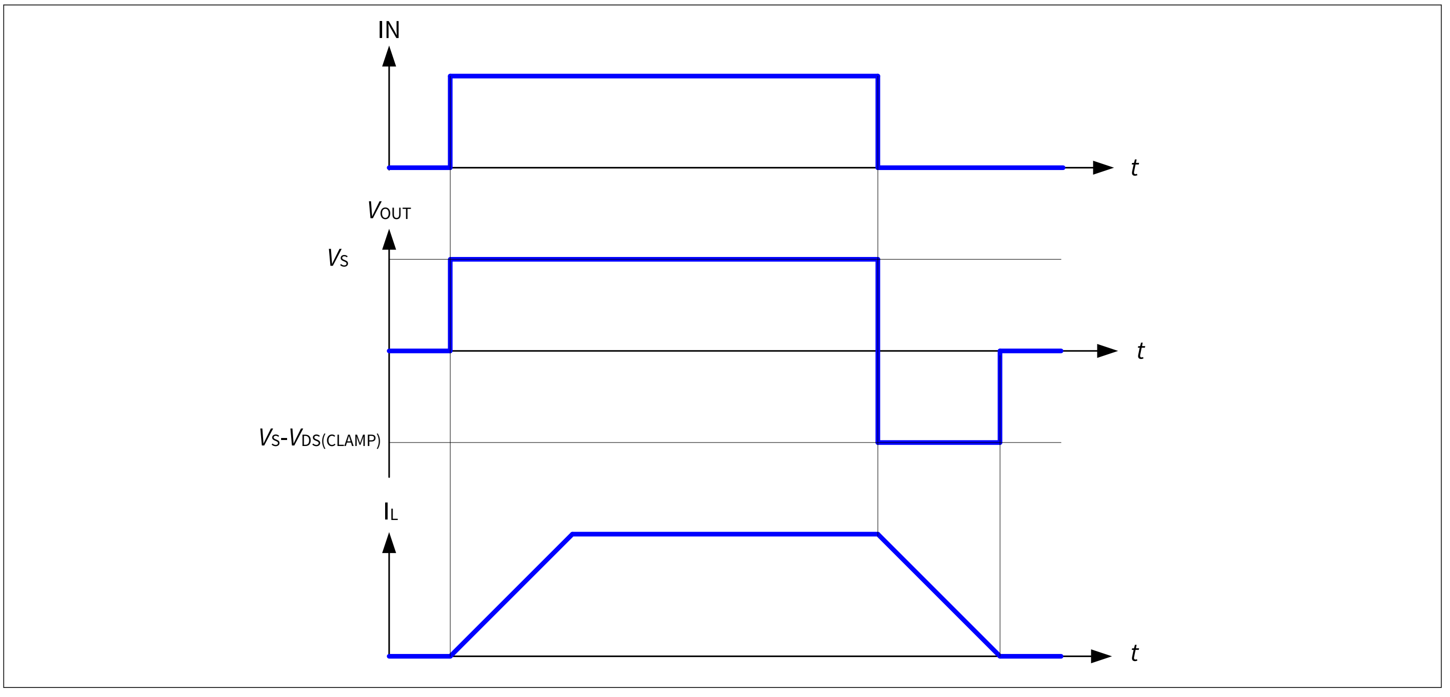


Figure 12 **Switching an inductive load**

***Note**: The device is not designed to be used as high side switch in an H-bridge configuration paired with external low side switches.*

5.3.2 Maximum load inductance

During demagnetization of inductive loads, energy has to be dissipated in the device. This energy can be calculated with following equation:

$$E = V_{DS(CLAMP)} \cdot \frac{L}{R_L} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L \right] \quad (1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Refer to Table 4 for the maximum allowed values of E_{AS} (single pulse energy).

5.4 Inverse current capability

In case of inverse current, meaning a voltage V_{INV} at the output higher than the supply voltage V_S, a current I_{INV} will flow from output to V_S pin via the body diode of the power transistor (refer to the figure below). The output stage follows the state of the IN pin, except if the IN pin goes from off to on during inverse. In that particular case, the output stage is kept off until the inverse current disappears. Nevertheless, the inverse current should not be higher than $I_{L(INV)}$. If the affected channel is on, the diagnostic will detect open load at on (the overtemperature signal is inhibited). At the appearance of V_{INV}, a parasitic diagnostic can be observed. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection functions are available.

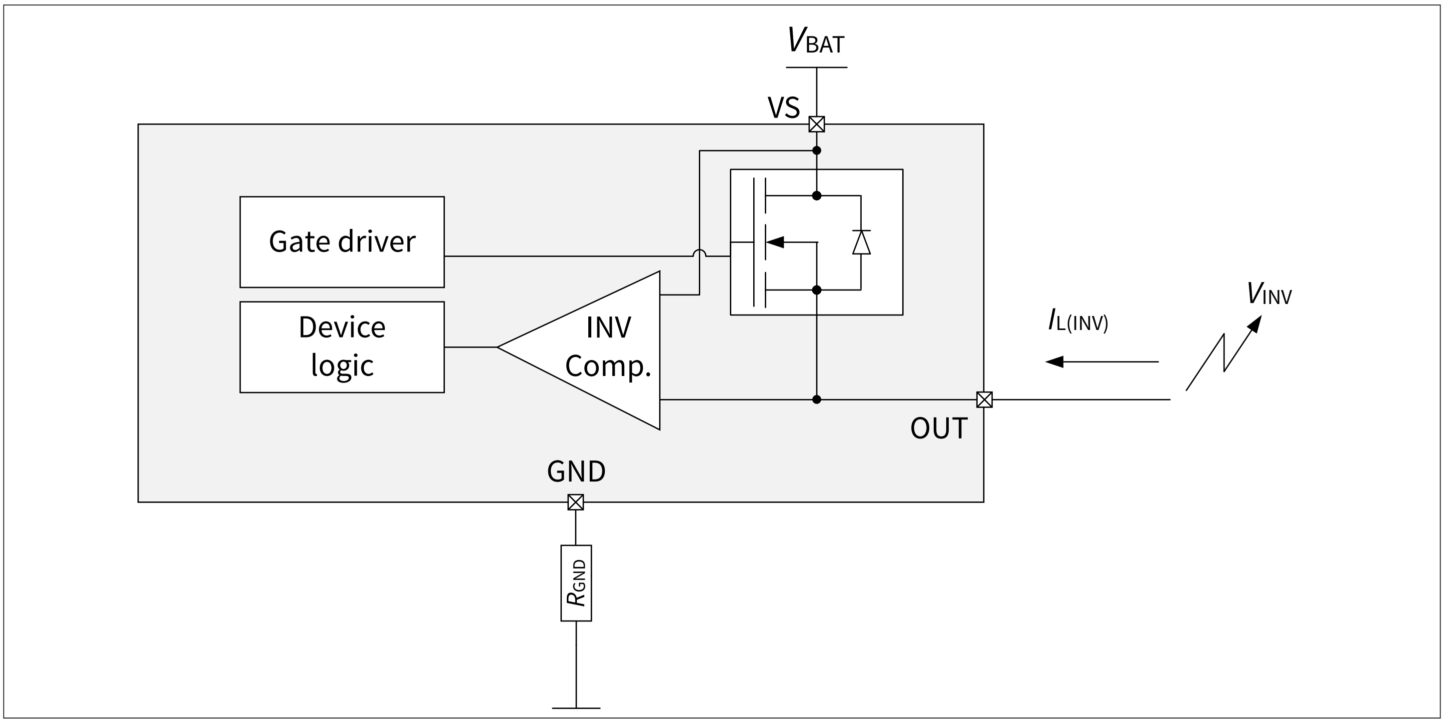


Figure 13 **Inverse current circuitry**

5.5 Electrical characteristics power stage

Table 8 Electrical characteristics power stage

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drain to source clamping voltage	$V_{DS(CLAMP)}$	65	70	75	V	I_{DS} = 20 mA	PRQ-103
Output voltage drop limitation at small load currents	$V_{DS(SLC)}$	–	10	25	mV	I_L = 50 mA	PRQ-102
Turn-ON delay time	t_{ON_delay}	–	35	70	µs	V_S = 48 V to V_{OUT} = 10% of V_S	PRQ-112
Turn-OFF delay time	t_{OFF_delay}	–	40	80	µs	V_S = 48 V to V_{OUT} = 90% of V_S	PRQ-113
Turn-ON time	t_{ON}	20	80	180	µs	V_S = 48 V to V_{OUT} = 90% of V_S	PRQ-109
Turn-OFF time	t_{OFF}	20	80	180	µs	V_S = 48 V to V_{OUT} = 10% of V_S	PRQ-110
Turn-ON / OFF matching	Δt_{SW}	-60	–	60	µs	V_S = 48 V t_{ON} - t_{OFF}	PRQ-111
Slew rate at turn-ON	dV/dt_{ON}	0.5	1.2	2.0	V/µs	V_S = 48 V from 30% to 70% of V_S	PRQ-106
Slew rate at turn-OFF	$-dV/dt_{OFF}$	0.5	1.2	2.0	V/µs	V_S = 48 V from 70% to 30% of V_S	PRQ-107
Slew rate matching	dV/dt	-0.3	0	0.3	V/µs	V_S = 48 V dV/dt_{ON} - dV/dt_{OFF}	PRQ-384
ON-state resistance at 25°C	$R_{DS(ON)\_25}$	–	75	–	mΩ	T_J = 25°C	PRQ-271
ON-state resistance at 150°C	$R_{DS(ON)\_150}$	–	–	150	mΩ	I_L = 2.5 A T_J = 150°C	PRQ-272
Nominal load current	$I_{L(NOM)}$	–	2.5	–	A	T_A = 85°C T_J < 150°C	PRQ-420
ILIM fraction to calculate the maximum application load current	$I_{LIM01\_fraction}$	–	–	0.70	–	[1)] $I_{L(APP),MAX} = I_{LIM01\_fraction} \cdot I_{LIM}$ 0.81 A ≤ I_{LIM} ≤ 1.87 A	PRQ-394

(table continues...)

Table 8 **(continued) Electrical characteristics power stage**

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ILIM fraction to calculate the maximum application load current	$I_{LIM02\_fraction}$	–	–	0.75	–	1) $I_{L(APP),MAX} = I_{LIM02\_fraction} \cdot I_{LIM}$ 1.87 A ≤ I_{LIM} ≤ 2.30 A	PRQ-395
ILIM fraction to calculate the maximum application load current	$I_{LIM03\_fraction}$	–	–	0.80	–	1) $I_{L(APP),MAX} = I_{LIM03\_fraction} \cdot I_{LIM}$ 2.30 A ≤ I_{LIM} ≤ 4.60 A	PRQ-396
ILIM fraction to calculate the maximum application load current	$I_{LIM04\_fraction}$	–	–	0.85	–	1) $I_{L(APP),MAX} = I_{LIM04\_fraction} \cdot I_{LIM}$ 4.60 A ≤ I_{LIM} ≤ 5.56 A	PRQ-397
Output leakage current per channel at 85°C	$I_{L(OFF)\_85}$	–	0.05	0.5	µA	2) IN = floating V_{OUT} = 0 V T_J ≤ 85°C	PRQ-278
Output leakage current per channel at 150°C	$I_{L(OFF)\_150}$	–	3	10	µA	IN = floating V_{OUT} = 0 V T_J = 150°C	PRQ-279
Inverse current capability	$I_{L(INV)}$	–	2.5	–	A	$V_S < V_{OUT}$	PRQ-269
Switch ON energy	E_{ON}	–	485	–	µJ	R_L = 50 Ω V_{OUT} = 90% of V_S V_S = 54 V	PRQ-264
Switch OFF energy	E_{OFF}	–	405	–	µJ	R_L = 50 Ω V_{OUT} = 10% of V_S V_S = 54 V	PRQ-265

1) This parameter describes the maximum nominal load capability of the channel from an electrical point of view when respecting the maximum T_J ≤ 150°C. Please note that depending on the individual thermal design of a real application (and a potentially insufficient thermal budget resulting hereof) additional restrictions for $I_{L(NOM)}$ may occur from thermal constraints in order not to exceed the maximum allowed junction temperature T_J = 150°C. The latter needs to be considered especially for cases where the current limit is adjusted to very high numbers and at high ambient temperature T_{AMB}).
2) Test at T_J = -40°C only

6 Protection functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the device from fault conditions described in the datasheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of ground protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning off (when it was previously on) or remains off, regardless of the voltage applied on IN pins.

In case of loss of device ground, it's recommended to use input resistors between the microcontroller and the device to ensure switching off of channels.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. The figure below sketches the situation.

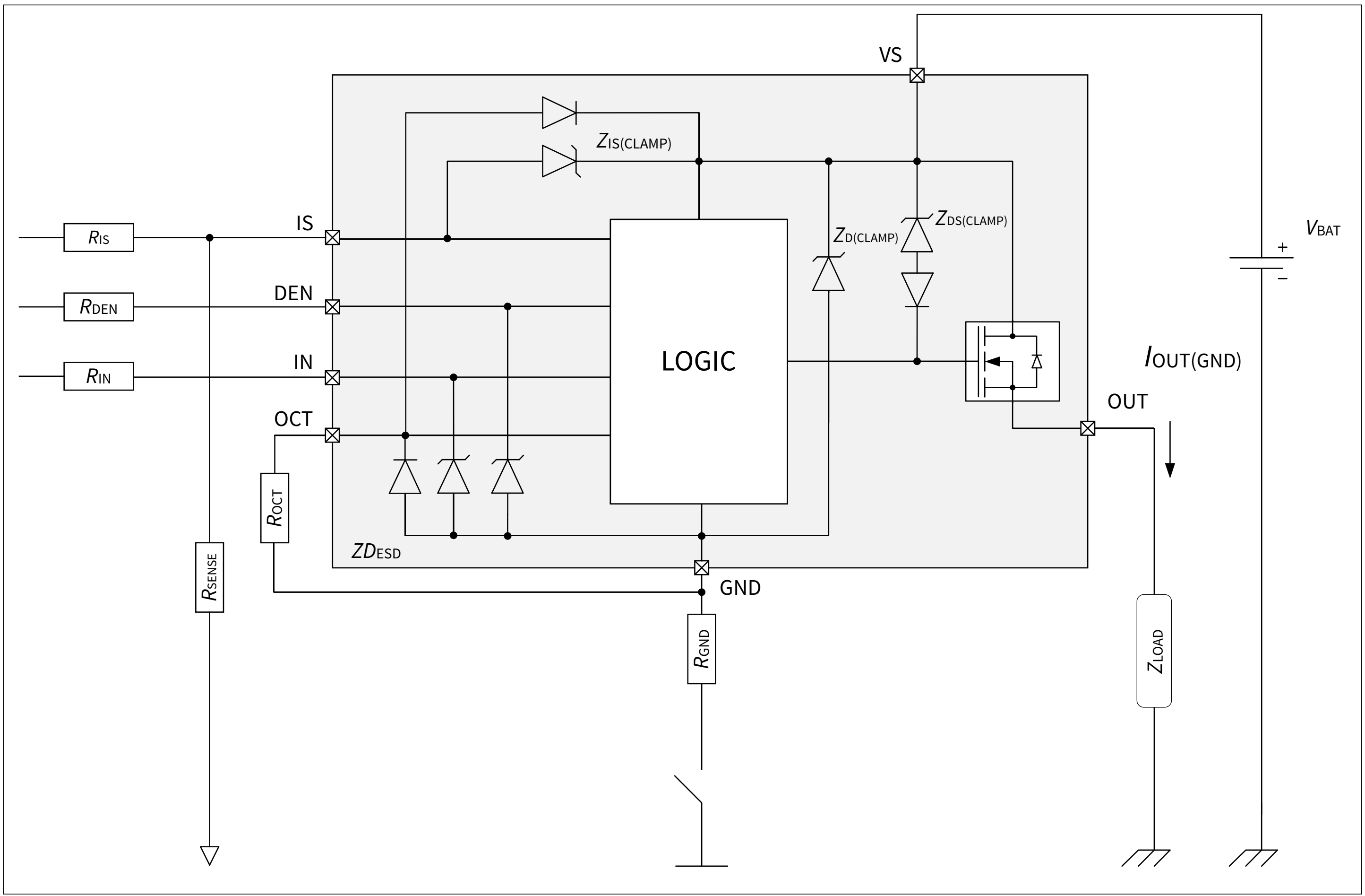


Figure 14 **Loss of ground protection with external components**

6.2 Undervoltage protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can take place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the $V_{S(NOM)}$ range.

6.3 Overvoltage protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{D(CLAMP)}$). To guarantee this mechanism operates properly in the application, the current in the circuitry has to be limited by a ground resistor. The figure below shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(CLAMP)}$, the power transistor switches ON and in addition the voltage across the logic section is clamped. As a result, the internal ground potential rises to V_S - $V_{S(CLAMP)}$. Due to the ESD Zener diodes, the potential at pin INx, DSEL, and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the device remains ON. In the case the device was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(CLAMP)}$, the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability.

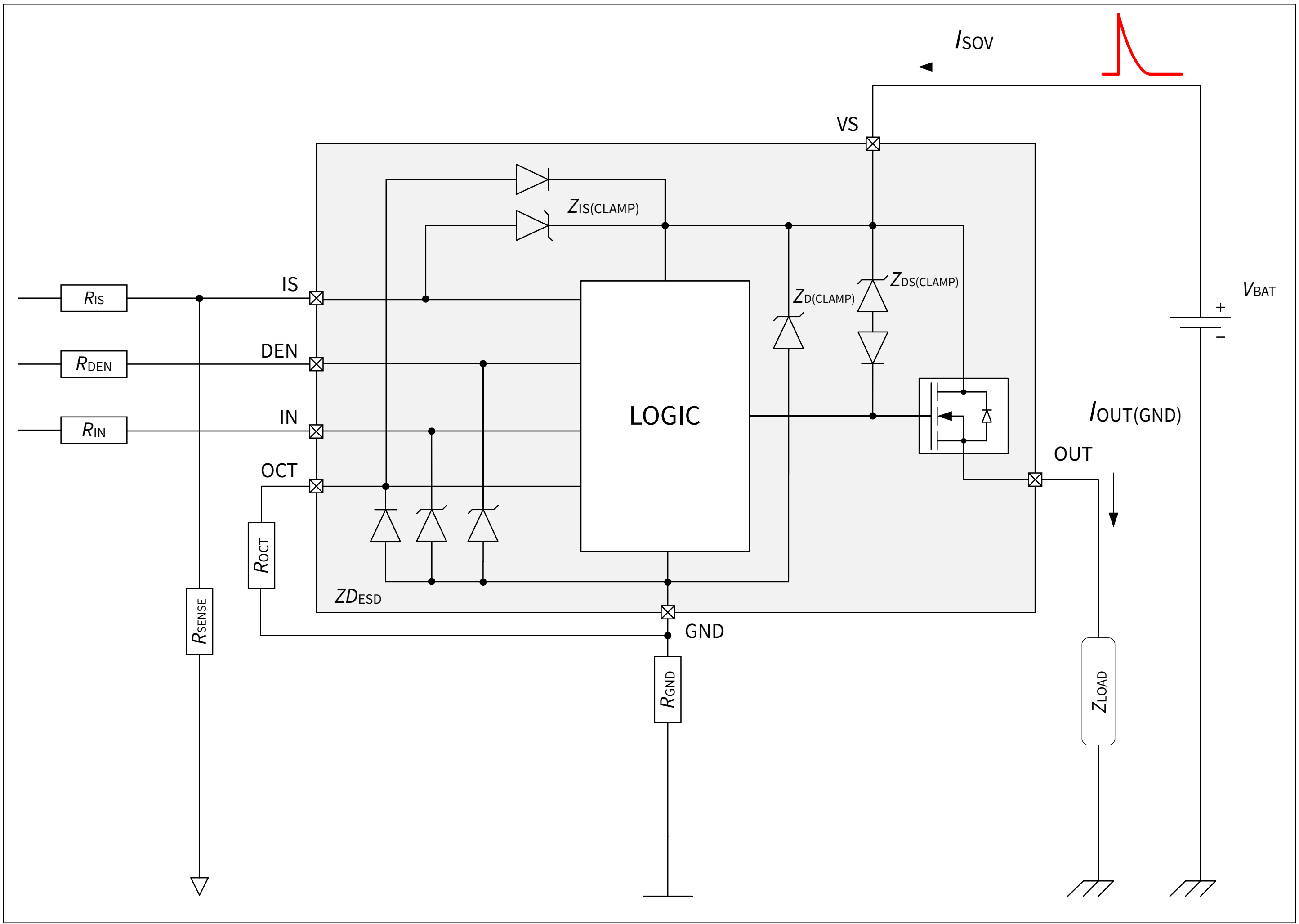


Figure 15 **Overvoltage protection with external components**

6.4 Overload protection

In the event of an overload, such as high risk inrush of a capacitive load, or short circuit to ground, the device offers several protection mechanisms.

6.4.1 Adjustable overcurrent protection

The device is protected against overload and short circuit to ground. It has an adjustable current limitation range from $I_{LIM,MIN}$ to $I_{LIM,MAX}$. This feature offers protection against overstress for the load as well as for the power output stage. The configured current threshold is independent of V_{DS} and T_J. If DMOS temperature increase is exceeding the device safe operation environment, overtemperature and dynamic tempertature protection mechanism will be triggered as shown in the Figure Overload protection.

For the adjustment of the current threshold for the output channel, the following equation can be considered:

$$I_{LIM} = (k_{ILIOCT} \cdot I_{OCT}) + \Delta I_{LIM} \quad (2)$$

where

$$I_{OCT} = (I_{LIM} - \Delta I_{LIM})/k_{ILIOCT} \quad (3)$$

To select the proper resistor value R_{OCT} connected between the OCT pin and device ground, the following equation can be considered:

$$R_{OCT} = (V_{OCT} \cdot k_{ILIOCT})/(I_{LIM} - \Delta I_{LIM}) \quad (4)$$

In case of an OCT pin short to ground with the current exceeding $I_{OCT(SHORT2GND)}$ the device will set the current limit value to $I_{LIMOC(SHORT2GND)}$. The behavior of how I_{OCT} is related to I_{LIM} is described in the figure below. However, due to the maximum rating of the allowed current through OCT pin I_{OCT}, it is not recommended to shorten the OCT pin to device GND. In the case of reverse battery condition, this could lead to violations of the maximum ratings, therefore I_{OCT} absolute maximum rating needs to be considered.

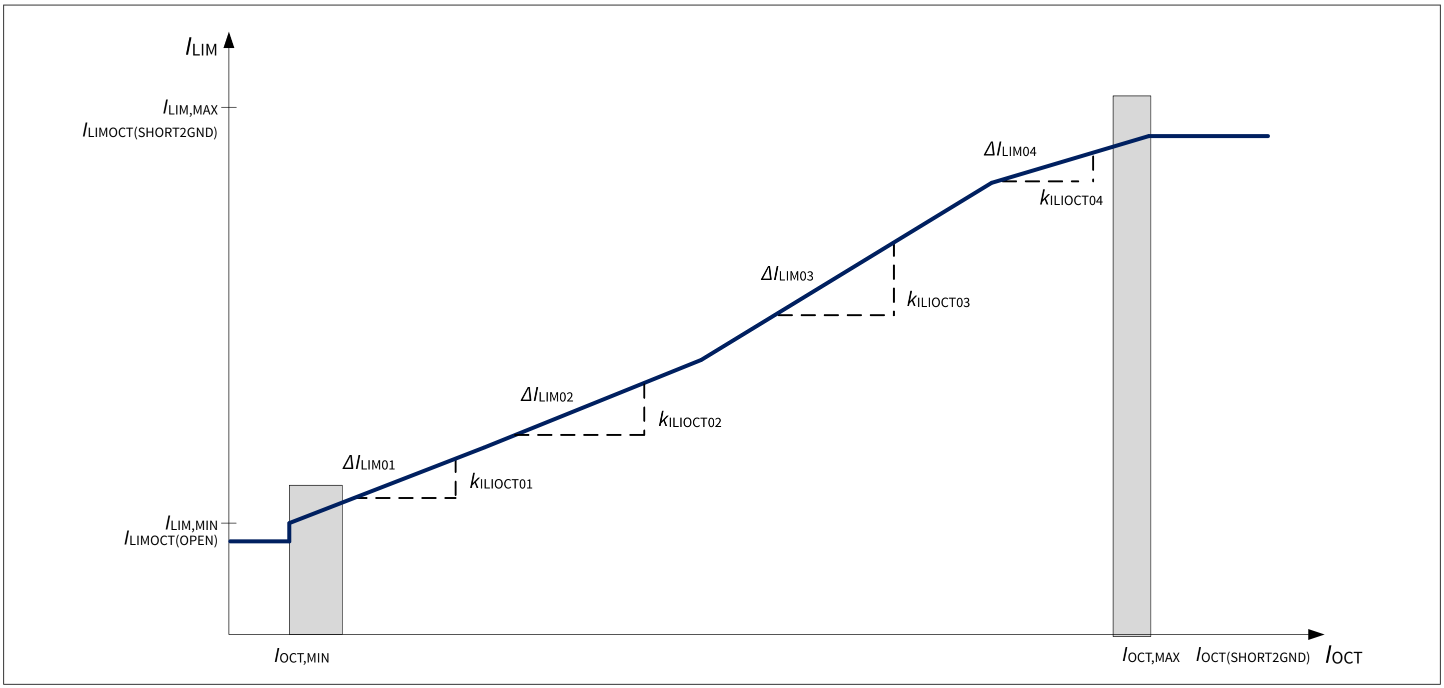


Figure 16 **Adjustable overcurrent threshold behavior**

When setting the required current limitation, make sure that there is a safety margin between the adjusted current limitation and the expected load current of the application. This is important to prevent unintentional activation of the current limitation circuit during normal operation. When the load current is close(r) to the adjusted current limitation threshold, the turn on slew rate becomes slower, causing a longer t_{ON} timing, while the turn off slew rate may become faster resulting in a shorter t_{OFF} timing. Keeping this safety margin ensures that the influence of the current limitation threshold on switching timings is moderate.

The maximum application load capability of the device at a certain current limitation threshold is given by the equation below:

$$I_{L(APP),MAX} = I_{LIM0x\_fraction} \cdot I_{LIM} \tag{5}$$

where x = 1 - 4. Refer to Electrical characteristics power stage.

6.4.2 Overtemperature protection

The device incorporates both an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature protection circuitry for the channel. Activation of either sensor will cause the overheated channel to switch OFF to prevent destruction. The channel remains switched OFF even when the temperature has cooled down to an acceptable value (latch behavior). No retry strategy is implemented to switch ON the channel when the DMOS temperature has cooled down and only the IN pin signal toggling can re-activate the power stage. The figure below depicts the behavior of the device during an overtemperature condition.

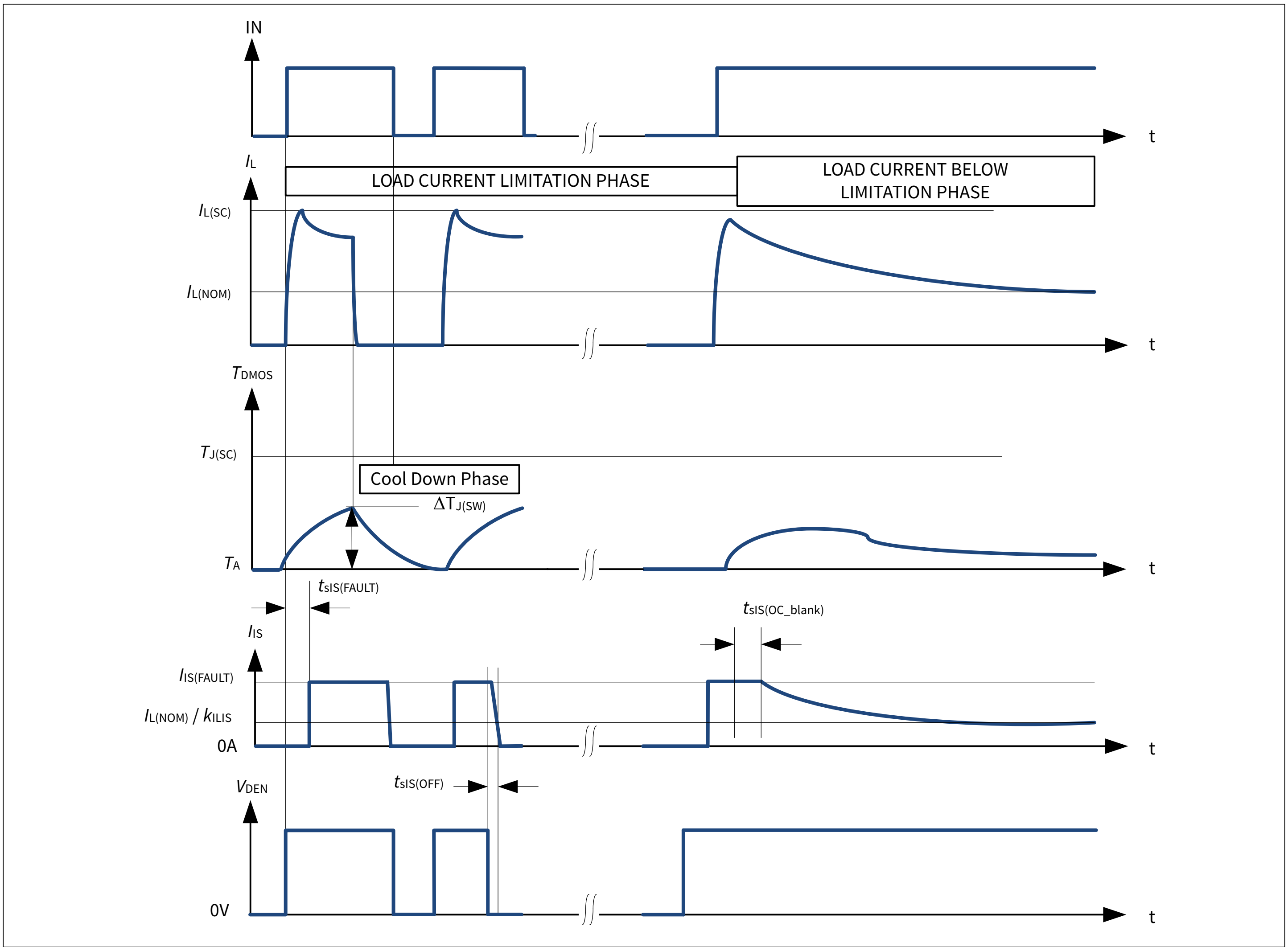


Figure 17 **Overload protection**

***Note**: For readability, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.*

6.5 Electrical characteristics - Protection functions

Table 9 Electrical characteristics protection functions

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Loss of ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	V_S = 48 V All pins are disconnected except VS and OUT	PRQ-116
Overvoltage							
Overvoltage protection	$V_{S(CLAMP)}$	65	70	75	V	$I_{SOV} \leq$ 20 mA	PRQ-120
Overload							
Dynamic temperature increase while switching	$\Delta T_{J(SW)}$	–	80	–	K	[1]	PRQ-123
Thermal shutdown temperature	$T_{J(SC)}$	150	170	200	°C	[1] [2]	PRQ-124
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	–	30	–	K	–	PRQ-125
Adjustable overcurrent limitation accuracy (low)	$I_{LIM01(ACC)}$	-70.3	–	70.3	%	0.81 A $\leq I_{LIM} \leq$ 1.87 A V_{DS} = 5 V	PRQ-300
Adjustable overcurrent limitation d-value (low)	ΔI_{LIM01}	–	0.58	–	A	0.81 A $\leq I_{LIM} \leq$ 1.87 A V_{DS} = 5 V	PRQ-301
Adjustable overcurrent limitation k-factor (low)	$k_{ILIOCT01}$	–	33.4k	–	–	0.81 A $\leq I_{LIM} \leq$ 1.87 A V_{DS} = 5 V	PRQ-302
Adjustable overcurrent limitation accuracy (medium1)	$I_{LIM02(ACC)}$	-40.2	–	40.2	%	1.87 A $\leq I_{LIM} \leq$ 2.30 A V_{DS} = 5 V	PRQ-303
Adjustable overcurrent limitation d-value (medium1)	ΔI_{LIM02}	–	0.24	–	A	1.87 A $\leq I_{LIM} \leq$ 2.30 A V_{DS} = 5 V	PRQ-304
Adjustable overcurrent limitation k-factor (medium1)	$k_{ILIOCT02}$	–	42.4k	–	–	1.87 A $\leq I_{LIM} \leq$ 2.30 A V_{DS} = 5 V	PRQ-305
Adjustable overcurrent limitation accuracy (medium2)	$I_{LIM03(ACC)}$	-37.5	–	37.5	%	2.30 A $\leq I_{LIM} \leq$ 4.60 A V_{DS} = 5 V	PRQ-306
Adjustable overcurrent limitation d-value (medium2)	ΔI_{LIM03}	–	-0.58	–	A	2.30 A $\leq I_{LIM} \leq$ 4.60 A V_{DS} = 5 V	PRQ-307
Adjustable overcurrent limitation k-factor (medium2)	$k_{ILIOCT03}$	–	57.1k	–	–	2.30 A $\leq I_{LIM} \leq$ 4.60 A V_{DS} = 5 V	PRQ-308

(table continues...)

Table 9 (continued) Electrical characteristics protection functions

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Adjustable overcurrent limitation accuracy (high)	$I_{LIM04(ACC)}$	-48.1	–	48.1	%	4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	PRQ-311
Adjustable overcurrent limitation d-value (high)	ΔI_{LIM04}	–	-6.46	–	A	4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	PRQ-312
Adjustable overcurrent limitation k-factor (high)	$k_{ILIOCT04}$	–	122.9k	–	–	4.60 A ≤ I_{LIM} ≤ 5.56 A V_{DS} = 5 V	PRQ-313
Current limitation value in case OCT pin open	$I_{LIMOCT(OPEN)}$	–	0.75	–	A	$I_{OCT} \leq I_{OCT(OPEN)}$	PRQ-309
Current limitation value in case OCT pin short to device ground	$I_{LIMOCT(SHORT2GND)}$	5.1	7.9	10.7	A	$I_{OCT} \geq I_{OCT(SHORT2GND)}$	PRQ-310

1) Functional test only
2) Test at T_J = 150°C only

7 Diagnostic functions

For diagnosis purposes, the device provides a combination of digital and analog signals at pin IS. These signals are called SENSE. In case the diagnostic is disabled via DEN (DEN set to "high"), pin IS becomes high impedance.

In case DEN is set to "high", the SENSE of the channel is enabled. In case DEN is set to "low", pin IS becomes high impedance.

7.1 IS pin

The device provides a sense signal called I_{IS} at pin IS. If a "hard" failure mode occurs (short circuit to GND/current limitation/overtemperature/excessive dynamic temperature increase or open load at OFF) a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is provided. The complete IS pin and diagnostic mechanism is described in the figure below. The accuracy of the sense current depends on temperature and load current. Due to the ESD protection, in connection to V_S, it is not recommended to share the IS pin with other devices if these devices are using another battery feed. The consequence is that the unsupplied device would be fed via the IS pin of the supplied device.

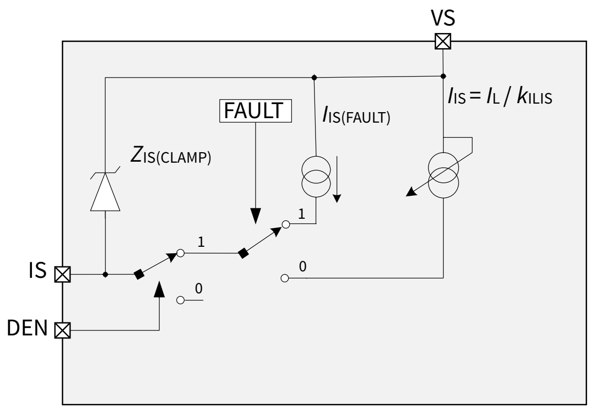


Figure 18 **Diagnostic block diagram**

7.2 SENSE signal in different operating modes

The table below gives a quick reference for the state of the IS pin during device operation.

Table 10 **SENSE signal, function of operation mode**

Operation mode	Input level	DEN	Output level	Diagnostic output
Normal operation	LOW	HIGH	Z	Z
Short circuit to GND	LOW	HIGH	~ GND	Z
Overtemperature	LOW	HIGH	Z	Z
Short circuit to V_S	LOW	HIGH	V_S	$I_{IS(FAULT)}$
Open load	LOW	HIGH	$< V_{OL(OFF)}$ $> V_{OL(OFF)}$[1)]	Z $I_{IS(FAULT)}$
Inverse current	LOW	HIGH	$\sim V_{INV}$	Z
OCT pin short circuit to GND	LOW	HIGH	Z	$I_{IS(FAULT)}$
Normal operation	HIGH	HIGH	$\sim V_S$	$I_{IS} = I_L / k_{ILIS}$
Current limitation	HIGH	HIGH	$< V_S$	$I_{IS(FAULT)}$
Short circuit to GND	HIGH	HIGH	~ GND	$I_{IS(FAULT)}$

(table continues...)

Table 10 (continued) SENSE signal, function of operation mode

Operation mode	Input level	DEN	Output level	Diagnostic output
Overtemperature $T_{J(SW)}$ event	HIGH	HIGH	Z	$I_{IS(FAULT)}$
Short circuit to V_S	HIGH	HIGH	V_S	$I_{IS} < I_L / k_{ILIS}$
Open load	HIGH	HIGH	$\sim V_S$[2]	$I_{IS} < I_{IS(OL)}$
Inverse current	HIGH	HIGH	$\sim V_{INV}$	$I_{IS} < I_{IS(OL)}$
OCT pin short circuit to GND	HIGH	HIGH	$\sim V_S$	$I_{IS} = I_L / k_{ILIS}$
Underload	HIGH	HIGH	$\sim V_S$[3]	$I_{IS(OL)} < I_{IS} < I_L / k_{ILIS}$
Diagnostic disabled	Don't care	LOW	Don't care	Z

1) With additional pull-up resistor
2) The output current has to be smaller than $I_{L(OL)}$
3) The output current has to be higher than $I_{L(OL)}$

7.3 Sense signal in the nominal current range

A sense resistor R_{IS} must be connected between IS pin and module ground if the current sense diagnosis is used. This resistor has to be higher than 560 Ω to limit the power losses in the sense circuitry. A typical value is 1.2 kΩ.

7.3.1 Sense signal variation as a function of temperature and load current

In some applications a better accuracy is required at smaller currents. To achieve this accuracy requirement, a calibration on the application is possible. To avoid multiple calibration points at different load and temperature conditions, the device allows limited derating of the k_{ILIS} value, at a given point. This derating is described by the parameter Δk_{ILIS}.

7.3.2 SENSE signal timing

The figure below shows the timing during settling and disabling of the SENSE.

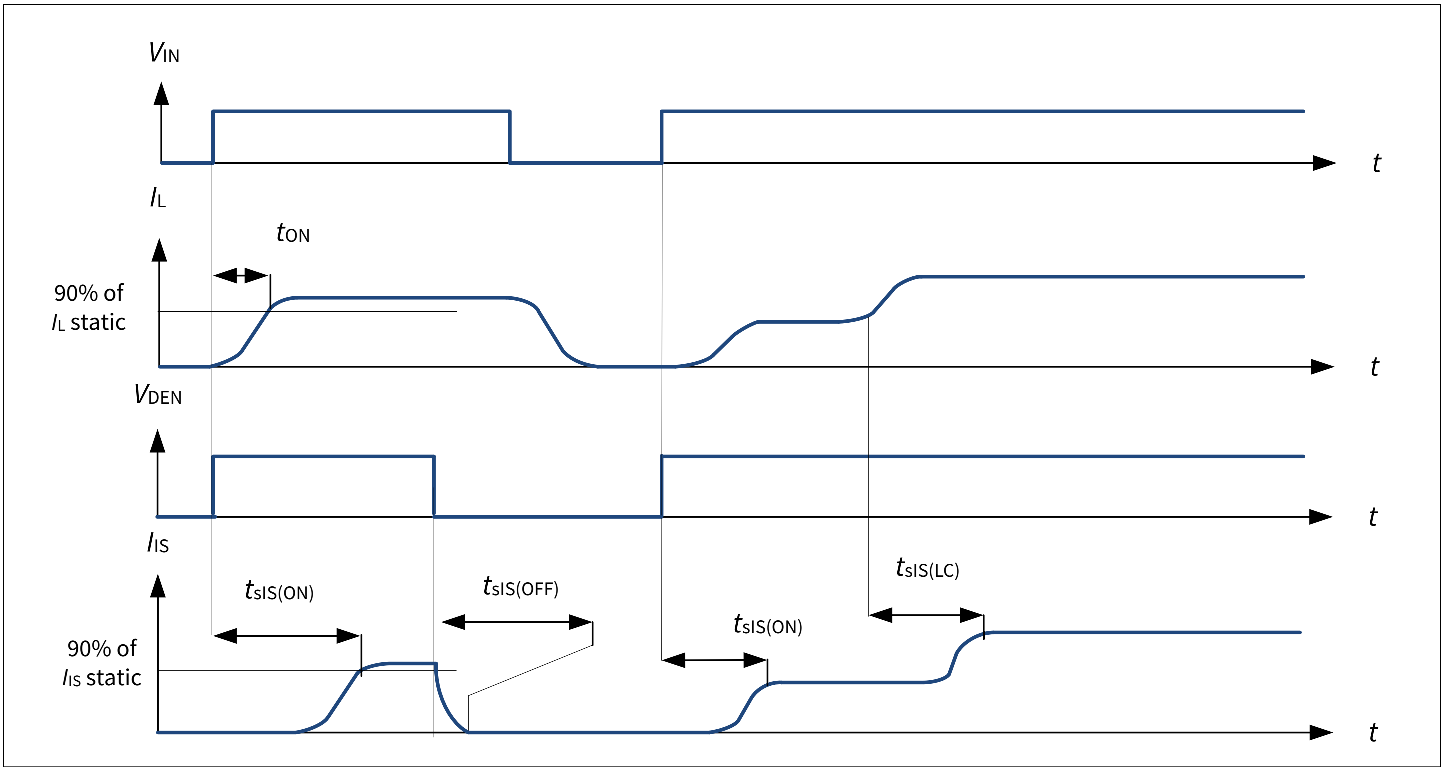


Figure 19 **SENSE enabling / disabling timings**

7.3.3 SENSE signal in open load

7.3.3.1 Open load in ON diagnostic

If the channel is ON, a leakage current can still flow through an open load, for example due to humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for this leakage current. If the current I_L flowing out the power DMOS is below this value, the device recognizes a failure, if the DEN is enabled. In that case, the SENSE current is below $I_{IS(OL)}$. Otherwise, the minimum SENSE current is given above parameter $I_{IS(OL)}$.

7.3.3.2 Open load in OFF diagnostic

For open load diagnosis in OFF state, an external output pull-up resistor (R_{OL}) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account. The figure below gives a sketch of the situation. $I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see Electrical characteristics power stage) and external leakages, for example due to humidity or corrosion in the application.

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended. If the channel is OFF, the output is no longer pulled down by the load and V_{OUT} rises to nearly V_S. This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional R_{PD} resistor can be used to pull V_{OUT} to 0 V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection (refer to Table 10).

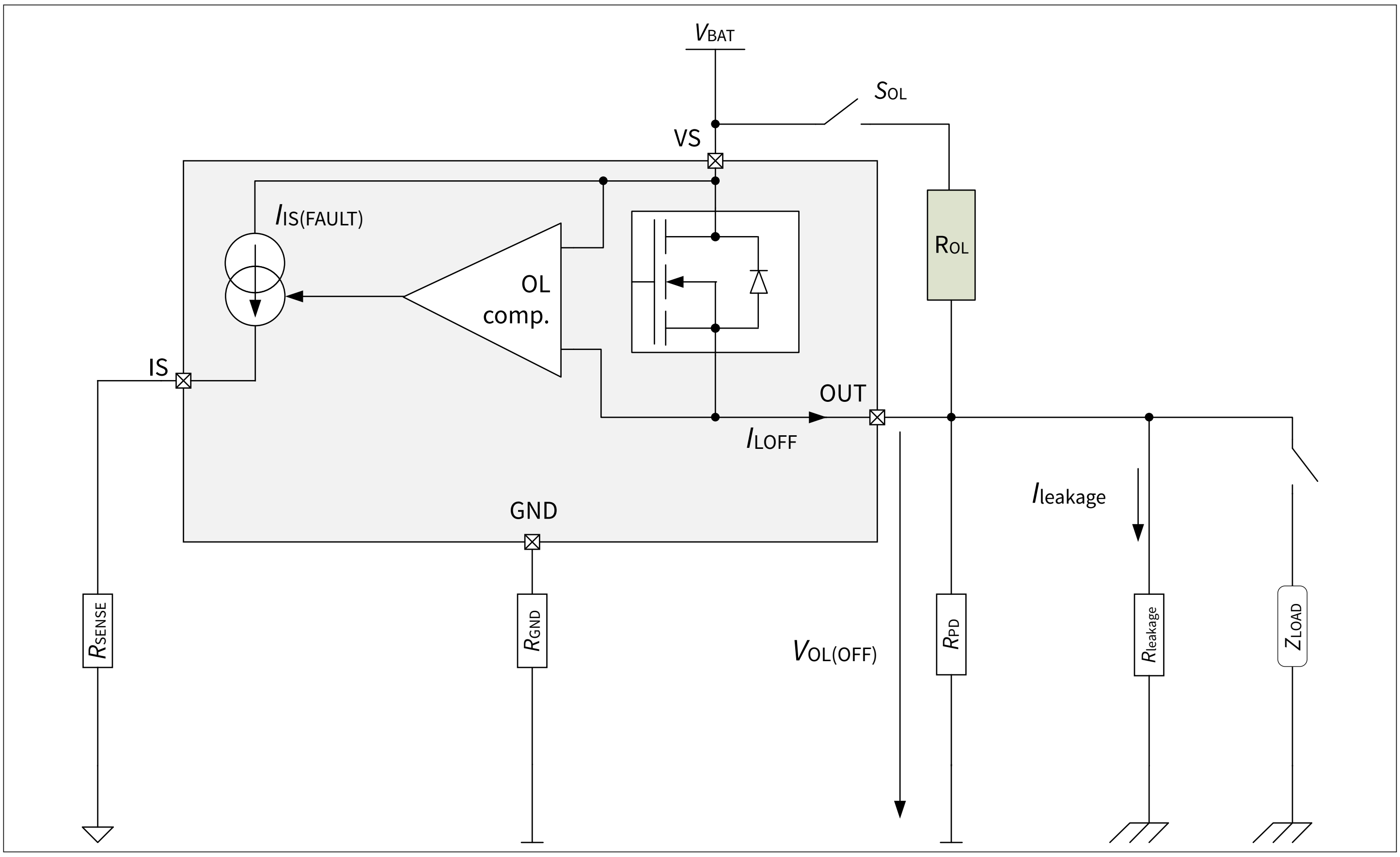


Figure 20 **Open load in OFF diagnostic electrical equivalent circuitry**

7.3.3.3 Open load diagnostic timing

The figure below shows the timing during either Open Load in ON or OFF condition when the DEN pin is HIGH. Please note that a delay $t_{sIS(FAULT\_OL\_OFF)}$ has to be respected after the falling edge of the input, when applying an open load in OFF diagnosis request, otherwise the diagnosis can be wrong.

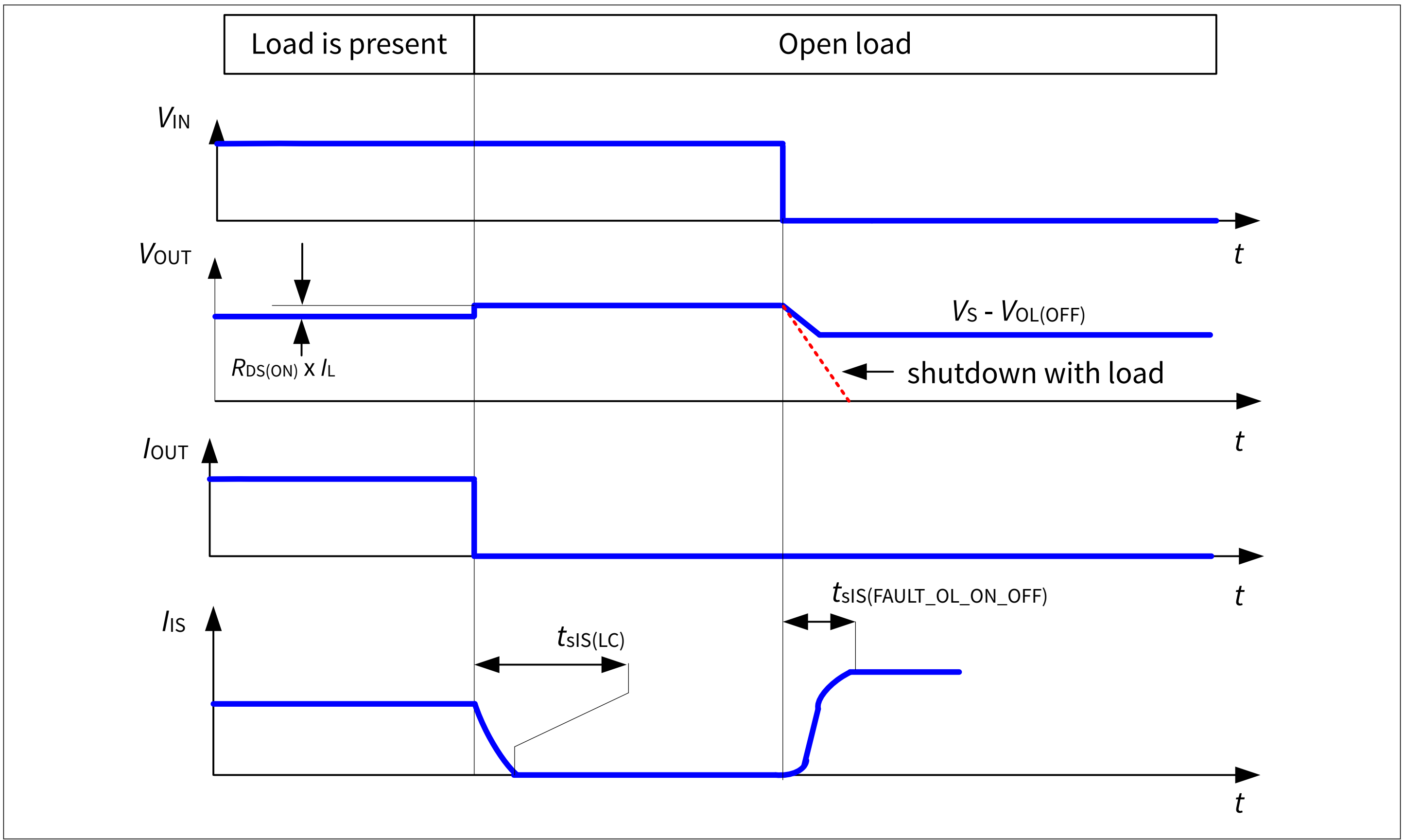


Figure 21 **SENSE signal in Open load in OFF**

7.3.4 SENSE signal with OUT in short circuit to VS

If there is a short circuit between the OUT pin and the supply V_S, all or portion (depending on the short circuit impedance) of the load current will flow through the short circuit. As a result, a lower current compared to the normal operation will flow through the DMOS of the device, which can be recognized at the current sense signal. The open load at OFF detection circuitry can also be used to distinguish a short circuit to V_S. In that case, an external resistor to ground R_{SC_VS} is required. The figure below provides an overview.

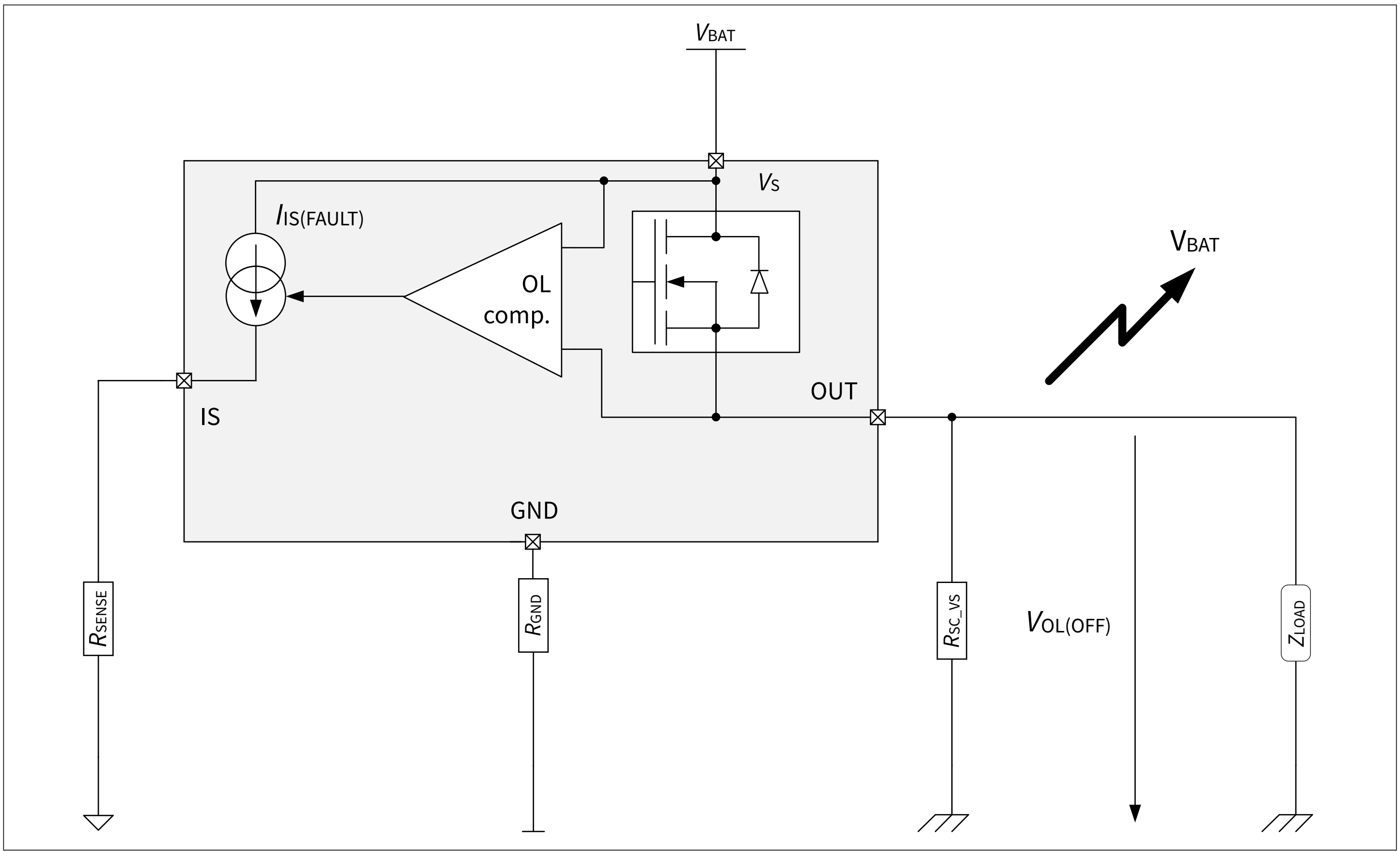


Figure 22 **Short circuit to VS equivalent electrical circuitry**

7.3.5 SENSE signal in case of overload

An overload condition is defined by a current flowing out of the DMOS reaching the current limitation and/or the absolute dynamic temperature swing $T_{J(SW)}$ is reached, and/or the junction temperature reaches the thermal shutdown temperature $T_{J(SC)}$. Refer to Chapter 6.4 for details.

In that case, the SENSE signal given is by $I_{IS(FAULT)}$ when the diagnostic is selected.

The device has a thermal latch behavior, such that when the overtemperature or the exceed dynamic temperature condition has disappeared, the DMOS is reactivated only when the IN is toggled LOW to HIGH. If the DEN pin is activated the SENSE follows the output stage. If no reset of the latch occurs, the device remains in the latching phase and $I_{IS(FAULT)}$ at the IS pin, even though the DMOS is OFF.

7.3.6 SENSE signal in case of inverse current

During inverse current, the sense signal will change to high impedance status when $V_{OUT} \geq V_S$ + 10 mV.

7.4 Electrical characteristics diagnostic functions

Table 11 Electrical characteristics diagnostic functions

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE general characteristics							
IS pin leakage current when sense is disabled	$I_{IS\_(DIS)}$	–	0.02	1	µA	IN = HIGH DEN = LOW $I_L \geq I_{L(NOM)}$	PRQ-129
SENSE fault current	$I_{IS(FAULT)\_-40}$	3	–	35	mA	IN = LOW DEN = HIGH V_{IS} = 0 V $V_{OUT} = V_S$ > 10 V T_J = -40°C	PRQ-389
SENSE fault current	$I_{IS(FAULT)\_25}$	4.5	–	35	mA	IN = LOW DEN = HIGH V_{IS} = 0 V $V_{OUT} = V_S$ > 10 V $T_J \geq$ 25°C	PRQ-390
SENSE signal saturation voltage	V_{SIS}	1	–	3.5	V	IN = LOW DEN = HIGH $V_{OUT} = V_S$ > 10 V I_{IS} = 6 mA	PRQ-130
Open load detection threshold in OFF state	$V_S - V_{OL(OFF)}$	4	–	6	V	IN = LOW DEN = HIGH	PRQ-126
Power supply to IS pin clamping voltage	$V_{IS(CLAMP)}$	65	70	75	V	I_{IS} = 5 mA	PRQ-132
SENSE timings							
Current sense settling time to stable operation after positive input slope on both IN and DEN pins	$t_{sIS(ON)}$	–	–	350	µs	IN and DEN from LOW to HIGH V_S = 48 V $I_L = I_{L3}$	PRQ-335
Current sense settling time to stable operation after positive input slope on both IN and DEN pins	$t_{sIS(ON)}$	–	–	350	µs	IN and DEN from LOW to HIGH V_S = 48 V $I_L = I_{L2}$	PRQ-400

(table continues...)

Table 11 (continued) Electrical characteristics diagnostic functions

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current sense settling time with load current stable and transition of the DEN	$t_{sIS(ON\_DEN)}$	–	–	10	µs	IN = HIGH DEN from LOW to HIGH $I_L = I_{L2}$	PRQ-401
Current sense settling time to stable operation after positive input slope on current load	$t_{sIS(LC)}$	–	–	15	µs	IN = DEN = HIGH from $I_L = I_{L2}$ to $I_L = I_{L3}$	PRQ-138
Current sense settling time to stable operation for open load detection in OFF state	$t_{sIS(FAULT\_OL\_OFF)}$	–	–	100	µs	IN = LOW DEN from LOW to HIGH $V_S = V_{OUT}$ = 48 V	PRQ-315
Current sense settling time to stable operation for open load detection in ON-OFF transition	$t_{sIS(FAULT\_OL\_ON\_OFF)}$	–	200	–	µs	IN from HIGH to LOW DEN = HIGH $V_S = V_{OUT}$ = 48 V	PRQ-141
Current sense settling time to stable operation for overload detection	$t_{sIS(FAULT)}$	–	–	170	µs	1) 2) IN = DEN from LOW to HIGH	PRQ-143
Current sense over current blanking time	$t_{sIS(OC\_blank)}$	–	350	–	µs	IN = DEN = HIGH V_{DS} from 5 V to 0 V	PRQ-144
Diagnostic disable time	$t_{sIS(OFF)}$	–	–	20	µs	IN = HIGH DEN from HIGH to LOW I_{IS} to < 50% I_L / k_{ILIS} $I_L = I_{L3}$	PRQ-145
Current sense							
Open load detection threshold in ON state	$I_{L(OL)}$	3	–	25	mA	$I_{IS(OL)}$ = 5 µA	PRQ-316
Current sense ratio #0	k_{ILIS0}	-75%	1450	+75%		I_{L0} = 50 mA	PRQ-329
Current sense ratio #1	k_{ILIS1}	-25%	1250	+25%		I_{L1} = 0.5 A	PRQ-330
Current sense ratio #2	k_{ILIS2}	-12%	1250	+12%		I_{L2} = 2.5 A	PRQ-331
Current sense ratio #3	k_{ILIS3}	-10%	1250	+10%		I_{L3} = 3.5 A	PRQ-332
Current sense ratio #4	k_{ILIS4}	-8%	1250	+8%		I_{L4} = 7 A	PRQ-333
current sense derating with current and temperature	Δk_{ILIS}	-6	0	+6	%	k_{ILIS3} versus k_{ILIS2}	PRQ-334

1) Functional test only
2) Test at T_J = -40°C only

8 Input pins

8.1 Input circuitry

The input circuitry is compatible with 3.3 V and 5 V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry is compatible with PWM applications. The figure below shows the electrical equivalent input circuitry. In case the pin is not needed, it must be connected to device ground (and not module ground) via a 10 kΩ input resistor.

All digital input pins use a comparator with hysteresis. The switching ON/OFF takes place in a defined region, set by the thresholds $V_{IN(L),MAX.}$ and $V_{IN(H),MIN.}$ The exact value where the ON and OFF take place are unknown and depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, a hysteresis is implemented. This ensures a certain immunity to noise.

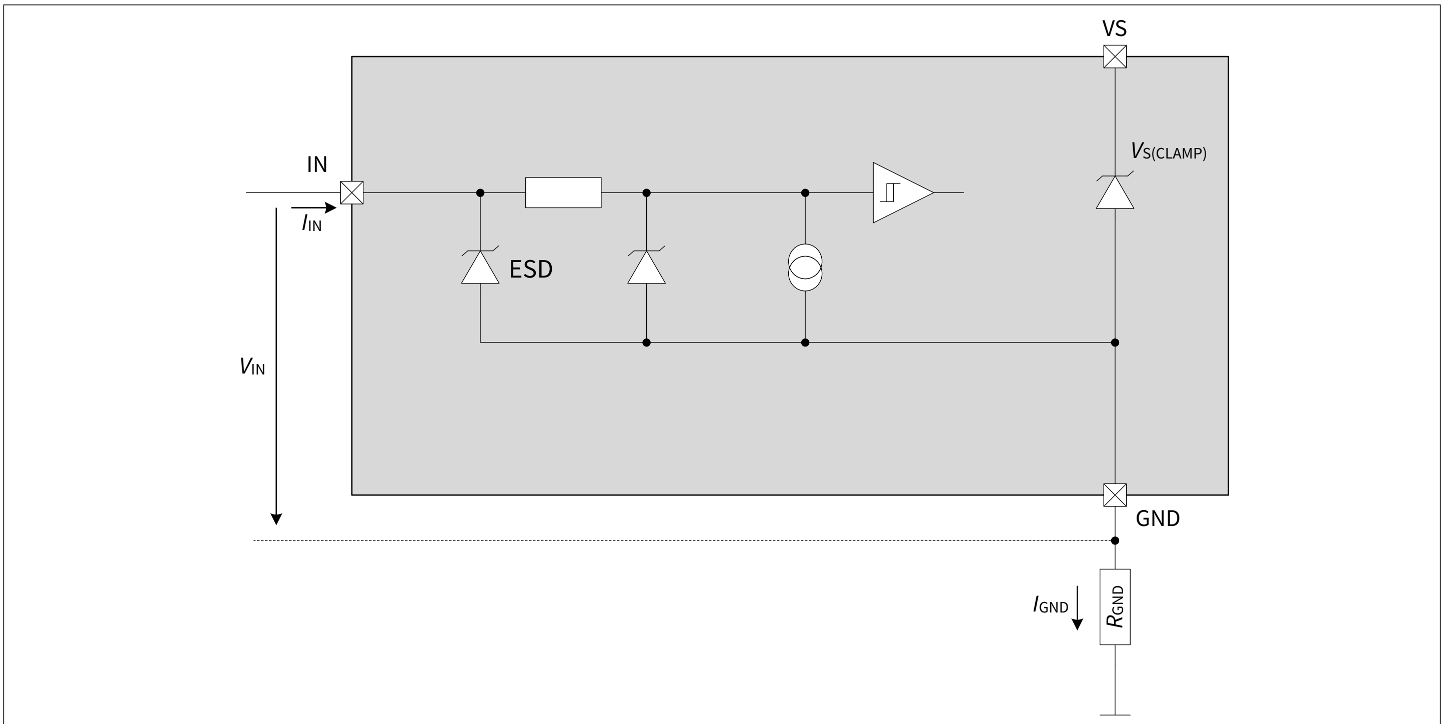


Figure 23 Input pin circuitry

8.2 DEN/DSEL pin

The DEN pin enables and disables the diagnostic functionality of the device. The pin has the same structure as the input pin, please refer to the figure above.

8.3 OCT pin

The device has one analog pin for direct control. To be able to adjust the overcurrent threshold for the OUT pin, the device offers an OCT pin. The pin needs to be connected to device ground via an external resistor R_{OCT} . The external adjustable current limit allows the flexibility to adjust to overcurrent limitation as defined in the table below. This improves the reliability of the system by limiting the inrush or overload current. The electrical equivalent of the overcurrent pin circuitry is shown in the figure below.

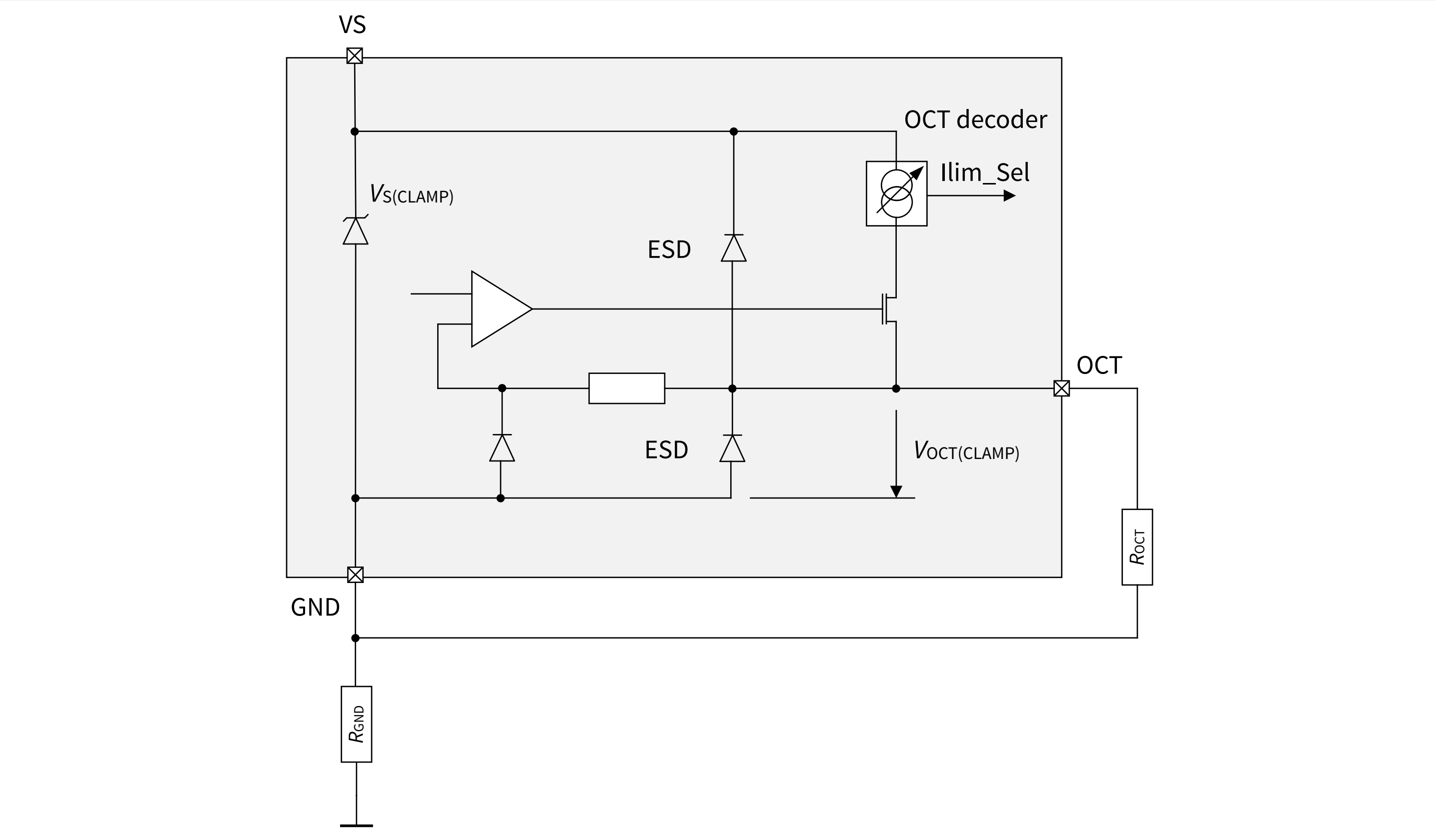


Figure 24 **Overcurrent pin circuit**

8.4 Electrical characteristics input pins

Table 12 Electrical characteristics input pins

$V_S = V_{S(NOM)}$, T_J = -40°C to 150°C.
Unless otherwise specified typical values: V_S = 48 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IN pin							
Low level input voltage range	$V_{IN(L)}$	-0.3	–	0.8	V	–	PRQ-147
High level input voltage range	$V_{IN(H)}$	2	–	6	V	–	PRQ-148
Input voltage hysteresis	$V_{IN(HYS)}$	–	250	–	mV	–	PRQ-149
Low level input current	$I_{IN(L)}$	1	10	25	μA	V_{IN} = 0.8 V	PRQ-150
High level input current	$I_{IN(H)}$	2	10	25	μA	V_{IN} = 5.5 V	PRQ-151
DEN pin							
Low level input voltage range	$V_{DEN(L)}$	-0.3	–	0.8	V	–	PRQ-153
High level input voltage range	$V_{DEN(H)}$	2	–	6	V	–	PRQ-154
Input voltage hysteresis	$V_{DEN(HYS)}$	–	250	–	mV	–	PRQ-155
Low level input current	$I_{DEN(L)}$	1	10	25	μA	V_{DEN} = 0.8 V	PRQ-156
High level input current	$I_{DEN(H)}$	2	10	25	μA	V_{DEN} = 5.5 V	PRQ-157
OCT pin							
Analog Input Clamping Voltage of Pin OCT	$V_{OCT(CLAMP)}$	–	V_S	–	V	I_{OCT} = 1 mA	PRQ-385
Analog Overcurrent Threshold Voltage	V_{OCT}	0.46	0.51	0.56	V	$I_{OCT,MIN} \leq I_{OCT} \leq I_{OCT,MAX}$ IN = HIGH	PRQ-386
Analog adjustable Overcurrent Range	I_{OCT}	6.67	–	97.84	μA	IN = HIGH	PRQ-387
OCT short to device ground detection current	$I_{OCT(SHORT2GND)}$	150	–	240	μA	DEN = HIGH IN = LOW	PRQ-388

9 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

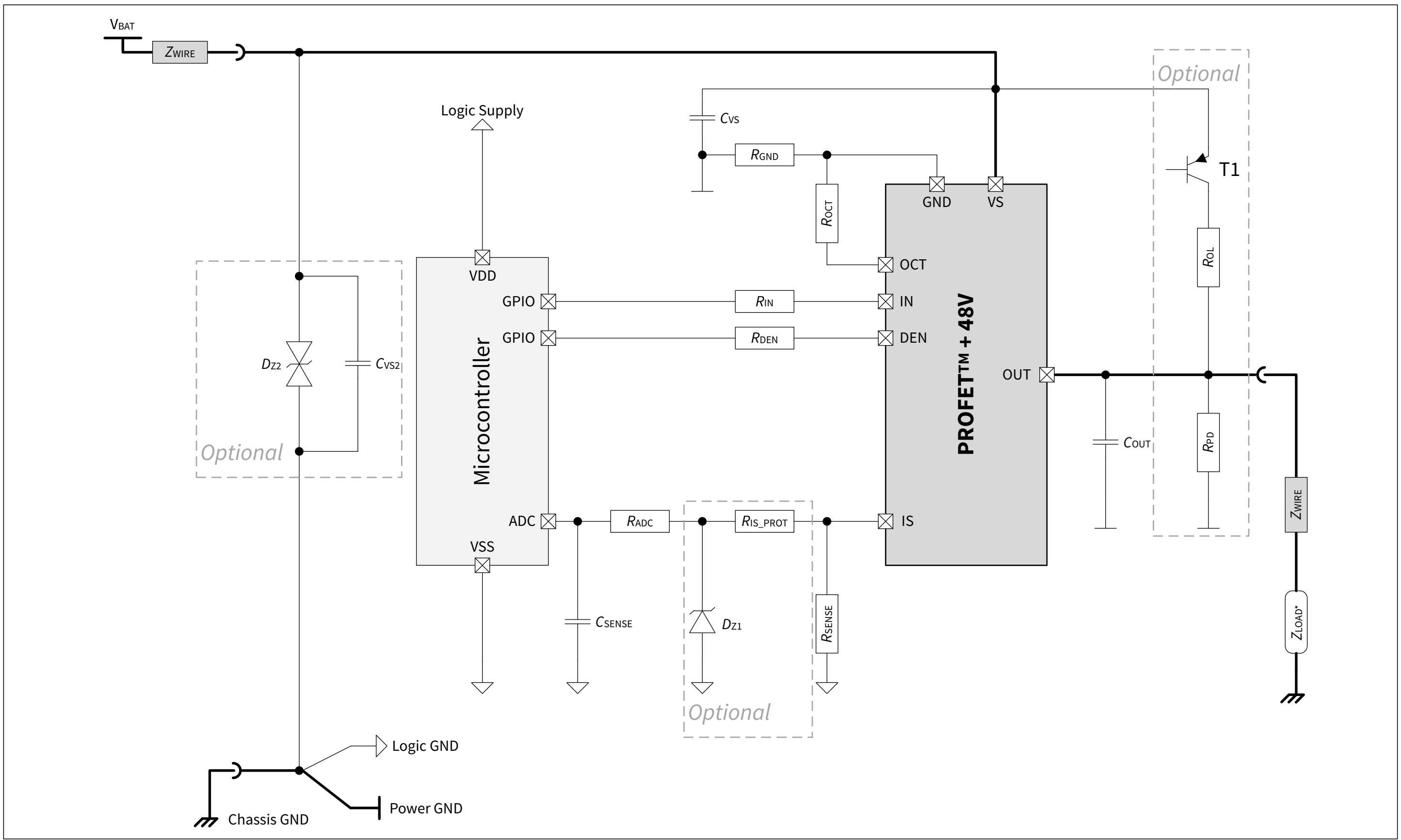


Figure 25 Application diagram

***Note**: This is a very simplified example of an application circuit. The function must be verified in the real application.*

Table 13 Bill of material

Reference	Value (typical)	Purpose
R_{IN}	10 kΩ	Protection of the microcontroller during overvoltage Enables channel switch OFF in case of loss of ground
R_{DEN}	10 kΩ	Protection of the microcontroller during overvoltage
R_{PD}	47 kΩ	Polarization of the output for short circuit to V_S detection. Improves device immunity to electromagnetic noise
R_{OL}	1.5 kΩ	Ensures polarization of the output during open load in OFF diagnostic
R_{SENSE}	1.2 kΩ	Sense resistor

(table continues...)

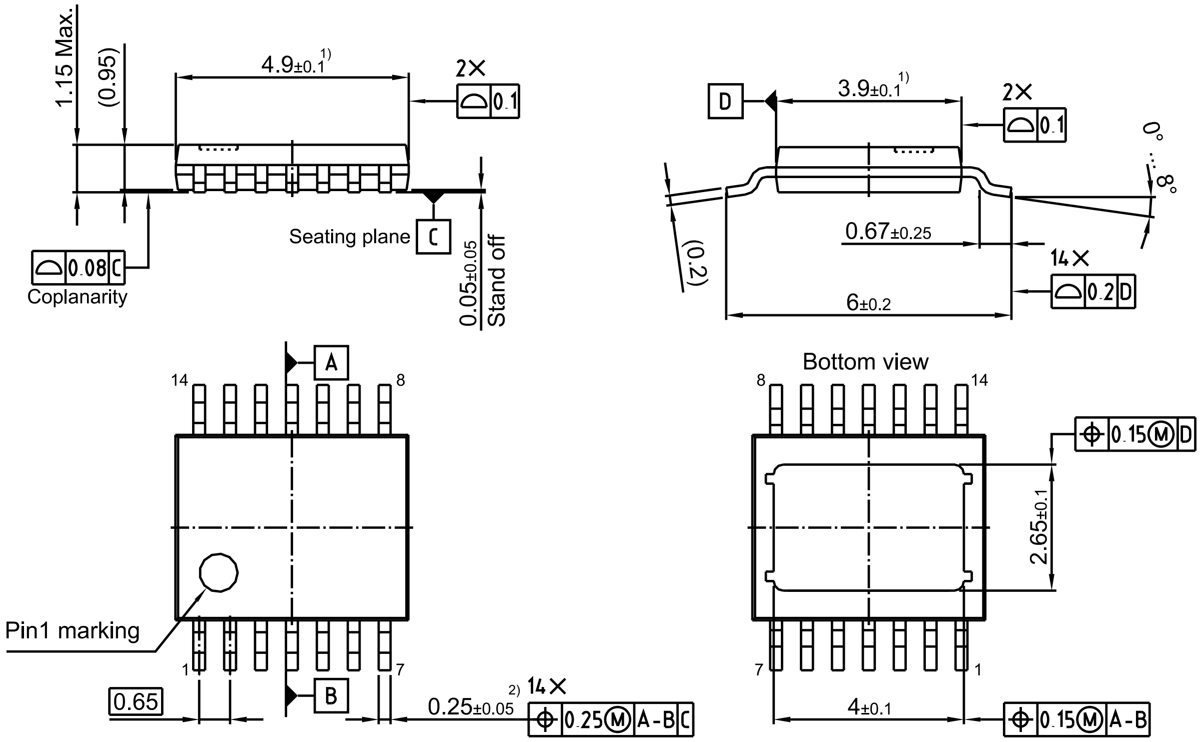
Table 13 (continued) Bill of material

Reference	Value (typical)	Purpose
R_{IS_PROT}	4.7 kΩ	Protection of the microcontroller during overvoltage and loss of ground. Value to be tuned with microcontroller specification
C_{SENSE}	100 pF	Sense signal filtering
R_{OCT}	5.3 kΩ - 70 kΩ	Adjustable overcurrent threshold with different resistors
C_{OUT}	10 nF	Protection of the device during ESD and BCI
T_1	Dual NPN/PNP	Switch the battery voltage for open load in OFF diagnostic
R_{GND}	27 Ω	Protection of the device during overvoltage
D_{Z2}	58 V Zener diode	Protection of the device during overvoltage
C_{VS2}	–	Filtering/buffer capacitor located at V_{BAT} connector. Value to be tuned according to application requirements
C_{VS}	100 nF	Filtering of voltage spikes at the battery line
R_{ADC}	4.7 kΩ	Protection of microcontroller ADC input during overvoltage, reverse polarity or loss of ground. Value to be tuned according to microcontroller specifications
D_{Z1}	7 V Zener diode	Protection of microcontroller during overvoltage. Value to be tuned according to microcontroller specifications

9.1 Further application information

- For further information, visit www.infineon.com
- Please contact Infineon for the pin behavioral assessment

10 Package



1) Does not include plastic or metal protrusion of 0.15 mm max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ±0.05; ±1°30'

Figure 26 **PG-TSDSO-14 package outline (RoHS-Compliant)**

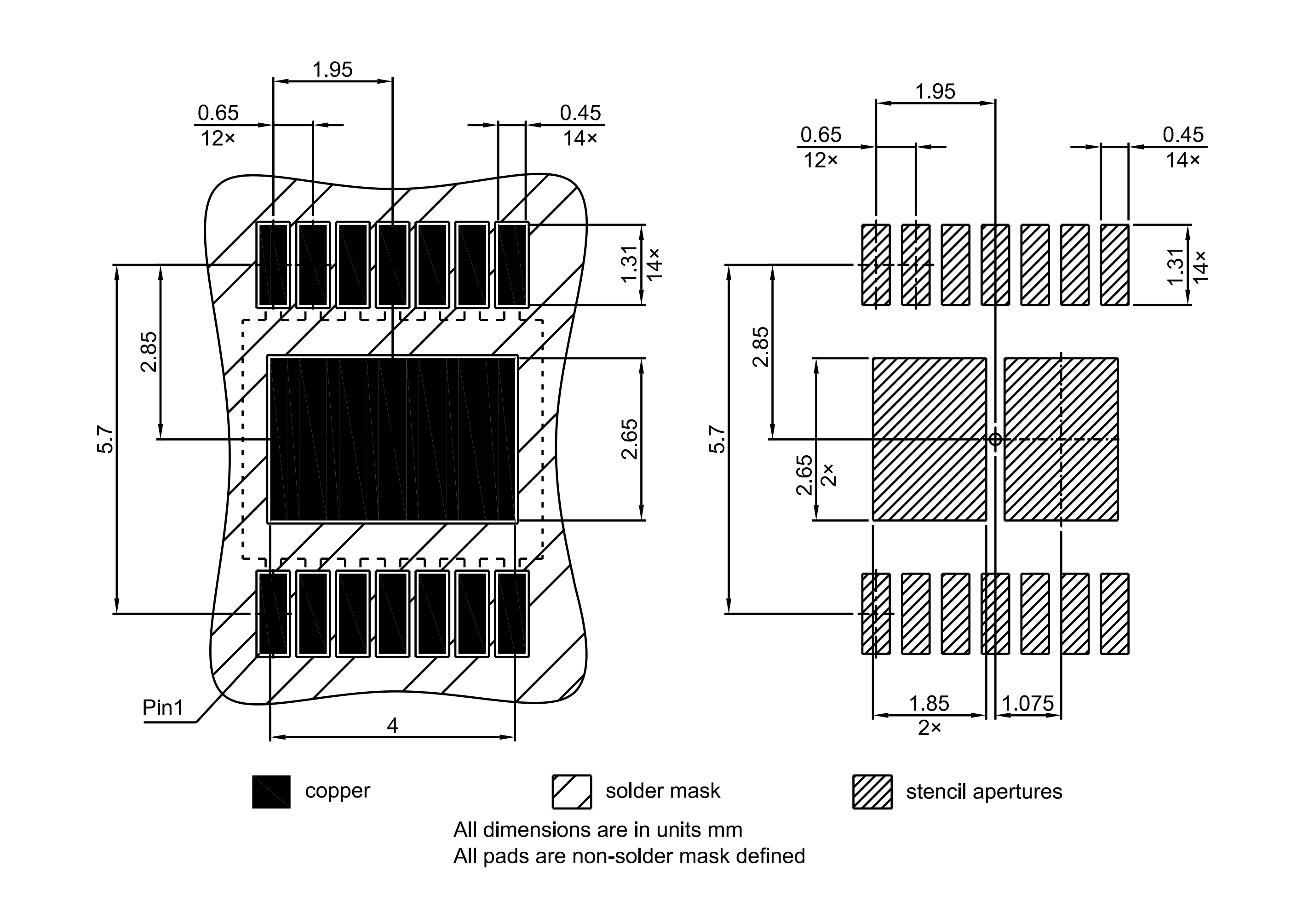


Figure 27 PG-TSDSO-14 package footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2025-11-15	• Initial document released

Trademarks

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