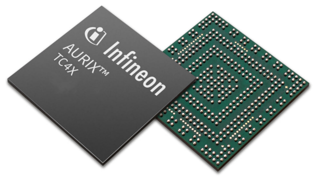
AURIX™ 3rd Generation 32-bit single-chip microcontroller



Features

- High performance microcontroller with 4 CPU cores
- CPUs are 32-bit super-scalar TriCore™ CPUs (TC1.8 LS) with virtual machine hardware support and double precision floating point arithmetic; 4 fully lockstepped cores
- Low latency SRAMs close to the CPUs
- 16 MB of embedded program NVM with multiple parallel banks and A/B swap option
- Up to 384 KB of embedded data NVM (includes both, DNVM 0 and DNVM 1)
- High performance cyber security architecture with 0.5 MB of program NVM and 128 KB of data NVM
- 1 DMA controller with 128 channels and 2 move engines
- ADC sub-system with 3 Delta-Sigma ADCs (DSADC), 10 SAR ADC cores. Each 2 SAR ADC cores share 16 inputs equipped with sample and hold stage (TMADC), 3 embedded DSP cores for flexible post processing of ADC results (CDSP)
- An eGTM timer unit with input and output channels
- High Resolution PWM
- 4 GPT12 timer units
- High speed communication interfaces (LETH, CANXL, xSPI, HSSL, SDMMC [new on AB step])
- Low speed communication interfaces (CAN, FlexRay, QSPI, ASCLIN, I2C)
- Sensor interfaces (SENT, PSI5, PSI5-S)
- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety and cyber security alarms
- Advanced debug and trace with support of run control debugging for multi-core and time aligned multi-core program and data trace for all CPUs in parallel, and 5 Gbps high speed serial trace interface
- Includes a DAP or JTAG port, with an optional DAPE port on select devices
- Digital programmable IO ports
- Volatile Memory Test (VMT) unit with ECC, memory initialization, and MBIST functions
- Power Management System and on-chip regulators
- Clock generation unit with system PLL and peripheral PLL
- Embedded voltage regulators

RoHS

AEC Qualified

Product validation

Product validation according to AEC-Q100, Grade 1.

Qualified for automotive applications.

Please read the sections "Important notice" and "Warnings" at the end of this document

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1 Device feature set

1.1 Device feature set description

The TC48x product has the following features:

- High performance microcontroller with 4 CPU cores
- 4 fully lock-stepped 32-bit super-scalar TriCore™ CPUs (TC1.8 LS) with hardware virtualization, overlay support (new on AB step), and double precision floating point arithmetic
- SRAM
  - Low latency SRAMs close to the CPUs, up to 3264 Kbyte
- Embedded NVM
  - Data NVM up to 384 Kbyte
  - Program NVM up to 16.5 Mbyte
  - Support of software over the air (SOTA) updates with improved A/B swap option
- High performance cyber security architecture
  - Cyber security real-time module (CSRM) with TriCore™ CPU with local low latency SRAM, private program and data NVM and security hardware accelerators
  - Cyber security satellite (CSS) with accelerators for various symmetric cryptographic algorithms, such as AES, SHA, and ChaChaPoly, multi-channel architecture for high throughput and accessible for all CPUs
- 1 DMA controller with 128 channels and 2 move engines
- ADC sub-system with
  - 3 Delta-Sigma ADCs (DSADC)
  - 10 SAR ADC cores. Each 2 SAR ADC cores share 16 inputs equipped with sample and hold stage (TMADC)
  - 3 embedded DSP cores for flexible post processing of ADC results (CDSP)
- An eGTM timer unit with 24 input and 72 output channels
- High Resolution PWM
- High speed communication interfaces
  - 3 x 10/100 Mbps Ethernet ports
  - A data routing engine (DRE) for low latency CAN routing, CAN to IEEE 1722 Ethernet packet translation, Ethernet to Ethernet routing
  - 2 CANXL nodes supporting up to 20* Mbps (*only with Fast pads)
  - 2 HSSL links
  - 1 SDMMC interface (new on AB step)
- Memory interfaces
  - xSPI supporting up to Quad
- Low speed communication interfaces
  - 20 CAN nodes with integrated CAN-to-CAN messages routing
  - 2 FlexRay channels
  - 8 Queued SPI channels with up to 16 chip selects each
  - 20 ASCLIN channels
  - 2 I2C interfaces
- Sensor Interfaces
  - 2 SENT modules with 15 channels each
  - 2 PSI5 channels, 1 PSI5-S module

- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety and cyber security alarms
- Advanced debug and trace
  - Rich support of run control debugging for multi-core, time aligned multi-core program and data trace for all CPUs in parallel
  - SGBT interface based on Aurora protocol
  - Up to 5 Gbps high speed serial trace interface
  - Use of Ethernet ports for debug and trace purposes
  - Includes a DAP or JTAG port, with an optional DAPE port on select devices
- Digital programmable IO ports
- Volatile Memory Test (VMT) with ECC, memory initialization and MBIST functions
- Power Management System and on-chip regulators
- Clock generation unit with system PLL and peripheral PLL
- Embedded voltage regulators

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself. That is, its function set, the temperature range, and the supply voltage
- The package and the type of delivery

This document describes the derivatives of the device. The following tables enumerates these derivatives and summarizes the differences.

1.2 Device feature set table

Table 1 Device feature set table

Feature		TC48x STD
CPUs	Type	TC1.8 LS
	Cores / checker cores	4 / 4
	Maximum frequency	400 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB for CPU 0, 1, 2, and 3
	DSPR	240 KB for CPU 0, 1, 2, and 3
	DLMU	512 KB for CPU 0, 1, 2, and 3
SRAM global	LMU	-
Program NVM	Size	4 MB (2x2 MB) each for CPU 0, 1, 2, and 3
	Banks	8
Data NVM	Size (single-ended)	D-NVM0 256 KB; D-NVM1 128 KB
CPU-CS	Type	TC1.8 non LS

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC48x STD
	Maximum frequency	200 MHz
Cache CPU-CS	Program	32 KB
	Data	16 KB
SRAM CPU-CS	PSPR	64 KB
	DSPR	112 KB
	DLMU	-
Program NVM CPU-CS	Size	0.5 MB
CSS	AES engine	3
	Channel 0	204 bytes Input FIFO and 256 bytes Output FIFO
	Channel 1-2	1548 bytes Input FIFO and 1536 bytes Output FIFO
	Channel 3-20	268 bytes Input FIFO and 192 bytes Output FIFO
PPU	Scalar core	-
	Vector width	-
	Cache	-
	VCCM	-
	CSM	-
	Vector DSP unit	-
	Maximum frequency	-
DMA	Channels	DMA0 128 ch
TMADC	SAR cores	10
	Sample and hold circuitry per 2 SAR cores	16
FC	Channels	-
DSADC	Channels	3
EXMOD	Channels	-
CDSP	Cores	3
	Data SRAM per core	3 KB
	Program SRAM per core	3 KB
GTM Classic	TIM	-
	TOM	-
	ATOM	-
	MCS	-

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC48x STD
	PSM RAM (FIFO, 1024 x 29 bit)	-
	TBU channels	-
	SPE	-
	BRC / DPLL	-
	DTM modules	-
eGTM	TIM	3 TIM * 8 ch = 24 input ch
	TOM	3 TOM * 16 ch = 48 16-bit output ch
	ATOM	3 ATOM * 8 ch = 24 24-bit output ch
	TBU channels	3
	SPE	3
	DTM modules	12 @ TOM, 6 @ ATOM
HRPWM	High Resolution PWM channels	3 x 8
Timer	GPT12	4
STM	Modules	1 per CPU
FlexRay	Modules	1 module with A and B channel
	Channels	2
CAN	Modules	5 MCMCAN modules and 1 CANXL module
	Channels	4 channels per MCMCAN and 2 channels per CANXL
	Nodes	20 M_CAN and 2 X_CAN nodes
	Nodes which support TT-CAN	-
	CAN routing accelerator	Yes
	CAN to Ethernet	Yes
QSPI	Modules (up to 16 chip select per module)	8
	HSIC Channels	-
ASCLIN	Channels	20
I2C	Interfaces	2
SENT	Modules	2
	Channels	15 channels per module
Audio subsystem	I2S/TDM instances	-
	I2S/TDM sample rate range	-
	Mixer instances	-

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC48x STD
	Mixer source:destination conversion ratios	-
	Mixer source sample rate range	-
	Mixer destination sample rate range	-
PSI5	Channels	2
PSI5-S	Modules	1
HSSL	Modules	2
MSC	Modules	-
xSPI	xSPI External Memory Interface (SDR support)	1
SDMMC	eMMC/SD Interface	1 (new on AB step)
LETH (10/100/1000 Mbps)	Modules	-
LETH (10/100 Mbps)	Modules	3
GETH	Modules	-
PCIe	Modules	-
HSPHY	MP8G PHY	1
	DLL (used for xSPI and RGMII)	-
FCE	Modules	-
Safety support	SMU	Yes
	IOM	No
SPU	Modules	-
RIF	CSI2 Modules	-
Security	CSRM	1
Debug	OCDS	Yes
	MCDS	1 x MCDS 4P (32 KB TBUF)
	SGBT	Yes for all ED
	DAPE	Yes for all ED
EVR	Type	EVRC Core Regulator
Low power features	Standby RAM	128 KB dLMU0 + 128 KB dLMU1
	SCR	Yes
Packages	Type	PG-LFBGA-292
IO	Type	5 V CMOS, 3.3 V CMOS, LVDS, and 1.8 V pad support

2 Marking options

2.1 Product name identifier

The product name details the following information:

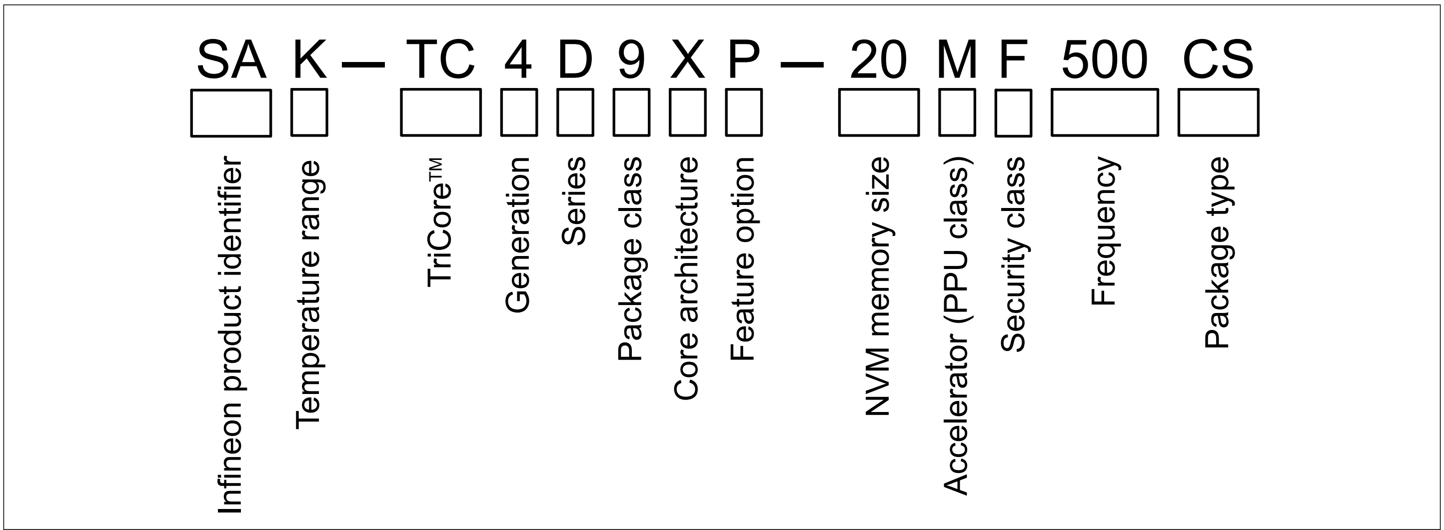


Figure 1 **Example of a product name**

Table 2 **Encoding of the product name**

Identifier	**Encoding**
Temperature range	
K	$T_{ambient}$ Temperature Range from -40°C up to +125°C
A	$T_{ambient}$ Temperature range from -40°C up to +105°C
L	$T_{ambient}$ Temperature range from -40°C up to +150°C
Series	
D	**D**omain, Zone
Z	**Z**one
9	Real-time control
8	Domain, Zone
6	Real-time control
5	Radar
4	Chassis, Zone
2	Chassis, Safety
E	**E**lectrification
P	**P**ower conversion
S	**S**afety
Package class	
5	188 - PIN

(table continues...)

Table 2 **(continued) Encoding of the product name**

Identifier	Encoding
6	224 - PIN
7	292 - PIN
9	436 - PIN
Core architecture	
L	Single Core
D	Dual Core
T	Triple Core
Q	Quad Core
P	Penta Core
X	Hexa Core
Feature option	
P	Standard
Q	Standard + CAN-XL
C, M, V	Customer specific
E	Emulation device (available only up to engineering sample maturity)
X	Extended feature
NVM memory size	
03	3 MB
04	4 MB
05	5 MB
06	6 MB
08	8 MB
12	12 MB
16	16 MB
20	20 MB
24	24 MB
Accelerator (PPU class)	
N	No PPU
E	PPU 128 bits
M	PPU 256 bits
Security class	
F	Full CSRM (1x TC 1.8 + private NVM)

(table continues...)

Table 2 (continued) Encoding of the product name

Identifier	Encoding
O	Full CSRM + SMx (1x TC 1.8 + private NVM)
Frequency	
400	400 MHz
500	500 MHz
Package type	
CC	BGA - CuP COM
CS	BGA - CuP STD
MC	BGA - OvM COM
MS	BGA - OvM STD
MR	BGA - OvM (Radar)

2.2 TC48x AA step variants

2.2.1 TC48x_AA step (Part 1)

A table listing the TC48x AA step variants.

Table 3 TC48x_AA step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
Step				
AA	AA	AA	AA	AA
Production Status				
Standard	Standard	Standard	Standard	Standard
Package Type				
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout				
BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm
Reference Silicon				
TC48x	TC48x	TC48x	TC48x	TC48x
Temperature Range (Ambient)				
SAK	SAK	SAK	SAK	SAK
Chip ID				
0x61E14923	0x61E2C923	0x61E2C9A3	0x61E14123	0x61E149A3

(table continues...)

Table 3 (continued) TC48x_AA step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
Cores / Checker Cores				
4/4	4/4	4/4	4/4	4/4
Max. Freq. (MHz)				
400	400	400	400	400
NVM Type				
RRAM	RRAM	RRAM	RRAM	RRAM
Program NVM (MB)				
16	16	16	12	16
Data NVM0 (KB)				
256	256	256	256	256
Total SRAM (without Cache) (KB)				
3440	3440	3440	3440	3440
Extension memory(KB)				
0	0	0	0	0
DSPR (KB)				
240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM
DLMU (KB)				
512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM
PSPR (KB)				
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support				
Yes	Yes	Yes	Yes	Yes
CSRM Available				
1	1	1	1	1
CSS Availability				
Yes	Yes	Yes	Yes	Yes
PPU Availability				
0	0	0	0	0
ADC - TMADC (Instances / Cores)				
5/10	5/10	5/10	5/10	5/10

(table continues...)

Table 3 (continued) TC48x_AA step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
ADC - Fast Compare Converters				
0	0	0	0	0
ADC - DS Converters				
3	3	3	3	3
DSEXMOD				
0	0	0	0	0
CDSP Cores				
3	3	3	3	3
HRPWM Instances				
3	3	3	3	3
GTM Classic / eGTM availability				
No / Yes	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)				
0	0	0	0	0
Light Ethernet (LETH) Instances (Mbps)				
3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)
PCIe Instances				
0	0	0	0	0
CAN (Modules/Nodes)				
5/5x4	5/5x4	5/5x4	5/5x4	5/5x4
CANXL(Modules/Nodes)				
0/0	1/2	1/2	0/0	0/0
FlexRay (Modules/Channels)				
1/1x2	1/1x2	1/1x2	1/1x2	1/1x2
HSSL Modules				
2	2	2	2	2
ASCLIN Modules				
20	20	20	20	20
QSPI Modules				
8	8	8	8	8
I2C Interfaces				
2	2	2	2	2

(table continues...)

Table 3 (continued) TC48x_AA step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
xSPI Module				
1	1	1	1	1
SENT Channels				
30	30	30	30	30
MSC Modules				
0	0	0	0	0
PSI5 Channels				
2	2	2	2	2
PSI5-S Module				
1	1	1	1	1
SDMMC Module				
No	No	No	No	No
Audio-TDM/I2S interfaces				
0	0	0	0	0
SGBT availability				
No	No	No	No	No
MCDS availability				
Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
DAPE availability				
No	No	No	No	No
CSI2 Interface				
0	0	0	0	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance				
No/0/0	No/0/0	No/0/0	No/0/0	No/0/0

2.2.2 TC48x_AA step (Part 2)

A continuation table listing the TC48x AA step variants.

Table 4 TC48x_AA step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Step			
AA	AA	AA	AA

(table continues...)

Table 4 (continued) TC48x_AA step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Production Status			
Standard	Standard	Emulation device	Emulation device
Package Type			
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout			
BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm
Reference Silicon			
TC48x	TC48x	TC48x	TC48x
Temperature Range (Ambient)			
SAK	SAK	SAK	SAK
Chip ID			
0x61E141A3	0x61E23123	0x61E44923	0x61E449A3
Cores / Checker Cores			
4/4	4/4	4/4	4/4
Max. Freq. (MHz)			
400	400	400	400
NVM Type			
RRAM	RRAM	RRAM	RRAM
Program NVM (MB)			
12	8	16	16
Data NVM0 (KB)			
256	256	256	256
Total SRAM (without Cache) (KB)			
3440	3440	3440	3440
Extension memory(KB)			
0	0	0	0
DSPR (KB)			
240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM
DLMU (KB)			
512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM
PSPR (KB)			
64 per CPU	64 per CPU	64 per CPU	64 per CPU

(table continues...)

Table 4 (continued) TC48x_AA step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Hypervisor Support			
Yes	Yes	Yes	Yes
CSRM Available			
1	1	1	1
CSS Availability			
Yes	Yes	Yes	Yes
PPU Availability			
0	0	0	0
ADC - TMADC (Instances / Cores)			
5/10	5/10	5/10	5/10
ADC - Fast Compare Converters			
0	0	0	0
ADC - DS Converters			
3	3	3	3
DSEXMOD			
0	0	0	0
CDSP Cores			
3	3	3	3
HRPWM Instances			
3	3	3	3
GTM Classic / eGTM availability			
No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)			
0	0	0	0
Light Ethernet (LETH) Instances (Mbps)			
3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)
PCIe Instances			
0	0	0	0
CAN (Modules/Nodes)			
5/5x4	5/5x4	5/5x4	5/5x4
CANXL(Modules/Nodes)			
0/0	0/0	1/2	1/2

(table continues...)

Table 4 (continued) TC48x_AA step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
FlexRay (Modules/Channels)			
1/1x2	1/1x2	1/1x2	1/1x2
HSSL Modules			
2	2	2	2
ASCLIN Modules			
20	20	20	20
QSPI Modules			
8	8	8	8
I2C Interfaces			
2	2	2	2
xSPI Module			
1	1	1	1
SENT Channels			
30	30	30	30
MSC Modules			
0	0	0	0
PSI5 Channels			
2	2	2	2
PSI5-S Module			
1	1	1	1
SDMMC Module			
No	No	No	No
Audio-TDM/I2S interfaces			
0	0	0	0
SGBT availability			
No	No	Yes	Yes
MCDS availability			
Limited MCDS	Limited MCDS	MCDS 4P	MCDS 4P
DAPE availability			
No	No	Yes	Yes
CSI2 Interface			
0	0	0	0

(table continues...)

Table 4 (continued) TC48x_AA step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance			
No/0/0	No/0/0	No/0/0	No/0/0

2.3 TC48x AB step variants

2.3.1 TC48x_AB step (Part 1)

A table listing the TC48x AB step variants.

Table 5 TC48x_AB step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
Step				
AB	AB	AB	AB	AB
Production Status				
Standard	Standard	Standard	Standard	Standard
Package Type				
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout				
BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm
Reference Silicon				
TC48x	TC48x	TC48x	TC48x	TC48x
Temperature Range (Ambient)				
SAK	SAK	SAK	SAK	SAK
Chip ID				
0x61E14923	0x61E2C923	0x61E2C9A3	0x61E14123	0x61E149A3
Cores / Checker Cores				
4/4	4/4	4/4	4/4	4/4
Max. Freq. (MHz)				
400	400	400	400	400
NVM Type				
RRAM	RRAM	RRAM	RRAM	RRAM
Program NVM (MB)				
16	16	16	12	16

(table continues...)

Table 5 (continued) TC48x_AB step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
Data NVM0 (KB)				
256	256	256	256	256
Total SRAM (without Cache) (KB)				
3440	3440	3440	3440	3440
Extension memory(KB)				
0	0	0	0	0
DSPR (KB)				
240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM
DLMU (KB)				
512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM
PSPR (KB)				
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support				
Yes	Yes	Yes	Yes	Yes
CSRM Available				
1	1	1	1	1
CSS Availability				
Yes	Yes	Yes	Yes	Yes
PPU Availability				
0	0	0	0	0
ADC - TMADC (Instances / Cores)				
5/10	5/10	5/10	5/10	5/10
ADC - Fast Compare Converters				
0	0	0	0	0
ADC - DS Converters				
3	3	3	3	3
DSEXMOD				
0	0	0	0	0
CDSP Cores				
3	3	3	3	3

(table continues...)

Table 5 (continued) TC48x_AB step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
HRPWM Instances				
3	3	3	3	3
GTM Classic / eGTM availability				
No / Yes	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)				
0	0	0	0	0
Light Ethernet (LETH) Instances (Mbps)				
3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)
PCIe Instances				
0	0	0	0	0
CAN (Modules/Nodes)				
5/5x4	5/5x4	5/5x4	5/5x4	5/5x4
CANXL(Modules/Nodes)				
0/0	1/2	1/2	0/0	0/0
FlexRay (Modules/Channels)				
1/1x2	1/1x2	1/1x2	1/1x2	1/1x2
HSSL Modules				
2	2	2	2	2
ASCLIN Modules				
20	20	20	20	20
QSPI Modules				
8	8	8	8	8
I2C Interfaces				
2	2	2	2	2
xSPI Module				
1	1	1	1	1
SENT Channels				
30	30	30	30	30
MSC Modules				
0	0	0	0	0
PSI5 Channels				
2	2	2	2	2

(table continues...)

Table 5 (continued) TC48x_AB step (Part 1)

SAK-TC487QP-16NF400MS	SAK-TC487QQ-16NF400MS	SAK-TC487QQ-16NO400MS	SAK-TC487QP-12NF400MS	SAK-TC487QP-16NO400MS
PSI5-S Module				
1	1	1	1	1
SDMMC Module				
Yes	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces				
0	0	0	0	0
SGBT availability				
No	No	No	No	No
MCDS availability				
Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
DAPE availability				
No	No	No	No	No
CSI2 Interface				
0	0	0	0	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance				
No/0/0	No/0/0	No/0/0	No/0/0	No/0/0

2.3.2 TC48x_AB step (Part 2)

A continuation table listing the TC48x AB step variants.

Table 6 TC48x_AB step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Step			
AB	AB	AB	AB
Production Status			
Standard	Standard	Emulation device	Emulation device
Package Type			
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout			
BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm	BGA292_STD 0.8 mm
Reference Silicon			
TC48x	TC48x	TC48x	TC48x

(table continues...)

Table 6 (continued) TC48x_AB step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
Temperature Range (Ambient)			
SAK	SAK	SAK	SAK
Chip ID			
0x61E141A3	0x61E23123	0x61E44923	0x61E449A3
Cores / Checker Cores			
4/4	4/4	4/4	4/4
Max. Freq. (MHz)			
400	400	400	400
NVM Type			
RRAM	RRAM	RRAM	RRAM
Program NVM (MB)			
12	8	16	16
Data NVM0 (KB)			
256	256	256	256
Total SRAM (without Cache) (KB)			
3440	3440	3440	3440
Extension memory(KB)			
0	0	0	0
DSPR (KB)			
240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM	240 in CPU0,1,2,3; 112 in CSRM
DLMU (KB)			
512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM	512 in CPU 0,1,2,3; 0 in CSRM
PSPR (KB)			
64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support			
Yes	Yes	Yes	Yes
CSRM Available			
1	1	1	1
CSS Availability			
Yes	Yes	Yes	Yes
PPU Availability			
0	0	0	0

(table continues...)

Table 6 (continued) TC48x_AB step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
ADC - TMADC (Instances / Cores)			
5/10	5/10	5/10	5/10
ADC - Fast Compare Converters			
0	0	0	0
ADC - DS Converters			
3	3	3	3
DSEXMOD			
0	0	0	0
CDSP Cores			
3	3	3	3
HRPWM Instances			
3	3	3	3
GTM Classic / eGTM availability			
No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)			
0	0	0	0
Light Ethernet (LETH) Instances (Mbps)			
3x (10/100)	3x (10/100)	3x (10/100)	3x (10/100)
PCIe Instances			
0	0	0	0
CAN (Modules/Nodes)			
5/5x4	5/5x4	5/5x4	5/5x4
CANXL(Modules/Nodes)			
0/0	0/0	1/2	1/2
FlexRay (Modules/Channels)			
1/1x2	1/1x2	1/1x2	1/1x2
HSSL Modules			
2	2	2	2
ASCLIN Modules			
20	20	20	20
QSPI Modules			
8	8	8	8

(table continues...)

Table 6 (continued) TC48x_AB step (Part 2)

SAK-TC487QP-12NO400MS	SAK-TC487QC-08NF400MS	SAK-TC487QE-16NF400MS	SAK-TC487QE-16NO400MS
I2C Interfaces			
2	2	2	2
xSPI Module			
1	1	1	1
SENT Channels			
30	30	30	30
MSC Modules			
0	0	0	0
PSI5 Channels			
2	2	2	2
PSI5-S Module			
1	1	1	1
SDMMC Module			
Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces			
0	0	0	0
SGBT availability			
No	No	Yes	Yes
MCDS availability			
Limited MCDS	Limited MCDS	MCDS 4P	MCDS 4P
DAPE availability			
No	No	Yes	Yes
CSI2 Interface			
0	0	0	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance			
No/0/0	No/0/0	No/0/0	No/0/0

3 Pin definition and functions

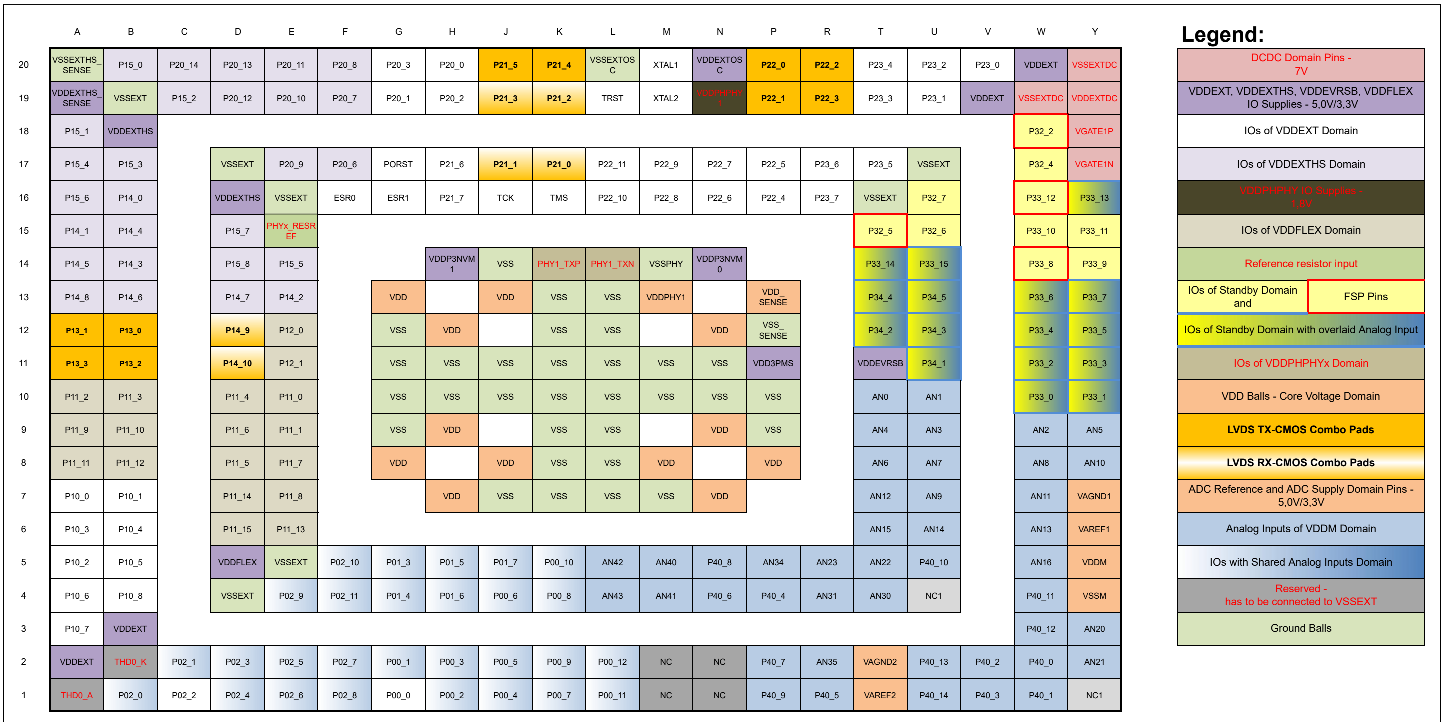
***Note**: Functions listed in the largest package of this device might not be available for smaller packages because of pin limitations.*

***Note**: To meet the specified RMII timing requirements for transmission outputs, select the appropriate RMII alternate output function (e.g. 'LETH0_P2_RMIIB_TXEN'). If the pin configuration table shows an associated registered RMII output for that pad as PO in "Ctrl" column (e.g. 'LETH0_P2_RMIIRB_TXEN'), then the corresponding 'PCSRSEL' bit for that pin slice shall be set to '1' to select the registered output path. If no registered mapping is listed as PO for that pad, 'PCSRSEL' does not need to be set for RMII output operation.*

In addition, to meet the specified timing requirements for the following functional blocks (XSPI, HSCT, HRPWM), 'PCSRSEL' bit for that pin slice shall be set to '1' if the signal is listed as PO for that pad.

3.1 Logic symbols for package variants

- BGA-292 STD, see Figure 2



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	VSSEXTHS_SENSE	P15_0	P20_14	P20_13	P20_11	P20_8	P20_3	P20_0	P21_5	P21_4	VSSEXTOSC	XTAL1	VDDEXTOSC	P22_0	P22_2	P23_4	P23_2	P23_0	VDDEXT	VSSEXTDC
19	VDDEXTHS_SENSE	VSSEXT	P15_2	P20_12	P20_10	P20_7	P20_1	P20_2	P21_3	P21_2	TRST	XTAL2	VDDPHPHY1	P22_1	P22_3	P23_3	P23_1	VDDEXT	VSSEXTDC	VDDEXTDC
18	P15_1	VDDEXTHS																	P32_2	VGATE1P
17	P15_4	P15_3		VSSEXT	P20_9	P20_6	PORST	P21_6	P21_1	P21_0	P22_11	P22_9	P22_7	P22_5	P23_6	P23_5	VSSEXT		P32_4	VGATE1N
16	P15_6	P14_0		VDDEXTHS	VSSEXT	ESR0	ESR1	P21_7	TCK	TMS	P22_10	P22_8	P22_6	P22_4	P23_7	VSSEXT	P32_7		P33_12	P33_13
15	P14_1	P14_4		P15_7	PHYx_RESREF											P32_5	P32_6		P33_10	P33_11
14	P14_5	P14_3		P15_8	P15_5			VDDP3NVM1	VSS	PHY1_TXP	PHY1_TXN	VSSPHY	VDDP3NVM0			P33_14	P33_15		P33_8	P33_9
13	P14_8	P14_6		P14_7	P14_2		VDD		VDD	VSS	VSS	VDDPHY1		VDD_SENSE		P34_4	P34_5		P33_6	P33_7
12	P13_1	P13_0		P14_9	P12_0		VSS	VDD		VSS	VSS		VDD	VSS_SENSE		P34_2	P34_3		P33_4	P33_5
11	P13_3	P13_2		P14_10	P12_1		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD3PMS		VDDEVRSB	P34_1		P33_2	P33_3
10	P11_2	P11_3		P11_4	P11_0		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		AN0	AN1		P33_0	P33_1
9	P11_9	P11_10		P11_6	P11_1		VSS	VDD		VSS	VSS		VDD	VSS		AN4	AN3		AN2	AN5
8	P11_11	P11_12		P11_5	P11_7		VDD		VDD	VSS	VSS	VDD		VDD		AN6	AN7		AN8	AN10
7	P10_0	P10_1		P11_14	P11_8			VDD	VSS	VSS	VSS	VSS	VDD			AN12	AN9		AN11	VAGND1
6	P10_3	P10_4		P11_15	P11_13											AN15	AN14		AN13	VAREF1
5	P10_2	P10_5		VDDFLEX	VSSEXT	P02_10	P01_3	P01_5	P01_7	P00_10	AN42	AN40	P40_8	AN34	AN23	AN22	P40_10		AN16	VDDM
4	P10_6	P10_8		VSSEXT	P02_9	P02_11	P01_4	P01_6	P00_6	P00_8	AN43	AN41	P40_6	P40_4	AN31	AN30	NC1		P40_11	VSSM
3	P10_7	VDDEXT																	P40_12	AN20
2	VDDEXT	THD0_K	P02_1	P02_3	P02_5	P02_7	P00_1	P00_3	P00_5	P00_9	P00_12	NC	NC	P40_7	AN35	VAGND2	P40_13	P40_2	P40_0	AN21
1	THD0_A	P02_0	P02_2	P02_4	P02_6	P02_8	P00_0	P00_2	P00_4	P00_7	P00_11	NC	NC	P40_9	P40_5	VAREF2	P40_14	P40_3	P40_1	NC1

Figure 2 **Logic symbol for the package variant BGA-292 STD**

Related information

BGA292_STD package variant pin configuration on page 28
Pad Sequence on page 173
Legend on page 199

3.2 BGA292_STD package variant pin configuration

Related information

Logic symbols for package variants on page 28
BGA292_STD package variant pin configuration on page 28
Pad Sequence on page 173

Legend on page 199

3.2.1 BGA292_STD port 00

Table 7 Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
G1	P00.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GPT121_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	EGTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	EGTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	P00.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	ASCLIN13_ATX_F	O4		Transmit output
	CAN10_TXD	O5		CAN transmit output node 0
	PSI5_TX0	O6		TXD outputs (send data)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT9	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G2	P00.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	GPT121_T2INA			Trigger/gate input of timer T2
	SENT0_SENT0B			Receive input channel 0
	EGTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1
	EGTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH11	AI		Analog Input for TMADC2 Channel 11
	P00.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	SENT0_SPC0	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT10	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H1	P00.2	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	I2C0_SCLG			Serial Clock Input 6
	SENT1_SENT0B			Receive input channel 0
	GPT121_T2EUDA			Count direction control input of timer T2
	EGTM_CDTM1_DTM2_5			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_5			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH10	AI		Analog Input for TMADC2 Channel 10
	P00.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	CAN21_TXD	O3		CAN transmit output node 1
	PSI5_TX0	O4		TXD outputs (send data)

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI3_SLSO4	O6		Master slave select output
	I2C0_SCL	O7		Serial Clock Output
	—	O8		Reserved
	EGTM_TOUT11	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H2	P00.3	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	I2C0_SDAG			Serial Data Input 6
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	CAN21_RXDA			CAN receive input node 1
	PSI5S0_RXA			RX data input
	SENT0_SENT1B			Receive input channel 1
	ASCLIN12_ARXA_F			Receive input
	EGTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	EGTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	ADC_TMADC2CH9	AI		Analog Input for TMADC2 Channel 9
	P00.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	ASCLIN12_ATX	O3		Transmit output
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	I2C0_SDA	O7		Serial Data Output
	—	O8		Reserved
	EGTM_TOUT12	O9		eGTM muxed output

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J1	P00.4	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SCU_E_REQ2C			ERU channel 2 input C
	SENT1_SENT1B			Receive input channel 1
	ASCLIN10_ARXA			Receive input
	GPT121_T5INA			Trigger/gate input of timer T5
	EGTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH8	AI		Analog Input for TMADC2 Channel 8
	P00.4	O0		General-purpose output
	—	O1		Reserved
	PSI5S0_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	—	O5		Reserved
	SENT1_SPC1	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT13	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J2	P00.5	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT2B			Receive input channel 2
	GPT121_T5EUDA			Count direction control input of timer T5
	CAN11_RXDB			CAN receive input node 1

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN12_ARXB_F			Receive input
	EGTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_2			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	ADC_TMADC2CH7	AI		Analog Input for TMADC2 Channel 7
	P00.5	O0		General-purpose output
	—	O1		Reserved
	ADC_PWM1	O2		Negative PWM
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	SENT0_SPC2	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT14	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J4	P00.6	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT2B			Receive input channel 2
	ASCLIN5_ARXA			Receive input
	GPT121_T6EUDA			Count direction control input of core timer T6
	EGTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	ADC_TMADC2CH6	AI		Analog Input for TMADC2 Channel 6
	P00.6	O0		General-purpose output
	—	O1		Reserved
	ADC_PWM0	O2		Positive PWM

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC2	O6		Transmit output
	GPT121_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT15	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K1	P00.7	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT3B			Receive input channel 3
	GPT120_T2INA			Trigger/gate input of timer T2
	GPT121_T6INA			Trigger/gate input of core timer T6
	EGTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_3			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_3			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	ADC_TMADC2CH5	AI		Analog Input for TMADC2 Channel 5
	P00.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	SENT0_SPC3	O6		Transmit output
	—	O7		Reserved

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT16	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K4	P00.8	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT3B			Receive input channel 3
	ASCLIN10_ARXB			Receive input
	EGTM_CDTM1_DTM3_2			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	EGTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	ADC_TMADC2CH4	AI		Analog Input for TMADC2 Channel 4
	P00.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	CAN40_TXD	O4		CAN transmit output node 0
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT17	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K2	P00.9	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT4B			Receive input channel 4
	GPT120_T4EUDA			Count direction control input of timer T4
	ASCLIN13_ARXA_F			Receive input
	ASCLIN4_ARXG			Receive input
	EGTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	ADC_TMADC2CH3	AI		Analog Input for TMADC2 Channel 3
	P00.9	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	ADC_EMUXCTRL13	O4		EMUX1 Control from TMADC to PORTS
	ASCLIN4_ATX	O5		Transmit output
	SENT0_SPC4	O6		Transmit output
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved
	EGTM_TOUT18	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K5	P00.10	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT4B			Receive input channel 4
	ASCLIN10_ARXE			Receive input
	GPT121_T3EUDA			Count direction control input of core timer T3
	EGTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC2CH2	AI		Analog Input for TMADC2 Channel 2
	P00.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN13_ATX	O3		Transmit output
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	SENT1_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT19	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L1	P00.11	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT5B			Receive input channel 5
	ASCLIN13_ARXB_F			Receive input
	CAN40_RXDA			CAN receive input node 0
	GPT121_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	ADC_TMADC2CH1	AI		Analog Input for TMADC2 Channel 1
	P00.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	ASCLIN13_ATX	O3		Transmit output
	—	O4		Reserved

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT20	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L2	P00.12	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	SENT1_SENT5B			Receive input channel 5
	GPT121_T4INA			Trigger/gate input of timer T4
	EGTM_CDTM0_DTM2_5			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_5			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	ADC_TMADC2CH0	AI		Analog Input for TMADC2 Channel 0
	P00.12	O0		General-purpose output
	—	O1		Reserved
	ADC_EMUXCTRL30	O2		EMUX3 Control from TMADC to PORTS
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT21	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 7 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.2 BGA292_STD port 01

Table 8 Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
G5	P01.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SLSIB			Slave select input
	SENT1_SENT12A			Receive input channel 12
	CAN32_RXDA			CAN receive input node 2
	LETH0_P0_MDIOB			LETH PortX MDIO interface data input
	LETH0_P0_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	EGTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	ADC_TMADC2CH14	AI		Analog Input for TMADC2 Channel 14
	P01.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	—	O3		Reserved
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	SENT1_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT111	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 8 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G4	P01.4	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN01_RXDC			CAN receive input node 1
	SENT0_SENT13A			Receive input channel 13
	EGTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	EGTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH13	AI		Analog Input for TMADC2 Channel 13
	P01.4	O0		General-purpose output
	—	O1		Reserved
	ADC_EMUXCTRL21	O2		EMUX2 Control from TMADC to PORTS
	ASCLIN9_ASLSO	O3		Slave select signal output
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT112	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H5	P01.5	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MRSTC			Master SPI data input
	ASCLIN9_ARXA_F			Receive input
	SENT1_SENT13A			Receive input channel 13
	CANXL00_RXDG			CANXL receive input node 0
	EGTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	EGTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	LETH0_P0_RXDG			LETH PortX TC14 interface receive data input

(table continues...)

Table 8 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC2CH12	AI		Analog Input for TMADC2 Channel 12
	P01.5	O0		General-purpose output
	—	O1		Reserved
	ADC_EMUXCTRL20	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT113	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H4	P01.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MTSRC			Slave SPI data input
	CAN32_RXDD			CAN receive input node 2
	EGTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	ADC_TMADC4CH8	AI		Analog Input for TMADC4 Channel 8
	P01.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN12_ATX	O2		Transmit output
	ASCLIN9_ASCLK_F	O3		Shift clock output
	QSPI3_MTSR	O4		Master SPI data output
	ASCLIN9_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 8 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT114	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J5	P01.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SCLKC			Slave SPI clock inputs
	ASCLIN9_ARXB_F			Receive input
	EGTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	ADC_TMADC4CH9	AI		Analog Input for TMADC4 Channel 9
	P01.7	O0		General-purpose output
	—	O1		Reserved
	ADC_EMUXCTRL22	O2		EMUX2 Control from TMADC to PORTS
	ASCLIN9_ATX_F	O3		Transmit output
	QSPI3_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT115	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.3 BGA292_STD port 02

Table 9 Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B1	P02.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXG			Receive input
	SCU_E_REQ3C			ERU channel 3 input C
	CAN31_RXDC			CAN receive input node 1
	ADC_TRIG56			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	ADC_TMADC4CH0	AI		Analog Input for TMADC4 Channel 0
	P02.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO1_F	O3		Master slave select output
	ADC_PWM1	O4		Negative PWM
	CAN00_TXD	O5		CAN transmit output node 0
	ERAY0_TXDA	O6		Transmit Channel A
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT0_F	O9		eGTM muxed output
	—	O10		Reserved
	QSPI3_SLSO5_F	O11		Master slave select output
	ASCLIN8_ASCLK_F	O12		Shift clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH0_F	PO		High resolution PWM 0 output channels
C2	P02.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2B			ERU channel 2 input B

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT14A			Receive input channel 14
	ADC_TRIG57			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	QSPI3_MRSTG_F			Master SPI data input
	CANXL00_RXDC			CANXL receive input node 0
	GPT121_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	LETH0_P0_RXDC			LETH PortX TC14 interface receive data input
	ADC_TMADC4CH1	AI		Analog Input for TMADC4 Channel 1
	P02.1	O0		General-purpose output
	—	O1		Reserved
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	ADC_PWM0	O4		Positive PWM
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT1_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
C1	P02.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT7B			Receive input channel 7
	EGTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM0_DTM2_6			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	EGTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	P02.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3_F	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDB	O6		Transmit Channel B
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O8		CANXL transmit output node 1
	EGTM_TOUT2_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN8_ASLSO_F	O12		Slave select signal output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH1_F	PO		High resolution PWM 0 output channels
D2	P02.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	PSI5_RX0B			RXD inputs (receive data) channel 0
	SENT1_SENT6B			Receive input channel 6
	EGTM_CDTM0_DTM3_6			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM3_6			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	SENT0_SENT12A			Receive input channel 12

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CANXL01_RXDC			CANXL receive input node 1
	LETH0_P1_RXDC			LETH PortX TC14 interface receive data input
	ADC_TMADC4CH2	AI		Analog Input for TMADC4 Channel 2
	P02.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT3_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D1	P02.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT6B			Receive input channel 6
	LETH0_P2_CRSD			LETH PortX MII carrier sense
	QSPI3_SLSIA_F			Slave select input
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	EGTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	EGTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1
	LETH0_P0_EDC			LETH PortX TC14 interface energy detection input

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MDIOC			LETH PortX MDIO interface data input
	ADC_TMADC4CH3	AI		Analog Input for TMADC4 Channel 3
	P02.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0_F	O3		Master slave select output
	PSI5S0_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT4_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH2_F	PO		High resolution PWM 0 output channels
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E2	P02.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT1C			Receive input channel 1
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S0_RXB			RX data input
	QSPI3_MRSTA_F			Master SPI data input
	EGTM_CDTM1_DTM3_7			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM5_6			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_6			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOC			LETH PortX MDIO interface data input
	ADC_TMADC4CH4	AI		Analog Input for TMADC4 Channel 4
	P02.5	O0		General-purpose output
	—	O1		Reserved
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST_F	O3		Slave SPI data output
	ASCLIN8_ASLSO_F	O4		Slave select signal output
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	QSPI3_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT5_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH3_F	PO		High resolution PWM 0 output channels
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E1	P02.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P0_AUX			LETH PortX auxilary snapshot signal
	SENT1_SENT0C			Receive input channel 0
	ASCLIN10_ARXH			Receive input
	GPT120_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	QSPI3_MTSRA_F			Slave SPI data input
	EGTM_CDTM0_DTM2_7			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM2_7			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	ADC_TMADC4CH5	AI		Analog Input for TMADC4 Channel 5
	P02.6	O0		General-purpose output
	—	O1		Reserved
	PSI5S0_TX	O2		TX data output
	QSPI3_MTSR_F	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT6_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH4_F	PO		High resolution PWM 0 output channels
F2	P02.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDH			CAN receive input node 2
	SENT0_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	SCU_E_REQ0F			ERU channel 0 input F
	QSPI3_SCLKA_F			Slave SPI clock inputs
	ADC_TRIG58			Triggers from PORTS to ADC
	EGTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	EGTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	EGTM_CDTM2_DTM3_6			Input mux of CDTM2_DTM3_AUXIN0/1
	ADC_TMADC4CH6	AI		Analog Input for TMADC4 Channel 6

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P02.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN8_ASLSO_F	O2		Slave select signal output
	QSPI3_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT7_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH5_F	PO		High resolution PWM 0 output channels
F1	P02.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT0C			Receive input channel 0
	GPT120_T4INA			Trigger/gate input of timer T4
	CAN30_RXDB			CAN receive input node 0
	SCU_E_REQ5G			ERU channel 5 input G
	ADC_TRIG59			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	ADC_TMADC4CH7	AI		Analog Input for TMADC4 Channel 7
	P02.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO5_F	O2		Master slave select output
	ASCLIN8_ASCLK_F	O3		Shift clock output

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT8_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH6_F	PO		High resolution PWM 0 output channels
E4	P02.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT10B			Receive input channel 10
	ASCLIN8_ARXA_F			Receive input
	EGTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	EGTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM3_7			Input mux of CDTM2_DTM3_AUXIN0/1
	ADC_TMADC4CH10	AI		Analog Input for TMADC4 Channel 10
	P02.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	ASCLIN8_ATX_F	O3		Transmit output
	CAN30_TXD	O4		CAN transmit output node 0
	CAN01_TXD	O5		CAN transmit output node 1
	SENT0_SPC10	O6		Transmit output
	ADC_EMUXCTRL03	O7		EMUX0 Control from TMADC to PORTS
	—	O8		Reserved
	EGTM_TOUT116_F	O9		eGTM muxed output

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH7_F	PO		High resolution PWM 0 output channels
F5	P02.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	SENT1_SENT10B			Receive input channel 10
	ASCLIN8_ARXB_F			Receive input
	EGTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM2_6			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	EGTM_CDTM2_DTM2_7			Input mux of CDTM2_DTM2_AUXIN0/1
	ADC_TMADC4CH11	AI		Analog Input for TMADC4 Channel 11
	P02.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT1_SPC10	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT117_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 9 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
F4	P02.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT11B			Receive input channel 11
	CAN30_RXDD			CAN receive input node 0
	SCU_E_REQ7G			ERU channel 7 input G
	EGTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	ADC_TMADC2CH15	AI		Analog Input for TMADC2 Channel 15
	P02.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN8_ASLSO	O3		Slave select signal output
	ASCLIN10_ATX	O4		Transmit output
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT118_F	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 10 Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A7	P10.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	SENT0_SENT13B			Receive input channel 13
	QSPI7_MRSTB			Master SPI data input
	EGTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	SENT1_SENT10C			Receive input channel 10
	CAN41_RXDE			CAN receive input node 1
	LETH0_P2_MII_RMII_RXD0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD0D			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	LETH0_P2_RXDF			LETH PortX TC14 interface receive data input
	P10.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10_F	O3		Master slave select output
	CAN30_TXD	O4		CAN transmit output node 0
	—	O5		Reserved
	—	O6		Reserved
	CANXL00_TXD	O7		CANXL transmit output node 0
	QSPI7_SLSO0	O8		Master slave select output
	EGTM_TOUT102	O9		eGTM muxed output
	ASCLIN0_ATX	O10		Transmit output
	—	O11		Reserved
	ERAY0_TXDA	O12		Transmit Channel A
	—	O13		Reserved
	CAN01_TXD	O14		CAN transmit output node 1
	ASCLIN0_ASCLK	O15		Shift clock output
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B7	P10.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA_F			Master SPI data input
	EGTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_2			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	LETH0_P2_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKB)
	ASCLIN0_ARXF			Receive input
	SENT0_SENT10C			Receive input channel 10
	P10.1	O0		General-purpose output
	—	O1		Reserved
	QSPI1_MTSR_F	O2		Master SPI data output
	QSPI1_MRST_F	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN0_ATX	O6		Transmit output
	CAN41_TXD	O7		CAN transmit output node 1
	QSPI7_SLSO1	O8		Master slave select output
	EGTM_TOUT103	O9		eGTM muxed output
	LETH0_P2_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	ASCLIN2_ARTS_F	O13		Ready to send output
	LETH0_P2_MIID_TXEN	O14		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A5	P10.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDE			CAN receive input node 2
	QSPI1_SCLKA_F			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2A			ERU channel 2 input A
	EGTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	LETH0_P2_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKB)
	P10.2	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI1_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	QSPI7_SLSO2	O8		Master slave select output
	EGTM_TOUT104	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO1	O12		Master slave select output
	LETH0_P2_MIID_TXD0	O13		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved
	LETH0_P2_RMIID_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD - registered*)

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A6	P10.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI1_MTSRA_F			Slave SPI data input
	SCU_E_REQ3A			ERU channel 3 input A
	GPT120_T5INB			Trigger/gate input of timer T5
	ASCLIN2_ARXH_F			Receive input
	EGTM_CDTM0_DTM3_2			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_5			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	EGTM_CDTM2_DTM3_3			Input mux of CDTM2_DTM3_AUXIN0/1
	LETH0_P2_MII_RXDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P10.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI1_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_SCLK	O8		Master SPI clock output
	EGTM_TOUT105	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO15	O12		Master slave select output
	ASCLIN1_ASLSO	O13		Slave select signal output
	ASCLIN3_ASLSO	O14		Slave select signal output
	—	O15		Reserved
B6	P10.4	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI1_MTSRC_F		VDDEXT / ES	Slave SPI data input
	GPT120_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	ASCLIN11_ARXB			Receive input
	CAN30_RXDA			CAN receive input node 0
	EGTM_CDTM2_DTM2_3			Input mux of CDTM2_DTM2_AUXIN0/1
	LETH0_P2_CRSB			LETH PortX MII carrier sense
	EGTM_CDTM2_DTM3_5			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	P10.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI1_SLSO8_F	O3		Master slave select output
	QSPI1_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT106	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	—	O11		Reserved
	LETH0_P2_MIID_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_MIID_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	ASCLIN3_ASLSO	O14		Slave select signal output
	LETH0_P2_RMIID_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD - registered*)
B5	P10.5	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	QSPI1_MRSTE_F			Master SPI data input
	CAN20_RXDA			CAN receive input node 0

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI5_MRSTE			Master SPI data input
	EGTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX_F	O2		Transmit output
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	—	O6		Reserved
	—	O7		Reserved
	QSPI1_MRST	O8		Slave SPI data output
	EGTM_TOUT107	O9		eGTM muxed output
	QSPI5_MRST	O10		Slave SPI data output
	—	O11		Reserved
	LETH0_P2_MIID_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	ERAY0_TXDB	O13		Transmit Channel B
	—	O14		Reserved
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)
A4	P10.6	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXD_F			Receive input
	QSPI3_MTSRB			Slave SPI data input
	ASCLIN7_ARXH			Receive input
	SENT1_SENT12B			Receive input channel 12
	EGTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	QSPI1_MRSTC_F			Master SPI data input
	EGTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK_F	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	CAN20_TXD	O5		CAN transmit output node 0
	QSPI1_MRST_F	O6		Slave SPI data output
	—	O7		Reserved
	SENT1_SPC12	O8		Transmit output
	EGTM_TOUT108	O9		eGTM muxed output
	QSPI5_MTSR	O10		Master SPI data output
	LETH0_P2_MIID_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	QSPI2_SLSO14	O12		Master slave select output
	CAN13_TXD	O13		CAN transmit output node 3
	ERAY0_TXENB	O14		Transmit Enable Channel B
	—	O15		Reserved
A3	P10.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA_F			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0B			ERU channel 0 input B
	CAN10_RXDH			CAN receive input node 0
	CAN13_RXDH			CAN receive input node 3
	ASCLIN9_ARXG			Receive input
	CANXL00_RXDE			CANXL receive input node 0
	QSPI1_MTSRD_F			Slave SPI data input
	QSPI7_MTSRD			Slave SPI data input
	EGTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_REFCLKB			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKB			LETH PortX MII receive clock
	LETH0_P2_REFCLKD			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKD			LETH PortX MII receive clock
	P10.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	ASCLIN9_ATX	O4		Transmit output
	CAN20_TXD	O5		CAN transmit output node 0
	CAN12_TXD	O6		CAN transmit output node 2
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI7_MRST	O8		Slave SPI data output
	EGTM_TOUT109	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN0_ARTS	O12		Ready to send output
	QSPI2_SLSO13	O13		Master slave select output
	—	O14		Reserved
	—	O15		Reserved
B4	P10.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1B			ERU channel 1 input B
	QSPI1_SLSIC_F			Slave select input
	CAN20_RXDB			CAN receive input node 0
	SENT1_SENT14A			Receive input channel 14
	CAN02_RXDG			CAN receive input node 2
	QSPI7_MRSTG			Master SPI data input
	EGTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1

(table continues...)

Table 10 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD1D			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	P10.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN5_ASLSO	O5		Slave select signal output
	ASCLIN7_ASLSO	O6		Slave select signal output
	—	O7		Reserved
	QSPI1_SLSO11	O8		Master slave select output
	EGTM_TOUT110	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 11 Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E10	P11.0	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	ASCLIN3_ARXB			Receive input
	EGTM_CDTM2_DTM4_2			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_2			Input mux of CDTM2_DTM5_AUXIN0/1
	XSPI0_RXD3C			Receive data
	EGTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	P11.0	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	LETH0_P0_MIIA_TXD3	O6		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT119	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDC3	O		Transmit data
E9	P11.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	XSPI0_RXD2C			Receive data
	EGTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	P11.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	LETH0_P0_MIIA_TXD2	O6		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT120	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 11 **(continued) Port 11 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDC2	O		Transmit data
A10	P11.2	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GPT121_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ASLSO	O2		Slave select signal output
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	LETH0_P0_MIIA_TXD1	O6		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD1	O7		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT95	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	CAN13_TXD	O15		CAN transmit output node 3
	LETH0_P0_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA - registered*)
B10	P11.3	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	CAN31_RXDD			CAN receive input node 1
	GPT121_T3EUDB			Count direction control input of core timer T3
	EGTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	P11.3	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_TXD	O2		LETH PortX TC14 interface transmit data output
	QSPI1_MRST	O3		Slave SPI data output
	ERAY0_TXDA	O4		Transmit Channel A
	CANXL00_TXD	O5		CANXL transmit output node 0
	LETH0_P0_MIIA_TXD0	O6		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD0	O7		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT96	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA - registered*)
D10	P11.4	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	EGTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	P11.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN13_TXD	O5		CAN transmit output node 3
	LETH0_P0_MIIA_TXER	O6		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT121	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CLKC	O15		Clock output
D8	P11.5	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	XSPI0_RXD1C			Receive data
	EGTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	LETH0_P0_TXCLKA			LETH PortX MII transmit clock
	P11.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT122	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDC1	O		Transmit data
D9	P11.6	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	GPT121_T4INB			Trigger/gate input of timer T4
	LETH0_P1_EDD			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOD			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	P11.6	O0		General-purpose output
	—	O1		Reserved
	ERAY0_TXENB	O2		Transmit Enable Channel B

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	LETH0_P0_MIIA_TXEN	O6		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXEN	O7		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT97	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	CAN00_TXD	O15		CAN transmit output node 0
	LETH0_P0_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E8	P11.7	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	CAN11_RXDD			CAN receive input node 1
	XSPI0_RXD0C			Receive data
	EGTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKA)
	P11.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT123	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDC0	O		Transmit data
E7	P11.8	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	CAN12_RXDD			CAN receive input node 2
	GPT121_T5INB			Trigger/gate input of timer T5
	EGTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKA)
	P11.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT124	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	$\overline{\text{XSPI0\_CSC1\_N}}$	O15		Chip select
A9	P11.9	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT121_T5EUDB			Count direction control input of timer T5
	CANXL00_RXDD			CANXL receive input node 0
	EGTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)
	LETH0_P0_RXDD			LETH PortX TC14 interface receive data input
	P11.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	GPT121_T3OUT	O6		External output for overflow/underflow detection of core timer T3
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT98	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B9	P11.10	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6B			ERU channel 6 input B
	QSPI1_SLSIA			Slave select input
	GPT121_T2INB			Trigger/gate input of timer T2
	CANXL01_RXDB			CANXL receive input node 1
	EGTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RMII_RXD0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)
	P11.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT99	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
A8	P11.11	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	LETH0_P1_MDIOA			LETH PortX MDIO interface data input
	GPT121_T2EUDB			Count direction control input of timer T2
	LETH0_P1_EDA			LETH PortX TC14 interface energy detection input
	EGTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	LETH0_P0_CRSA			LETH PortX MII carrier sense
	P11.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN12_TXD	O8		CAN transmit output node 2
	EGTM_TOUT100	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSC0_N	O15		Chip select
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B8	P11.12	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GPT121_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	LETH0_P0_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P0_RXCLKA			LETH PortX MII receive clock
	P11.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	CLOCK_EXTCLK1	O6		External clock output 1
	—	O7		Reserved
	EGTM_ECLK2	O8		CGM generated clock
	EGTM_TOUT101	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_TXD	O11		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O12		CANXL transmit output node 1
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E6	P11.13	I	SLOW / PU1 /	General-purpose input
	I2C1_SDAA			Serial Data Input 0

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN13_RXDD		VDDFLEX / ES	CAN receive input node 3
	CAN31_RXDA			CAN receive input node 1
	LETH0_P0_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKA)
	EGTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	P11.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT125	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D7	P11.14	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	I2C1_SCLA			Serial Clock Input 0
	CAN20_RXDF			CAN receive input node 0
	LETH0_P0_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P11.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 11 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT126	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D6	P11.15	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	LETH0_P0_COLA			LETH PortX MII collision detection
	EGTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	P11.15	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT127	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 12 Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E12	P12.0	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	CAN00_RXDC			CAN receive input node 0
	P12.0	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT128	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MDC	O11		LETH PortX MDIO interface clock output
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E11	P12.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	LETH0_P0_MDIOE			LETH PortX MDIO interface data input
	LETH0_P0_EDE			LETH PortX TC14 interface energy detection input
	P12.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT129	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 12 (continued) Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.2.7 BGA292_STD port 13

Table 13 Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose input
	ASCLIN10_ARXC_F			Receive input
	QSPI2_MRSTG_F			Master SPI data input
	GPT121_T6INB			Trigger/gate input of core timer T6
	CAN11_RXDG			CAN receive input node 1
	EGTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	P13.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ATX_F	O2		Transmit output
	QSPI2_SCLKN_F	O3		Master SPI clock output (LVDS N line)
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
	—	O8		Reserved
	EGTM_TOUT91	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved

(table continues...)

Table 13 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
A12	P13.1	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD_F			Receive input
	QSPI2_SCLKC_F			Slave SPI clock inputs
	LETH0_P2_COLC			LETH PortX MII collision detection
	EGTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	P13.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLKP_F	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	QSPI2_SCLK_F	O8		Master SPI clock output
	EGTM_TOUT92	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B11	P13.2	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	I2C0_SDAB			Serial Data Input 1
	CAN33_RXDA			CAN receive input node 3
	GPT121_T6EUDB			Count direction control input of core timer T6
	LETH0_P2_CRSC			LETH PortX MII carrier sense

(table continues...)

Table 13 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	P13.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASCLK_F	O2		Shift clock output
	QSPI2_MTSRN_F	O3		Master SPI data output (LVDS N line)
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	QSPI2_MTSR_F	O8		Master SPI data output
	EGTM_TOUT93	O9		eGTM muxed output
	QSPI2_MRST_F	O10		Slave SPI data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A11	P13.3	I	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI2_SLSIC_F			Slave select input
	EGTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASLSO_F	O2		Slave select signal output
	QSPI2_MTSRP_F	O3		Master SPI data output (LVDS P line)
	ASCLIN7_ASLSO_F	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	CAN33_TXD	O7		CAN transmit output node 3
	QSPI2_SLSO3_F	O8		Master slave select output
	EGTM_TOUT94	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 13 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIIA_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 14 Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B16	P14.0	I	FAST / PU1 / VDDEXTH S / ES2	General-purpose input
	SENT1_SENT8D			Receive input channel 8
	CAN41_RXDB			CAN receive input node 1
	LETH0_P2_EDH			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOH			LETH PortX MDIO interface data input
	EGTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	LETH0_P2_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKA			LETH PortX MII receive clock
	LETH0_P2_REFCLKC			LETH PortX RMII reference clock
	LETH0_P2_RXCLKC			LETH PortX MII receive clock
	P14.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT80	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P1_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O15		CANXL transmit output node 1
	EGTM_HRPWM1_CH0	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A15	P14.1	I	FAST / PU1 / VDDEXTHS / ES2	General-purpose input
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA_F			Receive input
	SENT0_SENT9D			Receive input channel 9
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3B			ERU channel 3 input B
	CANXL00_RXDB			CANXL receive input node 0
	EGTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	PMS_PINAWKP			PINA (P14.1) pin input
	LETH0_P2_MII_RMII_RXD0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	LETH0_P0_RXDB			LETH PortX TC14 interface receive data input
	P14.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	CAN41_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT81	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH1	PO		High resolution PWM 1 output channels
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E13	P14.2	I	SLOW / PU2 / VDDEXTHS / ES	General-purpose input
	CANXL01_RXDD			CANXL receive input node 1
	LETH0_P2_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKA)
	LETH0_P2_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	PMS_HWCFG2IN			HWCFG2 pin input
	LETH0_P1_RXDD			LETH PortX TC14 interface receive data input
	P14.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	ASCLIN0_ASLSO	O5		Slave select signal output
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT82	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P0_PPS	O13		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O14		Reserved

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B14	P14.3	I	SLOW / PU2 / VDDEXTHS / ES	General-purpose input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1A			ERU channel 1 input A
	LETH0_P1_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	PMS_HWCFG3IN			HWCFG3 pin input
	LETH0_P2_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT83	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B15	P14.4	I	SLOW / PU2 / VDDEXTHS / ES	General-purpose input
	CANXL01_RXDA			CANXL receive input node 1
	EGTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_1			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_1			Input mux of CDTM0_DTM3_AUXIN0/1
	LETH0_P1_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	PMS_HWCFG6IN			HWCFG6 pin input
	LETH0_P1_RXDA			LETH PortX TC14 interface receive data input
	P14.4	O0		General-purpose output
	—	O1		Reserved
	GPT123_T3OUT	O2		External output for overflow/underflow detection of core timer T3
	ASCLIN0_ARTS	O3		Ready to send output
	QSPI2_SLSO4	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT84	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A14	P14.5	I	FAST / PU2 /	General-purpose input

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI5_MRSTB		VDDEXTHS / ES	Master SPI data input
	EGTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P2_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	QSPI2_SLSO4_F	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT85	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_TXD	O11		LETH PortX TC14 interface transmit data output
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH2	PO		High resolution PWM 1 output channels
B13	P14.6	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI5_MTSRB			Slave SPI data input
	LETH0_P2_EDC			LETH PortX TC14 interface energy detection input
	GPT123_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	LETH0_P2_MDIOC			LETH PortX MDIO interface data input
	LETH0_P2_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	P14.6	O0		General-purpose output
	—	O1		Reserved
	QSPI5_MTSR	O2		Master SPI data output
	QSPI2_SLSO2_F	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	ASCLIN0_ASLSO_F	O5		Slave select signal output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	ASCLIN0_ATX_F	O8		Transmit output
	EGTM_TOUT86	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH3	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D13	P14.7	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	QSPI7_MTSRA			Slave SPI data input
	EGTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	LETH0_P2_RXDC			LETH PortX TC14 interface receive data input
	P14.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ARTS_F	O2		Ready to send output
	QSPI2_SLSO4_F	O3		Master slave select output

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT87	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A13	P14.8	I	SLOW / PU1 / VDDEXTHS / ES	General-purpose input
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	GPT123_T3EUDB			Count direction control input of core timer T3
	CANXL00_RXDA			CANXL receive input node 0
	QSPI7_MRSTA			Master SPI data input
	EGTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	LETH0_P0_RXDA			LETH PortX TC14 interface receive data input
	LETH0_P2_TXCLKA			LETH PortX MII transmit clock
	LETH0_P2_TXCLKC			LETH PortX MII transmit clock
	P14.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO_F	O3		Slave select signal output

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN0_ASLSO_F	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT88	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D12	P14.9	I	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose input
	ASCLIN0_ACTSA_F			Clear to send input
	QSPI2_MRSTFN_F			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	LETH0_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOA			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	P14.9	O0		General-purpose output
	—	O1		Reserved
	CAN23_TXD	O2		CAN transmit output node 3
	—	O3		Reserved
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT89	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIIA_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D11	P14.10	I	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN23_RXDA			CAN receive input node 3
	QSPI2_MRSTFP_F			Master SPI data input (LVDS P line)
	GPT123_T4INB			Trigger/gate input of timer T4
	EGTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	P14.10	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	—	O3		Reserved
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved
	LETH0_P2_RMIIA_TXD0	O8		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA)
	EGTM_TOUT90	O9		eGTM muxed output
	LETH0_P2_MIIA_TXD0	O10		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKC)
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output

(table continues...)

Table 14 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA - registered*)

3.2.9 BGA292_STD port 15

Table 15 Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B20	P15.0	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	SDMMC0_DAT7_IN			Read data in (new on AB step)
	GPT123_T2INB			Trigger/gate input of timer T2
	EGTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT71	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH4	PO		High resolution PWM 1 output channels
	SDMMC0_DAT7	O		Write data out (new on AB step)
A18	P15.1	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA_F			Receive input

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7B			ERU channel 7 input B
	GPT123_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	LETH0_P0_RXDE			LETH PortX TC14 interface receive data input
	P15.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	SDMMC0_CLK	O7		Card clock (new on AB step)
	—	O8		Reserved
	EGTM_TOUT72	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH5	PO		High resolution PWM 1 output channels
C19	P15.2	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	SENT0_SENT5D			Receive input channel 5
	QSPI2_MRSTE			Master SPI data input
	GPT123_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	XSPI0_RXD3B			Receive data
	P15.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SLSO0	O3		Master slave select output

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ATX_F	O4		Transmit output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK	O6		Shift clock output
	QSPI7_SCLK_F	O7		Master SPI clock output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT73	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB3	O		Transmit data
B17	P15.3	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	SDMMC0_CMD_IN			Command in (new on AB step)
	GPT123_T5EUDB			Count direction control input of timer T5
	ASCLIN1_ACTSC_F			Clear to send input
	QSPI7_SCLKC_F			Slave SPI clock inputs
	EGTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	LETH0_P2_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT74	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH6	PO		High resolution PWM 1 output channels
	SDMMC0_CMD	O		Command out (new on AB step)
A17	P15.4	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0A			ERU channel 0 input A
	SENT1_SENT5D			Receive input channel 5
	CAN42_RXDB			CAN receive input node 2
	GPT123_T5INB			Trigger/gate input of timer T5
	QSPI7_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	P15.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	QSPI7_MTSR_F	O7		Master SPI data output
	QSPI7_MRST_F	O8		Slave SPI data output
	EGTM_TOUT75	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E14	P15.5	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	ASCLIN1_ARXB_F			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4D			ERU channel 4 input D
	QSPI7_MTSRE_F			Slave SPI data input
	GPT123_T6INB			Trigger/gate input of core timer T6
	EGTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	P15.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	CAN42_TXD	O4		CAN transmit output node 2
	—	O5		Reserved
	I2C0_SDA	O6		Serial Data Output
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT76	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH7	PO		High resolution PWM 1 output channels
A16	P15.6	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	QSPI2_MTSRB			Slave SPI data input
	ASCLIN19_ARXA_F			Receive input
	LETH0_P1_MDIOG			LETH PortX MDIO interface data input
	GPT123_T6EUDB			Count direction control input of core timer T6

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_EDG			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	P15.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	QSPI5_SLSO3	O4		Master slave select output
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_MTSR_F	O7		Master SPI data output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT77	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D15	P15.7	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	ASCLIN19_ARXB_F			Receive input
	CAN43_RXDB			CAN receive input node 3
	GPT123_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI7_MRSTE_F			Master SPI data input
	EGTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	LETH0_P1_RXDB			LETH PortX TC14 interface receive data input

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P15.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	ASCLIN1_ARTS_F	O5		Ready to send output
	—	O6		Reserved
	QSPI7_SLSO10_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT78	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D14	P15.8	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5A			ERU channel 5 input A
	EGTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	P15.8	O0		General-purpose output
	—	O1		Reserved
	CAN43_TXD	O2		CAN transmit output node 3
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_SLSO11_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT79	O9		eGTM muxed output

(table continues...)

Table 15 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_T6OUT	O10		External output for overflow/underflow detection of core timer T6
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.10 BGA292_STD port 20

Table 16 Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H20	P20.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN03_RXDC			CAN receive input node 3
	CAN21_RXDC			CAN receive input node 1
	CBS_TGI0			Trigger input
	SCU_E_REQ6A			ERU channel 6 input A
	GPT120_T6EUDA			Count direction control input of core timer T6
	SENT1_SENT1D			Receive input channel 1
	GPT122_T2INB			Trigger/gate input of timer T2
	LETH0_P0_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	EGTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CLOCK_CLKA_SYSCLK			System clock input
	P20.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	ASCLIN3_ASCLK_F	O3		Shift clock output
	SENT1_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT59	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_MDC	O12		LETH PortX MDIO interface clock output
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB1_N	O15		Chip select
	HSCT0_SYSCLK_OUT	PO		sys clock output
	CBS_TGO0	O		Trigger output
G19	P20.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CBS_TGI1			Trigger input
	CAN40_RXDB			CAN receive input node 0
	EGTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	LETH0_P0_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	P20.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO_F	O2		Slave select signal output
	CAN32_TXD	O3		CAN transmit output node 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT60	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_RMIIB_TXD0	O13		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO1	O		Trigger output
H19	P20.2	I	S / PU / VDDEXT	General-purpose input
	$\overline{\text{TESTMODE}}$			Testmode Enable Input
	PMS_TESTMODEIN			TESTMODE pin input
G20	P20.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXC_F			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	SENT0_SENT3D			Receive input channel 3
	GPT122_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	XSPI0_RXD0B			Receive data
	LETH0_P0_TXCLKB			LETH PortX MII transmit clock
	P20.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	QSPI0_SLSO9_F	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved
	SENT0_SPC3	O8		Transmit output
	EGTM_TOUT61	O9		eGTM muxed output
	LETH0_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB0	O		Transmit data

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
F17	P20.6	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	SENT1_SENT3D			Receive input channel 3
	CAN32_RXDB			CAN receive input node 2
	GPT122_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	XSPI0_RXD1B			Receive data
	P20.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8_F	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	ASCLIN3_ASLSO_F	O5		Slave select signal output
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT62	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB1	O		Transmit data
F19	P20.7	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	SDMMC0_DAT0_IN			Read data in (new on AB step)
	SENT1_SENT0D			Receive input channel 0

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	EGTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	P20.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN9_ATX	O2		Transmit output
	ASCLIN3_ARTS_F	O3		Ready to send output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT63	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH7	PO		High resolution PWM 2 output channels
	SDMMC0_DAT0	O		Write data out (new on AB step)
F20	P20.8	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	SDMMC0_DAT1_IN			Read data in (new on AB step)
	LETH0_P0_CRSD			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	LETH0_P0_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P20.8	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0_F	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT64	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH0	PO		High resolution PWM 2 output channels
	SDMMC0_DAT1	O		Write data out (new on AB step)
E17	P20.9	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB_F			Slave select input
	SCU_E_REQ7A			ERU channel 7 input A
	ADC_TRIG62			Triggers from PORTS to ADC
	LETH0_P0_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	XSPI0_RXD2B			Receive data
	P20.9	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI0_SLSO1_F	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT65	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH1	PO		High resolution PWM 2 output channels
	XSPI0_TXDB2	O		Transmit data
E19	P20.10	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	SDMMC0_DAT2_IN			Read data in (new on AB step)
	EGTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI0_SLSO6_F	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT66	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH0_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH2	PO		High resolution PWM 2 output channels

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SDMMC0_DAT2	O		Write data out (new on AB step)
E20	P20.11	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI0_SCLKA_F			Slave SPI clock inputs
	SDMMC0_DAT3_IN			Read data in (new on AB step)
	ASCLIN18_ARXD			Receive input
	ASCLIN3_ACTSB_F			Clear to send input
	EGTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	P20.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT67	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH3	PO		High resolution PWM 2 output channels
	SDMMC0_DAT3	O		Write data out (new on AB step)
D19	P20.12	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI0_MRSTA_F			Master SPI data input
	SDMMC0_DAT4_IN			Read data in (new on AB step)
	EGTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	LETH0_P0_MII_RMII_RXD0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P20.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MRST_F	O3		Slave SPI data output
	QSPI0_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_MDC	O7		LETH PortX MDIO interface clock output
	—	O8		Reserved
	EGTM_TOUT68	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH4	PO		High resolution PWM 2 output channels
	SDMMC0_DAT4	O		Write data out (new on AB step)
D20	P20.13	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI0_SLSIA_F			Slave select input
	SDMMC0_DAT5_IN			Read data in (new on AB step)
	ASCLIN9_ARXH			Receive input
	ASCLIN18_ARXE			Receive input
	LETH0_P0_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	P20.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SLSO2_F	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK_F	O5		Master SPI clock output
	—	O6		Reserved

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT69	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CLKB	O15		Clock output
	EGTM_HRPWM2_CH5	PO		High resolution PWM 2 output channels
	SDMMC0_DAT5	O		Write data out (new on AB step)
C20	P20.14	I	FAST / PU1 / VDDEXTHS / ES	General-purpose input
	QSPI0_MTSRA_F			Slave SPI data input
	SDMMC0_DAT6_IN			Read data in (new on AB step)
	QSPI4_MRSTH			Master SPI data input
	LETH0_P0_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	P20.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT70	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 16 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	XSPI0_CSB0_N	O15		Chip select
	EGTM_HRPWM2_CH6	PO		High resolution PWM 2 output channels
	SDMMC0_DAT6	O		Write data out (new on AB step)

3.2.11 BGA292_STD port 21

Table 17 Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDN_F			Master SPI data input (LVDS N line)
	ASCLIN11_ARXC_F			Receive input
	HSCT1_RXDN			Rx data
	QSPI0_SCLKEN			Slave SPI clock inputs (LVDS N line)
	QSPI4_MRSTE			Master SPI data input
	ASCLIN17_ARXB			Receive input
	ASCLIN18_ARXF			Receive input
	GPT123_T6EUDA			Count direction control input of core timer T6
	EGTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI0_SCLKD			Slave SPI clock inputs
	P21.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX_F	O2		Transmit output
	GPT123_T6OUT	O3		External output for overflow/underflow detection of core timer T6
	—	O4		Reserved
	—	O5		Reserved
	QSPI0_SLSO8_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT51	O9		eGTM muxed output
	LETH0_P0_MIIB_TXD1	O10		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	CSCU_CSRM1	O		Pin Output Value
J17	P21.1	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDP_F			Master SPI data input (LVDS P line)
	ASCLIN11_ARXD_F			Receive input
	HSCT1_RXDP			Rx data
	QSPI0_SCLKEP			Slave SPI clock inputs (LVDS P line)
	ASCLIN18_ARXA_F			Receive input
	EGTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI0_SCLKF			Slave SPI clock inputs
	P21.1	O0		General-purpose output
	—	O1		Reserved
	CAN40_TXD	O2		CAN transmit output node 0
	GPT122_T3OUT	O3		External output for overflow/underflow detection of core timer T3
	—	O4		Reserved
	—	O5		Reserved
	QSPI0_SCLK_F	O6		Master SPI clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT52	O9		eGTM muxed output
	LETH0_P0_MIIB_TXER	O10		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CSCU_CSRM2	O		Pin Output Value
K19	P21.2	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SMU_EXT_EMERGENCYSTOP_REQ			Emergency Stop External Request B
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN_F			Master SPI data input (LVDS N line)
	ASCLIN11_ARXE_F			Receive input
	QSPI0_MTSRDN			Slave SPI data input (LVDS N line)
	SENT0_SENT2D			Receive input channel 2
	GPT123_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	QSPI0_MTSRE			Slave SPI data input
	QSPI4_MTSRC			Slave SPI data input
	ASCLIN18_ARXG			Receive input
	LETH0_P0_MDIOH			LETH PortX MDIO interface data input
	LETH0_P0_EDH			LETH PortX TC14 interface energy detection input
	P21.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_MTSR_F	O6		Master SPI data output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT53	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
J19	P21.3	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP_F			Master SPI data input (LVDS P line)
	QSPI0_MTSRDP			Slave SPI data input (LVDS P line)
	SENT1_SENT2D			Receive input channel 2
	GPT123_T3EUDA			Count direction control input of core timer T3
	EGTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	QSPI0_MTSRF			Slave SPI data input
	P21.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASCLK_F	O2		Shift clock output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT1_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_SLSO9_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT54	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	SENT0_SENT0D			Receive input channel 0
	ASCLIN18_ARXB_F			Receive input
	GPT123_T4INA			Trigger/gate input of timer T4
	EGTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	LETH0_P0_REFCLKB			LETH PortX RMII reference clock
	LETH0_P0_RXCLKB			LETH PortX MII receive clock
	P21.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASLSO_F	O2		Slave select signal output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT0_SPC0	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTN	O8		Slave SPI inverted data output
	EGTM_TOUT55	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDN	PO		Tx data
J20	P21.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	ASCLIN11_ARXF_F			Receive input
	SENT0_SENT1D			Receive input channel 1
	ASCLIN18_ARXC_F			Receive input
	QSPI0_MRSTE_F			Master SPI data input
	GPT123_T6INA			Trigger/gate input of core timer T6
	EGTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P21.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX_F	O3		Transmit output
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTP	O8		Slave SPI data output
	EGTM_TOUT56	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDP	PO		Tx data
H17	P21.6	I	FAST / PD3 / VDDEXT / ES	General-purpose input
	CAN33_RXDB			CAN receive input node 3
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF_F			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	QSPI0_SLSIC			Slave select input
	LETH0_P0_COLC			LETH PortX MII collision detection
	EGTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	P21.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved

(table continues...)

Table 17 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT57	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP3	I/PO		DAP:DAP3 Data I/O
	DAPE1	I/PO		DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
	CBS_TGO2	O		Trigger output
H16	P21.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	LETH0_P0_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKC)
	EGTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	P21.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	ASCLIN3_ASCLK	O3		Shift clock output
	CAN33_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved

(table continues...)

Table 17 **(continued) Port 21 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT58	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP2	I/PO		DAP:DAP2 Data I/O
	DAPE2	I/PO		DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
	TDO	PO		PU/TRIST controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) during reset (PORST=0). The default state after PORST release in DAP mode is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) . The default state after PORST release in JTAG mode is HighZ. In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4)
	CBS_TGO3	O		Trigger output

3.2.12 BGA292_STD port 22

Table 18 **Port 22 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
P20	P22.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MTSRB_F			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	QSPI5_MRSTC			Master SPI data input
	GPT123_T2INA			Trigger/gate input of timer T2
	EGTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	LETH0_P1_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.0	O0		General-purpose output

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR_F	O3		Master SPI data output
	QSPI4_SCLKN_F	O4		Master SPI clock output (LVDS N line)
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT47	O9		eGTM muxed output
	ASCLIN4_ASCLK_F	O10		Shift clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P19	P22.1	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MRSTB_F			Master SPI data input
	ASCLIN7_ARXE			Receive input
	GPT123_T2EUDA			Count direction control input of timer T2
	EGTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	LETH0_P1_REFCLKB			LETH PortX RMII reference clock
	LETH0_P1_RXCLKB			LETH PortX MII receive clock
	P22.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST_F	O3		Slave SPI data output
	QSPI4_SCLKP_F	O4		Master SPI clock output (LVDS P line)
	—	O5		Reserved
	QSPI5_SLSO9	O6		Master slave select output
	ASCLIN7_ATX	O7		Transmit output
	QSPI4_SLSO9	O8		Master slave select output
	EGTM_TOUT48	O9		eGTM muxed output

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN4_ATX_F	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R20	P22.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SLSIB_F			Slave select input
	CAN41_RXDA			CAN receive input node 1
	ASCLIN4_ARXH_F			Receive input
	GPT123_T4EUDA			Count direction control input of timer T4
	LETH0_P1_COLA			LETH PortX MII collision detection
	LETH0_P1_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	P22.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3_F	O3		Master slave select output
	QSPI4_MTSRN_F	O4		Master SPI data output (LVDS N line)
	—	O5		Reserved
	QSPI5_MTSR	O6		Master SPI data output
	QSPI4_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT49	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIA_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXEN	O13		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXEN	O14		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKA)

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIB_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB)
	HSCT1_TXDN	PO		Tx data
R19	P22.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SCLKB_F			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	GPT123_T5INA			Trigger/gate input of timer T5
	LETH0_P1_MII_RMII_RXD0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	LETH0_P1_REFCLKC			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKC			LETH PortX MII receive clock
	P22.3	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	QSPI4_SCLK_F	O3		Master SPI clock output
	QSPI4_MTSRP_F	O4		Master SPI data output (LVDS P line)
	—	O5		Reserved
	CAN41_TXD	O6		CAN transmit output node 1
	ASCLIN7_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT50	O9		eGTM muxed output
	ASCLIN4_ASLSO_F	O10		Slave select signal output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT1_TXDP	PO		Tx data
P16	P22.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SCU_E_REQ5E			ERU channel 5 input E
	ASCLIN7_ARXF			Receive input

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_T5EUDA			Count direction control input of timer T5
	LETH0_P1_MII_RMII_RXD0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	LETH0_P1_MII_RMII_RXD0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	LETH0_P1_RXDH			LETH PortX TC14 interface receive data input
	P22.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK_F	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved
	CAN13_TXD	O6		CAN transmit output node 3
	QSPI6_SLSO15_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT130	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
P17	P22.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRC			Slave SPI data input
	CAN42_RXDA			CAN receive input node 2
	CAN13_RXDC			CAN receive input node 3
	GPT122_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	LETH0_P1_REFCLKA			LETH PortX RMII reference clock
	LETH0_P1_RXCLKA			LETH PortX MII receive clock
	P22.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX_F	O2		Transmit output

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT131	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N16	P22.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC_F			Receive input
	LETH0_P1_AUX			LETH PortX auxilary snapshot signal (new on AB step)
	GPT122_T3EUDB			Count direction control input of core timer T3
	LETH0_P1_CRSA			LETH PortX MII carrier sense
	LETH0_P1_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	LETH0_P1_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT132	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N17	P22.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	GPT122_T4INB			Trigger/gate input of timer T4
	LETH0_P1_TXCLKA			LETH PortX MII transmit clock
	LETH0_P1_TXCLKB			LETH PortX MII transmit clock
	LETH0_P1_TXCLKC			LETH PortX MII transmit clock
	P22.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN17_ATX	O3		Transmit output
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT133	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
M16	P22.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKB			Slave SPI clock inputs
	LETH0_P2_AUX			LETH PortX auxilary snapshot signal (new on AB step)
	GPT122_T5INB			Trigger/gate input of timer T5
	LETH0_P1_COLC			LETH PortX MII collision detection
	LETH0_P1_RXDE			LETH PortX TC14 interface receive data input
	P22.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT134	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
M17	P22.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD_F			Receive input
	CAN22_RXDE			CAN receive input node 2
	LETH0_P1_EDE			LETH PortX TC14 interface energy detection input
	GPT122_T5EUDB			Count direction control input of timer T5
	LETH0_P1_MDIOE			LETH PortX MDIO interface data input
	P22.9	O0		General-purpose output

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	GPT122_T6OUT	O2		External output for overflow/underflow detection of core timer T6
	ASCLIN17_ATX_F	O3		Transmit output
	QSPI0_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT135	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
L16	P22.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRB			Slave SPI data input
	GPT122_T6INB			Trigger/gate input of core timer T6
	P22.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT136	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
	LETH0_P1_RMIIRC_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC - registered*)
L17	P22.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDE			CAN receive input node 3
	ASCLIN17_ARXA_F			Receive input
	GPT122_T6EUDB			Count direction control input of core timer T6
	LETH0_P1_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKA)
	LETH0_P1_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKB)
	P22.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	ASCLIN17_ATX_F	O3		Transmit output
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	CAN42_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT137	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved

(table continues...)

Table 18 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC - registered*)

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Table 19 Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
V20	P23.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN10_RXDC			CAN receive input node 0
	ASCLIN17_ARXC			Receive input
	QSPI6_SLSID_F			Slave select input
	EGTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	P23.0	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT41	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIA_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXER	O12		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXER	O13		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U19	P23.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXF_F			Receive input
	GPT123_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	SCU_E_REQ6F			ERU channel 6 input F
	ADC_TRIG61			Triggers from PORTS to ADC
	QSPI0_MRSTD			Master SPI data input
	LETH0_P1_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	LETH0_P1_RXDG			LETH PortX TC14 interface receive data input
	P23.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6_F	O3		Master slave select output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	CLOCK_EXTCLK0	O6		External clock output 0
	ASCLIN6_ASCLK_F	O7		Shift clock output
	QSPI6_MTSR_F	O8		Master SPI data output
	EGTM_TOUT42	O9		eGTM muxed output
	EGTM_ECLK0	O10		CGM generated clock
	ASCLIN16_ATX_F	O11		Transmit output
	QSPI6_SCLK_F	O12		Master SPI clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
U20	P23.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN7_ARXC			Receive input
	QSPI6_MRSTE_F			Master SPI data input
	EGTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	P23.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN6_ASCLK_F	O3		Shift clock output
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	CAN10_TXD	O6		CAN transmit output node 0
	QSPI6_SCLK_F	O7		Master SPI clock output
	QSPI6_SLSO3_F	O8		Master slave select output
	EGTM_TOUT43	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIA_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
T19	P23.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXA_F			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	GPT122_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI6_MTSRB_F			Slave SPI data input
	EGTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	P23.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI6_SLSO0	O7		Master slave select output
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT44	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIA_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD2	O13		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
T20	P23.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI6_MRSTD_F			Master SPI data input
	EGTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	P23.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASLSO_F	O2		Slave select signal output
	QSPI4_SLSO5_F	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO1_F	O8		Master slave select output
	EGTM_TOUT45	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIA_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKB)

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIA_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXD1	O14		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB)
	QSPI6_MTSR_F	O15		Master SPI data output
T17	P23.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN16_ARXA_F			Receive input
	LETH0_P1_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	P23.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX_F	O2		Transmit output
	QSPI4_SLSO4_F	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	QSPI6_SLSO2_F	O8		Master slave select output
	EGTM_TOUT46	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIA_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXD0	O13		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXD0	O14		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
R17	P23.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN22_RXDC			CAN receive input node 2
	QSPI6_MRSTA_F			Master SPI data input

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKA)
	LETH0_P1_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKB)
	LETH0_P1_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	P23.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX_F	O2		Transmit output
	ASCLIN6_ASLSO_F	O3		Slave select signal output
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_SLSO14_F	O7		Master slave select output
	QSPI6_MRST_F	O8		Slave SPI data output
	EGTM_TOUT138	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
R16	P23.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN11_RXDC			CAN receive input node 1
	ASCLIN16_ARXB_F			Receive input
	QSPI6_SCLKA_F			Slave SPI clock inputs
	LETH0_P1_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	LETH0_P1_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	EGTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	P23.7	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 19 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN16_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT139	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 20 Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W18	P32.2	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	CAN21_RXDD			CAN receive input node 1
	SMU_FSPIN2			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	UART_RXDH	I#		Receive input H
	WCAN_RXDF			Wake-up input F
	T0D			T0 capture input D
	T21EXG			T21 interrupt input G
	EXINT7			Interrupt 7 input
	P32.2	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	ASCLIN15_ATX_F	O4		Transmit output
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT38	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP2	O		FSP Output Signal - Generated by SMU
W17	P32.4	I	FAST / PU1 /	General-purpose input
	ASCLIN1_ACTSB			Clear to send input

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN15_ARXA_F		VDDEVRS B / ES	Receive input
	I2C0_SCLD			Serial Clock Input 3
	EGTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	SSC_MRSTD	I#		Master SPI data input D
	T21EXA			T21 interrupt input A
	T2CCU1_0A			T2 capture 1 input 0A
	EXINT8A			Interrupt 8 input A
	EXINT12A			Interrupt 12 input A
	I2CSCLA			Serial clock input A
	P32.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	—	O5		Reserved
	CLOCK_EXTCLK1	O6		External clock output 1
	CAN21_TXD	O7		CAN transmit output node 1
	I2C0_SCL	O8		Serial Clock Output
	EGTM_TOUT40	O9		eGTM muxed output
	EGTM_ECLK1	O10		CGM generated clock
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.1	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_0	O#6		T2 PWM channel 10

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DCDCSYNCO	O		DC-DC synchronization output
T15	P32.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	SENT0_SENT5C			Receive input channel 5
	ASCLIN17_ARXF			Receive input
	SMU_FSPIN3			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	SSC_MTSRD	I#		Slave SPI data input D
	PINRSTC			Reset input C
	T20EXO			T20 interrupt input O
	T2CCU1_1A			T2 capture 1 input 1A
	EXINT9A			Interrupt 9 input A
	EXINT13A			Interrupt 13 input A
	P32.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	SENT0_SPC5	O3		Transmit output
	ASCLIN5_ASLSO_F	O4		Slave select signal output
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT140	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP3	O		FSP Output Signal - Generated by SMU
U15	P32.6	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT1_SENT5C			Receive input channel 5
	I2C0_SDAD			Serial Data Input 3
	UART_RXDI	I#		Receive input I
	T1D			T1 capture input D
	T21A			T21 capture input A
	T2CCU1_2A			T2 capture 1 input 2A

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT10A			Interrupt 10 input A
	EXINT14A			Interrupt 14 input A
	I2CSDAA			Serial data input A
	P32.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	SENT1_SPC5	O3		Transmit output
	ASCLIN17_ATX	O4		Transmit output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	I2C0_SDA	O8		Serial Data Output
	EGTM_TOUT141	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_PPS	O12		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO4	O		Trigger output
U16	P32.7	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	CBS_TGI5			Trigger input
	CAN22_RXDB			CAN receive input node 2
	SENT0_SENT6C			Receive input channel 6
	ASCLIN15_ARXB_F			Receive input
	ADC_SIGN0			Sign for Carrier Cancellation
	LETH0_P1_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKB)
	WCAN_RXDH	I#		Wake-up input H
	T20EXH			T20 interrupt input H
	T2CCU1_3A			T2 capture 1 input 3A
	EXINT11A			Interrupt 11 input A
	EXINT15A			Interrupt 15 input A
	P32.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	SENT0_SPC6	O3		Transmit output
	ASCLIN15_ATX	O4		Transmit output
	ASCLIN17_ATX	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT142	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 20 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P2.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_3	O#6		T2 PWM channel 13
	PMSRTC32_OUT	O#7		RTC oscillator output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO5	O		Trigger output

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Table 21 Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W10	P33.0	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	SENT1_SENT9B			Receive input channel 9
	QSPI5_MRSTG			Master SPI data input
	GPT122_T6INA			Trigger/gate input of core timer T6
	EGTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_3			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_3			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	T21EXB	I#		T20 interrupt input B

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_0A			T2 capture 0 input 0A
	EXINT3A			Interrupt 3 input A
	EXINT12B			Interrupt 12 input B
	ADCOMPCH0			Analog input channel 0
	P33.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	SENT1_SPC9	O3		Transmit output
	ASCLIN15_ATX	O4		Transmit output
	ADC_EMUXCTRL03	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	QSPI5_MRST	O8		Slave SPI data output
	EGTM_TOUT22	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y10	P33.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX0C			RXD inputs (receive data) channel 0
	SENT0_SENT9B			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	GPT122_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	EGTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	UART_RXDK	I#		Receive input K
	SSC_SCLKD			Slave SPI clock input D
	T0A			T0 capture input A
	T20EXA			T2 interrupt input A
	T2CCU0_1A			T2 capture 0 input 1A
	EXINT4A			Interrupt 4 input A
	EXINT13B			Interrupt 13 input B
	ADCOMPCH1			Analog input channel 1
	P33.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	SENT0_SPC9	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT23	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.1	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W11	P33.2	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT8B			Receive input channel 8
	GPT120_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	ASCLIN14_ARXC_F			Receive input
	EGTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	WCAN_RXDE	I#		Wake-up input E
	SCRDAP0_1			SCRDAP0 input
	T21B			T21 capture input B
	T2CCU0_2A			T2 capture 0 input 2A
	EXINT5A			Interrupt 5 input A
	EXINT14B			Interrupt 14 input B
	ADCOMPCH2			Analog input channel 2
	P33.2	O0		General-purpose output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN14_ATX	O7		Transmit output
	SENT1_SPC8	O8		Transmit output
	EGTM_TOUT24	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	GPT122_T3OUT	O12		External output for overflow/underflow detection of core timer T3
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y11	P33.3	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT0_SENT8B			Receive input channel 8
	ASCLIN14_ARXA_F			Receive input
	EGTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	UART_RXDP	I#		Receive input P
	T20A			T20 capture input A
	T2CCU0_3A			T2 capture 0 input 3A
	EXINT6A			Interrupt 6 input A
	EXINT15B			Interrupt 15 input B
	ADCOMPCH3			Analog input channel 3
	P33.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN14_ATX	O7		Transmit output
	SENT0_SPC8	O8		Transmit output
	EGTM_TOUT25	O9		eGTM muxed output
	ASCLIN8_ATX	O10		Transmit output
	—	O11		Reserved
	GPT122_T6OUT	O12		External output for overflow/underflow detection of core timer T6
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_1	I/O		SCRDAP1 input
	SPD_1	I/O		Single pin SCRDAP1
W12	P33.4	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT7B			Receive input channel 7
	ASCLIN5_ARXB_F			Receive input
	ASCLIN14_ARXB_F			Receive input
	EGTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_1			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_1			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	UART_RXDC	I#		Receive input C
	WCAN_RXDP			Wake-up input P
	T1B			T1 capture input B
	T2CCU0_3D			T2 capture 0 input 3D
	EXINT0A			Interrupt 0 input A
	EXINT6D			Interrupt 6 input D
	EXINT12C			Interrupt 12 input C
	ADCOMPCH4			Analog input channel 4
	P33.4	O0		General-purpose output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	CAN13_TXD	O7		CAN transmit output node 3
	SENT1_SPC7	O8		Transmit output
	EGTM_TOUT26	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.4	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y12	P33.5	I	SLOW / PU1 /	General-purpose input
	GPT120_T4EUDB			Count direction control input of timer T4

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PSI5S0_RXC		VDDEVRS B / ES5	RX data input
	ASCLIN2_ACTSB			Clear to send input
	SENT1_SENT2C			Receive input channel 2
	CAN13_RXDB			CAN receive input node 3
	QSPI4_MRSTG			Master SPI data input
	EGTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	WCAN_RXDD	I#		Wake-up input D
	SSC_MRSTA			Master SPI data input A
	T0B			T0 capture input B
	T20EXB			T20 interrupt input B
	EXINT1A			Interrupt 1 input A
	EXINT13C			Interrupt 13 input C
	ADCOMPCH5			Analog input channel 5
	P33.5	O0		General-purpose output
	—	O1		Reserved
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output
	CAN13_TXD	O8		CAN transmit output node 3
	EGTM_TOUT27	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.5	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W13	P33.6	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT0_SENT12B			Receive input channel 12
	ASCLIN8_ARXD			Receive input
	GPT122_T2INA			Trigger/gate input of timer T2
	EGTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_2			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_2			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	UART_RXDL	I#		Receive input L
	SSC_MTSRA			Slave SPI data input A
	SCRDAP0_0			SCRDAP0 input
	T2CCU1_0B			T2 capture 1 input 0B
	EXINT2A			Interrupt 2 input A
	EXINT8B			Interrupt 8 input B
	ADCOMPCH6			Analog input channel 6
	P33.6	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	PSI5S0_TX	O7		TX data output
	SENT0_SPC12	O8		Transmit output
	EGTM_TOUT28	O9		eGTM muxed output
	QSPI4_MTSR	O10		Master SPI data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.6	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MTSR	O#2		Master SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y13	P33.7	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PSI5S0_RXD			RX data input
	SCU_E_REQ4A			ERU channel 4 input A
	SENT1_SENT11B			Receive input channel 11
	GPT122_T2EUDA			Count direction control input of timer T2
	ADC_TRIG60			Triggers from PORTS to ADC
	EGTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	WCAN_RXDB	I#		Wake-up input B
	SSC_SCLKA			Slave SPI clock input A
	T20B			T20 capture input B
	T21EXH			T21 interrupt input H
	T2CCU1_1B			T2 capture 1 input 1B
	EXINT0B			Interrupt 0 input B
	EXINT9B			Interrupt 9 input B
	ADCOMPCH7			Analog input channel 7
	P33.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	ADC_EMUXCTRL13	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	QSPI5_SLSO10	O7		Master slave select output
	SENT1_SPC11	O8		Transmit output
	EGTM_TOUT29	O9		eGTM muxed output
	QSPI4_SCLK	O10		Master SPI clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.7	O#0		General-purpose output
	UART_TXD	O#1		Transmit output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_0	I/O		SCRDAP1 input
	SPD_0	I/O		Single pin DAP0
W14	P33.8	I	FAST / HighZ / VDDEVRSB	General-purpose input
	ASCLIN2_ARXE			Receive input
	SMU_EXT_EMERGENCYSTOP_A_REQ			Emergency Stop External Request A
	SMU_FSPIN0			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	UART_RXDF	I#		Receive input F
	WCAN_RXDO			Wake-up input O
	T21EXN			T21 interrupt input N
	T2CCU1_3D			T2 capture 1 input 3D
	EXINT1B			Interrupt 1 input B
	EXINT11D			Interrupt 11 input D
	I2CSDAD			Serial clock input D
	P33.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	QSPI5_SLSO11_F	O7		Master slave select output
	QSPI6_SLSO13	O8		Master slave select output
	EGTM_TOUT30	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.0	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP0	O		FSP Output Signal - Generated by SMU
Y14	P33.9	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	XTAL3			XTAL3.RTC Oscillator
	GPT122_T4EUDA			Count direction control input of timer T4

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	T1A	I#		T1 capture input A
	T20EXC			T2 interrupt input C
	T2CCU0_0B			T2 capture 0 input 0B
	EXINT3B			Interrupt 3 input B
	EXINT14C			Interrupt 14 input C
	I2CSCLD			Serial clock input D
	P33.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO1	O3		Master slave select output
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ATX	O6		Transmit output
	QSPI5_SLSO12	O7		Master slave select output
	QSPI6_SLSO10	O8		Master slave select output
	EGTM_TOUT31	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.1	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W15	P33.10	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	EGTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	UART_RXDA	I#		Receive input A
	WCAN_RXDA			Wake-up input A
	RTC32_IN			RTC oscillator input
	T20EXP			T20 interrupt input P
	T21CLK32K			T21 external input
	EXINT2B			Interrupt 2 input B
	EXINT15C			Interrupt 15 input C
	P33.10	O0		General-purpose output
	—	O1		Reserved
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S0_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	QSPI5_SLSO13	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT32	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.2	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	XTAL4	PO		XTAL4. RTC Oscillator
Y15	P33.11	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SCLKA			Slave SPI clock inputs
	SMM_ESR2_PORT_IN			ESR2 pad data from PIN Slice
	QSPI5_SCLKF_F			Slave SPI clock inputs
	GPT122_T5INA			Trigger/gate input of timer T5
	EGTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	PMS_ESR2WKP			ESR2 pin input
	SSC_SCLKB	I#		Slave SPI clock input B
	PINRSTA			Reset input A
	T20C			T20 capture input C
	T2CCU0_1B			T2 capture 0 input 1B

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU1_2B			T2 capture 1 input 2B
	EXINT4B			Interrupt 4 input B
	EXINT10B			Interrupt 10 input B
	P33.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN5_ASCLK_F	O5		Shift clock output
	ADC_PWM1	O6		Negative PWM
	QSPI5_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT33	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	PMS_RTCOUT	O12		RTC output for P33.11
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.3	O#0		General-purpose output
	—	O#1		Reserved
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_2	O#6		T2 PWM channel 12
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_ESR2PORST	PO		ESR2 reset output. For details please refer to the PMS/SMM chapter.
W16	P33.12	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	GPT122_T5EUDA			Count direction control input of timer T5
	SMU_FSPIN1			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	PMS_PINCWKP			PINC (P33.12) pin input
	UART_RXDG	I#		Receive input G
	WCAN_RXDG			Wake-up input G
	SSC_MTSRB			Slave SPI data input B
	T1C			T1 capture input C
	T21C			T21 capture input C
	T2CCU0_2B			T2 capture 0 input 2B
	T2CCU1_3B			T2 capture 1 input 3B
	EXINT5B			Interrupt 5 input B
	EXINT11B			Interrupt 11 input B
	P33.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	CAN22_TXD	O5		CAN transmit output node 2
	ADC_PWM0	O6		Positive PWM
	QSPI5_MTSR_F	O7		Master SPI data output
	ASCLIN5_ATX_F	O8		Transmit output
	EGTM_TOUT34	O9		eGTM muxed output
	ASCLIN14_ATX_F	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_3	O#6		T2 PWM channel 13
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP1	O		FSP Output Signal - Generated by SMU
Y16	P33.13	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	ASCLIN1_ARXF			Receive input
	ADC_SIGN1			Sign for Carrier Cancellation
	QSPI4_MRSTA			Master SPI data input
	CAN22_RXDA			CAN receive input node 2
	GPT122_T6EUDA			Count direction control input of core timer T6
	QSPI5_MRSTD_F			Master SPI data input
	ASCLIN16_ARXF			Receive input
	EGTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	PMS_PINBWKP			PINB (P33.13) pin input
	UART_RXDB	I#		Receive input B
	WCAN_RXDC			Wake-up input C
	SSC_MRSTB			Master SPI data input B

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T0C			T0 capture input C
	T20EXD			T20 interrupt input D
	T2CCU0_3B			T2 capture 0 input 3B
	EXINT0C			Interrupt 0 input C
	EXINT6B			Interrupt 6 input B
	ADCOMPCH8			Analog input channel 8
	P33.13	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MRST	O3		Slave SPI data output
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	ASCLIN5_ASLSO_F	O6		Slave select signal output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT35	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
T14	P33.14	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI2_SCLKD			Slave SPI clock inputs
	CBS_TGI6			Trigger input
	CAN31_RXDB			CAN receive input node 1
	QSPI5_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	SSC_SCLKC	I#		Slave SPI clock input C
	EXTNMI			NMI input
	T21EXC			T21 interrupt input C
	EXINT1C			Interrupt 1 input C
	ADCOMPCH9			Analog input channel 9
	P33.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT143	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.6	O#0		General-purpose output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO6	O		Trigger output
U14	P33.15	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	CBS_TGI7			Trigger input
	QSPI5_SLSIB_F			Slave select input
	ASCLIN15_ARXC			Receive input
	SENT1_SENT14D			Receive input channel 14
	QSPI4_MTSRD			Slave SPI data input
	EGTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	UART_RXDE	I#		Receive input E
	PINRSTB			Reset input B
	T20EXE			T20 interrupt input E
	T2CCU0_0C			T2 capture 0 input 0C
	T2CCU1_0C			T2 capture 1 input 0C
	EXINT2C			Interrupt 2 input C
	EXINT3C			Interrupt 3 input C
	EXINT8C			Interrupt 8 input C
	ADCOMPCH10			Analog input channel 10
	P33.15	O0		General-purpose output

(table continues...)

Table 21 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	SENT1_SPC14	O8		Transmit output
	EGTM_TOUT144	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO7	O		Trigger output

3.2.16 BGA292_STD port 34

Table 22 Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U11	P34.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT0_SENT12D			Receive input channel 12
	GPT122_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	UART_RXDD	I#		Receive input D
	T21EXD			T21 interrupt input D
	T2CCU0_1C			T2 capture 0 input 1C
	T2CCU1_1C			T2 capture 1 input 1C
	EXINT4C			Interrupt 4 input C
	EXINT9C			Interrupt 9 input C
	ADCOMPCH11			Analog input channel 11
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	ASCLIN16_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	SENT0_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT146	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.0	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG0	O		PMS debugging power mode K
T12	P34.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	CAN20_RXDC			CAN receive input node 0
	SENT0_SENT14B			Receive input channel 14
	GPT122_T3EUDA			Count direction control input of core timer T3
	I2C1_SDAD			Serial Data Input 3
	EGTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	WCAN_RXDI	I#		Wake-up input I
	T20EXF			T20 interrupt input F
	T2CCU0_2C			T2 capture 0 input 2C
	EXINT5C			Interrupt 5 input C
	ADCOMPCH12			Analog input channel 12
	I2CSDAB			Serial data input B
	P34.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT147	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.1	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG1	O		PMS debugging power mode K
U12	P34.3	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN43_RXDA			CAN receive input node 3
	ASCLIN4_ARXE			Receive input
	SENT1_SENT14B			Receive input channel 14
	GPT122_T4INA			Trigger/gate input of timer T4
	I2C1_SCLD			Serial Clock Input 3
	EGTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PINRSTD	I#		Reset input D
	T21EXE			T21 interrupt input E
	T2CCU0_3C			T2 capture 0 input 3C
	EXINT0D			Interrupt 0 input D
	EXINT6C			Interrupt 6 input C
	ADCOMPCH13			Analog input channel 13
	I2CSCLB			Serial clock input B
	P34.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN4_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT148	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.2	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_3	O#6		T2 PWM channel 13
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG2	O		PMS debugging power mode K
T13	P34.4	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MRSTD			Master SPI data input
	SENT1_SENT13B			Receive input channel 13
	ASCLIN16_ARXE			Receive input
	EGTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	UART_RXDJ	I#		Receive input J
	SSC_MRSTC			Master SPI data input C
	T20EXG			T20 interrupt input P
	T2CCU1_2C			T2 capture 1 input 2C
	EXINT1D			Interrupt 1 input D
	EXINT10C			Interrupt 10 input C
	ADCOMPCH14			Analog input channel 14
	P34.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT149	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG3	O		PMS debugging power mode K
U13	P34.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	QSPI4_MRSTF			Master SPI data input
	SENT0_SENT13C			Receive input channel 13
	EGTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	WCAN_RXDJ	I#		Wake-up input J
	SSC_MTSRC			Slave SPI data input C
	T21EXF			T21 interrupt input F
	T2CCU1_3C			T2 capture 1 input 3C
	EXINT2D			Interrupt 2 input D
	EXINT11C			Interrupt 11 input C
	ADCOMPCH15			Analog input channel 15
	P34.5	O0		General-purpose output

(table continues...)

Table 22 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN8_ATX	O2		Transmit output
	CAN43_TXD	O3		CAN transmit output node 3
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	SENT0_SPC13	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT150	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG4	O		PMS debugging power mode K

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Table 23 Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	ADC_TMADC0CH0			Analog Input for TMADC0 Channel 0
	ADC_DSADC1PA			Analog Input for DSADC1 Positive Input A
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	ADC_TMADC0CH1			Analog Input for TMADC0 Channel 1
	ADC_DSADC1NA			Analog Input for DSADC1 Negative Input A
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	ADC_TMADC0CH2			Analog Input for TMADC0 Channel 2
	ADC_DSADC0PA			Analog Input for DSADC0 Positive Input A
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	ADC_TMADC0CH3			Analog Input for TMADC0 Channel 3
	ADC_DSADC0NA			Analog Input for DSADC0 Negative Input A
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	ADC_TMADC0CH4			Analog Input for TMADC0 Channel 4
	ADC_TMADC1CH0			Analog Input for TMADC1 Channel 0
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	ADC_TMADC0CH5			Analog Input for TMADC0 Channel 5
	ADC_TMADC1CH1			Analog Input for TMADC1 Channel 1
T8	AN6	I	D / HighZ / VDDM	Analog Input 6
	ADC_TMADC0CH6			Analog Input for TMADC0 Channel 6
	ADC_TMADC1CH2			Analog Input for TMADC1 Channel 2
U8	AN7	I	D / HighZ / VDDM	Analog Input 7
	ADC_TMADC0CH7			Analog Input for TMADC0 Channel 7
	ADC_TMADC1CH3			Analog Input for TMADC1 Channel 3
W8	AN8	I	D / HighZ / VDDM	Analog Input 8
	ADC_TMADC0CH8			Analog Input for TMADC0 Channel 8
U7	AN9	I	D / HighZ / VDDM	Analog Input 9
	ADC_TMADC0CH9			Analog Input for TMADC0 Channel 9
Y8	AN10	I	D / HighZ / VDDM	Analog Input 10
	ADC_TMADC0CH10			Analog Input for TMADC0 Channel 10
W7	AN11	I	D / HighZ / VDDM	Analog Input 11
	ADC_TMADC0CH11			Analog Input for TMADC0 Channel 11

(table continues...)

Table 23 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
T7	AN12	I	D / HighZ / VDDM	Analog Input 12
	ADC_TMADC0CH12			Analog Input for TMADC0 Channel 12
	ADC_DSADC0PB			Analog Input for DSADC0 Positive Input B
W6	AN13	I	D / HighZ / VDDM	Analog Input 13
	ADC_TMADC0CH13			Analog Input for TMADC0 Channel 13
	ADC_DSADC0NB			Analog Input for DSADC0 Negative Input B
U6	AN14	I	D / HighZ / VDDM	Analog Input 14
	ADC_TMADC0CH14			Analog Input for TMADC0 Channel 14
	ADC_DSADC1PB			Analog Input for DSADC1 Positive Input B
T6	AN15	I	D / HighZ / VDDM	Analog Input 15
	ADC_TMADC0CH15			Analog Input for TMADC0 Channel 15
	ADC_DSADC1NB			Analog Input for DSADC1 Negative Input B
W5	AN16	I	D / HighZ / VDDM	Analog Input 16
	ADC_TMADC1CH4			Analog Input for TMADC1 Channel 4
U5	AN17 / P40.10	I	S / PU1 / VDDM	Analog Input 17
				General-purpose input
	ADC_TMADC1CH5			Analog Input for TMADC1 Channel 5
	SENT0_SENT5A			Receive input channel 5
W4	AN18 / P40.11	I	S / PU1 / VDDM	Analog Input 18
				General-purpose input
	ADC_TMADC1CH6			Analog Input for TMADC1 Channel 6
	SENT1_SENT5A			Receive input channel 5
W3	AN19 / P40.12	I	S / PU1 / VDDM	Analog Input 19
				General-purpose input
	ADC_TMADC1CH7			Analog Input for TMADC1 Channel 7
	SENT0_SENT6A			Receive input channel 6
Y3	AN20	I	D / HighZ / VDDM	Analog Input 20
	ADC_TMADC1CH8			Analog Input for TMADC1 Channel 8
	ADC_DSADC2PA			Analog Input for DSADC2 Positive Input A
Y2	AN21	I	D / HighZ / VDDM	Analog Input 21
	ADC_TMADC1CH9			Analog Input for TMADC1 Channel 9
	ADC_DSADC2NA			Analog Input for DSADC2 Negative Input A

(table continues...)

Table 23 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
T5	AN22	I	D / HighZ / VDDM	Analog Input 22
	ADC_TMADC1CH10			Analog Input for TMADC1 Channel 10
R5	AN23	I	D / HighZ / VDDM	Analog Input 23
	ADC_TMADC1CH11			Analog Input for TMADC1 Channel 11
W2	AN24 / P40.0	I	S / PU1 / VDDM	Analog Input 24
				General-purpose input
	ADC_TMADC1CH12			Analog Input for TMADC1 Channel 12
	ADC_DSADC2PB			Analog Input for DSADC2 Positive Input B
	SENT0_SENT0A			Receive input channel 0
W1	AN25 / P40.1	I	S / PU1 / VDDM	Analog Input 25
				General-purpose input
	ADC_TMADC1CH13			Analog Input for TMADC1 Channel 13
	ADC_DSADC2NB			Analog Input for DSADC2 Negative Input B
	SENT1_SENT0A			Receive input channel 0
V2	AN26 / P40.2	I	S / PU1 / VDDM	Analog Input 26
				General-purpose input
	ADC_TMADC1CH14			Analog Input for TMADC1 Channel 14
	SENT0_SENT1A			Receive input channel 1
V1	AN27 / P40.3	I	S / PU1 / VDDM	Analog Input 27
				General-purpose input
	ADC_TMADC1CH15			Analog Input for TMADC1 Channel 15
	SENT1_SENT1A			Receive input channel 1
U2	AN28 / P40.13	I	S / PU1 / VDDM	Analog Input 28
				General-purpose input
	ADC_TMADC3CH0			Analog Input for TMADC3 Channel 0
	SENT1_SENT6A			Receive input channel 6
U1	AN29 / P40.14	I	S / PU1 / VDDM	Analog Input 29
				General-purpose input
	ADC_TMADC3CH1			Analog Input for TMADC3 Channel 1
	SENT0_SENT7A			Receive input channel 7
T4	AN30	I	D / HighZ / VDDM	Analog Input 30
	ADC_TMADC3CH2			Analog Input for TMADC3 Channel 2

(table continues...)

Table 23 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
R4	AN31	I	D / HighZ / VDDM	Analog Input 31
	ADC_TMADC3CH3			Analog Input for TMADC3 Channel 3
P4	AN32 / P40.4	I	S / PU1 / VDDM	Analog Input 32
				General-purpose input
	ADC_TMADC3CH4			Analog Input for TMADC3 Channel 4
	SENT0_SENT2A			Receive input channel 2
R1	AN33 / P40.5	I	S / PU1 / VDDM	Analog Input 33
				General-purpose input
	ADC_TMADC3CH5			Analog Input for TMADC3 Channel 5
	SENT1_SENT2A			Receive input channel 2
P5	AN34	I	D / HighZ / VDDM	Analog Input 34
	ADC_TMADC3CH6			Analog Input for TMADC3 Channel 6
R2	AN35	I	D / HighZ / VDDM	Analog Input 35
	ADC_TMADC3CH7			Analog Input for TMADC3 Channel 7
N4	AN36 / P40.6	I	S / PU1 / VDDM	Analog Input 36
				General-purpose input
	ADC_TMADC3CH8			Analog Input for TMADC3 Channel 8
	SENT0_SENT3A			Receive input channel 3
P2	AN37 / P40.7	I	S / PU1 / VDDM	Analog Input 37
				General-purpose input
	ADC_TMADC3CH9			Analog Input for TMADC3 Channel 9
	SENT1_SENT3A			Receive input channel 3
N5	AN38 / P40.8	I	S / PU1 / VDDM	Analog Input 38
				General-purpose input
	ADC_TMADC3CH10			Analog Input for TMADC3 Channel 10
	SENT0_SENT4A			Receive input channel 4
P1	AN39 / P40.9	I	S / PU1 / VDDM	Analog Input 39
				General-purpose input
	ADC_TMADC3CH11			Analog Input for TMADC3 Channel 11
	SENT1_SENT4A			Receive input channel 4
M5	AN40	I	D / HighZ / VDDM	Analog Input 40
	ADC_TMADC3CH12			Analog Input for TMADC3 Channel 12

(table continues...)

Table 23 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
M4	AN41	I	D / HighZ / VDDM	Analog Input 41
	ADC_TMADC3CH13			Analog Input for TMADC3 Channel 13
L5	AN42	I	D / HighZ / VDDM	Analog Input 42
	ADC_TMADC3CH14			Analog Input for TMADC3 Channel 14
L4	AN43	I	D / HighZ / VDDM	Analog Input 43
	ADC_TMADC3CH15			Analog Input for TMADC3 Channel 15

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Table 24 Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
K14	PHY1_TXP	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXP0	O		Transmit data (P line)
L14	PHY1_TXN	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXN0	O		Transmit data (N line)

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Table 25 System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
A1	THD0_A	I	—	Reserved - has to be connected to VSSEXT
B2	THD0_K	I	—	Reserved - has to be connected to VSSEXT
M20	XTAL1	I	XTAL / VDDEXTOSC	XTAL1. Main Oscillator/PLL/Clock generator input
M19	XTAL2	O	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output
L19	TRST	I	FAST / PU / VDDEXT	JTAG Module Reset/Enable Input
	DAPE0	I		DAPE: DAPE0 Data I/O DAPE: DAPE0 Data I/O (PD Devices: VSS)
J16	TCK	I	FAST / PD3 / VDDEXT	JTAG Module Clock Input
	DAP0	I		DAP:DAP0 Clock Input

(table continues...)

Table 25 (continued) System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
K16	TMS	I	FAST / PD3 / VDDEXT	JTAG Module State Machine Control Input
	DAP1	I/O		DAP:DAP1 Data I/O
G16	ESR1	I/O	FAST / PU1 / VDDEXT	ESR1 pad data
	SMM_ESR1_PORT_IN	I		ESR1 pad data from PIN Slice
	PMS_ESR1WKP	I		ESR1 pin input
F16	ESR0	I/O	FAST / OD / VDDEXT	ESR0 pad data
	SMM_ESR0_PORT_IN	I		ESR0 pad data from PIN Slice
	PMS_ESR0WKP	I		ESR0 pin input
G17	PORST	I/O	PORST / PD / VDDEXT	Power on Reset. Additional strong PD in case of power fail.
	PMS_PORSTOUT	O		Power On Reset Output. Additional strong PD in case of power fail.
	PMS_PORSTIN	I		Power On Reset Input. Additional strong PD in case of power fail.

3.2.20 BGA292_STD supply

Table 26 Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
U4	NC1_U4	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
Y1	NC1_Y1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
M1	NC_M1	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
M2	NC_M2	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
N1	NC_N1	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
N2	NC_N2	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
E15	PHYx_RESREF	I	—	PHYx Resistor Reference
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1
T2	VAGND2	I	—	Negative Analog Reference Voltage 2
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
T1	VAREF2	I	—	Positive Analog Reference Voltage 2

(table continues...)

Table 26 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
G13, G8, H12, H7, H9, J13, J8, M8, N12, N7, N9, P8	VDD	I	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
P11	VDD3PMS	I/O	—	Supply Buffer pin for Low quiescent regulator EVR3PMS regulator for 3V3 PMS and Standby domain component
T11	VDDEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
A2, B3, V19, W20	VDDEXT	I	—	External Power Supply (5V / 3.3V)
Y19	VDDEXTDC	I	—	External DCDC Supply (6V)
B18, D16	VDDEXTHS	I	—	External Power Supply (5V / 3.3V)
A19	VDDEXTHS_SENSE	I/O	—	External Power Supply (5V / 3.3V)
N20	VDDEXTOSC	I	—	External Power Supply for Oscillator (shall be supplied with same level as used for VDDEXT)
D5	VDDFLEX	I	—	External Power Supply for FLEX Port Pads (5V / 3.3V)
Y5	VDDM	I	—	External Power Supply (5V / 3.3V)
N14	VDDP3NVM0	I/O	—	Supply for programming / erasing RRAM modules
H14	VDDP3NVM1	I/O	—	Supply for programming / erasing RRAM modules
N19	VDDPHPHY1	I	—	PHY1 External Power Supply (1.8V)
M13	VDDPHY1	I	—	PHY1 Digital Core Power Supply (0.9V / 0.95V / 1V)
P13	VDD_SENSE	I/O	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
Y17	VGATE1N	O	—	DCDC N ch MOSFET gate driver output
Y18	VGATE1P	O	—	DCDC P ch MOSFET gate driver output
G10, G11, G12, G9, H10, H11, J10, J11, J14, J7, K10, K11, K12, K13, K7, K8, K9, L10, L11, L12, L13, L7, L8, L9, M10, M11, M7, N10, N11, P10, P9	VSS	I	—	Digital Ground
B19, D17, D4, E16, E5, T16, U17	VSSEXT	I	—	External Vss

(table continues...)

Table 26 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
W19, Y20	VSSEXTDC	I	—	DCDC Ground
A20	VSSEXTHS_SENSE	I/O	—	External Vss
L20	VSSEXTOSC	I	—	Oscillator Ground
Y4	VSSM	I	—	External Vss
M14	VSSPHY	I	—	PHY Digital Ground
P12	VSS_SENSE	I/O	—	Digital Ground

3.3 Pad Sequence

Related information

Logic symbols for package variants on page 28
BGA292_STD package variant pin configuration on page 28
Pad Sequence on page 173
Legend on page 199

3.3.1 Sequence of pads in pad frame

Table 27 Pad Sequence

Number	Pad name	Pad type	Comment
1	TSHIELD_SOC	—	
2	TREFE_SOC	—	
3	THD0_A	—	Reserved - has to be connected to VSSEXT
4	HEAT_V	—	
5	LS3TO5_INPEN_HWCFG_EXT_N	—	
6	THD0_K	—	Reserved - has to be connected to VSSEXT
7	DECAP20_EXT	—	
8	P10.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
9	SPACER10	—	
10	P10.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
11	PADS_BUF_P10	—	
12	P10.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
13	DECAP20_EXT	—	
14	VDDEXT_50_TL	Vx	Supply Voltage
15	DECAP20_EXT	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
16	P10.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
17	DECAP20_EXT	—	
18	VSSEXT_TL	Vx	Supply Voltage
19	P02.12	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
20	P03.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
21	P03.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
22	P03.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
23	P03.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
24	P03.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
25	P03.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
26	P03.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
27	ANT_SOC	—	
28	CASCGEN_t1	—	
29	LSENPS_t1	—	
30	HEAT_V	—	
31	VDD_V	Vx	Supply Voltage
32	VSS_V	Vx	Supply Voltage
33	LSTRIST_t1	—	
34	VDDEXT_50_TL	Vx	Supply Voltage
35	P03.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
36	VSSEXT_TL	Vx	Supply Voltage
37	P03.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
38	P03.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
39	P03.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
40	P03.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
41	P03.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
42	PADS_BUF_P03	—	
43	P03.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
44	P03.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
45	P02.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
46	P03.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
47	VDDEXT_50_TL	Vx	Supply Voltage
48	P02.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
49	VSSEXT_TL	Vx	Supply Voltage
50	P02.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
51	DECAP40_EXT	—	
52	DECAP40_EXT	—	
53	ANARES_TGATE_6	—	
54	HEAT_V	—	
55	VDD_V	Vx	Supply Voltage
56	VSS_V	Vx	Supply Voltage
57	DECAP20_EXT	—	
58	P02.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
59	DECAP20_EXT	—	
60	TCASC_SOC	—	
61	ANARES_TGATE_5	—	
62	P02.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
63	P02.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
64	P02.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
65	P02.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
66	P02.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
67	P02.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
68	DECAP40_NVM1	—	
69	VDDP3NVM1_33_TL	Vx	Supply Voltage
70	VSSNVM1_TL	Vx	Supply Voltage
71	DECAP40_NVM1	—	
72	VDDEXT_50_TL	Vx	Supply Voltage
73	DECAP40_NVM1	—	
74	P02.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
75	VSSEXT_TL	Vx	Supply Voltage
76	PADS_BUF_P02	—	
77	P02.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
78	P02.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
79	P02.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
80	P02.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
81	DECAP20_EXT	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
82	P01.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
83	P01.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
84	P01.9	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
85	P01.2	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
86	P01.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
87	VDDEXT_50_TL	Vx	Supply Voltage
88	P01.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
89	DECAP20_EXT	—	
90	VSSEXT_TL	Vx	Supply Voltage
91	P01.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
92	P01.4	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
93	P01.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
94	P00.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
95	PADS_BUF_P01	—	
96	ANT_SOC	—	
97	CASCGEN_t2	—	
98	ANT_SOC	—	
99	LSENPS_t2	—	
100	DECAP40_EXT	—	
101	HEAT_V	—	
102	VDD_V	Vx	Supply Voltage
103	VSS_V	Vx	Supply Voltage
104	DECAP20_EXT	—	
105	P01.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
106	DECAP20_EXT	—	
107	LSTRIST_t2	—	
108	P00.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
109	P01.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
110	P00.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
111	P00.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
112	DECAP20_EXT	—	
113	VDDEXT_50_TL	Vx	Supply Voltage
114	P01.5	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
115	VSSEXT_TL	Vx	Supply Voltage
116	P01.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
117	LS3TO5_EXT_WKPCLR_N	—	
118	DECAP20_EXT	—	
119	DECAP40_EXT	—	
120	PADS_BUF_P00	—	
121	VDD_V	Vx	Supply Voltage
122	VSS_V	Vx	Supply Voltage
123	SPACER10	—	
124	P01.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
125	DECAP40_EXT	—	
126	P01.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
127	P01.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
128	DECAP20_EXT	—	
129	HEAT_V	—	
130	BRIDGE_SOC2SB	—	
131	BRIDGE_PMS2SB	—	
132	DECAP40_EVRSB	—	
133	DIODE_TCP	—	
134	DECAP40_EVRSB	—	
135	ANARES_TGATE_5V	—	
136	P35.1	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
137	P35.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
138	P35.0	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
139	LSENPS_TGATE_5V	—	
140	VDDEVRSB_50_PAD	Vx	Supply Voltage
141	P35.5	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
142	VSSEVRSB_PAD	Vx	Supply Voltage
143	DGTPP_CONV	—	
144	TREF2E_CONV	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
145	AN9	D / HighZ / VDDM	Analog Input 9
146	AN10	D / HighZ / VDDM	Analog Input 10
147	AN0	D / HighZ / VDDM	Analog Input 0
148	AN1	D / HighZ / VDDM	Analog Input 1
149	AN2	D / HighZ / VDDM	Analog Input 2
150	AN3	D / HighZ / VDDM	Analog Input 3
151	AN4	D / HighZ / VDDM	Analog Input 4
152	AN5	D / HighZ / VDDM	Analog Input 5
153	AN6	D / HighZ / VDDM	Analog Input 6
154	AN7	D / HighZ / VDDM	Analog Input 7
155	AN8	D / HighZ / VDDM	Analog Input 8
156	AN12	D / HighZ / VDDM	Analog Input 12
157	AN11	D / HighZ / VDDM	Analog Input 11
158	AN14	D / HighZ / VDDM	Analog Input 14
159	AN13	D / HighZ / VDDM	Analog Input 13
160	CASCGENS_VDDM_l	—	
161	VSSM_CONVPAD	Vx	Supply Voltage
162	VDDM_50_CONVPAD _SENSE	Vx	Supply Voltage
163	AN22	D / HighZ / VDDM	Analog Input 22
164	AN16	D / HighZ / VDDM	Analog Input 16
165	AN19/P40.12	S / PU1 / VDDM	Analog Input 19 / General-purpose input
166	AN18/P40.11	S / PU1 / VDDM	Analog Input 18 / General-purpose input
167	AN21	D / HighZ / VDDM	Analog Input 21
168	AN20	D / HighZ / VDDM	Analog Input 20
169	AN23	D / HighZ / VDDM	Analog Input 23
170	AN15	D / HighZ / VDDM	Analog Input 15
171	AN17/P40.10	S / PU1 / VDDM	Analog Input 17 / General-purpose input
172	LSENPS_VDDM_l	—	
173	VAREF1	Vx	Supply Voltage
174	LSTRIST_VDDM_l	—	
175	VAGND1	Vx	Supply Voltage
176	TCASC_CONV	—	
177	LSENPS_VDDM_t	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
178	AN34	D / HighZ / VDDM	Analog Input 34
179	AN35	D / HighZ / VDDM	Analog Input 35
180	AN24/P40.0	S / PU1 / VDDM	Analog Input 24 / General-purpose input
181	AN25/P40.1	S / PU1 / VDDM	Analog Input 25 / General-purpose input
182	AN26/P40.2	S / PU1 / VDDM	Analog Input 26 / General-purpose input
183	AN27/P40.3	S / PU1 / VDDM	Analog Input 27 / General-purpose input
184	AN29/P40.14	S / PU1 / VDDM	Analog Input 29 / General-purpose input
185	AN28/P40.13	S / PU1 / VDDM	Analog Input 28 / General-purpose input
186	AN30	D / HighZ / VDDM	Analog Input 30
187	AN31	D / HighZ / VDDM	Analog Input 31
188	AN32/P40.4	S / PU1 / VDDM	Analog Input 32 / General-purpose input
189	AN33/P40.5	S / PU1 / VDDM	Analog Input 33 / General-purpose input
190	AN36/P40.6	S / PU1 / VDDM	Analog Input 36 / General-purpose input
191	AN37/P40.7	S / PU1 / VDDM	Analog Input 37 / General-purpose input
192	AN38/P40.8	S / PU1 / VDDM	Analog Input 38 / General-purpose input
193	AN39/P40.9	S / PU1 / VDDM	Analog Input 39 / General-purpose input
194	AN40	D / HighZ / VDDM	Analog Input 40
195	AN41	D / HighZ / VDDM	Analog Input 41
196	AN42	D / HighZ / VDDM	Analog Input 42
197	AN43	D / HighZ / VDDM	Analog Input 43
198	LSTRIST_VDDM_t	—	
199	VAGND2	Vx	Supply Voltage
200	VAREF2	Vx	Supply Voltage
201	VAGND3	Vx	Supply Voltage
202	VAREF3	Vx	Supply Voltage
203	CASCGENS_VDDM_t	—	
204	VSSM_CONVPAD	Vx	Supply Voltage
205	VDDM_50_CONVPAD	Vx	Supply Voltage
206	VSSM_CONVIF0	Vx	Supply Voltage
207	VDDM_50_CONVIF0	Vx	Supply Voltage
208	TREF2E_CONV	—	
209	DGTPP_CONV	—	
210	VSSEXT_CONVE	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
211	BUF5V_CONV	—	
212	VDDEXT_50_CONVE	Vx	Supply Voltage
213	CASCGENS_VDDEXT	—	
214	P00.12	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
215	P00.11	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
216	P00.10	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
217	P00.9	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
218	P00.8	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
219	P00.5	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
220	P00.6	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
221	P00.7	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
222	P00.4	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
223	P00.3	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
224	P00.2	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
225	P00.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
226	LSTRIST_VDDEXT	—	
227	LSENPS_VDDEXT	—	
228	TREF2E_CONV	—	
229	DGTPP_CONV	—	
230	P35.3	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
231	P35.4	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
232	DECAP40_EVRSB	—	
233	P33.0	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
234	SPACER10_EVRSB	—	
235	VSS_HS	Vx	Supply Voltage
236	VDD_HS	Vx	Supply Voltage
237	LS3TO5_P33_567_ENPS_SW	—	General-purpose I/O
238	LS3TO5_ADCOMP_SW_CTRL	—	
239	PADS_BUF_P34	—	
240	P33.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
241	P33.3	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
242	P33.2	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
243	P33.4	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
244	P33.5	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
245	VDDEVRSB_50_PAD	Vx	Supply Voltage
246	P34.3	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
247	VSSEVRSB_PAD	Vx	Supply Voltage
248	P34.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
249	P34.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
250	P33.7	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
251	PADS_BUF_P33	—	
252	ANT_PMS	—	
253	CASCGEN_I1	—	
254	ANT_PMS	—	
255	P33.6	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
256	P34.4	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
257	P34.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
258	VDDEVRSB_50_PAD	Vx	Supply Voltage
259	P33.8	FAST / HighZ / VDDEVRSB	General-purpose I/O
260	VSSEVRSB_PAD	Vx	Supply Voltage
261	DECAP40_EVRSB	—	
262	LS3TO5_FSP0_S_PD	—	
263	LSTRIST_I1	—	
264	VSS_HS	Vx	Supply Voltage
265	VDD_HS	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
266	LSENPS_l1	—	
267	LS3TO5_ESR2_S_PD	—	
268	LS3TO5_INPEN_ESR2	—	
269	PADVSS_SENSE	VDDEVRSB	
270	PADVDD_SENSE	VDDEVRSB	
271	LS3TO5_FSP1_S_PD	—	
272	P33.10	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
273	P33.9	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
274	LS3TO5_INPEN_PINC	—	
275	P33.11	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
276	P32.4	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
277	P33.14	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
278	P32.2	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
279	P33.12	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
280	P33.13	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
281	SPACER10_EVRSB	—	
282	VDDEVRSB_50_SENSE_PAD	Vx	Supply Voltage
283	SPACER10_EVRSB	—	
284	P33.15	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
285	VSSEVRSB_PAD	Vx	Supply Voltage
286	P32.7	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
287	P32.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
288	LS3TO5_INPEN_PINB	—	
289	P32.6	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
290	PADS_BUF_P32	—	
291	VSS_HS	Vx	Supply Voltage
292	VDD_HS	Vx	Supply Voltage
293	DECAP40_EVRSB	—	
294	LS3TO5_SB_WKPCLR	—	
295	DECAP40_EVRSB	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
296	DECAP40_NVM0_EVRSB	—	
297	VDDP3NVM0_33_EVRSB_TL	Vx	Supply Voltage
298	VSSNVM0_EVRSB_TL	Vx	Supply Voltage
299	DECAP40_NVM0_EVRSB	—	
300	DECAP40_NVM0_EVRSB	—	
301	VDDPMS1_H	Vx	Supply Voltage
302	VSS_HP	Vx	Supply Voltage
303	DECAP40_EVRSB	—	
304	VDDEVRSB_50_TL	Vx	Supply Voltage
305	VSSQ_TL	Vx	Supply Voltage
306	DECAP40_EVRSB	—	
307	VSSEVRSB_TL	Vx	Supply Voltage
308	VDDEVRSB_50_TL	Vx	Supply Voltage
309	BUF_VDDEVRSB2VCASC	—	
310	DIODE_TCP	—	
311	BRIDGE_PMS2SB	—	
312	VDDP3NVM0_33_PMS_SENSE	Vx	Supply Voltage
313	VSS_PMS	Vx	Supply Voltage
314	VDDP3NVM0_33_PMS	Vx	Supply Voltage
315	PMS_testmode	—	
316	VDDEXT_50_PMS	Vx	Supply Voltage
317	VDDEVRSB_50_PMS	Vx	Supply Voltage
318	VDD3PMS_27_PMS_SENSE	Vx	Supply Voltage
319	VSS_PMS	Vx	Supply Voltage
320	DGTPP_PMS	—	
321	VDDP3NVM0_33_PMS	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
322	VDDP3NVM0_33_PMS	Vx	Supply Voltage
323	VDDEXT_50_PMS	Vx	Supply Voltage
324	VDDEXT_50_PMS	Vx	Supply Voltage
325	DGTPP_PMS	—	
326	VSSEXTDC_PMS	Vx	Supply Voltage
327	VSSEXTDC_PMS	Vx	Supply Voltage
328	VSSEXTDC_PMS	Vx	Supply Voltage
329	VSSEXTDC_PMS	Vx	Supply Voltage
330	CTRL1V3N3	Vx	
331	CTRL1V3N0	Vx / VDDEXTDC	
332	CTRL1V3N1	Vx / VDDEXTDC	
333	CTRL1V3N2	Vx	
334	TPP7VLS_PMS	—	
335	CTRL1V3P3	Vx	
336	CTRL1V3P2	Vx	
337	CTRL1V3P1	Vx / VDDEXTDC	
338	CTRL1V3P0	Vx / VDDEXTDC	
339	VDDEXTDC_65_PMS	Vx	Supply Voltage
340	VDDEXTDC_65_PMS	Vx	Supply Voltage
341	VDDEXTDC_65_PMS	Vx	Supply Voltage
342	VDDEXTDC_65_PMS	Vx	Supply Voltage
343	TPP7V_PMS	—	
344	VDDEXTDC_65_PMS_SENSE	Vx	Supply Voltage
345	TPP7VE_PMS	—	
346	TCASC_PMS	—	
347	VDD3PMS_27_PMS	Vx	Supply Voltage
348	VDD3PMS_27_PMS	Vx	Supply Voltage
349	VDDEVRSB_50_PMS	Vx	Supply Voltage
350	VDDEVRSB_50_PMS	Vx	Supply Voltage
351	DGTPP_PMS	—	
352	BRIDGE_SOC2SB	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
353	BUF_VDDEXT2VCAS C	—	
354	HEAT_H	—	
355	DECAP20_EXT	—	
356	P31.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
357	DECAP20_EXT	—	
358	VSS_H	Vx	Supply Voltage
359	VDD_H	Vx	Supply Voltage
360	LS3TO5_EXT_WKPC LR_W	—	
361	PADS_BUF_P30	—	
362	LSTRIST_I2	—	
363	LSENPS_I2	—	
364	P31.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
365	P30.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
366	P30.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
367	P30.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
368	P30.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
369	DECAP20_EXT	—	
370	VDDEXT_50_SENSE_ TL	Vx	Supply Voltage
371	DECAP20_EXT	—	
372	P30.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
373	VSSEXT_TL	Vx	Supply Voltage
374	P30.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
375	P30.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
376	P30.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
377	P30.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
378	P30.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
379	HEAT_H	—	
380	CASCGEN_I2	—	
381	ANT_SOC	—	
382	P30.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
383	P30.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
384	P30.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
385	DECAP20_EXT	—	
386	VDDEXT_50_TL	Vx	Supply Voltage
387	P30.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
388	DECAP20_EXT	—	
389	VSSEXT_TL	Vx	Supply Voltage
390	P30.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
391	PADS_BUF_P23	—	
392	P30.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
393	DECAP40_EXT	—	
394	DECAP20_EXT	—	
395	P23.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
396	TREFE_SOC	—	
397	TSHIELD_SOC	—	
398	CRACK_SENSOR_1	—	
399	TOXMON	—	
400	TCASC_SOC	—	
401	P23.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
402	HEAT_V	—	
403	DECAP40_EXT	—	
404	P23.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
405	P23.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
406	DECAP20_EXT	—	
407	P23.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
408	DECAP40_EXT	—	
409	DECAP30_EXT	—	
410	DECAP20_EXT	—	
411	VSS_V	Vx	Supply Voltage
412	VDD_V	Vx	Supply Voltage
413	DECAP30_EXT	—	
414	VDDEXT_50_TL	Vx	Supply Voltage
415	P23.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
416	VSSEXT_TL	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
417	P23.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
418	P23.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
419	P22.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
420	TREFE_SOC	—	
421	PADS_BUF_P22	—	
422	P22.3	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
423	P22.2	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
424	HEAT_V	—	
425	P22.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
426	DECAP20_EXT	—	
427	P22.1	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
428	P22.0	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
429	ANT_PL_SOC	—	
430	P22.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
431	VDDEXT_50_TL	Vx	Supply Voltage
432	P22.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
433	VSSEXT_TL	Vx	Supply Voltage
434	P22.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
435	LSTRIST_b1	—	
436	CASCGEN_b1	—	
437	LSENPS_b1	—	
438	P22.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
439	P22.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
440	P22.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
441	P25.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
442	PADS_BUF_P25	—	
443	DECAP40_NVM0	—	
444	DECAP40_NVM0	—	
445	VSSNVM0_TL	Vx	Supply Voltage
446	VDDP3NVM0_33_TL	Vx	Supply Voltage
447	DECAP40_NVM0	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
448	HEAT_V	—	
449	VDD_V	Vx	Supply Voltage
450	VSS_V	Vx	Supply Voltage
451	DECAP40_EXT	—	
452	VDDEXTOSC_50_TL	Vx	Supply Voltage
453	XTAL1	XTAL / VDDEXTOSC	XTAL1. Main Oscillator/PLL/Clock generator input XTAL1. Main Oscillator/PLL/Clock Generator Input.
454	XTAL2	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
455	VSS_OSC	Vx	Supply Voltage
456	PHYx_RESREF	PHY	
457	VSSPHY1_TL	Vx	Supply Voltage
458	VDDPHY1_10_TL	Vx	Supply Voltage
459	VDDPHPHY1_18_TL	Vx	Supply Voltage
460	VSSPHY1_TL	Vx	Supply Voltage
461	VSSPHY1_TL	Vx	Supply Voltage
462	PHY1_TXP	PHY / VDDPHPHY1	Transmit data (P line)
463	VDDPHY1_10_TL	Vx	Supply Voltage
464	PHY1_TXN	PHY / VDDPHPHY1	Transmit data (N line)
465	VDDPHY1_10_TL	Vx	Supply Voltage
466	VSSPHY1_TL	Vx	Supply Voltage
467	VSSPHY1_TL	Vx	Supply Voltage
468	PHY1_RXP	PHY / VDDPHPHY1	Receive data (P line)
469	VDDPHPHY1_18_TL	Vx	Supply Voltage
470	PHY1_RXN	PHY / VDDPHPHY1	Receive data (N line)
471	VDDPHY1_10_TL	Vx	Supply Voltage
472	VSSPHY1_TL	Vx	Supply Voltage
473	VSSPHY_LDO	Vx	Supply Voltage
474	VDDPHPHY_18_LDO	Vx	Supply Voltage
475	VDDEXT_33_LDO	Vx	Supply Voltage
476	VSSEXT_LDO	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
477	SPACER10	—	
478	BANDGAP_VLVDS	—	
479	HEAT_V	—	
480	ANT_PL_SOC	—	
481	TRST	FAST / PU / VDDEXT	
482	ANT_PL_SOC	—	
483	PADS_BUF_P21	—	
484	LS3TO5_BG_B_BGEN5V_I	—	
485	VSS_V	Vx	Supply Voltage
486	VDD_V	Vx	Supply Voltage
487	DECAP20_EXT	—	
488	P21.3	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
489	P21.2	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
490	DECAP20_EXT	—	
491	TCK	FAST / PD3 / VDDEXT	
492	VDDEXT_50_TL	Vx	Supply Voltage
493	TMS	FAST / PD3 / VDDEXT	
494	VSSEXT_TL	Vx	Supply Voltage
495	P21.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
496	DECAP20_EXT	—	
497	P21.5	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
498	P21.4	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
499	LS3TO5_INPEN_ESR1	—	
500	P21.6	FAST / PD3 / VDDEXT / ES	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
501	HEAT_V	—	
502	LSTRIST_b2	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
503	VSS_V	Vx	Supply Voltage
504	VDD_V	Vx	Supply Voltage
505	LSENPS_b2	—	
506	P21.1	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
507	P21.0	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
508	TREFE_SOC	—	
509	P20.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
510	LS3TO5_INPEN_HWCFG_EXT_S	—	
511	VDDEXT_50_TL	Vx	Supply Voltage
512	DECAP40_NVM1	—	
513	P20.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
514	VSSEXT_TL	Vx	Supply Voltage
515	DECAP40_NVM1	—	
516	VDDP3NVM1_33_TL	Vx	Supply Voltage
517	VSSNVM1_TL	Vx	Supply Voltage
518	DECAP40_NVM1	—	
519	P20.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
520	ESR1	FAST / PU1 / VDDEXT	External System Request Reset 1. Default NMI function (Configuration options see also SMM / SCU chapter for details). EVR Wakeup Source. Behavior after power-on can be different. See also SMM chapter: External service request interface. Behavior for system reset differs to the warm power-on reset behavior and is in that case always pull-up
521	PADS_BUF_P20	—	
522	ANT_SOC	—	
523	CASCGEN_b2	—	
524	HEAT_V	—	
525	LS3TO5_INPEN_ESR0	—	
526	LS3TO5_ESR0_S_PD	—	
527	VSS_V	Vx	Supply Voltage
528	VDD_V	Vx	Supply Voltage

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
529	LSENPS_ESR0	—	
530	ESR0	FAST / OD / VDDEXT	External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SMM chapter for details. Behavior after power-on can be different. See also SMM chapter "External service request interface (ESRx)
531	LS3TO5_PORST_S_PD	—	
532	PORST	PORST / PD / VDDEXT	Power On Reset Input. Additional strong PD in case of power fail.
533	LS3TO5_PORST_W_PD	—	
534	P20.2	S / PU / VDDEXT	General-purpose I/O This pin is latched at power on reset release to enter test mode.
535	AND_WAKEUP_EXT_EXTHS	—	
536	DIODE	—	
537	P20.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
538	P20.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
539	P20.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
540	P20.11	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
541	VDDEXTHS_50_TL	Vx	Supply Voltage
542	P20.10	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
543	VSSEXTHS_TL	Vx	Supply Voltage
544	P20.9	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
545	LSTRIST_b3	—	
546	CASCGEN_b3	—	
547	DECAP20_EXTHS	—	
548	LSENPS_b3	—	
549	VSS_V	Vx	Supply Voltage
550	VDD_V	Vx	Supply Voltage
551	HEAT_V	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
552	P20.12	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
553	P20.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
554	DECAP20_EXTHS	—	
555	VDDEXTHS_50_TL_UNLOADED	Vx	Supply Voltage
556	DECAP20_EXTHS	—	
557	P20.13	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
558	DECAP30_EXTHS	—	
559	VSSEXTHS_TL_UNLOADED	Vx	Supply Voltage
560	DECAP40_EXTHS	—	
561	DECAP40_EXTHS	—	
562	DECAP30_EXTHS	—	
563	DECAP30_EXTHS	—	
564	Bridge_port16	—	
565	P16_SPARE	VDDHSIF	
566	DECAP11_HSIF	—	
567	VSS_33_H	Vx	Supply Voltage
568	VDD_33_H	Vx	Supply Voltage
569	DECAP40_HSIF	—	
570	DECAP40_HSIF	—	
571	P16.0	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
572	P16.1	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
573	DECAP40_HSIF	—	
574	VDDHSIF_33_TL	Vx	Supply Voltage
575	P16.3	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
576	P16.2	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
577	VSSHSIF_TL	Vx	Supply Voltage
578	P16.5	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
579	P16.4	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
580	VDDHSIF_33_TL	Vx	Supply Voltage
581	P16.8	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
582	TRIMANA	—	
583	P16.6	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
584	VSSHSIF_TL	Vx	Supply Voltage
585	P16.7	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
586	VDDHSIF_33_TL	Vx	Supply Voltage
587	P16.9	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
588	P16.10	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
589	VSSHSIF_TL	Vx	Supply Voltage
590	P16.12	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
591	P16.13	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
592	VDDHSIF_33_TL	Vx	Supply Voltage
593	P16.11	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
594	P16.14	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
595	LSENPS_P16	—	
596	VSSHSIF_TL	Vx	Supply Voltage
597	DECAP40_HSIF	—	
598	LSTRIST_P16	—	
599	VDD_33_H	Vx	Supply Voltage
600	VSS_33_H	Vx	Supply Voltage
601	Bridge_port16	—	
602	HEAT_H	—	
603	PADS_BUF_SOUTH	—	
604	P15.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
605	ANARES_TGATE_2	—	
606	P15.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
607	ANARES_TGATE_1	—	
608	P15.4	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
609	P15.1	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
610	ANARES_TGATE_3	—	
611	ANARES_TGATE_4	—	
612	P15.0	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
613	VDDEXTHS_50_TL	Vx	Supply Voltage
614	P15.3	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
615	VSSEXTHS_TL	Vx	Supply Voltage
616	P15.2	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
617	P15.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
618	P15.10	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
619	P15.11	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
620	P15.13	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
621	P15.12	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
622	P15.15	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
623	P15.5	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
624	P15.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
625	VDDEXTHS_50_TL	Vx	Supply Voltage
626	DECAP20_EXTHS	—	
627	P14.11	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
628	VSSEXTHS_TL	Vx	Supply Voltage
629	ANT_SOC	—	
630	P14.12	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
631	P14.13	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
632	PADS_BUF_P15	—	
633	VDD_H	Vx	Supply Voltage
634	VSS_H	Vx	Supply Voltage
635	LSENPS_r1	—	
636	HEAT_H	—	
637	CASCGEN_r1	—	
638	LSTRIST_r1	—	
639	P13.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
640	DECAP40_NVM1	—	
641	DECAP40_NVM1	—	
642	VSSNVM1_TL	Vx	Supply Voltage
643	VDDP3NVM1_33_TL	Vx	Supply Voltage
644	DECAP40_NVM1	—	
645	P13.9	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
646	P14.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
647	P14.15	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
648	TCASC_SOC	—	
649	P14.0	FAST / PU1 / VDDEXTHS / ES2	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
650	VDDEXTHS_50_TL	Vx	Supply Voltage
651	DECAP20_EXTHS	—	
652	P13.5	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
653	DECAP20_EXTHS	—	
654	VSSEXTHS_TL	Vx	Supply Voltage
655	LS3TO5_INPEN_PIN A	—	
656	P13.4	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
657	P14.3	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
658	P14.1	FAST / PU1 / VDDEXTHS / ES2	General-purpose I/O
659	P13.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
660	P13.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
661	P14.2	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
662	DECAP20_EXTHS	—	
663	HEAT_H	—	
664	P14.4	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
665	DECAP20_EXTHS	—	
666	VDD_H	Vx	Supply Voltage
667	VSS_H	Vx	Supply Voltage
668	LS3TO5_INPEN_HW CFG_EXTHS_E	—	
669	LSTRIST_r2	—	
670	LSENPS_r2	—	
671	LSTRIST_HWCFG_EX THS	—	
672	ANT_SOC	—	
673	CASCGEN_r2	—	
674	PADS_BUF_P14	—	
675	P14.5	FAST / PU2 / VDDEXTHS / ES	General-purpose I/O
676	VDDEXTHS_50_TL	Vx	Supply Voltage
677	P14.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
678	VSSEXTHS_TL	Vx	Supply Voltage
679	P14.8	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
680	P14.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
681	DECAP40_EXTHS	—	
682	P13.10	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
683	LS3TO5_TRIST_HWCFG_EXTHS	—	
684	VDD_H	Vx	Supply Voltage
685	VSS_H	Vx	Supply Voltage
686	DECAP30_EXTHS	—	
687	LS3TO5_BG_R_BGEN5V_I	—	
688	DECAP20_EXTHS	—	
689	ANT_SOC	—	
690	LS3TO5_EXTHS_WKPCLR	—	
691	TREFE_SOC	—	
692	P14.9	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
693	P14.10	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
694	HEAT_H	—	
695	BANDGAP_HLVDS	—	
696	PADS_BUF_P13	—	
697	P13.11	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
698	DECAP20_EXTHS	—	
699	P13.0	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
700	P13.1	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
701	DECAP20_EXTHS	—	
702	P13.12	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
703	VDDEXTHS_50_TL	Vx	Supply Voltage
704	DECAP20_EXTHS	—	
705	P13.13	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
706	VSSEXTHS_TL	Vx	Supply Voltage
707	P13.15	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
708	DECAP20_EXTHS	—	

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
709	P13.2	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
710	P13.3	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
711	TREFE_SOC	—	
712	HEAT_H	—	
713	P13.14	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
714	DIODE	—	
715	P11.3	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
716	LSTRIST_r3	—	
717	VDD_H	Vx	Supply Voltage
718	VSS_H	Vx	Supply Voltage
719	LSENPS_r3	—	
720	DECAP20_FLEX	—	
721	CASCGEN_r3	—	
722	DECAP20_FLEX	—	
723	P12.1	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
724	P12.0	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
725	P11.6	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
726	DECAP20_FLEX	—	
727	VDDFLEX_50_SENSE_TL	Vx	Supply Voltage
728	DECAP20_FLEX	—	
729	P11.0	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
730	DECAP20_FLEX	—	
731	VSSFLEX_TL	Vx	Supply Voltage
732	PADS_BUF_P11	—	
733	P11.2	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
734	P11.4	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
735	P11.5	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
736	P11.12	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
737	P11.10	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
738	P11.1	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
739	P11.7	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O

(table continues...)

Table 27 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
740	P11.9	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
741	P11.14	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
742	DECAP20_FLEX	—	
743	VDDFLEX_50_TL	Vx	Supply Voltage
744	P11.11	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
745	DECAP20_FLEX	—	
746	VSSFLEX_TL	Vx	Supply Voltage
747	DECAP20_FLEX	—	
748	P11.13	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
749	HEAT_H	—	
750	P11.15	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
751	DECAP20_FLEX	—	
752	P11.8	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
753	DIODE	—	
754	VDDEXT_50_TL	Vx	Supply Voltage
755	P10.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
756	DECAP30_EXT	—	
757	VSSEXT_TL	Vx	Supply Voltage
758	P10.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
759	LSTRIST_HWCFG_EXT	—	
760	P10.5	FAST / PU2 / VDDEXT / ES	General-purpose I/O
761	P10.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
762	P10.6	FAST / PU2 / VDDEXT / ES	General-purpose I/O
763	LS3TO5_TRIST_HWCFG_EXT	—	

3.4 Legend

Column 'Ctrl.'

- I = Input (for GPIO port lines with Pn_DRVCFG bit field Selection MODE = $0XXXX_B$)
- O = Output (for GPIO port lines the `O´ represents the HWOUT functions which are being controlled directly by the mapped hardware module)
- PO = Priority Output (for GPIO port lines the `PO´ represents the priority functions controlled by the Pn_PCSRSEL.PCSR bit-field, where PCSR is set)
- O0 = Output with Pn_DRVCFG bit field selection MODE = $1X0000_B$
- O1 = Output with Pn_DRVCFG bit field selection MODE = $1X0001_B$ (ALT1)
- O2 = Output with Pn_DRVCFG bit field selection MODE = $1X0010_B$ (ALT2)
- O3 = Output with Pn_DRVCFG bit field selection MODE = $1X0011_B$ (ALT3)
- O4 = Output with Pn_DRVCFG bit field selection MODE = $1X0100_B$ (ALT4)
- O5 = Output with Pn_DRVCFG bit field selection MODE = $1X0101_B$ (ALT5)
- O6 = Output with Pn_DRVCFG bit field selection MODE = $1X0110_B$ (ALT6)
- O7 = Output with Pn_DRVCFG bit field selection MODE = $1X0111_B$ (ALT7)
- O8 = Output with Pn_DRVCFG bit field selection MODE = $1X1000_B$ (ALT8)
- O9 = Output with Pn_DRVCFG bit field selection MODE = $1X1001_B$ (ALT9)
- O10 = Output with Pn_DRVCFG bit field selection MODE = $1X1010_B$ (ALT10)
- O11 = Output with Pn_DRVCFG bit field selection MODE = $1X1011_B$ (ALT11)
- O12 = Output with Pn_DRVCFG bit field selection MODE = $1X1100_B$ (ALT12)
- O13 = Output with Pn_DRVCFG bit field selection MODE = $1X1101_B$ (ALT13)
- O14 = Output with Pn_DRVCFG bit field selection MODE = $1X1110_B$ (ALT14)
- O15 = Output with Pn_DRVCFG bit field selection MODE = $1X1111_B$ (ALT15)
- I# and O# mark SCR peripheral mappings

Column 'Buffer type'

- FAST = Pad class FAST (5V/3.3V)
- HSFAST = Pad class HSFAST (3.3V/1.8V)
- SLOW = Pad class SLOW (5V/3.3V)
- LVDS_TX = Pad class LVDS Transmit
- LVDS_RX = Pad class LVDS Receive
- S = Pad class S (Analog Input overlayed with General Purpose Input)
- D = Pad class D (Analog Input)
- Porst = Porst input Pad
- XTAL1 = XTAL1 input Pad
- XTAL2 = XTAL2 output Pad
- Startup: Startup behavior in this document describes the behavior from supply rampup until LVD reset release of VDDEXT and VDDEVRSB is reached

  For startup behavior until VDDPPA and VDDPPSB level is reached please refer to PMS table "Pad state depending on VDDEVRSB and VDDEXT supply"
- PU = with pull-up device connected during startup + up to 12 x (1/fSB). The default state during and after reset ($\overline{\text{PORST}}$ = 0) is pull-up. Pull-up in Standby mode
- PU1 = with pull-up device connected, HighZ for VDDEVRSB pins, during startup + up to 12 x (1/fSB). The default state of GPIOs (Px.y) during reset ($\overline{\text{PORST}}$ = 0) is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4). The default state of GPIOs (Px.y) after reset ($\overline{\text{PORST}}$ = 1) is controlled through PORT reset value determined by PMS_PADCON.ALLTRIST (HWCFG6 P14.4). In Standby Mode the state is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4). See PMS, HWCFG[6]

- PU2 = with pull-up device connected during startup + up to 12 x (1/fSB) and reset ($\overline{\text{PORST}}$ = 0). The default state of GPIOs (Px.y) after reset ($\overline{\text{PORST}}$ = 1) is controlled through PORT reset value determined by PMS_PADCON.ALLTRIST (HWCFG6 P14.4). In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4)
- PD = with pull-down device connected during startup + up to 12 x (1/fSB). The default state during and after reset ($\overline{\text{PORST}}$ = 0) is pull-down. HighZ in Standby mode
- PD3 = with pull-down device connected during startup + up to 12 x (1/fSB). The default state of Pins during reset ($\overline{\text{PORST}}$ = 0) is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) with pull-down behavior if ALLTRIST=0. The default state after PORST release is pull-down with transition of the Pad Level from AL to TTL. In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) with pull-down behavior if ALLTRIST=0
- OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
- ES = Supports Emergency Stop
- ES1 = ES. ES is controlled by Pn_PCSRSEL register
- ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message
- ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI
- ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode
- ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR
- ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event

Related information

Logic symbols for package variants on page 28
BGA292_STD package variant pin configuration on page 28
Pad Sequence on page 173

4 Electrical characteristics

Attention**:* ***For TC48x AB step, all electrical parameters referenced in this document are to be treated as preliminary and are subject to change without notice.

4.1 Parameter interpretation

The parameters listed in this section represent both the characteristics of the device and its requirements on the system. To aid the interpretation of the parameters when evaluating them for a design, they are marked with a two-letter abbreviation in the 'Symbol' column.

- **CC**
  - Controller Characteristics which are a distinctive feature of the device and must be taken into account for a system design
- **SR**
  - System Requirements which must be provided by the microcontroller system in which the device is designed in to

4.2 Absolute maximum ratings

Note: *Stresses above the values listed under 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*

4.2.1 Absolute maximum ratings

Table 28 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} *SR*	-65	-	150	°C	Up to 65 h at T_J = 150°C
Maximum Junction Temperature	T_J *SR*	-40	-	160[1]	°C	
Voltage at $V_{DDEXTDC}$ EVRC supply pin with respect to $V_{SSEXTDC}$	$V_{DDEXTDC}$ *SR*	-0.7	-	7.0	V	Up to 2.8 h; EVRC in reset (no switching)
Voltage at V_{DDM}, V_{DDEXT} / $V_{DDEXTHS}$, V_{DDFLEX} and $V_{DDEVRSB}$ power supply pins with respect to V_{SSEXT}	V_{PADIO} *SR*	-0.7	-	6.5	V	Up to 2.8 h
		-0.7	-	5.7	V	Up to 72 h
Voltage at V_{DD} and V_{DDPHYx} power supply pins with respect to V_{SS}[2) 3)]	V_{DD} *SR*	-0.7	-	1.2	V	Up to 2.8 h
		-0.7	-	1.14	V	Up to 72 h
Voltage at $V_{DDPHPHYx}$ power supply pins with respect to V_{SS}	$V_{DDPHPHYx}$ *SR*	-0.7	-	2.4	V	Up to 2.8 h
		-0.7	-	2.0	V	Up to 72 h
Voltage on all analog and class S input pins with respect to V_{SS}[4)]	V_{IN} *SR*	-0.7	-	6.5	V	Up to 2.8 h
Voltage on V_{DDPHYx} (HSPHY) input pins with respect to V_{SSPHY}[4)]	V_{IN} *SR*	-0.7	-	1.2	V	Up to 2.8 h
Voltage on all other input pins with respect to V_{SS}.[4)]	V_{IN} *SR*	-0.7	-	6.5	V	Up to 2.8 h
Input current on any pin during overload condition [5)]	I_{IN} *SR*	-10	-	10	mA	Up to 2.8 h
Absolute maximum sum of all input circuit currents during overload condition for all ports[5)]	ΣI_{INx} *SR*	-100	-	100	mA	

1) Continuous operation of the device at Tj absolute max. is prohibited. Duration must comply with the temperature profiles approved by Infineon
2) Valid for cumulated overshoots of up to 2.8 h
3) Due to EVRC output voltage oscillation during switch off phase, V_{DD} can drop down to -0.7 V. For VDD an input level down up to -0.7 V during switch off phase will not cause any damage or reliability issues.
4) Voltages below V_{IN} (Min) have no impact to the device reliability as long as the times and currents defined in section Pin reliability in overload for the affected pad(s) are not violated.

5) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device

4.3 Pin reliability in overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- Allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined, the allowed time includes example temperature profiles. The number of hours in example temperature profiles are examples only, and the applicable numbers are defined by the customer profiles accepted by Infineon.
- Operating conditions are met for
  - pad supply levels
  - temperature

If a pin current is out of the operating conditions but within the overload parameters, then the parameters functionality of this pin as stated in the operating conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Related information

Operating conditions on page 206
Quality declarations on page 332
Example temperature profiles on page 211

4.3.1 Overload characteristics

Table 29 Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	Except LVDS
		-15[1)]	-	15[1)]	mA	Except LVDS; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-5	-	5	mA	Limited to 60 h over lifetime
		-3	-	3	mA	
Absolute sum of all analog input currents for analog inputs during overload conditon	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	V_{DDIO} + 2[2)]	V	Limited to 60 h over lifetime; valid for non LVDS and analog pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	

(table continues...)

Table 29 (continued) Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Static pin output current	I_{OUT} CC	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong
Overload coupling factor for digital inputs, negative	K_{OVDN} CC	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour fast pads; -5 mA < I_{IN} < 0 mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour slow pads; -5 mA < I_{IN} < 0 mA
		-	-	0.87		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	0.55		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} CC	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbour GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	$5*10^{-3}$		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for analog inputs, negative[3)]	K_{OVAN} CC	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5 mA < I_{IN} < 0 mA
		-	-	$1*10^{-5}$		else -5 mA < I_{IN} < 0 mA
Overload coupling factor for analog inputs, positive[3) 4)]	K_{OVAP} CC	-	-	$2*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; 0 mA < I_{IN} < 5 mA
		-	-	$2*10^{-5}$		else 0 mA < I_{IN} < 5 mA

1) Reduced TMADC / DSADC (if feature available) result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.
2) VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB
3) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.
4) In case of overload condition on analog inputs, the V_{DDEXT}/V_{DDM} supply must not float.

4.4 Operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC48x STD.

Digital supply voltages applied to the TC48x STD must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise stated in the Note / Test Condition column.

Related information

Pin reliability in overload on page 204

4.4.1 Clock operating conditions

Table 30 Clock operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
System PLL and Peripheral PLL clocks						
PLL0 output frequency from SYS PLL	f_{PLL0} *SR*	25	-	400	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} *SR*	25	-	160	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} *SR*	50	-	200	MHz	
PLL3 output frequency from PER PLL	f_{PLL3} *SR*	50	-	400[1)]	MHz	
System clocks - CPU						
CPU frequency (All CPUs)	f_{CPUx} *SR*	25[2)]	-	400	MHz	
CPU-CS frequency	f_{CPU_CS} *SR*	25[2)]	-	200	MHz	
System clocks						
SRI frequency	f_{SRI} *SR*	25[2)]	-	400	MHz	
SPB frequency	f_{SPB} *SR*	25[2)]	-	100	MHz	
TPB frequency[3)]	f_{TPB} *SR*	-	-	200	MHz	
COMPB frequency	f_{COMPB} *SR*	25[2)]	-	100	MHz	
FSI frequency	f_{FSI} *SR*	25[4)]	-	100	MHz	
eGTM frequency	f_{eGTM} *SR*	-	-	400	MHz	
LETH frequency	f_{LETH} *SR*	125	-	200	MHz	
MCANH frequency	f_{MCANH} *SR*	f_{MCAN}	-	200	MHz	
CANXL host frequency	f_{CANXLH} *SR*	f_{CANXL}	-	200	MHz	
Peripheral clocks						
DSADC frequency	f_{DSADC} *SR*	-	160[5)]	-	MHz	
TMADC frequency[6)]	f_{ADC} *SR*	-	160[5)]	-	MHz	
ERAY frequency	f_{ERAY} *SR*	-	80	-	MHz	
ASCLIN frequency	$f_{ASCLINx}$ *SR*	-	-	200	MHz	

(table continues...)

Table 30 (continued) Clock operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CAN frequency	f_{MCAN} *SR*	-	-	160	MHz	
CANXL frequency	f_{CANXL} *SR*	-	-	160	MHz	
LETH frequency	$f_{LETH100}$ *SR*	-	200[5]	-	MHz	Setting required when TC14 3 pin interface is used.
I2C frequency	f_{I2C} *SR*	-	-	100	MHz	
QSPI frequency	f_{QSPI} *SR*	-	-	200	MHz	
xSPI frequency[7]	f_{XSPI} *SR*	-	-	200[8]	MHz	
SGBT frequency	f_{SGBT} *SR*	-	20	25	MHz	
HRPWM reference clock frequency	f_{HRPWM} *SR*	-	f_{PLL0}	-	MHz	In case of HRPWM operation f_{PLL0} has to be set to 400 MHz

1) 400 MHz is the maximum PLL3 operating frequency for test operations only. It is strongly recommended that applications use the PLL3 output frequency of 200 MHz.
2) In case of operation with the f (MIN) value the ratio of f (MIN) / f_{SRI} and f(MIN) / f_{SPB} shall be 1/1
3) f_{TPB} needs to be at least two times higher than f_{SPB}
4) For FSI frequency f_{FSI} < 100 MHz the bank sleep feature shall not be used to ensure a proper shutdown operation of the NVM in case of a reset. Operation at f_{FSI} (Min) prolongs data memory and SOTA program memory write times significantly.
5) The proper functionality of the module can only be ensured for the typical clock frequency setting.
6) This clock is also used for CDSP modules (if available)
7) The appropriate baud rate divider in CCU and XSPI for the maximum supported data rate in each device must be selected for both fast (via HSPHY, if applicable) and slow (via GPIO) XSPI interfaces
8) The max. frequency setting is also valid for the clock named f_{XSPISL}.

Related information

Supply operating conditions on page 207
Limitation of supply voltage over time on page 210
Temperature operating conditions on page 211
Example temperature profiles on page 211

4.4.2 Supply operating conditions

Table 31 Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for EVRC DCDC regulator and MOSFET gate driver	$V_{DDEXTDC}$ *SR*	3.6	-	6.5	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode with EVRC active. Maximum DC voltage is 6.2V
		2.97[1]	-	5.5	V	HWCFG [2:1] = [00]. EVRC not used
		2.97[1]	-	3.63	V	HWCFG [2:1] = [01 or 10]. Low-voltage $V_{DDEXTDC}$ modes.

(table continues...)

Table 31 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for IO supply pins	V_{DDEXT} *SR*	4.5	5.0	5.5[2]	V	Nominal 5 V Pad / Port Pin supply range. 5 V pad parameters are valid. 5 V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid; a running NVM command sequence (e.g. program or erase) shall be suspended or aborted
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
External supply voltage for IO supply pins	$V_{DDEXTHS}$ *SR*	4.5	5.0	5.5[2]	V	Nominal 5 V Pad / Port Pin supply range. 5 V pad parameters are valid
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid
External supply voltage for main XTAL/Oscillator[3]	$V_{DDEXTOSC}$ *SR*	4.5	5.0	5.5[2]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid. 5V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
Supply voltage for non-volatile memory	$V_{DDP3NVM}$ *SR*	2.97	3.3	3.63	V	
External supply voltage for PMS, standby domains, standby pins and SCR	$V_{DDEVRSB}$ *SR*	2.97[4]	-	5.5[2]	V	

(table continues...)

Table 31 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for ADC modules and ANx analog and class S input pins with respect to VSSM	V_{DDM} *SR*	4.5	5.0	5.5[2]	V	Nominal ADC supply voltage range. ADC 5 V parameters are valid
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. Degraded ADC parameters are valid (see TMADC 5V chapter)
		2.97	3.3	3.63	V	Nominal ADC supply voltage range. Degraded ADC parameters are valid (see TMADC 5V chapter)
External supply voltage for IO supply for Flex port	V_{DDFLEX} *SR*	4.5	5.0	5.5[2]	V	5 V pad parameters are valid
		2.97	3.3	3.63	V	3.3 V pad parameters are valid
External supply voltage for HSPHY module[5]	$V_{DDPHPHYx}$ *SR*	1.62	1.8	1.98[6]	V	
Supply Voltage for core logic (V_{DD}) at unloaded supply pin.[7]	V_{DD} *SR*	0.943[8]	1.025	1.128[9]	V	V_{DD} (VID_CON.VDDNOM) setpoint value for slow and typical devices. V_{DD} setpoint value, if no voltage scaling possible (e.g. in case of fixed external supply voltage)
		0.897[8]	0.975	1.073[9]	V	V_{DD} (VID_CON.VDDNOM) setpoint value for fast devices
Supply Voltage for HSPHY core logic (V_{DDPHYx}) at unloaded supply pin	V_{DDPHYx} *SR*	0.943	1.025	1.107[9]	V	V_{DDPHYx} (VID_CON.VDDNOM) setpoint value for slow and typical devices. V_{DDPHYx} setpoint value, if no voltage scaling possible (e.g. in case of fixed external supply voltage)
		0.897	0.975	1.053[9]	V	V_{DDPHYx} (VID_CON.VDDNOM) setpoint value for fast devices
Core ground supply	V_{SS} *SR*	0	-	-	V	
Analog ground supply V_{SSM}	V_{SSM} *CC*	-0.1	0	0.1	V	
Minimum external voltage to ensure defined pad states for $V_{DDEVRSB}$ supplied pins	V_{DDPPSB} *CC*	2.4[10]	-	-	V	Default pad pull-up or tristate is ensured at respective $V_{DDEVRSB}$ supply level
Minimum external voltage to ensure defined pad states for V_{DDEXT} supplied pins	V_{DDPPA} *CC*	2.4[10]	-	-	V	Default pad pull-up or tristate is ensured at respective V_{DDEXT} supply level

1) $V_{DDEXTDC}$ supply voltage is allowed to drop down to 2.8 V during device start-up cranking phase.
2) Voltage overshoot up to 6.5 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
3) $V_{DDEXTOSC}$ and V_{DDEXT} shall be supplied from the same regulator source
4) $V_{DDEVRSB}$ supply voltage is allowed to drop down to 2.6 V during device start-up and standby mode.

5) If at least one HSPHYx module is used, all VDDPHPHYx and VDDPHYx supply rails in the device shall be supplied complying to operating range limits.
6) Voltage overshoot up to 2.4 V is permissible, provided that the duration is less than 2 h cumulated.
7) The V_{DD} voltage on the loaded VDD ball would be higher than that on the internal sense point indicated by the unloaded VDD_SENSE pin with respect to unloaded VSS_SENSE ball. The difference is attributed to the static and dynamic core voltage drop on the power distribution network. The loaded V_{DD} voltage is indicated by VDDPAD monitor and unloaded V_{DD} internal voltage is indicated by the VDD monitor respectively. It is expected that the external regulator static + dynamic voltage undershoot at unloaded VDD_SENSE point is limited to V_{DD} (Typ) - 6% as is documented in the max pattern current consumption use case to have adequate headroom for voltage monitoring and margin towards reset (VDDPRIUV limit).
8) For VDD VDDPRIUV (MIN) ≤ VDD < VDD (MIN) core logic operation is validated for patterns without additional load jumps to ensure device start-up. Analog performance of ADCs or HSPHYx are not being guaranteed. Operation at rated frequency is ensured in production test down to VDD VDDPRIUV reset limit at VDD sense point.
9) Voltage overshoot up to 1.2 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
10) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when V_{DDEXT} or $V_{DDEVRSB}$ has reached this level.

Related information

Clock operating conditions on page 206
Limitation of supply voltage over time on page 210
Temperature operating conditions on page 211
Example temperature profiles on page 211

4.4.3 Limitation of supply voltage over time

The maximum operation voltage for $V_{DDEXT/DDM}$ supply rails is limited over the complete lifetime.

***Note**: The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 32 Example voltage profile 1

$V_{DDEXT/DDM}$	Duration [h]
5.4 V < $V_{DDEXT/DDM}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{DDEXT/DDM}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{DDEXT/DDM}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{DDEXT/DDM}$ ≤ 4.85 V	≤ 15% of lifetime
4.5 V < $V_{DDEXT/DDM}$ ≤ 4.6 V	≤ 5% of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

***Note**: The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 33 Example voltage profile 2

V_{DD}	Duration [h]
$V_{DD, typ}$ - 3 % of $V_{DD, typ}$ < V_{DD} ≤ $V_{DD, typ}$ + 3 % of $V_{DD, typ}$	≤ 90% of lifetime

(table continues...)

Table 33 (continued) Example voltage profile 2

V_{DD}	Duration [h]
Operating $V_{DD, min} < V_{DD} \leq V_{DD, typ}$ - 3 % of $V_{DD, typ}$ AND $V_{DD, typ}$ + 3 % of $V_{DD, typ} < V_{DD} \leq$ Operating $V_{DD, max}$	≤ 10% of lifetime
Operating $V_{DD, max} < V_{DD} \leq$ Absolute maximum $V_{DD, max}$	as documented in absolute maximum ratings section.

Related information

Clock operating conditions on page 206
Supply operating conditions on page 207
Temperature operating conditions on page 211
Example temperature profiles on page 211

4.4.4 Temperature operating conditions

Table 34 Temperature operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A *SR*	-40	-	125	°C	valid for all SAK products
Junction Temperature	T_J *SR*	-40	-	160	°C	valid for all SAK products

Related information

Clock operating conditions on page 206
Supply operating conditions on page 207
Limitation of supply voltage over time on page 210
Example temperature profiles on page 211

4.4.5 Example temperature profiles

The maximum operating junction temperature T_J is limited over the complete lifetime.

***Note**: The following temperature profiles are provided as a reference distribution across the lifetime of the product. Application specific temperature profiles shall be separately aligned through Infineon customer support team and approved by Infineon Technologies towards fulfillment of the respective quality and reliability targets.*

Table 35 Standard temperature profile reference

Junction temperature T_J (°C)	Duration (*hours*)	Comments
≤ 160	300	Device in Operation in RUN mode
≤ 150	600	Device in Operation in RUN mode
≤ 145	1000	Device in Operation in RUN mode
≤ 140	1000	Device in Operation in RUN mode
≤ 135	1000	Device in Operation in RUN mode

(table continues...)

Table 35 (continued) Standard temperature profile reference

Junction temperature T_J (°C)	Duration (*hours*)	Comments
≤ 130	1200	Device in Operation in RUN mode
≤ 125	3000	Device in Operation in RUN mode
≤ 120	5000	Device in Operation in RUN mode
≤ 115	5000	Device in Operation in RUN mode
≤ 110	5000	Device in Operation in RUN mode
≤ 105	1000	Device in Operation in RUN mode
≤ 100	400	Device in Operation in RUN mode
	24500	Total operational lifetime
≤ 40	151000	Total non-operational lifetime Device in Standby 0 mode or is switched off

Table 36 Extended temperature profile reference

Junction temperature T_J (°C)	Duration (*hours*)	Comments
≤ 150	300	Device in Operation in RUN mode
≤ 140	600	Device in Operation in RUN mode
≤ 130	1000	Device in Operation in RUN mode
≤ 120	1800	Device in Operation in RUN mode
≤ 110	20000	Device in Operation in RUN mode
≤ 105	12300	Device in Operation in RUN mode
≤ 85	3000	Device in Operation in RUN mode
≤ 40	500	Device in Operation in RUN mode
≤ -40	500	Device in Operation in RUN mode
≤ 90	30000	Device in Operation in RUN mode (reduced performance)
≤ 85	30000	Device in Operation in RUN mode (reduced performance)
	100000	Total operational lifetime
≤ 40	75500	Total non-operational lifetime Device in Standby 0 mode or is switched off

Related information

Clock operating conditions on page 206
Supply operating conditions on page 207
Limitation of supply voltage over time on page 210
Temperature operating conditions on page 211
Pin reliability in overload on page 204
Quality declarations on page 332

4.5 Switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.1 ¬ PORST Pad characteristics

Table 37 ¬ PORST Pad characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PORST pad output current[1]	I_{PORST} *CC*	13	-	-	mA	V_{DDEXT} = 2.97 V; V_{PORST} = 0.9 V
Spike filter always blocked pulse duration	t_{SF1} *CC*	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} *CC*	263	-	-	ns	Without additional PORST Digtial Filter active (PORSTDF = 0)
Input high voltage level	V_{IH} *SR*	2.0	-	-	V	TTL; V_{DDEXT} = 2.97 V
		2.0	-	-	V	TTL; V_{DDEXT} = 4.5 V
Input low voltage level	V_{IL} *SR*	-	-	0.8	V	TTL; V_{DDEXT} = 2.97 V
		-	-	0.8	V	TTL; V_{DDEXT} = 4.5 V
Input hysteresis[2]	*HYS CC*	0.026 * V_{DDEXT}	-	-	V	None of the neighbour pads are used as output
Pull-down current[3] [1]	I_{PDL} *CC*	|15|	-	-	μA	V_{IL}; V_{DDEXT} = 2.97 V
		-	-	|130|	μA	V_{IH}; TTL
Input leakage current	I_{OZ} *CC*	-1000	-	1000	nA	$T_J \leq$ 150°C ; (0.1 * V_{DDEXT}) < V_{IN} < (0.9 * V_{DDEXT})
		-1050	-	1050	nA	$T_J \leq$ 150°C ; else
		-1100	-	1100	nA	$T_J \leq T_J$ (Max); (0.1 * V_{DDEXT}) < V_{IN} < (0.9 * V_{DDEXT})
		-1150	-	1150	nA	$T_J \leq T_J$ (Max); else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added

1) It is recommended that PORST pin shall be externally pulled high with a pull-up resistor in the range 1.4 kΩ up to 6.4 kΩ.
2) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

4.5.2 5 V switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.2.1 Fast 5V GPIO characteristics

Table 38 Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output parameters						
On-Resistance of pad output	R_{DSON} *CC*	65	225	295	Ohm	Driver = medium; $I_{OH / OL}$ = 2 mA
		31	55	80	Ohm	Driver = strong; $I_{OH / OL}$ = 8 mA [1)]

(table continues...)

Table 38 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise / Fall time	t_{RF} *CC*	1.6	-	4.5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}
		-	-	5.5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		4+0.55* C_L	4+0.75* C_L	12+1.1* C_L	ns	Driver = medium; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		2 + 0.57 * C_L	11 + 0.95 * C_L	20 + 1.35 * C_L	ns	Driver = medium, edge = medium; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		1.0+0.18 *C_L	2.5+0.27 *C_L	5.0+0.37 *C_L	ns	Driver = strong, edge = medium; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		1.5 + 0.18 * C_L	1.5 + 0.28 * C_L	10 + 0.4 * C_L	ns	Driver = strong, edge = medium; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		0.5+0.08 *C_L	0.5+0.11 *C_L	3.0+0.14 *C_L	ns	Driver = strong, edge = sharp; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}; else
		0.75 + 0.08 * C_L	0.75 + 0.11 * C_L	4 + 0.20 * C_L	ns	Driver = strong, edge = sharp; $C_L \leq$ 200 pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0

(table continues...)

Table 38 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Asymmetry of sending[2)]	t_{TX_ASYM} *CC*	-1	-	1	ns	C_L = 15 pF; driver = strong, edge = medium and driver = medium; valid for all data rates excluding clock tolerance
		-1.3	-	1.3	ns	C_L = 15 pF; driver = strong, edge = medium and driver = medium; valid for all data rates excluding clock tolerance; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Input parameters						
Input frequency	f_{IN} *CC*	-	-	160	MHz	
		-	-	40	MHz	Valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		0.76 * V_{DDIO}	-	-	V	AL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDIO}	V	AL
		-	-	0.32 * V_{DDIO}	V	AL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-95	-	95	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL

(table continues...)

Table 38 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input hysteresis[3]	*HYS CC*	0.09 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		0.065 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		210[4]	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[5]	I_{PUH} *CC*	|30|	-	-	µA	V_{IH}; AL or TTL
		|27|	-	-	µA	V_{IH}; AL or TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	|130|	µA	V_{IL}; AL or TTL
Equivalent resistance to pull-up device	R_{PUH} *CC*	30	-	42	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; Automotive level
		56	-	78	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; TTL level
Pull-down current[6]	I_{PDL} *CC*	|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
		|25|	-	-	µA	V_{IL}; TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	|130|	µA	V_{IH}; AL or TTL
Equivalent resistance to pull-down device	R_{PDL} *CC*	43	-	58	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; Automotive level
		18	-	25	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; TTL level

(table continues...)

Table 38 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} *CC*	-3900	-	3900	nA	$T_J \leq 150°C$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-4800	-	4800	nA	$T_J \leq 150°C$; else
		-4100	-	4100	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-5100	-	5100	nA	$T_J \leq T_J$ (Max); else
		-3700	-	3700	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_RX / Fast pad type
		-13000	-	13000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3900	-	3900	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_RX / Fast pad type
		-14500	-	14500	nA	$T_J \leq T_J$ (Max); LVDS_RX / Fast pad type; else
		-4600	-	4600	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_TX / Fast pad type
		-5800	-	5800	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-4800	-	4800	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; LVDS_TX / Fast pad type
		-6100	-	6100	nA	$T_J \leq T_J$ (Max); LVDS_TX / Fast pad type; else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
		-	2	3.5	pF	LVDS_RX pads; In addition 2.5 pF from package to be added
		-	2	4.2	pF	LVDS_TX pads; In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) The 8 mA condition is an Infineon internal test condition and not allowed as DC (or permanent) load on this standard pad.

2) This parameter defines the difference of the output signal delay parameter for rising and falling edge

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) For Pin P01.14 the Min value is 165 mV.
5) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
6) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Slow 5V GPIO characteristics on page 219
Class S 5V characteristics on page 222

4.5.2.2 Slow 5V GPIO characteristics

Table 39 Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output parameters						
On-Resistance of pad output	R_{DSON} CC	100	225	295	Ohm	Driver = medium; $I_{OH / OL}$ = 2 mA
Rise / Fall time[1]	t_{RF} CC	4+0.55* C_L	4+0.75* C_L	12+1*C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		4 + 0.55 * C_L	12 + 0.95 * C_L	20 + 1.35 * C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10% to 90% of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		1.5+0.25 *C_L	2.5+0.40 *C_L	7+0.55* C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		1.5+0.25 *C_L	2.5+0.40 *C_L	9+0.80* C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Asymmetry of sending[2]	t_{TX_ASYM} CC	-1.5	-	1.5	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input parameters						
Input frequency	f_{IN} CC	-	-	160	MHz	
		-	-	40	MHz	Valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0

(table continues...)

Table 39 **(continued) Slow 5V GPIO characteristics**

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		0.76 * V_{DDIO}	-	-	V	AL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDIO}	V	AL
		-	-	0.32 * V_{DDIO}	V	AL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-100	-	100	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.09 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.058 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		0.065 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		210	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[4)]	I_{PUH} *CC*	|30|	-	-	μA	V_{IH}; AL or TTL
		|27|	-	-	μA	V_{IH}; AL or TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	|130|	μA	V_{IL}; AL or TTL

(table continues...)

Table 39 (continued) Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-down current[5]	I_{PDL} *CC*	|30|	-	-	μA	V_{IL}; AL
		|28|	-	-	μA	V_{IL}; TTL
		|25|	-	-	μA	V_{IL}; TTL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	|130|	μA	V_{IH}; AL or TTL
Input leakage current	I_{OZ} *CC*	-1700	-	1700	nA	$T_J \leq 150°C$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-2000	-	2000	nA	$T_J \leq 150°C$; no analog input; else
		-1900	-	1900	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-2200	-	2200	nA	$T_J \leq T_J$ (Max); no analog input; else
		-2800	-	2800	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-3300[6]	-	3300[6]	nA	$T_J \leq 150°C$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
		-2900	-	2900	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-3500	-	3500	nA	$T_J \leq T_J$ (Max); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.
6) For $(V_{IN} > V_{DDM})$ or $(V_{IN} < V_{SSM})$ leakage is doubled.

Related information

Fast 5V GPIO characteristics on page 214
Class S 5V characteristics on page 222

4.5.2.3 Class S 5V characteristics

Table 40 Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDM}	-	-	V	AL
		0.76 * V_{DDM}	-	-	V	AL; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis[1)]	*HYS CC*	0.09 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		290	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[2)]	I_{PUH} *CC*	|30|	-	-	μA	V_{IH}; AL and TTL
		-	-	|130|	μA	V_{IL}; AL and TTL
Pull-down current[3)]	I_{PDL} *CC*	|30|	-	-	μA	V_{IL}; AL
		|28|	-	-	μA	V_{IL}; TTL
		-	-	|130|	μA	V_{IH}; AL and TTL
Input leakage current	I_{OZ} *CC*	-900	-	900	nA	$T_J \leq 150°C$; PDD option available
		-400	-	400	nA	$T_J \leq 150°C$; else
		-1100	-	1100	nA	$T_J \leq T_J$ (Max); PDD option available
		-500	-	500	nA	$T_J \leq T_J$ (Max); else

(table continues...)

Table 40 (continued) Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Fast 5V GPIO characteristics on page 214
Slow 5V GPIO characteristics on page 219

4.5.3 3.3 V switchable pad characteristics

Pad classes as Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.3.1 Fast 3.3V GPIO characteristics

Table 41 Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output parameters						
On-Resistance of pad output	R_{DSON} *CC*	65	225	295	Ohm	Driver = medium; $I_{OH / OL}$ = 2 mA
		31	55	80	Ohm	Driver = strong; $I_{OH / OL}$ = 8 mA 1)

(table continues...)

Table 41 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise / Fall time[2)]	t_{RF} *CC*	1.6	-	4.5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}
		-	-	5.3	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		2+0.5*C_L	5.5+0.75*C_L	10+1.25*C_L	ns	Driver = medium; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		2+0.5*C_L	10+0.6*C_L	18+1.15*C_L	ns	Driver = medium, edge = medium; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		1.5+0.18*C_L	1.5+0.28*C_L	8+0.43*C_L	ns	Driver = strong, edge = medium; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		0.75+0.08*C_L	0.75+0.11*C_L	2.5+0.21*C_L	ns	Driver = strong, edge = sharp; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		0.75+0.08*C_L	2+0.14*C_L	3.5+0.2*C_L	ns	Driver = strong, edge = sharp; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		-	-	5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 0.8 V to 2.0 V (RMII)

(table continues...)

Table 41 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Asymmetry of sending[3)]	t_{TX_ASYM} *CC*	-1	-	1	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
		-1.3	-	1.3	ns	C_L = 15 pF; driver = strong , edge = medium and driver = medium; valid for all data rates excluding clock tolerance; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Input parameters						
Input frequency	f_{IN} *CC*	-	-	160	MHz	
		-	-	40	MHz	Valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.40 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[4)]	*HYS CC*	0.055 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.081 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[5)]	I_{PUH} *CC*	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL
Pull-down current[6)]	I_{PDL} *CC*	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL

(table continues...)

Table 41 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-2300	-	2300	nA	$T_J \leq 150°C$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-2700	-	2700	nA	$T_J \leq 150°C$; else
		-2500	-	2500	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-2900	-	2900	nA	$T_J \leq T_J$ (Max); else
		-1800	-	1800	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_RX / Fast pad type
		-8000	-	8000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type; else
		-2000	-	2000	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_RX / Fast pad type
		-9000	-	9000	nA	$T_J \leq T_J$ (Max); LVDS_RX / Fast pad type; else
		-2800	-	2800	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_TX / Fast pad type
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-3000	-	3000	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/DDEXTHS})$; LVDS_TX / Fast pad type
		-3500	-	3500	nA	$T_J \leq T_J$ (Max); LVDS_TX / Fast pad type; else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) The 8 mA condition is an Infineon internal test condition and not allowed as DC (or permanent) load on this standard pad.
2) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
3) This parameter defines the difference of the output signal delay parameter for rising and falling edge
4) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise
5) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
6) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Slow 3.3V GPIO characteristics on page 227
Class S 3.3V characteristics on page 230

4.5.3.2 Slow 3.3V GPIO characteristics

Table 42 Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output parameters						
On-Resistance of pad output	R_{DSON} *CC*	125	225	320	Ohm	Driver = medium; $I_{OH / OL}$ = 2 mA
Rise / Fall time[1]	t_{RF} *CC*	2+0.5*C_L	5.5+0.75 *C_L	10+1.25 *C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		2+0.5*C_L	8+0.85* C_L	14+1.25 *C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
		2+0.30* C_L	3.5+0.50 *C_L	5+0.70* C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		2+0.3*C_L	5+0.5*C_L	8+0.7*C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}; valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Asymmetry of sending[2]	t_{TX_ASYM} *CC*	-1.3	-	1.3	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input parameters						
Input frequency	f_{IN} *CC*	-	-	160	MHz	
		-	-	40	MHz	Valid only for STANDBY0 and STANDBY1 mode if bit SCUSCR_PMS1IVRCON.PADPDIS = 0
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL

(table continues...)

Table 42 (continued) Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3]	*HYS CC*	0.055 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.081 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[4]	I_{PUH} *CC*	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL
Pull-down current[5]	I_{PDL} *CC*	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL

(table continues...)

Table 42 (continued) Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-1200	-	1200	nA	$T_J \leq 150°C$; no analog input; else
		-1200	-	1200	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-1300	-	1300	nA	$T_J \leq T_J$ (Max); no analog input; else
		-1700	-	1700	nA	$T_J \leq 150°C$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-1800[6]	-	1800[6]	nA	$T_J \leq 150°C$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
		-1800	-	1800	nA	$T_J \leq T_J$ (Max); $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-2000	-	2000	nA	$T_J \leq T_J$ (Max); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.
6) For $(V_{IN} > V_{DDM})$ or $(V_{IN} < V_{SSM})$ leakage is doubled.

Related information

Fast 3.3V GPIO characteristics on page 223
Class S 3.3V characteristics on page 230

4.5.3.3 Class S 3.3V characteristics

Table 43 Class S 3.3V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis[1]	*HYS CC*	0.055 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.085 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
Pull-up current[2]	I_{PUH} *CC*	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL
Pull-down current[3]	I_{PDL} *CC*	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL
Input leakage current	I_{OZ} *CC*	-700	-	700	nA	$T_J \leq 150°C$; PDD option available
		-400	-	400	nA	$T_J \leq 150°C$; else
		-800	-	800	nA	$T_J \leq T_J$ (Max); PDD option available
		-500	-	500	nA	$T_J \leq T_J$ (Max); else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Fast 3.3V GPIO characteristics on page 223
Slow 3.3V GPIO characteristics on page 227

4.5.4 Class D characteristics

Table 44 Class D characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} *CC*	-1000	-	1000	nA	$T_J \leq 150°C$; PDD option available
		-800	-	800	nA	$T_J \leq 150°C$; valid for AN9, AN10, AN34, AN35, AN57
		-100	-	100	nA	$T_J \leq 150°C$; else
		-1100	-	1100	nA	$T_J \leq T_J$ (Max); PDD option available
		-900	-	900	nA	$T_J \leq T_J$ (Max); valid for AN9, AN10, AN34, AN35, AN57
		-110	-	110	nA	$T_J \leq T_J$ (Max); else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added

4.5.5 ADC reference pads characteristics

Table 45 ADC reference pads characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} *CC*	-4 [1)]	-	4 [1)]	μA	$T_J \leq T_J$ (Max); $V_{AREF} \leq V_{DDM}$; used for TMADC and FCC (if available); valid for BGA292
		-14 [1)]	-	14 [1)]	μA	$T_J \leq T_J$ (Max); $V_{AREF} \leq V_{DDM}$ + 50 mV; used for TMADC and FCC (if available); valid for BGA292
		-4 [2)]	-	4 [2)]	μA	$T_J \leq T_J$ (Max); $V_{AREF} \leq V_{DDM}$; used for DSADC; valid for BGA436 & BGA292
		-12 [2)]	-	12 [2)]	μA	$T_J \leq T_J$ (Max); $V_{AREF} \leq V_{DDM}$ + 50 mV; used for DSADC; valid for BGA436 & BGA292

1) Limit is valid for VAREF2 pin.
2) Limit is valid for VAREF1 pin and used for DSADC.

4.5.6 Driver mode selection for slow and fast pads

Table 46 Driver mode selection for Slow pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium edge (m)

Table 47 Driver mode selection for Fast pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium edge (m)
X	1	1	Speed grade 4	Reserved. ***Note**: Do not use this combination!*

4.6 High performance LVDS pad characteristic

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC48x STD. It is composed out of an LVDS pad and a fast pad.

C_L = 2.5 pF for all LVDS parameters.

***Note**: Driver ground potential difference is defined as driver-receiver potential difference, that can result in a voltage shift when comparing the driver output voltage level and the receiver input voltage level of a transmitted signal.*

***Note**: R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represented in either by R_{IN} or by R_T = 100Ω but not both.*

***Note**: Default after start-up = CMOS function*

4.6.1 LVDS - IEEE standard LVDS general purpose link (GPL)

Table 48 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Driver dc characteristics						
Output voltage high	V_{oh} *CC*	-	-	1475	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00 and 01
		-	-	1500	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10 and 11
Output voltage low	V_{ol} *CC*	925	-	-	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00 and 01
		900	-	-	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10 and 11
Output differential voltage	V_{od} *CC*	380	-	500	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 11; Multi slave operation
		240	-	330	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00
		280	-	370	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 01
		320	-	410	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10
Output differential voltage in Sleep Mode[1)]	V_{ODSM} *CC*	-5	-	20	mV	R_T = 100 Ohm ± 20%; LPCRx.VDIFFADJ = xx
Output offset (Common mode) voltage	V_{os} *CC*	1125	-	1275	mV	R_T = 100 Ohm ± 1%
Output impedance	R_o *CC*	40	-	140	Ohm	
Delta output impedance	dR_o *SR*	-	-	10	%	

(table continues...)

Table 48 (continued) LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Change in V_{OD} between 0 and 1	dV_{od} *CC*	-	-	25	mV	R_T = 100 Ohm ± 1%
Change in V_{OS} between 0 and 1	dV_{os} *CC*	-	-	25	mV	R_T = 100 Ohm ± 1%
Driver ac characteristics						
Duty cycle	t_{duty} *CC*	45	-	55	%	
Fall time (20% - 80%)	t_{fall20} *CC*	-	-	0.75[2)]	ns	Z_L = 100 Ohm ± 20% at 2 pF external load
Rise time (20% - 80%)	t_{rise20} *CC*	-	-	0.75[3)]	ns	Z_L = 100 Ohm ± 20% at 2 pF external load
Receiver dc characteristics						
Input voltage range	V_i *SR*	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ± 10%
		0	-	2000	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ± 20%
Input differential threshold	V_{idth} *SR*	-100	-	100	mV	Driver ground potential difference < 925 mV
Receiver ac characteristics						
Pad setup time	t_{SET_LVDS} *CC*	-	10	13	µs	

1) Common Mode voltage of TX is maintained
2) t_{fall20} = 0.75 ns + (C_L - 2)[pF]*20 ps. C_L defines the external load.
3) t_{rise20} = 0.75 ns + (C_L - 2)[pF]*20 ps. C_L defines the external load.

Related information

LVDS pad input model on page 235

4.6.2 LVDS pad input model

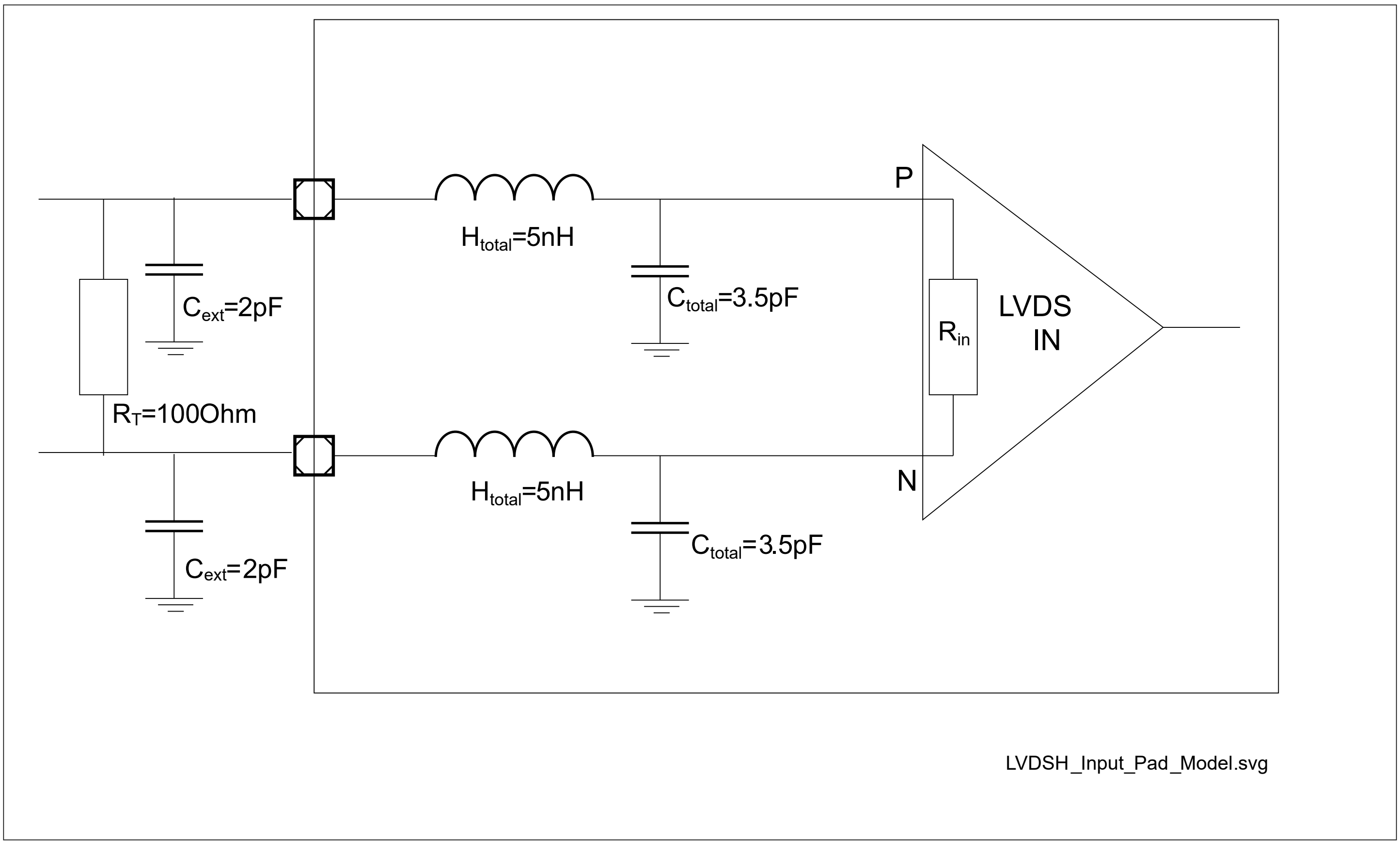


Figure 3 **LVDS pad input model**

Related information

LVDS - IEEE standard LVDS general purpose link (GPL) on page 233

4.7 TMADC characteristics

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of (V_{AREF} - V_{AGND}) ≥ 4.5 V.

If the reference voltage range is below 4.5 V, for example 3.3 V, the accuracy parameter values increase by a factor of 1.1 / k, where k = 3.3 V / 4.5 V. If TUE is specified with ±4 LSB_{12} at 4.5 V the corresponding value at 3.3 V will be: 4 LSB_{12} × (1.1 × 4.5 V / 3.3 V) = 6 LSB_{12} → ±6 LSB_{12}.

***Note**: Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).*

***Note**: Digital functions overlapping analog inputs influence accuracy.*

***Note**: The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and EN_{RMS} = 1.0 LSB the additional peak-peak noise error is ±(4 × 1.0) = 8 LSB_{12}.*

4.7.1 TMADC 5V characteristics

Table 49 TMADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC internal regulator characteristics						
TMADC IVR output voltage	V_{DDK} *CC*	-	2.4	-	V	
Deviation of IVR output voltage V_{DDK}	dV_{DDK} *CC*	-2.0	-	2.0	%	Based on device-specific value
TMADC reference voltage characteristics						
Analog reference voltage	V_{AREF} *SR*	V_{DDM} - 0.1	V_{DDM}	V_{DDM} + 0.05[1]	V	2.97 V ≤ V_{DDM} ≤ 5.5 V
Negative reference voltage[2]	V_{AGND} *SR*	V_{SSM} - 0.05	V_{SSM}	V_{SSM} + 0.05	V	V_{SSM} and V_{AGND} are connected together
Reference input charge consumption per conversion (from V_{AREF})[3]	Q_{CONV} *CC*	-	-	10	pC	
TMADC accuracy						
Total Unadjusted Error[4) 5) 6) 7) 8) 9)]	*TUE CC*	-4	-	4	LSB	12-bit resolution DC input; 4.5 V ≤ V_{DDM} ≤ 5.5 V
Integral Non-linearity[4) 5) 8)]	EA_{INL} *CC*	-3	-	3	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Differential Non-linearity[4) 5) 10) 8)]	EA_{DNL} *CC*	-1	-	2	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Gain error[4) 5) 8) 9)]	EA_{GAIN} *CC*	-4	-	4	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Offset[4) 5) 6) 8)]	EA_{OFF} *CC*	-4	-	4	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
RMS Noise[4) 5) 6) 11) 12) 7)]	EN_{RMS} *CC*	-	0.5	1.2	LSB	12bit resolution DC input

(table continues...)

Table 49 (continued) TMADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC input characteristics						
Analog input voltage range	V_{AIN} *SR*	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Analog input charge consumption[13)]	Q_{AINS} *CC*	-	-	6.0	pC	
Input leakage when channel is enabled[13)]	$I_{LEAKCHEN}$ *CC*	-	-	150	nA	
Input leakage when channel is disabled[13)]	$I_{LEAKCHDIS}$ *CC*	-	-	150	nA	
TMADC timing						
Converter reference clock[14)]	f_{ADCI} *SR*	80	-	80	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		40	-	40	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Conversion time (excluding sample and hold time)	t_{CONV} *CC*	16	-	16	cycles	Measured between two conversion start-points, thus these numbers are valid for pipelined conversions [15)]
Sampling time[16)]	t_{mstc} *SR*	50	-	-	ns	Valid for the continous conversion mode; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		100	-	-	ns	Valid for the continous conversion mode; 2.97 V ≤ V_{DDM} < 4.5 V
		100	-	-	ns	Valid for a single conversion; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		200	-	-	ns	Valid for a single conversion; 2.97 V ≤ V_{DDM} < 4.5 V
Sampling time monitor channel	t_{mmstc} *SR*	1	-	-	µs	
Calibration time	t_{CAL} *CC*	-	-	3	ms	Valid for power up calibration and recalibration; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	6	ms	Valid for power up calibration and recalibration; 2.97 V ≤ V_{DDM} < 4.5 V
Hold Time for pending Sample	t_{HOLD} *SR*	-	-	3	µs	4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	6	µs	2.97 V ≤ V_{DDM} < 4.5 V

(table continues...)

Table 49 (continued) TMADC 5V characteristics

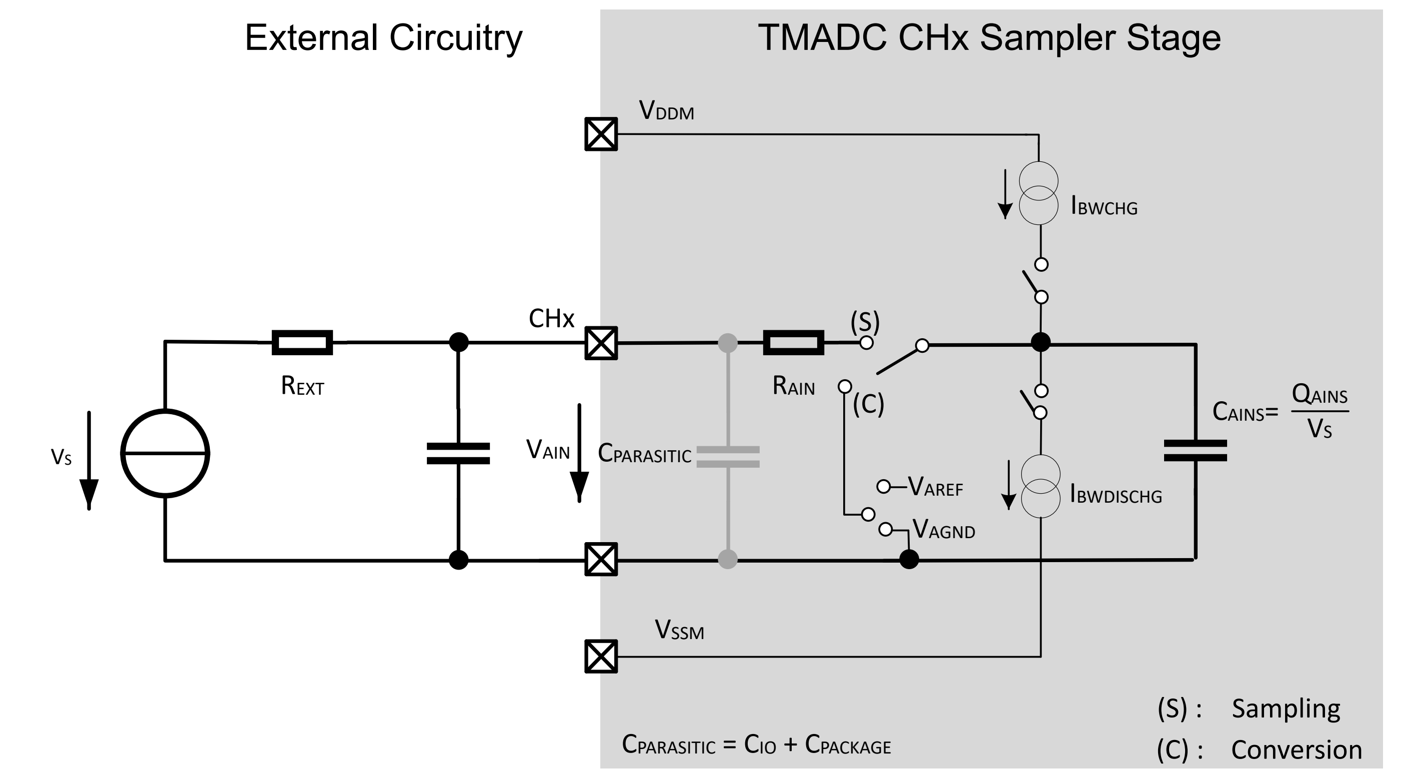
Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Wakeup time	t_{WUDIS} *CC*	-	-	20	µs	From module disable state (MODCFG.RUN set from zero to one); 4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	20	µs	From module disable state (MODCFG.RUN set from zero to one); 2.97 V ≤ V_{DDM} < 4.5 V
TMADC diagnosis characteristics						
Converter diagnostics voltage accuracy	dV_{CSD} *CC*	-1	-	1	%	Referred to V_{DDM}
Resistance of the pull-down test device[17)]	R_{PDD} *CC*	-	-	0.3	kOhm	Measured at pad input voltage V_{IN} = V_{DDM} / 2
Broken wire detection charge current	I_{BWCHG} *CC*	5	10	15	µA	
Broken wire detection discharge current	$I_{BWDISCHG}$ *CC*	5	10	15	µA	

1) For V_{DDM} = 5.5 V the valid Max. value is 5.5 V
2) VAGND shall be directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
3) Parameter is valid for the typical value of V_{AREF}-V_{AGND}. If a reduced V_{AREF}-V_{AGND} voltage is used this parameter will decrease linearly.
4) This parameter is valid for V_{AREF}-V_{AGND} equal or higher than the typical value * 0.9. If a reduced V_{AREF}-V_{AGND} voltage is used this parameter can increase. If V_{AREF}-V_{AGND} is reduced with the factor k (k is the quotient built out of the reduced reference voltage and the 4.5 V), the parameter will increase with 1.1/k. e.g., k = 3.3 V/4.5 V = 0.73 → 1.1/k = 1.5 → 1.5 * TUE: 6 LSB at 3.3 V reference
5) This parameter is only guaranteed with a maximum supply voltage ripple on VDDM / VSSM of 20 mVpp in a frequency band from 1 kHz to 10 MHz. Supply voltage ripples above 10 MHz must be smaller than 5 mV. This must be guaranteed by high quality power supply sources and proper blocking capacitors
6) This parameter is valid for analog inputs within Pads not sharing digital functions. Parameter for analog inputs sharing digital functions (pad type Slow and Fast) will increase by 3 LSB
7) Resulting worst case combined error is arithmetic combination of *TUE* and user-defined distribution of EN_{RMS}
8) Start-up calibration is a prerequisite to achieve TMADC accuracy specification. It needs to be repeated when channel to SAR-core mapping is changed. Refer to user manual TMADC chapter "Module start-up calibration" for details.
9) For extended range (Input Voltage > 80% FS) error will increase by 1 LSB
10) Monotonic characteristic, no missing codes (after calibration)
11) Only valid if VAGND is directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
12) The value is derived from a 1 sigma distribution
13) The specified value does not include the pin leakage current I_{OZ}. I_{OZ} has to be added to get the total current value.
14) This is the operating frequency of TMADC selectable by the bit 'TMADC supply level' (SUPLLEV.TMADCSUP)
15) f_{ADCI} clock cycles
16) Sampling time is a configurable parameter (see details in the user manual)
17) Enabling of the pull down test device is only allowed in PWM operation with a duty cycle of ≤ 50% and a frequency of 1 kHz

Related information

TMADC input structure figure on page 239

4.7.2 TMADC input structure figure



Q_{AINS} : Analog input charge

R_{AIN} : Analog input switch resistance → ($t_{mstc(Min)}$/C_{AINS})/10, where $t_{mstc(Min)}$ is either 50ns (5V) or 100ns (3.3V)

I_{BWCHG} : Broken wire detection charge current

$I_{BWDISCHG}$: Broken wire detection discharge current

Figure 4 **Equivalent Circuitry for Analog Inputs**

Related information

TMADC 5V characteristics on page 236

4.8 DSADC characteristics

The DSADC parameters describe the product properties and do not include external circuitry.

They are only valid for a voltage range 4.5 V ≤ V_{DDM} ≤ 5.5 V and junction temperatures T_J ≤ 150 °C if not defined explicitly.

The signal-noise ratio (SNR) is specified for differential inputs. For single ended operation and for quasi-differential mode (i.e. using VCM) the resulting signal-noise ratio is reduced by 6 dB.

4.8.1 DSADC 5V characteristics

Table 50 DSADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DSADC reference voltage requirements						
Positive reference voltage	V_{AREF} *SR*	V_{DDM} - 0.1	V_{DDM}	V_{DDM} + 0.05[1]	V	
Reference ground voltage[2]	V_{AGND} *SR*	V_{SSM} - 0.05	V_{SSM}	V_{SSM} + 0.05	V	V_{SSM} and V_{AGND} are connected together
DSADC accuracy						
Common mode voltage accuracy[3]	dV_{CM} *CC*	-2	-	2	%	Common mode voltage is derived from V_{DDM}. Accuracy mismatch between V_{AREF} and V_{DDM} not included.
Gain error degradation[4] [5]	ED_{GAIN} *CC*	-0.2[6]	±0.1[6]	0.2[6]	%	$T_J \leq 150°C$; Target, calibrated, V_{AREF} constant after calibration; f_{MOD} = 10 MHz
		-[6]	±0.25[6]	-[6]	%	$150°C < T_J \leq T_J$ (Max); V_{AREF} constant after calibration; f_{MOD} = 10 MHz
		-1	-	1	%	Calibrated once; f_{MOD} = 10 MHz
		-10	-	10	%	Uncalibrated; f_{MOD} = 10 MHz
DC offset error	ED_{OFF} *CC*	-5[6]	-	5[6]	mV	Calibrated; f_{MOD} = 10 MHz
		-25	-	25	mV	Calibrated once; f_{MOD} = 10 MHz
		-50	-	50	mV	Uncalibrated; f_{MOD} = 10 MHz
Signal-Noise Ratio for differential input signals	*SNR CC*	86	-	-	dB	$T_J \leq 150°C$; f_{PB} = 30 kHz; f_{MOD} = 10 MHz
		83	-	-	dB	$T_J \leq 150°C$; f_{PB} = 50 kHz; f_{MOD} = 10 MHz; dithering disabled
		67	-	-	dB	$T_J \leq 150°C$; f_{PB} = 100 kHz; f_{MOD} = 10 MHz; dithering disabled
Signal to Noise Ratio single ended mode	SNR_{se} *CC*	-	SNR-6dB	-	dB	
Signal-Noise Ratio degradation	*DSNR CC*	-	-	3	dB	150 °C < $T_J \leq T_J$ (Max); Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range	*SFDR CC*	60	-	-	dB	f_{MOD} = 10 MHz
DSADC input characteristics						
Analog input voltage range	V_{DSIN} *SR*	V_{SSM}	-	V_{AREF}	V	
Average input current[7] [8]	I_{AVG} *CC*	-6	±0.5	6	µA	Valid for f_{MOD} = 10 MHz; $T_J \leq 150°C$ [9]

(table continues...)

Table 50 (continued) DSADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Analog input leakage current[8]	I_{A_leak} *CC*	-200	-	200	nA	$T_J \leq 150°C$; for one modulator [9]
Common mode voltage bias resistance	R_{BIAS} *CC*	100	130	170	kOhm	On-chip variation ≤ ±2.5%.
Input signal bandwidth	*BW SR*	-	-	100	kHz	
Common Mode Rejection in differential mode	CMR_{DIFF} *CC*	65	-	-	dB	
DSADC timing						
On-chip modulator clock frequency	f_{MOD} *SR*	10	-	10	MHz	
DSM start-up time	t_{START} *CC*	-	-	8	µs	Time from enable till valid output bitstream; $4.5 V \leq V_{DDM} \leq 5.5 V$
Output sampling rate	f_D *CC*	9.76	-	1250	kHz	

1) For V_{DDM} = 5.5 V the valid Max. value is 5.5 V
2) VAGND shall be directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball).
3) On pins with overlaid GPIO function limits are extended by 1% (25mV) due to leakage current for T_j > 150°C
4) This parameter is valid within the defined range of f_{MOD}.
5) Gain mismatch error between the different DSADC channels is within ±0.5%.
6) Recalibration needed in case of a temperature change ΔT_j > 20°C.
7) For detailed information, refer to User Manual Chapter.
8) The specified value does not include the pin leakage current I_{OZ}. I_{OZ} has to be added to get the total current value.
9) In case T_J (Max) operating condition value is lower than 150°C, operating condition value is valid instead.

4.9 High Resolution PWM characteristics

4.9.1 HRPWM characteristics

Table 51 HRPWM characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output resolution mean[1][2]	*RES CC*	152.25	156	160.25	ps	Measurement based on output frequency variation
Peak to Peak Variation of Output Resolution	RES_{PP} *CC*	-1000	-	1000	ps	SysPLL FM modulation off; driver = strong, edge = sharp; calculated to 3σ variation [3]

1) Parameter values are valid for PWM frequencies ≤ 500 kHz
2) Parameter values are valid for 10% ≤ PWM Duty Cycle ≤ 90%
3) RMS variation of Output Resolution (1σ) can be calculated by $RES_{PP}/6$

4.10 External clock sources

OSC_XTAL is used to provide an accurate clock source for the device. It enables the connection of an external 20 MHz to 50 MHz crystals outside of the device. Ceramic resonators are also supported.

The purpose of the RTC 32 kHz oscillator is to offer a precise and power saving clock option for the device in its lower power modes like Sleep and Standby.

***Note**: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

4.10.1 OSC_XTAL characteristics

Table 52 OSC_XTAL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Oscillator frequency[1)]	f_{OSC} *SR*	20	-	50	MHz	External clock mode selected, if shaper is not bypassed
		20	-	50	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} *CC*	-	-	3[2)]	ms	Valid for above specified f_{OSC} range and 8 pF load capacitance
Input voltage at XTAL1	V_{IX} *SR*	-0.3	-	2.7	V	External crystal mode
		-0.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed
Input high voltage at XTAL1	V_{IHBX} *SR*	3.15	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC}$ = 5 V
		2.08	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC}$ = 3.3 V
Input low voltage at XTAL1	V_{ILBX} *SR*	-0.5	-	0.5	V	
Input amplitude (peak to peak) at XTAL1	V_{PPX} *SR*	1.0	-	3.0	V	External crystal mode; valid for 20 MHz ≤ f_{OSC} ≤ 50 MHz
		2.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; valid for 20 MHz ≤ f_{OSC} ≤ 50 MHz
Input current at XTAL1	I_{IX1} *CC*	-70	-	70	µA	DC input voltage sweep from 0V < V_{IN} < $V_{DDEXTOSC}$; $T_J = T_J$ (Max)
Duty cycle at XTAL1	DC_{X1} *SR*	40	-	60	%	External clock mode, if shaper is not bypassed; V_{XTAL1} = 0.5*V_{PPX}
Absolute RMS jitter at XTAL1	J_{ABSX1} *SR*	-	-	28	ps	External clock mode, if shaper is not bypassed;10 KHz to f_{OSC} / 2

(table continues...)

Table 52 (continued) OSC_XTAL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Slew rate at XTAL1	SR_{XTAL1} *SR*	0.3	-	-	V/ns	External clock mode, if shaper is not bypassed; Maximum 30% difference between rising and falling slew rate
Internal load capacitor	C_{L0} *CC*	1.0	1.2	1.4	pF	Enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} *CC*	2.1	2.3	2.5	pF	Enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} *CC*	5.4	5.9	6.4	pF	Enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} *CC*	8.1	8.7	9.3	pF	Enabled via bit OSCCON.CAP3EN
Internal load stray capacitance between XTAL1 and XTAL2	C_{XINTS} *CC*	1.15	1.20	1.25	pF	
Internal load stray capacitance between XTAL1 and ground	C_{XTAL1} *CC*	4.7	5.6	6.6	pF	

1) SGMII protocol operation via HSPHY is only possible with 25MHz or 40 MHz
2) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decreases

Related information

RTC 32 kHz oscillator characteristics on page 243

4.10.2 RTC 32 kHz oscillator characteristics

Table 53 RTC 32 kHz oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating input frequency of external crystal	f_{OSC} *CC*	-	32.768	-	kHz	The range depends on external crystal accuracy
Start-up time	T_{SU} *CC*	-	-	5	s	
Input high voltage at XTAL3	V_{IHBX} *CC*	-	-	$V_{DDEVRSB}$ + 0.5	V	
Input low voltage at XTAL3	V_{ILBX} *CC*	-0.5	-	-	V	
Oscillation amplitude at XTAL PADIN	V_{PP} *CC*	0.3	0.5	$V_{DDEVRSB}$	V	
Input hysteresis for shaper	V_{HYS} *CC*	-	50	-	mV	RTC_CON0.HYSEN = 1
Oscillator bias current	I_{bias} *CC*	0.45	0.75	1.2	µA	Lowest gain setting: RTC_CON0.GAINSEL = 01
		0.75	1.3	1.7	µA	Highest gain setting: RTC_CON0.GAINSEL = 11

(table continues...)

Table 53 **(continued) RTC 32 kHz oscillator characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total current consumption of RTC	I_{RTC} *CC*	-	3	6	µA	

Related information

OSC_XTAL characteristics on page 242

4.11 Internal clock sources

The TC48x STD provides two fully integrated clock options:

- Back-up clock
- Standby clock

The 100 MHz clock source is a precise on-chip clock. After start-up, the 100 MHz clock source has a lower accuracy (see f_{BACKUT}) and the clock source is later trimmed by the start-up software (see f_{BACKT} parameter).

The Standby clock source is used during standby mode. Its accuracy is specified by the f_{SB} and f_{SBT} parameters. This clock source is trimmed after start-up.

4.11.1 Back-up oscillator characteristics

Table 54 Back-up oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Back-up clock frequency before trimming	f_{BACKUT} CC	70	100	130	MHz	V_{DDEXT}, $V_{DDEVRSB} \geq 2.97$ V
Back-up clock frequency after trimming	f_{BACKT} CC	98	100	102	MHz	V_{DDEXT}, $V_{DDEVRSB} \geq 2.97$ V
Back-up clock fine trim LSB	$f_{BACKLSBFT}$ CC	18	-	40	kHz	

Related information

Standby oscillator characteristics on page 245

4.11.2 Standby oscillator characteristics

Table 55 Standby oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Standby clock before trimming	f_{SB} CC	30	70	110	kHz	V_{DDEXT}, $V_{DDEVRSB} \geq 2.97$ V
Standby clock after trimming	f_{SBT} CC	62	70	75	kHz	V_{DDEXT}, $V_{DDEVRSB} \geq 2.97$ V
Standby clock fine trim LSB	$f_{SBLSBFT}$ CC	1.82	2.03	2.24	kHz	LPOSCGAIN=0

Related information

Back-up oscillator characteristics on page 245

4.12 System Phase Locked Loop (SYS_PLL) characteristics

The following characteristics are valid for the System Phase Locked Loop (SYS_PLL). In order to achieve the specified performance of the module following constrains need to be considered:

***Note**: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.*

***Note**: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

4.12.1 System PLL characteristics

Table 56 System PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Modulation Amplitude	*MA CC*	0	-	2	%	
Peak Period jitter[1)]	*DP CC*	-150	-	150	ps	Without modulation (PLL output frequency); valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; peak is equal to 5 sigma RMS jitter at DCO output
Peak accumulated jitter	D_{PP} *CC*	-5	-	5	ns	Without modulation (PLL output frequency); valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Total long term jitter	J_{TOT} *CC*	-	-	10	ns	Including modulation (PLL output frequency); MA 2%; valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over at least 1000 output clock observances
PLL lock-in time	t_L *CC*	4	-	100	µs	

1) Scaling division on the measurement to be applied: sqrt (f_{DCO} / $f_{Aquired}$), at maximum 16

4.13 Peripheral Phase Locked Loop (PER_PLL) characteristics

The following characteristics are valid for the Peripheral Phase Locked Loop (PER_PLL). In order to achieve the specified performance of the module following constrains need to be considered:

***Note**: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.*

***Note**: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

4.13.1 Peripheral PLL characteristics

Table 57 Peripheral PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak Period jitter[1)]	*DP CC*	-150	-	150	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; peak is equal to 5 sigma RMS valid at DCO output
Peak accumulated jitter	D_{PPI} *CC*	-700	-	700	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Peak accumulated jitter at SYSCLK pin	D_{PP} *CC*	-1000	-	1000	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
RMS accumulated jitter	D_{RMS} *CC*	-150	-	150	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Absolute RMS jitter (PLL out)	J_{ABS20} *CC*	-92	-	92	ps	Valid for f_{REF} = 20 MHz; f_{DCO} = 800 MHz; integration range from 10 kHz to about f_{DCO} divided by 2
PLL lock-in time	t_L *CC*	4	-	100	µs	

1) Scaling division on the measurement to be applied: sqrt (f_{DCO} / $f_{Aquired}$), at maximum 16

4.14 Power supply topology and power supply characteristics

4.14.1 Power supply topology

***Note**: Not all supply rails are available for all package variants.*

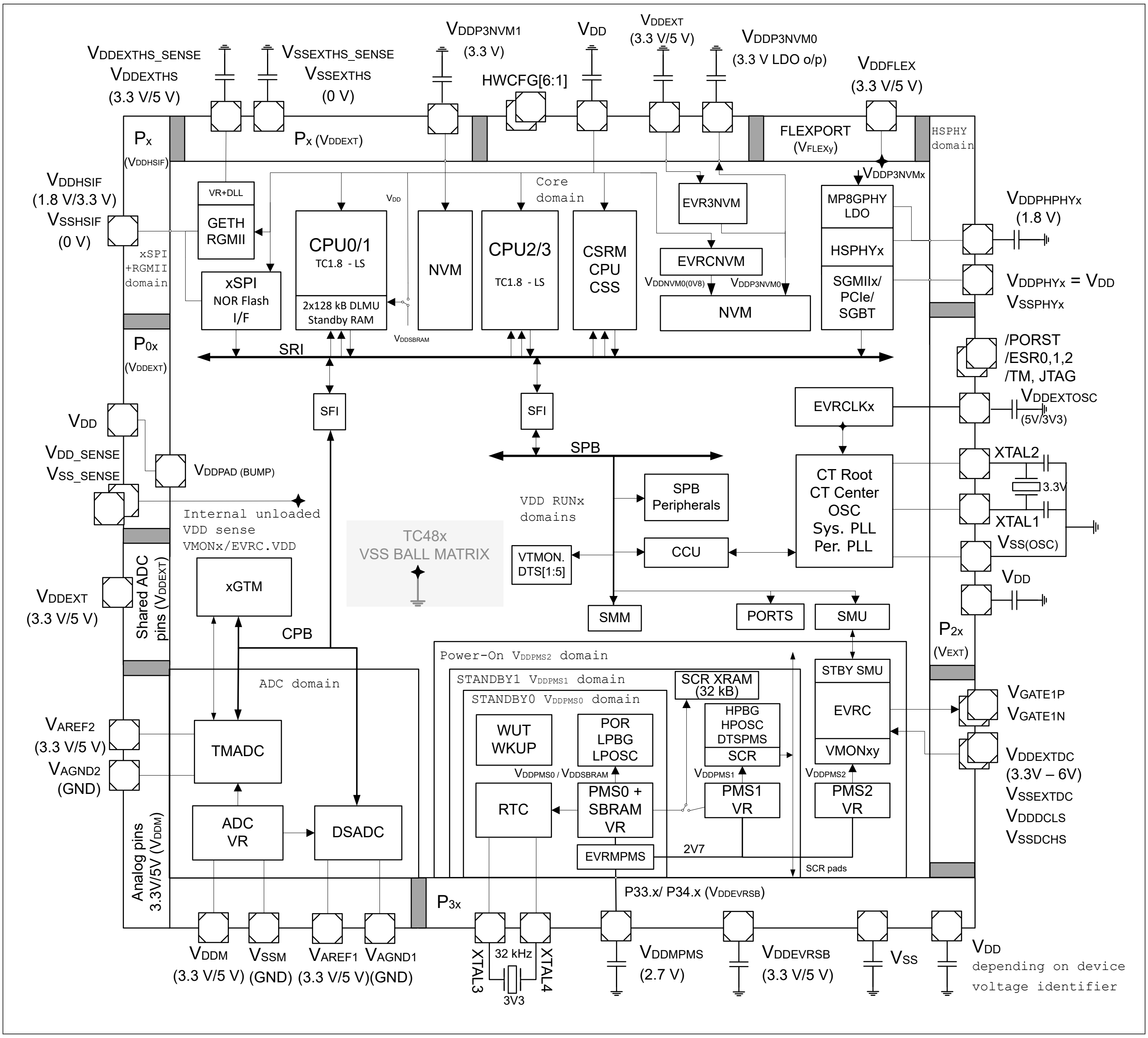


Figure 5 Power Supply Topology

Related information

Supply ramp-up and ramp-down behavior on page 249
LVD reset characteristics on page 250
Line Transients on page 251

4.14.2 Supply ramp-up and ramp-down behavior

This section presents the behavior of the supply rails during ramp-up, ramp-down, and dynamic operational phases.

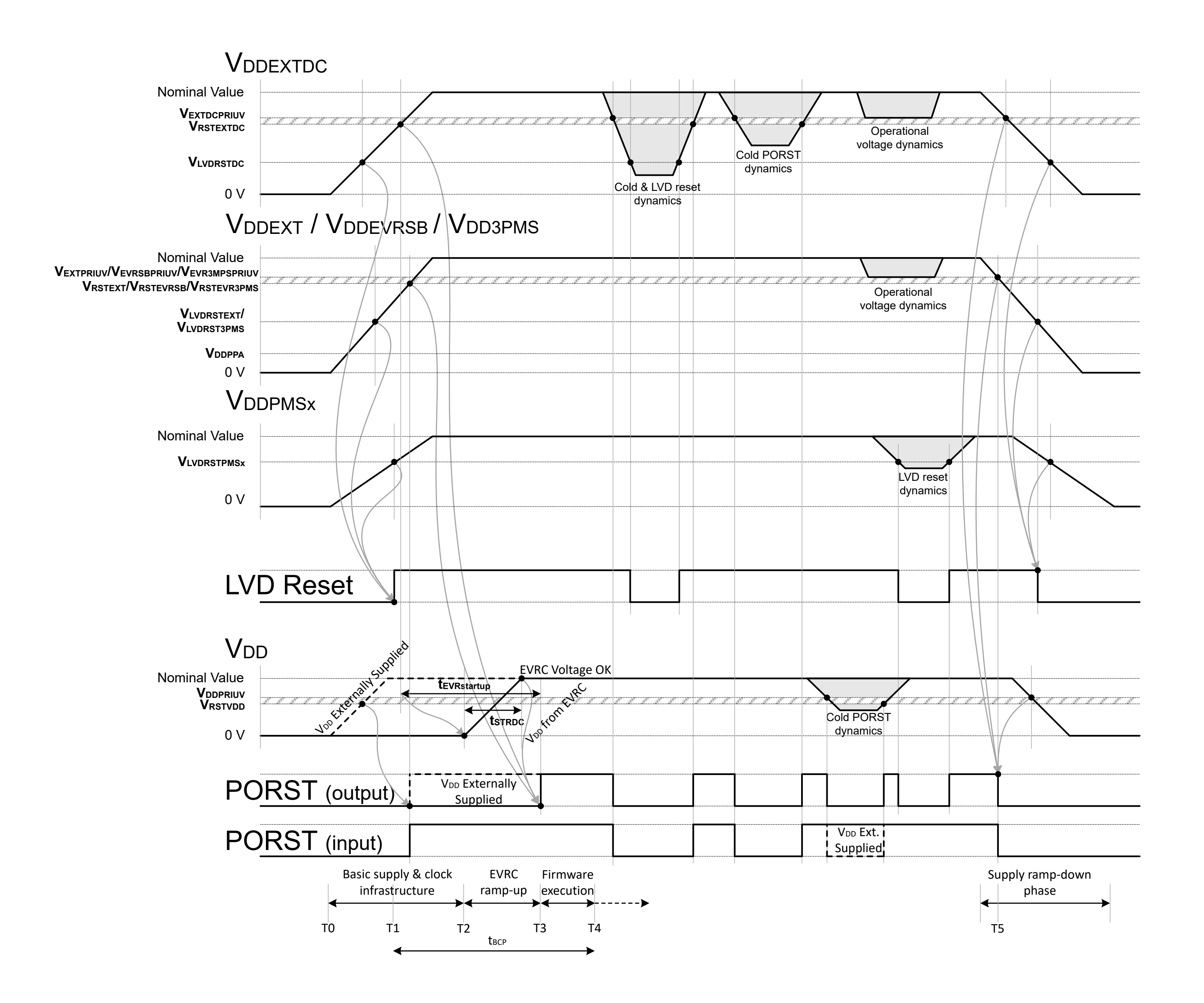


Figure 6 **Supply ramp-up and ramp-down behavior**

- The start-up slew rates for the supply rails shall comply to the respective data sheet parameters dV_{xx}/dt. The slope is defined as the maximum tangential slope between 0% to 100% voltage level. The actual waveform may not represent the specification
- In case of an external regulator for the V_{DD} supply rail, it is ensured that the load jumps to the external regulator (from the V_{DD} rail) are limited during the start-up phase to the dI_{DDDYN_STRT} data sheet parameter
- PORST is active or asserted when either PORST (input) or PORST (output) is active or asserted
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold (V_{RSTxx} parameter in the datasheet)
- PORST (output) active means that the microcontroller asserts the reset internally and drives the PORST pin low, propagating the reset to external devices. The PORST (output) is asserted by the MCU when at least one supply domain violates its primary under-voltage reset threshold. The PORST (output) is de-asserted by the microcontroller when all relevant supplies (with VMONP_VxxRST.RESETOFF = 0) are above their primary reset thresholds and the basic supply and clock infrastructure is available

The power sequence as shown in the figure above is enumerated as follows:

- T0 is the begin of the supply ramp-up from the external regulator
- T1 is the point in time when LVD reset is released. The LVD resets are released when $V_{DDEXTDC}$, V_{DDEXT}, V_{DD3PMS}, and V_{DDPMSx} are above their LVD reset levels (denoted as $V_{LVDRSTxx}$)
- T0 up to T2 refers to the period in time when basic supply and clock infrastructure components are made available as the external supply ramps up. The band-gap and internal clock sources are started. The supply mode is evaluated based on the *HWCFG* pins. These events are initiated after LVD reset release at T1
- T2 refers to the point in time where a soft start of the EVRC is initiated. PORST (input) does not have any effect on the EVRC output and the regulator continues to generate the respective voltage though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the t_{STRDC} time (data sheet parameter) to avoid overshoots
- T3 refers to the point in time when all supplies are above their primary reset thresholds, denoted as V_{RSTxx}. There are two parameters denoting the primary reset threshold, respectively V_{RSTxx} (which is the untrimmed threshold) and $V_{xxPRIUV}$ (which is the trimmed threshold). Their values are located closely to each other and are indicated therefore as a thin hashed region in the figure above. During the supply ramp-up phase, the untrimmed threshold V_{RSTxx} is used for the first PORST release. After the firmware execution phase, the trimmed threshold $V_{xxPRIUV}$ is used for the PORST assertions. Subsequent reset releases occur at the untrimmed threshold V_{RSTxx}, since the primary voltage monitors reset thresholds VMONP_VxxRST.RESETTRIM are being reset to the V_{RSTxx} values also after a cold PORST (see the "Cold PORST" reset values of the VMONP_VxxRST registers)
- The supply start-up phase is completed when the regulator outputs are stable and operational and all voltages have ramped up. Consequently cold PORST reset is released when all voltages on the primary monitors are above their minimum operational limits (V_{RSTxx}/$V_{xxPRIUV}$)
- T4 refers to the point in time when the firmware execution is completed and the user code execution starts, with CPU0 running at the f_{BACKT} clock frequency. The time between T1 and T4 is documented as t_{BCP} (cold power on reset boot time, datasheet parameter)
- T5 refers to the point in time during the supply ramp-down phase when at least one of the supplies (either externally provided or internally generated) drops below its respective primary under-voltage reset threshold $V_{xxPRIUV}$

Related information

Power supply topology on page 248
LVD reset characteristics on page 250
Line Transients on page 251

4.14.3 LVD reset characteristics

Table 58 LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTEXT}$ *CC*	2.5	-	2.77	V	Supply ramp-down and undershoots
		2.53	-	2.8	V	Supply ramp-up
$V_{DDEXTDC}$ LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTDC}$ *CC*	2.5	-	2.77	V	Supply ramp-down and undershoots
V_{DD3PMS} LVDANA reset undervoltage detector compartor threshold	$V_{LVDRST3PMS}$ *CC*	2.16	-	2.4	V	Supply ramp-down and undershoots
		2.11	-	2.43	V	Supply ramp-up

(table continues...)

Table 58 (continued) LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPMS0} LVDPMSx undervoltage detector compartor threshold	$V_{LVDRSTPMS0}$ *CC*	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
V_{DDPMS1}, V_{DDPMS2} and $V_{DDSBRAM}$ LVDPMSx undervoltage detector compartor threshold	$V_{LVDRSTPMS1}$ *CC*	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
L_{VDx} reset assertion.response time on under voltage for V_{DDEXT} , $V_{DDEVRSB}$, $V_{DDEXTDC}$ and V_{DDPMSx} detectors	t_{LVD} *CC*	-	1	3	µs	LVD assertion
Input high voltage level for HWCFG pins on LVDANA reset release	V_{IH_HWCFG} *SR*	0.7*V_{DDIO}[1]	-	-	V	V_{DDIO} = $V_{LVDRSTEXT}$ [1]
Input low voltage level for HWCFG pins on LVDANA reset release	V_{IL_HWCFG} *SR*	-	-	0.44*V_{DDIO}[1]	V	V_{DDIO} = $V_{LVDRSTEXT}$ [1]
$V_{DDEXTDC}$ LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTDC}$ *CC*	2.53	-	2.8	V	Supply ramp-up

1) V_{DDIO} corresponding to the supply voltage of the IO supply domains V_{DDEXT} or $V_{DDEXTHS}$

Related information

Power supply topology on page 248
Supply ramp-up and ramp-down behavior on page 249
Line Transients on page 251

4.14.4 Line Transients

Table 59 Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External VDDEXT / VDDEXTHS and VDDEVRSB supply ramp-up and ramp-down slope[1) 2)]	dV_{DDEXT}/dt *SR*	8.3E-6	1	50	V/ms	
External VDDM supply ramp-up and ramp-down slope[1) 2)]	dV_{DDM}/dt *SR*	8.3E-6	1	50	V/ms	
External VDD supply ramp-up and ramp-down slope[1) 2)]	dV_{DD}/dt *SR*	8.3E-06[2)]	1	50	V/ms	
$V_{DDEXTDC}$ voltage during cranking	$V_{DDEXTDC\ CRANKING}$ *SR*	2.97	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Cold PORST is not triggered

(table continues...)

Table 59 (continued) Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ voltage during standby	$V_{DDEXTDC\ STANDBY}$ *SR*	0.0	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Higher standby current if VDDEXTDC is kept supplied
V_{DDEXT} voltage during cranking	$V_{DDEXT\ CRANKING}$ *SR*	2.97	-	5.5	V	Cold PORST is not triggered
V_{DDEXT} voltage during standby	$V_{DDEXT\ STANDBY}$ *SR*	0.0	-	5.5	V	Higher standby current if V_{DDEXT} is kept supplied
$V_{DDEVRSB}$ voltage during cranking	$V_{DDEVRSB\ CRANKING}$ *SR*	2.97	-	5.5	V	Cold PORST is not triggered
$V_{DDEVRSB}$ voltage during standby	$V_{DDEVRSB\ STANDBY}$ *SR*	2.6	-	5.5	V	
Active pull-up time on VDDEXT/ VDDEXTHS pins during startup	t_{PULLUP} *SR*	-	250	600	µs	HWCFG6=0 time where the internal pull-up is active during device startup before switching to tri-state

1) The device is robust against residual voltage ramp-up starting between [0 up to minimal operational voltage] for V_{DDEXT}, $V_{DDEVRSB}$, $V_{DDEXTDC}$, V_{DDHSIF} (if applicable), V_{DDM} and V_{DD}.
2) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Related information

Power supply topology on page 248
Supply ramp-up and ramp-down behavior on page 249
LVD reset characteristics on page 250

4.15 PMS characteristics

The PMS is comprised of 3 power domain partitions PMS0, PMS1, and PMS2, to support the low power STANDBY0 and STANDBY1 modes. Each of the domains has its own voltage regulator:

- VDDPMS0 is used for the PMS0 domain
- VDDPMS1 is used for the PMS1/PMS2 domains

The EVRC SMPS regulator is also included in the PMS. Its purpose is to provide the main VDD core voltage.

The entire power supply topology can be found in chapter 'Power Supply Topology'.

Related information

Power supply topology on page 248

4.15.1 EVR3PMS

Table 60 EVR3PMS

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage range during operation	V_{IN} *SR*	2.86	-	5.5	V	Input supply is VDDEVRSB; valid for 5V and 3.3V supply mode. Voltage at supply pin
Extended input voltage range during operation	V_{IN_EXT} *SR*	2.55	-	6.50	V	Input supply during start-up with slopes defined by parameter dV_{DDEXT}/dt. Input supply is VDDEVRSB; valid for 3.3V and 5V supply mode
Output voltage range including load/line regulation, static error and aging after trimming	V_{OUTT} *CC*	2.484	2.7	3	V	Specified at the VDD3PMS internal sense point. 1) 2)
Output voltage range including load/line regulation, static error and aging before trimming	V_{OUT_UT} *CC*	2.4	-	3	V	Specified at the VDD3PMS internal sense point. current load=55mA(max) and for load transient condition, • *d*I=0.01mA to 20.01mA and the vice versa, *d*t=3us • *d*I=0.01mA to 0.16mA and the vice versa, *d*t=20ns 3)
External output buffer capacitor	C_{OUT} *SR*	0.5	1.0	1.35	µF	4)

1) Only valid in the input voltage range during operation
2) Load and line transient with *dV*/*dt*<=1V/ms can occur at the same time instance. Max.static and dynamic error=<8% of typical voltage
3) Valid for extended voltage range
4) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before C_{out}

Related information

VDDPMS0 and VDDSBRAM regulator characteristics on page 254

VDDPMS1 regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS characteristics on page 257
EVRC SMPS external components on page 260
Internal supply voltage operating conditions on page 263

4.15.2 VDDPMS0 and VDDSBRAM regulator characteristics

Table 61 VDDPMS0 and VDDSBRAM regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEVRSB}$ voltage range during start-up and operation mode transitions	$V_{DDEVRSBIN}$ *SR*	2.6	-	6.5	V	Operation between 5.5 V and 6.5 V is limited to max. 2.8 h
VDDPMS0 regulator output voltage Static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS0UT}$ *CC*	0.88	0.95	1	V	
VDDPMS0 regulator output voltage range including load/ line regulation and aging	V_{DDPMS0} *CC*	0.88	0.95	1	V	
VDDPMS0 maximum output load current	$I_{DDPMS0MAX}$ *SR*	-	-	0.8	mA	
VDDPMS0 and VDDSBRAM regulator line transient response	dV_{DDPMS0}/ dV_{IN} *CC*	-15	-	15	mV	dV/dT = 50 V/ms; dV < I 2.97-5.5 V I; C_L = 1 nF (C_L is an on-chip load capacitor)

Related information

EVR3PMS on page 253
VDDPMS1 regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS characteristics on page 257
EVRC SMPS external components on page 260
Internal supply voltage operating conditions on page 263

4.15.3 VDDPMS1 regulator characteristics

Table 62 VDDPMS1 regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS1UT}$ *CC*	0.936	0.98	1.024	V	

(table continues...)

Table 62 (continued) VDDPMS1 regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - trimmed	$V_{DDPMS1T}$ *CC*	0.93	0.95	0.97	V	Standby mode at 70 kHz
		0.96	0.98	1	V	Standby mode and operation at 100 MHz
VDDPMS1 regulator output voltage range including load/ line regulation and aging	V_{DDPMS1} *CC*	0.91	0.95	0.97	V	Standby mode at 70 kHz
		0.94	0.98	1.00	V	Standby mode and operation at 100 MHz
VDDPMS1 maximum output load current	$I_{DDPMS1MAX}$ *SR*	-	-	12	mA	
VDDPMS1 regulator load transient response	dV_{DDPMS1}/dI_{OUT} *CC*	-60	-	60	mV	$dI < \pm 3$ mA; $t_r = 0.01$ µs; $t_f = 0.01$ µs; $T_{settle} = 20$ µs; $C_L = 1.5$ nF (C_L is an on-chip load capacitor); VDDPMS1 regulator in high current sink mode
Maximum load step limitation of VDDPMS1 regulator	dI_{DDPMS1}/dI_{OUT} *SR*	-	-	4	mA	SW limits load jumps
VDDPMS1 regulator line transient response	dV_{DDPMS1}/dV_{IN} *CC*	-15	-	15	mV	$dV/dT = 50$ V/ms; $dV <$ I 2.97-5.5 V I

Related information

EVR3PMS on page 253
VDDPMS0 and VDDSBRAM regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS characteristics on page 257
EVRC SMPS external components on page 260
Internal supply voltage operating conditions on page 263

4.15.4 EVR3NVM

Table 63 EVR3NVM

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage range during operation	V_{IN} *SR*	4.2	5.0	5.5	V	Input supply is VDDEXT; valid for 5V supply mode. Voltage at supply pin
Extended input voltage range during operation	V_{IN_EXT} *SR*	2.97	-	6.50	V	Operation between 5.5V and 6.5V is limited to max. 2.8h; Input supply during start-up with slopes defined by parameter dV_{DDEXT}/dt. Input supply is VDDEXT; valid for 5V supply mode

(table continues...)

Table 63 (continued) EVR3NVM

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage range including load/line regulation and aging	V_{OUT} CC	2.97	3.30	3.63	V	Specified at the VDDP3NVM internal sense point [1)]
Output voltage range at startup	V_{OUT_START} CC	2.7	-	-	V	Only for RRAM read operations; valid for VDDEXT<2,97V, Iload<=40mA [2)]
Output static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.234	-	3.39	V	Specified at the VDDP3NVM internal sense point. [3)]
Load transient response - trimmed	dV_{OUT}/dI_{OUT} CC	-132	-	-	mV	Specified at the VDDP3NVM internal sense point. dI=16mA to 100mA, dt=6,5ns, dI=4mA to 40mA, dt=2,8ns, t_{settle}=8µs. Settling assumed when V_{OUT} reaches a voltage level equivalent to ±1% of the static accuracy before the load transient. The dynamic error limit is 4% wrt. the static accuracy. [4)]
		-	-	132	mV	Specified at the VDDP3NVM internal sense point. dI=100mA to 16mA, dt=6,5ns, dI=40mA to 4mA, dt=2,8ns, t_{settle}=8µs. Settling assumed when VOUT reaches a voltage level equivalent to ±1% of the static accuracy before the load transient. The dynamic error limit is 4% wrt. the static accuracy. [4)]
Line transient response[5)]	dV_{OUT}/dV_{IN} CC	-	-	33	mV	dV_{IN}/dt=1V/ms, dV=4,2V to 5,5V , I_{OUT}=140mA
		-33	-	-	mV	dV_{IN}/dt=1V/ms, dV=5,5V to 4,2V, I_{OUT}=140mA
Maximum output current of the regulator	I_{MAX} CC	-	-	140	mA	[4)]

(table continues...)

Table 63 (continued) EVR3NVM

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Startup Time	t_{STRTUP} *CC*	-	-	500	µs	V_{DDEXT}>2,97V. Startup time is defined when the LDO is enabled and V_{OUT}>=2,7V
External output buffer capacitor	C_{OUT} *SR*	1.1	2.2	2.97	µF	[6)]
Output buffer capacitor ESR	C_{OUT_ESR} *SR*	-	-	100	mΩ	f > 0.5MHz; f < 10MHz
Dropout voltage	$V_{DROPOUT}$ *CC*	-	-	400	mV	Dropout operation for V_{IN} < 3.7V; no external load applied

1) No external inductive load permissible if EVR3NVM is used
2) V_{DDEXT} input voltage drops up to 2.97V leading to lower $V_{DDP3NVM}$ output sufficient to ensure RRAM read operations
3) No external inductive load permissible if EVR3NVM is used
4) Only valid in the input voltage range during operation
5) EVR3NVM is robust against residual voltage ramp-up starting between 0 - 2.97 V. The generated voltage itself follows a soft ramp-up over the t_{STR} time to avoid overshoots
6) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before C_{out}

Related information

EVR3PMS on page 253
VDDPMS0 and VDDSBRAM regulator characteristics on page 254
VDDPMS1 regulator characteristics on page 254
EVRC SMPS characteristics on page 257
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Internal supply voltage operating conditions on page 263

4.15.5 EVRC SMPS characteristics

Table 64 EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEXTDC}$ Voltage range during start-up	$V_{INEXTDCSTRT}$ *SR*	2.6[1)]	-	4.43	V	$V_{DDEXTDC}$ = 3.3V nominal voltage. Operation between 3.63 V and 4.43 V is limited to max. 2.8 h with EVRC in reset (no switching)
		3.5	-	7.0	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode, Operation between 6.5 V and 7.0 V is limited to 2.8 h with EVRC in reset (no switching).

(table continues...)

Table 64 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEXTDC}$ voltage range during operation mode	$V_{INEXTDC}$ *SR*	2.97	-	3.63	V	$V_{DDEXTDC}$ = 3.3 V nominal voltage
		3.6	-	6.5	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode. Maximum DC voltage is 6.2V
Input $V_{DDEXTDC}$ and $V_{DDEVRSB}$ peak to peak Voltage Ripple during start-up and operation, at the external regulator output	$V_{INRIPPLE}$ *SR*	-	0.1	0.3	V	100 kHz < f_{ripple} < 3 MHz; square/sinusoidal ripple may be assumed
SMPS regulator output voltage range including load/line regulation and aging - trimmed	V_{DDDC} *CC*	0.983	1.025	1.087	V	$I_{DDSLEEP} \leq I_{DDDC} \leq I_{DDDCMAX}$; V_{ID} = slow + typical samples; for load transients $\|dI\|$ < 200 mA
		0.936	0.975	1.034	V	$I_{DDSLEEP} \leq I_{DDDC} \leq I_{DDDCMAX}$; V_{ID} = fast samples; for load transients $\|dI\|$ < 200 mA
SMPS regulator static voltage output accuracy without dynamic load/line regulation - trimmed	V_{DDDCT} *CC*	1.004	1.025	1.046	V	$I_{DDSLEEP} \leq I_{DDDC} \leq I_{DDDCMAX}$; V_{ID} = slow + typical samples; Voltage at V_{DD_SENSE} (EVRC feedback)
		0.955	0.975	0.995	V	$I_{DDSLEEP} \leq I_{DDDC} \leq I_{DDDCMAX}$; V_{ID} = fast samples; Voltage at V_{DD_SENSE} (EVRC feedback)
SMPS regulator static voltage output accuracy without dynamic load/line regulation - untrimmed	V_{DDDCUT} *CC*	0.975	1.025	1.075	V	$I_{DD\_LEAK} \leq I_{DDDC} \leq I_{DDDCSTRT}$
Programmable switching frequency after trimming	f_{DCDC} *SR*	-	0.8	-	MHz	$I_{DDDC} \leq I_{DDDCMAX}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
		-	0.45	-	MHz	$I_{DDDC} \leq I_{DDDCMAX}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
Start-up time	t_{STRDC} *CC*	0.2	-	1.5	ms	SMPS start-up mode; it is defined as the EVRC ramp-up time from 0V until V_{DD} nominal voltage reached, on condition that all other PORST requirements were released before; $I_{DDDC} = I_{DDDCSTRT}$
Switching frequency modulation spread	ΔT_{DCSPR} *SR*	-	10	-	ns	Modulation spread of the switching frequency, expressed as time period instead of frequency

(table continues...)

Table 64 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum ripple at I_{MAX}	ΔV_{DDDC} *CC*	-	-	14	mV	$I_{DDDCSTRT} \leq I_{DDDC} \leq I_{DDDCMAX}$; ΔV_{DDDC} = (peak-to-peak ripple / 2)
Current consumption of SMPS regulator at minimum load	I_{DCNL} *CC*	-	-	30	mA	f_{DCDC} = 0.8 MHz; I_{DDDC} = 10 mA; T_J = 25°C; current drawn from the $V_{DDEXTDC}$ rail
Standby/Quiescent current consumption of SMPS regulator	I_{DCSTBY} *CC*	-	53	80	µA	EVRC off in standby mode; current drawn from the $V_{DDEXTDC}$ rail; $V_{DDEXTDC}$ LV case (3.3 V); $V_{DDEXTDC}$ = 3.3 V ± 10%
		-	183	250	µA	EVRC off in standby mode; current drawn from the VDDEXTDC rail; VDDEXTDC HV case (VDDEXTDC= 6.5V)
SMPS regulator peak efficiency	n_{DC} *SR*	-	85	-	%	V_{IN} = 3.3 V; f_{DCDC} = 0.45 MHz
		-	85	-	%	V_{IN} = 3.3 V; f_{DCDC} = 0.8 MHz
Maximum output current	$I_{DDDCMAX}$ *CC*	-	-	3.0	A	HE case, RUN Mode [2)]
SMPS regulator line transient response	dV_{DDDCT} / dV_{IN} *CC*	-6	-	6	%	Expressed as % of V_{DDDC} nominal value; dV/dt = 70 V/ms; $\lvert dV\rvert < \lvert V_{INEXTDCSTRT}$ (Min) - $V_{INEXTDCSTRT}$ (Max)$\rvert$; does not include EVRC ripple.
		-1	-	1	%	Expressed as % of V_{DDDC} nominal value; dV/dt = 1 V/ms; $\lvert dV\rvert < \lvert V_{INEXTDCSTRT}$ (Min) - $V_{INEXTDCSTRT}$ (Max)$\rvert$; does not include EVRC ripple.
SMPS regulator load transient response before trimming	dV_{DDDCUT} / dI_{OUT} *CC*	-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $\lvert dI\rvert$ < dI_{DDDYN_STRT}; $I_{DDDC} = I_{DDDCSTRT}$; t_r = 0.1 µs; t_f = 0.1 µs; V_{DDDC} untrimmed; T_{settle} = 20 µs (Typ), 70 µs (Max); HE components; includes EVRC ripple
		-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $\lvert dI\rvert < \lvert dI_{DDDYN\_LBIST}\rvert$; $I_{DDDC} = I_{DDDCSTRT}$; EVRC bandgap and clock trimmed but operated with default coefficients; HE components; includes EVRC ripple

(table continues...)

Table 64 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input Synchronisation frequency	$f_{DCDCSYNC}$ *SR*	0.42	0.45	0.49	MHz	f_{DCDC} = 0.45 MHz HE case
		0.72	0.8	0.9	MHz	f_{DCDC} = 0.8 MHz HE case
Feedback ADC resolution for voltage scaling	dV_{FBADC} *SR*	-	2.83	-	mV	Used for scaling of VDD target value in EVRC_CON0 register. Feedback ADC nominal range < 1.446 V

1) LCDCDC standalone lower limit. The minimum startup voltage of LCDCDC also depends on LVD reset threshold and Primary undervoltage thresholds of VDDEVRSB, VDDEXT, VDDEXTDC

2) HE refers to EVRC configuration and components for $I_{DD} < I_{DDDCMAX}$ for HE case

Related information

EVR3PMS on page 253
VDDPMS0 and VDDSBRAM regulator characteristics on page 254
VDDPMS1 regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS external components on page 260
Internal supply voltage operating conditions on page 263

4.15.6 EVRC SMPS external components

Table 65 EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External output capacitor value	C_{OUT} *SR*	20.8	32	43.2	µF	$I_{DDDC} \leq I_{DDDCMAX}$; f_{DCDC} = 0.8 MHz; 22 µF + 10 µF connected in parallel
		28.6	44	59.4	µF	$I_{DDDC} \leq I_{DDDCMAX}$; f_{DCDC} = 0.45 MHz; 2 x 22 µF connected in parallel
External output capacitor ESR	C_{OUT_ESR} *SR*	-	-	100	Ohm	f = 10 Hz
		-	-	20	mOhm	f ≥ 0.5 MHz ; f ≤ 10 MHz
External input capacitor values (Buffer + Decoupling)[1]	C_{IN} *SR*	14.3 + 0.065	22 + 0.1[2]	29.7 + 0.135	µF	$I_{DDDC} \leq I_{DDDCMAX}$; f_{DCDC} = 0.45 MHz
		14.3 + 0.065	22 + 0.1[2]	29.7 + 0.135	µF	$I_{DDDC} \leq I_{DDDCMAX}$; f_{DCDC} = 0.8 MHz
External input capacitor ESR	C_{IN_ESR} *SR*	-	-	20	mOhm	f ≥ 0.5 MHz; f ≤ 10 MHz
		-	-	100	Ohm	f = 100 Hz
External inductor value	L_{DC} *SR*	1.54	2.2	2.86	µH	f_{DCDC} = 0.8 MHz
		1.54	2.2	2.86	µH	f_{DCDC} = 0.45 MHz

(table continues...)

Table 65 (continued) EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External inductor DCR	L_{DC_DCR} *SR*	-	-	0.02	Ohm	Max. value depending on output current
External Inductor Saturation Current Margin	ΔI_{SAT} *SR*	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} $+\Delta I_{SAT}$
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} *SR*	-	1	-	V	NMOS
		-	-1	-	V	PMOS

(table continues...)

Table 65 (continued) EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SMPS regulator load transient response after trimming	dV_{DDDCT}/ dI_{OUT} CC	-3	-	9	%	Expressed as % of V_{DDDC} nominal value; -800 mA < dI < 0 mA; negative value specifies the max. undershoot after the overshoot; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_f = 0.1 µs; T_{settle} = 40 µs; application reset load drop; includes EVRC ripple 3)
		-3	-	4.0	%	Expressed as % of V_{DDDC} nominal value; -200 mA < dI < 200 mA; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_r = 0.1 µs; t_f = 0.1 µs; T_{settle} = 20 µs; Sync mode disabled; 2 x CPU load jump; includes EVRC ripple
		-3	-	16	%	Expressed as % of V_{DDDC} nominal value; -1.2 A < dI < 0 A; negative value specifies the max. undershoot after the overshoot; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_f = 0.1 µs; T_{settle} = 100 µs; cold or warm PORST load drop; includes EVRC ripple 3)
		-3	-	9	%	Sync enabled; expressed as % of *V*DDDC nominal value; -800 mA < dI < 0 mA; negative value specifies the max. undershoot after the overshoot; *I*DD (Freerun) ≤ *I*DDDC ≤ *I*DDDCMAX; *tf* = 0.1 µs; *T*settle = 40 µs; application reset load drop; includes EVRC ripple 3)
		-4.5	-	16	%	Sync enabled; expressed as % of *V*DDDC nominal value; -1.2 A < dI < 0 A; negative value specifies the max. undershoot after the overshoot; *I*DD (Freerun) ≤ *I*DDDC ≤ *I*DDDCMAX; *tf* = 0.1 µs; *T*settle = 100 µs; cold or warm PORST load drop; includes EVRC ripple

(table continues...)

Table 65 **(continued) EVRC SMPS external components**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
						3)

1) The "+" means that both (Buffer and Decoupling) Capacitors have to be connected in parallel close to the external power stage. The smaller one (Decoupling Capacitor) needs to be placed as close as possible to the source connection of the PMOS.
2) Additional external components maybe required depending on EMI/EMC requirements
3) T_{settle} is the time after which the V_{DD} output voltage returns to within ±1.5% of the static EVRC output voltage value without any load transient.

Related information

EVR3PMS on page 253
VDDPMS0 and VDDSBRAM regulator characteristics on page 254
VDDPMS1 regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS characteristics on page 257
Internal supply voltage operating conditions on page 263

4.15.7 Internal supply voltage operating conditions

Table 66 **Internal supply voltage operating conditions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Internal core supply voltage for PMS0	V_{DDPMS0} *SR*	0.80	0.95	1.08	V	
Internal core supply voltage for PMS1 and PMS2	$V_{DDPMS1,2}$ *SR*	0.81	0.95	1.08	V	Standby mode at 70 kHz
		0.81	0.98	1.13	V	Standby mode and operation at 100 MHz

Related information

EVR3PMS on page 253
VDDPMS0 and VDDSBRAM regulator characteristics on page 254
VDDPMS1 regulator characteristics on page 254
EVR3NVM on page 255
EVRC SMPS characteristics on page 257
EVRC SMPS external components on page 260

4.16 System mode dependent and reset timing characteristics

4.16.1 System state timings

Table 67 System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY0 entry transition time from STANDBY1_70k mode on SCR events	t_{STBY10} *CC*	-	-	50	µs	
STANDBY0 exit transition time to STANDBY1 _70k mode on wake-up events	t_{STBY01} *CC*	-	-	150	µs	
Standby RAM supply switch activation time during Run mode on V_{DDEXT} or V_{DD} primary undervoltage event	$t_{STBYRAM}$ *CC*	-	-	1	µs	dLMU Standby RAM supply switched
STANDBY1 entry transition time from RUN mode on V_{DDEXT} or V_{DD} undervoltage event	$t_{RxSTBY1}$ *CC*	-	1	10	µs	Current consumption $I_{STANDBY1}$ reached
STANDBY1 transition time to disable Bandgap and ADCOMP	$t_{ADC100M}$ *CC*	-	-	10	µs	SCR ADCOMP and HPBG disable, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to enable Bandgap and ADCOMP	$t_{100MADC}$ *CC*	-	-	50	µs	SCR ADCOMP_CON.EN_REQ request until ADCOMP_RESHSTAT.EN_STAT set to 1. ADCOMP SUCAL not considered, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to disable back-up clock	$t_{100M70k}$ *CC*	-	-	110	µs	SCR f_{SBT} clock request via SCU_CLK.DIV_REQ to switch off f_{BACKT} clock, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to enable back-up clock	$t_{70k100M}$ *SR*	-	-	170	µs	SCR f_{BACKT} clock request via SCU_CLK.DIV_REQ until SCU_CLK.DIV_STAT is updated
Minimum HWCFG hold time after LVDANA reset release during start-up	t_{HWCFG} *SR*	200	-	600	µs	HWCFG latch after start-up for EVRC configuration. V_{DDEXT}, $V_{DDEVRSB}$ and $V_{DDEXTDC}$ above LVD detector levels. R_{HWCFG} = 4.7 kOhm ± 50%, V_{IL} = see V_{IL_HWCFG}, V_{IH} = see V_{IH_HWCFG}.
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ *SR*	360	-	-	µs	Valid for all primary voltage monitors to ensure proper reset shutdown sequencing.

(table continues...)

Table 67 (continued) System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MBIST execution time extending the boot time	t_{MBIST} *CC*	-	-	6	ms	Key-on MBIST (4N-DT, f_{SRI}=100 MHz) and consecutive initialization. Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
		-	25	-	ms	Key-off MBIST (4N-DT, f_{SRI} = MAX). Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
LBIST execution time	t_{LBIST} *CC*	-	-	50	ms	Key-off LBIST; Time per LBIST-Cluster; Reset time excluded
		-	-	6	ms	Key-on LBIST; Reset time excluded
Timing-Window available for placement of external Tool-Requests via COMDATA/ Cerberus	t_{WINDOW} *CC*	800	-	-	µs	In case of DXCPL used, shortened SPD-0-bitwidth in Activation sequence required.
Transitioning time to permanent reset	t_{WCST} *CC*	-	-	43	ms	Time is a sum of t_{BCP} (incl. EVR ramp-up) + t_{BCP} (w/o EVR ramp-up) + 2 * (FW fault handling time + $t_{CPU0WDT}$ + t_{RTC} + $t_{WARMRSTSEQ}$)

Related information

Reset timings on page 265
Power, pad and reset timing figure on page 267

4.16.2 Reset timings

Table 68 Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Cold Power on Reset Boot Time [1)]	t_{BCP} *CC*	-	-	3.5	ms	Firmware execution time after PORST release without EVRC ramp-up; RAM initialization, LBIST execution and CSRM boot time is not included [2)]
		-	3	5.5	ms	dV_{DDEXT}/dT = 1 V/ms; V_{DDEXT} > $V_{LVDRST5}$; boot time after Cold PORST including EVRC ramp-up, PBIST and Firmware execution time; RAM initialization and CSRM boot time are not included

(table continues...)

Table 68 (continued) Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary VMONP monitors	t_{EVRPOR} *CC*	10[3]	-	-	µs	
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} *SR*	-	1[4]	-	ms	
EVRC ramp-up time till cold PORST reset release	$t_{EVRstartup}$ *CC*	-	1	2	ms	It is defined from the $V_{EXTDCPRIUV}$ reset threshold crossing until cold PORST reset release. dV/dT=1 V/ms; EVRC active
Application Reset Boot Time	t_{BAR} *CC*	-	-	750	µs	operating with max. frequencies, with valid BMHD header; Warm Reset Sequencing Delay Time not included
System Reset Boot Time [2]	t_{BSR} *CC*	-	-	2	ms	w/o SWAP, with valid BMHD header
Warm PORST reset boot time[2]	t_{BWP} *CC*	-	-	3.3	ms	Start from internal NVM with configured BMHD. Time does not include RAM initialization, Foreground CSRM-Boot, ABM and LBIST-Runtime
Warm Reset Sequencing Delay Time	$t_{WARMRSTSEQ}$ *CC*	-	-	300	µs	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ *CC*	600	-	1200	ns	
Ports inactive after ESR0 reset active	t_{PI} *CC*	-	-	8 / f_{SPB}	ns	
Ports inactive after PORST reset active	t_{PIP} *CC*	-	-	600	ns	
Hold time from PORST rising edge	t_{POH} *SR*	360	-	-	ns	
Setup time to PORST rising edge	t_{POS} *SR*	0	-	-	ns	
SCR reset boot time [2]	$t_{SCRBOOT}$ *CC*	-	-	60	µs	On user mode entry at 20 MHz SCR core clock, Standby exit, WDT (System) double bit ECC reset and soft reset
		-	-	230	µs	On user mode entry at 70 kHz SCR core clock, Standby exit, WDT (System) double bit ECC reset and soft reset

1) RAM initialization in SSW of PMEM, DMEM, PTAG, DTAG and DLMU RAMs add 1000 µs in addition.
2) From release of PORST by PMS
3) Cold PORST reset is driven by µC and maintained in an extended voltage range between V_{DDPPA} limit and absolute maximum rating voltage limits.
4) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on V_{DDEXT}, V_{DDHSIF} (if applicable) and V_{DD} rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The t_{POA} additional time is recommended for a robust start-up and not a mandatory requirement.

Related information

System state timings on page 264
Power, pad and reset timing figure on page 267

4.16.3 Power, pad and reset timing figure

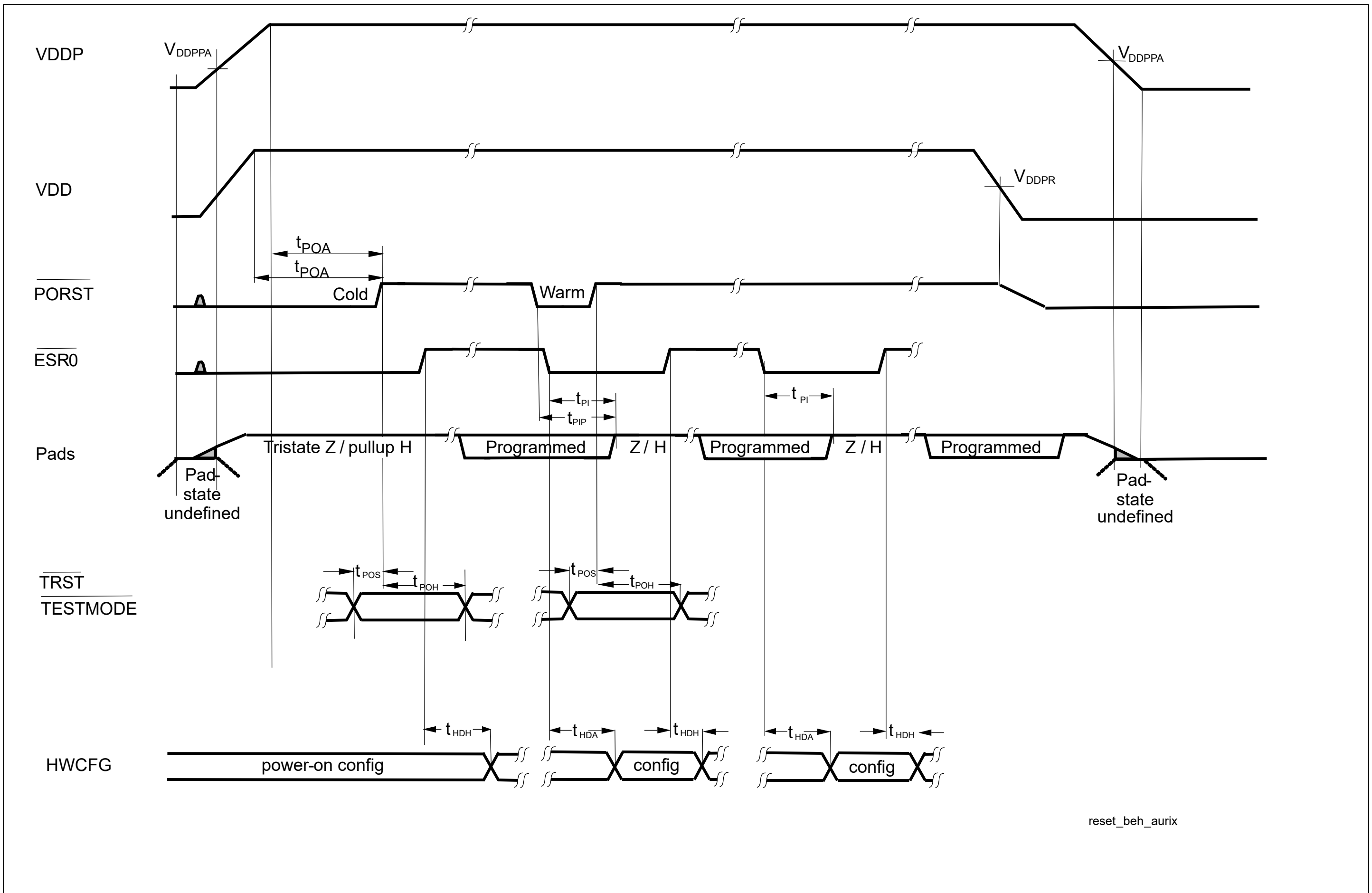


Figure 7 **Power, pad and reset timing**

Related information

System state timings on page 264
Reset timings on page 265

4.17 PMS voltage monitoring characteristics

The supply rails monitored by primary and secondary voltage monitors are measured by primary and secondary monitor ADCs. Four ADC topologies are used for this purpose:

- Tracking High Voltage ADC (TRKHV)
- Tracking Core ADC (TRKCORE)
- SAR High Voltage ADC (SARHV)
- SAR Core ADC (SARCORE)

The characteristics of this ADCs can be found in the following sub-chapter.

4.17.1 Primary and secondary voltage monitor ADC characteristics

Table 69 Primary and secondary voltage monitor ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Core tracking ADC characteristics						
Core tracking ADC least significant bit	$V_{TRKCORELSB}$ *CC*	-	2.830	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
Core tracking ADC measurement latency	$t_{TRKCORE}$ *CC*	-	-	21	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
High-voltage tracking ADC characteristics						
High-voltage tracking ADC least significant bit	$V_{TRKHVLSB}$ *CC*	-	22.64	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage tracking ADC measurement latency	t_{TRKHV} *CC*	-	160	164	ns	Back-up Clock oscillator trimmed; spike FILTER = 0
Core SAR ADC characteristics						
Core SAR ADC least significant bit	$V_{SARCORELSB}$ *CC*	-	0.586	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
Core SAR ADC measurement latency	$t_{SARCORE}$ *CC*	-	420	430	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used; after firmware boot
High-voltage SAR ADC least significant bit	$V_{SARHVLSB}$ *CC*	-	4.741	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage SAR ADC characteristics						
High-voltage SAR ADC measurement latency	t_{SARHV} *CC*	-	-	780	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
Medium-voltage SAR ADC characteristics						
Medium-voltage SAR ADC least significant bit	$V_{SARMVLSB}$ *CC*	-	2.83	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation

4.17.2 Primary voltage monitors

4.17.2.1 Primary voltage monitors parameters overview

***Note**: This table includes all voltage rails available for the TC4x family. The availability per derivative can be looked up in the Primary voltage monitors characteristics table.*

Table 70 Primary voltage monitors parameters

Voltage rail	VMONP LSB datasheet parameter	Primary under-voltage reset threshold after trimming - datasheet parameter	Effect of primary under-voltage reset threshold violation[1)]
V_{DD}	$V_{TRKCORELSB}$	$V_{DDPRIUV}$	Cold PORST
V_{DDEXT}	$V_{SARHVLSB}$	$V_{EXTPRIUV}$	Cold PORST
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{EXTDCPRIUV}$	Only when EVRC is enabled, a power state transition corresponding to an EVRC failure is triggered. The primary monitor triggers not only a cold PORST, but a deeper power state where the EVRC regulator is disabled, until the supply raises above the reset release threshold.
$V_{DDEXTHS}$	$V_{SARHVLSB}$	$V_{EXTHSRIUV}$	Cold PORST
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{EVRSBPRIUV}$	Cold PORST
V_{DD3PMS}	$V_{SARMVLSB}$	$V_{DD3PMSPRIUV}$	Cold PORST
$V_{DDP3NVM}$	$V_{SARMVLSB}$	$V_{DDP3NVMPRIUV}$	Cold PORST
V_{DDM}	$V_{SARHVLSB}$	$V_{DDMPRIUV}$	Cold PORST
$V_{DDPHPHYx}$	$V_{SARMVLSB}$	$V_{PHPHYPRIUV}$	Cold PORST
V_{DDHSIF}	$V_{SARMVLSB}$	$V_{HSIFPRIUV}$	Cold PORST
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADPRIUV}$	Cold PORST
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUPRIUV}$	Cold PORST
V_{DDLMUx}	$V_{SARCORELSB}$	$V_{DDLMUPRIUV}$	Cold PORST
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYPRIUV}$	Cold PORST

1) Only if the respective VMONP_VxxRST.RESETOFF bit is set to zero.

Related information

Primary voltage monitors characteristics on page 270

4.17.2.2 Primary voltage monitors characteristics

Table 71 Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Non-configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold before trimming [1]	$V_{RSTEXTDC}$ *CC*	2.6	-	3	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
V_{DDEXT} primary undervoltage reset threshold before trimming [1]	V_{RSTEXT} *CC*	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
$V_{DDEVRSB}$ primary undervoltage reset threshold before trimming[1]	$V_{RSTEVRSB}$ *CC*	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
V_{DD} primary undervoltage reset threshold before trimming	V_{RSTVDD} *CC*	-	-	0.894	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
Configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold after trimming	$V_{EXTDCPRIUV}$ *CC*	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; $V_{DDEXTDC}$ = 3.3 V mode [2]
		3.328	3.396	3.464	V	Default cold PORST PRIUV threshold = 0x12C; RESETHYS = 0x0; $V_{DDEXTDC}$ high-voltage mode [2]
V_{DDEXT} primary undervoltage reset threshold after trimming	$V_{EXTPRIUV}$ *CC*	2.791	2.863	2.935	V	Default cold PORST PRIUV threshold = 0x25C; RESETHYS = 0x0; V_{DDEXT} = 3.3 V mode
		4.274	4.361	4.449	V	Configurable cold PORST PRIUV threshold = 0x398; RESETHYS = 0x0; V_{DDEXT} = 5 V mode

(table continues...)

Table 71 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEVRSB}$ primary undervoltage reset threshold after trimming[1]	$V_{EVRSBPRIUV}$ *CC*	4.274	4.361	4.449	V	Configurable cold PORST PRIUV threshold = 0x398; RESETHYS = 0x0; V_{DDEXT} = 5 V mode [2]
		2.791	2.863	2.935	V	Default cold PORST PRIUV threshold = 0x25C; RESETHYS = 0x0; V_{DDEXT} = 3.3 V mode [2]
V_{DDEXT}, $V_{DDEVRSB}$, and V_{DDM} primary undervoltage monitor threshold during supply ramp-down (dV_{IO}/dt)	$V_{EXTPRIUVMIN}$ *CC*	2.76	-	-	V	Valid for dV_{IO} / dt = 50 V / ms; with one single ADC input used; for $V_{DDEVRSB}$, V_{DDEXT} and V_{DDM} with a maximum spike filter setting of 0
V_{DDM} primary undervoltage reset threshold after trimming[1]	$V_{DDMPRIUV}$ *CC*	4.274	4.361	4.449	V	Configurable cold PORST PRIUV threshold = 0x398; RESETHYS = 0x0; V_{DDM} = 5 V mode [2]
		2.791	2.863	2.935	V	Default cold PORST PRIUV threshold = 0x25C; RESETHYS = 0x0; V_{DDM} = 3.3 V mode [2]
$V_{DDP3NVM}$ primary undervoltage reset threshold after trimming[1]	$V_{DDP3NVMPRIUV}$ *CC*	2.535	2.601	2.666	V	Default cold PORST PRIUV threshold = 0x396; RESETHYS = 0x0 [2]
V_{DDPHYx} primary undervoltage reset threshold after trimming[1]	$V_{DDPHYPRIUV}$ *CC*	0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2]
		0.896	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]

(table continues...)

Table 71 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DD} primary undervoltage reset threshold after trimming[1)]	$V_{DDPRIUV}$ *CC*	0.851	0.869	0.887	V	Default cold PORST PRIUV threshold = 0x133; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2)]
		0.895[3)]	0.914	0.933	V	Configurable cold PORST PRIUV threshold = 0x143; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2)]
V_{DDPAD} primary undervoltage reset threshold after trimming[4)]	$V_{DDPADPRIUV}$ *CC*	0.852	0.870	0.888	V	Default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2)]
		0.896	0.915	0.934	V	Configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2)]
V_{DDEXT} and $V_{DDEVRSB}$ PBIST primary overvoltage monitor threshold	V_{PBIST5} *CC*	5.499	5.789	6.078	V	
V_{DD} PBIST primary overvoltage monitor threshold	V_{PBISTC} *CC*	1.128	1.200	1.272	V	
$V_{DDEXTHS}$ primary undervoltage reset threshold after trimming	$V_{EXTHSPRIUV}$ *CC*	2.791	2.863	2.935	V	Default cold PORST PRIUV threshold = 0x25C; RESETHYS = 0x0; VDDEXTHS = 3,3 V mode
V_{DD3PMS} primary undervoltage reset threshold after trimming	$V_{DD3PMSPRIUV}$ *CC*	2.348	2.411	2.475	V	Default cold PORST PRIUV threshold = 0x354; RESETHYS = 0x0

1) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins/dedicated sense pins (VDDxx_SENSE) if available
2) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
3) V_{RSTxx} parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as $V_{xxPRIUV}$ parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.
4) The reset release on supply ramp-up is delayed by a time duration 20-40 μs after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. In case the 3.3 V supply is provided externally, the internal drop will cause a reset at a higher voltage of 3.0 V at the VDDHSIF (if available) pin.

Related information

Primary voltage monitors parameters overview on page 269

4.17.3 Secondary voltage monitors

4.17.3.1 Secondary voltage monitors parameters overview

Note: *This table includes all voltage rails available for the TC4x family. The availability per derivative can be looked up in the Secondary voltage monitors characteristics table.*

Table 72 Secondary voltage monitors parameters

Voltage rail	VMONS LSB datasheet parameter	Secondary voltage monitor accuracy after trimming - datasheet parameter	Secondary voltage monitor conversion time - datasheet parameter	Effects of secondary voltage monitoring thresholds violation[1)]
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{DDEVRSBMON}$	t_{SARHV}	UV, OV alarm
V_{DDEXT}	$V_{SARHVLSB}$	$V_{DDEXTMON}$	t_{SARHV}	UV, OV alarm
V_{DD3PMS}	$V_{SARMVLSB}$	$V_{DD3PMSMON}$	t_{SARHV}	UV, OV alarm
$V_{DDP3NVM}$	$V_{SARMVLSB}$	$V_{DDP3NVMMON}$	t_{SARHV}	UV, OV alarm
V_{DDM}	$V_{SARHVLSB}$	V_{DDMMON}	t_{SARHV}	UV, OV alarm
V_{DDFLEX}	$V_{SARHVLSB}$	$V_{DDFLEXMON}$	t_{SARHV}	UV, OV alarm
V_{DD}	$V_{SARCORELSB}$	V_{DDMON}	$t_{SARCORE}$	UV, OV alarm
V_{DDPMS0}	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	$t_{SARCORE}$	UV, OV alarm
V_{DDPMS2}	$V_{SARCORELSB}$	$V_{DDPMS2MON}$	$t_{SARCORE}$	UV, OV alarm
$V_{DDSBRAM}$	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	$t_{SARCORE}$	UV, OV alarm
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADMON}$	$t_{SARCORE}$	UV, OV alarm
$V_{DDPHPHYx}$	$V_{SARMVLSB}$	$V_{DDPHPHYxMON}$	t_{SARHV}	UV, OV alarm
V_{DDHSIF}	$V_{SARMVLSB}$	$V_{DDHSIFMON}$	t_{SARHV}	UV, OV alarm
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYxMON}$	$t_{SARCORE}$	UV, OV alarm
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUMON}$	$t_{SARCORE}$	UV, OV alarm
$V_{DDEXTHS}$	$V_{SARHVLSB}$	$V_{DDEXTHSMON}$	t_{SARHV}	UV, OV alarm
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{DDEXTDCMON}$	t_{TRKHV}	UV, OV alarm

1) Only if the corresponding VMONS_VxxCON.UVMOD, respectively VMONS_VxxCON.OVMOD, are not zero.

Related information

Secondary voltage monitors characteristics on page 274

4.17.3.2 Secondary voltage monitors characteristics

Table 73 Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ secondary supply monitor accuracy after trimming	$V_{DDEXTDCMON}$ CC	3.549	3.622	3.695	V	$V_{DDEXTDC}$ = 3.3 V mode; xxVAL monitoring threshold = 3.622 V = 0xA0 (OV); FILTER = 0 1)
		3.439	3.509	3.580	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 3.509 V = 0x09B (UV); FILTER = 0 1)
		6.367	6.498	6.628	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 6.498 V = 0x11F (OV); FILTER = 0 1)
		2.906	2.966	3.026	V	$V_{DDEXTDC}$ = 3.3 V mode; xxVAL monitoring threshold = 2.966 V = 0x83 (UV); FILTER = 0 1)
V_{DDEXT} secondary supply monitor accuracy after trimming	$V_{DDEXTMON}$ CC	3.540	3.631	3.723	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x2FE(OV); FILTER = 0 1)
		2.893	2.968	3.042	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 2.968 V = 0x272 (UV); FILTER = 0 1)
		5.389	5.499	5.610	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x488 (OV); FILTER = 0 1)
		4.408	4.499	4.589	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 4.499 V = 0x3B5 (UV); FILTER = 0 1)

(table continues...)

Table 73 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEVRSB}$ secondary supply monitor accuracy after trimming	$V_{DDEVRSBMON}$ CC	2.893	2.968	3.042	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 2.968 V = 0x272(UV); FILTER = 0 [1]
		3.540	3.631	3.732	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x2FE (OV); FILTER = 0 [1]
		4.408	4.499	4.589	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 4.499 V = 0x3B5(UV); FILTER = 0 [1]
		5.389	5.499	5.610	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x488 (OV); FILTER = 0 [1]
$V_{DDP3NVM}$ secondary supply monitor accuracy after trimming[2]	$V_{DDP3NVMMON}$ CC	3.630	3.704	3.778	V	xxVAL monitoring threshold = 3.704 V = 0x51D (OV); FILTER = 0 [1]
		2.646	2.700	2.754	V	xxVAL monitoring threshold = 2.7 V = 0x3BA (UV); FILTER = 0 [1]
V_{DDM} secondary supply monitor accuracy after trimming	V_{DDMMON} CC	2.893	2.968	3.042	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 2.968 V = 0x272 (UV); FILTER = 0 [1]
		3.540	3.631	3.723	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x2FE (OV); FILTER = 0 [1]
		5.389	5.499	5.610	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 5.499V = 0x488(OV); FILTER = 0 [1]
		4.408	4.499	4.589	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 4.499 V = 0x3B5 (UV); FILTER = 0 [1]

(table continues...)

Table 73 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDFLEX} secondary supply monitor accuracy after trimming	$V_{DDFLEXMON}$ CC	2.893	2.968	3.042	V	V_{DDFLEX} = 3.3 V mode; xxVAL monitoring threshold = 2.968 V = 0x272(UV); FILTER = 0 1)
		3.540	3.631	3.723	V	V_{DDFLEX} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x2FE(OV); FILTER = 0 1)
		4.408	4.499	4.589	V	V_{DDFLEX} = 5 V mode; xxVAL monitoring threshold = 4.499 V = 0x3B5(UV); FILTER = 0 1)
		5.389	5.499	5.610	V	V_{DDFLEX} = 5V mode; xxVAL monitoring threshold=5.499V= 0x488(OV); FILTER=0 1)
$V_{DDPHPHYx}$ secondary supply monitor accuracy after trimming	$V_{DDPHPHYxMON}$ CC	1.586	1.619	1.652	V	xxVAL monitoring threshold = 1.619 V = 0x23C(UV); FILTER = 0 1)
		1.941	1.981	2.021	V	xxVAL monitoring threshold = 1.981 V = 0x2BC(OV); FILTER = 0 1)
V_{DDPHYx} secondary supply monitor accuracy after trimming	$V_{DDPHYxMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 1)
		1.084	1.107	1.130	V	xxVAL monitoring threshold = 1.107 V = 0x761(OV); FILTER = 0 1)
V_{DD} secondary supply monitor accuracy after trimming 3)	V_{DDMON} CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 1)
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 1)
V_{DDPMS0} and $V_{DDSBRAM}$ secondary supply monitor accuracy after trimming 2)	$V_{DDPMS0MON}$ CC	0.768	0.785	0.801	V	xxVAL monitoring threshold = 0.785 V = 0x53B(UV); FILTER = 0 1)
		1.079	1.102	1.125	V	xxVAL monitoring threshold = 1.102 V = 0x759(OV); FILTER = 0 1)

(table continues...)

Table 73 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPMS1} and V_{DDPMS2} secondary supply monitor accuracy after trimming[2)]	$V_{DDPMS2MON}$ CC	0.778	0.794	0.810	V	xxVAL monitoring threshold = 0.794 V = 0x54B(UV); FILTER = 0 [1)]
		1.129	1.153	1.177	V	xxVAL monitoring threshold = 1.153 V = 0x7B0(OV); FILTER = 0 [1)]
V_{DDPAD} secondary supply monitor accuracy after trimming	$V_{DDPADMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 [1)]
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 [1)]
$V_{DDEXTHS}$ secondary supply monitor accuracy after trimming	$V_{DDEXTHSMON}$ CC	2.893	2.968	3.042	V	VDDEXT = 3.3 V mode; xxVAL monitoring threshold = 2.972 V = 0x272(UV); FILTER = 0
		3.540	3.631	3.723	V	VDDEXT = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x2FE(OV); FILTER = 0
		4.408	4.499	4.589	V	VDDEXT = 5 V mode; xxVAL monitoring threshold = 4.499 V = 0x3B5(UV); FILTER = 0
		5.389	5.499	5.610	V	VDDEXT = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x488(OV); FILTER = 0
V_{DD3PMS} secondary supply monitor accuracy after trimming	$V_{DD3PMSMON}$ CC	2.422	2.485	2.548	V	xxVAL monitoring threshold = 2.485 V = 0x36E(UV); FILTER = 0
		2.925	3.000	3.075	V	xxVAL monitoring threshold = 3.0 V = 0x424(OV); FILTER = 0

1) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
2) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.
3) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins

Related information

Secondary voltage monitors parameters overview on page 273

4.18 Stand-by Controller (SCR)

4.18.1 SCR SAR ADC characteristics

Table 74 SCR SAR ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal SCR ADC Least Significant Bit Voltage	V_{LSB} CC	-	2.8302	-	mV	11 bit resolution. 5.7962V full range; BACKUP OSC and HPBG trimmed
Wake up Time at Digital Startup	t_{WUADC} CC	436	436	436	cycles	cycle time = 2 / f_{BACKT}
Startup Calibration Time	t_{SCAL} CC	1830	1830	1830	cycles	cycle time = 2 / f_{BACKT}
Sampling Time[1)]	t_{SMV} CC	400	-	-	ns	configurable via ADCOMP_CON.STSEL
Conversion Time	t_{convMV} CC	18	18	18	cycles	cycle time = 2 / f_{BACKT}
Integral Non-Linearity	E_{INL} CC	-4	-	4	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Differential Non - Linearity	E_{DNL} CC	-1	-	3	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Offset Error	E_{OFFSET} CC	-4	-	4	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Gain Error	E_{GAIN} CC	-11	-	11	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Total Unadjusted Error	E_{TUE} CC	-12	-	12	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Current consumption on VDDEVRSB supply	$I_{\_VDDEVRSB}$ CC	-	0.8	1.55	mA	when ADC is turned on
RMS Noise	EN_{RMS} CC	-	2	3	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated
Input charge consumption per conversion[2)]	Q_{AIN} CC	-	-	19	pC	V_{ain} = $V_{DDEVRSB}$ = 5.5 V. Value applies for the first conversion after channel selection
Input charge consumption for consecutive conversions [2)]	Q_{SAMPLE} CC	-	-	2.5	pC	V_{ain} = $V_{DDEVRSB}$ = 5.5 V. Value applies for consecutive conversions, excluding the initial conversion after channel selection
Routing capacitance	C_{ROUTE} CC	-	-	3	pF	

1) A lower minimum sampling time can be chosen resulting in a degradation of the ADC performance (TUE degradation by 1LSB for $V_{DDEVRSB}$ ≤ 3.63V)

2) pad leakage current is not considered and has to be added to the ADC input current

4.18.2 SCR input structure figure

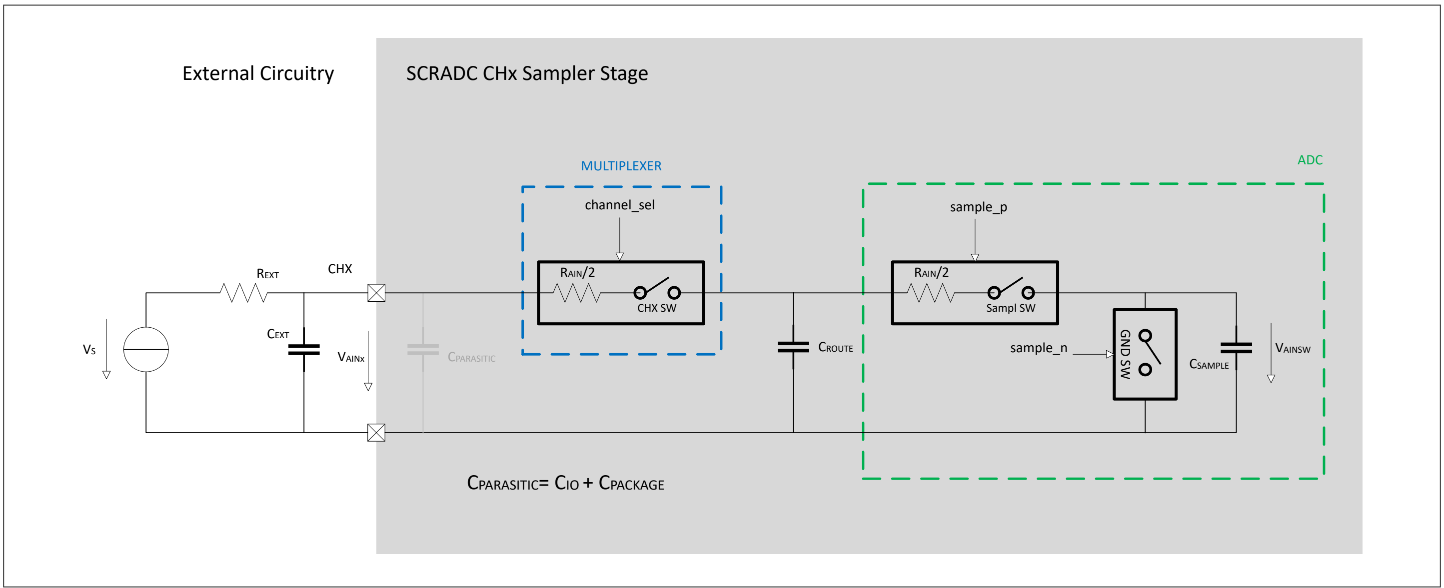


Figure 8 Equivalent circuitry for analog inputs

4.19 Temperature sensor characteristics

The temperature monitoring of the TC48x STD consists of:

- VTMON DTS
- PMS DTS

The VTMON DTS modules (VTMON.DTS[0:x]) are multiple on-chip temperature sensors at different locations across the microcontroller.

The PMS DTS is a temperature sensor dedicated for the PMS.

4.19.1 VTMON DTS characteristics

Table 75 VTMON DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	t_M *CC*	-	-	2	ms	Measured between consecutive conversions
Temperature difference between DTS instances excluding accuracy	ΔT *CC*	-3	-	3	°C	Based on Real and Max pattern distribution and thermal simulations
Inherent DTS accuracy over temperature range	T_{NL} *CC*	-1	-	1	°C	Total accuracy is defined by T_{ACC}, the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	T_{CALACC} *CC*	-2	-	2	°C	Calibration points at T_J = -40°C and T_J = 127°C
Total DTS accuracy after calibration and trimming	T_{ACC} *CC*	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$; valid for all VTMON.DTS[0:x] instances
Extended Operating temperature range only for DTS	T_{SR} *SR*	-45	-	ABS T_J (Max)	°C	Junction temperature
Thermal runaway and shutdown monitoring range[1) 2)]	T_{TSD} *CC*	-	-	ABS T_J (Max)	°C	Alarm to SMU to trigger reset

1) The operating temperature range of the device is defined and limited by the operating temperature range definition within the chapter "Operating conditions". It is not allowed to operate the device in the thermal runaway and thermal shutdown range.
2) User has to ensure that the range is adapted according to the specified operating conditions valid for its application.

Related information

PMS DTS characteristics on page 280

4.19.2 PMS DTS characteristics

Table 76 PMS DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	t_M *CC*	-	-	2	ms	Measured between consecutive conversions

(table continues...)

Table 76 (continued) PMS DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Inherent DTS accuracy over temperature range	T_{NL} *CC*	-1	-	1	°C	Total accuracy is defined by T_{ACC} , the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	T_{CALACC} *CC*	-2	-	2	°C	Calibration points at T_J = -40°C and T_J = 127°C
Total DTS accuracy after calibration and trimming	T_{ACC} *CC*	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$
Extended Operating temperature range only for DTS	T_{SR} *SR*	-45	-	165	°C	Junction temperature

Related information

VTMON DTS characteristics on page 280

4.20 Current consumption characteristics

The total power supply current defined here consists of leakage and switching components.

Application relevant values are typically lower than those given in the following tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

4.20.1 Definition of TC48x application use cases

The power pattern definition for all functional blocks is described in this section.

***Note**: The use case of a functional block may not be applicable to both (STD and COM devices). For availability of a functional block, refer to features chapter.*

Table 77 TC48x application use cases

Functional block	Real 0	Com	FreeRUN one CPU
Supply Voltage	VDDEXT, VDDEXTHS, VDDEXTDC, VDDEVRSB = 5V + 2% VDD (TYP) + 2% VDDFLEX (TYP) + 2% VDDPHPHYx and VDDPHYx are not supplied VDD Voltage Scaling active EVRC disabled	VDDEXT, VDDEXTHS, VDDEXTDC, VDDEVRSB = 3.3V + 2% VDD, VDDPHYx (TYP) + 2% VDDHSIF, VDDPHPHYx (TYP) + 2% VDD Voltage Scaling active EVRC disabled	VDDEXT, VDDEXTHS, VDDEXTDC, VDDEVRSB = 5V/3.3V + 2% VDD, VDDPHYx (TYP) + 2% VDDFLEX/VDDHSIF, VDDPHPHYx (TYP) + 2% VDD Voltage Scaling active EVRC disabled
Temperature	TJ = 150°C	TJ = 150°C	TJ = 160°C (STD) TJ = 150°C (COM)
Production Split	Respective Fast corner for SLOW and FAST splits	Respective Fast corner for SLOW and FAST splits	Respective Fast corner for SLOW and FAST splits
Integration time	20 ms	20 ms	20 ms
PACKAGE	STD	COM	
PORTS	minimal pattern activity	minimal pattern activity	
SMM	RUN1 mode	RUN1 mode	RUN1 mode
CLOCK	XTAL = 25 MHz fSYSPLL_DCO = 800 MHz fPLL0 = 400 MHz	XTAL = 25 MHz fSYSPLL_DCO = 800 MHz fPLL0 = 400 MHz	XTAL = 25 MHz fSYSPLL_DCO = 800 MHz fPLL0 = 400 MHz
Bus Interface	fSRI = fFSI2 = 400 MHz, fSPB = fFSI = 100 MHz	fSRI = fFSI2 = fCSS = 400 MHz fSPB = fFSI = 100 MHz	fSRI = fFSI2 = 400 MHz, fSPB = fFSI = 100 MHz
CPU0	CPU active at 400 MHz and executing power pattern	CPU active at 400 MHz and executing power pattern	CPU active at 400 MHz and executing power pattern
CPU1	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive

(table continues...)

Table 77 **(continued) TC48x application use cases**

Functional block	Real 0	Com	FreeRUN one CPU
CPU2	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive
CPU3	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive
DMA0	DMA Real pattern	DMA Real pattern	inactive
IR	enabled	enabled	inactive
LMU	Not Available	Not Available	Not Available
NVM	Read activity from all RRAM modules with 50% dutycycle. Periodic Data RRAM write • Assumptions for the 2 x data banks: - 50% of the time in Read mode - Every 1 ms write 128B of data into each of the data banks - Rest of the time is Read-idle • Assumptions for the 2 x program banks: - 50% of the time in Read mode - Rest of the time is Read-idle	Read activity from all RRAM modules with 50% dutycycle. Periodic Data RRAM write • Assumptions for the 2 x data banks: - 50% of the time in Read mode - Every 1 ms write 128B of data into each of the data banks - Rest of the time is Read-idle • Assumptions for the 2 x program banks: - 50% of the time in Read mode - Rest of the time is Read-idle	inactive
CSRM	CSRM CPU active @ 200 MHz executing power pattern with 60% activity RNG and PKC active	CSRM CPU active @ 200 MHz executing power pattern with 60% activity RNG and PKC active	CPU inactive
CSS	inactive	SGMII AES GCM MACsec Long Frames usecase fCSS = fSRI	inactive
GETH	inactive	SGMII1 active @1Gbit/s GETH Controller @ 250 MHz	inactive
HSPHY	HSPHY inactive	HSPHY active	inactive
HSSL	inactive	inactive	inactive

(table continues...)

Table 77 (continued) TC48x application use cases

Functional block	Real 0	Com	FreeRUN one CPU
xSPI	inactive	active 100 Mbaud	inactive
DRE	inactive	SGMII1 active @ 1 Gbit/s DRE active, Ethernet CAN routing fDRE = fSRI	inactive
SDMMC	inactive	inactive	inactive
CAN	4 modules active fCAN = 160 MHz	4 modules active fCAN = 160 MHz	inactive
CAN XL	inactive	inactive	inactive
ERAY	inactive	ERAY0 active fERAY = 80 MHz	inactive
LETH	1 x LETH0 channels active 1 x RMII mode fLETH = fSRI/4	2x LETH0 channels active 2 x RMII mode fLETH = fSRI/4	inactive
ASCLIN	4 modules active fASCLINF/S = 200/160 MHz	8 modules active fASCLINF/S = 200/160 MHz	inactive
SENT	inactive	inactive	inactive
PSI5	inactive	inactive	inactive
PSI5S	inactive	inactive	inactive
MSC	inactive	inactive	inactive
QSPI	4 modules active fQSPI = 200 MHz	6 modules active fQSPI = 200 MHz	inactive
I2C	1 modules active fI2C = 66.6 MHz	1 modules active fI2C = 66.6 MHz	inactive
VTMON	All DTS instances active	All DTS instances active	inactive
Logic TEST	inactive	inactive	inactive
VMT	inactive	inactive	inactive
SCR	inactive	inactive	inactive
PMS, SCU	default reset state	default reset state	default reset state
WTU	inactive	inactive	inactive
SMU	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled
FCE	Not Available	Not Available	Not Available

(table continues...)

Table 77 (continued) TC48x application use cases

Functional block	Real 0	Com	FreeRUN one CPU
eGTM	3TIM + 3TOM+ 3ATOM active f eGTM = 200/400 MHz	3TIM + 3TOM+ 3ATOM active f eGTM = 200/400 MHz	inactive
GPT12	2 modules active	2 modules active	inactive
GST	Not Available	Not Available	Not Available
ADC.TMADC	2 modules active f TMADC = 160 MHz	3 modules active f TMADC = 160 MHz	inactive
ADC.DSADC	Not Available	Not Available	Not Available
ADC.CDSP	inactive	inactive	inactive
DEBUG	inactive	inactive	inactive
SGBT & TRACE[1)]	inactive	inactive	inactive
Audio	inactive	inactive	inactive

1) In case of SGBT or TRACE usage a current adder of 160 mA typ. on VDD rail has to be considered. The current consumption is generated by the trace pattern 2POBs+2SRIBOBs.

Note: *Modules which are inactive are clock-gated by setting respective module clock control register CLC.DISS = 0x1.*

Related information

Current consumption and power dissipation overview in RUN mode on page 285
Respective supply rail currents in RUN mode on page 286
Current consumption in SLEEP and STANDBY modes on page 287
Load Transients on page 289

4.20.2 Current consumption and power dissipation overview in RUN mode

Table 78 Current consumption and power dissipation overview in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sum of all currents with DC-DC EVRC regulator active	$I_{DDTOTDC}$ *CC*	-	-	600[1)]	mA	Real0 power pattern; T_J = 150°C; $V_{DDEXTDC}$ = 5V; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%
Maximum power dissipation	*PD SR*	-	-	2400	mW	Real0 power pattern; T_J = 150°C; $V_{DDEXTDC}$ = 5V; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%

1) $I_{DDTOTDC} = I_{DCNL}$ (EVRC) (Max) + I_{DDEXT} (Max) + $I_{DDEXTHS}$ (Max) + I_{DDM} (Max) + $I_{DDEVRSB}$ (Max) + I_{DDFLEX} (Max) + [(I_{DD} (Max) * V_{DD}) / ($V_{DDEXTDC}$ * 72% Efficiency)]

Related information

Definition of TC48x application use cases on page 282
Respective supply rail currents in RUN mode on page 286
Current consumption in SLEEP and STANDBY modes on page 287
Load Transients on page 289

4.20.3 Respective supply rail currents in RUN mode

Table 79 Respective supply rail currents in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD supply rail currents						
Sum of I_{DD} core supply currents (incl. I_{DD_LEAK}+ I_{DD_DYN})	I_{DD} *CC*	-	-	2000	mA	Freerun power pattern with CPU0 (@max IPC) active; T_J = T_J (Max); V_{DD} (Typ) + 2%
		-	-	1980	mA	Real0 power pattern; T_J = 150°C; V_{DD} (Typ) + 2%
VDDEVRSB supply rail currents						
$I_{DDEVRSB}$ supply current (incl. leakage)	$I_{DDEVRSB}$ *CC*	-	-	30	mA	Freerun power pattern; T_J = T_J (Max); $V_{DDEVRSB}$ (Typ) + 2%
VDDEXT/VDDEXTHS supply rail currents						
I_{DDEXT} / $I_{DDEXTHS}$ supply current (incl. leakage and $I_{IEXTLVDS}$)	I_{DDEXT} *CC*	-	-	54 1) 2)	mA	Real0/1 power pattern; T_J = T_J (Max); V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%
VDDFLEX / VDDHSIF (if applicable) supply rail currents						
I_{DDFLEX} supply current (incl. leakage)	I_{DDFLEX} *CC*	-	-	3	mA	Real0 power pattern; T_J = T_J (Max); V_{DDFLEX} (Typ) + 2%
VDDM supply rail currents						
I_{DDM} supply current (incl. leakage)	I_{DDM} *CC*	-	-	25	mA	Real0 power pattern; T_J = T_J (Max); V_{DDM} (Typ) + 2%
VDDPHPHYx supply rail currents						
$I_{DDPHPHYx}$ supply current (incl. leakage)	$I_{DDPHPHYx}$ *CC*	-	-	3	mA	Freerun power pattern; T_J = T_J (Max); $V_{DDPHPHY}$ (Typ) + 2%; HSPHY disabled
VDDPHYx supply rail currents						
I_{DDPHYx} supply current (incl. I_{DDPHYx_LEAK} + I_{DDPHYx_DYN})	I_{DDPHYx} *CC*	-	-	60	mA	Freerun power pattern; T_J = T_J (Max); V_{DDPHY} (Typ) + 2%

1) IDDEXT includes total NVM current
2) Until cold PORST is released, a higher current of up to 1 mA on $I_{DDP3NVM}$ is expected during ramp-up of VDDP3NVM rail.

Related information

Definition of TC48x application use cases on page 282

Current consumption and power dissipation overview in RUN mode on page 285
Current consumption in SLEEP and STANDBY modes on page 287
Load Transients on page 289

4.20.4 Current consumption in SLEEP and STANDBY modes

Table 80 Current consumption in SLEEP and STANDBY modes

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SLEEP mode current consumption						
∑ Sum of all IDD core supply currents in SLEEP mode	I_{SLEEP} *CC*	-	-	100	mA	All CPUs in idle; All peripherals in SLEEP mode; SCR inactive; $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25°C; $V_{DDEXTDC}$ = 5 V; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DD} = 0.9 V.
∑ Sum of all currents in STANDBY0 mode drawn at VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rail	$I_{STANDBY2}$ *CC*	-	796	-	uA	64kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR XRAM not supplied; T_J = 25°C; f_{SCR} = 70 kHz; HWCFG [2:1] = [11]; High-voltage VDDEXTDC modes; All rails VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rails are supplied with $V_{DDEVRSB}$ (Typ) + 2%
		-	658	-	uA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM supplied; T_J = 25°C; f_{SCR} = 70 kHz; HWCFG [2:1] = [11]; High-voltage VDDEXTDC modes; All rails VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rails are supplied with $V_{DDEVRSB}$ (Typ) + 2%
		-	788	-	uA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM supplied; T_J = 25°C; f_{SCR} = 70 kHz; HWCFG [2:1] = [00, 01 or 10]; Low-voltage VDDEXTDC modes; All rails VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rails are supplied with $V_{DDEVRSB}$ (Typ) + 2%.
Power down current on VDDM and VAREF domain	I_{VDDM} *CC*	-	440	530	uA	T_J = 25°C; The rails VDDM and VAREF are supplied with V_{DDM} (Typ) + 2%

(table continues...)

Table 80 (continued) Current consumption in SLEEP and STANDBY modes

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY0 mode current consumption without memory retention						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{STBYPMS0}$ *CC*	-	65	-	μA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM not supplied; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDPMS0} + 4%;
STANDBY0 current consumption with memory retention (dLMU)						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{STBYPMS0}$ *CC*	-	75	-	μA	32kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR XRAM not supplied; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDPMS0} + 4%
STANDBY1 mode current consumption						
VDDPMS1 Standby domain current in STANDBY1 mode at VDDEVRSB rail	$I_{STBYPMS1}$ *CC*	-	270	-	uA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%
		-	4	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 1.25 MHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; dI_{SCR}/dt < ±500 uA
		-	10.5	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 100 MHz; T_J = T_J (Max); $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; dI_{SCR}/dt < ±3 mA
		-	6	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 20 MHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; dI_{SCR}/dt < ±3 mA

Related information

Definition of TC48x application use cases on page 282
Current consumption and power dissipation overview in RUN mode on page 285
Respective supply rail currents in RUN mode on page 286
Load Transients on page 289

4.20.5 Load Transients

Table 81 Load Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IDD core dynamic current load jump during LBIST	dI_{DDDYN_LBIST} *CC*	-300	-	600	mA	Key-on LBIST; t_r = 20 µs; t_f = 15 µs; T_{DWELL} > 20 µs; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 5%
		-600	-	800	mA	Key-off LBIST; t_r = 50 µs; t_f = 20 µs; T_{DWELL} > 20 µs; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 3%
IDD core dynamic current load jump by MBIST	dI_{DDDYN_VMT} *CC*	-330	-	330	mA	t_{MBIST} < 6ms. VMT Ganging procedure for SRAM test and initialization (definition refer to VMT chapter in User Manual); V_{DD} (Typ) - 3%
IDD core dynamic current load jump during start-up (e.g.: Supply ramp-up, Clock ramp-up, Firmware execution, Processor unit activation, PORST deassertion)	dI_{DDDYN_STRT} *CC*	-250	-	250	mA	t_r = 0.02 µs; t_f = 0.02 µs; T_{DWELL} = 100 µs; regulator untrimmed; V_{DD} (Typ) - 3%

Related information

Definition of TC48x application use cases on page 282
Current consumption and power dissipation overview in RUN mode on page 285
Respective supply rail currents in RUN mode on page 286
Current consumption in SLEEP and STANDBY modes on page 287

4.21 AC characteristics

All AC parameters are specified for the complete operating range defined in Chapter 4.4 unless otherwise noted. Unless otherwise noted, the timings are defined with the following guidelines:

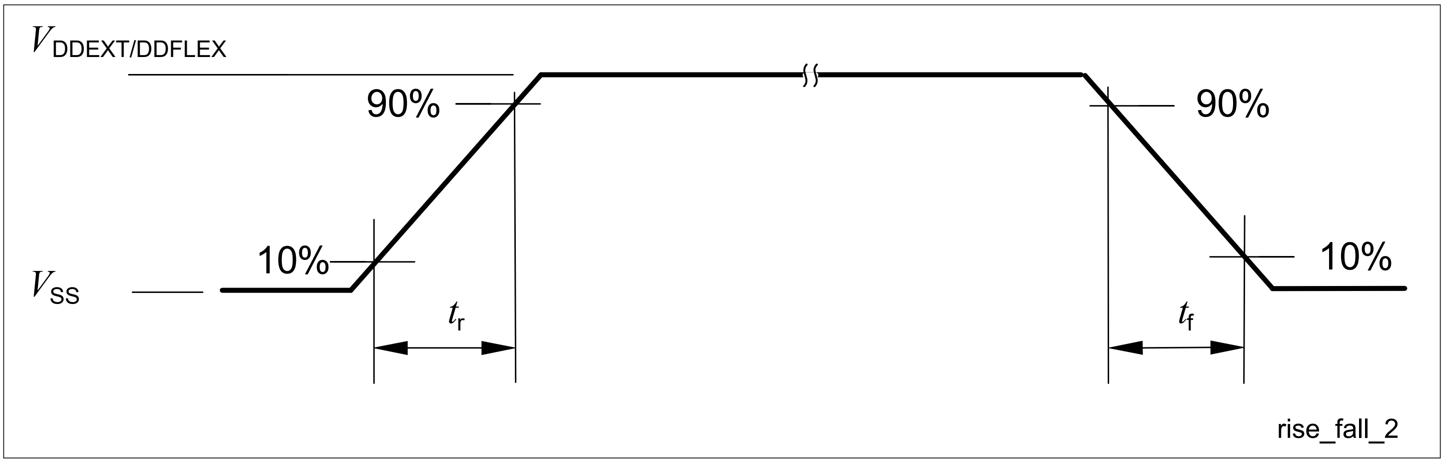


Figure 9 Definition of rise and fall times

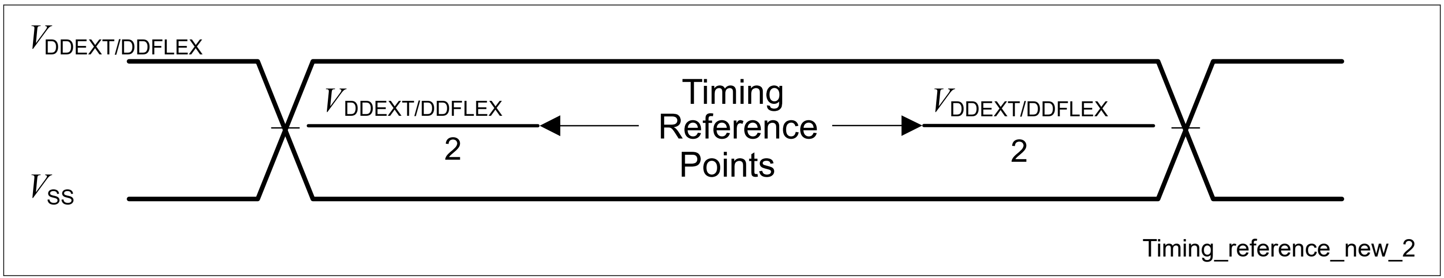


Figure 10 Time Reference Point Definition

4.22 ASCLIN SPI Master timing characteristics

This section defines the timing characteristics for the ASCLIN module in the TC48x STD. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 82 Segment definition

Segment	Ports	Module
0	Port00, Port01, Port02, Port10	ASCLIN2, ASCLIN8, ASCLIN9, ASCLIN12, ASCLIN13
1	Port13, Port14, Port15	ASCLIN0, ASCLIN1, ASCLIN7, ASCLIN10, ASCLIN19
2	Port32, Port33, Port34	ASCLIN5, ASCLIN14, ASCLIN15
3	Port22, Port23	ASCLIN4, ASCLIN6, ASCLIN16, ASCLIN17
4	Port20, Port21	ASCLIN3, ASCLIN11, ASCLIN18

4.22.1 ASCLIN Master Mode timing for strong sharp (ss) output pads

Table 83 ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	20	-	-	ns	C_L = 25 pF
Deviation from ideal duty cycle	t_{500} *CC*	-2	-	2	ns	C_L = 25 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-3.5	-	3.5	ns	C_L = 25 pF; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-5.0	-	5.0	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	C_L = 25 pF; else

(table continues...)

Table 83 (continued) ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-3	-	3.5	ns	C_L = 25 pF; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-5.0	-	5.1	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-7	-	7	ns	C_L = 25 pF; else
MRST setup to ASCLKO latching edge	t_{52} *SR*	25	-	-	ns	C_L = 25 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		29	-	-	ns	C_L = 25 pF; else
MRST hold from ASCLKO latching edge	t_{53} *SR*	-2	-	-	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-2	-	-	ns	C_L = 25 pF; else

Related information

ASCLIN Master Mode timing for strong medium (sm) output pads on page 292
ASCLIN Master Mode timing for medium (m) output pads on page 294
ASCLIN SPI Master timing figures on page 294

4.22.2 ASCLIN Master Mode timing for strong medium (sm) output pads

Table 84 ASCLIN Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	50	-	-	ns	C_L = 50 pF

(table continues...)

Table 84 (continued) ASCLIN Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Deviation from ideal duty cycle	t_{500} *CC*	-5	-	5	ns	C_L = 50 pF
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	C_L = 50 pF; else
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	C_L = 50 pF; else
MRST setup to ASCLKO latching edge	t_{52} *SR*	35	-	-	ns	C_L = 50 pF; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		36	-	-	ns	C_L = 50 pF; else
MRST hold from ASCLKO latching edge	t_{53} *SR*	-5	-	-	ns	C_L = 50 pF

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 291
ASCLIN Master Mode timing for medium (m) output pads on page 294
ASCLIN SPI Master timing figures on page 294

4.22.3 ASCLIN Master Mode timing for medium (m) output pads

Table 85 ASCLIN Master Mode timing for medium (m) output pads

Note: The following timing parameters are valid for all mappings of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	160	-	-	ns	C_L = 50 pF
Deviation from ideal duty cycle	t_{500} *CC*	-10	-	10	ns	C_L = 50 pF
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-20	-	20	ns	C_L = 50 pF
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-20	-	20	ns	C_L = 50 pF
MRST setup to ASCLKO latching edge	t_{52} *SR*	80	-	-	ns	C_L = 50 pF
MRST hold from ASCLKO latching edge	t_{53} *SR*	-13	-	-	ns	C_L = 50 pF

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 291
ASCLIN Master Mode timing for strong medium (sm) output pads on page 292
ASCLIN SPI Master timing figures on page 294

4.22.4 ASCLIN SPI Master timing figures

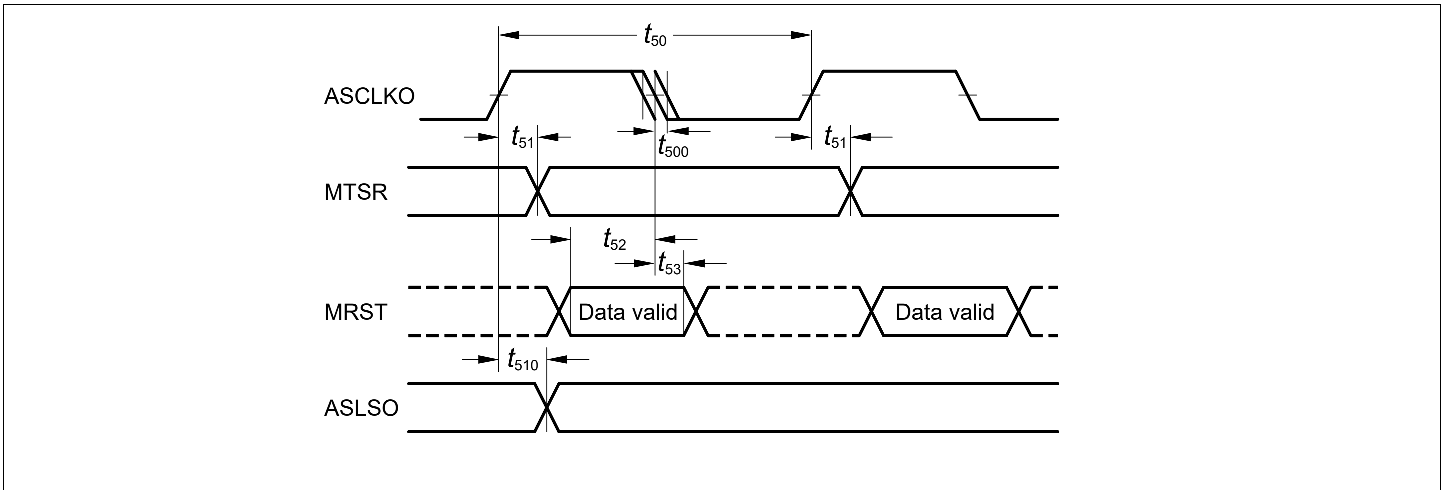


Figure 11 ASCLIN SPI Master Timing

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 291
ASCLIN Master Mode timing for strong medium (sm) output pads on page 292
ASCLIN Master Mode timing for medium (m) output pads on page 294

4.23 Inter-IC (I2C) interface timing characteristics

The I2C module of the TC48x STD supports following operating modes:

- Standard mode for speeds up to 100 kbits/s
- Fast mode for speeds up to 400 kbits/s
- High Speed mode for speeds up to 3.4 Mbits/s

***Note**: All I2C timing values are SR for Master Mode and CC for Slave Mode.*

4.23.1 I2C standard mode timing

Table 86 I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

I2C fast mode timing on page 296
I2C high speed mode timing on page 297
I2C standard and fast mode timing figures on page 298

4.23.2 I2C fast mode timing

Table 87 I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

I2C standard mode timing on page 295
I2C high speed mode timing on page 297
I2C standard and fast mode timing figures on page 298

4.23.3 I2C high speed mode timing

Table 88 I2C high speed mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Fall time of SCL	t_{11}	10[1]	-	40[1]	ns	Bus line load C_b = 100 pF
Fall time of SDA	t_{12}	10[1]	-	80[1]	ns	Bus line load C_b = 100 pF
Rise time of SCL	t_{13}	10[1]	-	40[1]	ns	Bus line load C_b = 100 pF
Rise time of SDA	t_{14}	10[1]	-	80[1]	ns	Bus line load C_b = 100 pF
Data hold time	t_3	0[1]	-	70[1]	ns	Bus line load C_b = 100 pF
Data set-up time	t_4	10[1]	-	-	ns	Bus line load C_b = 100 pF
Low period of SCL clock	t_5	160[1]	-	-	ns	Bus line load C_b = 100 pF
High period of SCL clock	t_6	60[1]	-	-	ns	Bus line load C_b = 100 pF
Hold time for the (repeated) START condition	t_7	160[1]	-	-	ns	Bus line load C_b = 100 pF
Set-up time for (repeated) START condition	t_8	160[1]	-	-	ns	Bus line load C_b = 100 pF
Set-up time for STOP condition	t_9	160[1]	-	-	ns	Bus line load C_b = 100 pF

1) Values are defined for C_b = 100 pF, for the Timing of C_b = 400 pF see the I2C Standard.

Related information

I2C standard mode timing on page 295
I2C fast mode timing on page 296
I2C standard and fast mode timing figures on page 298

4.23.4 I2C standard and fast mode timing figures

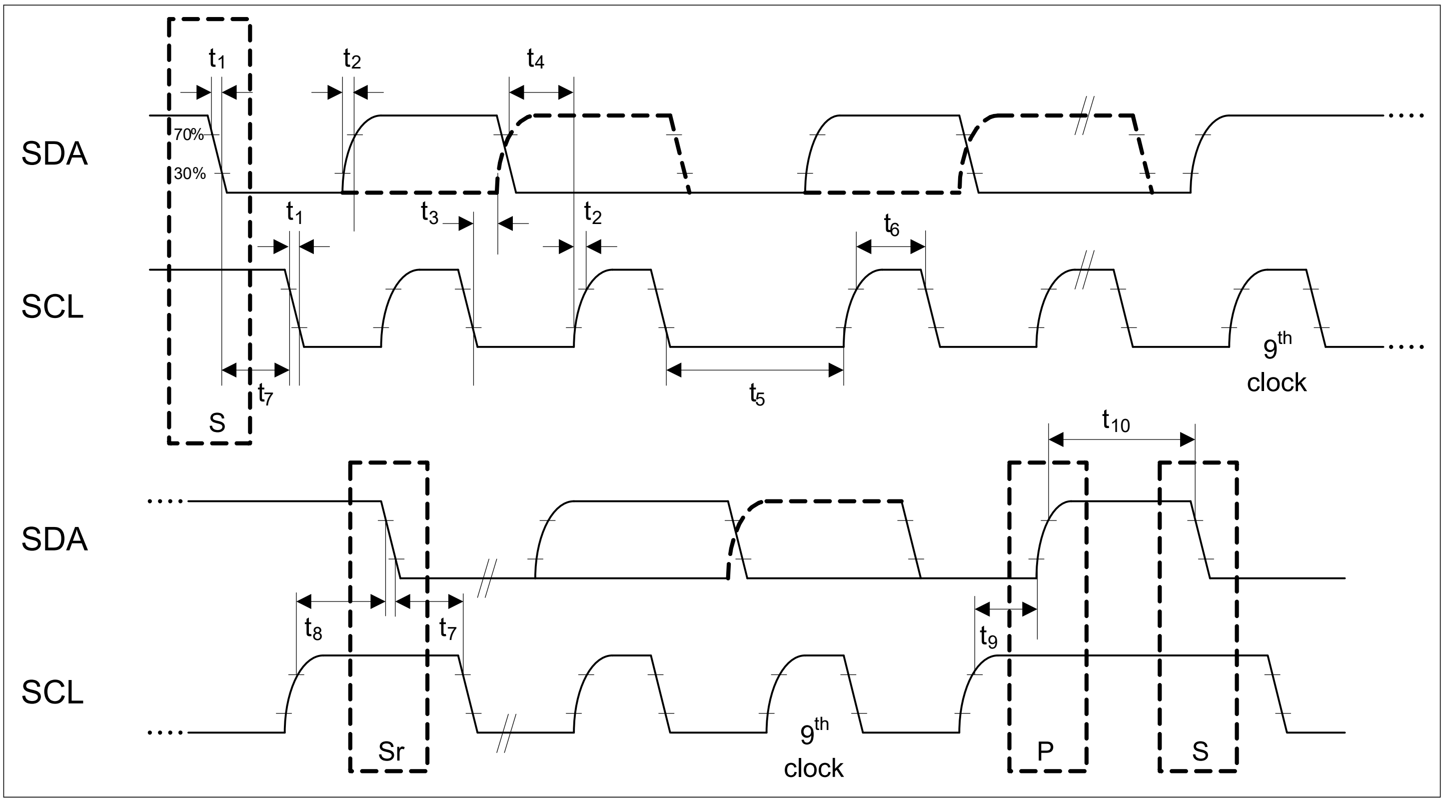


Figure 12 I2C standard and fast mode timing

Related information

I2C standard mode timing on page 295
I2C fast mode timing on page 296
I2C high speed mode timing on page 297

4.24 CAN characteristics

4.24.1 CAN internal receive delay for all pads

Table 89 CAN internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CAN RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	t_{RXD} *CC*	-	-	15 + (2*(1/ f_{MCAN}))	ns	

Related information

CAN internal transmit delay for strong sharp (ss) output pads on page 299
CAN internal transmit delay for medium (m) output pads on page 299
CAN internal transmit delay for strong medium (sm) output pads on page 300

4.24.2 CAN internal transmit delay for strong sharp (ss) output pads

Table 90 CAN internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	16	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF
		-	-	18	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	19.	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF

Related information

CAN internal receive delay for all pads on page 298
CAN internal transmit delay for medium (m) output pads on page 299
CAN internal transmit delay for strong medium (sm) output pads on page 300

4.24.3 CAN internal transmit delay for medium (m) output pads

Table 91 CAN internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	19.5	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	24.5	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 20 pF
		-	-	23	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	28	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 20 pF

Related information

CAN internal receive delay for all pads on page 298
CAN internal transmit delay for strong sharp (ss) output pads on page 299
CAN internal transmit delay for strong medium (sm) output pads on page 300

4.24.4 CAN internal transmit delay for strong medium (sm) output pads

Table 92 CAN internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	19.75	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	21.00	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF
		-	-	21.5	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	24.00	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF

Related information

CAN internal receive delay for all pads on page 298
CAN internal transmit delay for strong sharp (ss) output pads on page 299
CAN internal transmit delay for medium (m) output pads on page 299

4.25 CAN XL characteristics

4.25.1 CANXL internal receive delay for all pads

Table 93 CANXL internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CANXL RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	t_{RXD} *CC*	-	-	15 + (2*(1/ f_{CANXL}))	ns	

Related information

CANXL internal transmit delay for strong sharp (ss) output pads on page 301
CANXL internal transmit delay for medium (m) output pads on page 301
CANXL internal transmit delay for strong medium (sm) output pads on page 302

4.25.2 CANXL internal transmit delay for strong sharp (ss) output pads

Table 94 CANXL internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	16.10	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF
		-	-	16.5	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17.5	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF

Related information

CANXL internal receive delay for all pads on page 300
CANXL internal transmit delay for medium (m) output pads on page 301
CANXL internal transmit delay for strong medium (sm) output pads on page 302

4.25.3 CANXL internal transmit delay for medium (m) output pads

Table 95 CANXL internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	19	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	24	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 20 pF
		-	-	22.5	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	27	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 20 pF

Related information

CANXL internal receive delay for all pads on page 300
CANXL internal transmit delay for strong sharp (ss) output pads on page 301
CANXL internal transmit delay for strong medium (sm) output pads on page 302

4.25.4 CANXL internal transmit delay for strong medium (sm) output pads

Table 96 CANXL internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	18	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	20	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF
		-	-	19	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	22	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF

Related information

CANXL internal receive delay for all pads on page 300
CANXL internal transmit delay for strong sharp (ss) output pads on page 301
CANXL internal transmit delay for medium (m) output pads on page 301

4.26 E-Ray characteristics

The timing characteristics of following sub-chapter are valid for the driver setting = strong and edge configuration = sharp of the output drivers with a load capacitance of C_L = 25 pF.

4.26.1 Transmit characteristics

Table 97 Transmit characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}$ *CC*	-	-	9	ns	C_L = 25 pF
Fall time of TxEN	$t_{dCCTxENFall25}$ *CC*	-	-	9	ns	C_L = 25 pF
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25}$ *CC*	-	-	9	ns	20% - 80%; C_L = 25 pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}$ *CC*	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}$ *CC*	-	-	25	ns	
Asymmetry of sending	t_{tx_asym} *CC*	-2.45	-	2.45	ns	C_L = 25 pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}$ *CC*	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}$ *CC*	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sum} *CC*	-	-	9	ns	

Related information

Receive characteristics on page 303

4.26.2 Receive characteristics

Table 98 Receive characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25}$ *SR*	-30.5	-	43.0	ns	C_L = 25 pF

(table continues...)

Table 98 (continued) Receive characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15}$ *SR*	-31.5	-	44.0	ns	C_L = 15 pF
Threshold for detecting logical high	$T_{uCCLogic1}$ *SR*	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ *SR*	30	-	65	%	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ *CC*	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ *CC*	-	-	10	ns	

Related information

Transmit characteristics on page 303

4.27 QSPI timing characteristics, Master and Slave Mode

This section defines the timings for the QSPI in the TC48x STD. For the specified timing values it is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 99 Segment definition

Segment	Ports	Module
0	Port01, Port02, Port10, Port11	QSPI1, QSPI3
1	Port13, Port14, Port15	QSPI2, QSPI7
2	Port33	QSPI5
3	Port22, Port23	QSPI4, QSPI6
4	Port20, Port21	QSPI0

4.27.1 QSPI Master Mode timing characteristics

***Note**: Pad asymmetry (defined by parameter t_{TX_ASYM}) is already included in the timing characteristics that follow.*

***Note**: The following timings are only valid when the same pad type with the same speed grade configuration are used for all output signals.*

4.27.1.1 QSPI Master Mode timing for strong sharp (ss) output pads

Table 100 QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	20	-	-	ns	C_L = 25 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-2	-	2	ns	C_L = 25 pF; timing parameter is only valid for the preferred QSPI module mappings (corresponding signals mapped to those pads are marked with suffix _F)

(table continues...)

Table 100 (continued) QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-4	-	5	ns	C_L = 25 pF; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.5	-	4.5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	C_L = 25 pF; else
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-4	-	5	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.0	-	5.5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	C_L = 25 pF; else
MRST setup to SCLK latching edge	t_{52} *SR*	25[1) 2)]	-	-	ns	C_L = 25 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		26.5[1) 2)]	-	-	ns	C_L = 25 pF; else

(table continues...)

Table 100 (continued) QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MRST hold from SCLK latching edge	t_{53} *SR*	-2[1) 2)]	-	-	ns	C_L = 25 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-2[1) 2)]	-	-	ns	C_L = 25 pF; else

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong medium (sm) output pads on page 307
QSPI Master Mode timing for medium (m) output pads on page 308
QSPI Master Mode timing for LVDS output pads (clock/data) on page 309
QSPI Master Mode timing figures on page 310

4.27.1.2 QSPI Master Mode timing for strong medium (sm) output pads

Table 101 QSPI Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	50	-	-	ns	C_L = 50 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-5	-	5	ns	C_L = 50 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-10	-	10	ns	C_L = 50 pF; else
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-10	-	10	ns	C_L = 50 pF; else

(table continues...)

Table 101 (continued) QSPI Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MRST setup to SCLK latching edge	t_{52} *SR*	35[1)2)]	-	-	ns	C_L = 50 pF
MRST hold from SCLK latching edge	t_{53} *SR*	-5[1)2)]	-	-	ns	C_L = 50 pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 305
QSPI Master Mode timing for medium (m) output pads on page 308
QSPI Master Mode timing for LVDS output pads (clock/data) on page 309
QSPI Master Mode timing figures on page 310

4.27.1.3 QSPI Master Mode timing for medium (m) output pads

Table 102 QSPI Master Mode timing for medium (m) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	160	-	-	ns	C_L = 50 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-10	-	10	ns	C_L = 50 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-20	-	20	ns	C_L = 50 pF
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-20	-	20	ns	C_L = 50 pF
MRST setup to SCLK latching edge	t_{52} *SR*	80[1)2)]	-	-	ns	C_L = 50 pF
MRST hold from SCLK latching edge	t_{53} *SR*	-13[1)2)]	-	-	ns	C_L = 50 pF; QSPI; valid for identical pad types of category Fast with configuration driver = medium and edge = medium
		-13[1)2)]	-	-	ns	C_L = 50 pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 305
QSPI Master Mode timing for strong medium (sm) output pads on page 307
QSPI Master Mode timing for LVDS output pads (clock/data) on page 309
QSPI Master Mode timing figures on page 310

4.27.1.4 QSPI Master Mode timing for LVDS output pads (clock/data)

Table 103 QSPI Master Mode timing for LVDS output pads (clock/data)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	20[1]	-	-	ns	C_L = 25 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-1[1]	-	1[1]	ns	C_L = 25 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-3[1]	-	4[1]	ns	C_L = 25 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-4.0	-	10	ns	C_L = 25 pF; else
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-4[1]	-	8.0[1]	ns	C_L = 25 pF; driver strength ss
		-10[1]	-	13.5[1]	ns	C_L = 25 pF; driver strength sm
		-30[1]	-	30[1]	ns	C_L = 25 pF; driver strength m
MRST setup to SCLK latching edge	t_{52} *SR*	18[1]	-	-	ns	C_L = 25 pF; valid for LVDS Input pads only
MRST hold from SCLK latching edge	t_{53} *SR*	-1[1]	-	-	ns	C_L = 25 pF; valid for LVDS Input pads only

1) The load (C_L = 25 pF) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 305
QSPI Master Mode timing for strong medium (sm) output pads on page 307
QSPI Master Mode timing for medium (m) output pads on page 308
QSPI Master Mode timing figures on page 310

4.27.1.5 QSPI Master Mode timing figures

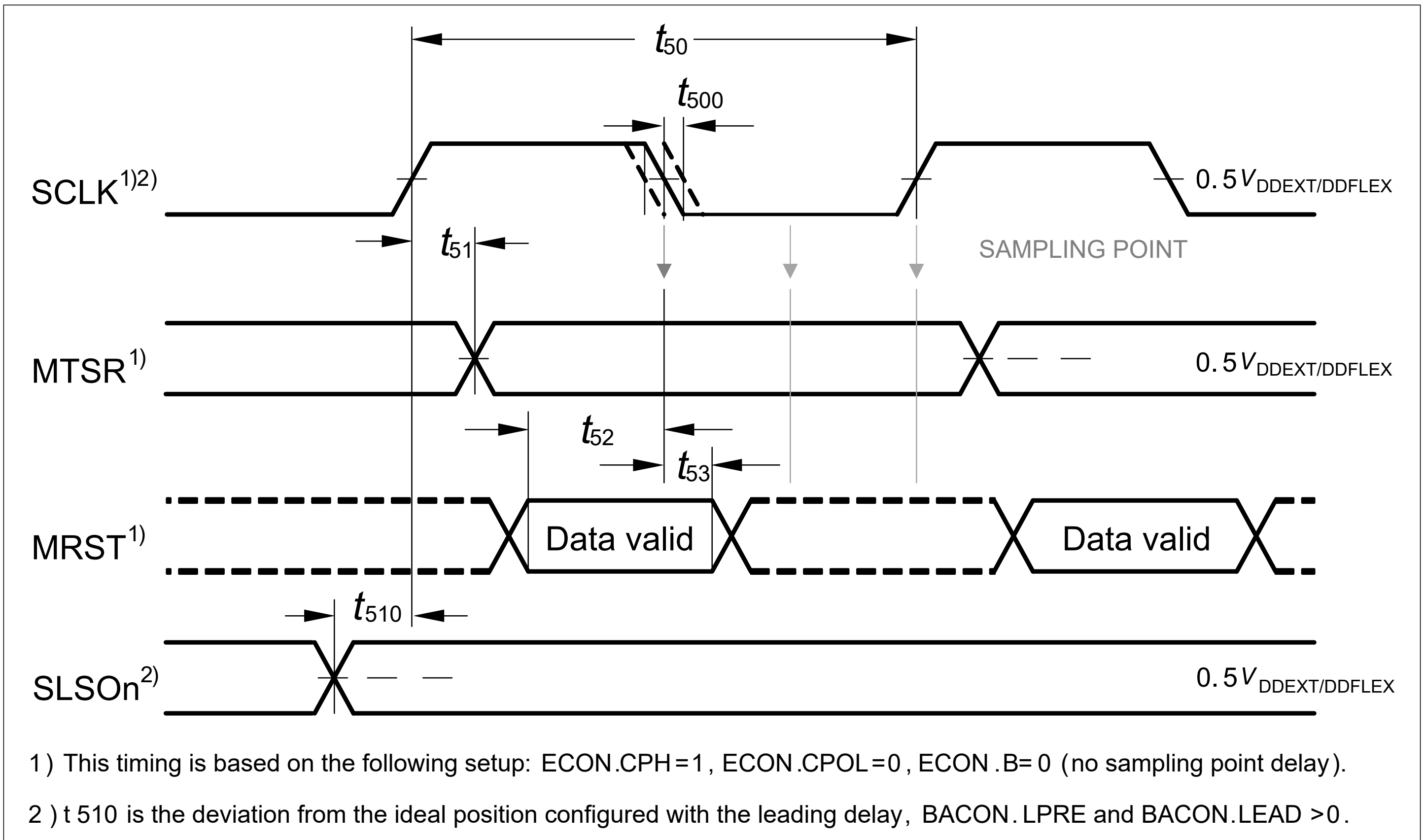


Figure 13 QSPI master mode timing

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 305
QSPI Master Mode timing for strong medium (sm) output pads on page 307
QSPI Master Mode timing for medium (m) output pads on page 308
QSPI Master Mode timing for LVDS output pads (clock/data) on page 309

4.27.2 QSPI Slave Mode timing characteristics

4.27.2.1 QSPI Slave Mode timing

Table 104 QSPI Slave Mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} *SR*	4 x T_{Max}[1)]	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ *SR*	40	-	60	%	

(table continues...)

Table 104 (continued) QSPI Slave Mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	t_{56} *SR*	6	-	-	ns	Input Level AL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		11.5	-	-	ns	Input Level AL; else
		6	-	-	ns	Input Level TTL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		11	-	-	ns	Input Level TTL; else
MTSR hold from SCLK latching edge	t_{57} *SR*	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} *SR*	4	-	-	ns	Input Level AL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		7.5	-	-	ns	Input Level AL; else
		6	-	-	ns	Input Level TTL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		7	-	-	ns	Input Level TTL; else
SLSI hold from last SCLK latching edge	t_{59} *SR*	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL

(table continues...)

Table 104 (continued) QSPI Slave Mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MRST delay from SCLK shift edge	t_{60} *CC*	2	-	24	ns	driver = strong, edge = sharp; C_L = 50 pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast or signals mapped to port slices within a segment
		-	-	27.5	ns	driver = strong, edge = sharp; C_L = 50 pF; else
		5	-	35	ns	driver = strong, edge = medium; C_L = 50 pF
		12	-	-	ns	medium driver; C_L = 50 pF; QSPI
		14	-	-	ns	medium driver; C_L = 50 pF; SCR SSC
		-	-	80	ns	medium driver; C_L = 50 pF

1) $T_{MAX} = 1/f_{QSPI}$ (Max)

Related information

QSPI Slave Mode timing figures on page 312

4.27.2.2 QSPI Slave Mode timing figures

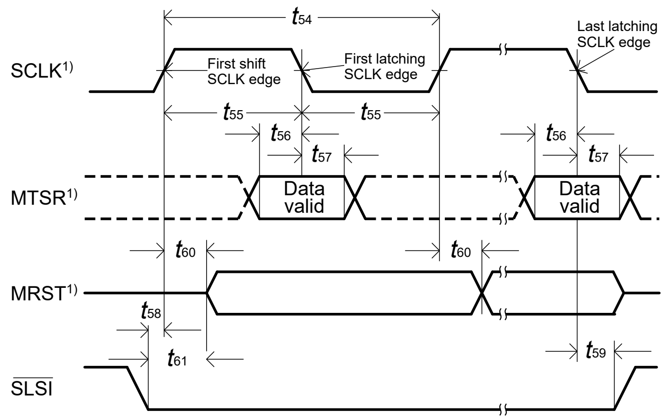


Figure 14 Slave mode timing

Related information

QSPI Slave Mode timing on page 310

4.28 SDMMC Interface timing characteristics

4.28.1 SDMMC timing

Table 105 SDMMC timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period Data Transfer Mode	t_1 *CC*	20	-	-	ns	Push-pull; $C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock period Indentification Mode	t_2 *CC*	-	-	2500	ns	Open-drain; $C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock low time	t_3 *CC*	6.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock high time	t_4 *CC*	6.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data output valid time before rising clock edge	t_5 *CC*	3	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data output valid time after rising clock edge	t_6 *CC*	3	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data input hold time	t_7 *SR*	2.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels
Data Input delay time	t_8 *SR*	-	-	13.7	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels
Data Input setup time	t_9 *SR*	5.2	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels

Related information

SDMMC timing figure on page 313

4.28.2 SDMMC timing figure

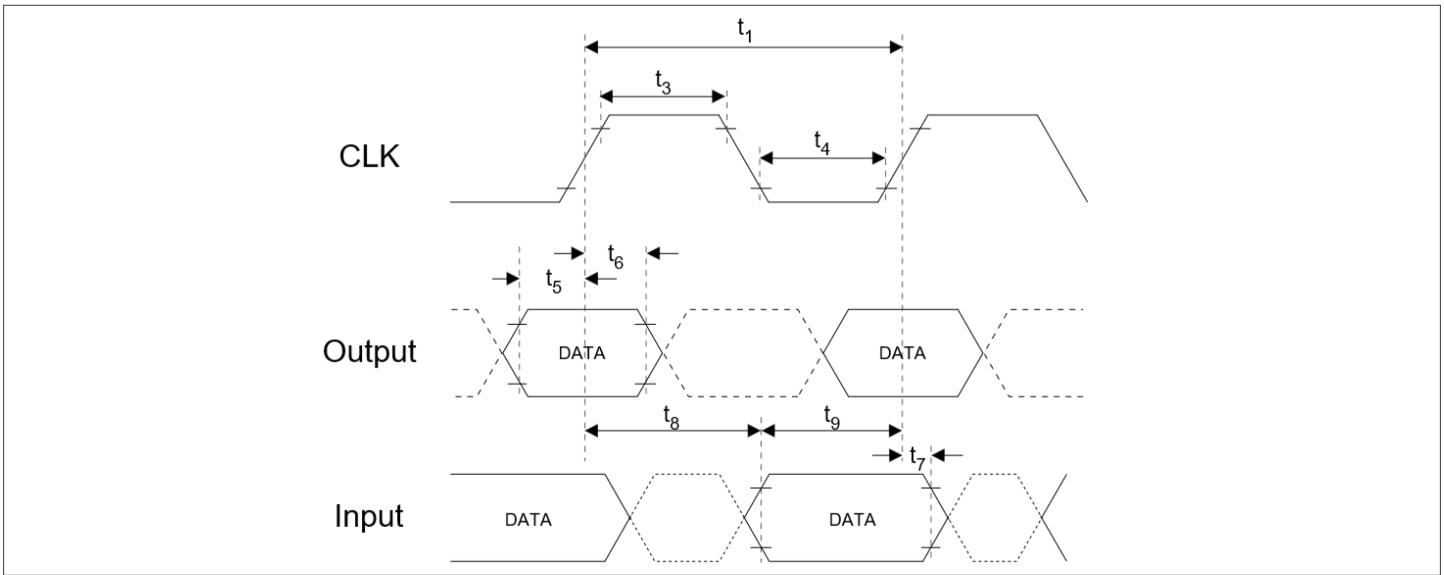


Figure 15 SDMMC Timing

Related information

SDMMC timing on page 313

4.29 HSCT characteristics

4.29.1 HSCT - Rx parasitics and loads

Table 106 HSCT - Rx parasitics and loads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Parasitic inductance budget	H_{total} *CC*	-	-	10	nH	Value is valid for the desired HSCT transmission speed of 320 Mbps. Total Budget for complete receiver, including package, pins and bond wire. The contribution of the silicon is negligible.
Capacitance total budget	C_{total} *CC*	-	-	7	pF	Total Budget for complete receiver, including silicon, package, pins and bond wire. The maximum contribution of the package to the overall budget is 3.5 pF.

Related information

HSCT - Rx/Tx setup timing characteristics on page 314
HSCT characteristics on page 315
HSCT eye diagram on page 316

4.29.2 HSCT - Rx/Tx setup timing characteristics

Table 107 HSCT - Rx/Tx setup timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Disable time of the LVDS pad	$t_{LVDSDIS}$ *CC*	-	-	20	ns	
RX o/p duty cycle	*DCrx CC*	40	-	60	%	
Wakeup time from Sleep Mode	t_{SWU} *CC*	-	-	250	ns	
RX start-up time	t_{rxi} *CC*	-	-	600	ns	Wake-up RX from power down.
TX start-up time	t_{tx} *CC*	-	-	280	ns	Wake-up TX from power down.

Related information

HSCT - Rx parasitics and loads on page 314
HSCT characteristics on page 315
HSCT eye diagram on page 316

4.29.3 HSCT characteristics

Table 108 HSCT characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Bit Error Rate based on 20 MHz reference clock at Slave PLL side	BER_{20} *CC*	-	-	10EXP-12		at 320 Mbps with 20 MHz Sysclk
Bit Error Rate based on 25 MHz reference clock at Slave PLL side	BER_{25} *CC*	-	-	10EXP-12		at 320 Mbps with 25 MHz Sysclk
Transition time from RX Disable to RX Low Speed Mode	t_{DISLS} *CC*	-	-	1000	ns	Transition time from RX Disable to RX Low Speed Mode
Transition time from RX High/Low Speed Mode to RX Medium Speed Mode	t_{HLSMS} *CC*	-	-	500	ns	Transition time from RX High/Low Speed Mode to RX Medium Speed Mode
Transition time from RX High/ Medium Speed Mode to RX Low Speed Mode	t_{HMSLS} *CC*	-	-	700	ns	Transition time from RX High/ Medium Speed Mode to RX Low Speed Mode
Transition time from TX High Speed Mode to TX Low Speed Mode	t_{HSLS} *CC*	-	-	800	ns	Transition time from TX High Speed Mode to TX Low Speed Mode
Transition time from TX Low Speed Mode to TX High Speed Mode	t_{LSHS} *CC*	-	-	500	ns	Transition time from TX Low Speed Mode to TX High Speed Mode
Transition time from RX Medium/Low Speed Mode to RX High Speed Mode	t_{MLSHS} *CC*	-	-	400	ns	Transition time from RX Medium/Low Speed Mode to RX High Speed Mode
HSCT physical layer power-on	t_{PON} *CC*	-	-	1.5	µs	HSCT physical layer power-on
Eye Opening	*EO CC*	55	-	-	%	at 320 Mbps with 25 MHz Sysclk
		55	-	-	%	at 320 Mbps with 20 MHz Sysclk

Related information

HSCT - Rx parasitics and loads on page 314
HSCT - Rx/Tx setup timing characteristics on page 314
HSCT eye diagram on page 316

4.29.4 HSCT eye diagram

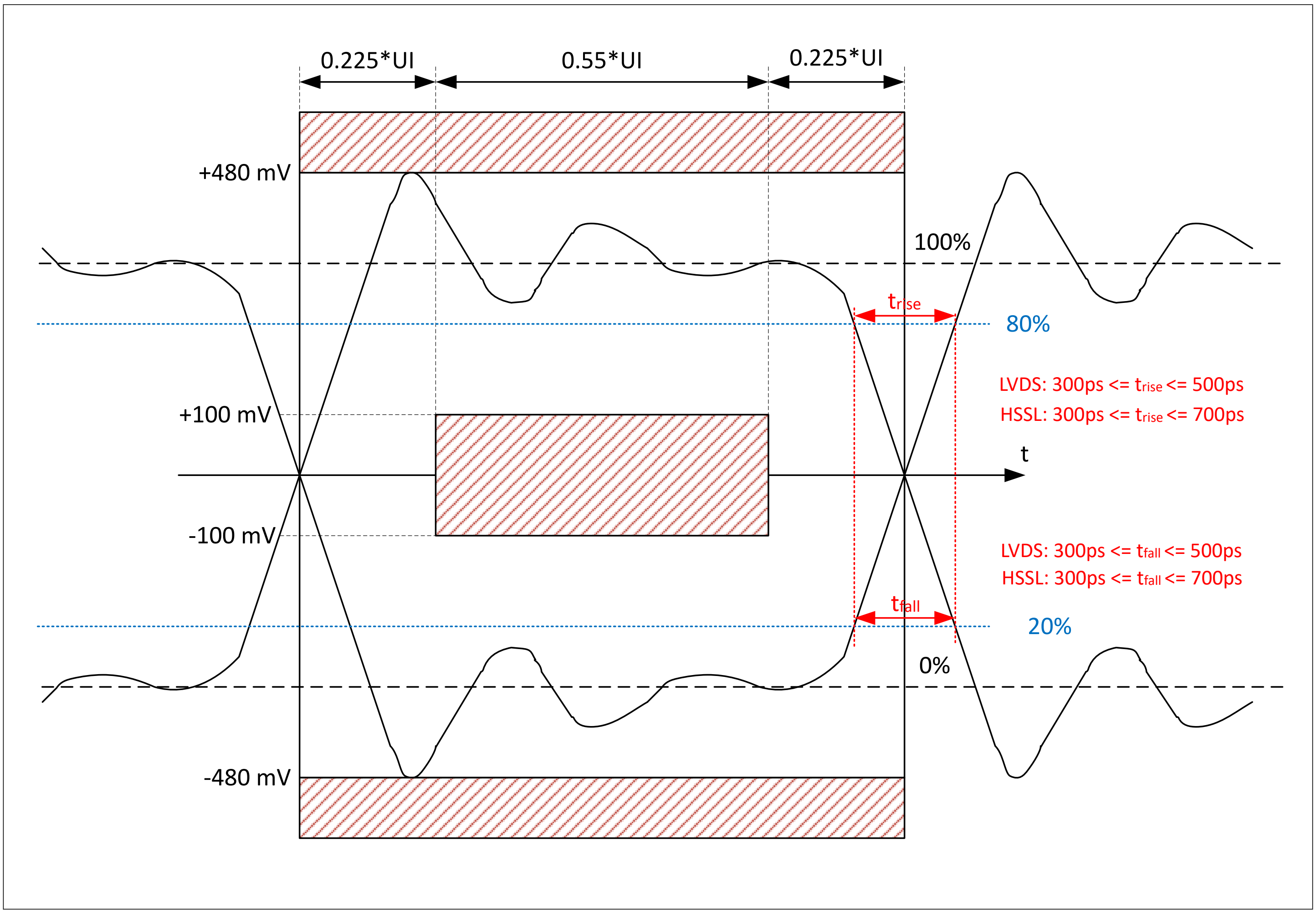


Figure 16 **HSCT eye diagram**

Related information

HSCT - Rx parasitics and loads on page 314
HSCT - Rx/Tx setup timing characteristics on page 314
HSCT characteristics on page 315

4.30 Ethernet Interface (ETH) timing characteristics

4.30.1 ETH definition of measurement reference points

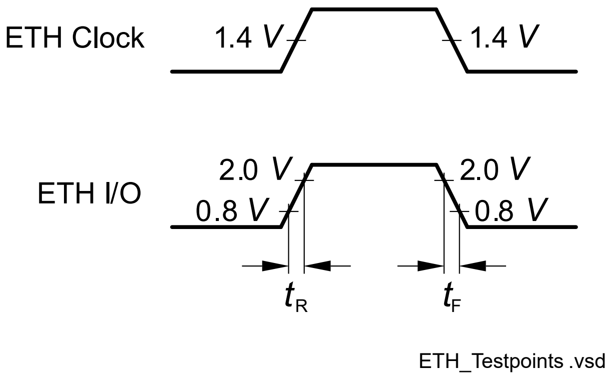


Figure 17 ETH Measurement Reference Points

4.30.2 ETH Management signal timing characteristics (ETH_MDC, ETH_MDIO)

The timing characteristics listed in the following sub-chapter are valid for the Ethernet (ETH) management signals MDC Management Data clock) and MDIO (Management Data Input/output). The following signal timings are valid for 3.3 V.

4.30.2.1 ETH management signal timing

Table 109 ETH management signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 *CC*	80	-	-	ns	C_L = 25 pF
ETH_MDC high time	t_2 *CC*	16	-	-	ns	C_L = 25 pF
ETH_MDC low time	t_3 *CC*	16	-	-	ns	C_L = 25 pF
ETH_MDIO setup time (output)	t_4 *CC*	10	-	-	ns	C_L = 25 pF
ETH_MDIO hold time (output)	t_5 *CC*	10	-	-	ns	C_L = 25 pF
ETH_MDIO data valid (input)	t_6 *SR*	0	-	20	ns	C_L = 25 pF

Related information

ETH management signal timing figures on page 318

4.30.2.2 ETH management signal timing figures

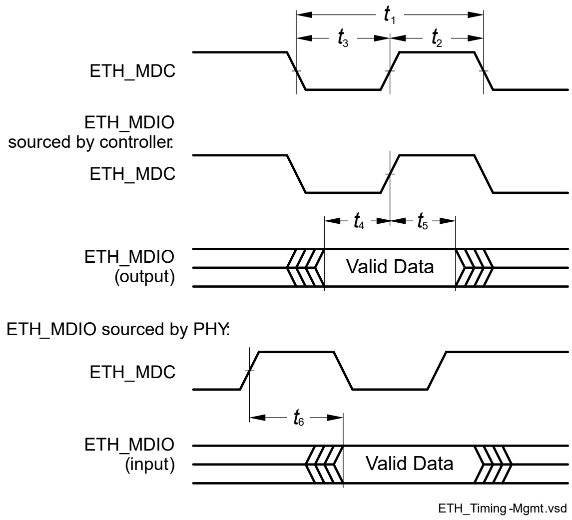


Figure 18 ETH management signal timing

Related information

ETH management signal timing on page 317

4.30.3 ETH 10BASE-T1S signal timing characteristics

In the following sub-chapter, the timing characteristics of the ETH 10BASE-T1S (Three Pin Interface) are listed.

4.30.3.1 ETH 10BASE-T1S signal timing

Table 110 ETH 10BASE-T1S signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit data '0' low duration	$t_{LowTXD0}$ *CC*	-	20	-	ns	C_L = 25 pF
Transmit data '0' high duration	$t_{HighTXD0}$ *CC*	-	60	-	ns	C_L = 25 pF
Transmit data '1' low or high duration	$t_{LowHighTXD1}$ *CC*	-	20	-	ns	C_L = 25 pF
RXD signal low pulse duration	t_{LowRXD} *SR*	12	-	-	ns	
RXD signal high pulse duration	$t_{HighRXD}$ *SR*	12	-	-	ns	
ED signal low pulse duration	t_{LowED} *SR*	21	-	-	ns	

Related information

ETH 10BASE-T1S signal timing figure on page 319

4.30.3.2 ETH 10BASE-T1S signal timing figure

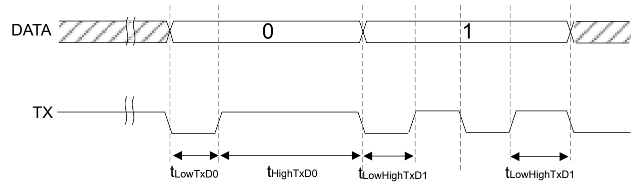


Figure 19 **10BASE-T1S Signal Timing**

Related information

ETH 10BASE-T1S signal timing on page 318

4.30.4 ETH MII timing characteristics

In the following sub-chapter, the timing characteristics of the MII (Media Independent Interface) are listed. The following signal timings are valid for 3.3 V.

4.30.4.1 ETH MII signal timing

Table 111 **ETH MII signal timing**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period	t_7 *SR*	-	40	-	ns	C_L = 25 pF; baudrate = 100 Mbps
		-	400	-	ns	C_L = 25 pF; baudrate = 10 Mbps
Clock high time	t_8 *SR*	14	-	26	ns	C_L = 25 pF; baudrate = 100 Mbps
		140[1)]	-	260[2)]	ns	C_L = 25 pF; baudrate = 10 Mbps
Clock low time	t_9 *SR*	14	-	26	ns	C_L = 25 pF; baudrate = 100 Mbps
		140[1)]	-	260[2)]	ns	C_L = 25 pF; baudrate = 10 Mbps
Input setup time	t_{10} *SR*	10	-	-	ns	C_L = 25 pF
Input hold time	t_{11} *SR*	10	-	-	ns	C_L = 25 pF
Output valid time	t_{12} *CC*	0	-	25	ns	C_L = 25 pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

Related information

ETH MII signal timing figures on page 320

4.30.4.2 ETH MII signal timing figures

Ethernet media independent interface (ETH MII) signal timing.

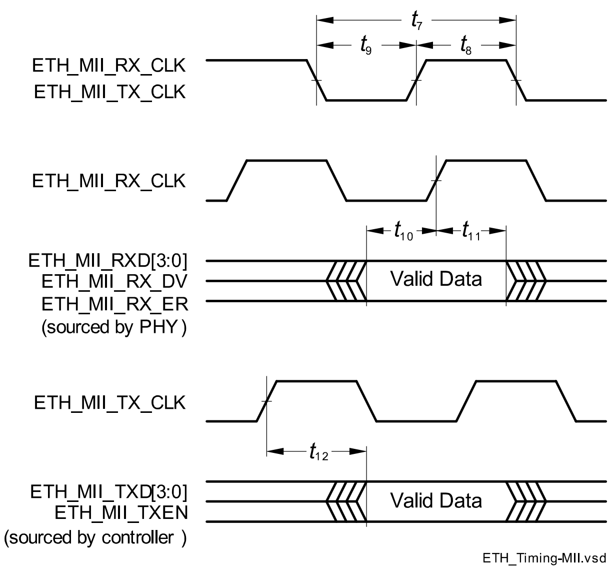


Figure 20 ETH MII signal timing

Related information

ETH MII signal timing on page 319

4.30.5 ETH RMII timing characteristics

The following sub-chapter contains the timing characteristics of the RMII (Reduced Media Independent Interface).

4.30.5.1 ETH RMII signal timing valid for 3.3V

Table 112 ETH RMII signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} *SR*	-	20	-	ns	50 ppm; C_L = 25 pF
ETH_RMII_REF_CL clock high time	t_{14} *SR*	7[1]	-	13[2]	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15} *SR*	7[1]	-	13[2]	ns	C_L = 25 pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time	t_{16} *CC*	4	-	-	ns	C_L = 25 pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time	t_{17} *CC*	2	-	-	ns	C_L = 25 pF
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18} *CC*	-	-	15.7	ns	C_L = 25 pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

Related information

ETH RMII signal timing figures on page 321

4.30.5.2 ETH RMII signal timing figures

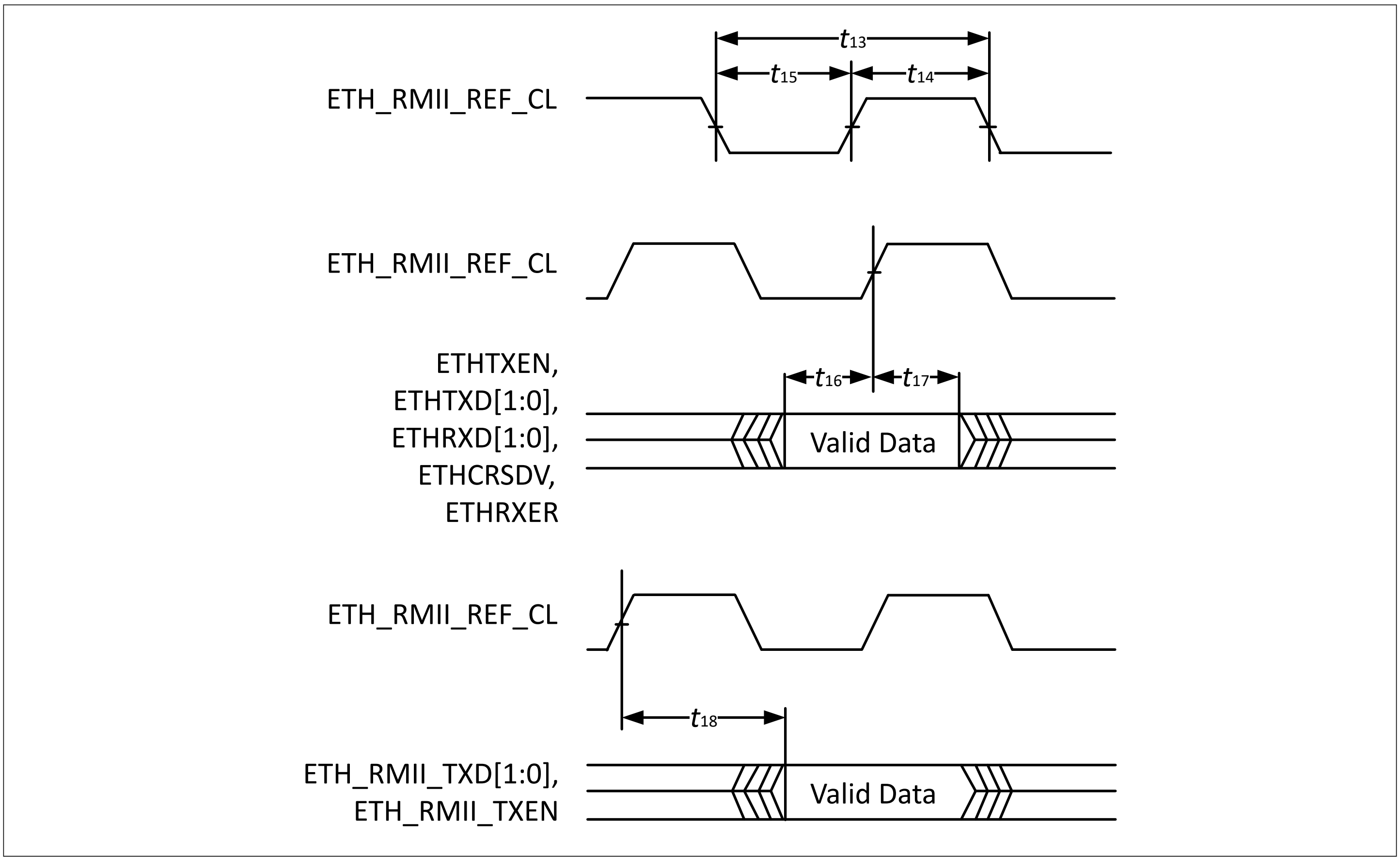


Figure 21 **ETH RMII signal timing**

Related information

ETH RMII signal timing valid for 3.3V on page 320

4.31 FSP timing characteristics

Table 113 **FSP timing characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1, respectively between FSP2 and FSP3	$t_{FSPSKEW}$ *CC*	-5	-	5	ns	C_L = 50 pF, driver = strong, edge = sharp
		-6	-	6	ns	C_L = 50 pF, driver = strong, edge = medium
		-12.5	-	12.5	ns	C_L = 50 pF, driver = medium

4.32 NVMR characteristics

Table 114 NVMR characteristics

Note: The timing values specified in the table below are valid for fFSI = 100 MHz

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data Memory Write Time per Page (8 Byte)[1) 2)]	$t_{WR\_D\_P}$ *CC*	-	150	550	µs	Typical and Max write time valid for f_{FSI} = 100 MHz
Program Memory access delay	t_{AD_P} *CC*	-	-	22.5	ns	
Data Memory access delay	t_{AD_D} *CC*	-	-	50[3)]	ns	
Tight margin read duration	$t_{TIGHT\_MARGIN\_READ}$ *CC*	-	-	10	µs	
Bank - Active to Sleep execution time	t_{BANK_SLEEP} *CC*	-	-	40	µs	
Bank - Wake up from Sleep execution time	t_{BANK_WAKEUP} *CC*	-	-	110	µs	
Program Memory Endurance per page	N_{E_P} *CC*	-	-	1000	data updates	
Data Memory Endurance per page	N_{E_D} *CC*	-	-	250000	data updates	
Program Memory Retention Time	t_{RET_P} *CC*	20	-	-	years	valid for T_J = 110 °C; valid for up to max. program memory endurance per page [4)]
Data Memory Retention Time	t_{RET_D} *CC*	20	-	-	years	valid for T_J = 110 °C [4)]
Junction temperature limit for Program Memory write operations	T_{JPMEM} *SR*	-	-	125	°C	
Write throughput for program memory[5) 2)]	$t_{WR\_throughput\_P}$ *CC*	3.2	3.2	-	Mbps	

1) This parameter is also valid for UCB
2) A maximum of four memory banks can be programmed in parallel. E.g. 4 PRRAM banks, or 3 PRRAM banks + 1 DRRAM bank, or 2 PRRAM banks + 2 DRRAM banks.
3) If f_{FSI} = f_{SRI}, the access delay increases by 10ns at f_{FSI} = 100 MHz
4) Refer to "Example temperature profiles" section for a reference temperature distribution. Customers application specific temperature profiles shall be reviewed through customer support team to ensure fulfilling targeted Retention and endurance parameters.
5) Please note that the specification is in Mbits per second, with the parameter value given per PRRAM bank. The total throughput scales with the number of PRRAM bank instances on the device as x * $t_{WR\_throughput\_P}$, where x is the number of PRRAM banks. If the device has more than four PRRAM banks, the write throughput is capped at 4 * $t_{WR\_throughput\_P}$. The given value is assuming 50% data updates in a page.

4.33 xSPI timing characteristics

4.33.1 xSPI SDR timing without data strobe

Table 115 xSPI SDR timing without data strobe

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit frequency in SDR mode	f_{TX_SDR} *CC*	-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; driver = strong, edge = sharp
Receive frequency in SDR mode	f_{RX_SDR} *CC*	-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; V_{DDEXT} = 3.3 V
Clock low to input valid timing[1)]	t_V *SR*	1	-	8	ns	Valid for Port 11 (only available in STD package variant) and Port 20; f_{RX_SDR} ≤ 25 MHz; V_{DDEXT} = 3.3 V; depending on the system load the sample delay shall be adapted by setting the corresponding value inside register RX_SAMPLE_DELAY.RSD; C_L = 15 pF
Output hold time[1)]	t_{hosdr} *CC*	2.0	-	-	ns	C_L = 15 pF
Output setup time[1)]	t_{susdr} *CC*	2.0	-	-	ns	C_L = 15 pF

1) Timing is measured at 50% of the output level

Related information

xSPI SDR without data strobe timing figure on page 323

4.33.2 xSPI SDR without data strobe timing figure

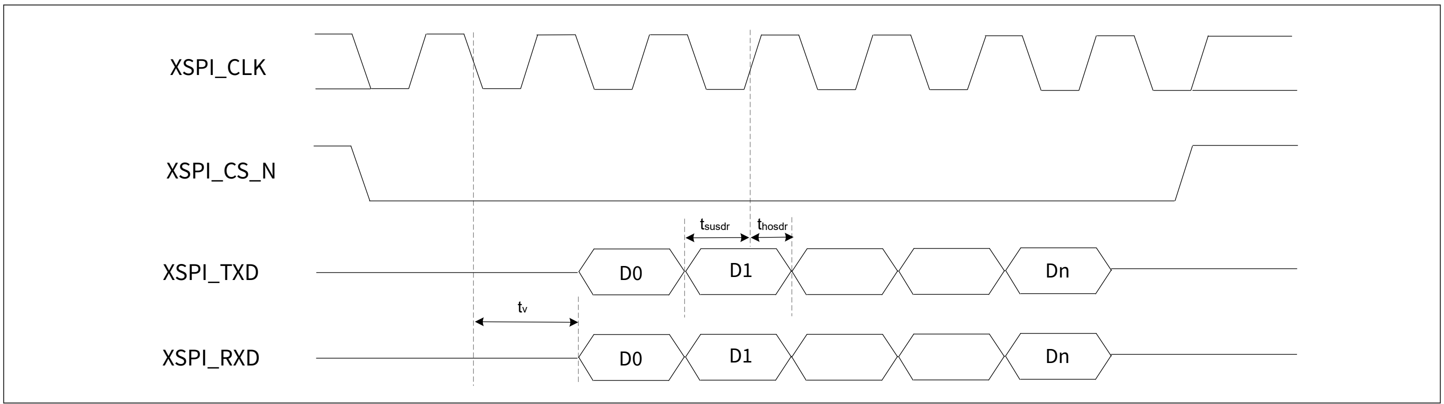


Figure 22 SDR without Data Strobe Timing

Related information

xSPI SDR timing without data strobe on page 323

4.34 DAP timing characteristics

The following characteristics are applicable for communication through the DAP debug interface.

4.34.1 DAP timing

Table 116 DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} *SR*	6.25	-	-	ns	
DAP0 high time	t_{12} *SR*	2	-	-	ns	
DAP0 low time	t_{13} *SR*	2	-	-	ns	
DAP0 clock rise time	t_{14} *SR*	-	-	1.5	ns	f = 160 MHz
		-	-	4	ns	f = 40 MHz
		-	-	2	ns	f = 80 MHz
DAP0 clock fall time	t_{15} *SR*	-	-	1.5	ns	f = 160 MHz
		-	-	4	ns	f = 40 MHz
		-	-	2	ns	f = 80 MHz
DAP1 setup to DAP0 rising edge[1)]	t_{16} *SR*	4	-	-	ns	f = 160 MHz or f = 80 MHz
		5	-	-	ns	f = 40 MHz
DAP1 hold after DAP0 rising edge	t_{17} *SR*	2	-	-	ns	
DAP1 valid per DAP0 clock period[1)]	t_{19} *CC*	3	-	-	ns	C_L = 20 pF; f = 160 MHz
		8	-	-	ns	C_L = 20 pF; f = 80 MHz
		10	-	-	ns	C_L = 50 pF; f = 40 MHz

1) Timing parameter and parameter value is also valid for the DAP2 and DAP3 lines

Related information

SCR DAP timing on page 324
DAP timing figures on page 325

4.34.2 SCR DAP timing

Table 117 SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} *SR*	50	-	-	ns	
DAP0 high time	t_{12} *SR*	15	-	-	ns	
DAP0 low time	t_{13} *SR*	15	-	-	ns	
DAP0 clock rise time	t_{14} *SR*	-	-	8	ns	f = 20 MHz
DAP0 clock fall time	t_{15} *SR*	-	-	8	ns	f = 20 MHz

(table continues...)

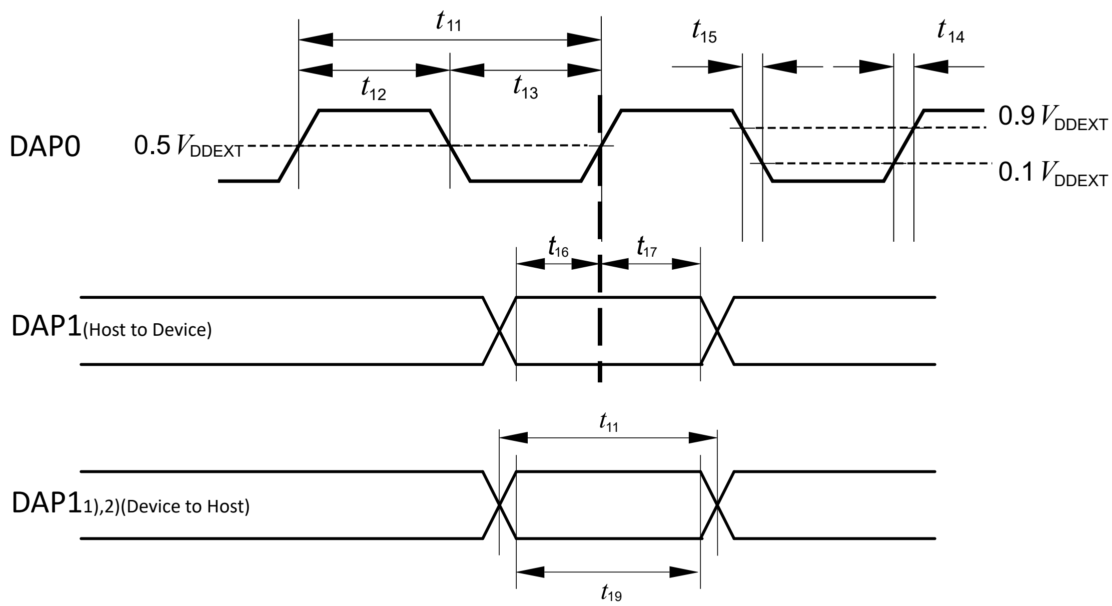
Table 117 (continued) SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP1 setup to DAP0 rising edge	t_{16} *SR*	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} *SR*	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} *CC*	30	-	-	ns	C_L = 20 pF; f = 20 MHz

Related information

DAP timing on page 324
DAP timing figures on page 325

4.34.3 DAP timing figures



1) The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

2) No explicit setup and hold times are given for DAP1 for the direction Device to Host. Only t11 and t19 are guaranteed and the tool may set the sample point freely.

Figure 23 DAP timing

Related information

DAP timing on page 324
SCR DAP timing on page 324

4.35 JTAG timing characteristics

The following characteristics are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

The explanation of the timing characteristics can be found in the 'JTAG timing figures' sub-chapter.

4.35.1 JTAG timing

Table 118 JTAG timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TCK clock period	t_1 *SR*	50	-	-	ns	
TCK high time	t_2 *SR*	10	-	-	ns	
TCK low time	t_3 *SR*	10	-	-	ns	
TCK clock rise time	t_4 *SR*	-	-	4	ns	
TCK clock fall time	t_5 *SR*	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 *SR*	10.4	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 *SR*	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 *CC*	3.0	-	-	ns	$C_L \leq 20$ pF
		-	-	26.5	ns	$C_L \leq 50$ pF
TDO hold after TCK falling edge	t_{18} *CC*	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 *CC*	-	-	28	ns	$C_L \leq 50$ pF
TDO valid output to high impedance from TCK falling edge	t_{10} *CC*	-	-	14	ns	$C_L \leq 50$ pF

Related information

JTAG timing figures on page 327

4.35.2 JTAG timing figures

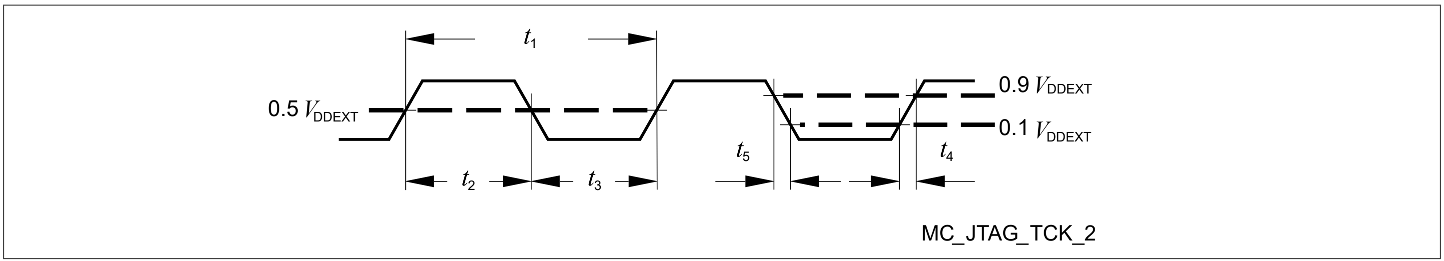


Figure 24 **Test clock timing (TCK)**

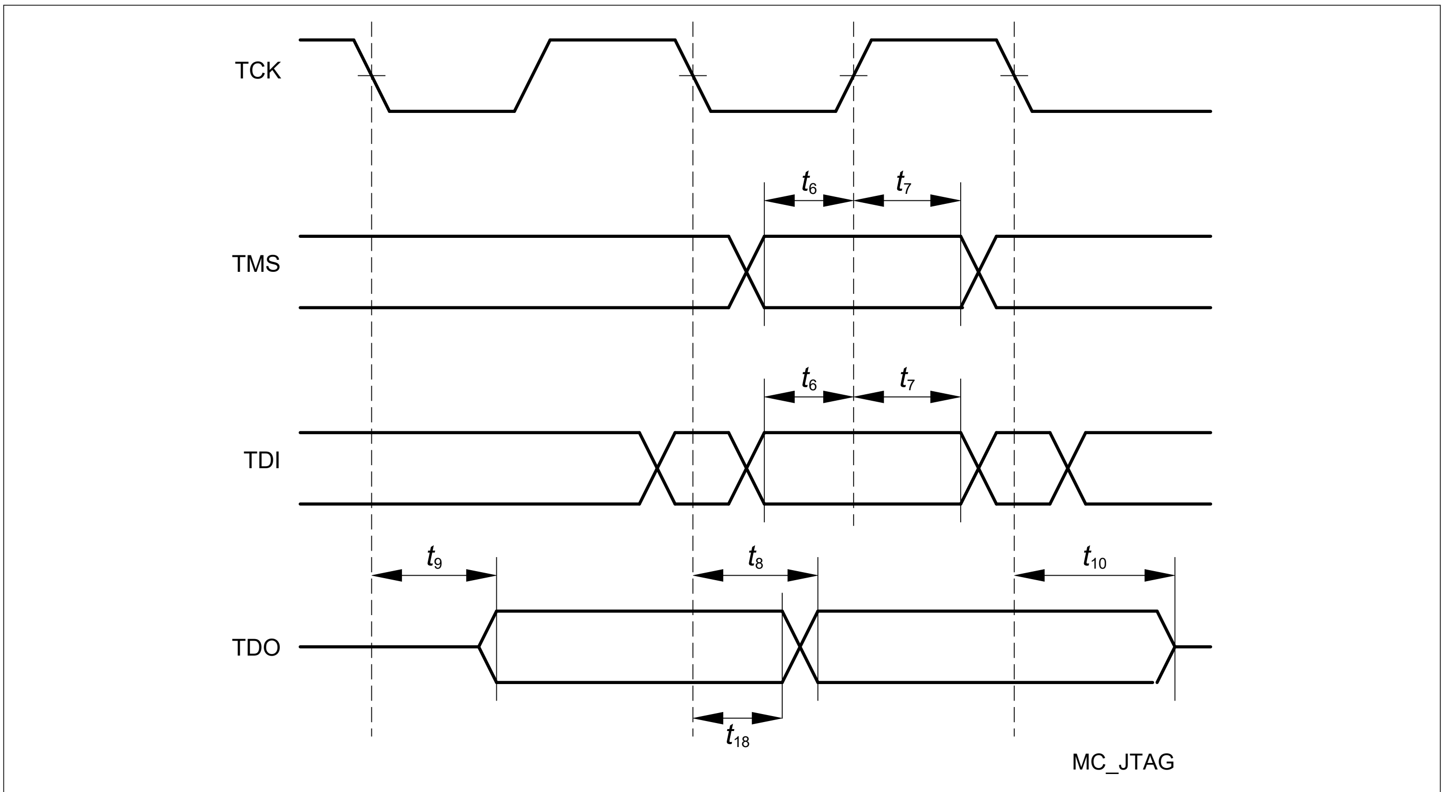


Figure 25 **JTAG timing**

Related information

JTAG timing on page 326

4.36 SGBT characteristics

SGBT is a trace interface dedicated for laboratory use only. Defined timing is only valid for laboratory conditions.

4.36.1 SGBT transmitter characteristics

Table 119 SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Differential signal characteristics						
Differential p-p voltage	$TX\_V_{diff\_pp}$ CC	600	-	1200	mV	
Differential DC impedance	$TX\_Z_{diff\_dc}$ CC	80	-	120	Ohm	
AC characteristics						
Rise time 20%-80%	TX_T_{rise} CC	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Fall time 20%-80%	TX_T_{fall} CC	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Differential skew	TX_T_{skew} CC	-	-	20	ps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	20	ps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	20	ps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
Deterministic jitter	J_D CC	-	-	0.15	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.17	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.17	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

(table continues...)

Table 119 (continued) SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total jitter	J_T *CC*	-	-	0.35	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.35	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.35	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
External AC coupling capacitance	$TX\_C_{ac\_ext}$ *SR*	75	100	200	nF	
Timing characteristics						
Data rate	*TX_DR CC*	4999.5	5000	5000.5	Mbps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		3999.6	4000	4000.4	Mbps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		1999.8	2000	2000.2	Mbps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

4.37 External components

4.37.1 HSPHY external components

Table 120 HSPHY external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High speed PHY (HSPHY) resistor reference[1)]	$R_{RESREFx}$ *SR*	194	196	198	Ohm	Resistor has to be placed between pin PHYx_RESREF and VSSPHY plane on PCB

1) Reference resistor value is valid for SGMII, PCIE and SGBT operation using the HSPHY (if functions are available).

4.37.2 Buffering and decoupling capacitors

Table 121 Buffering and decoupling capacitors

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitances on VDD pins / rail[1) 2) 3)]	C_{VDD_EXTBUF} *SR*	-	10 + 10 + 4.7	-	µF	Core supply provided externally and EVRC is off.
Capacitances on VDD pins / rail[2)]	C_{VDD_EXTDEC} *SR*	-	2x1000 +2x100 +2x47	-	nF	Capacitors placed on bottom PCB layer below center ball matrix.
Capacitances on VDDEXT pins / rail[2) 4)]	C_{VDDEXT_EXTBUF} *SR*	-	4.7	-	µF	
Capacitances on VDDEXT pins / rail[2)]	C_{VDDEXT_EXTDEC} *SR*	-	4 x 100	-	nF	
Capacitances on VDDEXTHS pins / rail[2)]	$V_{DDEXTHS\_EXTDEC}$ *SR*	-	1 x 100	-	nF	
Capacitances on VDDEXTOSC pins / rail[2)]	$C_{VDDEXTOSC\_EXTDEC}$ *SR*	-	100	-	nF	XTAL supply. Decoupling to local VSSOSC ground
Capacitances on VDDEXT pins / rail[2)]	$C_{VDDFLEX\_EXTDEC}$ *SR*	-	100	-	nF	
Capacitances on VDDEVRSB pins / rail[2)]	$C_{VDDEVRSB\_EXTDEC}$ *SR*	-	100	-	nF	
Capacitances on VDDP3NVM pins / rail[2)]	$C_{VDDP3NVM\_EXTDEC}$ *SR*	-	100	-	nF	
Capacitances on VDDEXTDC pins / rail[2) 5)]	$C_{VDDEXTDC\_EXTDEC}$ *SR*	-	100	-	nF	Capacitor can be omitted for the use cases VDDEXTDC is tied to VDDEXT and EVRC is not used.
Capacitances on each VDDMx pins / rail[2)]	C_{VDDM_EXTDEC} *SR*	-	100	-	nF	
Filter on VAREFx pins / rail[2)]	C_{VAREF_EXTFIL} *SR*	-	2.2	-	µF	Additional Resistor depending on noise and use case
Capacitances on each VDDPHPHYx pins / rail[2)]	$C_{VDDPHPHYx\_EXTDEC}$ *SR*	-	1000 + 100	-	nF	Bigger capacitor may be omitted if regulator capacitors present
Capacitances on each VDDPHYx pins / rail[2) 6)]	$C_{VDDPHYx\_EXTDEC}$ *SR*	-	2200 + 100	-	nF	Capacitors for each HSPHY unit to ensure SGMII LETH/ GETH (1Gbps) functionality. Ferrite bead is required to suppress high-frequency noise of power supply.

1) The capacitors can be omitted if additional buffer capacitors from the regulator generating the respective supply are placed close to the uC depending on load jumps, current consumption and bandwidth of the regulator.

2) The given capacitors serve as a reference example considering typical power pattern use cases and load jumps as documented in the datasheet. This is derived based on an example PCB implementation and regulator schematic scheme as shown in the figure and is verified only by simulation and validation and not characterization. The capacitances may not cover all extremities of use cases, all external regulators and components, therefore the implementation need to be additionally validated by the user together with the chosen regulators to ensure function. The tolerances of the capacitors need to be confirmed by the chosen capacitor vendor and adequate derating margins shall be applied for temperature, dc bias, lifetime and maximum continuous operation duration. Therefore

Infineon cannot take liability on capacitor performance or tolerance, PCB implementations and external regulator schemes and this needs to be ensured by the user.

3) If EVRC is used, the components specified in the EVRC regulator specification shall be considered instead.

4) If an equivalent capacitor is available from an external regulator, the capacitance is not needed.

5) Component size 0402 can be used in order to realize a capacitor placement as close as possible to the ball/pin. Other capacitance values and component sizes are also possible.

6) High-frequency noise of power supply might occur due to a noisy switch mode power supply or by sharing other supply domains with HSPHY

4.38 Quality declarations

Related information

Pin reliability in overload on page 204
Example temperature profiles on page 211

4.38.1 Quality parameters

Table 122 Quality parameters

Quality Parameters (Golden Reference)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	*MSL CC*	-	-	3		Conforming to JEDEC J-STD-020 for 260°C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} *SR*	-	-	250	V	for all balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} *SR*	-	-	1000	V	Conforming to JESD22-A114-B
Operation Lifetime	t_{OP} *CC*	-	-	24500	hour	see "Example temperature profile" as an example
Number of allowed power cycles	N_{PC} *SR*	-	-	$1.5*10^6$	cycles	

4.38.2 SRAM related fault tolerance

Table 123 SRAM related fault tolerance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum number of acceptable hard Single-Bit Errors[1)]	M_{SBE} *CC*	-	-	4		Total RAM considered SRAM_TOT = 4235 kB [1)]
Maximum number of Bitline-oriented Errors	M_{BLE} *CC*	-	-	2		

1) The parameter considers all RAMs being used by application except the ones specifically marked in the User Manual device specific VMT chapter with "Exclude from test".

5 Package information

Topics:

- PG-LFBGA-292

You can find all of the Infineon packages, types of packing and package related information, on our internet pages: www.infineon.com/products.

5.1 PG-LFBGA-292

5.1.1 PG-LFBGA-292 outline

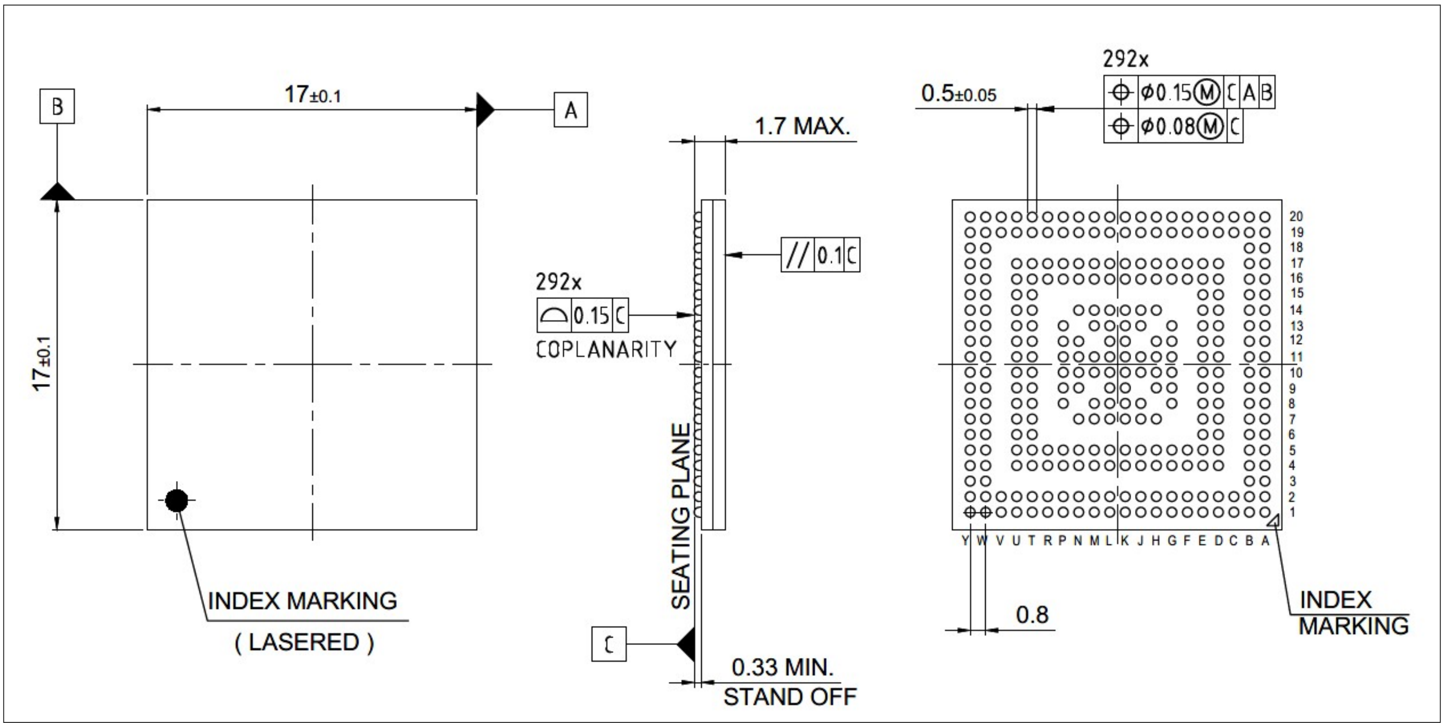


Figure 26 PG-LFBGA-292 Outline

5.1.2 PG-LFBGA-292 characteristics

Table 124 PG-LFBGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	$R_{th\text{-}JCT}$ CC	-	3.7[1)]	-	K/W	Real0 power pattern used; Uniform power distribution
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	$R_{th\text{-}JCB}$ CC	-	3.7[1)]	-	K/W	Real0 power pattern used; Uniform power distribution

(table continues...)

Table 124 (continued) PG-LFBGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_ECU}$ *CC*	-	18.25	-	K/W	Standard cooling stack and PCB considered as described in UM. Real0 Power Pattern with reduced ambient temperature T_A = 105°C.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_uC}$ *CC*	-	8.6	-	K/W	Real0 Power Pattern with reduced ambient temperature T_A = 105°C.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_ECU}$ *CC*	-	13.2	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_uC}$ *CC*	-	5	-	K/W	Real0 power pattern used.
Junction Temperature	T_{J_PKG} *SR*	-40	-	160[2)]	°C	Allowed T_J for power dissipation ≤ T_{PD}

1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (RTH_JCA, RTH_JCA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_JCA, RTH_JCA) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: (TJ = TA + RTHJA * PD), where the RTHJA is the total thermal resistance between the junction and the ambient. RTH_JCT and RTH_JCB case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). RTHJA is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.

2) Maximum allowed Power Dissipation can be estimated for different temperatures using the following equation: T_{PD} = (TPCBMax_ECU - TA_ECU) / (RthJA_x_ECU - PsiJB_x_uC CC). The production test is carried out for the maximum power dissipation PD (Max power pattern) at the corresponding reduced T_{J_PKG} temperature.

6 Revision history

Reference	Subjects (major changes since previous revision)
V 1.0, 2026-03	
	Initial version

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