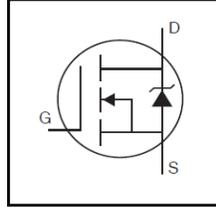


HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Enhanced dV/dT and dI/dT capability
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



| | |
|--------------------------|---------------|
| V_{DSS} | 75V |
| $R_{DS(on)}$ typ. | 2.1mΩ |
| max. | 2.6mΩ |
| I_D (Silicon Limited) | 260A Ⓞ |
| I_D (Package Limited) | 240A |



| | | |
|------|-------|--------|
| G | D | S |
| Gate | Drain | Source |

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|--------------------------|--------------------|----------|-----------------------|
| | | Form | Quantity | |
| AUIRFS3107-7TRL | D ² Pak 7 Pin | Tape and Reel Left | 800 | AUIRFS3107-7TRL |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|---------------------------|--|-------------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) | 260Ⓞ | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) | 190 | |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited) | 240 | |
| I_{DM} | Pulsed Drain Current ② | 1060 | |
| $P_D @ T_C = 25^\circ C$ | Maximum Power Dissipation | 370 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy (Thermally Limited) ③ | 320 | mJ |
| I_{AR} | Avalanche Current ② | See Fig.14,15, 22a, 22b | A |
| E_{AR} | Repetitive Avalanche Energy ② | | mJ |
| dv/dt | Peak Diode Recovery ④ | 13 | V/ns |
| T_J | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| T_{STG} | | | |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|-----------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑤⑥ | — | 0.40 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ⑤ | — | 40 | |

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

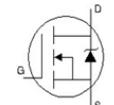
Static @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|-------|------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 75 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.083 | — | V/°C | Reference to 25°C, I _D = 5mA ② |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 2.1 | 2.6 | mΩ | V _{GS} = 10V, I _D = 160A ⑤ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Trans conductance | 260 | — | — | S | V _{DS} = 25V, I _D = 160A |
| R _G | Gate Resistance | — | 2.1 | — | Ω | |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 75V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 75V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

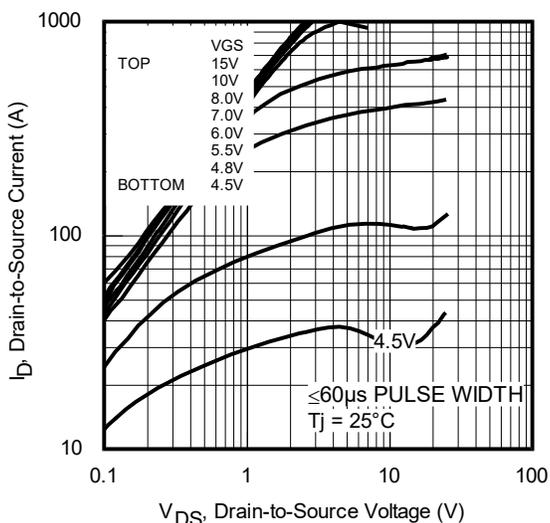
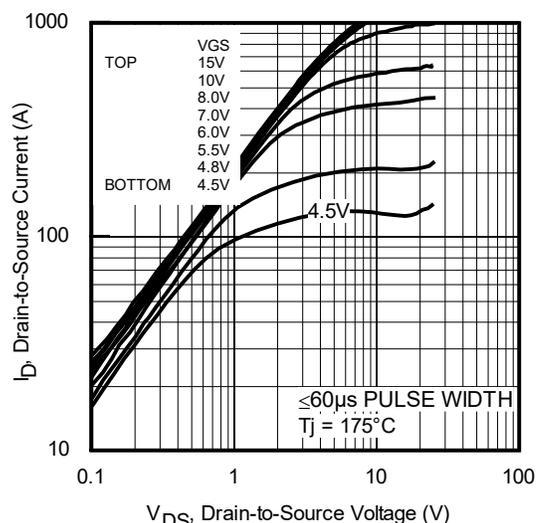
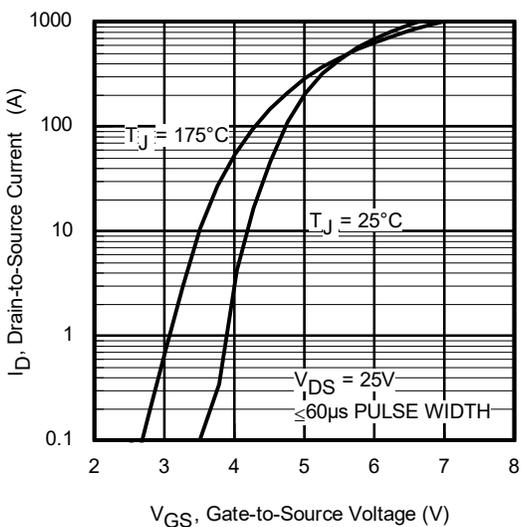
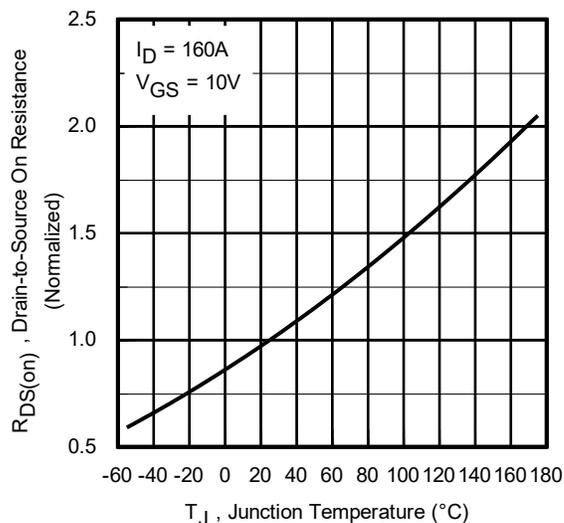
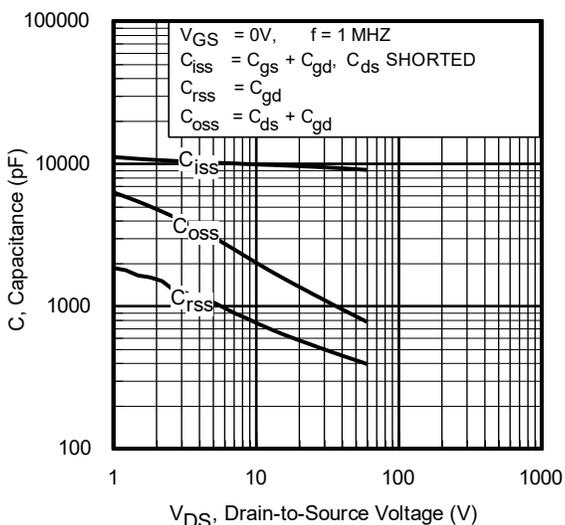
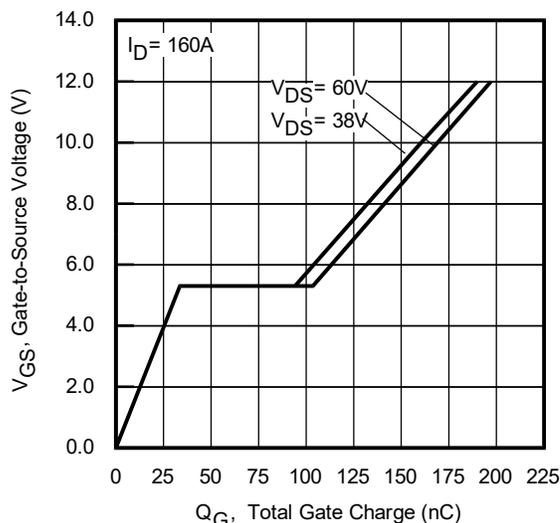
| | | | | | | |
|---------------------------|---|---|------|-----|---|--|
| Q _g | Total Gate Charge | — | 160 | 240 | nC | I _D = 160A V _{DS} = 38V V _{GS} = 10V ⑤ |
| Q _{gs} | Gate-to-Source Charge | — | 38 | — | | |
| Q _{gd} | Gate-to-Drain Charge | — | 57 | — | | |
| Q _{sync} | Total Gate Charge Sync. (Q _g - Q _{gd}) | — | 103 | — | ns | V _{DD} = 49V I _D = 160A R _G = 2.7Ω V _{GS} = 10V ⑤ |
| t _{d(on)} | Turn-On Delay Time | — | 17 | — | | |
| t _r | Rise Time | — | 80 | — | | |
| t _{d(off)} | Turn-Off Delay Time | — | 100 | — | | |
| t _f | Fall Time | — | 64 | — | pF | V _{GS} = 0V V _{DS} = 50V f = 1.0MHz |
| C _{iss} | Input Capacitance | — | 9200 | — | | |
| C _{oss} | Output Capacitance | — | 850 | — | | |
| C _{riss} | Reverse Transfer Capacitance | — | 400 | — | | |
| C _{oss eff.(ER)} | Effective Output Capacitance (Energy Related) | — | 1150 | — | | |
| C _{oss eff.(TR)} | Effective Output Capacitance (Time Related) | — | 1500 | — | V _{GS} = 0V, V _{DS} = 0V to 60V ⑥ | |

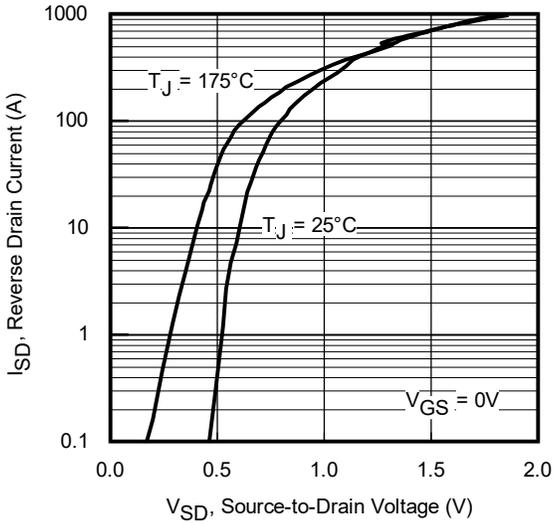
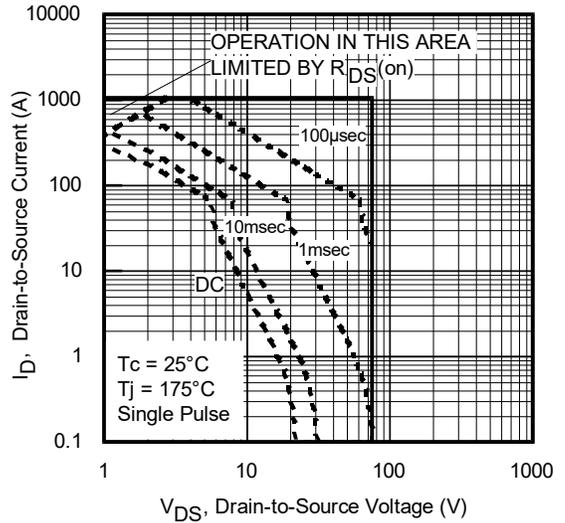
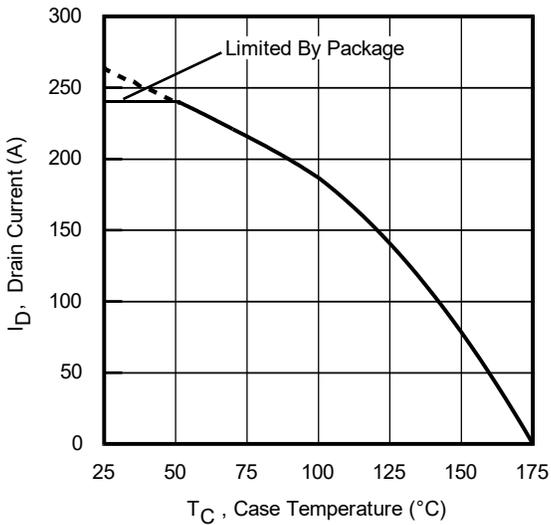
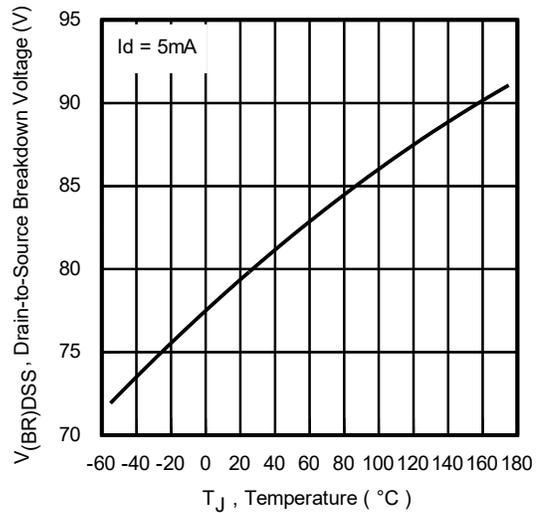
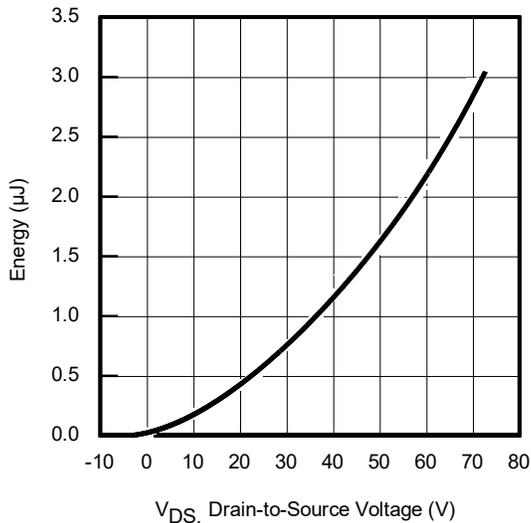
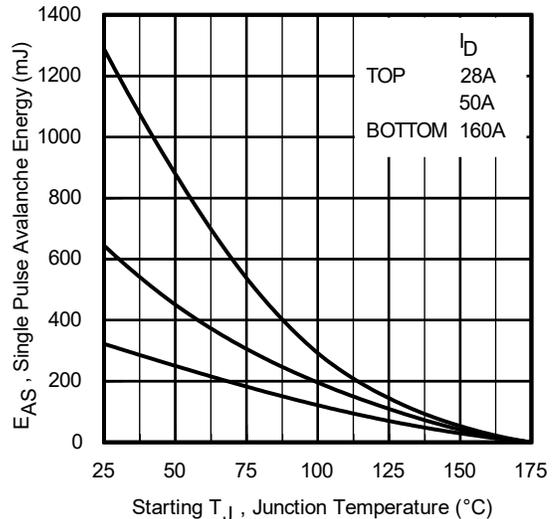
Diode Characteristics

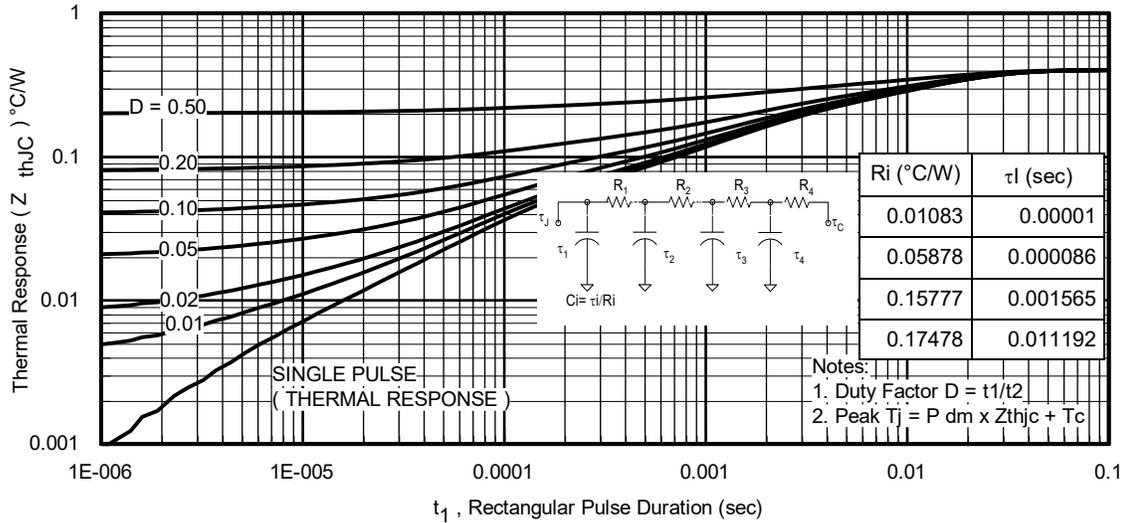
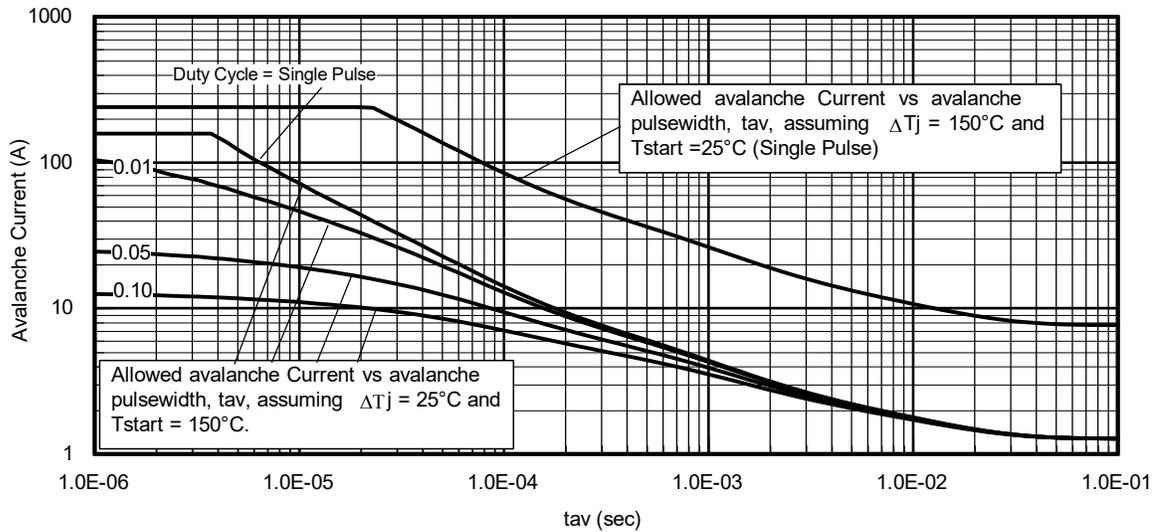
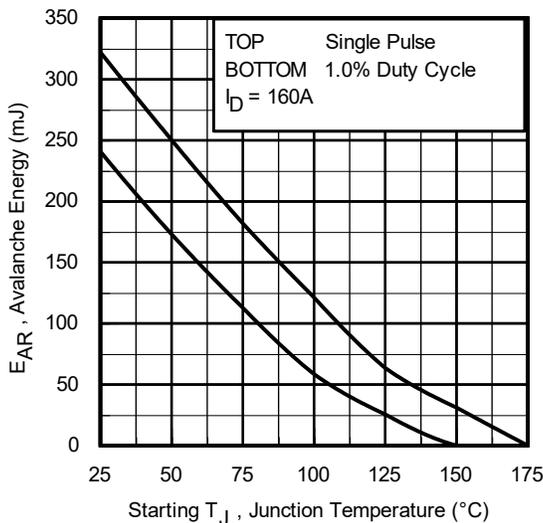
| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------|--|--|------|-------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 260 ① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ② | — | — | 1060 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 160A, V _{GS} = 0V ③ |
| t _{rr} | Reverse Recovery Time | — | 52 | — | ns | T _J = 25°C V _{DD} = 64V |
| | | — | 63 | — | | T _J = 125°C I _F = 160A, |
| Q _{rr} | Reverse Recovery Charge | — | 110 | — | nC | T _J = 25°C di/dt = 100A/μs ⑤ |
| | | — | 160 | — | | T _J = 125°C |
| I _{RSM} | Reverse Recovery Current | — | 3.8 | — | A | T _J = 25°C |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.026mH, R_G = 25Ω, I_{AS} = 160A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ I_{SD} ≤ 160A, di/dt ≤ 1420A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R_θ is measured at T_J approximately 90°C.
- ⑩ R_{θJC} value shown is at time zero


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig. 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical Coss Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Avalanche Current vs. Pulse width

**Notes on Repetitive Avalanche Curves , Figures 14, 15:
 (For further info, see AN-1005 at www.infineon.com)**

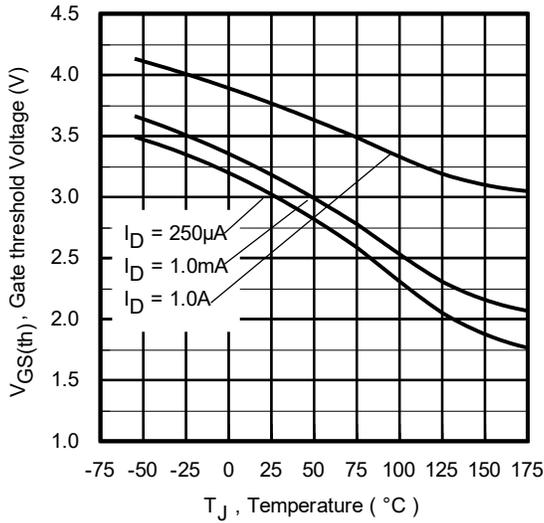
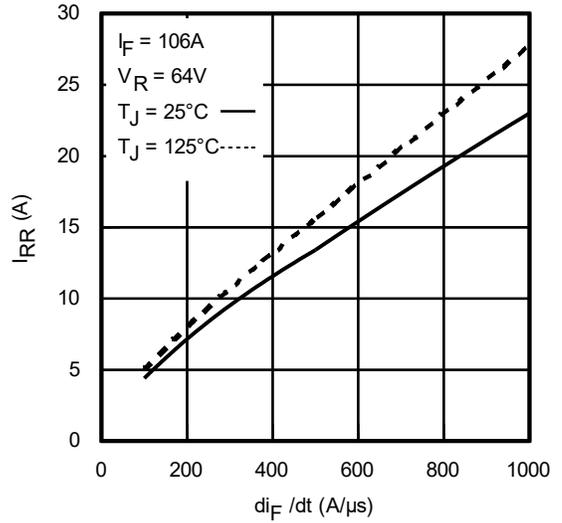
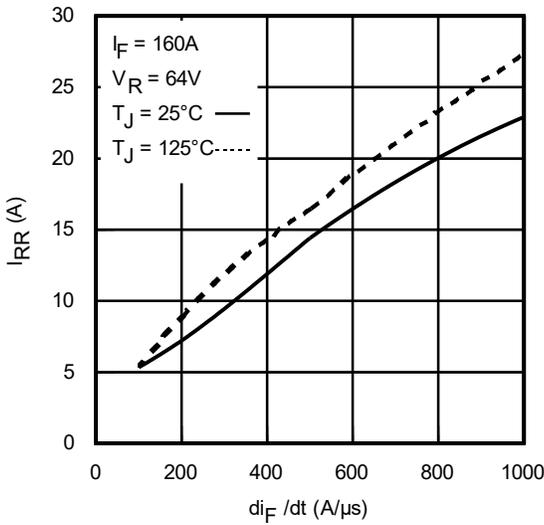
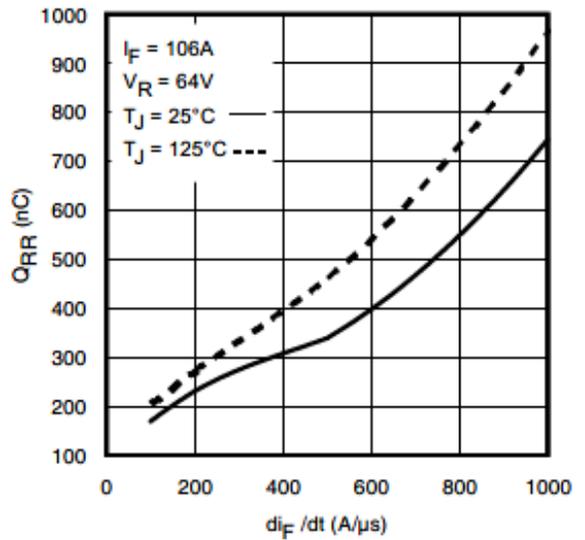
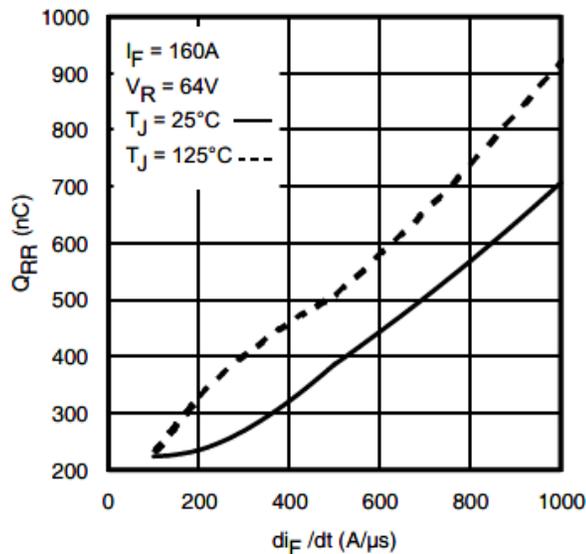
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

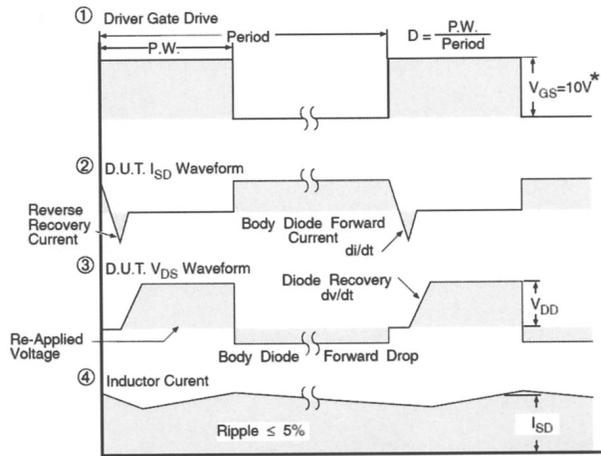
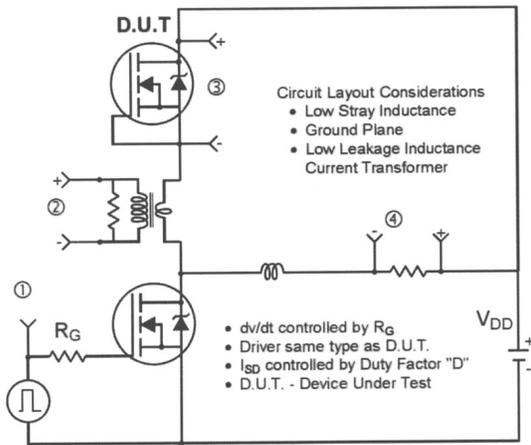
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig. 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. di_F/dt

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Stored Charge vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

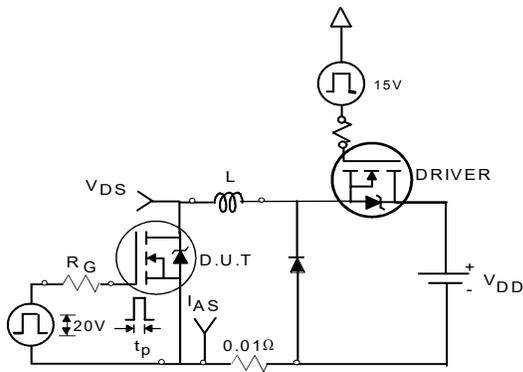


Fig 22a. Unclamped Inductive Test Circuit

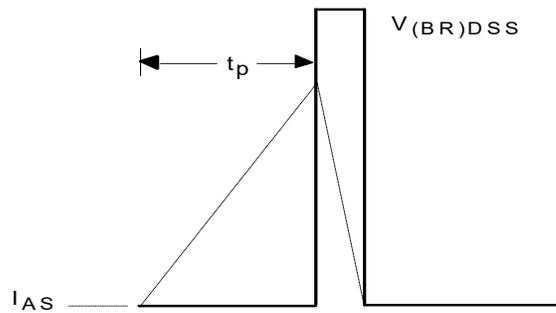


Fig 22b. Unclamped Inductive Waveforms

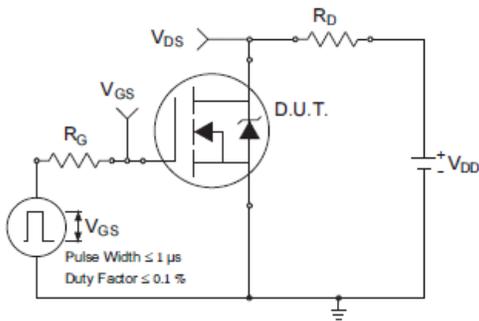


Fig 23a. Switching Time Test Circuit

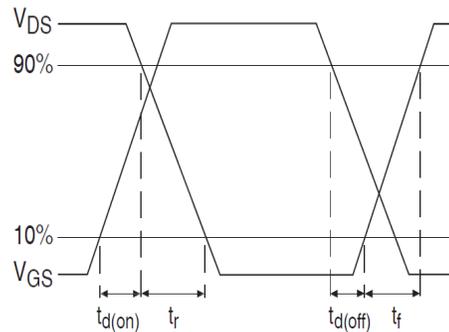


Fig 23b. Switching Time Waveforms

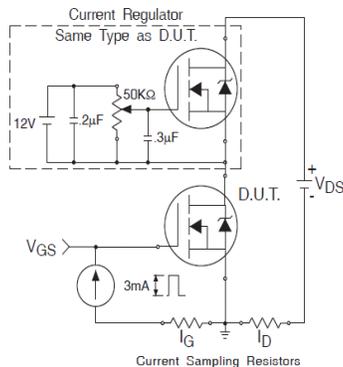


Fig 24a. Gate Charge Test Circuit

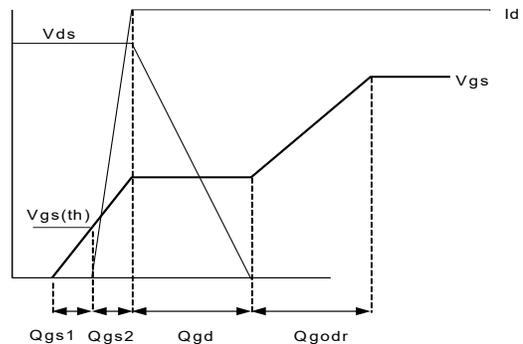
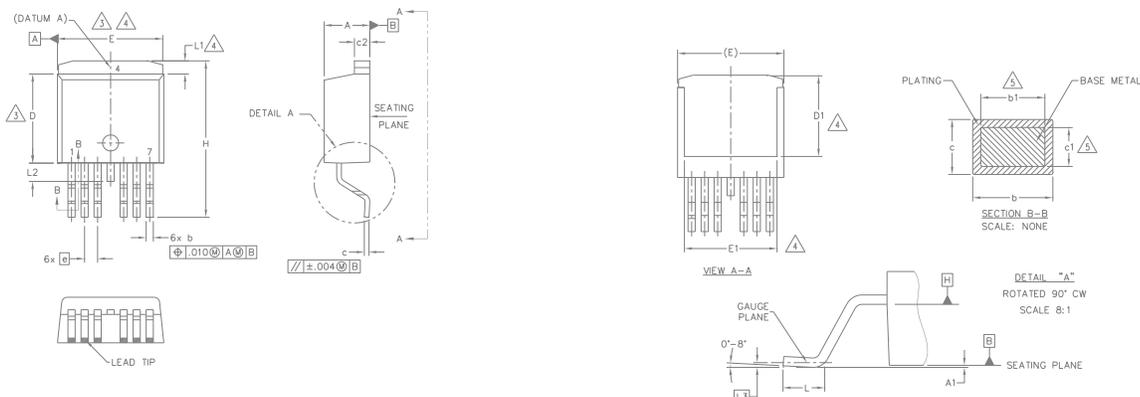


Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

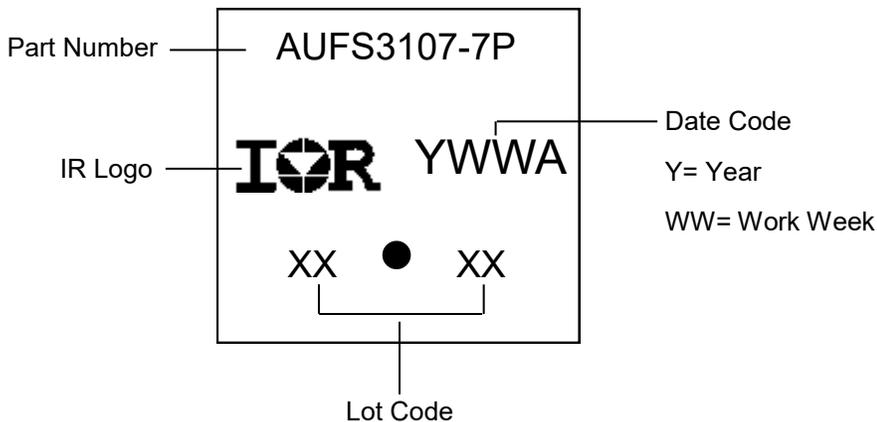


| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | — | 0.254 | — | .010 | |
| b | 0.51 | 0.99 | .020 | .036 | |
| b1 | 0.51 | 0.89 | .020 | .032 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | 7.42 | .270 | .292 | 4 |
| E | 9.65 | 10.54 | .380 | .415 | 3,4 |
| E1 | 6.22 | 8.48 | .245 | .334 | 4 |
| e | 1.27 BSC | | .050 BSC | | |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | — | 1.68 | — | .066 | 4 |
| L2 | — | 1.78 | — | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | |

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

D²Pak - 7 Pin Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak - 7 Pin Tape and Reel

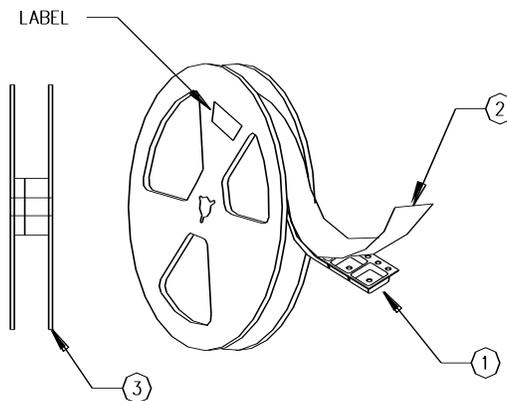
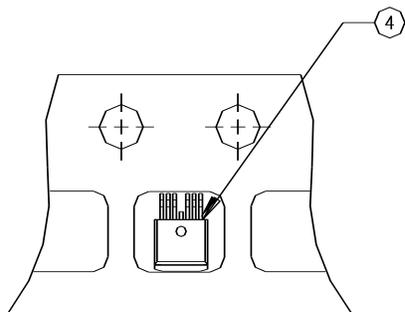
NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

| | | | |
|-----------------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | D ² -Pak 7 Pin | MSL1 |
| ESD | Machine Model | Class M4 (+/- 800V) [†] AEC-Q101-002 | |
| | Human Body Model | Class H3A (+/- 6000V) [†] AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 2000V) [†] AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

† Highest passing voltage.

Revision History

| Date | Comments |
|------------|--|
| 10/20/2015 | <ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. |
| 05/12/2025 | <ul style="list-style-type: none"> Corrected typo in Part Number |

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