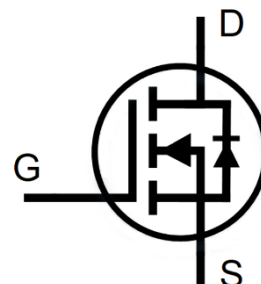


Automotive CoolSiC™ Gen2pE MOSFET

Quality Requirement Category: Automotive

Features

- Blocking voltage 750V (rated)
- Low $R_{DS(ON)}$
- Low switching losses
- Low Q_G and C_{rss}
- Extended operation at 200°C up to 100h
- Integrated gate resistor
- Easy paralleling of MOSFET
- Short circuit rugged technology



Applications

- Motor drive traction inverter

Description

- Recommended for power modules

Product Validation

- Technology qualified for automotive applications. Product validation according to AEC-Q101.

Key Performance Parameters

Chip Type	V_{DSS}	I_{DDC}	$R_{DS(on)}$	Die Size (total)
AIMC75R007D31M2P	750V	168A ^a	7.3mΩ	25mm ²

^a Chip capability with appropriate assembly. Calculated based on theoretical $R_{thJC} = 0.4$ [K/W]

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1 Maximum Ratings ^b

Parameter	Symbol	Conditions	Value	Unit
Drain-source voltage	V_{DSS}	$-40^{\circ}\text{C} \leq T_{vj} \leq 200^{\circ}\text{C}$	750	V
Continuous DC drain current, limited by $T_{vj\max}$	I_{DDC}	$V_{GS} = 18\text{V}$, $T_c = 25^{\circ}\text{C}$	131 ^c 168 ^d	A
Peak reverse drain current	I_{SM}	$V_{GS} = -3\text{V}$, $T_c = 25^{\circ}\text{C}$, $T_{\text{pulse}} = 2\mu\text{s}$	218	A
Maximum gate-source voltage	V_{GS}		-10 ... +23	V
Operating virtual junction temperature	T_{vj}	over lifetime	-40 ... +185	$^{\circ}\text{C}$
		100 hours	+185 ... +200	$^{\circ}\text{C}$

2 Recommended Values

Parameter	Symbol	Conditions	Value	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-3	V

^b Not subject to production test, verified by design/characterization.

^c Chip capability with appropriate assembly. Calculated based on theoretical $R_{thJC} = 0.66$ [K/W].

^d Chip capability with appropriate assembly. Calculated based on theoretical $R_{thJC} = 0.4$ [K/W].

3 Electrical Characteristics

Specification limits valid over product lifetime if not stated otherwise.

Parameter	Symbol	Conditions		Value			Unit
				min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{mA}$	$T_{vj} = -40^{\circ}\text{C}^{\text{e}}$	750	-	-	V
			$T_{vj} = 25^{\circ}\text{C}$	750	-	-	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	750	-	-	
Gate-source threshold voltage ^f (tested after 1ms pulse at $V_{GS} = +20\text{V}$)	$V_{GS(th)}$	$I_D = 19.9\text{mA}, V_{GS} = V_{DS}$	$T_{vj} = 25^{\circ}\text{C}$	3.5	4.1	4.7	V
			$T_{vj} = 175^{\circ}\text{C}^{\text{e}}$	2.6	3.2	3.8	
			$T_{vj} = 185^{\circ}\text{C}^{\text{e}}$	2.57	3.17	3.77	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	-	3.1	-	
Drain-source resistance	$R_{DS(on)}$	$V_{GS} = 18\text{V}, I_D = 80\text{A}$	$T_{vj} = 25^{\circ}\text{C}$	-	7.3	9.1 ^f	mΩ
						9.6	
			$T_{vj} = 175^{\circ}\text{C}^{\text{e}}$	-	11.0	13.0 ^f	
						13.3	
			$T_{vj} = 185^{\circ}\text{C}^{\text{e}}$	-	11.6	13.6 ^f	
						14.0	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	-	12.4	14.5 ^f	
						14.8	
Source-drain resistance	$R_{SD(on)}$	$V_{GS} = 18\text{V}, I_D = -80\text{A}$	$T_{vj} = 25^{\circ}\text{C}^{\text{e}}$	-	7.3	-	mΩ
			$T_{vj} = 175^{\circ}\text{C}^{\text{e}}$	-	11.0	-	
			$T_{vj} = 185^{\circ}\text{C}^{\text{e}}$	-	11.6	-	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	-	12.4	-	
Zero gate-voltage drain current	I_{DSS}	$V_{DS} = 750\text{V}, V_{GS} = 0\text{V}$	$T_{vj} = 25^{\circ}\text{C}$	-	0.9	50	μA
			$T_{vj} = 175^{\circ}\text{C}^{\text{e}}$	-	6	100	
			$T_{vj} = 185^{\circ}\text{C}^{\text{e}}$	-	6.8	114	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	-	8.3	-	
Positive gate-source leakage current	I_{GSS+}	$V_{DS} = 0\text{V}, V_{GS} = 23\text{V}$	$T_{vj} = 25^{\circ}\text{C}$	-	1	200	nA
			$T_{vj} = 175^{\circ}\text{C}^{\text{e}}$	-	4	400	
			$T_{vj} = 185^{\circ}\text{C}^{\text{e}}$	-	8	400	
			$T_{vj} = 200^{\circ}\text{C}^{\text{e}}$	-	11	-	

^e Not subject to production test, verified by design/characterization.

^f Values specified for zero hour not according to AEC-Q101.

Parameter	Symbol	Conditions		Value			Unit
				min.	typ.	max.	
Negative gate-source leakage current	I_{GSS-}	$V_{DS} = 0V$, $V_{GS} = -10V$	$T_{vj} = 25^{\circ}C$	-	0.1	100	nA
			$T_{vj} = 175^{\circ}C^g$	-	0.4	100	
			$T_{vj} = 185^{\circ}C^g$	-	0.8	100	
			$T_{vj} = 200^{\circ}C^g$	-	1.1	-	
Internal gate resistor ^{g, h}	$R_{G,int}$	$f = 100kHz$, $dV = 25mV$, $T_{vj} = 25^{\circ}C$		-	4.3	-	Ω
Forward transconductance ^g	g_{fs}	$V_{DS} = 20V$, $I_D = 80A$, $T_{vj} = 25^{\circ}C$		-	66	-	S
Input capacitance ^g	C_{iss}	$V_{DS} = 470V$, $f = 100kHz$, $dV = 25mV$, $T_{vj} = 25^{\circ}C$		-	5765	-	pF
Output capacitance ^g	C_{oss}			-	365	-	
Reverse transfer capacitance ^g	C_{rss}			-	27	-	
Gate charge ^g	Q_G	$V_{DS} = 470V$, $I_D = 80A$, $V_{GS(on)} = 18V$, $V_{GS(off)} = -3V$, $T_{vj} = 25^{\circ}C$		-	186	-	nC
Gate-to-source charge ^g	Q_{GS}			-	58	-	
Gate-to-drain charge ^g	Q_{GD}			-	29	-	
Turn-on energy ^{i, j}	E_{on}	$V_{DS} = 470V$, $I_D = 80A$, $V_{GS(on)} = 18V$, $V_{GS(off)} = -3V$, $L_s = 20nH$, $dV_{DS}/dt = 20V/ns$, $T_{vj} = 25^{\circ}C$		-	0.6	-	mJ
Turn-off energy ⁱ	E_{off}			-	0.3	-	

^g Not subject to production test, verified by design/characterization.

^h The internal gate resistor includes the implemented and layout dependent gate resistance.

ⁱ Not subject to production test, characterized in TO-247-4 package on a reference test setup.

^j Body diode E_{rec} included.

4 Body Diode Characteristics

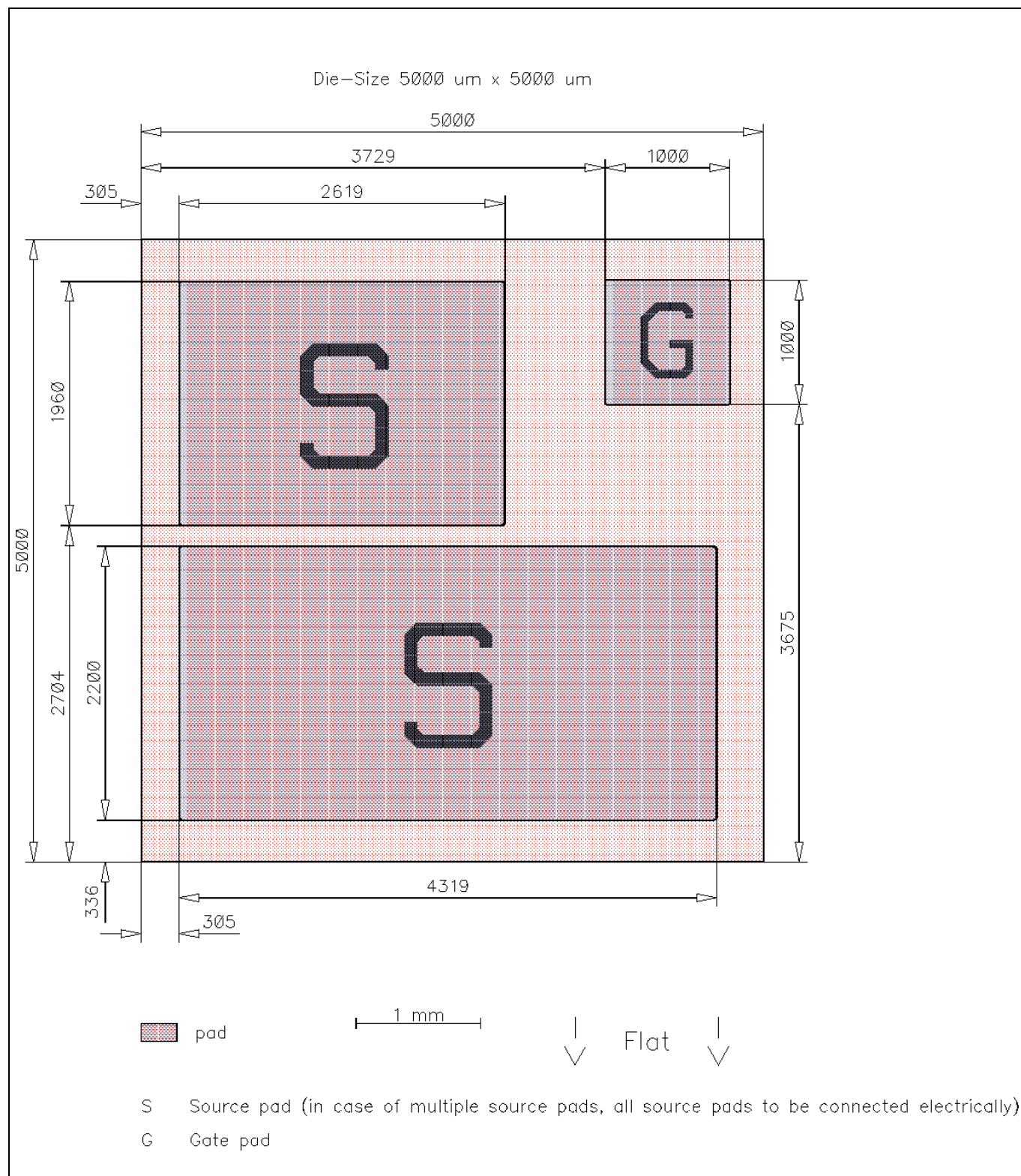
Specification limits valid over product lifetime if not stated otherwise.

Parameter	Symbol	Conditions		Value			Unit
				min.	typ.	max.	
Drain-source reverse voltage	V_{SD}	$I_F = 80A$, $V_{GS} = -3V$	$T_{vj} = 25^{\circ}C$	3.6	4.4	5.2	V
			$T_{vj} = 175^{\circ}C^k$	3.1	3.9	4.7	
			$T_{vj} = 185^{\circ}C^k$	3.05	3.85	4.65	
			$T_{vj} = 200^{\circ}C^k$	-	3.8	-	
Reverse recovery charge ^k	Q_{rr}	$V_{DS} = 470V$, $I_D = 80A$, $V_{GS(on)} = 18V$, $V_{GS(off)} = -3V$, $di/dt = 1kA/\mu s$, $T_{vj} = 25^{\circ}C$		-	130.4	-	nC
Reverse recovery time ^k	t_{rr}			-	22.5	-	ns
Peak reverse recovery current ^k	I_{rm}			-	9.7	-	A

5 Mechanical Parameters

Chip size after sawing	x = 4.97mm, y = 4.97mm	
Raster size	x = 5.00mm, y = 5.00mm	
Area total	25	mm ²
Source pad size	See die drawing	
Gate pad size	See die drawing	
SiC thickness	110	μm
Chip thickness (incl. Imide)	130	μm
Passivation front side	Photoimide	
Pad metal	NiP/Pd	
Backside metal	Ag - system	
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C	
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment	

6 Die Drawing



Legend:

- S = Source
- G = Gate

7 Bare Die Product Specifics

Note: The MOSFET wafer level test cannot cover the full range of customer application conditions. Therefore it is the responsibility of the customer to test all performance characteristics, which are relevant for their specific application, at the package level.

Description

- AQL 0.1 for visual inspection according to failure catalogue

Revision History

Document version	Date of release	Description of changes
V1.0	2026-01-14	Final Datasheet

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Edition 2026-01-14

Published by

Infineon Technologies AG

81726 München, Germany

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