英飞凌512 Mb/1 Gb SEMPER™闪存存储器

四线 SPI，1.8 V/3.0 V

特性

- 英飞凌 45 纳米 MIRRORBIT™ 技术，在每个存储单元中存储两个数据位
- 扇区布局选项
  - 全局统一：地址空间由所有 256 KB 扇区组成
  - 混合配置 1：地址空间由32个 4 KB 扇区组成，这些扇区组分别在顶部或底部，其余扇区均为 256 KB
  - 混合配置 2：地址空间由32个 4 KB 扇区组成，顶部和底部均等分配各一半，其余扇区均为 256 KB
- 256 或 512 字节的页写入缓存
- 1024字节（32x32字节）的OTP安全存储区域
- 四线 SPI
  - 支持 1S-1S-4S、1S-4S-4S、1S-4D-4D、4S-4S-4S、4S-4D-4D 协议
  - SDR 选项运行速度高达 83 MBps（166 MHz 时钟速度）
  - DDR 选项运行速度高达 102 MBps（102 MHz 时钟速度）
- 双线 SPI
  - 支持1S-2S-2S协议
  - SDR 选项运行速度高达 41.5 MBps（166 MHz 时钟速度）
- SPI
  - 支持1S-1S-1S协议
  - SDR 选项运行速度高达 21 MBps（166 MHz 时钟速度）
- 功能安全特性
  - 业界首款符合 ISO26262 ASIL B 标准并支持 ASIL-D 等级的 NOR 闪存以确保功能安全
  - 英飞凌 Endurance Flex 架构提供高耐久性和长保留分区
  - 数据完整性CRC（循环冗余校验）检测内存阵列中的错误
  - SafeBoot 报告器件初始化失败、检测配置损坏并提供恢复选项
  - 内置纠错码 (ECC) 可以在内存阵列数据上纠正单比特错误并检测双比特错误 (SECDED)
  - 扇区擦除状态指示器可以提示擦除过程中的意外掉电
- 保护功能
  - 用于内存阵列和器件配置的传统扇区写保护
  - 针对每个内存阵列扇区的高级扇区保护
- 自动启动可支持上电后立即访问内存阵列
- 通过JEDEC串行闪存复位信号协议 / 独立的 RESET# 引脚 / DQ3_RESET# 引脚进行硬件复位
- 串行闪存设备可发现参数 (SFDP)用来描述器件功能和特性
- 器件标识、制造商标识和唯一标识
- 数据完整性
  - 512 Mb 设备
    - 主阵列至少可进行 1,280,000 次写入-擦除循环

- 1 Gb 设备
  - 主阵列至少可进行 2,560,000 次写入-擦除循环
- 所有设备
  - 4KB 扇区至少可进行 300,000 次写入-擦除循环
  - 至少 25 年的数据保留时间

• 供电电压

- 1.7 V 至 2.0 V（HS-T）

- 2.7 V 至 3.6 V（HL-T）

• 等级/温度范围

- 工业级（–40°C ~ +85°C）
- 扩展的工业级（ –40°C ~ +105°C）
- 汽车级，AEC-Q100 3 级（–40°C ~ +85°C）
- 汽车级，AEC-Q100 2 级（–40°C ~ +105°C）
- 汽车级，AEC-Q100 1 级（–40°C ~ +125°C）

• 封装

- 512 MB
  - 16 引脚 SOIC（300 mil）- SO3016
  - 24 球 BGA 6 x 8 毫米
  - 8 触点 WSON 6 x 8 毫米
  - 1GB
    - 16 引脚 SOIC（300 mil）- SO3016
    - 24 球 BGA 8 x 8 毫米
    - 16 引脚 SOIC（300 mil）

性能总结

表 1　　最大读取率

Transaction	Initial access latency (Cycles)	Clock rate (MHz)	MBps
SPI Read	0	50	6.25
SPI Fast Read	9	166	20.75
Dual Read SDR	7	166	41.5
Quad Read SDR	10	166	83
Quad Read DDR	7	102	102

表 2　　典型编程和擦除速率

Operation	KBps
256B page programming (4KB sector/256KB sector)	595/533
512B page programming (4KB sector/256KB sector)	753/898
256 KB sector erase	331
4 KB sector erase	95

表 3　　典型电流消耗

Operation	Current (mA)
SDR Read 50 MHz	10
SDR Read 166 MHz	53
DDR Read 102 MHz	50
Program	50
Erase	50
Standby (HS-T)	0.011
Standby (HL-T)	0.014
Deep power down (HS-T)	0.0013
Deep power down (HL-T)	0.0022

数据完整性

表 4　　写入/擦除 (PE) 耐久性 - 高耐久性 (256KB 扇区)

Sectors in partition	Minimum PE cycles	Minimum retention time	Unit
512 (Default for 1 Gb devices)	2,560,000	2	Years
508	2,540,000		
504	2,520,000		
...	...		
256 (Default for 512 Mb devices)	1,280,000		
252	1,260,000		
128	640,000		
...	...		
28	140,000		
24	120,000		
20	100,000		

注释：*最小周期是针对整个高耐久性分区的。*

表 5　　写入/擦除耐久性 - 长数据保持分区（256 KB 扇区）

Minimum PE cycles	Minimum retention time	Unit
500	25	Years

注释：最小周期针对每个扇区。

表 6　　写入/擦除耐久性 4 KB 扇区和非易失性寄存器阵列

Flash memory type	Minimum cycles	Unit	Minimum retention time	Unit
Program/Erase cycles per 4 KB sector	500	PE cycles	25	Years
	300,000 ***Note**: It is required to restrict the power loss events to 300 times per sector during program or erase operation to achieve the mentioned endurance cycles.*		2	

（表格续下页……）

表 6 （续）写入/擦除耐久性 4 KB 扇区和非易失性寄存器阵列

Flash memory type	Minimum cycles	Unit	Minimum retention time	Unit
Program/Erase cycles per persistent protection bits (PPB) array or nonvolatile register array ***Note**: Each write transaction to a nonvolatile register causes a PE cycle on the entire nonvolatile register array.*	500		25	

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1 引脚分配和信号描述

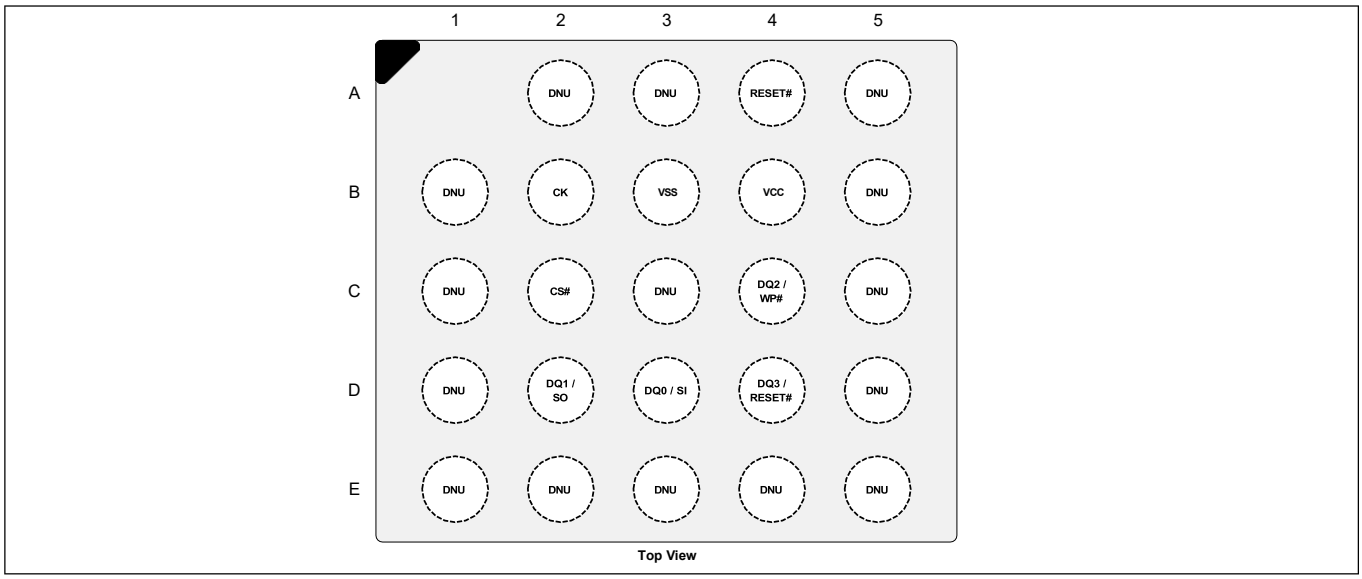

图 1 24 球BGA引脚样式[1)]

1. 如果使用超声波清洁方法，BGA封装的闪存器件可能被损坏。如果封装体长时间暴露在 150°C 以上的温度下，封装和/或数据完整性可能会受到损害

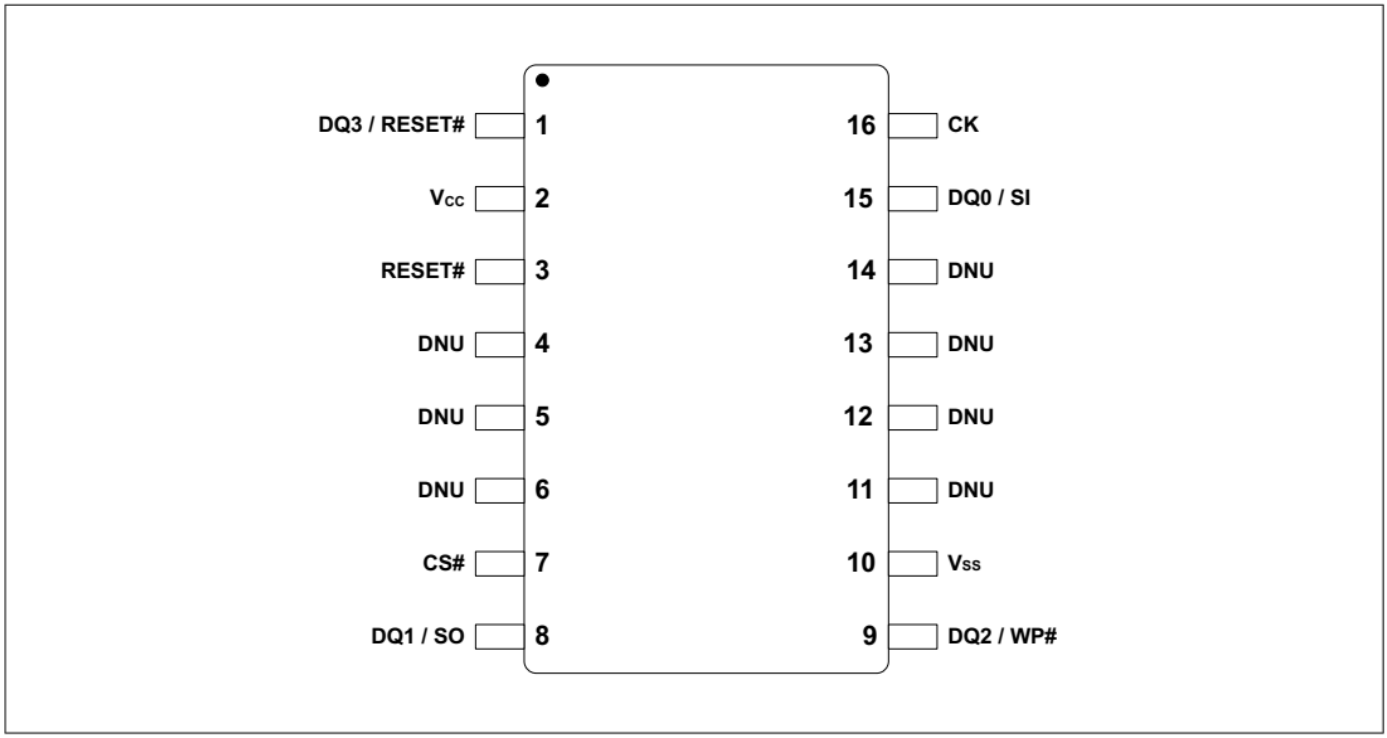

图 2　　16 引脚 SOIC 封装 (SO316)，顶视图

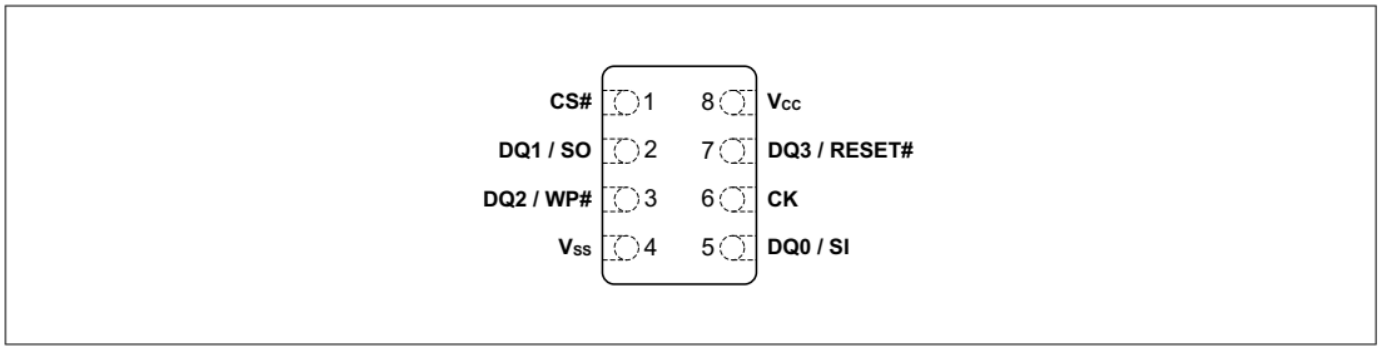

图 3　　8连接引脚封装（WSON 6×8），顶视图

表 7　　信号描述

Symbol	Type	Mandatory/ optional	Description
CS#	Input	Mandatory	**Chip Select (CS#).** All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH.

（表格续下页……）

表 7　　（续）信号描述

Symbol	Type	Mandatory/ optional	Description
CK			**Clock (CK).** Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DQ0/SI	Input/Output		Serial Input (SI) for single SPI protocol **DQ0 Input/Output** for Dual or Quad SPI protocol
DQ1/SO			Serial Output (SO) for single SPI protocol **DQ1 Input/Output** for Dual or Quad SPI protocol
DQ2/WP#	Input/Output (weak Pull-up)		Write Protect (WP#) for single and dual SPI protocol **DQ2 Input/Output** for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad transactions or write protection. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register transactions.
DQ3/RESET#			**RESET#** for single and dual SPI protocol. This signal can be configured as RESET# when CS# is HIGH or Quad SPI protocol is disabled. **DQ3 Input/Output** for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad SPI transactions or RESET#
RESET#	Input (weak Pull-up)	Optional	**Hardware Reset (RESET#).** When LOW, the device will self initialize and return to the array read state. DQ[3:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.
V_{CC}	Power Supply	Mandatory	Core Power Supply
V_{SS}	Ground Supply		Core Ground
DNU	–	–	Do Not Use.

2 接口概述

2.1 概述

英飞凌 Quad SPI 接口 SEMPER™ 系列产品是高速 CMOS, MIRRORBIT™ 工艺闪存式存储器件。SEMPER™ 闪存式存储器专为功能安全而设计，基于 ISO 26262 标准进行开发，通过 ASIL-B 等级认证并支持最高 ASIL-D 等级。

配备Quad SPI接口的SEMPER™ 闪存式存储器支持传统的单位SPI串行输入和输出、可选的两位（双 I/O 或 DIO）以及四位宽的四 I/O (QIO) 和四线外设接口 (QPI) 协议。此外，还有针对 QIO 和 QPI 的 DDR 读取传输，可在时钟的两个边沿传输地址并读取数据。

从器件读取操作是并发导向的。读取传输可以配置为使用回卷并发或线性并发。回卷并发从单个页读取，而线性突发可以读取整个存储阵列。

每个存储器位的擦除状态为一个逻辑1。编程操作会将逻辑1（低电平）修改为逻辑0（高电平）。只有擦除操作才能将内存位从 0 更改为 1。擦除必须对完整扇区（4 KB 或 256 KB）执行擦除操作。

SEMPER™ 闪存存储器提供灵活的扇区布局。地址空间既可以配置为统一的 256 KB 扇区阵列，也可以配置为混合配置 1，其中三十二个 4 KB 扇区分组在顶部或底部，而剩余的扇区全部为 256 KB，或者配置为混合配置 2，其中三十二个 4 KB 扇区在顶部和底部之间平均分配各半，而剩余的扇区全部为 256 KB。

在单个写入操作期间使用的页写入缓存可配置为 256 字节或 512 字节。512 字节选项提供最高的写入吞吐量。

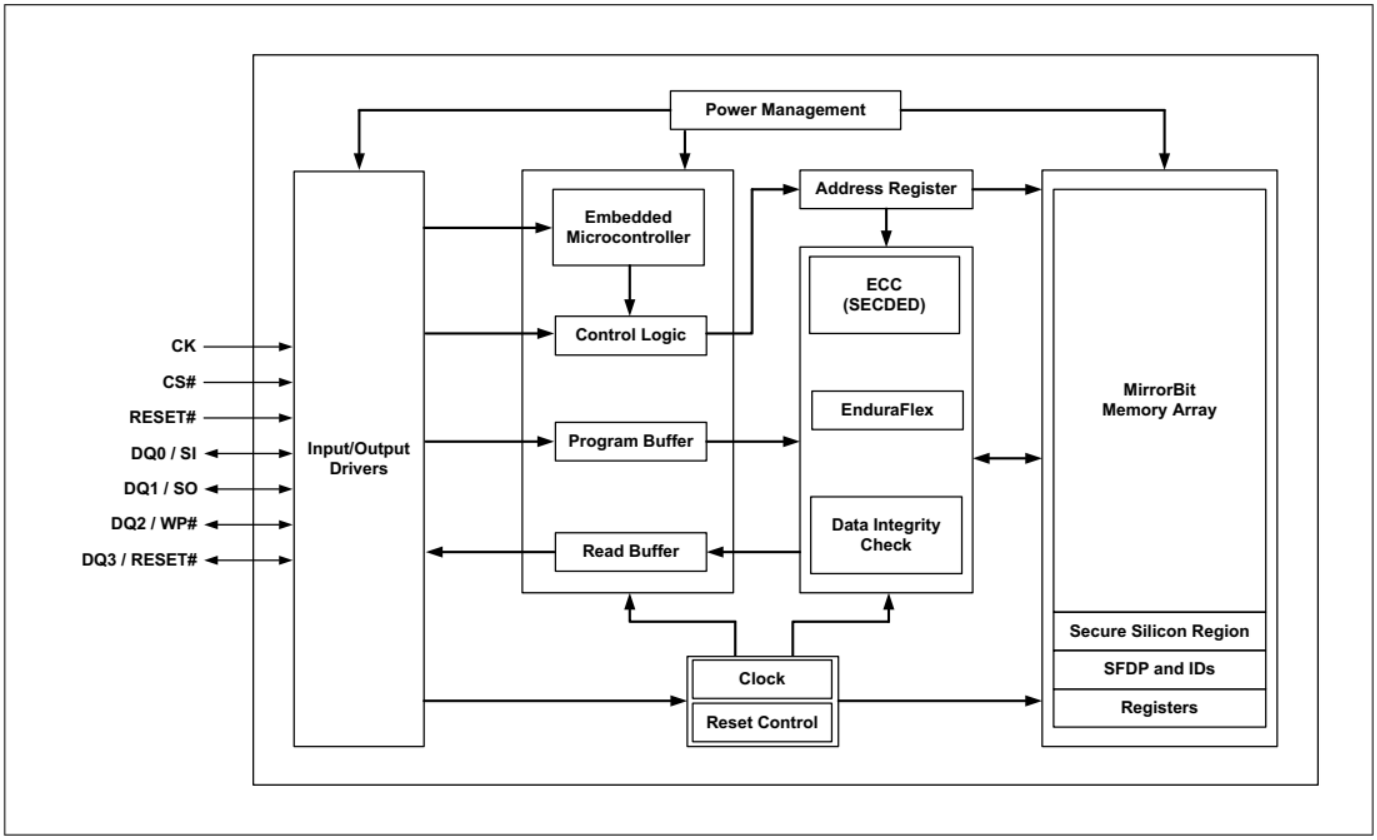

图 4 逻辑框图

配备Quad SPI 接口的SEMPER™ 闪存式存储器由多种密度组成，具有 1.8 V 和 3.0 V 核心和 I/O 电压选项。

器件控制逻辑分成两个并行的操作区，Host Interface Controller（主机接口控制器，HIC）和 Embedded Algorithm Controller（嵌入式算法控制器，EAC）。HIC监控器件输入的信号电平，并根据需要驱动输出，以完成与主机系统间的读取和写入数据传输。HIC在读取传输时将传递当前所在的地址映射中的数据；将写入传输地址和数据信息放入EAC指令存储器内；告知EAC电源转换以及写入传输。EAC在写入传输后查看指令存储器中的合法指令序列，并执行相关的嵌入式算法。

更改存储器阵列中的非易失性数据时，需要执行复杂的操作序列，这些操作被称为嵌入式算法（EA）。这些算法完全由器件内部的EAC来管理。主算法执行主阵列数据的写入和擦除。主机系统将指令代码写入到闪存器件中。EAC接收指令用于执行所有必要的步骤以完成指令，并在EA执行期间提供状态信息。

直接从闪存执行代码通常称为原位运行(XIP)。通过将XIP与SEMPER™ 闪存式存储器设备一起使用，以更高的时钟速率进行 Quad 或 DDR Quad SPI传输，数据传输速率可以匹配或超过传统并行或异步 NOR 闪存式存储器，同时显着减少信号数量。

英飞凌 Endurance Flex 架构使得系统设计人员能够根据其特定应用来定制 NOR 闪存擦写耐久性和数据保持特性。 主控定义高耐久性或长保留时间的分区，提供高达 100 万次以上的擦写循环或 25 年的数据保留时间。

配备Quad SPI 接口的SEMPER™ 闪存式存储器通过在存储器阵列写入期间生成嵌入式汉明纠错码来支持错误检测和纠正。然后，该 ECC 码用于读取过程中单比特位和双比特位错误检测以及单比特位错误纠正。

配备Quad SPI接口的SEMPER™ 闪存式存储器具有内置诊断功能，为主控系统提供器件状态。

- 写入和擦除操作：报告写入或擦除成功、失败和暂停状态
- 错误检测与纠正：具有地址捕获和错误计数的 1 比特位和/或 2 比特位错误状态
- 数据完整性检查：对内存阵列内容进行错误检测
- SafeBoot：报告正确的闪存式存储器初始化和配置损坏恢复
- 扇区擦除状态：报告每个扇区的擦除成功或失败状态
- 扇区擦除计数器：计算每个扇区的擦除次数

2.2 信号协议

2.2.1 SEMPER™ 闪存式存储器的Quad SPI时钟模式

配备Quad SPI接口的SEMPER™ 闪存式存储器可由嵌入式总线主设备以以下两种时钟模式之一驱动：

- **模式 0**，时钟极性在 CS# 下降时处于低电平，并保持低电平，直到捕获输入时变为高电平。
- **模式 3**，时钟极性在 CS# 下降时为高电平，然后在捕获输入时由低电平变为高电平。

对于这两种模式， SDR协议中数据在 CK 信号的上升沿被锁存到器件中，而 DDR 协议中数据在 CK 信号的两个边沿被锁存到器件中。输出数据在 CK 时钟信号的下降沿可用。对于 DDR 协议，不支持模式 3。

两种模式的区别在于当总线主机处于待机模式且不传输任何数据时的时钟极性。

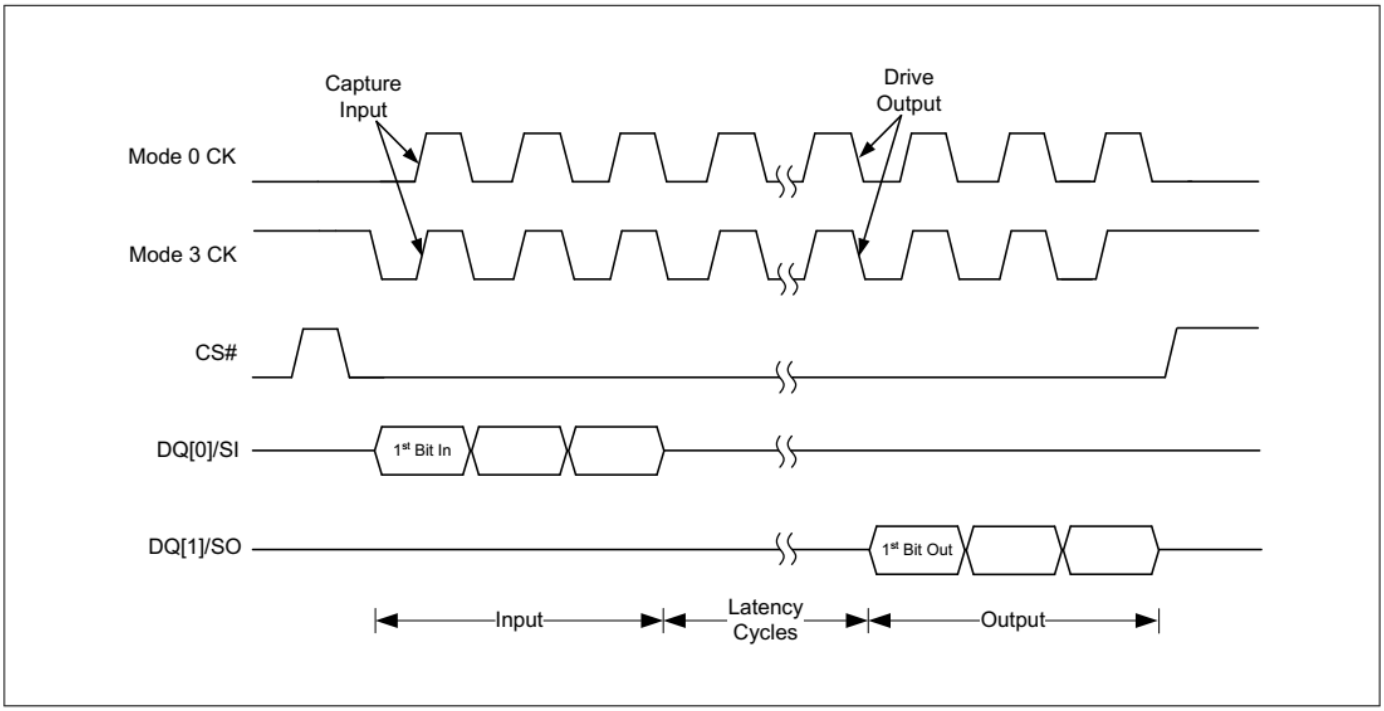

图 5　　SPI SDR模式支持

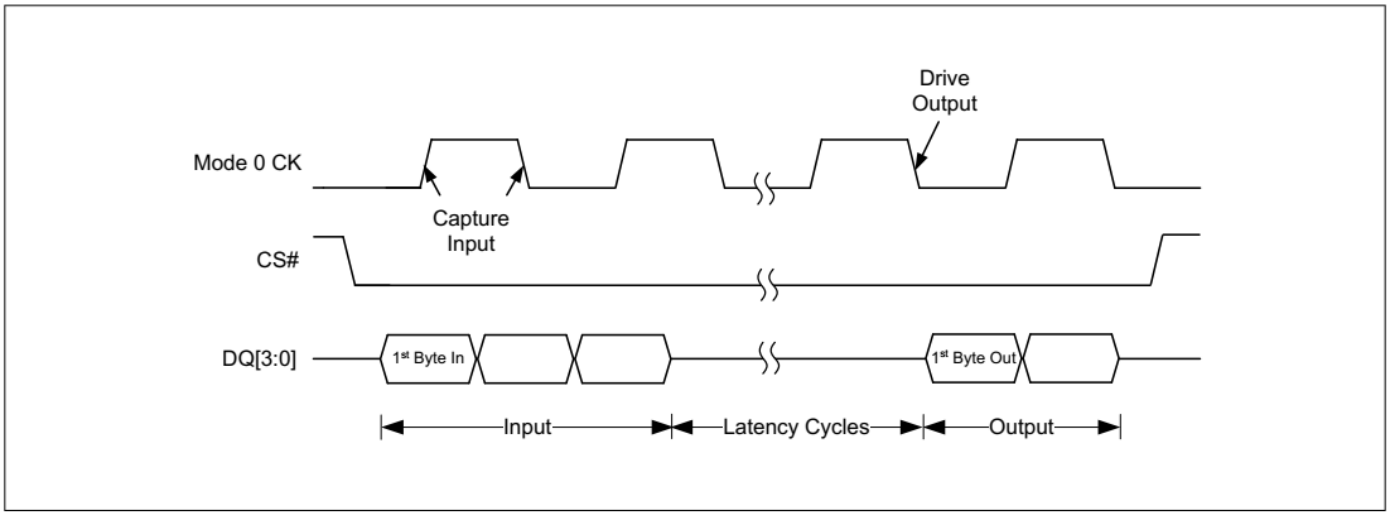

图 6　　SPI DDR模式支持

2.3　　传输协议

传输

- 在 CS# 为选通（低电平）期间，时钟信号 (CK) 被切换，同时指令信息首先在数据 (DQ) 信号上传输，然后是地址和数据从主控传输到闪存式存储器器件。 在从闪存式存储器件向主控传输读取数据或从主控向闪存式存储器件写入数据期间，时钟持续切换。当主控传输了所需数量的数据时，主控将驱动 CS# 处于非选通状态（高电平）。CS# 被选通的时间段称为总线上的一个命令传输。
- 当 CS# 处于非选通状态时，CK 无需切换。
- 指令发送发生在每次命令传输开始时。地址、延迟周期和数据传输阶段是可选的，它们的存在取决于传输的协议模式或指令。

传输采集

- CK 标记主控和存储器之间每个比特位或多个比特位的传输。指令、地址和写入数据位传输发生在SDR传输中的 CK 上升沿，或发生在 DDR 传输中的每个 CK 沿。

注释：在写入或擦除（嵌入式操作）期间，所有读取闪存存储阵列的尝试都将被忽略。嵌入式操作将继续执行，不会产生任何影响。在嵌入式操作期间，只能接受非常有限的指令集。这些内容在**"暂停和恢复嵌入式操作"**中讨论 在 分页 67。

协议术语

- 传输过程中使用的DQ信号的数量取决于当前的协议模式或传输的指令。延迟周期不使用 DQ 信号进行信息传输。协议模式选项由指令、地址和数据阶段使用的数据速率和 DQ 宽度（DQ 信号数）描述，格式如下：

  WR-WR-WR，其中：

  - 第一个WR是指令位宽度和速率。
  - 第二个WR是地址位宽度和速率。
  - 第三个WR是数据位宽度和速率。
- 位宽值可以是 1、2 或 4。对于 SDR，R 的值为 S；对于 DDR，R 的值为 D。SDR在一个时钟周期的上升沿和下降沿具有相同的传输值。DDR 在每个时钟的上升沿和下降沿可以有不同的传输值。
- 示例：
  - 1S-1S-1S表示指令为1比特位宽SDR ，地址为1比特位宽SDR ，数据为1比特位宽SDR 。
  - 4S-4D-4D 表示指令为 4 比特位宽SDR ，地址和数据传输为 4 比特位宽 DDR。

协议定义

- 具备Quad SPI接口SEMPER™闪存式存储器定义的协议模式：
  - 1S-1S-1S：指令传输、地址传输和数据传输期间使用一个 DQ 信号。 所有阶段均为 SDR。
  - 1S-2S-2S：一个DQ信号用于指令传输，两个DQ信号用于地址传输和数据传输。 所有阶段均为 SDR。
  - 1S-1S-4S：指令和地址传输时使用一个DQ信号，数据传输时使用四个DQ信号。 所有阶段均为 SDR。
  - 1S-4S-4S：一个DQ信号用于指令传输，四个DQ信号用于地址传输，还有数据传输。 所有阶段均为 SDR。
  - 1S-4D-4D： 指令传输使用一个DQ信号并以SDR方式，地址和数据传输使用四个DQ信号并以DDR方式。
  - 4S-4S-4S：指令传输、地址传输和数据传输期间使用的四个 DQ 信号。 所有阶段均为 SDR。
  - 4S-4D-4D： 指令传输使用的四个DQ信号并以SDR方式，地址和数据传输使用的四个DQ信号并以DDR方式。
- 每个传输都以一个 8 比特位（1 字节）指令开始。该指令选择要执行的信息传输类型或器件操作。
- 所有协议都支持 3 或 4 字节寻址。

1S-1S-1S 协议（单输入/输出，SIO）

- 1S-1S-1S 模式是上电复位 (POR) 后的首选默认协议，但闪存式存储器设备可配置为复位之后为四线模式。

- 该协议使用DQ[0]/ SI将信息从主控传输到闪存式存储器器件，使用DQ[1]/SO 将信息从闪存式存储器器件传输到主控。 在每个 DQ 上，信息按照每个字节内从最高有效位 (MSb) 到最低有效位 (LSb) 的顺序放置在 DQ 线上。连续地址字节按从最高顺序到最低顺序的顺序进行传输。连续数据字节按照从最低地址到最高地址的顺序进行传输。
- 在 1S-1S-1S 中，DQ[3:2] 不用于数据传输阶段。DQ[2] 可用作 WP#，DQ[3] 可用作 RESET# 输入。否则，DQ[3:2]信号将呈高阻态。

1S-2S-2S 协议（双输入/输出，DIO）

- 该协议使用 DQ[1:0] 信号。8 比特位指令按从 MSb 到 LSb 的顺序放置在 DQ[0] 上。 地址字节的最低位 (LSb) 放在 DQ[0] 上，下一个顺序位放在 DQ[1] 信号上，依此类推。连续地址字节按从最高顺序到最低顺序的顺序进行传输。SDR 中的连续数据字节按照从最低地址到最高地址的顺序传输。
- 在 1S-2S-2S 中，DQ[3:2] 不用于数据传输阶段。DQ[2] 可用作 WP#，DQ[3] 可用作 RESET# 输入。否则，DQ[3:2]信号将呈高阻态。

1S-1S-4S 协议（四线输出读取，QOR）

- 该协议使用 DQ[3:0] 信号。8 比特位指令和地址按照 MSb 到 LSb 的顺序放置在 DQ[0] 上。 SDR 中的连续数据字节按照从最低地址到最高地址的顺序传输。

1S-4S-4S 和 1S-4D-4D 协议（四线输入/输出，QIO）

- 该协议使用 DQ[3:0] 信号。8 比特位指令按从 MSb 到 LSb 的顺序放置在 DQ[0] 上。地址字节的 LSb 放置在 DQ[0] 上，每个高阶位放置在依次更高编号的 DQ 信号上。连续地址字节按从最高顺序到最低顺序的顺序进行传输。SDR 中的连续数据字节按照从最低地址到最高地址的顺序传输。DDR 中的顺序数据字节
  仅以字节对（字）的形式传输，其中字节顺序取决于在该协议模式下写入或烧录字节的顺序。连续数据字节按照从最低地址到最高地址的顺序进行传输。

4S-4S-4S 和 4S-4D-4D 协议（四线外设接口，QPI）

- 此协议使用 DQ[3:0] 信号。每个字节的 LSb 放在 DQ[0] 上，每个高阶位放在依次编号较高的 DQ 信号上。连续地址字节按从高到低的顺序传输。SDR 中的连续数据字节按从低到高地址的顺序传输。DDR 中的连续数据字节仅以字节对（字）的形式传输，其中字节顺序取决于在该协议模式下写入或烧录字节的顺序。连续数据字节按低到高地址的顺序传输。串行外设接口（SPI，1S-1S-1S）到四线外设接口（QPI，4S-4S-4S 和 4S-4D-4D）展示了所有协议模式下的传输格式。

2.3.1 串行外设接口（SPI、1S-1S-1S）

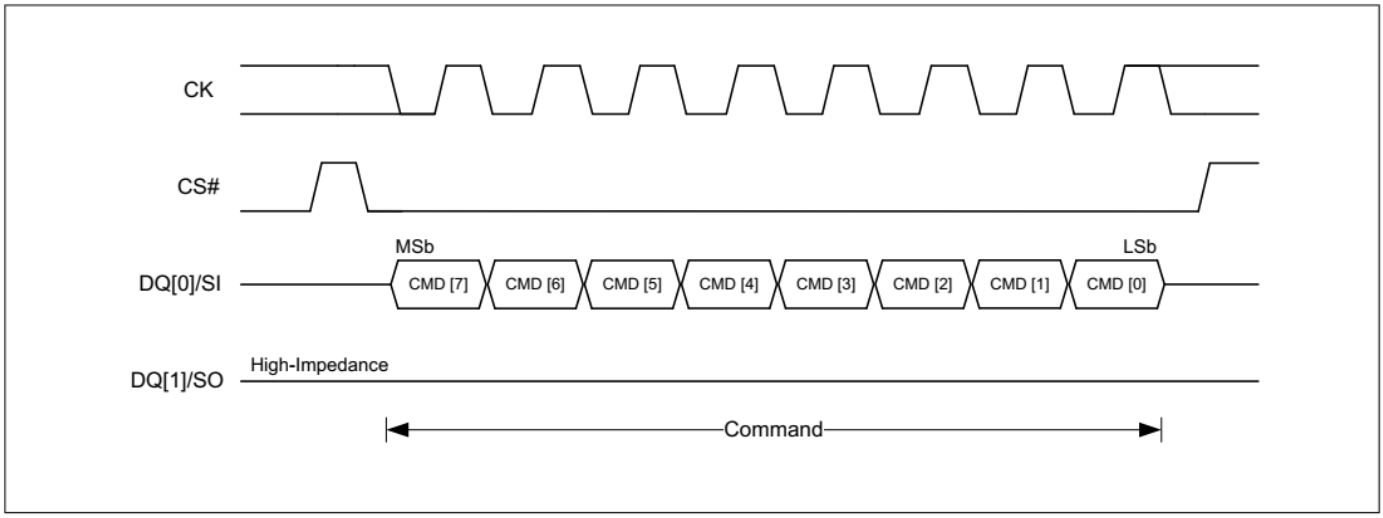

图 7　　带指令输入的SPI传输

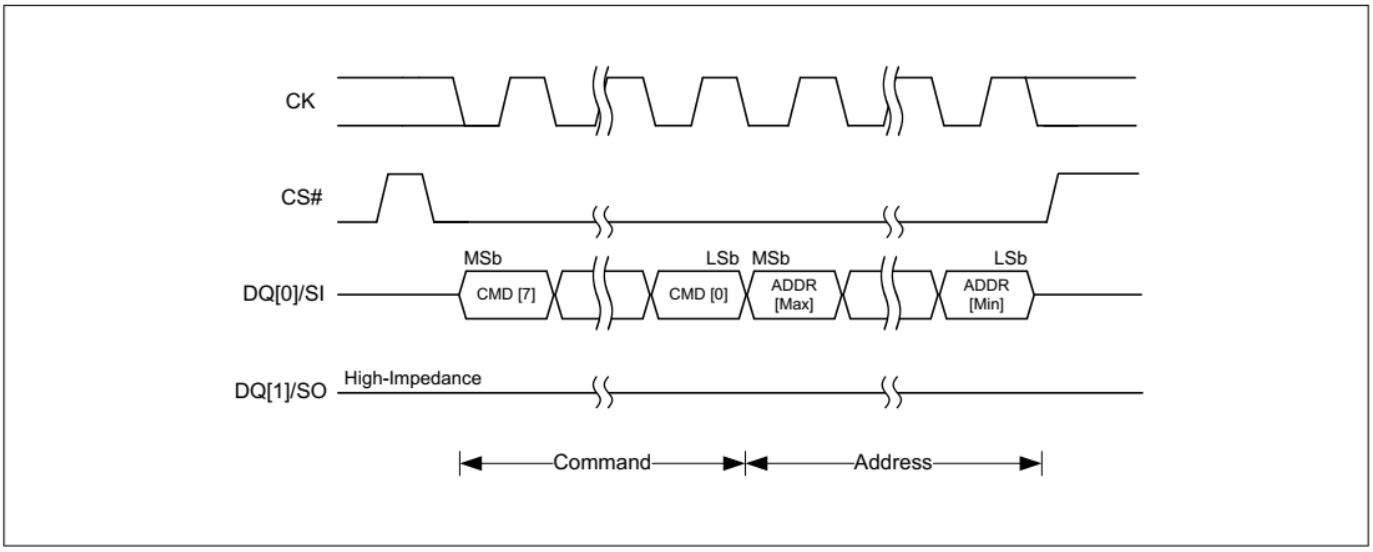

图 8　　带有指令和地址输入的SPI传输

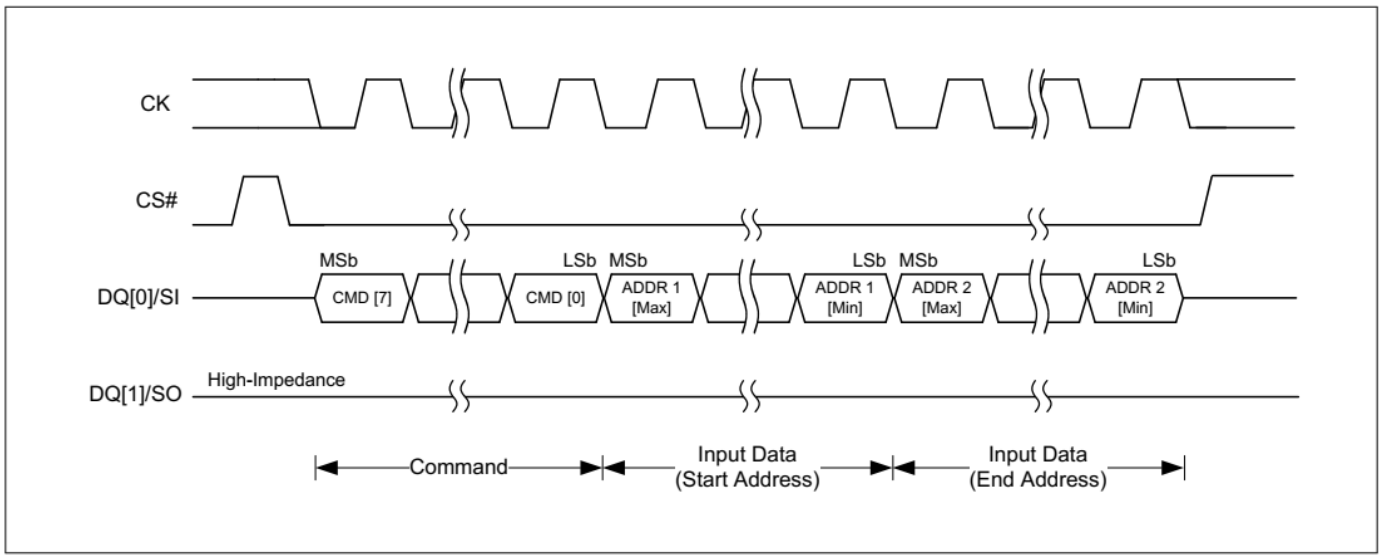

图 9　　带有指令和两个输入地址的SPI传输

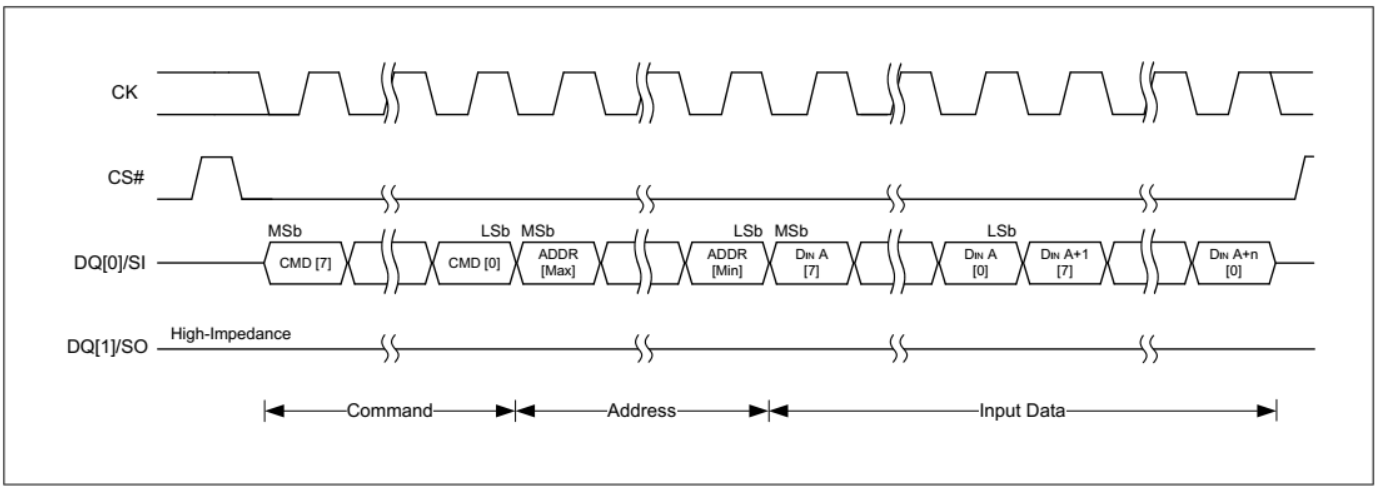

图 10　　带有指令、地址和数据输入的SPI写入传输

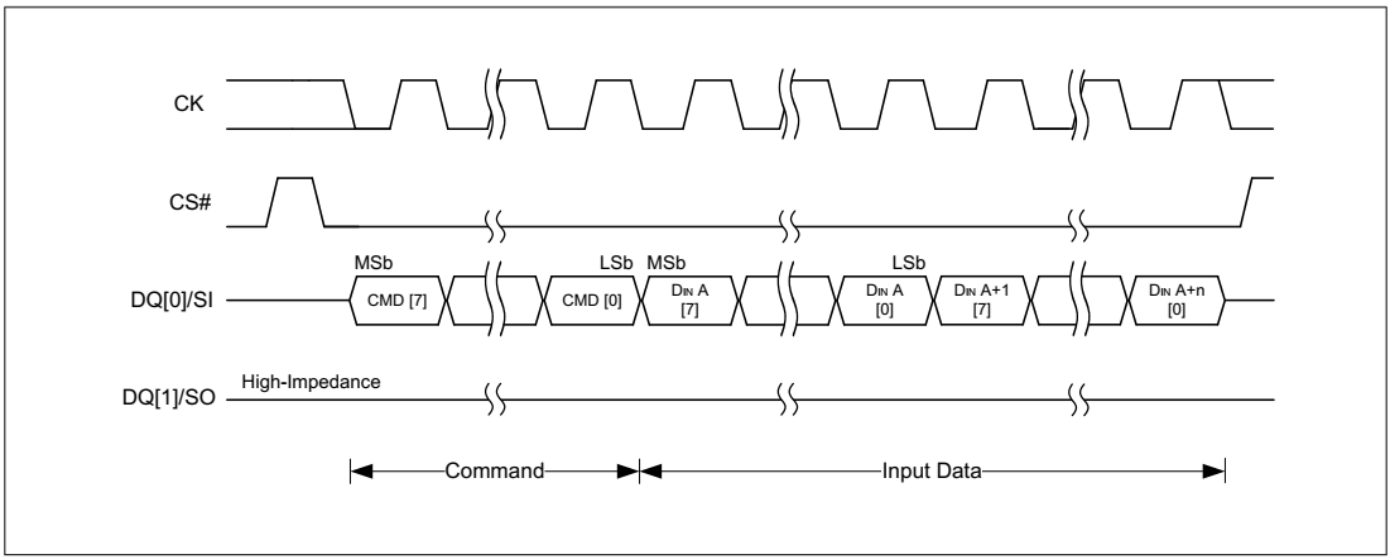

图 11　　带有指令和数据输入的SPI写入传输

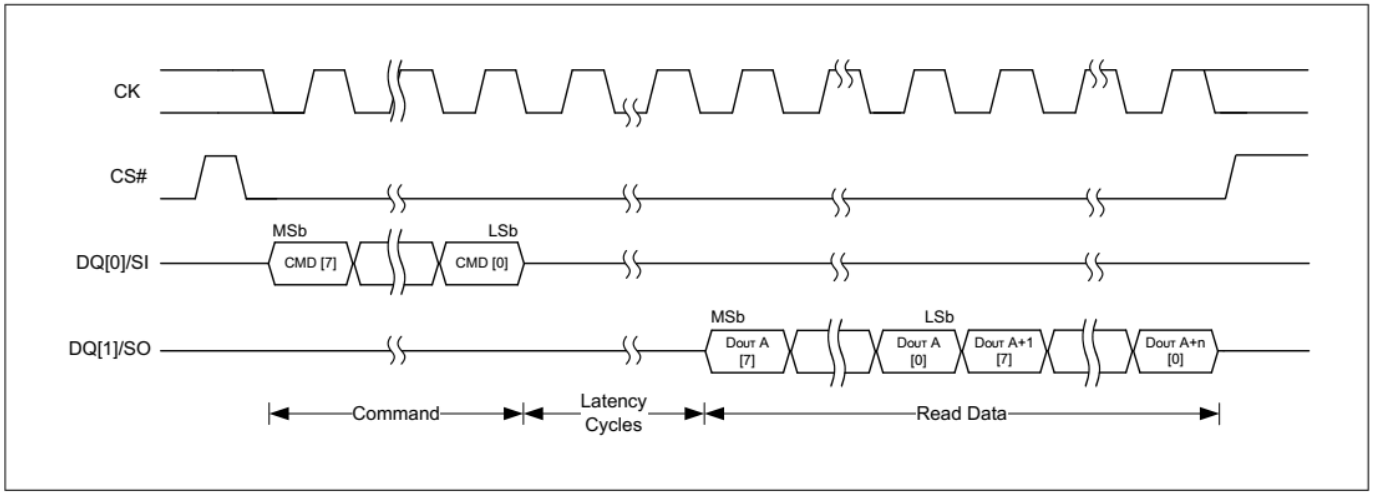

图 12　　带指令输入的SPI读取传输（输出延迟） [2, 3]

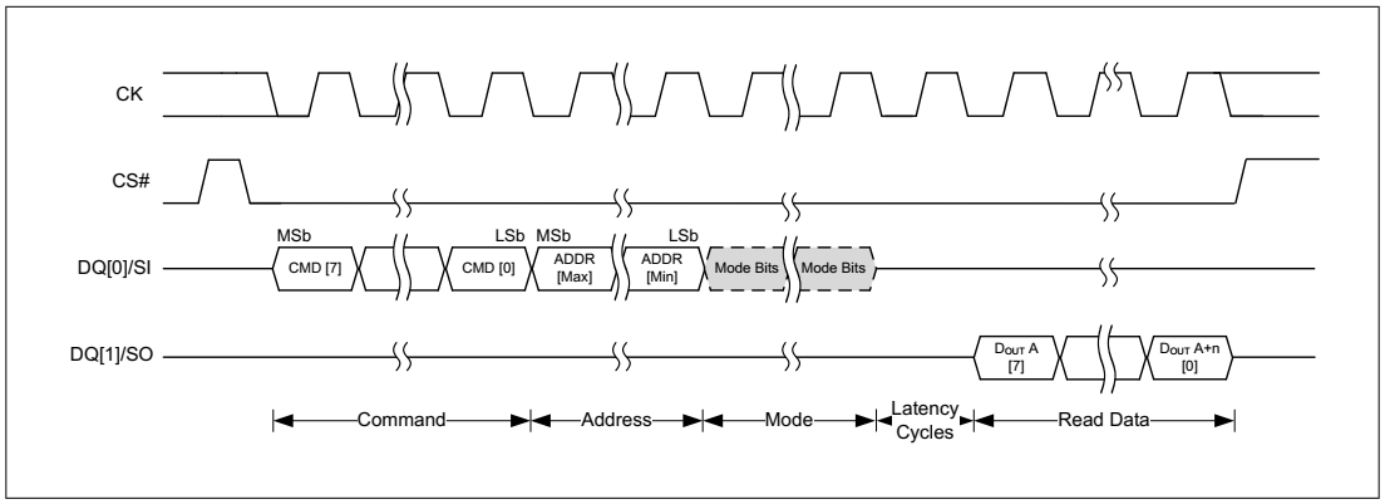

图 13　　具有指令和地址输入的SPI读取传输（输出延迟） [4]

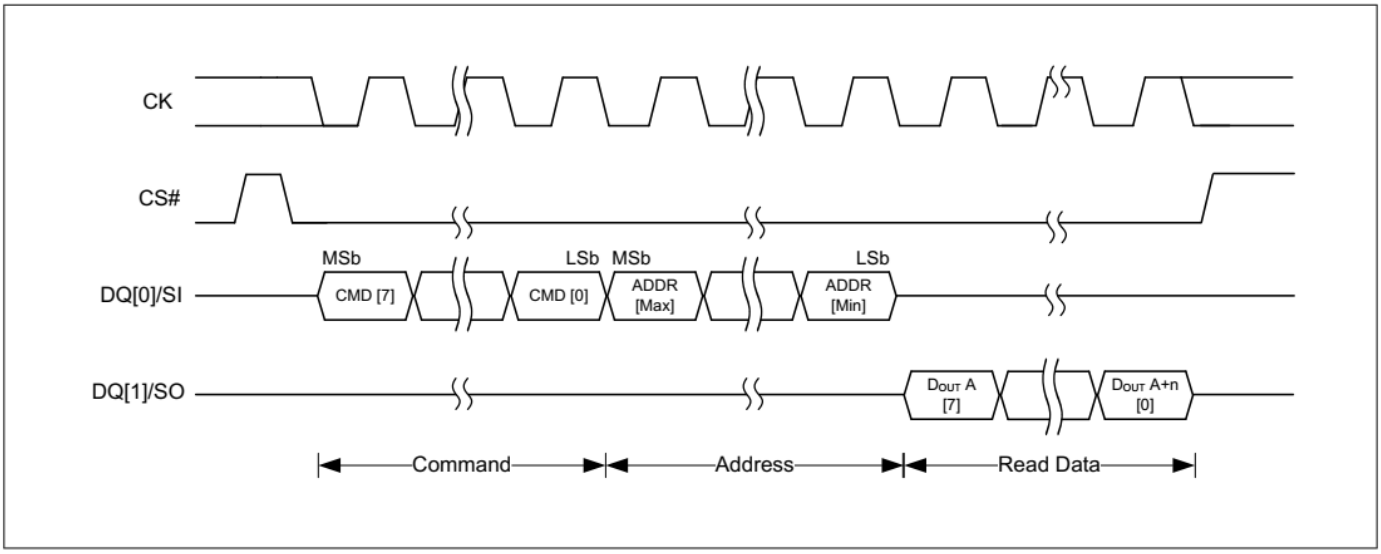

图 14　　具有指令和地址输入的SPI读取传输（无输出延迟）

2. 对于状态寄存器 1 和 2，读取的字节数据是更新后的状态。
3. 在 Data Learning Pattern 读取的情况下，每字节输出 DLP。
4. 对于 RDAY2_4_0 传输，主控必须提供模式位。

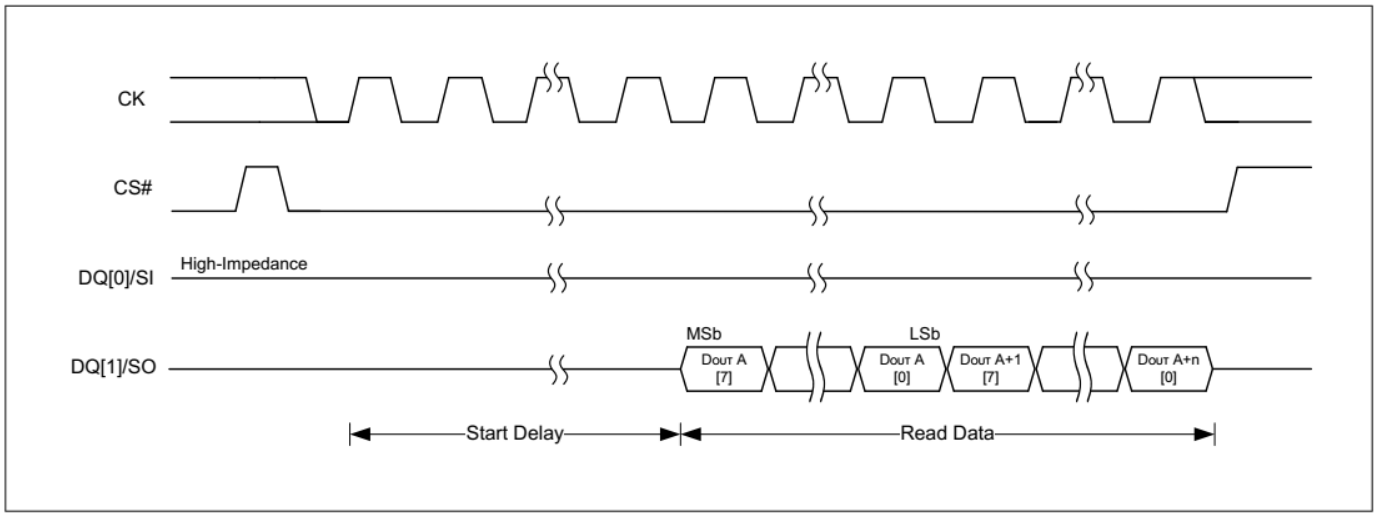

图 15　　带输出数据序列的 SPI 传输（AutoBoot）

2.3.2　双 IO SPI（DIO、1S-2S-2S）

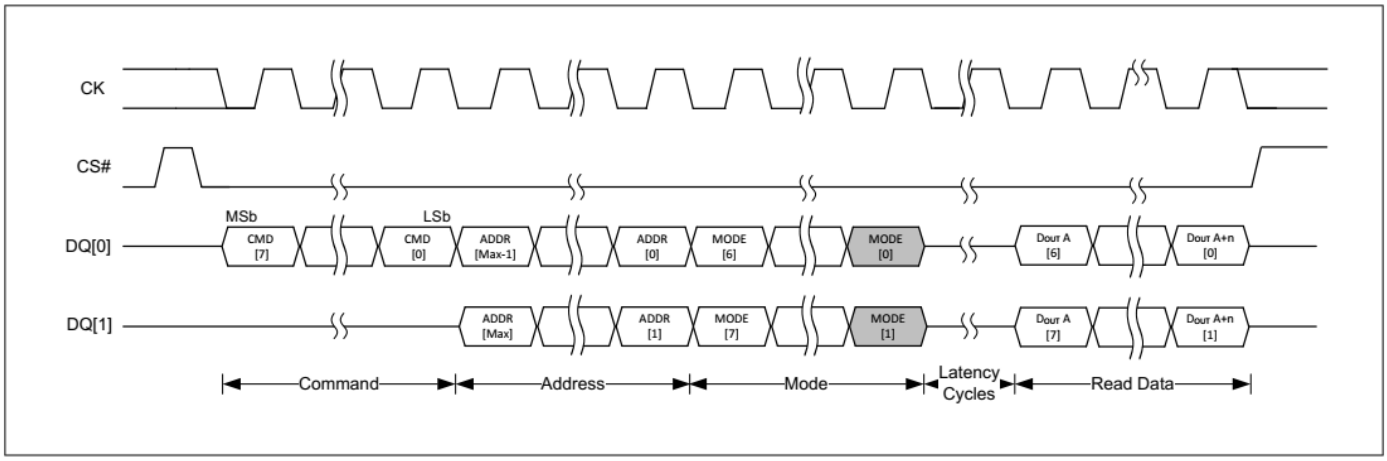

图 16　　带有指令、地址和模式输入的 DIO 读取传输（输出延迟）

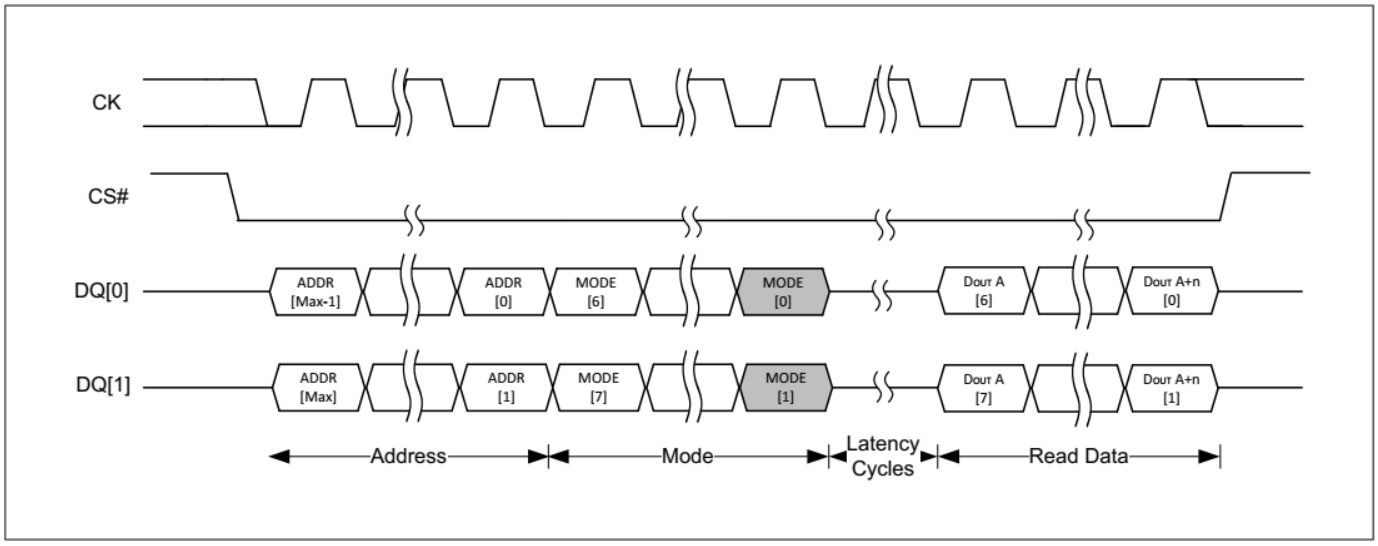

图 17　　具有地址和模式输入的 DIO 连续读取传输（输出延迟）

2.3.3 四线输出读取 SPI（QOR、1S-1S-4S）

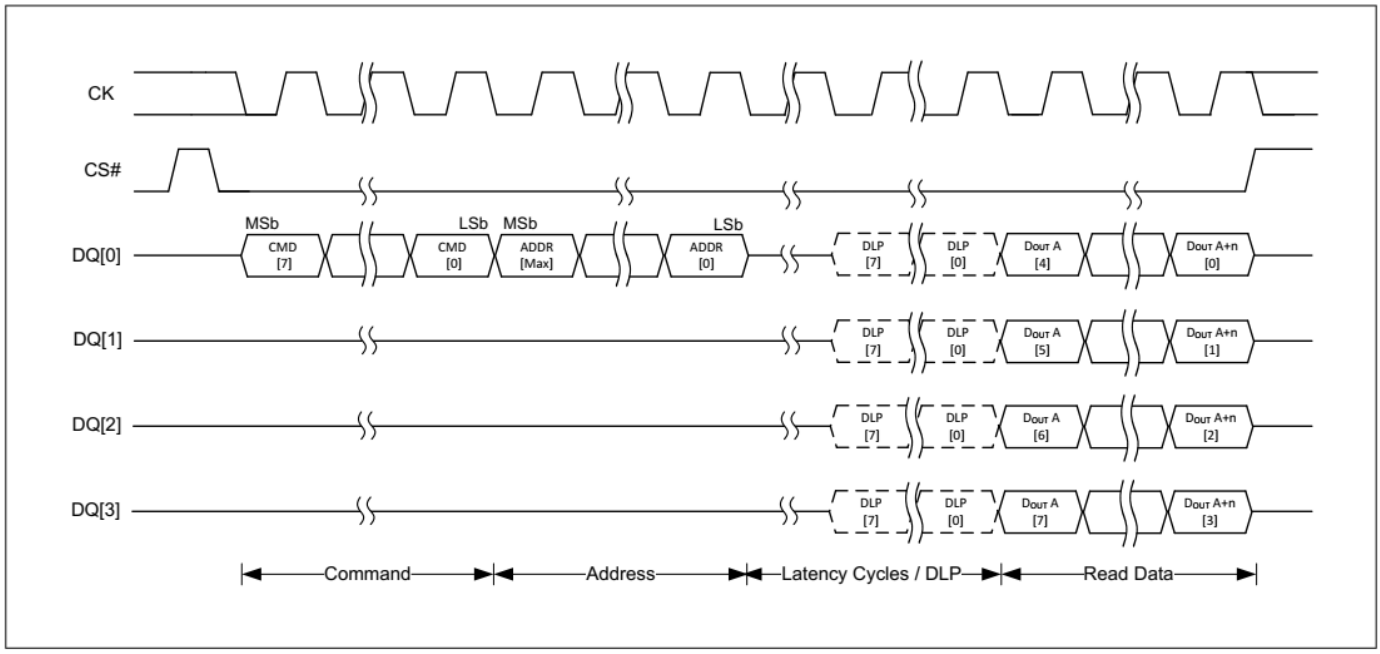

图 18　　带有指令、地址和模式输入的 QOR SDR读取传输（输出延迟）

2.3.4 四线 IO SPI（QIO、1S-4S-4S、1S-4D-4D）

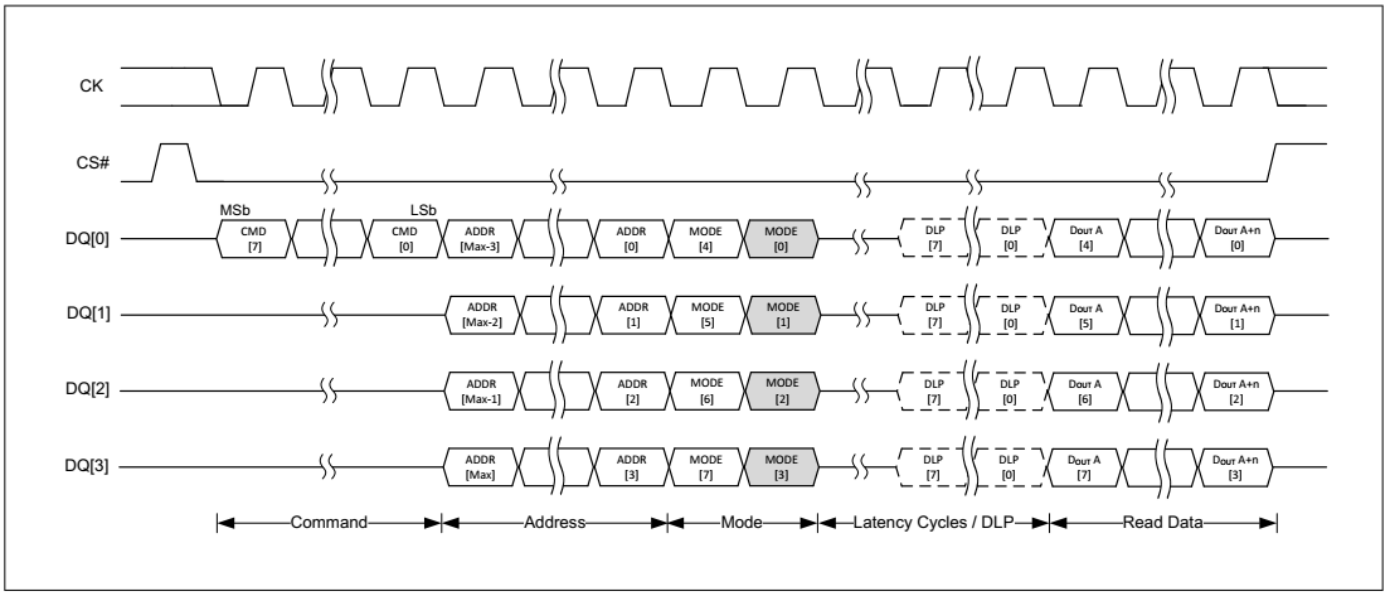

图 19　　带有指令、地址和模式输入的QIO SDR读取传输（输出延迟） [5]

5. 无需关注灰色位数据

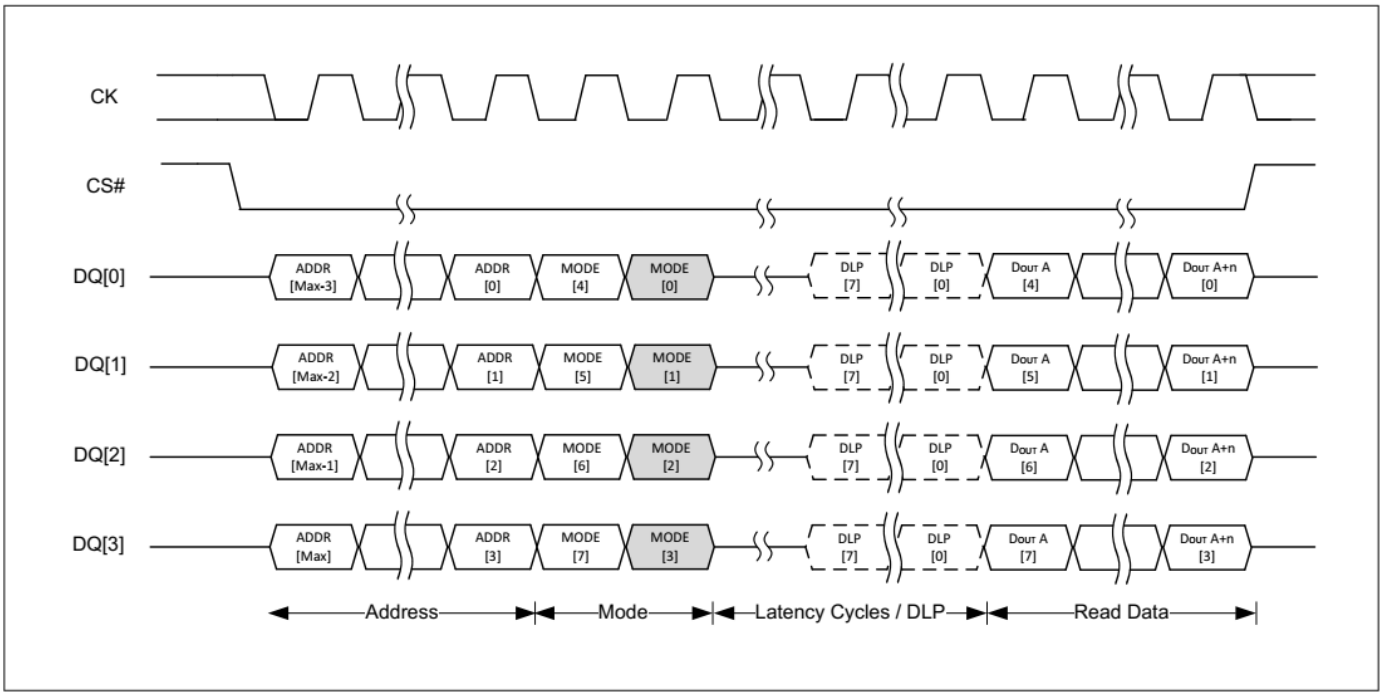

图 20　　具有地址和模式输入的 QIO SDR 连续读取传输（输出延迟） [5]

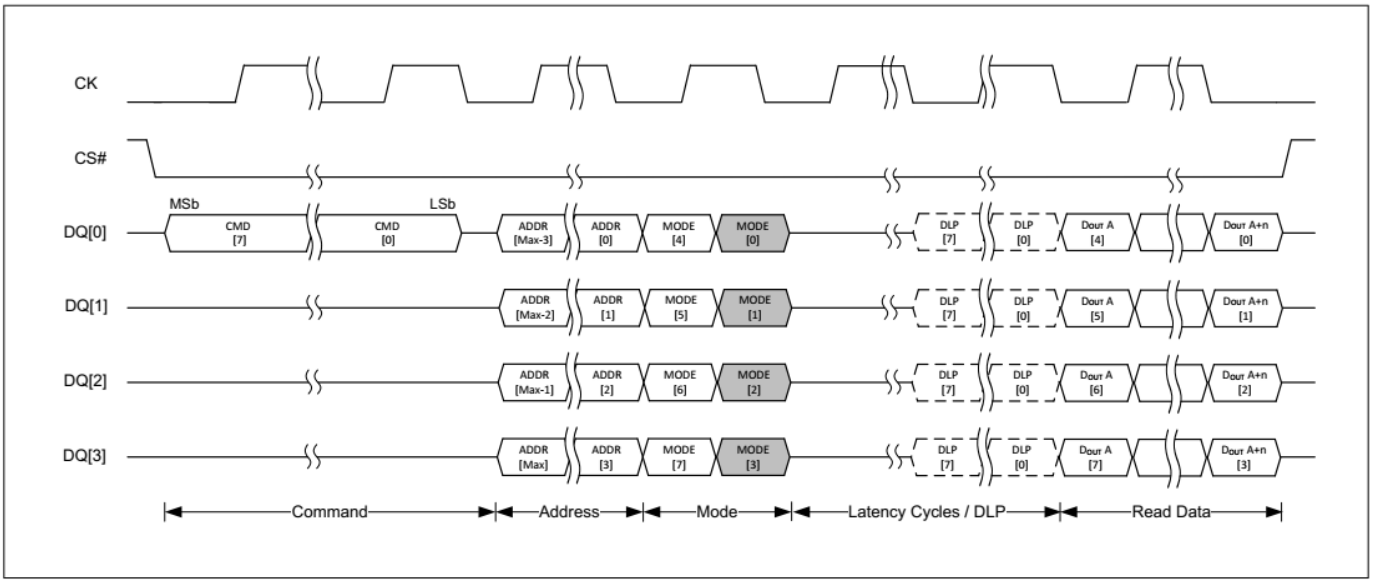

图 21　　带有指令、地址和模式输入的QIO DDR 读取传输（输出延迟）

5. 无需关注灰色位数据

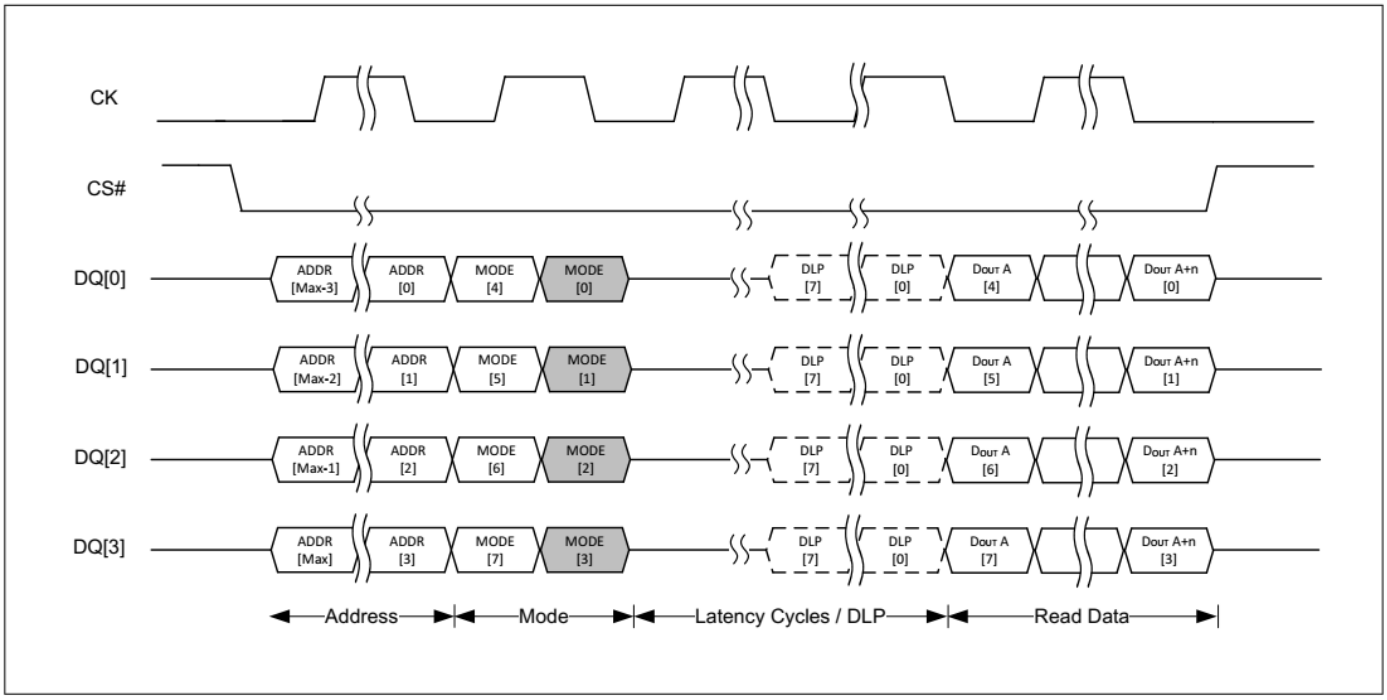

图 22　　具有地址和模式输入的 QIO DDR 连续读取传输（输出延迟）

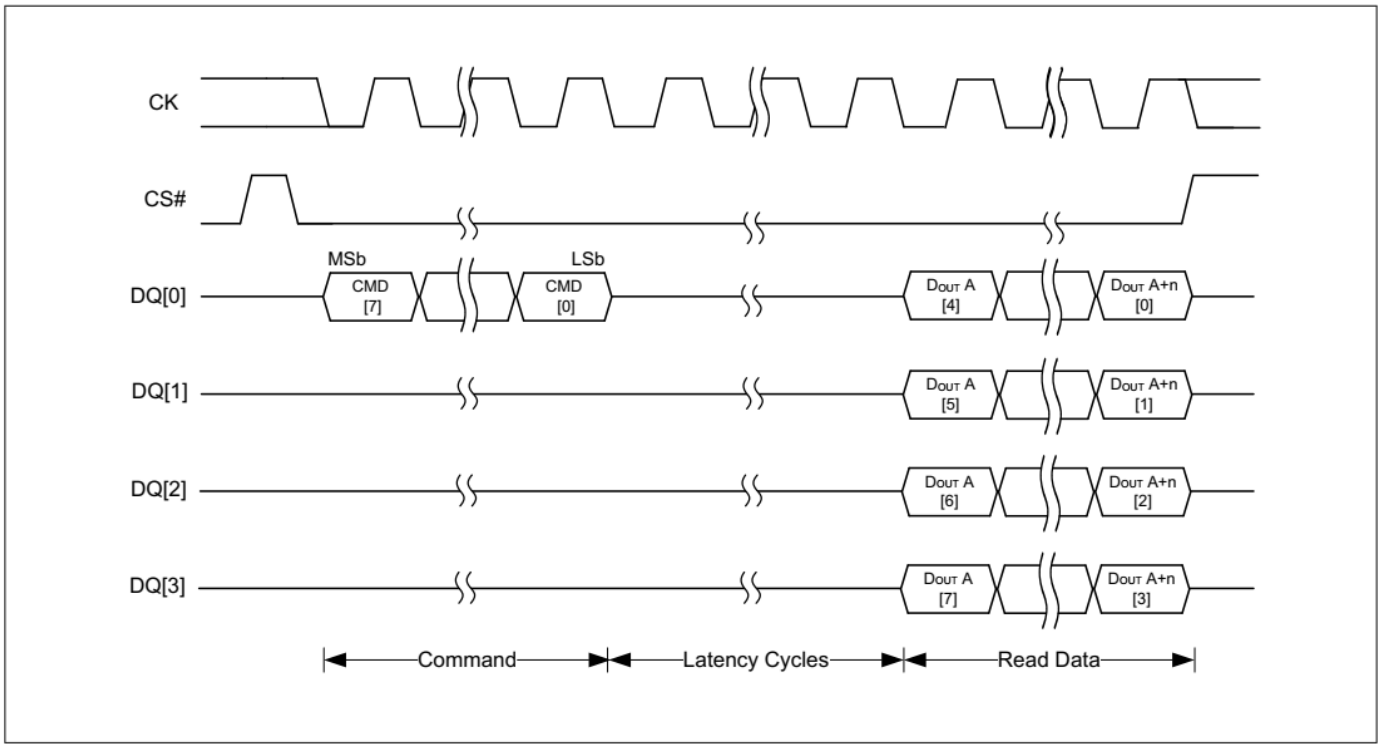

图 23　　带指令输入的四线 ID 读取传输（输出延迟）

2.3.5 四线外设接口（QPI、4S-4S-4S 和 4S-4D-4D）

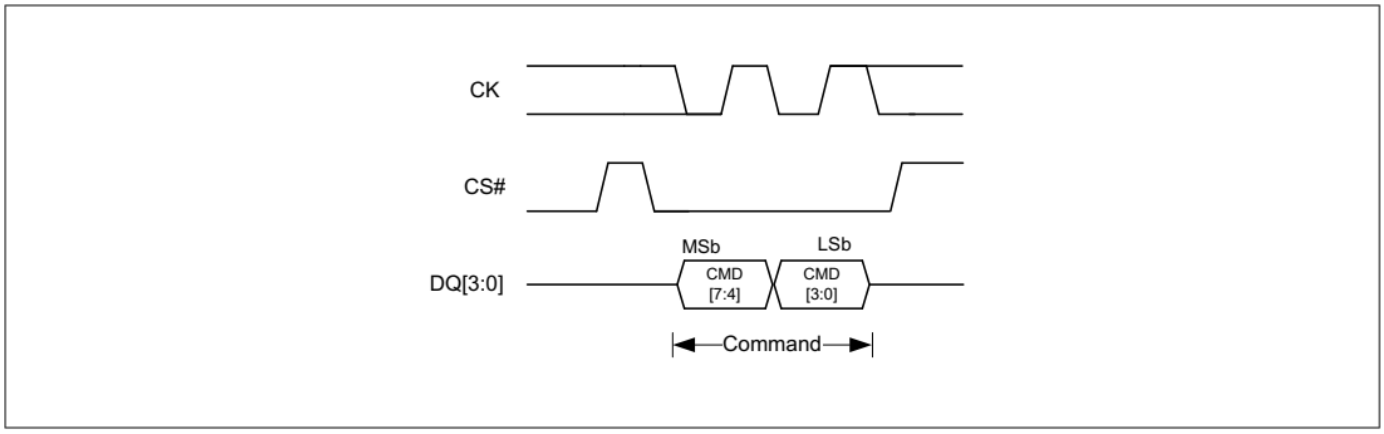

图 24　　带指令输入的 QPI SDR传输

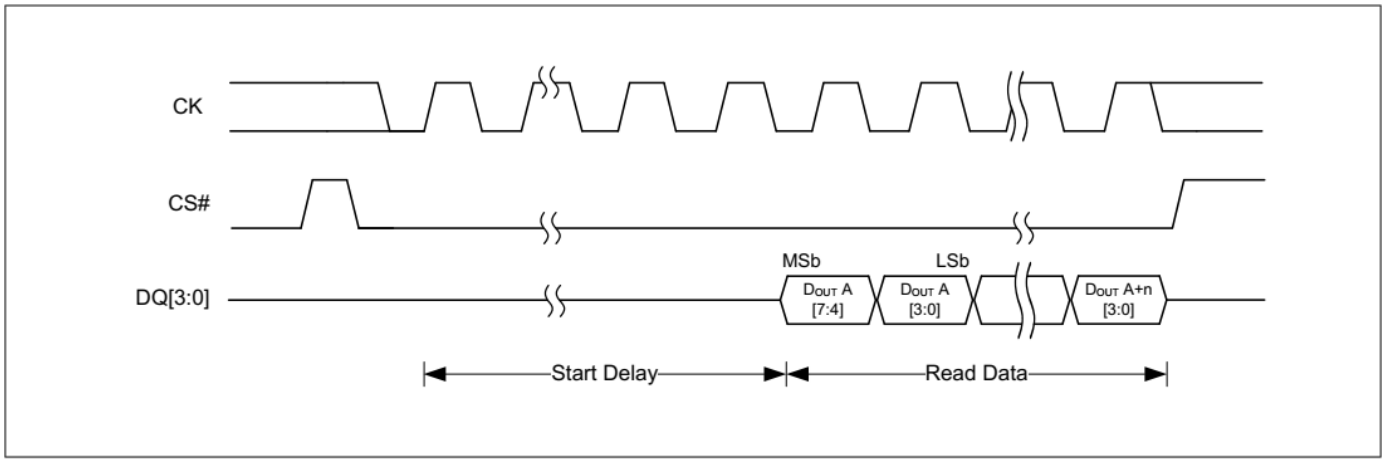

图 25　　具有输出数据序列的 QPI 传输（AutoBoot）

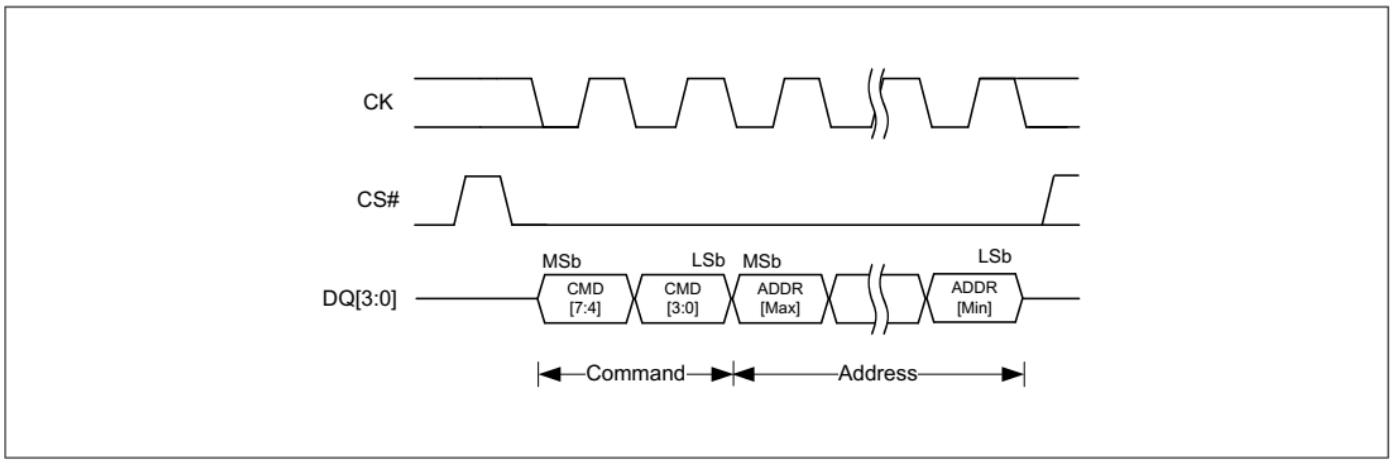

图 26　　具有指令和地址输入的 QPI SDR传输

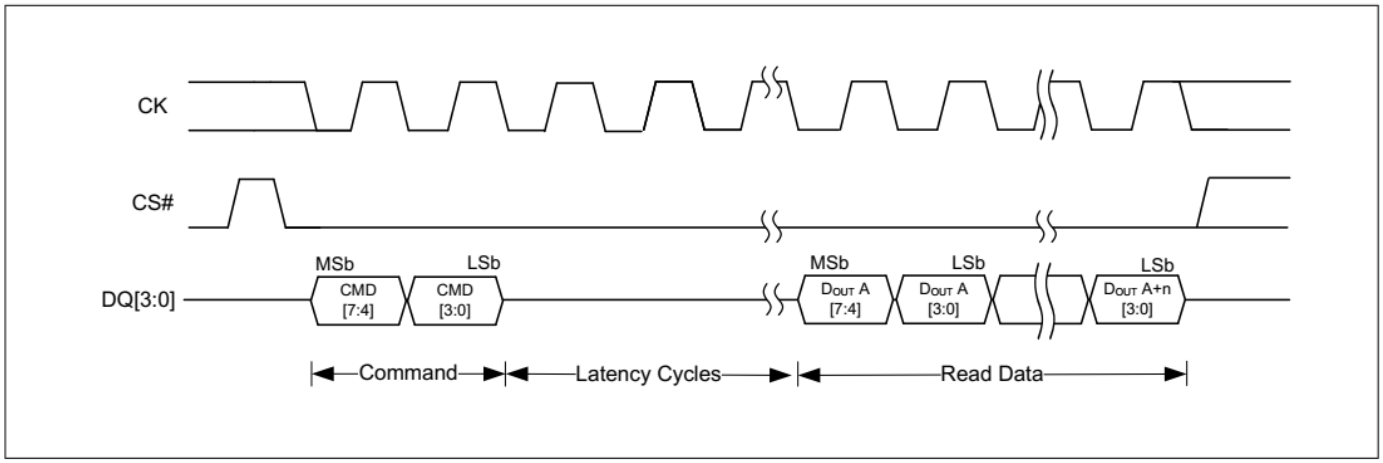

图 27　　带有指令输入的 QPI SDR读取传输（输出延迟）

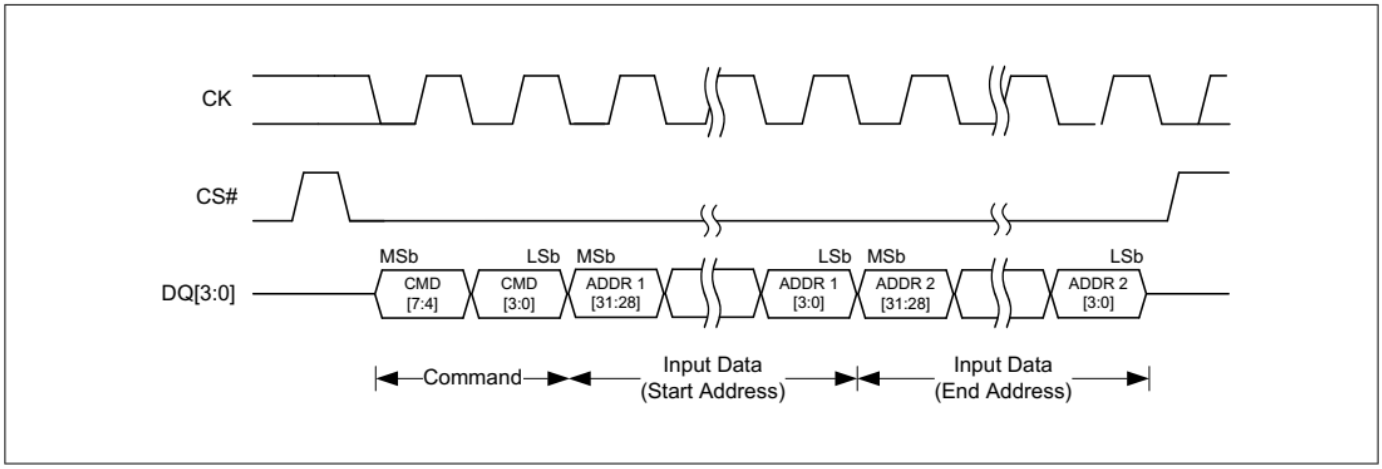

图 28　　带有指令和两个地址输入的 QPI SDR传输

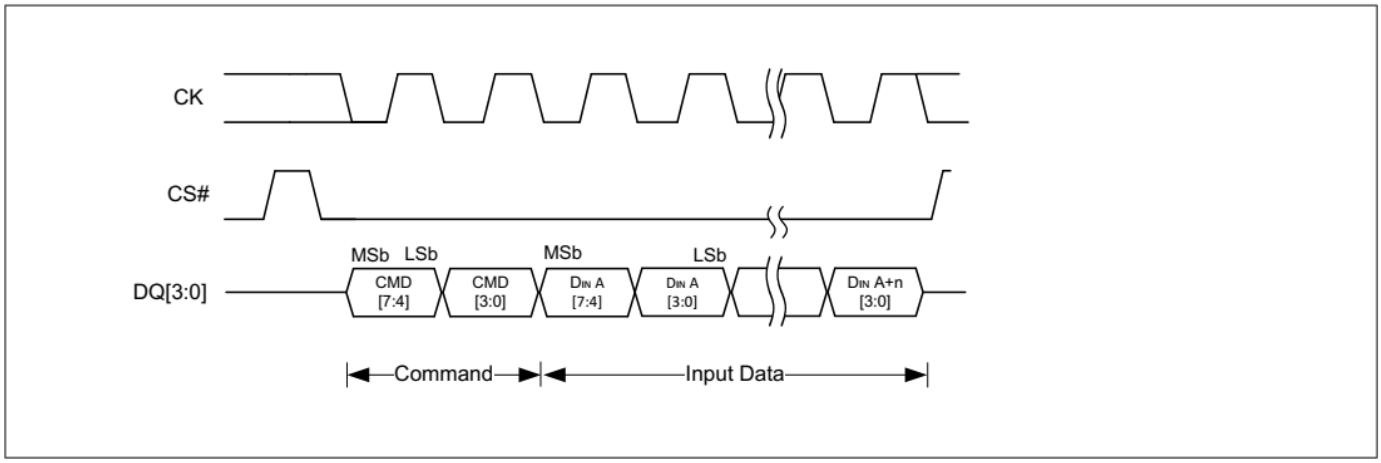

图 29　　带有指令和数据输入的 QPI SDR传输

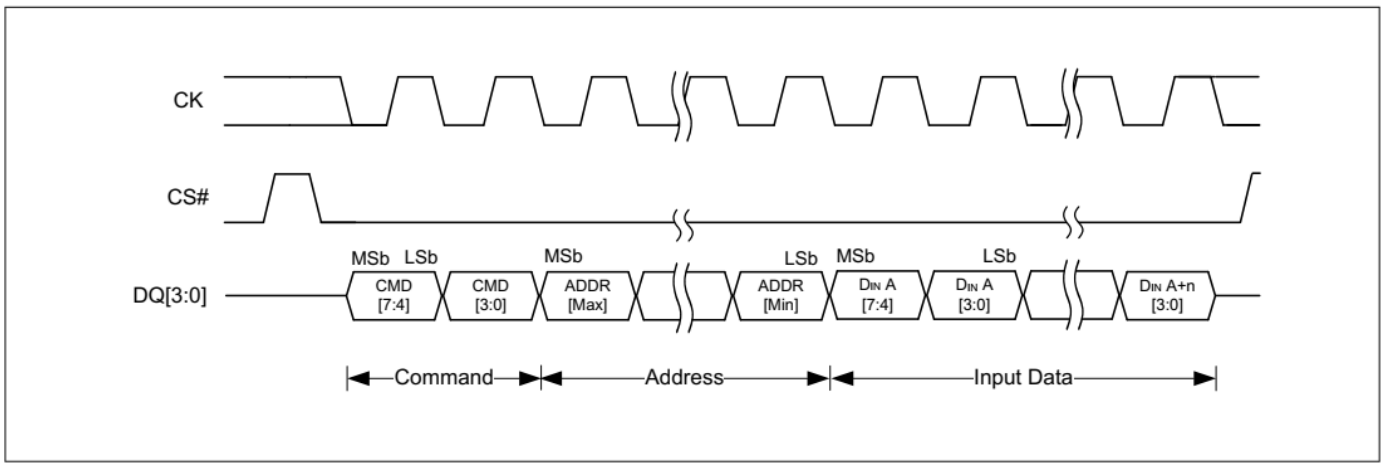

图 30　　具有指令、地址和数据输入的 QPI SDR写入传输

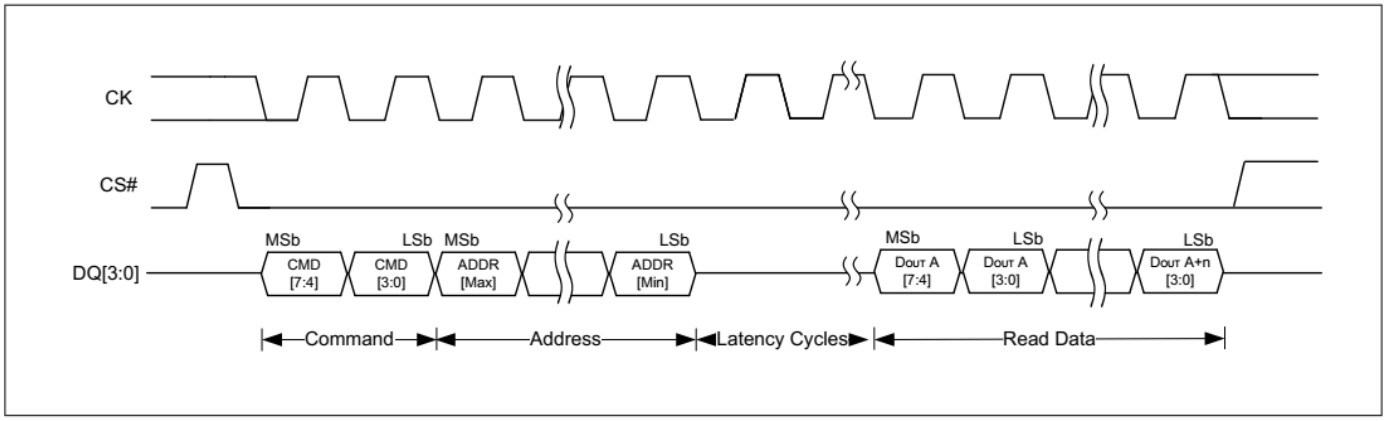

图 31　使用指令和地址输入的 QPI SDR读取传输（输出延迟）

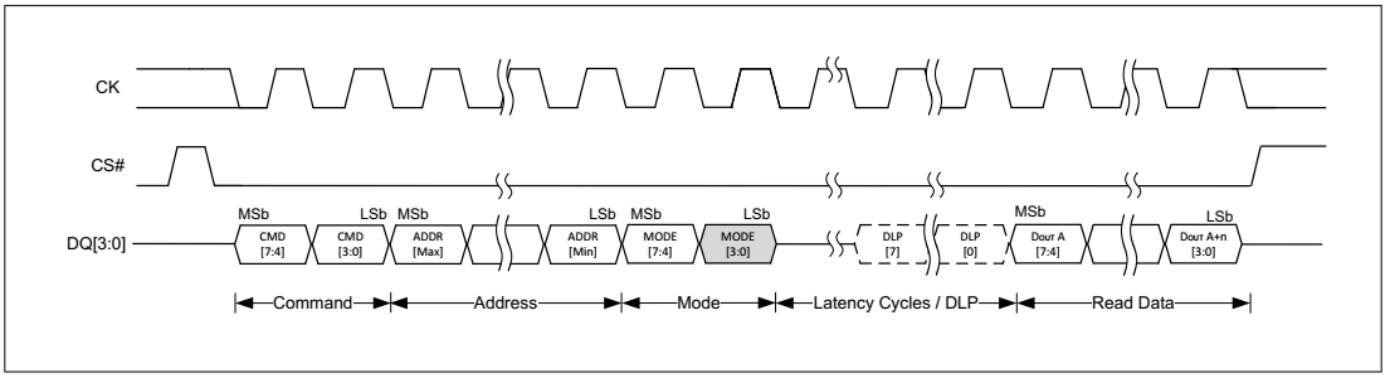

图 32　　具有指令、地址和模式输入（输出延迟）的 QPI SDR读取传输[6]

6. 无需关注灰色位数据。

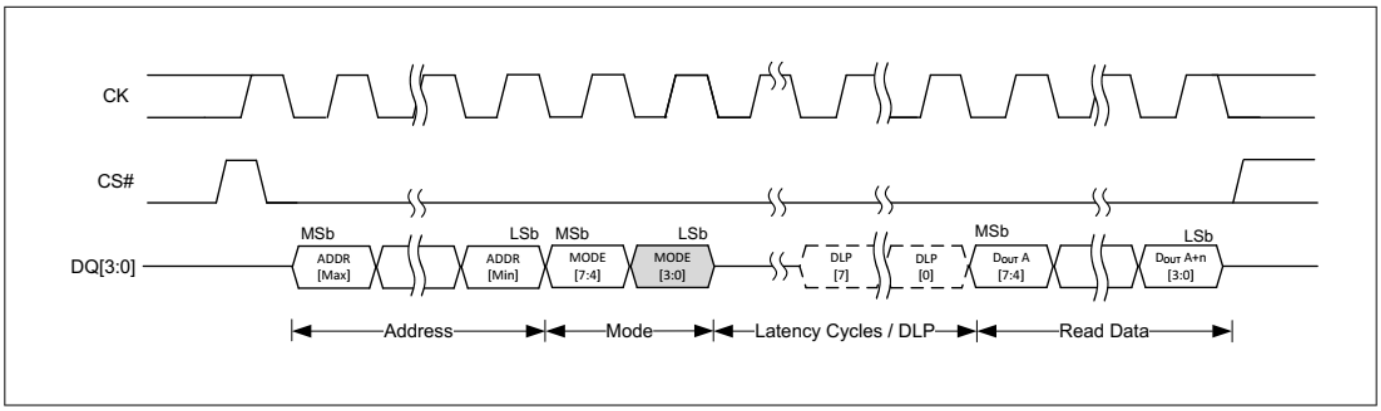

图 33　　具有地址和模式输入的 QPI SDR 连续读取传输（输出延迟） [6]

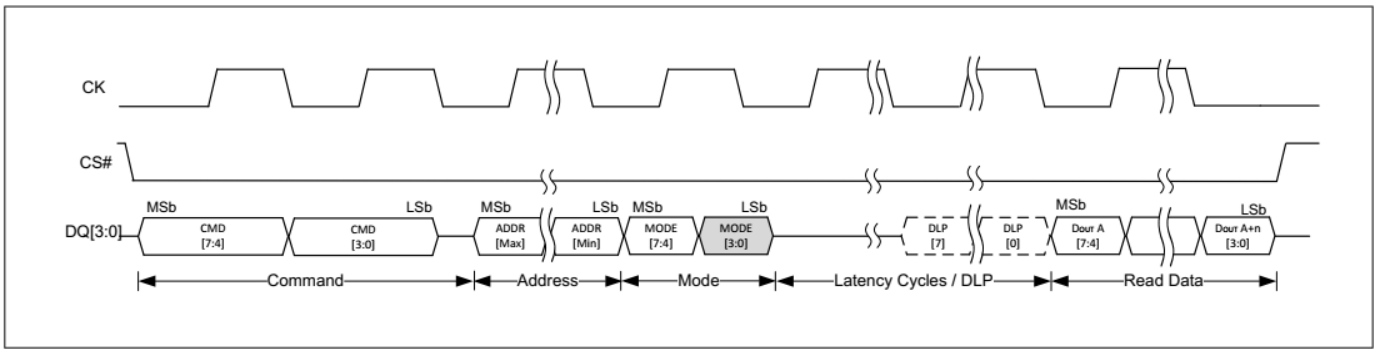

图 34　　具有指令、地址和模式输入（输出延迟）的 QPI DDR 读取传输[6]

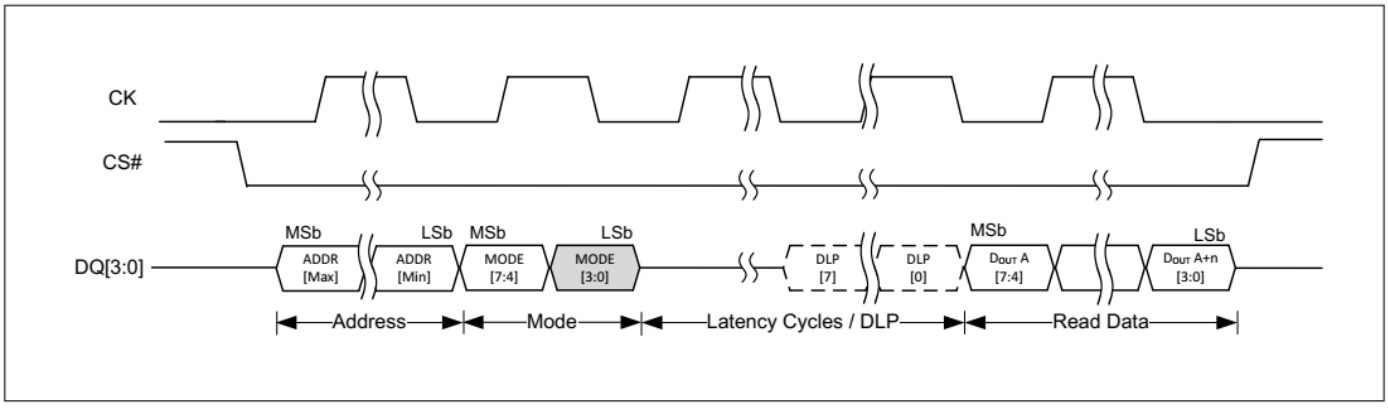

图 35　　具有地址和模式输入的 QPI DDR 连续读取传输（输出延迟） [6]

7. 无需关注灰色位数据。

2.4 寄存器命名规则

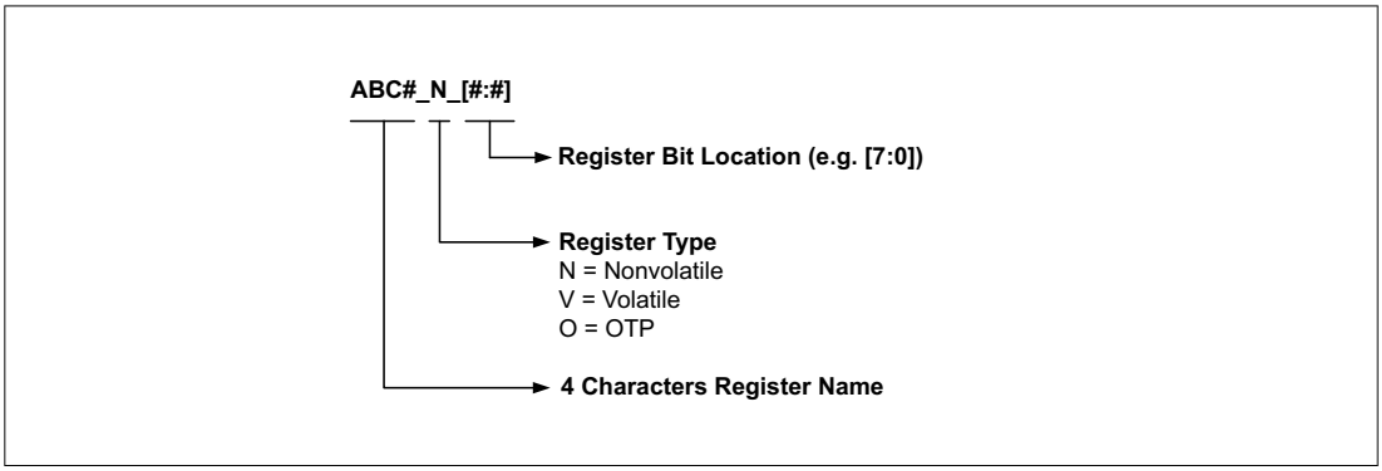

图 36 寄存器命名规则

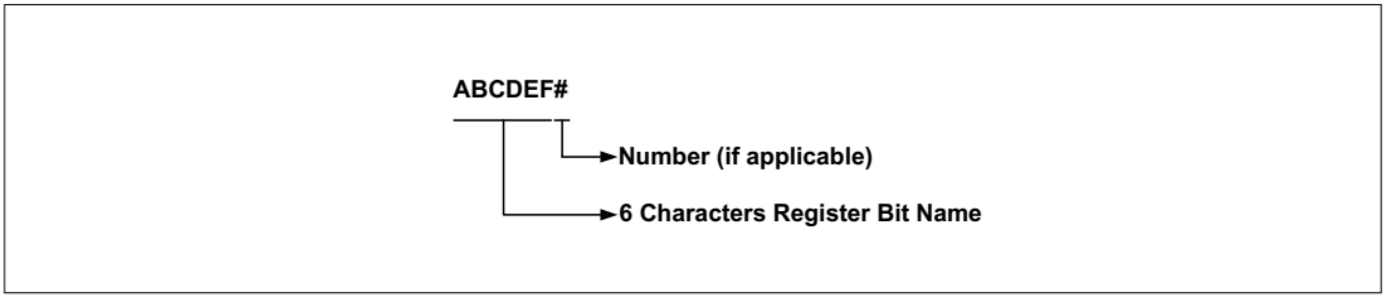

图 37 寄存器位域命名规则

2.5 命令传输命名规则

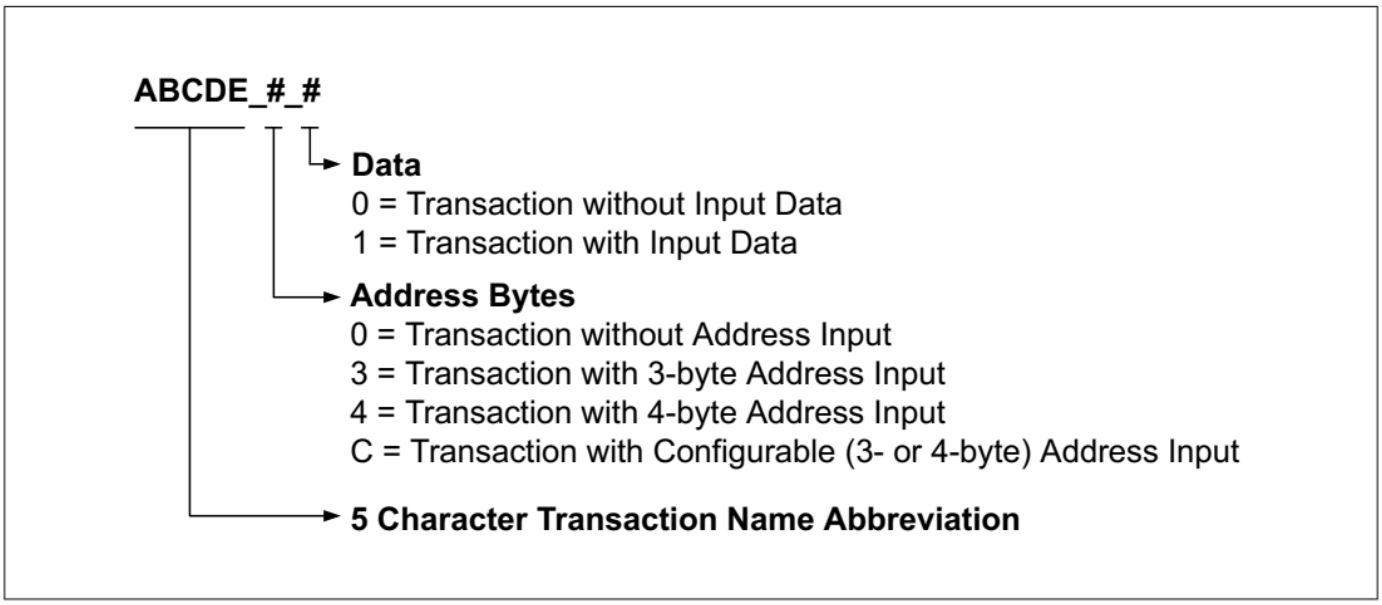

图 38 传输命名规则

3 地址空间映射

HL-T/HS-T系列支持24位和32位（4字节）地址，支持512 Mb或1 Gb容量的设备。 4 字节地址允许直接寻址最多 4 GB (32 Gb) 的地址空间。可以通过写入相应的配置寄存器来更改地址字节选项，或者也可以使用单独的传输进入（EN4BA_0_0）和退出（EX4BA_0_0）4 字节地址模式。

除了闪存存储器存储阵列以外，HL-T/HS-T 家族还包括制造商 ID、器件 ID、唯一 ID、串行闪存闪式存储器可发现参数 (SFDP)、安全存储区域 (SSR) 和寄存器的独立地址空间。

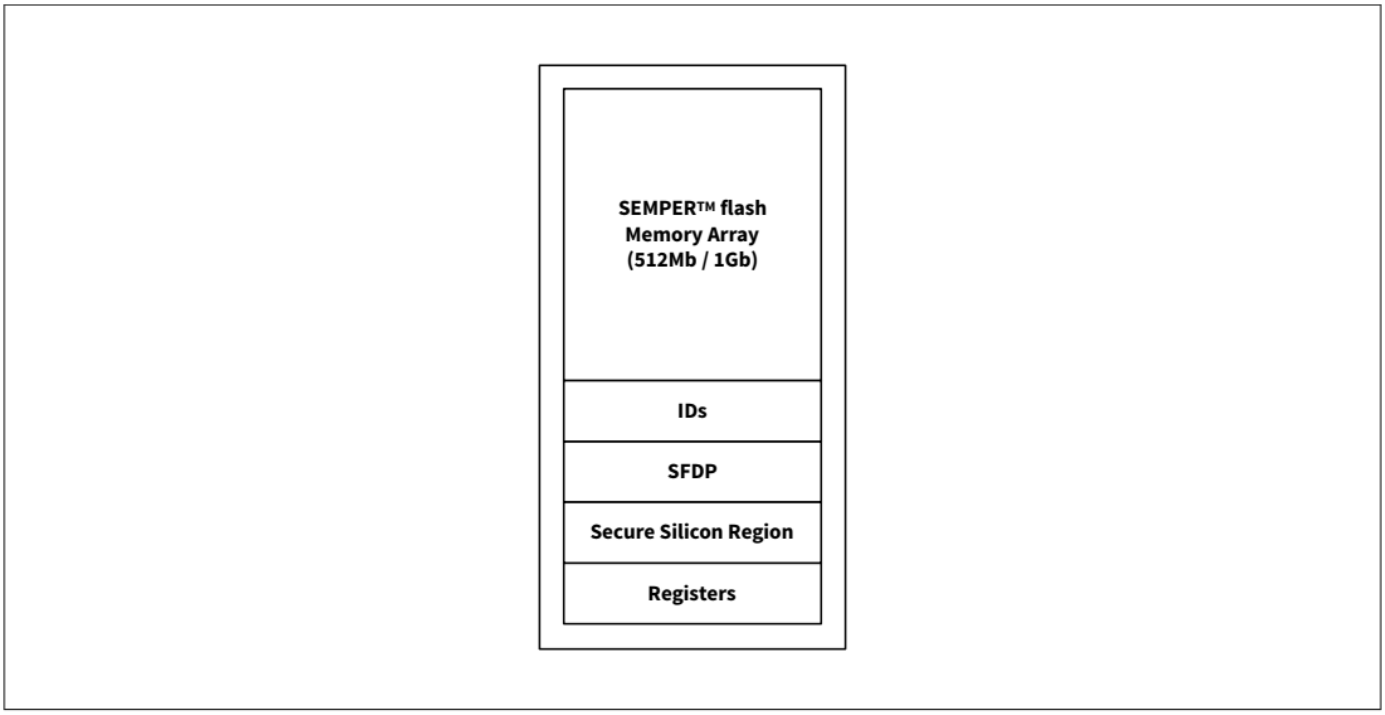

图 39 HL-T/HS-T 地址空间映射概述

3.1 SEMPER™闪存式存储器存储阵列

闪存式存储器主要的扇区结构被划分为单元并称之为物理扇区。

HL-T/HS-T系列扇区分布支持以下选项：

- 512 Mb、1 Gb 支持 256 KB 统一扇区选项
- 512 Mb、1 Gb 混合扇区选项
  - 物理的 32 个 4 KB 扇区和 1 个 128 KB 扇区配置为地址空间顶部或底部，其余所有扇区均为 256 KB
  - 地址空间的顶部和底部均设有各 16 个 4 KB 物理的扇区和 1 个 192 KB 扇区，其余所有扇区均为 256 KB

配置寄存器1和配置寄存器3中的扇区架构选择位的组合支持HL-T/HS-T家族的不同扇区架构选项。更多信息请参见“寄存器”部分章节。

表8　256 KB统一扇区地址映射[1]

Sector size (KB)	S25HL01GT and S25HS01GT			S25HL512T and S25HS512T		
	Sector count	Sector range	Byte address range (sector starting address– sector ending address)	Sector count	Sector range	Byte address range (sector starting address– sector ending address)
256	512	SA00	00000000h–0003FFFFh	256	SA00	00000000h–0003FFFFh
		:	:		:	:
		SA511	07FC0000h–07FFFFFFh		SA255	03FC0000h-03FFFFFFh

1. 配置：CFR3N[3] = 1。

表 9　底部混合配置 32 个 4 KB 扇区和 256 KB 统一扇区地址映射[1]

Sector size (KB)	S25HL01GT and S25HS01GT			S25HL512T and S25HS512T		
	Sector count	Sector range	Byte address range (sector starting address –sector ending address)	Sector count	Sector range	Byte address range (sector starting address –sector ending address)
4	32	SA00	00000000h–00000FFFh	32	SA00	00000000h–00000FFFh
		:	:		:	:
		SA31	0001F000h–0001FFFFh		SA31	0001F000h–0001FFFFh
128	1	SA32	00020000h–0003FFFFh	1	SA32	00020000h–0003FFFFh
256	511	SA33	00040000h–0007FFFFh	255	SA33	00040000h–0007FFFFh
		:	:		:	:
		SA543	07FC0000h–07FFFFFFh		SA287	03FC0000h–03FFFFFFh

1. 配置：CFR3N[3] = 0，CFR1N[6] = 0，CFR1N[2] = 0。

表 10　顶部混合配置 32 个 4 KB 扇区和 256 KB 统一扇区地址映射[1]

Sector size (KB)	S25HL01GT and S25HS01GT			S25HL512T and S25HS512T		
	Sector count	Sector range	Byte address range (sector starting address –sector ending address)	Sector count	Sector range	Byte address range (sector starting address –sector ending address)
256	511	SA00	00000000h–0003FFFFh	255	SA00	00000000h–0003FFFFh
		:	:		:	:
		SA510	07F80000h–07FBFFFFh		SA254	03F80000h–03FBFFFFh
128	1	SA511	07FC0000h–07FDFFFFh	1	SA255	03FC0000h–03FDFFFFh
4	32	SA512	07FE0000h–07FE0FFFh	32	SA256	03FE0000h–03FE0FFFh
		:	:		:	:
		SA543	07FFF000h–07FFFFFFh		SA287	03FFF000h–03FFFFFFh

1. 配置：CFR3N[3] = 0，CFR1N[6] = 0，CFR1N[2] = 1。

表 11　　混合配置 2 底部十六个和顶部十六个 4 KB 扇区地址映射[1]

Sector size (KB)	S25HL01GT and S25HS01GT			S25HL512T and S25HS512T		
	Sector count	Sector range	Byte address range (sector starting address– sector ending address)	Sector count	Sector range	Byte address range (sector starting address– sector ending address)
4	16	SA00	00000000h–00000FFFh	16	SA00	00000000h–00000FFFh
		:	:		:	:
		SA15	0000F000h–0000FFFFh		SA15	0000F000h–0000FFFFh
192	1	SA16	00010000h–0003FFFFh	1	SA16	00010000h–0003FFFFh
256	510	SA17	00040000h–0007FFFFh	254	SA17	00040000h–0007FFFFh
		:	:		:	:
		SA526	07F80000h–07FBFFFFh		SA270	03F80000h–03FBFFFFh
192	1	SA527	07FC0000h–07FEFFFFh	1	SA271	03FC0000h–03FEFFFFh
4	16	SA528	07FF0000h–07FF0FFFh	16	SA272	03FF0000h–03FF0FFFh
		:	:		:	:
		SA543	07FFF000h–07FFFFFFh		SA287	03FFF000h–03FFFFFFh

1. 配置：CFR3N[3] = 0，CFR1N[6] = 1。

这些是使用几个扇区作为参考的简明表格。有一些地址范围未明确列出。所有 4 KB 扇区地址类型为 xxxxx000h–xxxxxFFFh。所有 256 KB 扇区地址类型为 xxx00000h–xxx3FFFFh、xxx40000h–xxx7FFFFh、xx80000h–xxxCFFFFh 或 xxD0000h–xxxFFFFFh。

3.2　　ID地址空间

存储器的这个特定区域被分配给制造商、器件和唯一标识：

- 制造商标识由 JEDEC 指定（见表 95）。
- 器件标识由 Infineon 分配（见表 95）。
- 64 比特位唯一编号位于唯一器件 ID 地址空间的 8 个字节中。此唯一 ID 可用作软件可读的序列号，该序列号对于每个器件都是唯一的（见表 96）。

没有为这些 ID 定义地址空间，因为只能通过提供相应的命令传输来读取它们。读取这些ID的传输不需要地址。该地址空间中的数据是只读数据。

3.3　　JEDEC JESD216串行闪存可发现参数(SFDP)空间

SFDP 标准提供了一种一致的方法，在内部参数表的标准设置中描述该串行闪存式存储器装置的功能和特性。主控系统软件可以查询这些参数表，以进行所需的调整，以适应不同的功能。SFDP 地址空间有一个从地址零开始的帧头，用于标识 SFDP 数据结构并为每个参数提供指针。 SFDP 地址空间由英飞凌烧录，对于主控系统是只读的（见表 91 至表 94）。

表 12 SFDP 地址映射概述

Byte address	Description
0000 h	Location zero within JEDEC JESD216D SFDP space - start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
0100 h	Start of SFDP parameter tables The SFDP parameter table data starting at 0100h
...	Remainder of SFDP parameter tables followed by either more parameters or undefined space

3.4 SSR 地址空间

每个 HS/L-T 家族存储器器件都有一个 1024 字节的安全存储区域，即OTP地址空间。 该地址空间与主闪存式存储器阵列是分开的。SSR 区域分为 32 个可单独锁定、32 字节对齐和长度的区域。

在从零地址开始的 32 字节区域中：

- 最低 16 个字节包含 128 位随机数。该随机数无法写入、擦除或烧录，任何尝试都会返回 PRGERR 标志。
- 接下来的 4 个字节用于为每个安全区域提供一个比特位（总共 32 位），一旦将位设置为“0”，便可永久防止其被写入、擦除或烧录。
- 所有其他字节均被保留。

剩余区域在从英飞凌出厂时会被擦除，并可用于对额外的永久性数据进行编程。

表 13 SSR 地址映射

Region	Byte address range	Contents	Initial delivery state
Region 0	000 h	LSB of Infineon Programmed Random Number	Infineon Programmed Random Number
	...	...	
	00 Fh	MSB of Infineon Programmed Random Number	
	010 h to 013 h	Region Locking Bits Byte 10 h [bit 0] locks region 0 from programming when = 0 ... Byte 13 h [bit 7] locks region 31 from programming when = 0	All Bytes = FFh
	014 h to 01 Fh	Reserved for future use (RFU)	All Bytes = FFh
Region 1	020 h to 03 Fh	Available for User Programming	All Bytes = FFh
Region 2	040 h to 05 Fh	Available for User Programming	All Bytes = FFh
...	...	Available for User Programming	All Bytes = FFh
Region 31	3E0h to 3FFh	Available for User Programming	All Bytes = FFh

3.5 寄存器

寄存器是一小组存储器单元，用于配置 HS/LT 系列存储器器件的操作方式，或报告器件操作的状态。寄存器通过特定的指令和地址来访问。表 14 显示该器件中每个可用寄存器的地址映射。

表 14 寄存器地址映射

Function	Register type	Register name	Volatile component address (hex)	Nonvolatile component address (hex)
Device Status	Status Register 1	STR1N[7:0], STR1V[7:0]	0x00800000	0x00000000
	Status Register 2	STR2V[7:0]	0x00800001	N/A
Device Configuration	Configuration Register 1	CFR1N[7:0], CFR1V[7:0]	0x00800002	0x00000002
	Configuration Register 2	CFR2N[7:0], CFR2V[7:0]	0x00800003	0x00000003
	Configuration Register 3	CFR3N[7:0], CFR3V[7:0]	0x00800004	0x00000004
	Configuration Register 4	CFR4N[7:0], CFR4V[7:0]	0x00800005	0x00000005
Infineon Endurance Flex architecture	Infineon Endurance Flex architecture Selection Register 0 [1:0]	EFX0O[1:0]	N/A	0x00000050
	Infineon Endurance Flex architecture Selection Register 1 [7:0]	EFX1O[7:0]	N/A	0x00000052
	Infineon Endurance Flex architecture Selection Register 1 [10:8]	EFX1O[10:8]	N/A	0x00000053
	Infineon Endurance Flex architecture Selection Register 2 [7:0]	EFX2O[7:0]	N/A	0x00000054
	Infineon Endurance Flex architecture Selection Register 2 [10:8]	EFX2O[10:8]	N/A	0x00000055
	Infineon Endurance Flex architecture Selection Register 3 [7:0]	EFX3O[7:0]	N/A	0x00000056
	Infineon Endurance Flex architecture Selection Register 3 [10:8]	EFX3O[10:8]	N/A	0x00000057
	Infineon Endurance Flex architecture Selection Register 4 [7:0]	EFX4O[7:0]	N/A	0x00000058

（表格续下页……）

表 14　　（续）寄存器地址映射

Function	Register type	Register name	Volatile component address (hex)	Nonvolatile component address (hex)
	Infineon Endurance Flex architecture Selection Register 4 [10:8]	EFX4O[10:8]	N/A	0x00000059
Error Correction	ECC Status Register	ESCV[7:0]	0x00800089	N/A
	ECC Error Detection Count Register [7:0]	ECTV[7:0]	0x0080008A	
	ECC Error Detection Count Register [15:8]	ECTV[15:8]	0x0080008B	
	ECC Address Trap Register [7:0]	EATV[7:0]	0x0080008E	
	ECC Address Trap Register [15:8]	EATV[15:8]	0x0080008F	
	ECC Address Trap Register [23:16]	EATV[23:16]	0x00800040	
	ECC Address Trap Register [31:24]	EATV[31:24]	0x00800041	
AutoBoot	AutoBoot Register [7:0]	ATBN[7:0]	N/A	0x00000042
	AutoBoot Register [15:8]	ATBN[15:8]		0x00000043
	AutoBoot Register [23:16]	ATBN[23:16]		0x00000044
	AutoBoot Register [31:24]	ATBN[31:24]		0x00000045
Data Learning	Data Learning Register [7:0]	DLPN[7:0], DLPV[7:0]	0x00800010	0x00000010
Erase Count	Sector Erase Count Register [7:0]	SECV[7:0]	0x00800091	N/A
	Sector Erase Count Register [15:8]	SECV[15:8]	0x00800092	
	Sector Erase Count Register [23:16]	SECV[23:16]	0x00800093	
Data Integrity Check	Data Integrity Check CRC Register [7:0]	DCRV[7:0]	0x00800095	
	Data Integrity Check CRC Register [15:8]	DCRV[15:8]	0x00800096	
	Data Integrity Check CRC Register [23:16]	DCRV[23:16]	0x00800097	
	Data Integrity Check CRC Register [31:24]	DCRV[31:24]	0x00800098	

（表格续下页……）

表 14　　（续）寄存器地址映射

Function	Register type	Register name	Volatile component address (hex)	Nonvolatile component address (hex)
Protection and Security	Advanced Sector Protection Register [7:0]	ASPO[7:0]	N/A	0x00000030
	Advanced Sector Protection Register [15:8]	ASPO[15:8]		0x00000031
	ASP PPB Lock Register (Persistent Protection Block)	PPLV[7:0]	0x0080009B	N/A
	ASP Password Register [7:0]	PWDO[7:0]	N/A	0x00000020
	ASP Password Register [15:8]	PWDO[15:8]		0x00000021
	ASP Password Register [23:16]	PWDO[23:16]		0x00000022
	ASP Password Register [31:24]	PWDO[31:24]		0x00000023
	ASP Password Register [39:32]	PWDO[39:32]		0x00000024
	ASP Password Register [47:40]	PWDO[47:40]		0x00000025
	ASP Password Register [55:48]	PWDO[55:48]		0x00000026
	ASP Password Register [63:56]	PWDO[63:56]		0x00000027

4 特性

4.1 错误检测和纠正

HL-T/HS-T系列设备通过在存储器阵列写入期间生成嵌入式汉明纠错码来支持错误检测和纠正。然后，该 ECC 代码用于读取操作期间的错误检测和纠正。ECC基于 16 字节数据单位。当 16 字节数据单位被加载到写入缓存并传输到 128 比特位队列线进行写入时（在擦除操作之后），每个数据单位的 8 比特位ECC也被写入到主控系统软件不可见的存储器阵列部分中。 然后在每次读取操作期间检查此ECC信息。数据单位内的 1 比特位错误将由ECC逻辑纠正。16字节数据单位是启用ECC最小写入颗粒度。

当在 16 字节数据单位中首次编程任意数量的数据时，计算的ECC是整个数据单位的数值。如果随后将附加数据编程到相同的数据单位中，但没有擦除，则该数据单位的ECC被禁用，并且 1 比特的ECC禁用位会被置位。需要扇区擦除操作才能再次对该数据单位启用 ECC 功能。

这些是对用户公开的自动操作。无感的ECC特性增强了向每个数据单位写入一次数据这种典型写入操作的数据可靠性，同时还通过仍然允许单字节写入和比特位遍历（在这种情况下， ECC将被禁用）这种相同的数据单位被多次写入的方式来提升与前几代产品的软件兼容性。

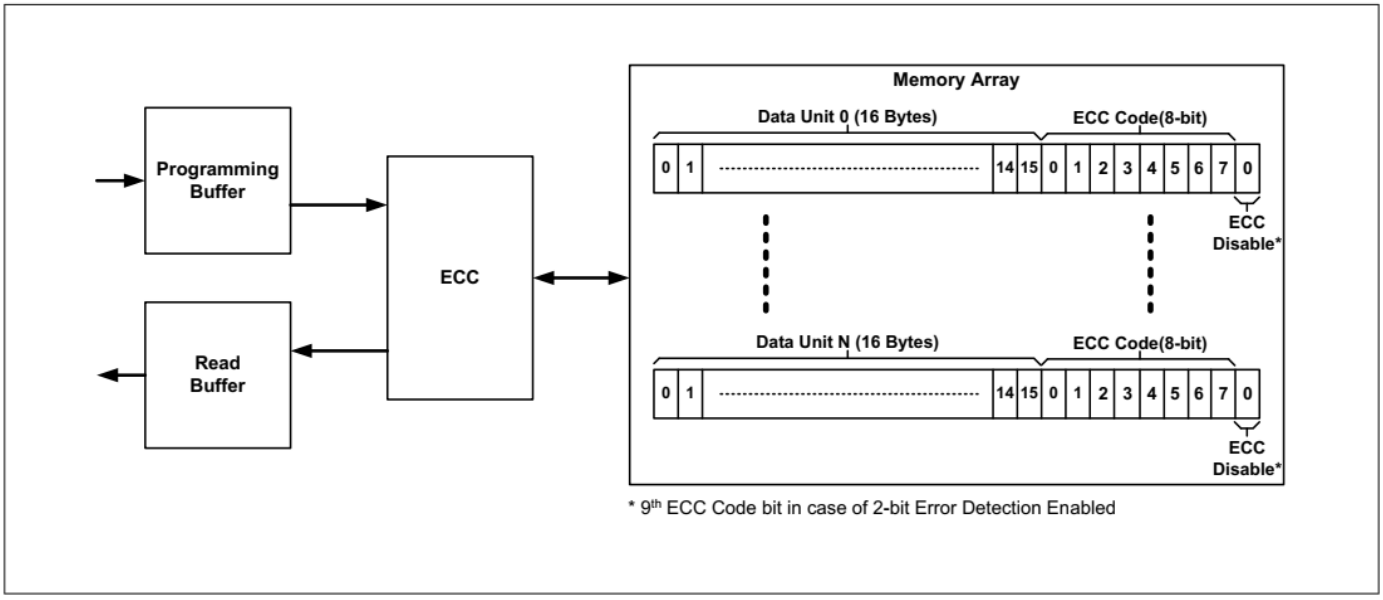

图 40 16 字节ECC数据单位示例

SEMPER™ NOR 闪存存储器默认支持 2 位错误检测的 ECC 配置。在此配置下，任何数据单位中的 1 比特位错误得到纠正，并且任何 2比特位错误都被检测并报告。 16 字节单位数据需要 9 比特位纠错码以进行 2 比特位错误检测。当启用 2 比特位错误检测时，不允许对同一数据单元（无擦除）进行字节写入、比特位遍历或多次写入操作，这将导致写入错误。将 ECC 模式从 1 比特位错误检测更改为 2 比特位错误检测，或从 2 比特位错误检测更改为 1 比特位错误检测将使内存阵列中的所有数据无效。当改变ECC模式时，主控必须先将器件中的所有扇区内的数据擦除。如果在未擦除已写入数据的情况下更改 ECC 模式，则后续读取操作将导致未定义的行为。

4.1.1 ECC错误报告

当检测到ECC错误时，有四种方法可以向主控系统报告。

- ECC数据单位状态提供数据单位中 1 比特位或 2 比特位错误的状态。
- ECC状态寄存器提供自上次ECC清零或复位以来1比特位或2比特位错误的状态。
- ECC地址捕获寄存器捕获在POR或复位后遇到的存储器阵列读取期间第一个ECC错误的地址位置。
- ECC 错误检测计数器会记录读取过程中数据单位中发生的 1 比特位或 2 比特位错误的数量。

4.1.1.1 ECC数据单元状态 (EDUS)

- 每个数据单元中的ECC状态由8比特位ECC数据单位状态提供。
- ECC状态传输输出所寻址的数据单位的ECC状态。 ECC数据单元状态的内容则指示对于所选择的数据单位，是否存在已纠正的1比特位错误、检测到的2比特位错误、或针对该数据单元的ECC是否已经被禁用。

表 15 ECC数据单位状态

Bits	Field name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EDUS[7:4]	RESRVD	Reserved For future use	V => R	0000	These bits are Reserved for future use.
EDUS[3]	ECC2BD	ECC Error 2-bit Error Detection Flag	V => R	0	This bit indicates whether a two bit error is detected in the data unit, if two bit ECC error detection is enabled CFR4V[3] = 1. When CFR4V[3] = 0 and 2-bit error detection is disabled, ECC2BD bit will always be '0'. ***Note**: If 2 bit error detection is enabled (CFR4V[3] = 1), the ECCOFF bit will not be set to 1b while performing single byte programming or bit walking in a data unit that was already partially programmed. An attempt to do such byte programming or bit walking will result in a Program Error.* Selection options: 1 = Two Bit Error detected 0 = No error
EDUS[2]	RESRVD	Reserved For future use	V => R	0	This bit is Reserved for future use.

（表格续下页……）

表 15 （续）ECC 数据单元状态

Bits	Field name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EDUS[1]	ECC1BC	ECC Error 1-bit Error Detection and Correction Flag	V => R	0	This bit indicates whether an error was corrected in the data unit. Selection options: 1 = Single Bit Error corrected in the addressed data unit 0 = No single bit error was corrected in the addressed data unit
EDUS[0]	ECCOFF	Data Unit ECC OFF/ON Flag	V => R	0	This bit indicates whether the ECC syndrome is OFF in the data unit. Selection options: 1 = ECC is OFF in the selected data unit 0 = ECC is ON in the selected data unit Dependency: CFR4x[3]

4.1.1.2 ECC 状态寄存器 (ECSV)

- 8 比特位ECC状态寄存器提供自上次ECC清零或复位后正常读取期间 1 比特位或 2 比特位错误的状态。ECC 状态寄存器没有用户可编程的非易失性比特位，所有定义的比特位都是易失性的只读比特位。这些位的默认状态是由硬件置位的。
- 可以通过 Read Any Register 命令来访问 ECC 状态寄存器。基于 Read Any Register 的 ECSV 的正确序列读取如下：
  - 使用任意读取操作从内存阵列读取数据
  - ECSV 由器件更新
  - ECSV 通过 Read Any Register 命令提供自上次清零、复位或复位以来任何ECC事件的状态。
- ECSV 通过POR 、 JEDEC串行闪存器件复位信号协议、硬件/软件复位或清除ECC状态复位操作来清除。

4.1.1.3 ECC 错误地址捕获 (EATV)

- 一个 32 比特位寄存器用于在读取闪存式存储器阵列单元期间首先遇到ECC错误时来捕获相应ECC数据单位地址。仅

  在POR 、硬件复位或ECC清零、复位传输后遇到的第一个使能的ECC错误类型（“仅 2 比特位”或“1 比特位或 2比特位”，取决于 CFR4N[3] 中选择）时的地址。EATV 寄存器仅在读取传输期间更新。

EATV 寄存器包含检测到错误时访问的地址。故障位可能并不位于寄存器中指示的当前地址，而是位于检测到错误所在的对齐 16 字节ECC数据单位内。如果在单次读取操作期间在多个ECC数据单位中发现错误，则仅在 EATV 寄存器中捕获第一个失败的ECC单位的地址。

- 清除ECC状态寄存器传输、 POR或JEDEC信号协议/硬件/软件复位会清除地址捕获寄存器。

4.1.1.4 ECC错误检测计数器（ECTV）

- 一个16位寄存器用于计数从闪存阵列读取数据时发生的1比特位或2比特位错误的数量。
  只有在主阵列中识别的错误才会导致错误检测计数器递增。ECTV 寄存器仅在读取传输期间更新。读取 ECC 状态传输不会影响 ECTV 寄存器。

16 比特位错误检测计数器将不会递增超过 FFFFh。然而，ECC 仍在继续发挥作用。

请注意在连续读取操作期间，当检测到 1 比特位或 2 比特位错误时，时钟可能会继续切换，并且存储器器件将继续增加数据地址并将新数据放置在 DQ 信号上；遇到的任何带有错误的额外数据单元都将被计数，直到 CS# 恢复为高电平。

在读取命令传输期间，对于发现错误的每个数据单位，仅计为一个错误。 每个读取传输将导致目标数据单位的新读取。如果多个读取命令传输访问包含错误的相同数据单位，则每次读取该数据单位时，错误计数器将递增。

当 2 比特位错误检测未启用且同一数据单位被写入多次时，该数据单位的ECC错误检测将被禁用，因此无法识别或计数错误。

- 可以使用 Read Any Register 命令来读取 ECC 错误检测计数器寄存器。
- ECTV 寄存器在POR 、 JEDEC信号协议/硬件/软件复位或者使用清除ECC状态寄存器时置位为 0。

4.1.2 ECC 相关寄存器和命令传输

表16 ECC相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Configuration Register - 4 (CFR4N, CFR4V) (see Table 58)	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
ECC Status Register (ECSV) (see Table 61)	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)
ECC Address Trap Register (EATV) (see Table 62)	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)
ECC Error Detection Counter Register (ECTV) (see Table 63)	Read ECC Status (RDECC_4_0, RDECC_C_0)	Read ECC Status (RDECC_4_0, RDECC_C_0)
	Clear ECC Status Register (CLECC_0_0)	Clear ECC Status Register (CLECC_0_0)

4.2 英飞凌 Endurance Flex 架构（负载均衡）

英飞凌 Endurance Flex 架构允许将主存储器阵列划分为可配置成高耐久性或长数据保留时间的区域。英飞凌 Endurance Flex 架构在高耐久性区域实现负载均衡，其中写入/擦除周期均匀分布在负载均衡池的所有

扇区中。通过避免单个扇区的过早磨损，这极大地提高了器件的可靠性。

从架构上看，英飞凌 Endurance Flex 架构的负载均衡算法基于逻辑扇区到物理扇区的映射。在部件的使用寿命周期内，此映射会发生改变，以保持所有物理扇区的写入/擦除周期的均匀分布。逻辑到物理的映射信息存储在专用的闪存式存储器阵列中，该阵列在交换扇区时更新。当擦除操作时，会发生扇区交换。

英飞凌 Endurance Flex 架构的高耐用区域要求至少设置 20 个扇区。 为了在配置长数据保留时间、高耐久性或两个区域之间提供灵活性，提供了四个指针边界架构。出厂默认设置将所有扇区指定为高耐久性，作为负载均衡池的一部分，并且所有指针边界均被禁用。这四个指针边界最多可用于划分成五个区域，每个区域均可配置为长数据保留时间或高耐久性。

图 41 概述了英飞凌 Endurance Flex 架构。它显示了基于不同扇区架构的五个可能区域。

注释：
1. 4 KB 扇区不属于英飞凌 Endurance Flex 架构的一部分。

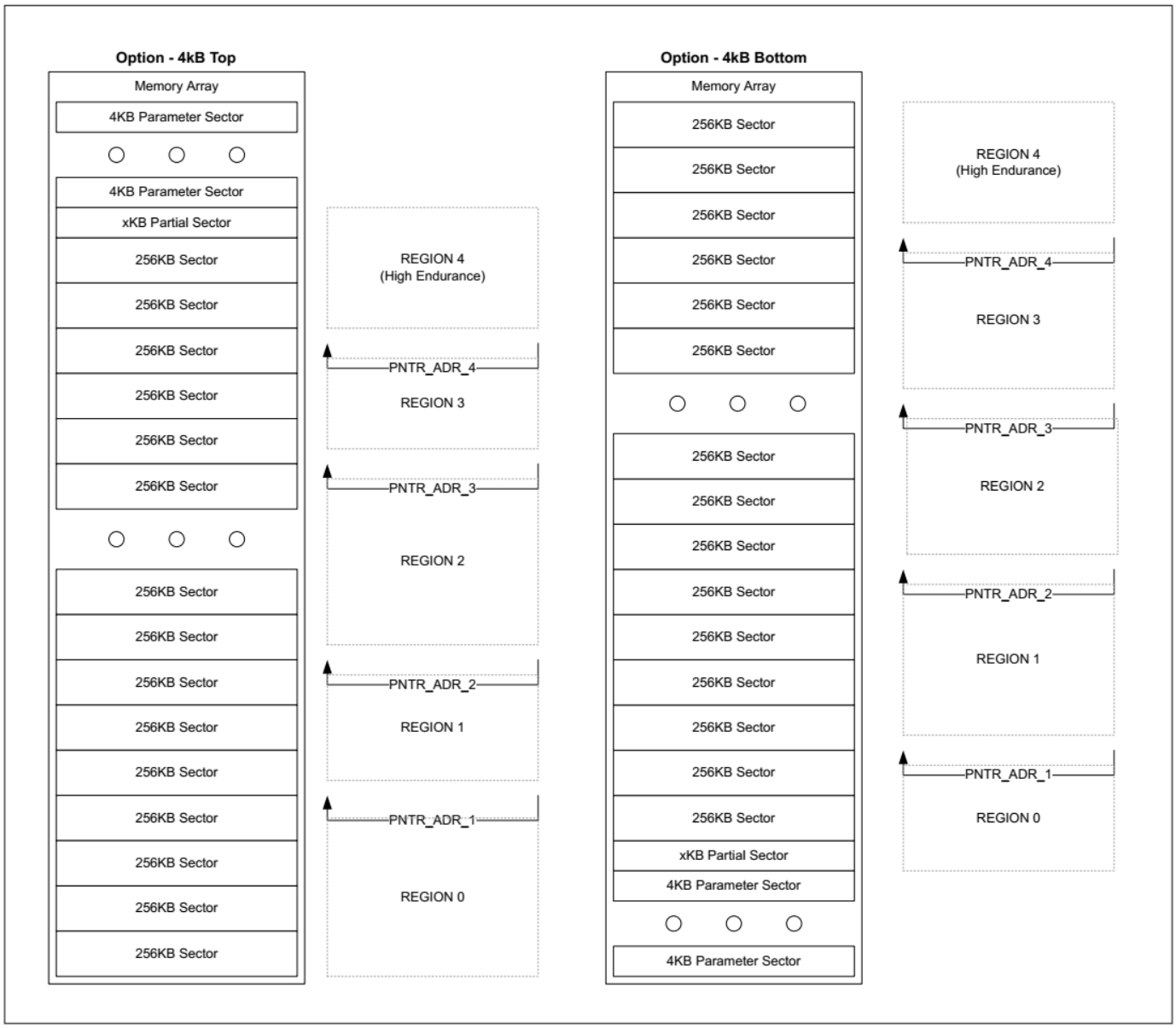

图 41 Infineon Endurance Flex 架构概述

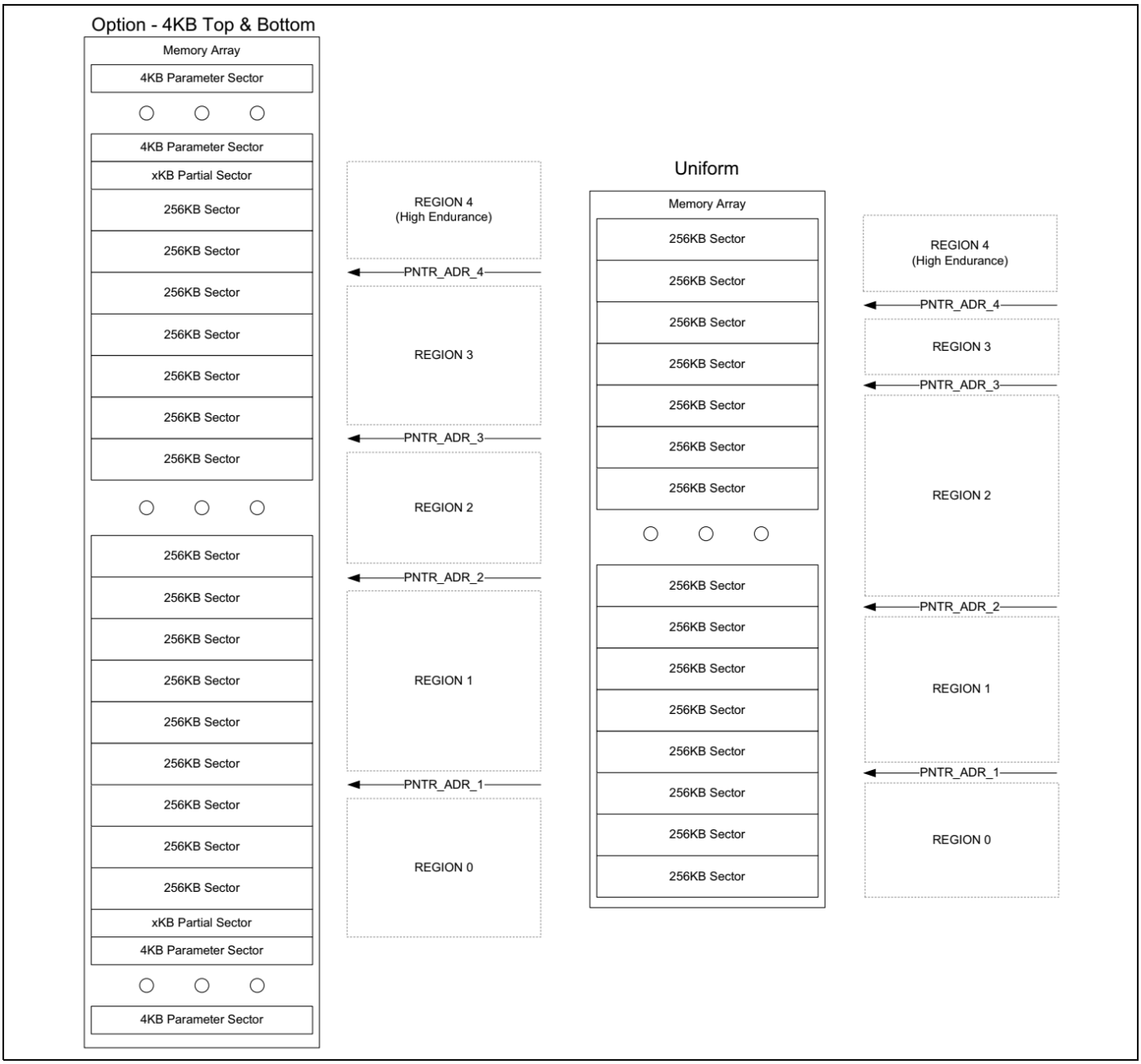

图 42 Infineon Endurance Flex 架构概述（续）

表 17 区域定义[1)], [2)], [3)], [4)]

Region	Lower limit	Upper limit
0	Sector 0	Address Pointer 1
1	Address Pointer 1	Address Pointer 2
2	Address Pointer 2	Address Pointer 3

表格续下页

表 17 （续）区域定义[1)] , [2)] , [3)] , [4)]

Region	Lower limit	Upper limit
3	Address Pointer 3	Address Pointer 4
4	Address Pointer 4	Highest Sector

1) 指针边界地址必须遵循以下规则：
- Pointer#4 address > Pointer#3 address
- Pointer#3 address > Pointer#2 address
- Pointer#2 address > Pointer#1 address

2) 4KB 扇区被排除在外。

3) 要求在客户首次为器件上电时配置高数据耐久性和长数据保留时间区域。一旦配置完成，就不能再更改。

4) 任何高耐久性区域的最少为 20 个扇区。

4.2.1 配置 1：最大耐久性 - 单一高耐久性区域

当所有 256 KB 扇区均指定为高耐久性时，可实现最大耐久性。必须使用 Infineon Endurance Flex 架构指针边界将所有扇区指定为高耐久性。最大耐久性指针边界配置如表 18所示。

表 18 英飞凌 Endurance Flex 架构指针边界值，用于最大耐久性配置[1]

Pointer #	Pointer address EPTADn[8:0]	Region type ERGNTn	Pointer enable# EPTEBn	Global region selection GBLSEL	Wear leveling enable WRLVEN
0	N/A	N/A	N/A	1’b1	1’b1
1	9’b111111111	1’b1	1’b1	N/A	N/A
2	9’b111111111				
3	9’b111111111				
4	9’b111111111				

1) 这也是该器件的默认配置。

4.2.2 配置 2：两个区域选择 - 一个长数据保留时间区域和一个高耐久性区域

必须使用 Infineon Endurance Flex 架构指针边界来划分长数据保留时间或高耐久性扇区。区域 0 定义为长数据保留，由 16 个扇区组成。区域 1 定义为高耐久性，有 240 个扇区。表 19显示了两个区域配置的指针边界设置。定义的指针数量基于配置的区域数量。

表 19　英飞凌 Endurance Flex 架构指针边界值（双区域配置）

Pointer #	Pointer address EPTADn[8:0]	Region type ERGNTn	Pointer enable# EPTEBn	Global region selection GBLSEL	Wear leveling enable WRLVEN
0	N/A	N/A	N/A	1’b0	1’b1
1	9’b000010000	1’b1	1'b0	N/A	N/A
2	9’b111111111	1’b1	1'b1		
3					
4					

4.2.3　英飞凌 Endurance Flex 架构相关寄存器和命令传输

表 20　英飞凌 Endurance Flex 架构相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Infineon Endurance Flex architecture Selection Registers (EFX4O, EFX3O, EFX2O, EFX1O, EFX0O) (see Infineon endurance flex architecture selection register (EFXx))	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)

4.3　数据完整性 CRC（循环冗余校验）

HL-T/HS-T家族设备具有一组命令，用于在内存阵列中用户定义的地址范围上执行硬件加速的循环冗余校验（CRC）计算。 CRC计算是另一种类似于写入或擦除的嵌入式操作，其在计算进行时器件处于繁忙状态。 循环冗余校验（CRC）操作使用以下 CRC32 校验公式来确定 CRC 校验值。

CRC32 多项式: $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^{9} + X^{8} + X^{6} + 1$

通过输入DICHK_4_1命令传输来启动校验值生成序列。该命令包括将起始地址加载到 CRC（循环冗余校验）开始地址寄存器中，该寄存器标识将由 CRC（循环冗余校验）计算覆盖的地址范围的开始。 该命令还包括将结束地址加载到 CRC（循环冗余校验）结束地址寄存器中。将 CS# 拉高会启动 CRC（循环冗余校验）计算。CRC（循环校验）过程计算起始地址到结束地址中包含的数据的校验值。

在计算期间，器件进入忙碌状态 (STR1V[0] - RDYBSY = 1)。校验值计算完成后，器件将返回到空闲状态 (STR1V[0] - RDYBSY = 0)，并且可以读取计算出的校验值。 校验值存储在数据完整性 CRC 寄存器 (DCRV[31:0]) 中，并且可以使用 Read Any Register (RDARG_C_0) 命令来读取。

仅当器件处于空闲状态时，才能启动校验值计算；并且一旦启动，就可以用 CRC 暂停命令

（SPEPD_0_0）从存储器阵列读取数据。在暂停状态期间，状态寄存器 2 中的 CRC 暂停状态位将会置位 (STR2V[4] - DICRCS = 1)。一旦暂停挂起，主控可以读取状态寄存器，从队列中读取数据，并可以通过CRC 恢复命令（RSEPD_0_0）恢复CRC（循环冗余校验）计算。
结束地址 (ENDADD) 必须至少比起始地址 (STRADD) 高 4 个地址。如果 ENDADD < STRADD + 3，则检查值计算将中止/退出，器件将返回到就绪状态(STR1V[0] - RDYBSY = 0). 数据完整性 CRC（循环冗余校验） 中止/退出状态位将会置位 (STR2V[3] - DICRCA = 1) 来指示中止条件。一旦置位，DICRCA 位可以通过软件复位或有效的后续 CRC（循环冗余校验）指令执行来清除。如果 ENDADD < STRADD + 3，则校验值将保留不确定的数据。

注释：*CRC（循环冗余校验）校验值计算期间的任何无效命令传输都可能损坏校验值数据。*

4.3.1 数据完整性检查相关寄存器和命令传输

表 21 数据完整性 CRC（循环冗余校验）相关寄存器和命令传输

Related registers	**Related SPI transactions (see Table 79)**	**Related quad SPI transactions (see Table 83)**
Status Register 1 (STR1N, STR1V) (see Table 47)	Data Integrity Check (DICHK_4_1)	Data Integrity Check (DICHK_4_1)
Status Register 2 (STR2V) (see Table 50)	Suspend Erase/Program/Data Integrity Check (SPEPD_0_0)	Suspend Erase/Program/Data Integrity Check (SPEPD_0_0)
Data Integrity CRC Check-Value Register (DCRV) (see Table 60)	Resume Erase/Program/Data Integrity Check (RSEPD_0_0)	Resume Erase/Program/Data Integrity Check (RSEPD_0_0)

4.4 数据保护机制

数据保护用于防止对存储的数据和器件配置进行意外更改。这包括无意擦除或写入存储阵列以及写入配置寄存器，这些都可能改变器件的功能。 本文将会介绍三种类型的保护机制，包括保护单个或一组扇区、保护部分或整个内存阵列。
图 43 显示不同保护机制以及适用数据区域的概述。

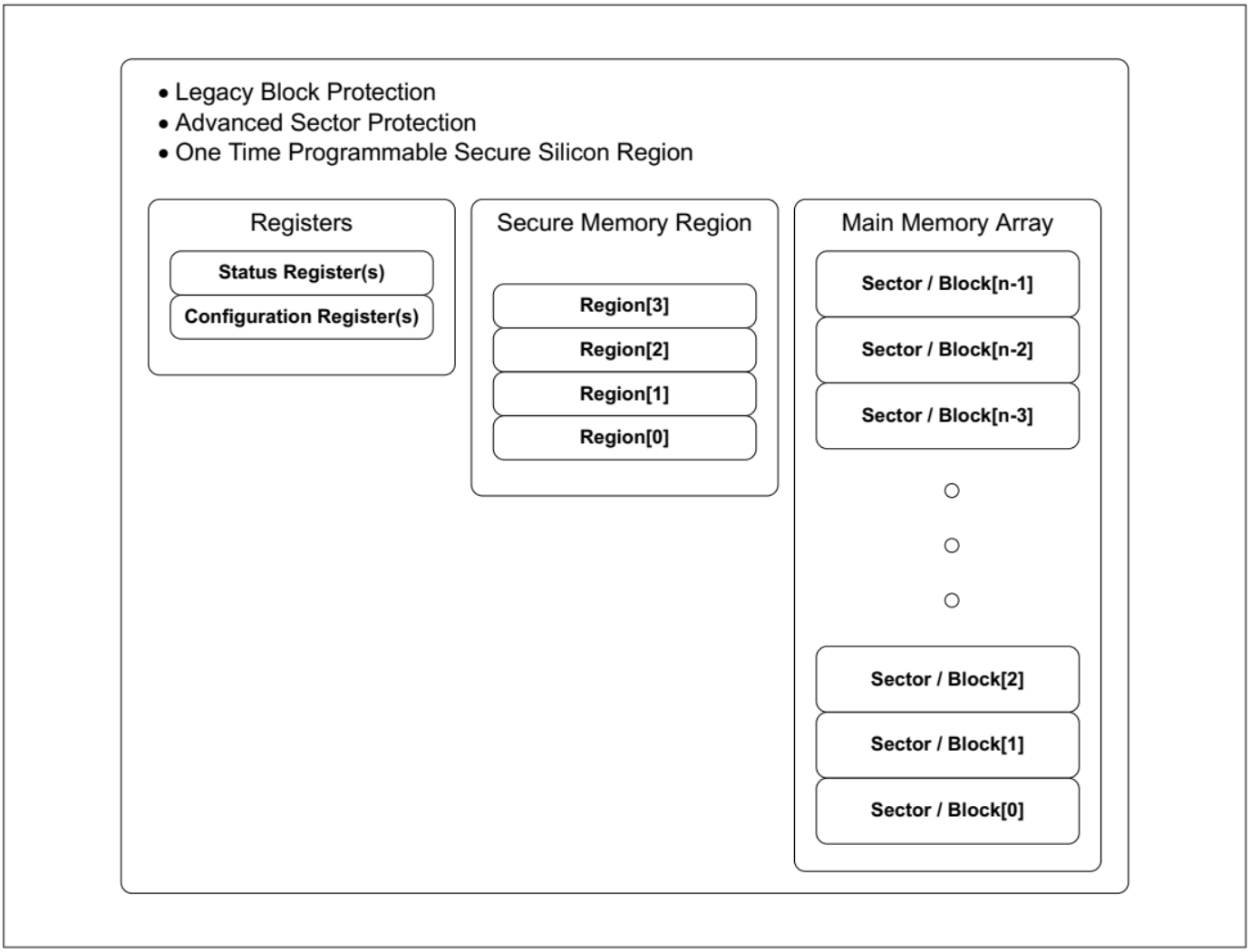

图 43　　数据保护和安全（写入/编程/擦除）机制

4.4.1　传统块保护 (LBP)

传统块保护（LBP）是基于功能块的数据保护机制。 LBP 支持与传统串行 NOR 闪存设备的兼容性。LBP 通过保护状态寄存器和配置寄存器为存储器阵列和器件配置中的数据提供保护。

4.4.1.1　存储阵列保护

存储器阵列的保护是通过功能块大小选择来实现的，这是通过状态寄存器 1 (STR1N[4:2]/STR1V[4:2] - LBPROT[2:0]) 和配置寄存器 1 (CFR1N[5]/CFR1V[5] - TBPROT) 中存在的位的组合来实现的。

表 22 提供LBP存储阵列功能块选择汇总。

表 22　　传统块存储阵列保护选择

CFR1N[5] / CFR1V[5]TBPROT	STR1N[4]/ STR1V[4]LBPROT[2]	STR1N[3]/ STR1V[3]LBPROT[1]	STR1N[2]/ STR1V[2]LBPROT[0]	Memory array block size	512Mb (KBs)	1Gb (KBs)
0	0	0	0	None	0	0
0	0	0	1	Upper 64th	1024	2048
0	0	1	0	Upper 32nd	2048	4096
0	0	1	1	Upper 16th	4096	8192
0	1	0	0	Upper 8th	8192	16384
0	1	0	1	Upper 4th	16384	32768
0	1	1	0	Upper Half	32768	65536
0	1	1	1	All sectors	65536	131072
1	0	0	0	None	0	0
1	0	0	1	Lower 64th	1024	2048
1	0	1	0	Lower 32nd	2048	4096
1	0	1	1	Lower 16th	4096	8192
1	1	0	0	Lower 8th	8192	16384
1	1	0	1	Lower 4th	16384	32768
1	1	1	0	Lower Half	32768	65536
1	1	1	1	All sectors	65536	131072

4.4.1.2　配置保护

LBP 在配置寄存器 1 （CFR1N[4,0]/CFR1V[4,0] - PLPROT、TLPROT）中具有选择位，可以永久或暂时保护状态和配置寄存器，从而再次保护器件的配置。 临时保护在下一个掉电或硬件复位或JEDEC串行闪存式器件复位信号协议之前保持有效。

表 23　　选项 2 - 传统块配置保护选择[1]

CFR1N[4]/ CFR1V[4]PLPROT	CFR1N[0]/ CFR1V[0]TLPROT	Register protection status
0	0	Status and Configuration registers are unprotected
1	X	Status and Configuration registers are permanently protected (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS)
0	1	Status and Configuration registers are Protected till next Power down (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS)

1) 保护配置也会保护已被选择保护的存储阵列块。

4.4.1.3 写入保护信号

写保护 (DQ2_WP#) 信号输入与状态寄存器的去使能位 (STR1x[7]) 相结合，以提供硬件输入信号控制保护。当 WP# 为低电平且 STR1x[7] 置位为“1”时，状态寄存器 1（STR1N 和 STR1V）和配置寄存器 1（CFR1N 和 CFR1V）受到保护而不被更改。 这可以防止禁用或更改功能块保护位定义的保护。

4.4.1.4 传统块保护流程图

LBP保护机制流程图如**图 44**。

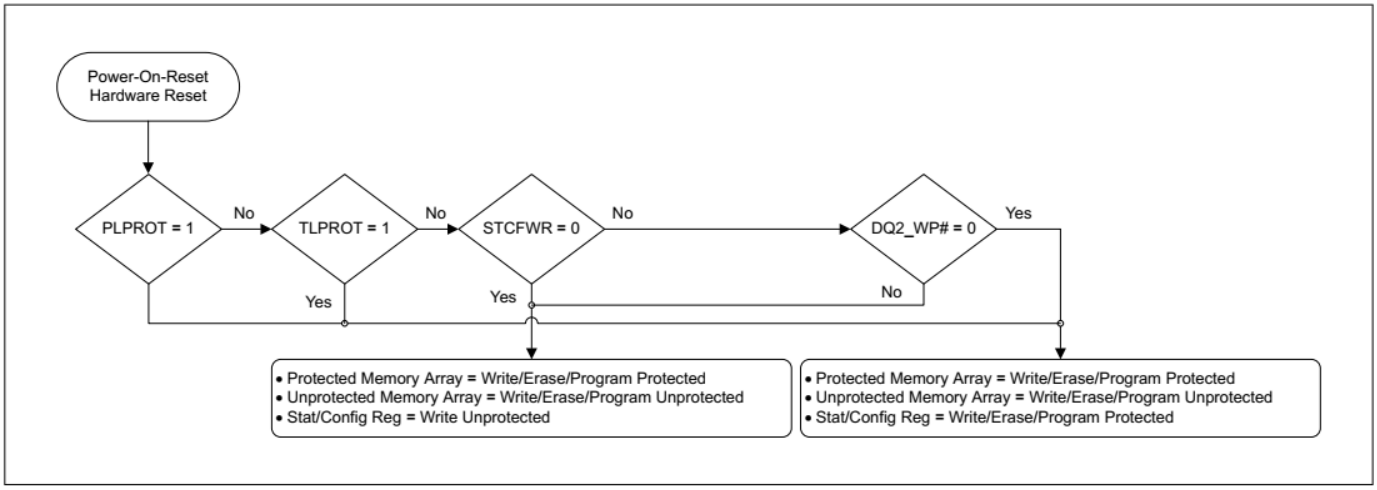

图44 传统块保护流程图

4.4.1.5 LBP 相关寄存器和命令传输

表 24 LBP相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Status Register 1 (STR1N, STR1V) (see Table 47)	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
Configuration Register 1 (CFR1N, CFR1V) (see Table 51)	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)
	Read Status Register 1 (RDSR1_0_0)	Read Status Register 1 (RDSR1_0_0)
	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)

4.4.2 高级扇区保护（ASP）

高级扇区保护 (ASP) 机制允许每个存储器阵列扇区通过易失性或非易失性锁定功能进行独立控制，以防止擦除或写入。非易失性锁定配置也可以被锁定，也可以受密码保护。

主存储器阵列扇区通过易失性（DYB）和非易失性（PPB）保护位对进行保护和编程。每个DYB /PPB 位对可以单独设置为“0”，保护相关扇区，或清除为“1”，不保护相关扇区。 DYB保护位可以根据需要经常置位和清除，而 PPB 位则不易丢失，必须遵守各自基于技术的耐久性要求。图 45 显示 ASP 的概述。

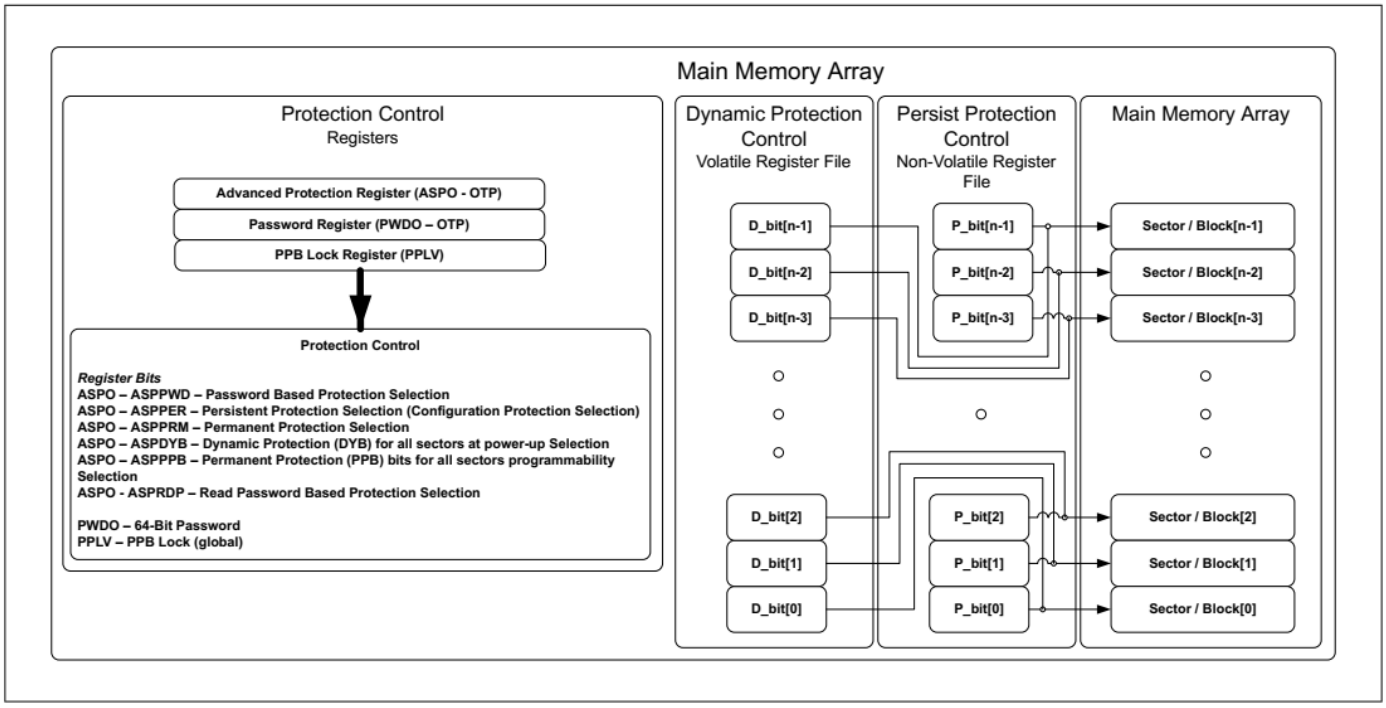

图 45　　高级扇区保护（非易失）

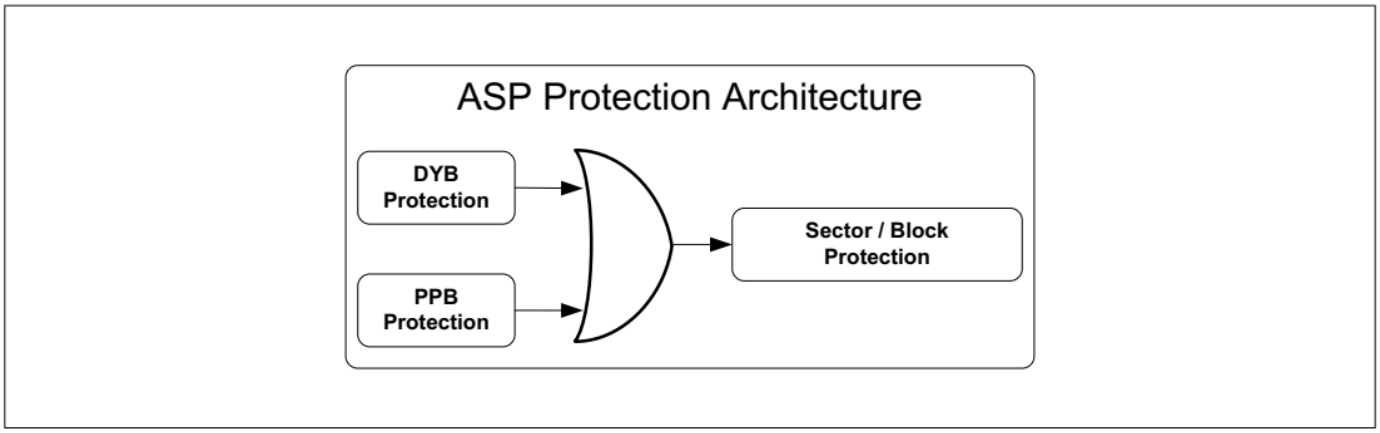

图 46　　DYB 和 PPB 保护控制

ASP 提供了丰富的配置选项，可根据设计或系统需求生成多种数据保护机制。这些配置选项在“配置保护”通过“ASP 相关寄存器和命令传输”进行描述。

4.4.2.1　配置保护

ASP 提供了通过持久保护机制来保护器件配置的措施。 选择高级扇区保护寄存器 (ASPO[1] - ASPPER) 中的位 1 可选择持久保护机制并保护以下寄存器或寄存器位不被写入或编程：

- CFR1V[6, 5, 4, 2]/CFR1N[6, 5, 4, 2] - SP4KBS, TBPROT, PLPROT, TB4KBS
- CFR3N[3]/CFR3V[3] - UNHYSA
- ASPO[15:0]
- PWDO[63:0]

持久保护机制流程图如图 47 所示。

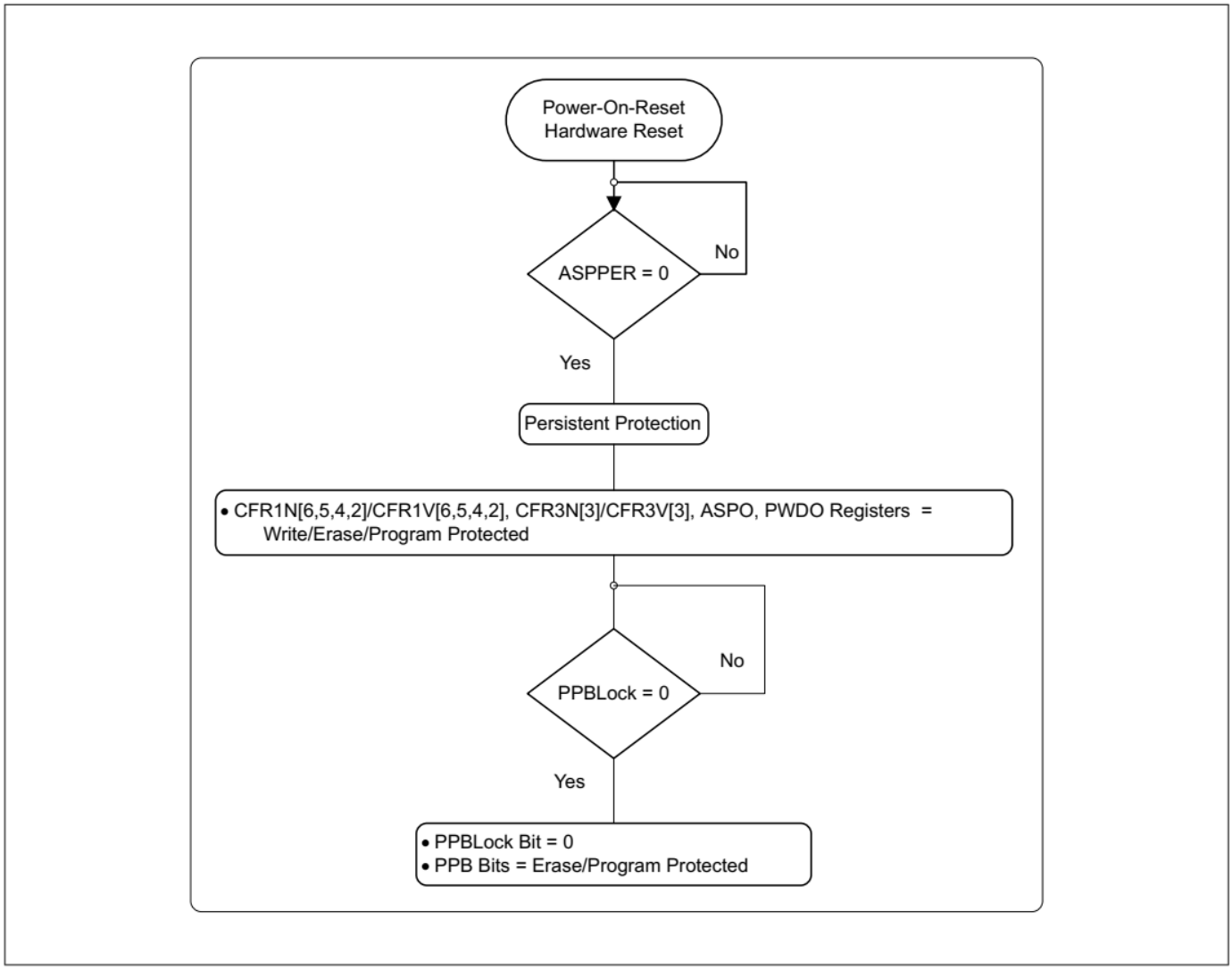

图47　　持久保护机制流程图

4.4.2.2　动态 DYB（易失性）扇区保护

动态保护比特(DYB)是易失性位，并且每个扇区只有一个唯一的DYB，可以按照扇区为单位单独进行修改。DYB只控制那些已清除PPB的扇区的保护。通过发出DYB写入命令传输， DYB被置位为“0”或清除为“1”，从而分别将每个扇区置于受保护或不受保护的状态。 使用该功能，可以轻易保护扇区，避免意外改变相应扇区。另外需要更改时也可以轻易取消对其保护。DYB可以在需要时随时设为0或清除为1。

在动态扇区保护机制中，提供了一个选项，可以在上电（受保护）时将所有DYB易失性保护位重置为“0”，从本质上保护所有扇区免受擦除或写入的影响。在高级扇区保护寄存器 (ASPO[4] - ASPDYB) 中选择位 4 将为所有扇区在 Power-up 时选择动态保护 (DYB)机制。如果需要，这些DYB位可以单独设置为“1”。上电动态扇区保护机制流程图如图 48所示。

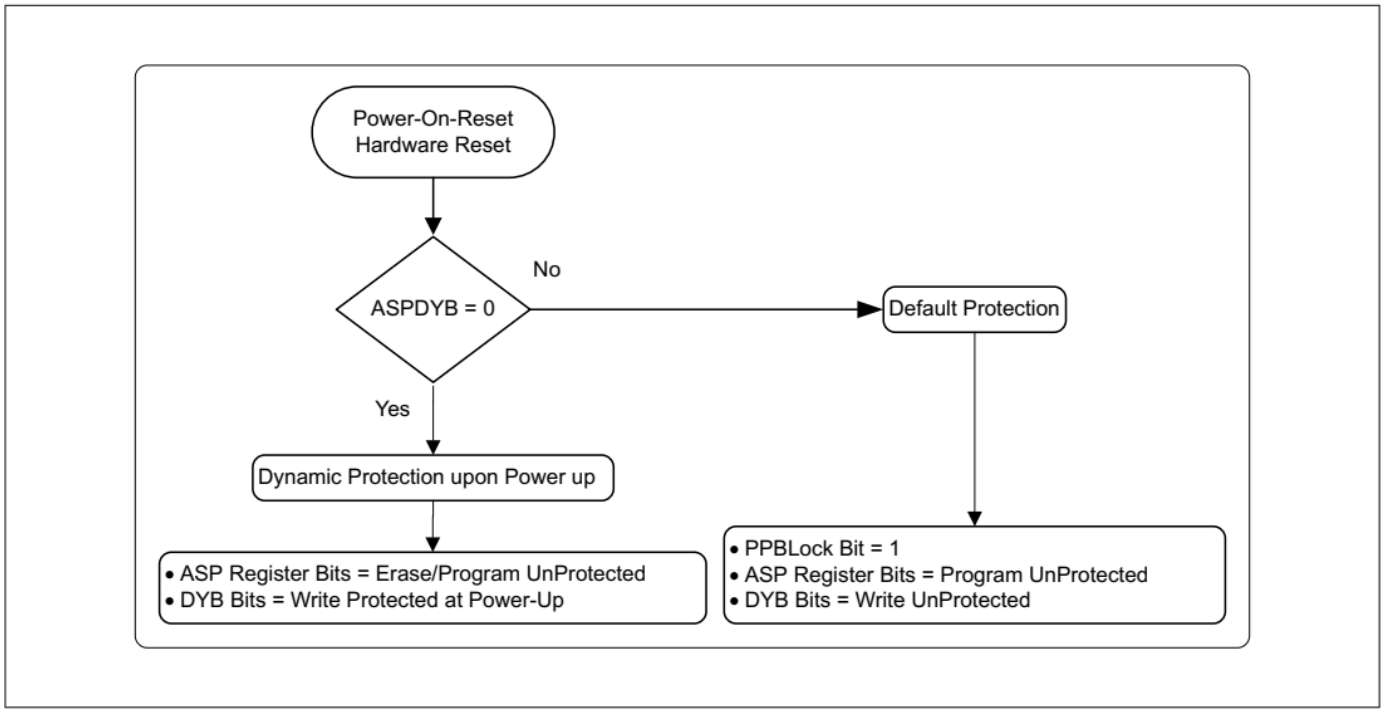

图48　　动态扇区保护机制流程图

4.4.2.3　永久/临时 PPB（非易失性）扇区保护

每个非易失性位（PPB）为单个存储器扇区提供非易失性保护，该存储器扇区保持锁定状态（启用保护），直到其对应的位被清除为“1”。 有两个选项可以控制 ASP 中基于 PPB 的非易失性选择，即永久和临时。

4.4.2.4　永久性 PPB 保护机制

PPB位于一个单独的非易失性闪存阵列中。为每个扇区分配一个PPB位。当一个PPB位被写入为0时，相应的扇区受到保护，不能对它执行写入和擦除操作。PPB位可单独写入，但必须按组进行擦除。这与各个字可以在主阵列中单独写入，但整个扇区必须同时擦除的方式类似。编程一个PPB位需要典型的字编程时间。在 PPB 位写入操作或 PPB 位擦除期间，可以访问状态寄存器来确定操作是否完成。擦除所有PPB需要典型的扇区擦除时间。

永久性 PPB 保护机制，顾名思义，是永久性的并且永远不会改变。一旦决定了 PPB 保护架构，选择高级扇区保护寄存器（ASPO[0]）中的位 0 即可为所有 PPB 位启用永久保护，从而禁用所有 PPB 擦除和写入操作。ASPO 也受到保护以避免被写入或编程。

永久PPB保护机制流程图如图 49 所示。

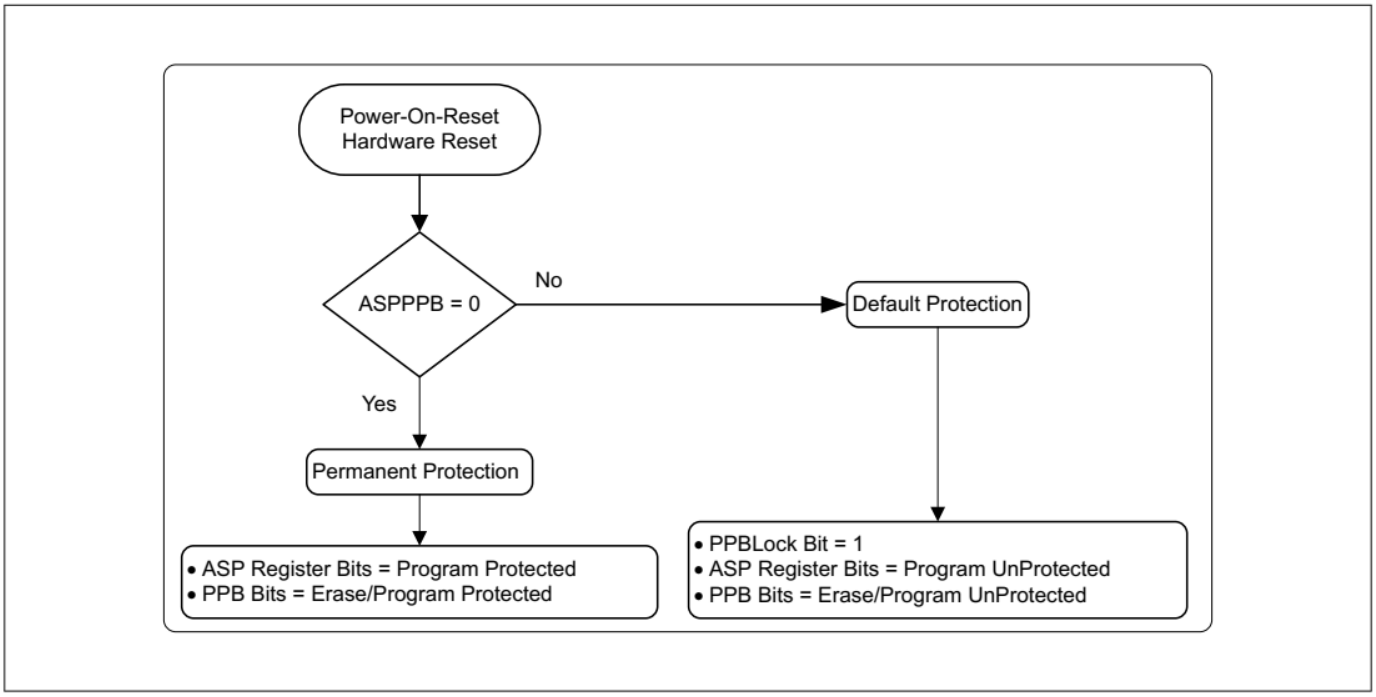

图 49　　永久 PPB 扇区保护流程图

4.4.2.5　临时 PPB 保护机制

基于 PPB 的非易失性保护架构可以被暂时锁定，从而禁止擦除和写入各个 PPB 位。持久保护位锁(PPBLock)是一个易失性位，用于保护所有PPB位。当清除为0时，它锁定所有PPB；设成1时，允许更改PPB。每个器件只有一个PPB锁定位。PPBLock 命令传输（WRPLB_0_0）用于清零，将位复位为“0”。只有当所有PPB位均配置为所需的设置后，才将PPB锁定位清零。PPB 锁定位在POR或硬件复位期间置位为“1”。 当使用 PPBLock 命令传输清除时，没有软件指令序列可以设置 PPBLock，只有额外的硬件复位或上电可以设置 PPBLock。

注释：　*临时PPB 保护不需要任何ASP 配置。*

4.4.2.6　密码保护机制

密码保护机制要求使用 64 位密码来设置 PPBLock，从而实现更高级别的安全性。 除了密码要求外，在上电和复位后，PPB锁定还将清除为0以确保在上电时提供保护。通过输入整个密码并成功执行密码解锁指令后，PPB锁定将设为1，从而允许修改扇区PPB。选择高级扇区保护寄存器 (ASPO[2] - ASPPWD) 中的位 2 可选择密码保护机制。密码保护机制还可以保护 ASPO 免遭写入或编程。

注释：　*在选择密码保护机制之前，必须先对密码进行编程。密码解锁SPI命令传输(PWDUL_0_1) 用于提供用于提供密码以进行比对。*

密码保护机制流程图如图 50 所示。

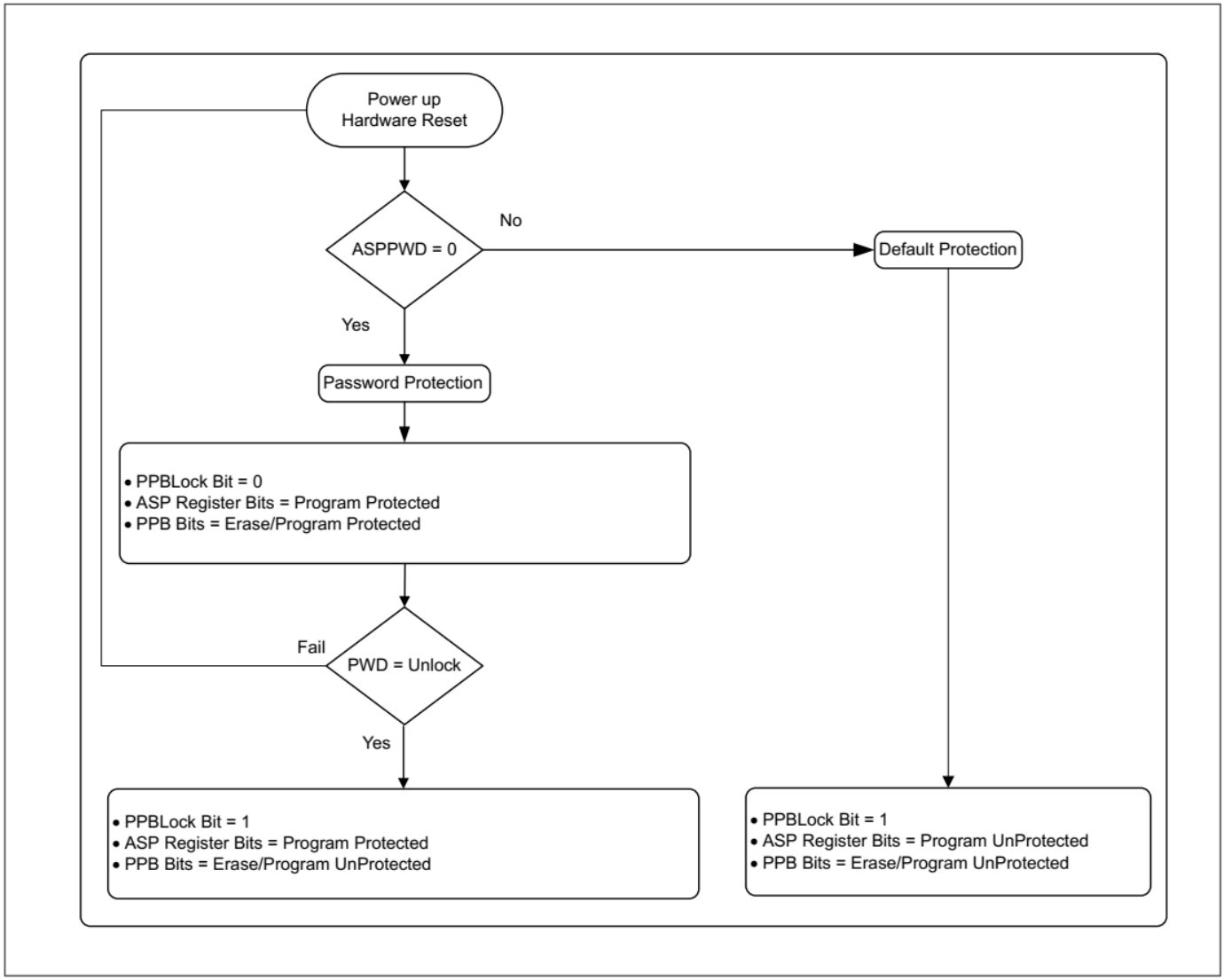

图50　　密码保护机制流程图

4.4.2.7　读取密码保护机制

读取密码保护机制可以用来取代密码保护机制，并提供最强大的数据保护。读取密码保护机制可以保护存储阵列免遭读取、写入和擦除。在密码解锁命令传输成功完成之前，只有配置寄存器 1 (CFR1x[5] - TBPROT) 的第 5 位选择的最低或最高 (256 KB) 扇区地址范围保持可读。无论读取命令传输中提供的扇区地址是什么，“0”都表示从最顶部的扇区选择，“1”则表示从最底部的扇区选择。注意，从阵列的读保护部分读取的数据将别名回到可读区域。

在提供密码之前，处于密码读取模式期间允许清除写入和擦除错误标志命令、所有存储器读取命令、密码解锁命令、读取制造商和器件 ID 命令、读取 SFDP 命令、读取状态寄存器-1 命令、读取状态寄存器-2 命令、读取ECC状态命令、清零，读取ECC状态寄存器命令和进入 DPD 模式命令。

注释：　　*在选择读取密码保护机制之前，必须先对密码进行烧录。密码解锁SPI命令(PWDUL_0_1)用于提供用于比较的密码。*

读密码保护机制流程图如图 51 所示。

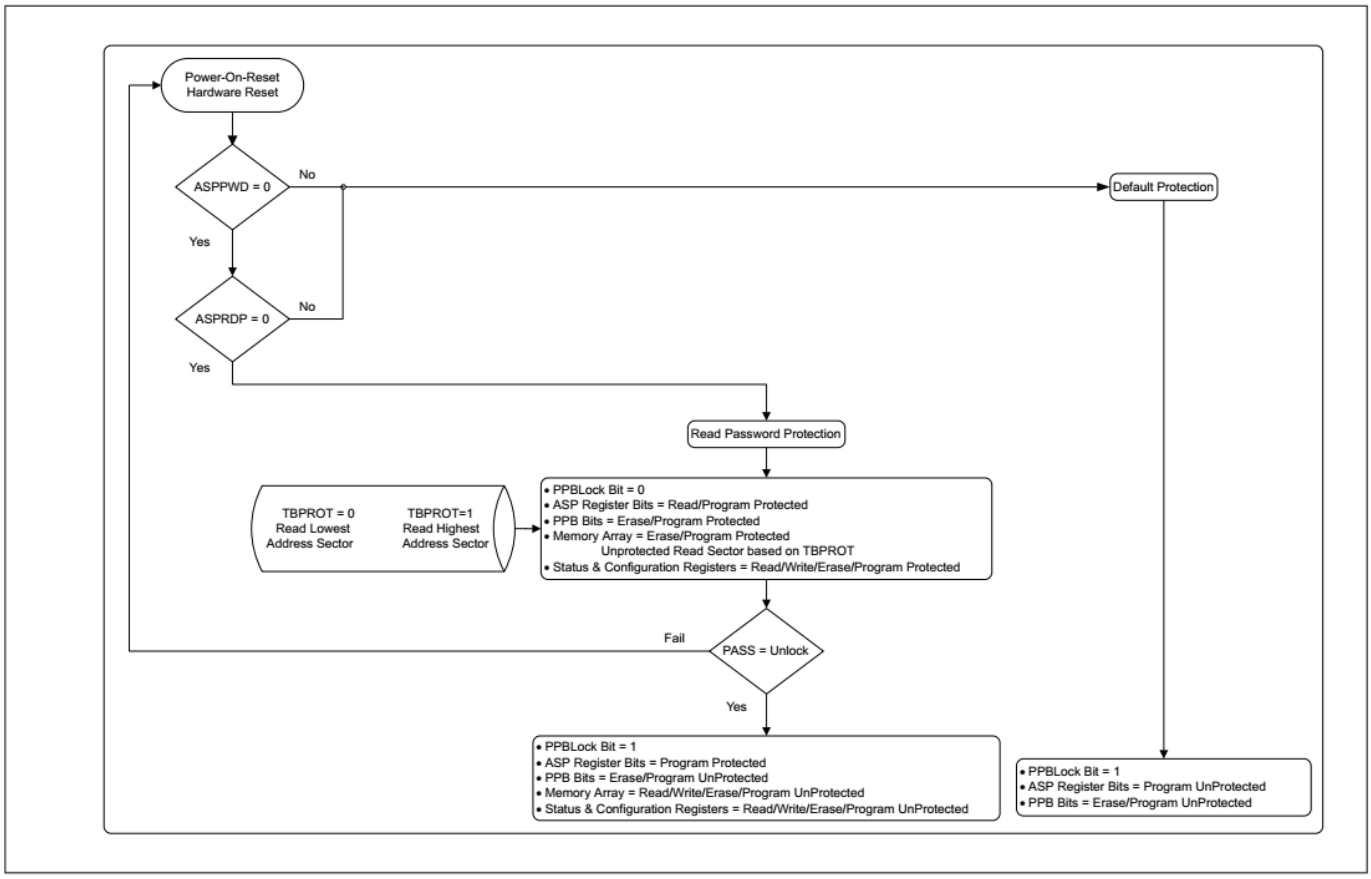

图 51　　读取密码保护机制流程图

4.4.2.8　PPB 位 - OTP 选择

ASP 提供了一个配置选项来永久禁止 PPB 擦除命令传输(ERPPB_0_0)。这使得所有 PPB 位都为 OTP。使用此选项，一旦选择了 PPB 保护，将永远无法更改。
选择高级扇区保护寄存器 (ASPO[3] - ASPPPB) 中的位 3 使得 PPB 位变成 OTP属性。

4.4.2.9　通用ASP使用准则

- 持久保护 (ASPPER) 和密码保护 (ASPPWD) 是互斥的 - 只能写入一个选项。
- 如果需要读取密码保护（ASPRDP），必须与密码保护（ASPPWD）同时进行编程。
- 一旦密码被烧录并验证，密码保护机制（ASPPWD）必须被写入（为 0）以防止读取密码。
- 当读取密码机制和密码保护机制启用时（即 如果将 ASPO[5] - ASPRDP, ASPO[2] - ASPPWD 写入为 0，则所有地址都会重定向到引导扇区，直到使用对的密码正确输入至密码解锁序列。此时，读取密码模式被禁用并且所有寻址都将选择至正确的位置。
- 当读密码保护模式激活时，不允许对存储空间进行写入或写入寄存器。

4.4.2.10 ASP 相关寄存器和命令传输

表 25 ASP 相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Advanced Sector Protection Register (ASPO) (see Note)	Read Dynamic Protection Bit (RDDYB_4_0, RDDYB_C_0)	Read Dynamic Protection Bit (RDDYB_4_0, RDDYB_C_0)
Configuration Register 1 (CFR1N, CFR1V) (see Table 51)	Write Dynamic Protection Bit (WRDYB_4_1, WRDYB_C_1)	Write Dynamic Protection Bit (WRDYB_4_1, WRDYB_C_1)
	Read Persistent Protection Bit (RDPPB_4_0, RDPPB_C_0)	Read Persistent Protection Bit (RDPPB_4_0, RDPPB_C_0)
	Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0)	Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0)
	Erase Persistent Protection Bit (ERPPB_0_0)	Erase Persistent Protection Bit (ERPPB_0_0)
	Write PPB Protection Lock Bit (WRPLB_0_0)	Write PPB Protection Lock Bit (WRPLB_0_0)
	Read Password Protection Mode Lock Bit (RDPLB_0_0)	Read Password Protection Mode Lock Bit (RDPLB_4_0)
	Password Unlock (PWDUL_0_1)	Password Unlock (PWDUL_4_1)
	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)
	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)

4.4.3 安全存储区域（SSR）

安全存储区域（SSR）是一个 1024 字节的内存区域（与主内存阵列分开）。 1024 字节分为 32 个可单独锁定的 32 字节区域。图 52 提供了SSR的概述。

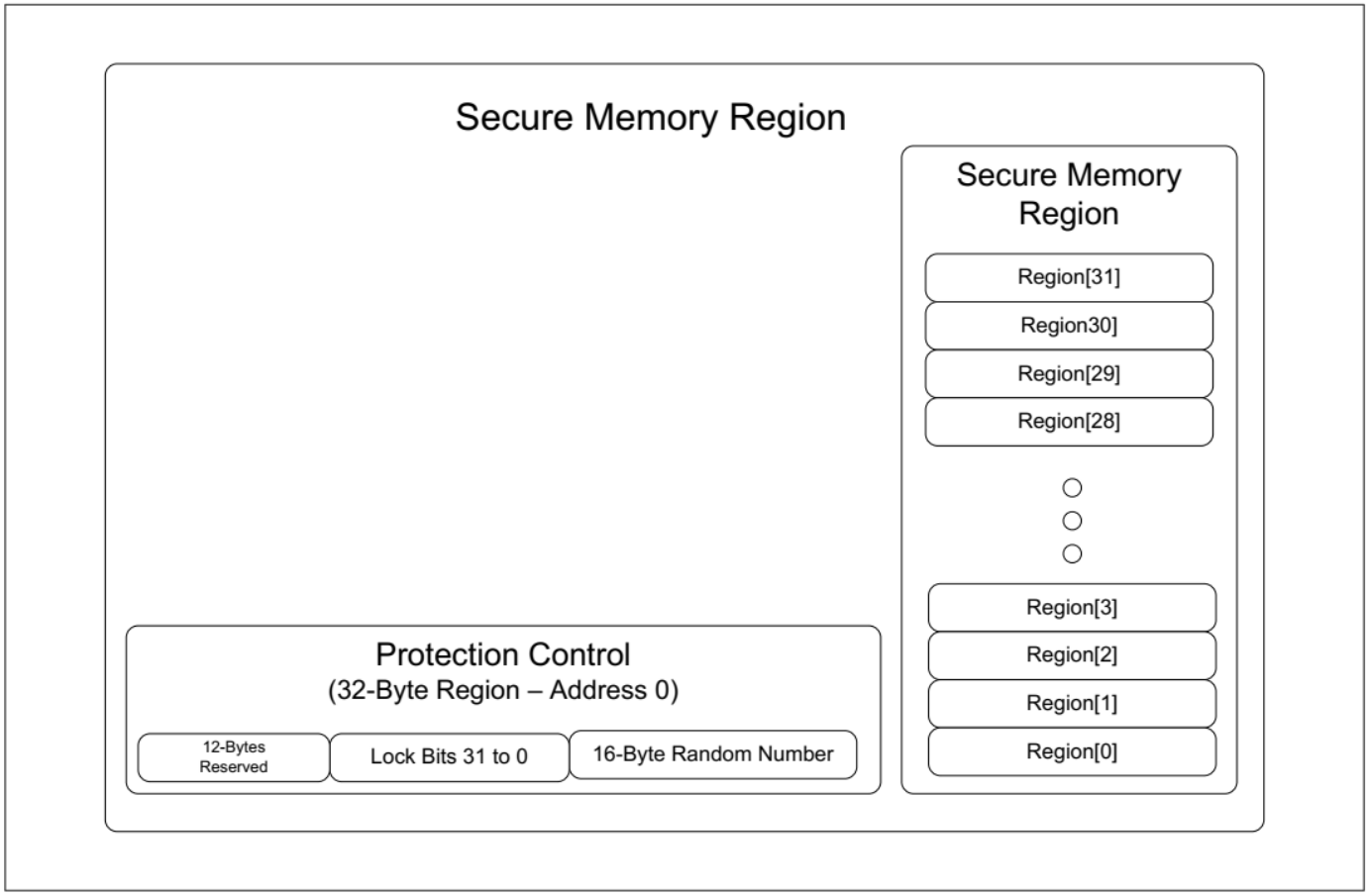

图 52　　OTP 保护（非易失性）

第一个 32 字节区域（从地址 0 开始）为其他 32 字节区域提供保护机制。该区域的最低十六个字节包含一个 128 位随机数。随机数不可写入、擦除或编程。接下来的四个字节（总共 32 位）如果置位为“0”可以为剩余的若干个32 字节区域提供写入保护 - 每 32 字节区域对应一个位。所有其他字节均被保留。

注释： *尝试对128 位随机数进行擦除和写入将分别导致ERSERR 或PRGERR。需要硬件复位才能使器件返回待机模式。*

4.4.3.1　　SSR 相关寄存器和命令传输

表 26　　SSR 相关寄存器和命令传输

Related registers	**Related SPI transactions (see Table 79)**	**Related quad SPI transactions (see Table 83)**
N/A	Program Secure Silicon Region (PRSSR_C_1)	Program Secure Silicon Region (PRSSR_C_1)
	Read Secure Silicon Region (RDSSR_C_0)	Read Secure Silicon Region (RDSSR_C_0)

4.5 安全启动

SEMPER™闪存存储器包含一个嵌入式微处理器，用于初始化器件、管理嵌入式操作以及执行其他高级功能。该嵌入式设备的初始化失败或非易失性配置寄存器的配置损坏可能会导致闪存式存储器器件无法使用。除非发生灾难性事件，例如嵌入式硬件的永久损坏，一般情况下器件是可以恢复的。

SafeBoot 特性允许状态寄存器轮询通过错误编码的方式来检测嵌入式初始化故障或配置寄存器损坏。

4.5.1 微控制器初始化失败检测

如果嵌入在闪存式存储器器件中的微控制器初始化失败，硬件复位一般可以恢复该器件，除非是灾难性故障。 该硬件复位必须由主控控制器发起。 一旦检测到微控制器初始化失败，闪存存储器会自动恢复到其默认启动引导模式 (1S-1S-1S)，并在其状态寄存器中提供故障签名。

表 27 显示检测到初始化失败时器件的状态寄存器位。

表 27 状态寄存器 1 上电检测签名

Bit	Field name	Function	Detection signature
STR1V[7]	STCFWR	Status Register and Configuration Registers Protection Selection against write (erase/program)	0
STR1V[6]	PRGERR	Programming Error Status Flag	1
STR1V[5]	ERSERR	Erasing Error Status Flag	1
STR1V[4]	LBPROT[2:0]	Legacy Block Protection based memory Array size selection ***Note**: LBPROT[2:0] can be anything from 000 to 111 based on Block Protection configuration.*	0
STR1V[3]			0
STR1V[2]			0
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	0
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	1

表 28 检测到上电失败时的接口配置[1]

Interface	Transactions supported	Register type	Address (# of bytes)	Frequency of operation	Register read latency (# of clock cycles)	Output impedance
SPI (1S-1S-1S)	Read Status Register 1 (RDSR1_0_0)Read Any Register (RDARG_C_0)	Status Register (Volatile Only)	4	Maximum (allowed for RDSR1_0_0, RDARG_C_0)	2	45 Ω

*1)*为了读取状态寄存器，将非易失性状态寄存器地址提供给 RDARG_C_0 将产生不确定的结果。

4.5.1.1 主控轮询行为

主控将需要通过状态重置轮询序列来确定器件中是否发生初始化故障。该序列的流程图如图 53 所示。

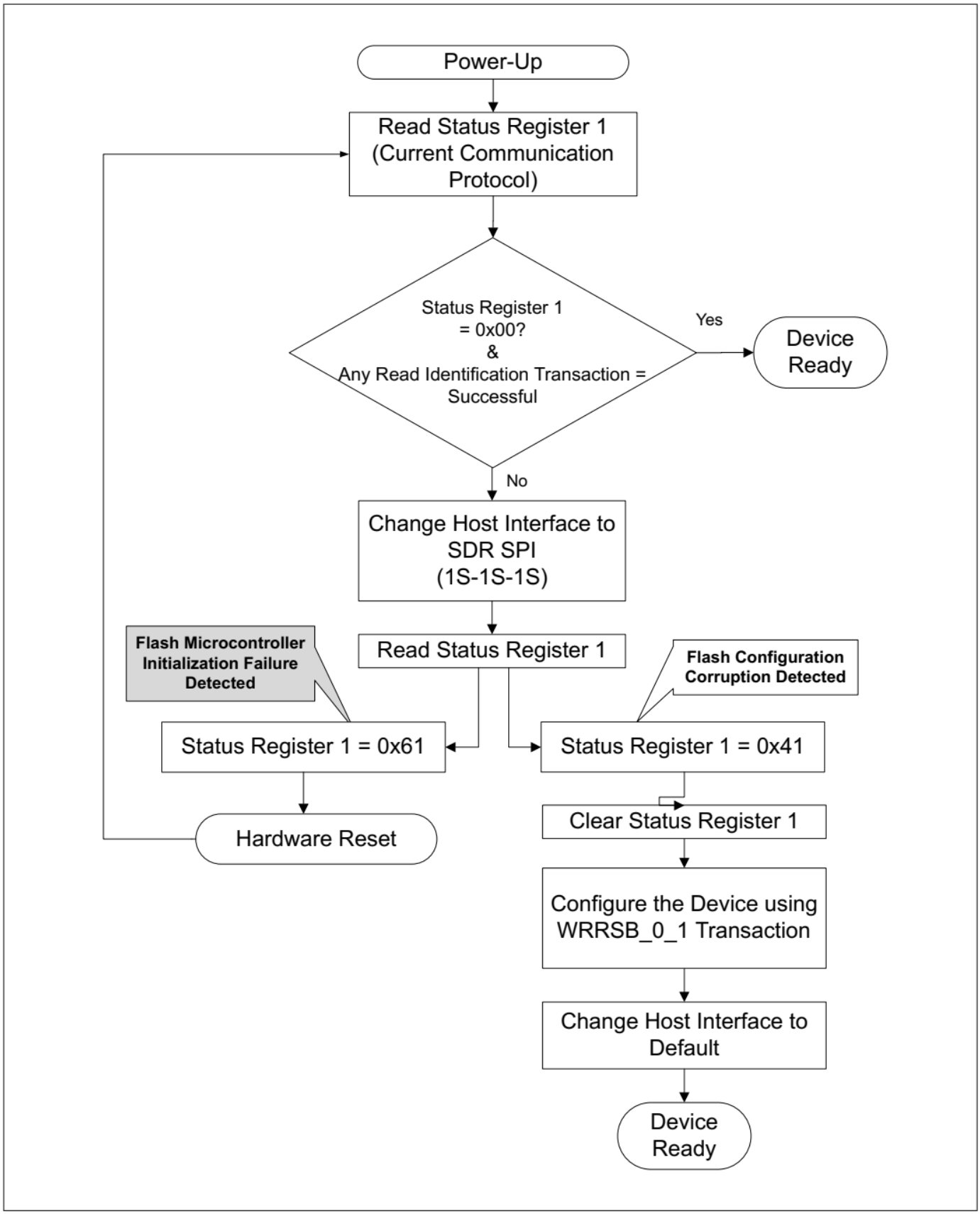

图 53　　用于微控制器初始化故障检测的主控轮询序列

注释： *轮询序列必须仅从较高的I/O 接口配置开始到较低的I/O 接口配置。例如，4S-4D-4D 到1S-1S-1S。*

4.5.1.2 微控制器初始化初始化失败检测相关寄存器和命令序列

表 29 微控制器初始化失败相关寄存器和命令序列

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Status Register 1 Volatile (STR1V) (see Table 47)	Read Any Register (RDARG_C_0)	N/A
	Read Status Register-1 (RDSR1_0_0)	

4.5.2 配置损坏检测

如果在器件的配置更新期间（例如写入非易失性寄存器时），发生掉电或硬件复位，则写入寄存器命令序列将被中断。 器件将返回到待机模式，但由于嵌入式写入操作过早终止，非易失性寄存器数据很可能已被损坏。 在下次上电时，将检测到配置损坏，并且器件将恢复为其默认的启动引导模式（1S-1S-1S）并允许再次重写配置。器件将维持配置的保护机制。

表 30 展示检测到配置损坏时器件的状态寄存器位。

表 30 状态寄存器 1 配置损坏检测签名

Bit	Field name	Function	Detection signature
STR1V[7]	STCFWR	Status Register and Configuration Registers Protection Selection against write (erase/program)	0
STR1V[6]	PRGERR	Programming Error Status Flag	1
STR1V[5]	ERSERR	Erasing Error Status Flag	0
STR1V[4]	LBPROT[2:0]	Legacy Block Protection based memory Array size selection	0
STR1V[3]		***Note**: LBPROT[2:0] can be anything from 000 to 111 based on Block Protection configuration.*	0
STR1V[2]			0
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	0
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	1

表 31 检测到配置损坏时的接口配置

Interface	Transactions supported	Address (# of bytes)	Frequency of operation	Register read latency (# of clock cycles)	Output impedance
SPI (1S-1S-1S)	All SPI (1S-1S-1S) transactions	4	Maximum	2	45 Ω

注释： *如果电路供电电压V_{cc}在规格范围内，并且硬件复位不能解决问题，请更换闪存式存储器器件。*

4.5.2.1 主控轮询行为

主控将需要通过状态寄存器轮询序列来确定器件中是否发生配置损坏。该序列的流程图如图 54 所示

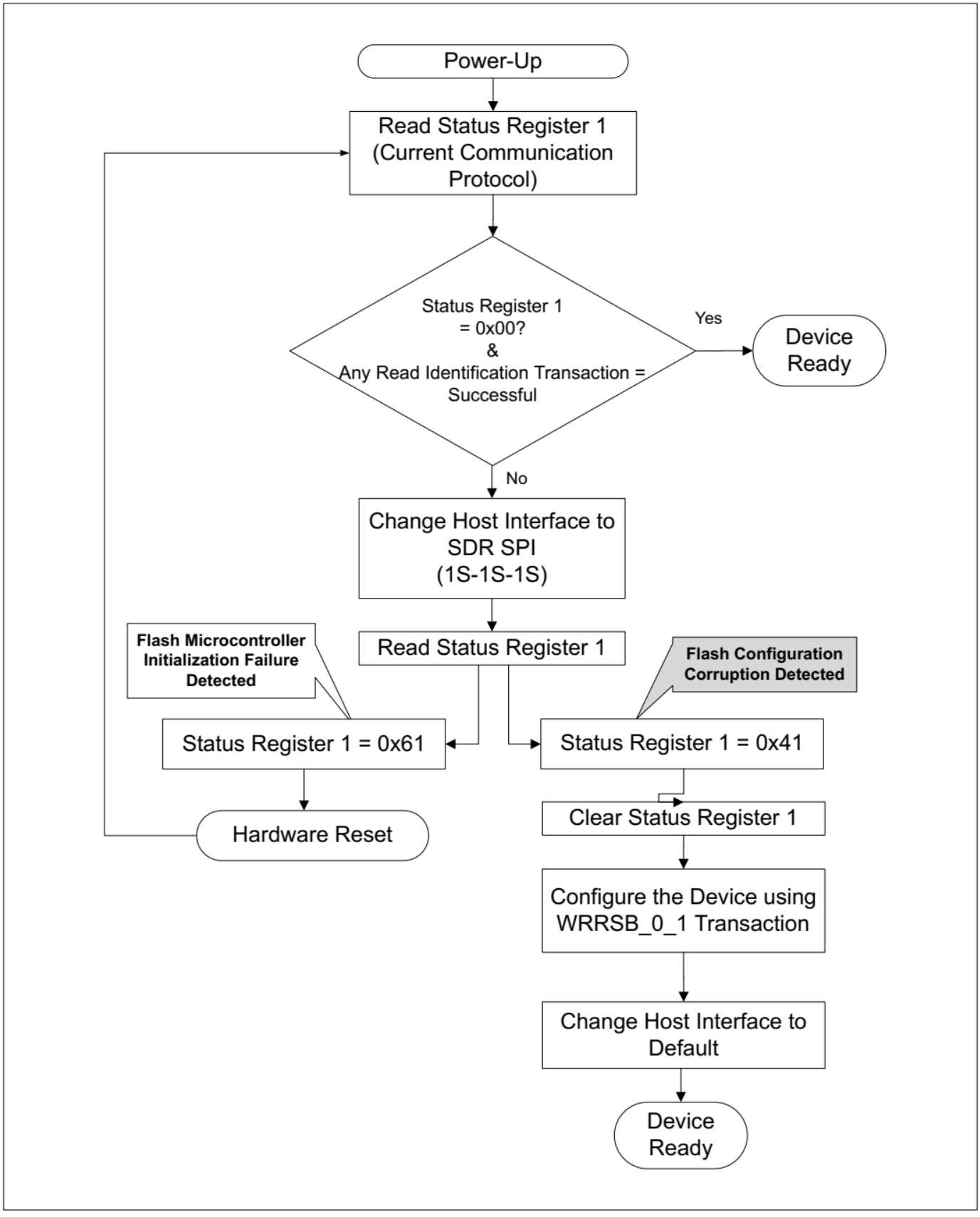

图 54　　配置损坏检测的主控轮询序列

注释： *轮询序列必须从较高的I/O 接口配置开始到较低的I/O 接口配置。例如，4S-4D-4D 到1S-1S-1S。反之则不然。*

4.5.2.2 配置损坏检测相关寄存器

表 32 配置损坏检测相关寄存器和传输命令

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Status Register 1 Volatile (STR1V) (see Table 47)	All 1S-1S-1S transactions	N/A

4.6 自动启动

AutoBoot 允许主控在上电后或硬件复位后从 HL-T/HS-T 设备家族读取数据，而无需发送任何读取命令（包括地址）。根据器件配置，一旦 CS# 变为低电平并且 CK 被切换，数据就会在接口 I/O 上输出。

读取数据的起始地址在 AutoBoot 寄存器 (ATBN[31:9] - STADR[22:0]) 中指定。该起始地址可以位于内存中的任何页边界位置（512 字节页边界）。AutoBoot寄存器中还标识了启动延迟，它以时钟周期数 (ATBN[8:1] - STDLY[7:0]) 表示。这个延迟是在数据读取之前设定的。可以对延迟进行编程以满足主控的要求，但需要根据操作频率满足内存访问时间的最小量。强烈建议在AutoBoot执行成功或失败后检查状态寄存器 1 的值，以验证配置是否损坏（SafeBoot）。

注释： *必须禁用AutoBoot 的Wrap 功能。*

注释： *当读取密码功能启用时，自动启动将被禁用，作为高级扇区保护的一部分。当读取密码功能启用时，建议禁用，不能使用AutoBoot (ATBN[0] - ATBTEN)。*

注释： *强烈建议在长数据保留区域中分配第一个AutoBoot 地址。*

4.6.1 AutoBoot 相关的寄存器和命令传输

表 33 AutoBoot 相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
AutoBoot Register (ATBN) (see Table 72)	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)
	AutoBoot transaction (see Figure 15)	AutoBoot QPI transaction (see hik1745388706386Figure 26)

4.7 读取

HL-T/HS-T 支持不同的读命令传输来访问不同的存储器映射，即：读存储器阵列、读器件标识、读寄存器、读安全存储区域、读DYB和 PPB保护位。

这些读取命令传输可以使用传输协议部分提到的任何协议，并且可能可以使用以下功能：

- 读取命令传输需要在地址之后增加延迟周期，以留出时间访问内存阵列（1S-1S-1S 协议的 RDAY1_4_0 和 RDAY1_C_0 除外）（参见表 54）。
- 读取命令传输可以在数据开始之前的延迟周期内，对所有数据输出使用由内存驱动的数据学习类型码 (DLP)（请参阅“数据学习类型码（DLP）”）。
- 读取命令传输具有 8、16、32 或 64 字节的回卷读取长度和对齐组选项（参见表58 和表59 ）。

4.7.1 读取身份识别命令传输

共有三种唯一标识交易，每种交易都支持单 SPI 和四SPI协议（见表 79）。

4.7.1.1 读取器件标识命令传输

读取器件标识 (RDIDN_0_0) 命令传输提供对制造商标识和器件标识的读取访问。 该命令传输使用 (CFR3V[7:6]) 的延迟周期来实现 166MHz 的最大时钟频率。

4.7.1.2 读取四线识别

读取四线标识 (RDQID_0) 命令传输提供对制造商标识、器件标识信息的读取访问。此命令传输是在 QPI 模式下读取 RDIDN_0_0 命令传输提供的相同信息的另一种方法。在所有其他方面，该命令传输的行为与 RDIDN_0_0 命令传输相同。

仅当器件处于四线模式（CFR1V[1] = 1）时，才能识别该命令传输。 该指令传输在 DQ0-DQ3 上移入。当指令的最后一位移入器件后，然后是延迟周期，然后在 DQ0-DQ3 上依次移出 1 字节制造商标识和 2 字节器件标识。 如果继续将输出移位到定义的 ID 地址空间的末尾，则会提供未定义的数据。命令传输的最大时钟频率为 166 MHz。

4.7.1.3 读取 SFDP 命令传输

读取串行闪存式存储器可发现参数 (RSFDP_3_0) 命令传输提供对JEDEC串行闪存式存储器发现参数 (SFDP) 的访问（见表 79)。命令传输使用 3 字节地址方式。如果设置了非零地址，则 SFDP 空间中的选定位置为数据读取的起点。这样可以随机访问 SFDP 空间中的任何参数。RSFDP_3_0 命令传输支持连续（顺序）读取。需要八个延迟周期。在提供密码之前，读取 SFDP 命令传输不支持读取密码模式。读取 SFDP 命令传输的最大时钟频率为 50 MHz。

4.7.1.4 读取唯一标识命令传输

读取唯一标识（RDUID_0_0）命令传输类似于读取器件标识命令传输，但访问每个器件唯一且不同的 64 位数字。它是工厂预烧录。

4.7.1.5 读取身份识别相关寄存器及命令传输

表 34 读取身份识别相关寄存器及命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Configuration Register 3 (CFR3N, CFR3V) (see Table 56)	Read Identification (RDIDN_0_0)	Read Identification (RDIDN_0_0)
	Read Serial Flash Discoverable (RSFDP_3_0)	Read Serial Flash Discoverable (RSFDP_3_0)
	Read Unique Identification (RDUID_0_0)	Read Unique Identification (RDUID_0_0)
		Read Quad Manufacturer and Device Identification (RDQID_0_0)

4.7.2 读取内存阵列命令传输

内存阵列数据可以从任意字节界限开始从内存中读取。数据字节按顺序从逐渐升高的字节地址读取，直到主控通过驱动 CS# 输入高电平来结束数据传输。如果字节地址达到闪存阵列的最大地址，则读取将从阵列的地址零继续。

4.7.2.1 SPI 读取和快速读取命令传输

SPI SDR读取和快速SDR读取命令传输（1S-1S-1S）用来向后兼容旧版的主控系统快速SDR读取命令传输可采用 3 字节或 4 字节地址选项。该协议不支持用于捕获数据的 DLP。可以选择回卷读取长度。读取命令传输的最大时钟频率为 50 MHz，并且不需要延迟周期。快速读取命令传输使用 (CFR2V[3:0]) 的延迟周期来实现 166 MHz 的最大时钟频率（参见表 79）。

读取快速 4 字节命令传输在地址后面具有连续读取的模式位，因此，在第一个读取快速 4 字节指令发送 Axh 的模式位类型码（指示后续命令传输也将是读取快速 4 字节指令）后，随后的一系列读取快速 4 字节命令传输可以省略八位指令输入。 在系列中的第一个读取快速 4 字节指令以 8 位指令开始，后跟地址，然后跟八个周期的模式位，后跟可选的延迟周期。 如果模式唤醒类型码为 Axh，则假定下一个命令传输是不提供指令位的另外的快速读取 4 字节命令传输。 该命令传输从地址开始，然后是模式位，然后是可选延迟周期。然后，位于给定地址的内存内容将通过 DQ1_SO 移出。

4.7.2.2 读取 SDR 双 I/O 命令传输

读取SDR双 I/O 命令传输使用双 I/O SDR (1S-2S-2S) 协议提供高数据吞吐量。此协议不支持 DLP 数据捕获。可以使用回卷读取长度选项。它支持 3 或 4 字节地址选项。它支持模式位和连续读取命令传输。此命令传输使用由 (CFR2V[3:0]) 设置的延迟周期，使能最大 166 MHz 时钟频率（见表 79）。

4.7.2.3 读取 SDR 四线输出命令传输

读取 SDR 四线输出事务使用 SDR 四线输出 (1S-1S-4S) 协议。该协议支持 DLP 数据捕获。可以选择回卷读取长度。它支持 3 字节或 4 字节地址

4.7.2.4 读取 SDR 和 DDR 四线 I/O 命令传输

读取 SDR 四线 I/O 命令传输使用 SDR 四线 I/O（1S-4S-4S）协议，读取 DDR 四线 I/O 命令传输使用 DDR 四线 I/O（1S-4D-4D）协议。这些协议支持 DLP 数据捕获。可以选择回卷读取长度。这两种命令传输还支持模式位和连续读取命令传输。在SDR Quad I/O 命令传输中，模式位类型码为 Axh，并且下一个命令传输被视为不提供指令位的额外的SDR Quad I/O 命令传输。

在 DDR 四线 I/O 事务中，模式位模式为 A5h，并且假定下一个事务是另一个不提供指令位的 DDR 四线 I/O 事务。它们支持 3 字节或 4 字节的地址选项。这些事务使用延迟周期 (CFR2V[3:0]) 来实现最大 166 MHz 的时钟频率（参见表 79）。

4.7.2.5 读取 QPI SDR 和 DDR 命令传输

读取 QPI SDR 命令传输使用 SDR QPI(4S-4S-4S) 协议，读取 QPI DDR 命令传输使用 DDR QPI (4S-4D-4D) 协议。这些协议支持 DLP 数据捕获。可以选择回卷读取长度。这两种命令传输还支持模式位和连续读取命令传输。在SDR QPI命令传输中，模式类型码是Axh，并且假设下一个命令传输是不提供指令位的额外SDR QPI命令传输。

在 DDR QPI 事务中，模式位模式为 A5h，并且假定下一个事务是一个不提供指令位的附加 DDR QPI 事务。它们支持 3 字节或 4 字节的地址选项。这些事务使用延迟周期 (CFR2V[3:0]) 来使最大时钟频率达到 166 MHz（参见表79）。

4.7.2.6 读取内存阵列相关的寄存器和命令传输

表 35 读取内存阵列相关的寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related dual I/O transactions (see Table 80)	Related quad SPI transactions (see Table 83)
Configuration Register 2 (CFR2N, CFR2V) (see Table 54)	Read SDR (RDAY1_4_0, RDAY1_C_0)	Read SDR Dual I/O (RDAY3_4_0, RDAY3_C_0)	Read SDR Quad Output (RDAY4_4_0, RDAY4_C_0)
Configuration Register 4 (CFR4N, CFR4V) (see Table 58)	Read Fast SDR (RDAY2_4_0, RDAY2_C_0)	Continuous Read SDR Dual I/O (RDAY6_4_0, RDAY6_C_0)	Read SDR Quad I/O (RDAY5_4_0, RDAY5_C_0)
Data Learning Pattern (DLPN, DLPV) (see Table 69)	–	–	Continuous Read SDR Quad I/O (RDAY6_4_0, RDAY6_C_0)
	–	–	Read DDR Quad I/O (RDAY7_4_0, RDAY7_C_0)
	–	–	Continuous Read DDR Quad I/O (RDAY8_4_0, RDAY8_C_0)

（表格续下页.....）

表 35 （续）读取存储器阵列相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related dual I/O transactions (see Table 80)	Related quad SPI transactions (see Table 83)
	–	–	Read QPI SDR (RDAY5_4_0, RDAY5_C_0)
	–	–	Continuous Read QPI SDR (RDAY6_4_0, RDAY6_C_0)
	–	–	Read QPI DDR (RDAY7_4_0, RDAY7_C_0)
	–	–	Continuous Read QPI DDR (RDAY8_4_0, RDAY8_C_0)

4.7.3 读取寄存器命令传输

有多个寄存器用于报告嵌入式操作状态或控制器件配置选项。寄存器包含易失性位和非易失性位。有两种方法可以读取寄存器。读取任何寄存器命令传输提供了一种读取所有器件寄存器的方法：通过地址选择非易失性和易失性。还有专用的寄存器读取命令传输，它们是根据寄存器定义的，并且只读取该寄存器的内容。

4.7.3.1 读取任何寄存器

读取任何寄存器（RDARG_C_0）事务是读取所有器件寄存器的最佳方式，无论是非易失性还是易失性。该事务包括要读取的寄存器的地址（参见表 79 ）。接下来是一些延迟周期（CFR2V[3:0]）用于读取非易失性寄存器和 CFR3V[7:6] 用于读取易失性寄存器。参见表 55 对于 NV 寄存器延迟周期和表 57 对于易失性寄存器延迟周期。然后，返回所选择的发送内容。如果继续读访问，则返回相同寻址的寄存器内容，直到事务终止；每个 RDARG_C_0 事务仅读取一个字节地址。对于超过 1 字节数据的读取，必须再次使用 RDARG_C_0 事务来读取每字节数据。

RDARG_C_0 命令传输的最大时钟频率为 166 MHz。

RDARG_C_0 命令传输可在嵌入式操作期间用于读取状态寄存器 1 (STR1V)。它不用于读取 ASP PPB 访问寄存器 (PPAV) 和 ASP 动态功能块访问寄存器 (DYAV) 等寄存器。需要单独的指令来选择和读取所访问阵列中的位置。如果通过编程 ASPR[2:0] 选择了 ASP 密码保护模式，则 RDARG_C_0 事务将从 PASS 寄存器位置读取无效数据。读取未定义的位置会提供未定义的数据。

4.7.3.2 读取状态寄存器命令传输

读取状态寄存器（RDSR1_0_0、RDSR2_0_0）命令传输允许读取状态寄存器的易失性内容。该命令传输使用 (CFR3V[7:6]) 的延迟周期来读取易失性寄存器，以实现 166 MHz 的最大时钟频率。

状态寄存器内容的易失性版本可随时读取，即使在烧录、擦除或写入操作正在进行时也是如此。

通过提供八个时钟周期的整倍数，可以连续读取状态寄存器 1。每读取八个周期就会更新一次状态。

4.7.3.3 读取配置寄存器命令传输

读取配置寄存器（RDCR1_0_0）命令传输允许读取配置寄存器的易失性内容。该命令传输使用 (CFR3V[7:6]) 的延迟周期来读取易失性寄存器，以实现 166 MHz 的最大时钟频率。

状态寄存器内容的易失性版本可随时读取，即使在烧录、擦除或写入操作正在进行时也是如此。

通过提供八个时钟周期的倍数，可以连续读取配置寄存器。每读取八个周期就会更新一次状态。

4.7.3.4 读取动态保护位 (DYB) 访问寄存器命令传输

读取DYB访问寄存器（RDDYB_4_0、RDDYB_C_0）命令传输读取DYB访问寄存器的内容。该命令传输使用 (CFR3V[7:6]) 的延迟周期来读取易失性寄存器，以实现 166 MHz 的最大时钟频率。可以连续读取DYB访问寄存器，但DYB寄存器的地址不会递增，因此无法以这种方式读取整个DYB数组。必须使用单独的读取 DYB 命令传输来读取每个位置。

4.7.3.5 读取持久保护位 (PPB) 访问寄存器命令传输

读取 PPB 访问寄存器（RDPBB_4_0、RDPBB_C_0）命令传输读取 PPB 访问寄存器的内容。该命令传输使用 (CFR2V[3:0]) 的延迟周期来实现 166 MHz 的最大时钟频率。可以连续读取 PPB 访问寄存器，但 PPB 寄存器的地址不会递增，因此无法以这种方式读取整个 PPB 格式。 必须使用单独的读取 PPB 命令传输来读取每个位置。

4.7.3.6 读取 PPB 锁定寄存器命令传输

读取 PPB 锁定寄存器 (RDPLB_0_0) 命令传输允许读取非易失性寄存器的内容。该命令传输使用 (CFR3V[7:6]) 的延迟周期来读取易失性寄存器，以实现 166 MHz 的最大时钟频率。可以连续读取 PPB 锁定位。

4.7.3.7 读取ECC数据单元状态

读取ECC数据单元状态（RDECC_4_0、RDECC_C_0）命令传输用于确定所寻址的单元数据的ECC状态。 在此命令传输中，地址的 LSb 必须与ECC数据单元对齐。该命令传输使用 (CFR3V[7:6]) 的延迟周期来读取易失性寄存器，从而使最大时钟频率达到 166 MHz。

所选ECC单元的ECC状态的字节内容随之输出。任何后续数据都将是不确定的。要读取下一个ECC单元状态，应将另一个 RDECC_4_0 或 RDECC_C_0 命令传输发送到下一个地址，增量为 16 [数据单元大小/8] 字节。

4.7.3.8 读取寄存器相关的寄存器和命令传输

表 36 读寄存器相关的寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Configuration Register 2 (CFR2N, CFR2V) (see Table 54)	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
Configuration Register 3 (CFR3N, CFR3V) (see Table 56)	Read Status Register 1 (RDSR1_0_0)	Read Status Register 1 (RDSR1_0_0)
	Read Status Register 2 (RDSR2_0_0)	Read Status Register 2 (RDSR2_0_0)
	Read DYB (RDDYB_4_0, RDDYB_C_0)	Read DYB (RDDYB_4_0, RDDYB_C_0)
	Read PPB (RDPPB_4_0, RDPPB_C_0)	Read PPB (RDPPB_4_0, RDPPB_C_0)
	Read PPB Lock (RDPLB_0_0)	Read PPB Lock (RDPLB_0_0)
	Read ECC Status (RDECC_4_0, RDECC_C_0)	Read ECC Status (RDECC_4_0, RDECC_C_0)
	Read Configuration Register 1 (RDCR1_0_0)	Read Configuration Register 1 (RDCR1_0_0)

4.7.4 数据学习模式 (DLP)

该器件支持数据学习类型码 (DLP)，允许主控控制器优化数据捕获窗口。 READ 前导训练仅在 Quad Mode READ 中可用。可编程训练类型码存储在 DLP 寄存器中。 为了进行训练，必须将非零类型码存储在 DLP 寄存器中。 器件在延迟周期内输出类型码。 由于前三个延迟时钟周期被视为延迟周期，因此主控输入的地址末尾和器件输出的类型码之间的总线转换时间不是问题。 所有 IO 信号传输相同的数据学习类型码位。

器件在延迟周期期间输出学习类型码。 IO 信号上驱动的类型码取决于 READ 命令传输可用的延迟周期数。 如果将SDR操作的延迟设置为至少 9 个时钟周期，则器件将在输出读取数据之前的最后 8 个时钟周期在 IO 上输出类型码。 然而，如果延迟设置为小于9个时钟周期，则不会输出任何数据学习类型码。如果将 DDR 操作的延迟设置为至少 5 个时钟周期，则器件将在输出读取数据之前的最后 4 个时钟周期在 IO 上输出类型码。 但是，如果延迟设置为小于 4 个时钟周期，则不会输出任何数据学习类型码。

4.7.4.1 数据学习模式相关寄存器和命令传输

表 37 DLP 相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Data Learning Register (DLPN, DLPN) (see tables 54)	Program Data Learning Pattern (PRDLP_0_1)	Program Data Learning Pattern (PRDLP_0_1)

（表格续下页……）

表 37 （续）DLP 相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
	Write Data Learning Pattern (WRDLP_0_1)	Write Data Learning Pattern (WRDLP_0_1)
	Read Data Learning Pattern Register (RDDLP_0_0)	Read Data Learning Pattern Register (RDDLP_0_0)

4.8 写入

有用于写入寄存器的写入命令传输。这些写入命令传输可以使用命令传输协议部分中提到的 SPI 和 Quad SPI 协议：

4.8.1 写入使能命令传输

写入使能 (WRENB_0_0) 命令传输将状态寄存器 1 (STR1V[1]) 的写入程序使能状态 (WRPGEN) 位设置为“1”。通过发出写入使能 (WRENB_0_0) 命令传输来使能写入、编程和擦除命令传输，WRPGEN 位必须置位为“1”（参见表79 ）。

4.8.2 易失性寄存器的写入使能

可以通过发送 WRENV_0_0 命令传输，然后接着发送任何写入寄存器命令传输来写入易失性状态和配置寄存器。这使得可以更灵活地快速更改系统配置和内存保护方案，而无需等待典型的非易失性位写周期，也不会影响状态或配置非易失性寄存器位的耐用性。WRENV_0_0 命令传输仅用于指示下一个写寄存器命令传输改变易失性状态和配置寄存器位值。

4.8.3 写无效命令传输

写无效（WRDIS_0_0）命令传输将状态注册1（STR1V[1]）的写程序使能状态（WRPGEN）位清除为“0”。

可以通过发出写无效 (WRDIS_0_0) 命令传输来将 WRPGEN 位清除为 0，来禁止那些需要将 WRPGEN 位置为 '1' 才能执行的命令。用户可以使用 WRDIS_0_0 命令传输来保护内存区域，防止无意的写入、烧录或擦除操作破坏内存内容。当 RDYBSY 位 = 1 (STR1V[0]) 时，WRDIS_0_0 命令传输在嵌入式操作期间被忽略（参见表79 ）。

4.8.4 清除写入和擦除失败标志命令传输

清除写入和擦除失败标志（CLPEF_0_0）命令传输将位STR1V[5]（擦除错误标志）和位STR1V[6]（写入错误标志）重置为“0”。即使当器件保持忙且 RDYBSY 置位为“1”时，该命令传输也会被接受，即使当任一故障位为置位且器件保持忙时。本次命令传输执行后，WRPGEN 位将保持不变（见表 79 ）。

4.8.5 清除ECC状态寄存器命令传输

清零，复位ECC状态寄存器(CLECC_0_0)命令传输复位位ECSV[4](2位ECC检测)、位ECSV[3](1位ECC校正)、INSV[1:0] ECC检测状态位、地址捕获寄存器EATV[31:0]和ECC检测元件ECTV[15:0]。在执行此命令之前，没有必要设置 WRPGEN 位。即使器件仍处于繁忙状态且 WRPGEN 置位为“1”，清除ECC状态寄存器交易

也会被接受，因为当任一故障位为置位时，器件仍保持忙碌状态。该指令执行后，WRPGEN 位将保持不变（见表 79）。

4.8.6 写入寄存器命令传输

写入寄存器（WRREG_0_1）命令传输允许将新值写入状态寄存器和配置寄存器。在器件接受写寄存器命令传输之前，必须收到写使能或易失性寄存器写使能的命令传输。成功解码写使能指令后，器件会将状态寄存器中的 WRPGEN 置位，以实现任何写操作。

写寄存器命令传输是通过将指令和数据字节移到 DQ0_SI 上输入来实现的。状态和配置寄存器的长度为一个数据字节。

WRR 操作首先擦除寄存器，然后将新值编程为单一操作。如果 WRREG_0_1 操作失败，则写寄存器命令传输将置位 PRGERR 或 ERSERR 位。

4.8.7 写入任意寄存器命令传输

写入任意寄存器（WRARG_C_1）命令传输提供了一种写入任何器件寄存器（非易失性或易失性）的方法。该命令传输包括要写入的寄存器的地址，后面跟着要写入寻址寄存器的一个字节的数据（见表 79）。

在器件接受 WRARG_C_1 命令传输之前，必须发出并解码写使能 (WRENB_0_0) 命令传输，这将状态寄存器中的写入/编程使能位 (WRPGEN) 设置为可以进行任何写入操作。可以检查 STR1V[0] 中的 RDYDSY 位来确定操作何时完成。可以检查 STR1V[6:5] 中的 PRGERR 和 ERSERR 位来确定操作期间是否发生任何错误。

一些寄存器混合了多种位类型和单独的规则来控制哪些位可以被修改。有些位是只读的，有些是 OTP，有些被指定为保留位（DNU）。

只读位永远不会被修改，并且 WRARG_C_1 命令传输数据字节中的相关位将被忽略，而不会设置编程或擦除错误指示（STR1V[6:5] 中的 PRGERR 或 ERSERR）。因此，WRARG_C_1 数据字节中这些位的值并不重要。

OTP位只能被编程为与其默认状态相反的位。将OTP位写回到其默认状态的操作将被忽略，并且不会发生任何错误。

由WRARG_C_1数据改变的非易失性位需要更新非易失性寄存器写入时间(tW)。更新过程包括对非易失性寄存器位进行擦除和编程操作。如果更新的部分或程序部分失败，则 STR1V 中的相关故障位和 RDYBSY 位将置位为“1”。

状态寄存器 1 可以被重复读取（轮询）来监测 RDYBSY 位（STR1V[0]）和错误位（STR1V[6,5]）并确定何时寄存器写入完成或失败。如果发生写入失败，则使用 CLPEF_0_0 命令传输清除错误状态并使器件返回待机状态。

ASP PPB 锁定寄存器 (PPLV) 寄存器不能通过 WRARG_C_1 命令传输写入。只有写 PPB 锁定位 (WRPLB_0_0) 命令传输可以写入 PPLV 寄存器。

数据完整性检查寄存器不能通过 WRARG_C_1 命令传输写入。通过运行数据完整性检查命令传输（DICHK_4_1）来加载数据完整性检查寄存器。

4.8.8 写入 PPB 锁定位

写入 PPB 锁定位 (WRPLB_0_0) 命令传输将 PPB 锁定寄存器 PPLV[0] 清除为零。PPBLCK 位用于保护 PPB 位。当 PPLV[0] = 0 时，PPB 编程/擦除命令传输将被中止。在读取密码保护模式下，PPBLCK 位还用于控制地址的高阶位，方法是强制将地址范围限制为存储引导代码的一个扇区，直到提供读取密码（见

表 79 ）。

在器件接受 WRPLB_0_0 命令传输之前，必须发出写使能 (WRENB_0_0) 命令传输并器件对其进行解码，这会将状态寄存器中的写/编程使能 (WRPGEN) 设置为 1，以允许任何写操作。

操作进行期间，仍可读取状态寄存器以检查 RDYBSY 位的值。在自定时操作期间，WRPGEN 位为“1”，操作完成后为“0”。当写入 PPB 锁事务完成后，RDYBSY 位被置位为“0”（参见表 79）。

4.8.9 进入4字节地址模式

输入 4 字节地址模式 (EN4BA_0_0) 命令传输将易失性地址长度位 (CR2V[7]) 设置为“1”，以将大多数 3 字节地址指令更改为需要 4 字节地址。 读取 SFDP （RSFDP_3_0） 命令传输不受地址长度位的影响。JEDEC JESD216 标准要求 RSFDP_3_0 始终只有 3 个字节的地址。

POR 、硬件或软件复位将根据非易失地址长度位 (CR2N[7]) 中的定义来设置地址长度。

4.8.10 退出 4 字节地址模式

退出 4 字节地址模式 (EX4BA_0_0) 指令将易失性地址长度位 (CR2V[7]) 设置为“0”，以将大多数 3 字节地址指令更改为需要 3 字节的地址。 该指令不会仅影响 4 字节地址指令，该指令仍将继续要求 4 字节地址。

4.8.11 写入命令相关的寄存器和命令传输

表 38 写入命令相关的寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related Quad SPI transactions (see Table 83)
Status Register 1 (STR1N, STR1V) (see Table 47)	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)
	Write Registers (WRREG_0_1)	Write Registers (WRREG_0_1)
	Write Enable Volatile (WRENV_0_0)	Write Enable Volatile (WRENV_0_0)
	Write Disable (WRDIS_0_0)	Write Disable (WRDIS_0_0)
ECC Status Register (ECSV) (see Table 61)	Clear Program and Erase Failure Flags (CLPEF_0_0)	Clear Program and Erase Failure Flags (CLPEF_0_0)
	Clear ECC Status Register (CLECC_0_0)	Clear ECC Status Register (CLECC_0_0)
Address Trap Register (EATV) (see Table 62)	Write Any Register (WRARG_C_1)	Write Any Register (WRARG_C_1)
ECC Detection Counter (ECTV) (see Table 63)	Write PPB Lock Bit (WRPLB_0_0)	Write PPB Lock Bit (WRPLB_0_0)
Configuration Register 2 (CFR2V) Table 54	Enter 4 Byte (EN4BA_0_0), Exit 4 Byte (EX4BA_0_0)	Enter 4 Byte (EN4BA_0_0), Exit 4 Byte (EX4BA_0_0)

4.9 编程

有用于将数据编程到存储器阵列、安全区域和持久保护位的写入命令传输。

这些写入命令传输可以使用 SPI 或 Quad SPI 协议：

在器件接受任何写入命令传输之前，必须先发出写使能 (WRENB_0_0) 命令传输并由器件解码。如果状态寄存器中的写/编程使能 (WRPGEN) 设置为“1”以允许程序操作，然后写入命令传输才能由器件执行。当一个写入命令传输完成时，WRPGEN 位被复位为‘0’。

当写入命令传输正在进行时，可以读取状态寄存器 1 以检查器件就绪/忙碌 (RDYBSY) 位的值。自定时写入命令传输期间，RDYBSY 位为“1”，完成时为“0”。

可以检查 STR1V[6] 中的 PGMERR 位来确定写入命令传输期间是否发生任何错误。

应用于已通过任何保护方式进行写保护的扇区的写入命令传输将不会被执行，并且将置位 PGMERR 状态失败。

当 CS# 被驱动到逻辑高电平状态时，写入命令传输将被启动。

4.9.1 编程粒度

HS/L-T家族支持多次写入（位遍历），其中在“1”上写入为“0”而不执行扇区擦除操作。 此器件的非 AEC-Q100 工业温度范围（-40°C 至 +85°C）允许位遍历操作。每一个ECC数据单元在相邻两次擦除之间只允许进行一次写入操作（单次写入）的规则适用于较高温度范围（-40°C 至 +105°C) 和 (–40°C 至 +125°C) 器件以及所有 AEC-Q100 器件。

没有执行擦除操作的多次写入将会使该器件的当前数据单元的ECC功能被禁用。注意如果启用了 2 位 ECC ，则同一扇区内的多次写入将导致写入错误。

4.9.2 页编程

分页写入是通过将要写入的数据加载到分页缓存并发出写入命令传输以将数据从缓存移至内存阵列来完成的。这设置了可使用单个写入命令传输进行写入的数据量的上限。分页写入允许在一次操作中对最多 1 个分页大小（256 或 512 字节）进行写入。 分页大小由配置寄存器 3 的CFR3V[4] 位来决定。分页在分页大小地址边界上对齐。在每个分页写入操作中，可以对从一个位到一个分页大小进行写入。 建议写入16字节长度的倍数和对齐的程序块。这样可确保 ECC 不会被禁用。为了获得最佳的分页写入吞吐率，写入应以 512 字节边界对齐的整页 512 字节进行，并且每个分页只写入一次。

4.9.3 写入分页命令传输

写入分页（PRPGE_4_1、PRPGE_C_1）命令传输将数据写入到存储器阵列中。如果向器件发送的数据大于分页大小（256B 或 512B），则在起始地址和分页对齐结束边界之间的空间中，数据加载序列将从分页中的最后一个字节回卷到同一分页的零字节位置，并开始重写分页中先前加载的任何数据。如果向器件发送的数据少于分页，则发送的数据字节将从分页内提供的地址开始按顺序进行写入，而不会对同一分页的其他字节产生任何影响。写入过程由器件内部控制逻辑管理。PRGERR 位指示写入命令传输中是否发生了阻止写入成功完成的错误。这包括尝试对受保护区域进行写入（见表 79）。

4.9.4 写入安全区域命令传输

写入安全区域 (PRSSR_C_1) 命令传输将数据写入到SSR中，该 SSR 与主阵列数据位于不同的地址空间中，并且是OTP 。 SSR为 1024 字节，因此对于此命令传输，从 A31 到 A10 的地址位必须为零（见表 79 ）。编程SSR空间时，需要将起始地址对齐到 32 位，即地址位 A1 和 A0 应为 0'b，主控应置位 CS# 以与 32 位对齐。

可以检查 STR1V[6] 中的 PRGERR 位来确定操作期间是否发生任何错误。为了以位粒度对OTP阵列进行编程，数据字节内的其余位可以设置为“1”。

每个 SSR 存储空间均可被写入一次或多次，前提是该区域未被锁定。尝试在锁定的区域中写入“0”将失败，并且 STR1V[6] 中的 PRGERR 位置位为 '1'。 写入一次后，即使在受保护的区域也不会发生错误并且不会置位PRGERR位。 后续写入仅可对未写入的位（即为“1”的数据）进行。在同一个ECC单元内写入多次将会使该数据单元上的ECC禁用。

4.9.5 写入持久保护位 (PPB)

写入持久保护位（PRPPB_4_0、PRPPB_C_0）命令传输对 PPB 寄存器中的位进行写入，以保护所提供地址的扇区不被写入或擦除（见表 79 ）。

可以检查 STR1V[6] 中的 PRGERR 位来确定操作期间是否发生任何错误。当尝试对受 ASPPPB （ASPO[3]）、ASPPRM （ASPO[0]）和 PPBLCK （PPLV[0]）位保护的 PPB 位进行写入时，写入 PPB 位命令传输将会中止/退出。

4.9.6 写入相关的寄存器和命令传输

表 39 写入相关的寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Status Register 1 (STR1N, STR1V) (see Table 47)	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)
	Program Page (PRPGE_4_1, PRPGE_C_1)	Program Page (PRPGE_4_1, PRPGE_C_1)
Advance Sector Protect Register (ASPO) (see Table 64)	Program Secure Silicon (PRSSR_C_1)	Program Secure Silicon (PRSSR_C_1)
ASP PPB Lock (PPLV) (see Table 66)	Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0)	Program Persistent Protection Bit (PRPPB_4_0, PRPPB_C_0)
ECC Status Register (ECSV) (see Table 61)	Clear Program and Erase Failure Flags (CLPEF_0_0)	Clear Program and Erase Failure Flags (CLPEF_0_0)

4.10 擦除

对于内存阵列和持久保护位，有擦除命令传输可以将数据位变为“1”（所有字节均为 FFh）。

在器件接受任何擦除命令传输之前，必须发出写使能 (WRENB_0_0) 命令传输并且被器件接收对其进行解码。如果状态寄存器中的 Write/Program 使能位 (WRPGEN) 置位为 '1' 来使能擦除操作，擦除命令传输才能被器件执行。当一个命令传输完成时，WRPGEN 位复位为“0”。

当命令传输处理正在进行时，可以读取状态 1 以检查器件就绪/忙 (RDYBSY) 位的值。自定时擦除命令传输期间，RDYBSY 位为“1”，完成时为“0”。

可以检查 STR1V[5] 中的 ERSERR 位来确定擦除命令传输期间是否发生任何错误。

应用于已通过块保护位或 ASP 写保护的扇区的擦除命令传输将不会被执行，并且将置位 ERSERR 状态失败位。

当 CS# 被驱动到逻辑高电平状态时，将启动擦除命令传输。

该器件出厂时的默认状态是所有字节均为 FFh。

4.10.1 擦除 4KB 扇区命令传输

擦除4KB扇区（ER004_4_0，ER004_C_0）命令传输将4KB扇区的所有位设置为“1”（所有字节均为FFh）（参见表 79）。

仅当器件配置为统一扇区（CFR3V [3] = 1）时，此命令传输将被忽略。如果将擦除 4KB 扇区命令传输发送到非 4KB 扇区地址，则器件将中止/退出该操作，并且不会设置 ERSERR 状态失败位。

4.10.2 擦除 256 KB 扇区命令传输

擦除256 KB 扇区（ER256_4_0、ER256_C_0）命令传输将寻址扇区中的所有位设置为“1”（所有字节均为 FFh）（参见表 79 ）。

器件配置选项 (CFR3V[3]) 决定是否使用混合扇区架构。CFR3V[3] = 0 时, 4 KB 区扇覆盖器件地址空间的最高或最低地址 128 KB 或 64 KB 的一部分。如果扇区擦除命令传输应用于被 4 KB 扇区覆盖的 256 KB 扇区，则被覆盖的 4 KB 扇区不受扇区影响。仅可见（非覆盖）的128 KB 或 192 KB 扇区的部分会被擦除。
当 CFR3V[3] = 1 时，器件地址空间中没有 4 KB 扇区，扇区擦除命令传输始终在完全可见的 256 KB 扇区上运行。

当 BLKCHK 启用时，扇区擦除命令传输首先评估扇区的擦除状态。如果发现该扇区已被擦除，则擦除操作将中止。仅当在扇区中找到写入位时才会执行擦除操作。禁用 BLKCHK 将无条件执行擦除操作。

4.10.3 擦除芯片命令传输

擦除芯片（ERCHP_0_0）命令传输将整个闪存阵列内的所有位设置为“1”（所有字节均为 FFh）（参见表 79 ）。

仅当块保护位（BP2、BP1、BP0）置位为0时，才能执行擦除芯片命令传输。 若BP位不为零，则不执行命令传输，且ERSERR状态失败位不置位。命令传输将跳过任何受高级扇区保护DYB或 PPB 保护的扇区，并且 ERSERR 状态失败位将不会设置。

4.10.4 擦除持久保护位 (PPB) 命令传输

擦除 PPB 命令传输（ERPPB_0_0）将所有 PPB 位设置为‘1’（见表 79 ）。如果 PPB 位受 ASPPPB (ASPO[3])、ASPPRM (ASPO[0]) 和 PPBLCK (PPLV[0]) 位保护，则此命令传输将中止/退出。

4.10.5 擦除状态及计数

4.10.5.1 评估擦除状态命令传输

评估擦除状态 (EVERS_C_0) 指令用于验证对已指定地址的扇区进行的擦除操作是否完全成功。所选扇区被成功擦除，则擦除状态位 (STR2V[2]) 置位为 1。如果选定的扇区未被完全擦除，则 STR2V[2] 为“0”。在此事务之前不需要进行写/编程使能命令（设置 WRPGEN 位）。但是，RDYBSY 位由器件本身置位，并在操作结束时清除，这在读取状态时可在 STR1V[0] 中看到（参见表 79）。

评估擦除状态命令传输可用于检测由于电压跌落、复位或擦除操作期间故障而导致的擦除操作何时失败。该命令传输需要 t_{EES} 完成并更新 STR2V 中的擦除状态。可以读取 RDYBSY 位 (STR1V[0]) 来确定评估擦除状态命令传输何时完成。如果发现扇区未擦除完成并且 STR2V[2] = 0 的情况，则必须再次擦除扇区以确保扇区内数据的可靠存储。

4.10.5.2 扇区擦除计数命令传输

扇区擦除计数 (SEERC_C_0) 命令传输输出指定扇区的扇区擦除次数。扇区扇区计数存储在扇区扇区计数 (SECV[22:0]) 寄存器中，并且可以通过使用读取任何寄存器命令传输 (RDARG_C_0) 来读取。 RDYBSY 位由器件本身置位，并在操作结束时清除，如读取状态时在 STR1V[0] 中可见（见表 79 ）。

该命令传输需要 t_{SEC}时间来完成并更新 SECV[22:0] 寄存器。可以读取 RDYBSY 位 (STR1V[0]) 以确定扇区计数命令传输何时完成。 SECV[23]位用于确定所报告的扇区擦除计数是否已损坏并已复位。

4.10.6 擦除相关寄存器及命令传输

表 40 擦除相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Status Register 1 (STR1N, STR1V) (see Table 47)	Write Enable (WRENB_0_0)	Write Enable (WRENB_0_0)
Status Register 2 (STR2V) (see Table 50)	Erase 4KB Sector (ER004_4_0, ER004_C_0)	Erase 4KB Sector (ER004_4_0, ER004_C_0)
	Erase 256KB Sector (ER256_4_0, ER256_C_0)	Erase 256KB Sector (ER256_4_0, ER256_C_0)
ASP PPB Lock (PPLV) (see Table 66)	Erase Chip (ERCHP_0_0)	Erase Chip (ERCHP_0_0)
ECC Status Register (ECSV) (see Table 61)	Evaluate Erase Status (EVERS_C_0)	Evaluate Erase Status (EVERS_C_0)
Sector Erase Count Register (SECV) (see Table 73)	Sector Erase Count (SEERC_C_0)	Sector Erase Count (SEERC_C_0)
	Erase Persistent Protection Bit (PPB) transaction (ERPPB_0_0)	Erase Persistent Protection Bit (PPB) transaction (ERPPB_0_0)

4.11 暂停和恢复嵌入式操作

HL-T/HS-T 器件可以中断和暂停正在运行的嵌入式操作，例如擦除、写入或数据一致性检查。 一旦主控完成中间操作并将相应的恢复命令传输发送到器件，它还可以恢复暂停的操作。

4.11.1 擦除、写入或数据完整性检查暂停

暂停命令传输允许系统中断写入、擦除或数据完整性检查操作，然后从任何其他非擦除暂停扇区、非编程暂停页面或阵列中读取数据。器件必须检查状态寄存器1 (STR1V[0]) 中的 Ready/Busy 状态标志 (RDYBSY)，以获得写入、擦除或数据一致性检查操作是否已经停止。

4.11.1.1 写入暂停

- 写入暂停仅在写入操作期间有效。
- 状态寄存器 2（STR2V[0]）中的写入操作暂停状态标志（PROGMS）可用于确定在 RDYBSY 变为“0”时写入操作是否已暂停或已完成。
- 可以暂停写入操作以允许读取操作。
- 在写入暂停的分页内的任何地址读取都会产生不确定的数据。

4.11.1.2 擦除挂起

- 擦除挂起命令仅在扇区擦除操作期间有效。
- 状态寄存器 2 (STR2V[1]) 中的擦除操作暂停状态标志 (STR2V[1]) 可用于确定在 RDYBSY 变为“0”时擦除操作是否已暂停或已完成。
- 芯片擦除操作不能暂停。
- 可以暂停擦除操作以允许写入操作或读取操作。
- 在擦除暂停期间，可以读取 DYB 阵列来检查扇区保护情况。
- 在已暂停的擦除、写入或数据完整性检查操作的情况下，不允许进行新的擦除操作。在这种情况下，擦除命令传输将被忽略。
- 读取擦除暂停扇区内的任何地址都会产生不确定的数据。

4.11.1.3 数据完整性检查暂停

- 数据完整性检查暂停仅在数据完整性检查计算操作期间有效。
- 状态寄存器 2 (STR2V[4]) 中的存储器数据完整性检查暂停标志 (DICRCS) 可用于确定在 RDYBSY 更改为“0”时数据完整性检查操作是否已暂停或已完成。
- 可以暂停数据完整性检查操作以允许读取操作。

在擦除、写入或数据完整性检查暂停期间，不允许执行写入任何寄存器或擦除持久保护位命令传输。因此，在暂停挂起期间不可能更改块保护或 PPB 位。如果有扇区在擦除暂停期间可能需要写入，则这些扇区应该仅受 DYB 位的保护，这些 DYB 位可以在擦除暂停期间关闭。

完成暂停操作所需的时间为t_{PEDS}。

擦除挂起的编程操作完成后，EAC返回擦除挂起状态。系统可以通过读取状态寄存器来确定写入操作的状态，就像在执行标准写入操作一样。

表 41 列出暂停操作期间允许的命令传输。

表 41　　暂停期间允许的命令传输

Transaction name	Allowed during erase suspend	Allowed during program suspend	Allowed during data integrity check suspend
Write Disable (WRDIS_0_0)	Yes	No	No

（表格续下页.....）

表 41 （续）暂停期间允许的命令传输

Transaction name	Allowed during erase suspend	Allowed during program suspend	Allowed during data integrity check suspend
Read Status Register 1 (RDSR1_0_0)		Yes	Yes
Write Enable (WRENB_0_0)		No	No
Write Enable Volatile (WRENV_0_0)			
Read Status Register 2 (RDSR2_0_0)		Yes	Yes
Read Configuration Register 1 (RDCR1_0_0)			
Program Page (PRPGE_4_1, PRPGE_C_1)		No	No
Read ECC Status (RDECC_4_0, RDECC_C_0)		Yes	Yes
Clear ECC Status Register (CLECC_0_0)			
Read PPB Lock Bit (RDPLB_0_0)			
Resume Program/Erase/Data Integrity Check (RSEPD_0_0)			
Resume Program/Erase (RSEPA_0_0)			
Program SSR (PRSSR_C_1)		No	No
Read SSR (RDSSR_C_0)		Yes	Yes
Read Unique ID (RDUID_0_0)		Yes	
Read SFDP (RSFDP_3_0)			
Read Quad Manufacturer and device Identification (RDQID_0_0)			
Read Any Register (RDARG_C_0)			
Software Reset Enable (SRSTE_0_0)			
Clear Program and Erase Failure Flags (CLPEF_0_0)			
Software Reset (SFRST_0_0)			
Legacy Software Reset (SFRSL_0_)			
Read Identification Register (RDIDIN_0_0) (manufacturer and device identification)			
Suspend Program/Erase/Data Integrity Check (SPEPD_0_0)		No	No
Suspend Program/Erase (SPEPA_0_0)			
Read DYB (RDDYB_4_0, RDDYB_C_0)		Yes	Yes
Read PPB (RDPPB_4_0, RDPPB_C_0)			
Read SDR (RDAY1_C_0, RDAY1_4_0)			
Read Fast SDR (RDAY2_C_0, RDAY2_4_0)			

（表格续下页……）

表 41　　（续）挂起期间允许的命令传输

Transaction name	Allowed during erase suspend	Allowed during program suspend	Allowed during data integrity check suspend
Read SDR Dual I/O (RDAY3_C_0, RDAY3_4_0)			
Read SDR Quad Output (RDAY4_C_0, RDAY4_4_0)			
Read SDR Quad I/O (RDAY5_C_0, RDAY5_4_0)			
Read DDR Quad I/O (RDAY7_C_0, RDAY7_4_0)	Yes	Yes	Yes
Read Data Learning Pattern (RDDLP_0_0)			

4.11.2　擦除、写入或数据完整性检查恢复

必须通过发送擦除、写入或数据完整性检查恢复命令传输才能恢复暂停的操作。在写入、擦除或数据完整性检查暂停期间完成写入或读取操作后，将发送恢复命令传输以恢复暂停的操作。

发出“擦除”、“编程”或“数据完整性检查恢复”命令后，状态寄存器 1 中的 RDYBSY 位将置位为 1，如果暂停，则编程操作将恢复。如果没有暂停写入操作，则暂停的擦除操作将恢复。如果没有暂停的写入、擦除或数据完整性检查操作，则恢复命令传输将被忽略。

写入、擦除或数据一致性检查操作可以根据需要中断。例如，写入暂停命令传输可以紧跟在写入恢复命令传输之后，但为了使写入或擦除操作能够完成，在恢复和下一个暂停命令传输之间必须有一段大于或等于 t_{PEDRS} 时间间隔。

图 55 显示暂停和恢复操作的流程。

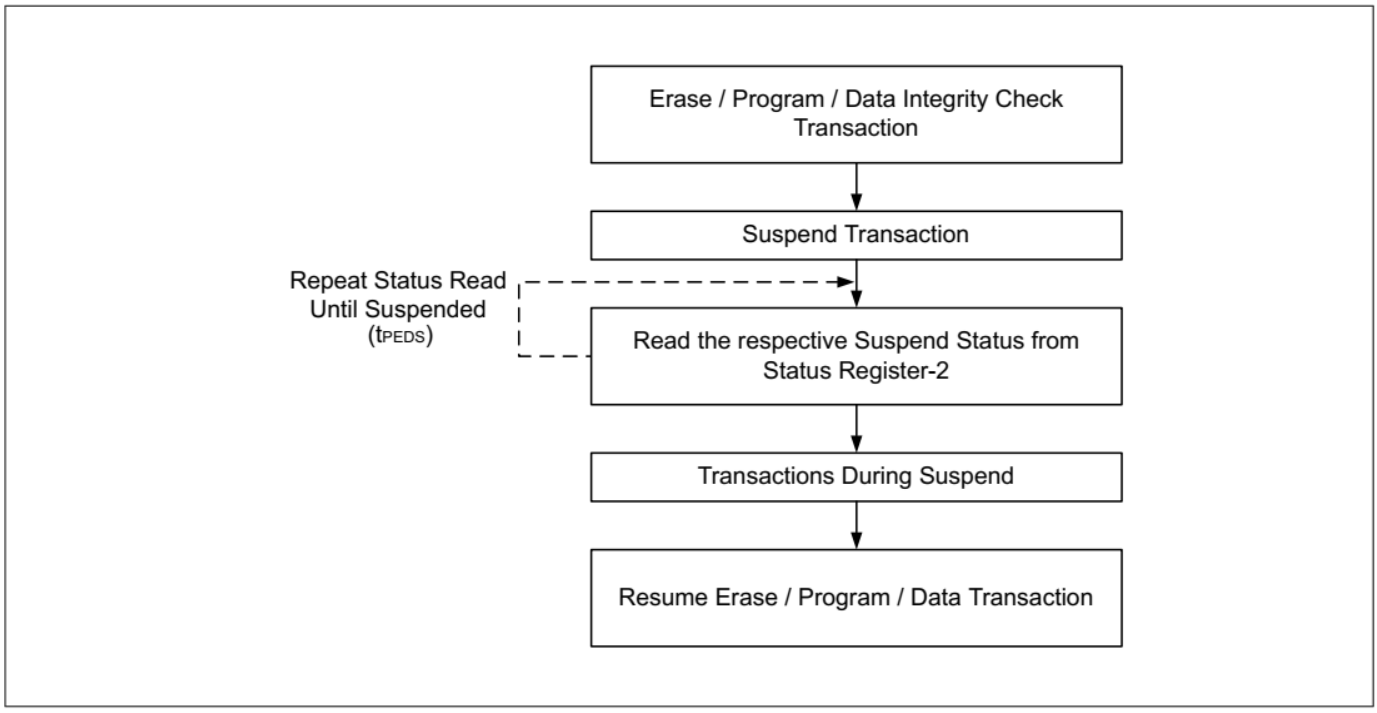

图 55　　暂停和恢复流程

4.11.3　暂停及恢复相关寄存器及命令传输

表 42　　擦除相关寄存器和命令传输

Related registers	**Related SPI transactions (see Table 79)**	**Related quad SPI transactions (see Table 83)**
Status Register 1 (STR1N, STR1V) (see Table 47)	Suspend Erase/Program/Data Integrity Check (SPEPD_0_0)	Suspend Erase/Program/Data Integrity Check (SPEPD_0_0)
Status Register 2 (STR2V) (see Table 50)	Resume Erase/Program/Data Integrity Check (RSEPD_0_0)	Resume Erase/Program/Data Integrity Check (RSEPD_0_0)
	Suspend Erase/Program (SPEPA_0_0)	Suspend Erase/Program (SPEPA_0_0)
	Resume Erase/Program (RSEPA_0_0)	Resume Erase/Program (RSEPA_0_0)
	Read Any Register (RDARG_C_0)	Read Any Register (RDARG_C_0)
	Read Status Register-1 (RDSR1_0_0)	Read Status Register-1 (RDSR1_4_0)
	Read Status Register-2 (RDSR2_0_0)	Read Status Register-2 (RDSR2_4_0)

4.12　复位

HL-T/HS-T器件支持四种复位机制。

- 硬件复位（使用 RESET# 输入引脚和 DQ3_RESET# 引脚）
- 上电复位 (POR)

- JEDEC串行闪存式器件复位信令协议
- 软件复位

4.12.1 硬件复位（使用 RESET# 输入引脚和 DQ3_RESET# 引脚）

RESET# 输入启动复位操作，从逻辑高电平转换为逻辑低电平，持续时间 > t_{RP}，并使器件执行在 POR 期间执行的完整复位过程。硬件复位过程需要 t_{RH} 时间才能完成。见表90 了解时序规范。

当CS# 处于高电平状态的时间超过 t_{CS} 时间或未启用四线或 QPI 模式时，DQ3_RESET# 输入将在以下情况下启动复位操作。DQ3_RESET# 输入具有至 V_{CC}的内部上拉，如果不使用四线或 QPI 模式，则可以悬空。CS# 变为高电平并保持 t_{CS}之后为存储器或主控系统提供了在CS#为低电平时将 DQ3 用作四线或 QPI 模式 I/O 信号之后将 DQ3 驱动为高电平的时间。然后，至 V_{CC} 内部上拉将保持 DQ3_RESET# 为高电平，直到主控系统开始驱动 DQ3_RESET#。当CS#在nt_{CS} 时间内保持高电平时，DQ3_RESET#输入将会被忽略，以避免意外的复位操作。如果将CS# 驱动为低电平以启动新的命令传输，则 DQ3_RESET# 将用作 DQ3。

当器件未处于四线或 QPI 模式时，或当 CS# 为高电平时，DQ3_RESET# 在 t_{CS} 后从 VIL 转换为 VIH 的持续时间大于 t_{RP} 时，器件将以与 POR 相同的方式进行机械复位。机械复位过程需要 t_{RH}的时间才能完成。如果在上电期间（t_{PU}）由于任何原因，POR 过程未能正确完成，则 RESET# 变为低电平将启动完整 POR 过程，而不是机械复位过程，并且需要 t_{PU} 才能完成 POR 过程。

附加 DQ3_RESET# 说明

- 如果 RESET# 和 DQ3_RESET# 输入选项均可用，则系统中仅使用一个复位选项。通过设置 CFR2N[5] = 0 将 DQ3_RESET 设置为仅作为 DQ3 操作，DQ3_RESET# 输入复位操作可以不使能。如果未将 RESET# 输入连接或绑定到 V_{IH}， 则 RESET# 输入将被禁用。在再次变为低电平以启动硬件复位之前， RESET# 和 DQ3_RESET# 必须在 t_{PU} 之后保持为高电平并持续 t_{RS} 时间。
- 当 DQ3_RESET# 被驱动为低电平并持续至少 (t_{RP}) 时（在 t_{CS} 之后），器件将终止正在进行的任何操作，使所有输出处于高阻态，并在 t_{RH} 期间忽略所有读/写命令传输。器件将接口重置为待机状态。
- 如果启用了四线或QPI模式以及DQ3_RESET#特性，则主机在t_{CS}期间不应将DQ3拉低，以避免DQ3驱动器冲突。在四线或QPI模式下向主机传输数据的事务之后（例如：四线I/O读取），主机在t_{CS}期间应将DQ3_RESET#拉高，以避免意外的复位操作。
  在 Quad 模式下，紧接着向存储器传输数据的事务（例如：页编程）之后，主机系统应在 t_{CS} 期间将 DQ3_RESET# 拉高，以避免意外的复位操作。如果启用了 Quad 模式，则在 t_{CS} 期间拉低 DQ3_RESET# 将被忽略。

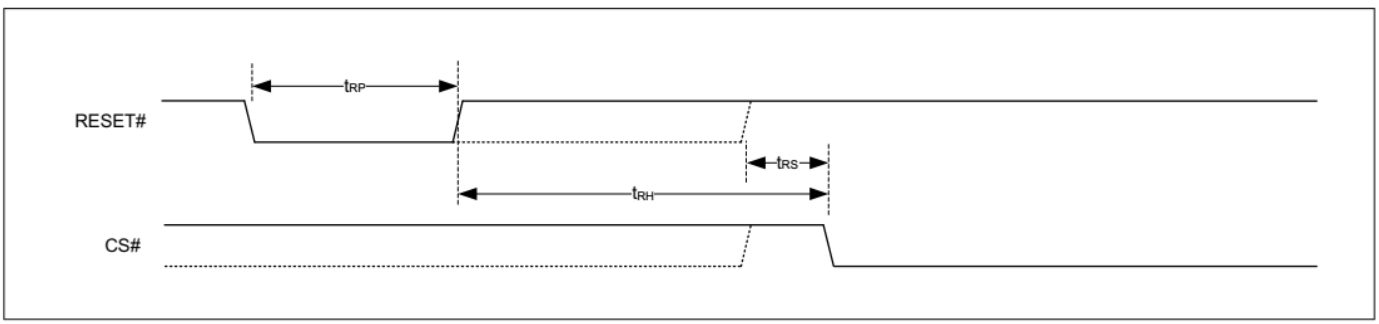

图 56 使用 RESET# 输入进行硬件复位（复位脉冲 = t_{RP} (min)）

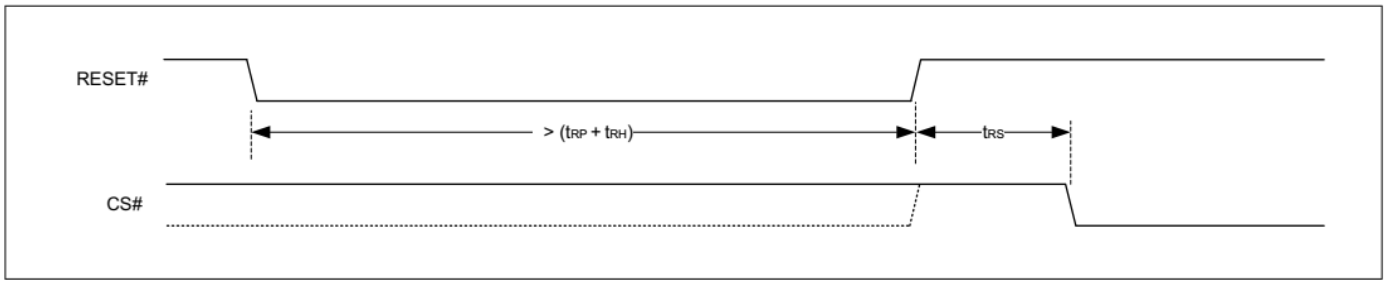

图 57　　使用 RESET# 输入进行硬件复位（复位脉冲 > (t_{RP} + t_{RH})）

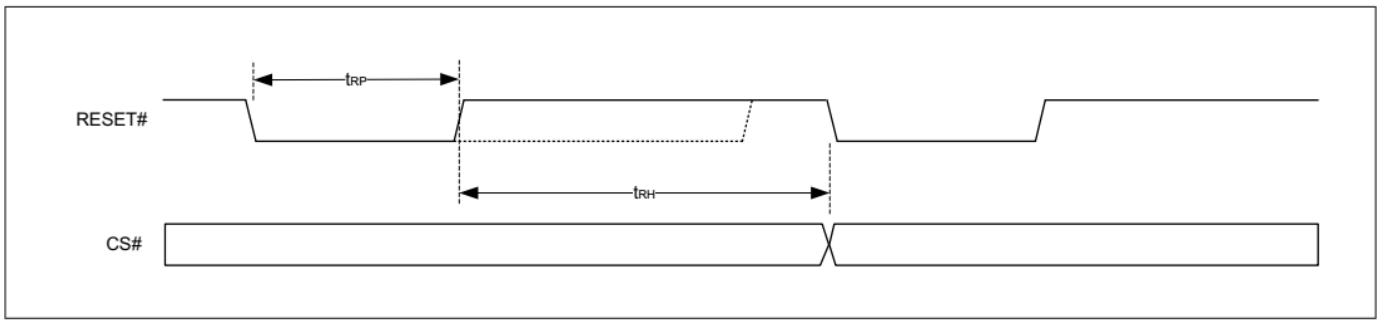

图 58　　使用 RESET# 输入的硬件复位（背对背硬件复位）

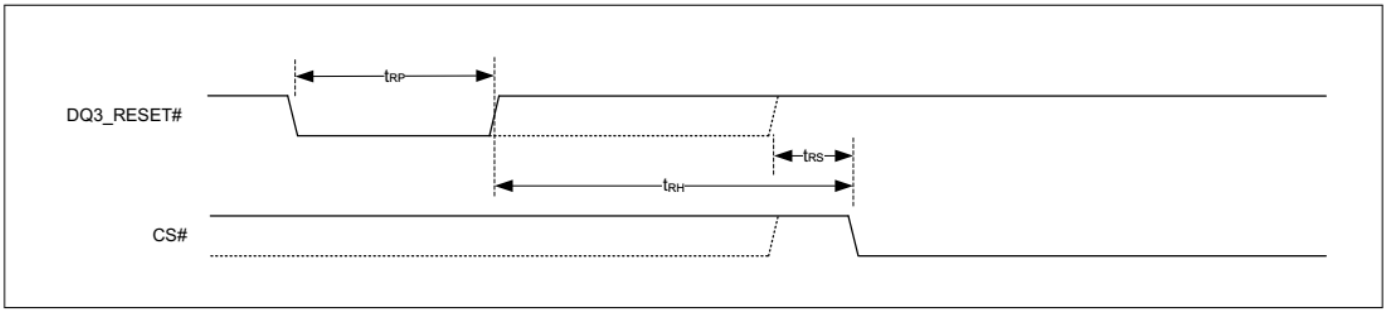

图 59　　当四线或 QPI 模式禁用且 DQ3_RESET# 启用时的硬件复位

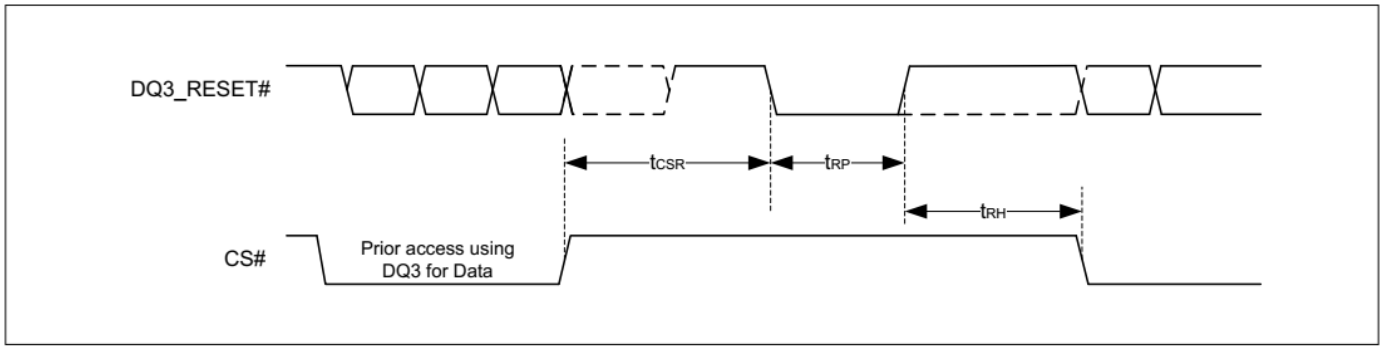

图 60　　当使用四线或 QPI 模式和 DQ3_RESET# 启用时的硬件复位

4.12.2　上电复位 (POR)

器件执行POR 过程，直到 V_{CC} 上升到最小 V_{CC}阈值以上，后经过t_{PU} 时间延迟 （见图 61 和 图 62)。上电期间 (t_{PU}) 器件不得被选通。因此，CS# 必须随 V_{CC} 同步上升。在 t_{PU} 结束之前，不得向器件发送任何命令传输。见表 90 的时序规范。

POR 期间会忽略 RESET#。如果 POR 期间 RESET# 为低电平，并在 t_{PU} 结束后保持低电平 ，则 CS# 必须保持高电平，直到RESET# 返回高电平后并保持 t_{RS}为止。

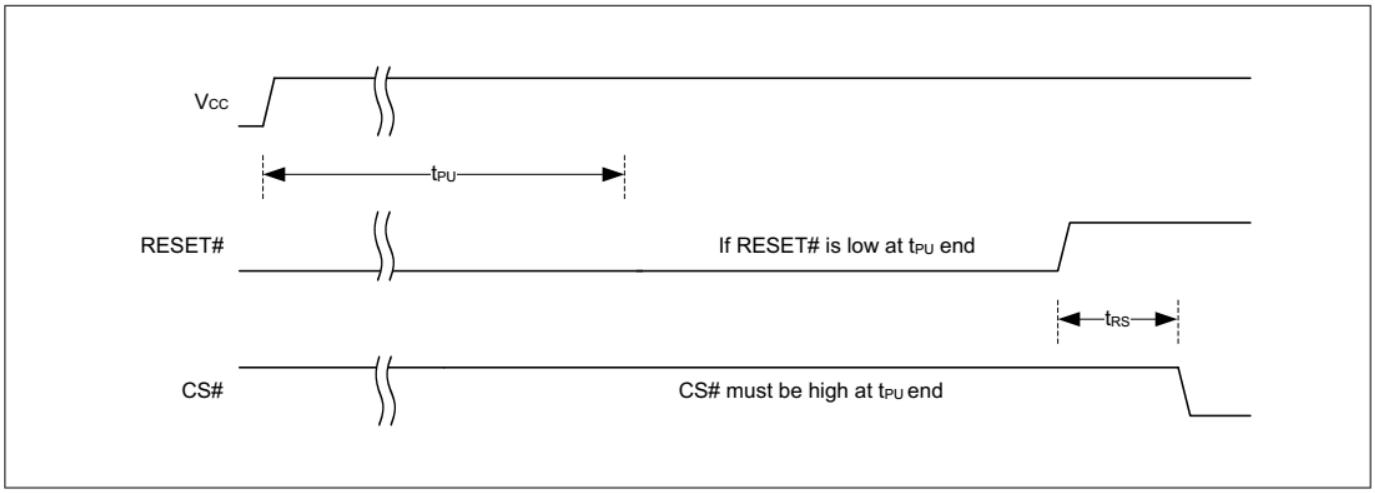

图 61　　POR 结束时复位低电平

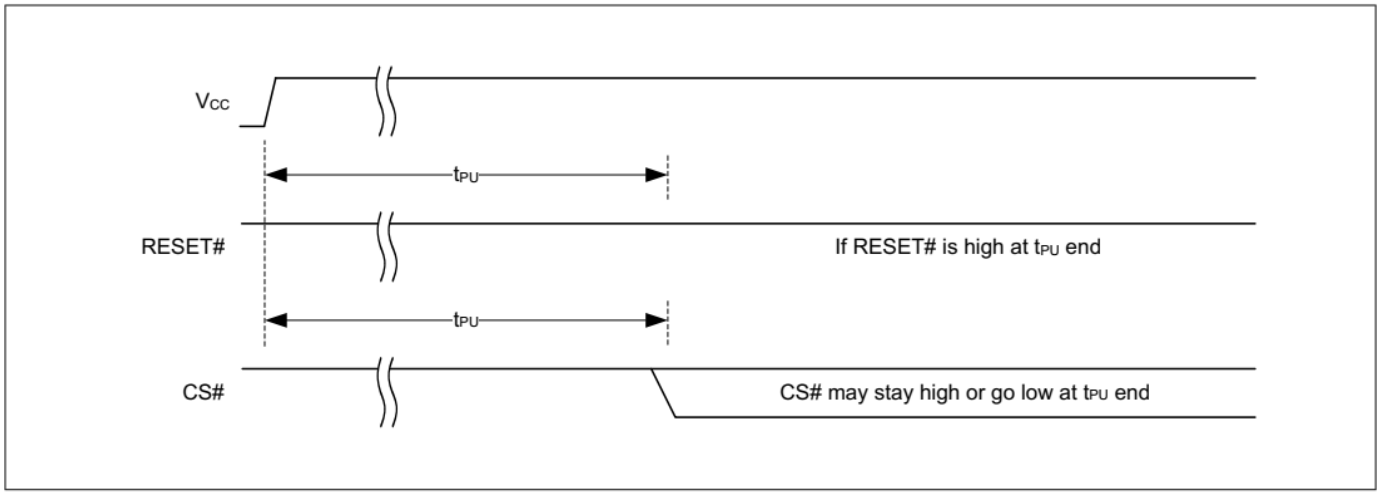

图 62　　POR 结束时复位高电平

4.12.3　JEDEC串行闪存式器件复位信令协议

JEDEC串行闪存式设备复位信令协议需要 CS# 和 DQ0 信号。 该复位方法定义了一个信令协议，使用现有信号来启动SPI闪存式器件硬件复位，独立于器件运行模式或封装引脚数量。

信令协议如图 63所示。见表 90定义的时序规范。JEDEC 串行闪存式设备复位信令协议步骤如下：

- CS# 驱动为低电平有效。
- CK 在高电平或低电平状态下均保持稳定。
- CS# 和 DQ0 均被驱动为低电平。
- CS# 被驱动为高电平（无效）。
- 重复以上四个步骤，每次交替DQ0的状态总共四次。
- 复位发生在第四个 CS# 周期完成后，并且它变为高电平（非活动）时。

在第四个 CS# 脉冲后，从设备触发其内部复位，器件终止任何正在进行的操作，使所有输出为高阻态，并忽略 t_{RESET} 期间的所有读/写命令传输。然后器件将处于待机状态。

该复位序列不适用于正常上电的情况，而仅适合在器件未对系统作出响应时使用。无论器件处于什么状态，此复位序列都可以运行。

因此， JEDEC串行闪存式器件复位信号协议对于不支持 RESET# 引脚的封装非常有用，可提供与硬件复位相同的行为。

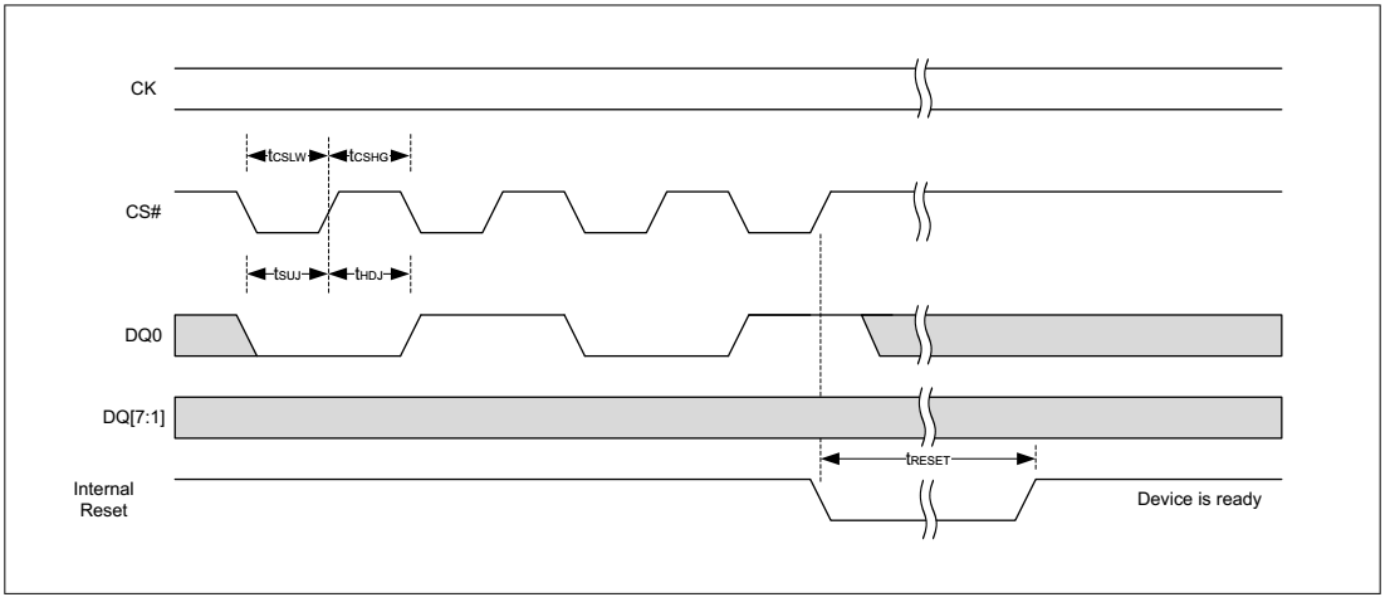

图 63　　JEDEC串行闪存式器件复位信令协议

4.12.4　软件复位

软件控制的复位命令传输通过从非易失性默认值（保护寄存器除外）重新加载至易失寄存器，将器件恢复到其初始上电状态。它还会终止嵌入式操作。当 CS# 在命令传输结束时变为高电平时，将执行复位命令传输 (SFRST_0_0)，并需要 t_{SR}时间来执行。见表 90 时序规范。

在复位命令传输 (SFRST_0_0) 之前需要立即执行复位使能 (SRSTE_0_0) 命令传输，以便软件复位执行两个命令传输的序列。 SRSTE_0_0 命令传输之后除 SFRST_0_0 以外的任何命令传输都将清除复位使能条件，并防止后面的 SFRST_0_0 命令传输被识别。

复位（SFRST_0_0）命令传输紧接着 SRSTE_0_0 命令传输，从而启动软件复位过程。 在软件复位期间，在器件的易失性和非易失性配置状态相同时，仅支持状态寄存器 1 的 RDSR1_0_0 和 RDARG_C_0 操作。如果配置状态在软件复位期间发生变化，则只能在软件复位时间过去后才可读取状态寄存器 1。

软件复位与 RESET# 的状态无关。如果 RESET# 为高电平或未连接，并且发出软件复位命令传输，则器件将执行软件复位。

传统软件复位 (SFRSL_0_0) 是启动软件复位过程的单一命令传输。 默认情况下，此指令是禁用的，但可以通过配置 CFR3V[0] = 1 来启用，以实现与英飞凌传统设备的软件兼容性。

4.12.4.1　软件复位相关寄存器和命令传输

表 43　　擦除相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
N/A	Software Reset Enable (SRSTE_0_0)	Software Reset Enable (SRSTE_0_0)

（表格续下页.....）

表 43 （续）擦除相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
	Software Reset (SFRST_0_0)	Software Reset (SFRST_0_0)
	Legacy Software Reset (SFRSL_0_0)	Legacy Software Reset (SFRSL_0_0)

4.12.5 复位行为

表 44 复位行为

Transaction/Register name	POR	Hardware reset and JEDEC serial flash reset signaling protocol	Software reset
Summary	• Device Reset • Status Bits Reset • All Volatile Registers Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations	• Device Reset • Status Bits Reset • All Volatile Registers Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations	• Device Reset • Status Bits Reset • Configuration Reload to Default • Volatile Protection Reset to Default • Nonvolatile Protection unchanged • Reset all Embedded operations
Interface Requirements	• All Inputs - Ignored • All Outputs - Tristated	• All Inputs - Ignored • All Outputs - Tristated	Transactions (SRSTE_0_0, SFRST_0_0)
Status Registers	Load from Nonvolatile Registers	Load from Nonvolatile Registers	Load from Nonvolatile Registers
Configuration Registers	Load from Nonvolatile Registers	Load from Nonvolatile Registers	Load from Nonvolatile Registers
Protection Registers	PPB Lock Register - Load based on ASPO[2:1]	PPB Lock Register - Load based on ASPO[2:1]	PPB Lock Register - No Change
	DYB Access Register - Load based on ASPO[4]	DYB Access Register - Load based on ASPO[4]	DYB Access Register - No Change
	Password Register - Load based on ASPO[2] and ASPO[0]	Password Register - Load based on ASPO[2] and ASPO[0]	Password Register - No Change
ECC Status Register	Load 0x00	Load 0x00	Load 0x00
Data Learning Pattern Register	Load from Nonvolatile Registers	Load from Nonvolatile Registers	No Change

（表格续下页.....）

表 44 （续）复位行为

Transaction/Register name	POR	Hardware reset and JEDEC serial flash reset signaling protocol	Software reset
AutoBoot Register	Load from Nonvolatile Registers	Load from Nonvolatile Registers	No Change
Data Integrity Check Register	Load 0x00	Load 0x00	Load 0x00
ECC Error Count Register	Load 0x00	Load 0x00	Load 0x00
Address Trap Register	Load 0x00	Load 0x00	Load 0x00
Infineon Endurance Flex architecture Register	Load from Nonvolatile Registers	Load from Nonvolatile Registers	No Change
I/O Mode	Load from Nonvolatile Registers	Load from Nonvolatile Registers	No Change
Memory/Register Erase in Progress	Not Applicable	Abort Erase	Abort Erase
Memory/Register Program in Progress	Not Applicable	Abort Program	Abort Program
Memory/Register Read in Progress	Not Applicable	Abort Read	Not Applicable

4.13 电源模式

4.13.1 有源电源和备用电源模式

当片选（CS）为低电平时，器件被启用并处于有效电源模式。当 CS 为高电平时，器件被禁用，但仍可能处于有效电源模式，直到所有编程、器件和写操作完成。然后器件进入待机功率模式，功率功耗降至 ISB。参见表 88 参数规格。

4.13.2 深度掉电（DPD）模式

虽然正常运行期间的待机电流相对较低，但通过 DPD 模式可以进一步降低待机电流。较低的功率消耗使得 DPD 模式特别适用于电池供电的应用。

4.13.2.1 进入 DPD 模式

器件可以通过两种方式进入 DPD 模式：

1. 使用命令传输进入 DPD 模式
2. 上电或复位后进入 DPD 模式

使用进入深度掉电模式命令传输进入 DPD 模式

通过发送进入深度掉电模式命令传输 (ENDPD_0_0) 然后等待 t_{ENTDPD} 延迟，即可使能 DPD 模式。在锁存指令字节后，必须将 CS# 引脚驱动为高电平。否则，将不会执行 DPD 命令传输。在 CS# 引脚驱动为高电平后，

在 t_{ENTDPD} 时间内进入掉电状态（参见表 90 时序规范），并且功耗将降至 IDPD（参见表 88 参数规范）。DPD 只能从空闲状态进入。仅当器件未执行嵌入式算法（如易失性状态寄存器 1、器件就绪/忙状态标志 (RDYBSY) 位清除为零 (STR1V[0] = RDYBSY = 0) 所示）时，才接受 DPD 命令传输。在 t_{ENDPD}时间内不允许向器件发送任何命令传输。

上电或复位后进入 DPD 模式

如果 DPDPOR 配置位为使能（CFR4NV[2] = 1），则在上电、硬件复位或JEDEC串口闪存式器件复位信令协议完成后，器件将处于 DPD 模式。在POR 或复位期间，CS# 应跟随VCC上施加的电压进入 DPD 模式，如图 64所示。在 t_{ENTDPD} 时间内不允许向器件发送任何命令传输。

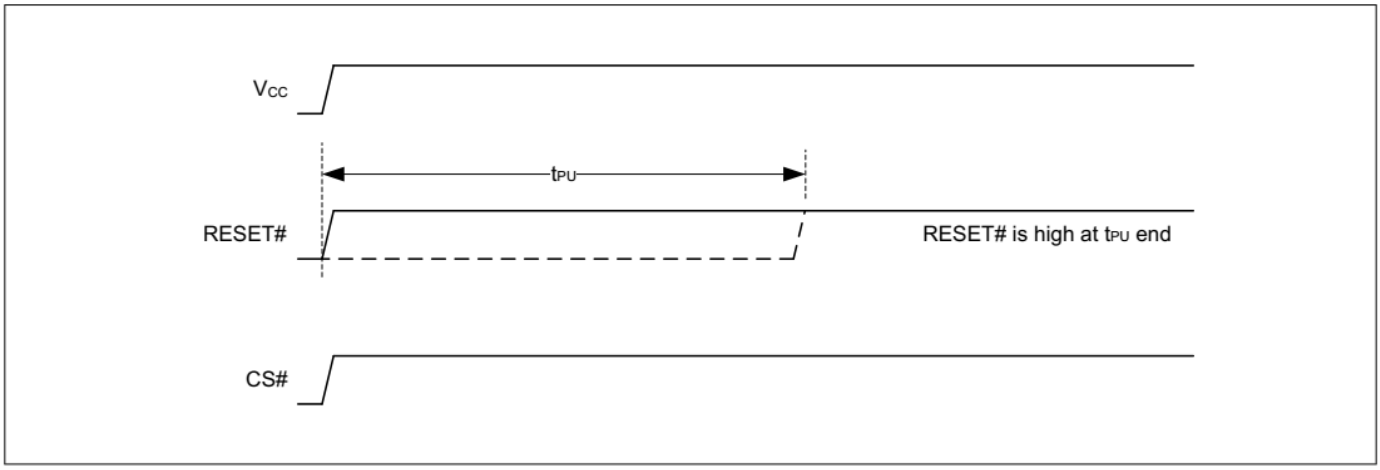

图 64　　上电或复位时进入 DPD 模式

4.13.2.2　退出 DPD 模式

器件离开 DPD 模式可通过以下方式之一：

硬件复位后退出 DPD 模式

当器件处于 DPD 且 CFR4NV[2] = 0 时，硬件复位会将器件返回到待机模式。

根据 CS# 脉冲退出 DPD 模式

器件在收到宽度为 t_{CSDPD} 的CS# 脉冲后退出 DPD。 CS# 应在脉冲后驱动为高电平。 DPD退出后，需要CS#上的高电平到低电平跳变来启动命令传输周期。退出 DPD 模式需要 t_{EXTDPD}时间。器件直到 t_{EXTDPD}之后才会响应。

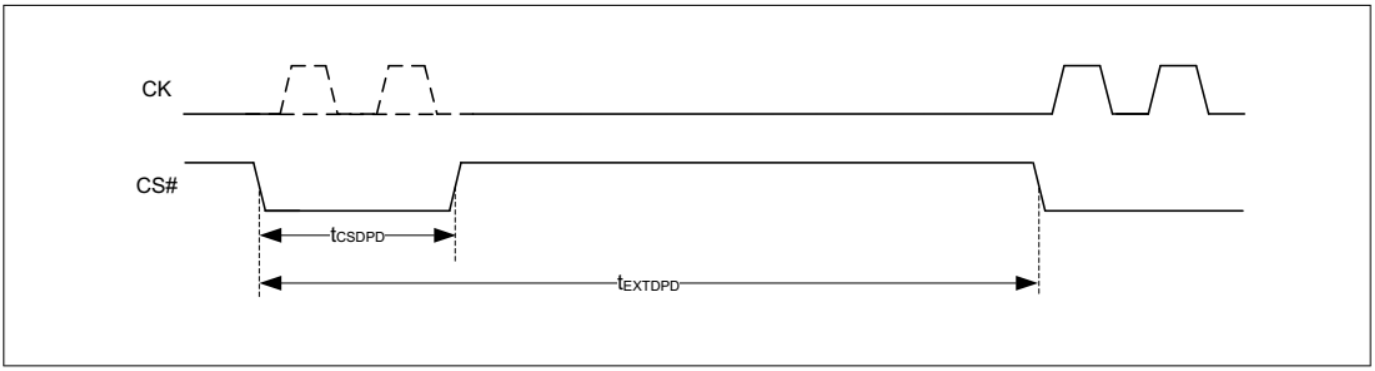

图 65　　退出DPD模式

器件在 DPD 期间保持其配置，这意味着器件退出 DPD 时的状态与进入 DPD 时的状态相同。ECC 状态、ECC 错误检测计数器、地址捕获和中断状态寄存器等寄存器将被清除。

4.13.2.3 DPD 相关寄存器和命令传输

表 45 擦除相关寄存器和命令传输

Related registers	Related SPI transactions (see Table 79)	Related quad SPI transactions (see Table 83)
Configuration Register 4 (CFR4N, CFR4V) (see Table 58)	Enter Deep Power Down Mode (ENDPD_0_0)	Enter Deep Power Down Mode (ENDPD_0_0)

4.14 上电和掉电

在 V_{CC} 达到如下正确值之前，一定不要在电压上升或掉电时选通该器件：

- V_{CC}（最小值）在电压上升时，然后再延迟 tPU
- V_{SS}在掉电时

4.14.1 上电

在 V_{CC} 上升到最低 V_{CC} 阈值之后， 器件将忽略所有事务，直到经过t_{PU} 时间延迟（见图 66)。但是，如果 V_{CC} 在 t_{PU} 期间返回到 V_{CC}(min) 以下， 则不能保证器件的正确运行。在 t_{PU} 结束之前，不应向器件发送任何命令传输。

器件在 t_{PU} 期间会消耗 IPOR 电流。上电完成（t_{PU}）后，WRPGEN 位将被复位，并且设备可以选择进入 DPD 模式或待机模式。配置寄存器 4（CFR4N[2]）中的 DPDPOR 位用于控制设备在 POR 完成后进入 DPD 模式还是待机模式（参见表 58）。如果启用 DPDPOR 位（CFR4N[2] = 1），设备在上电后将进入 DPD 模式。要使器件在 POR 后返回待机模式，需要执行硬件复位（RESET# 和 DQ3_RESET#）。

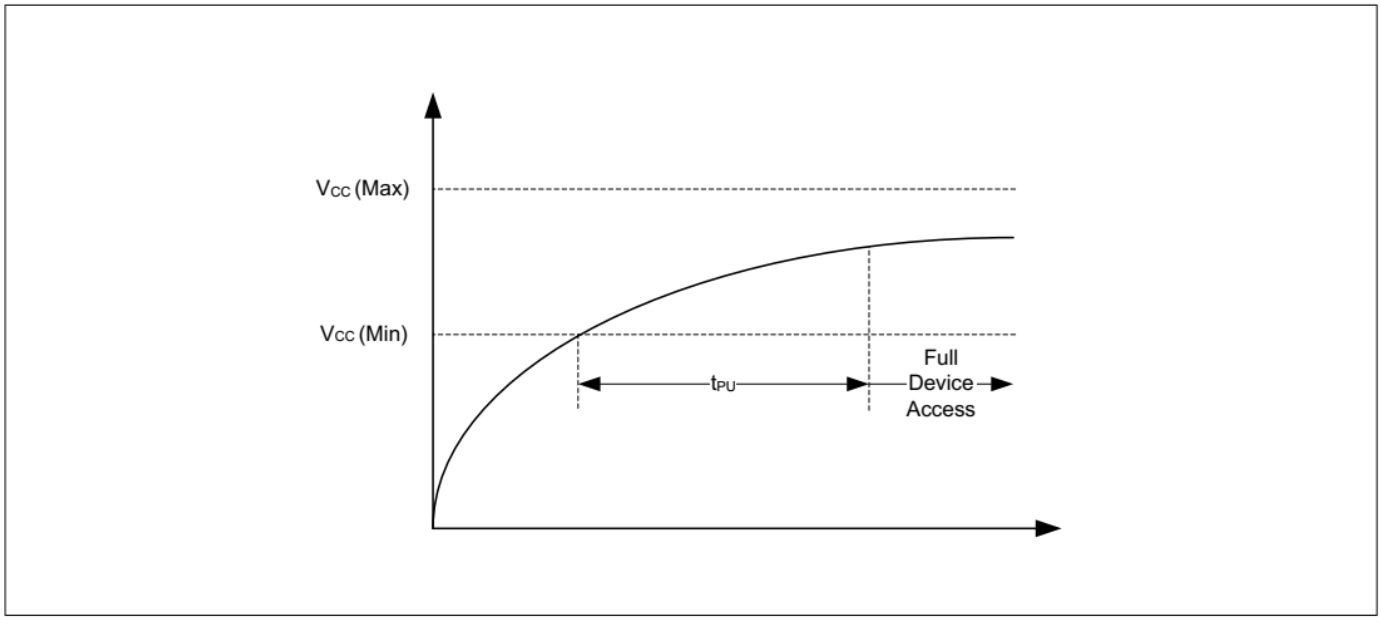

图 66 上电

4.14.2 掉电

在掉电或电压降至 V_{CC} （截止）以下时，电压必须降至 V_{CC} 以下（低电平）并持续 t_{PD} 时间，以使部件正确初始化（见 图 67)。如果在降压期间 V_{CC} 保持在 V_{CC} (截止)以上，则部件将保持初始化状态，并在 V_{CC} 再次高于V_{CC} (最小) 时正常工作。如果在上电后POR 未正确完成，则需要 RESET# 信号来重新启动 POR 过程。

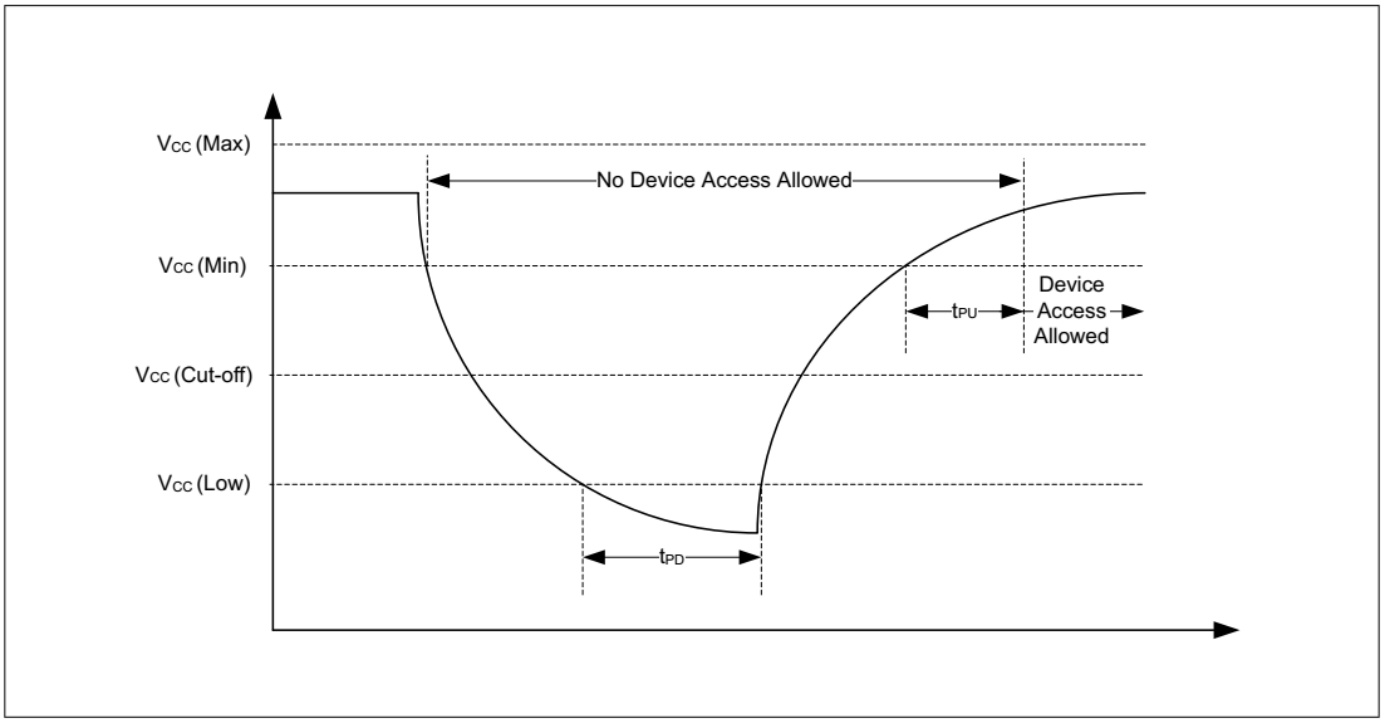

图 67 掉电或电压下降

5 寄存器

寄存器是一小组存储单元，用于配置和报告器件操作的状态。HL-T/HS-T 系列器件使用单独的非易失性和易失性存储组来实现不同的寄存器位类型，以实现传统版兼容性和新功能。每个寄存器都由一组易失性位和关联的非易失性位（如果需要持久性）组成。在上电、硬件复位或软件复位期间，寄存器非易失性位中的数据将传输到易失性位，以提供易失性位的默认状态。将新数据写入寄存器的非易失性位时，易失性位也会使用新数据进行更新。但是，将新数据写入易失性寄存器位时，非易失性位将保留旧数据。寄存器结构如图 68所示。

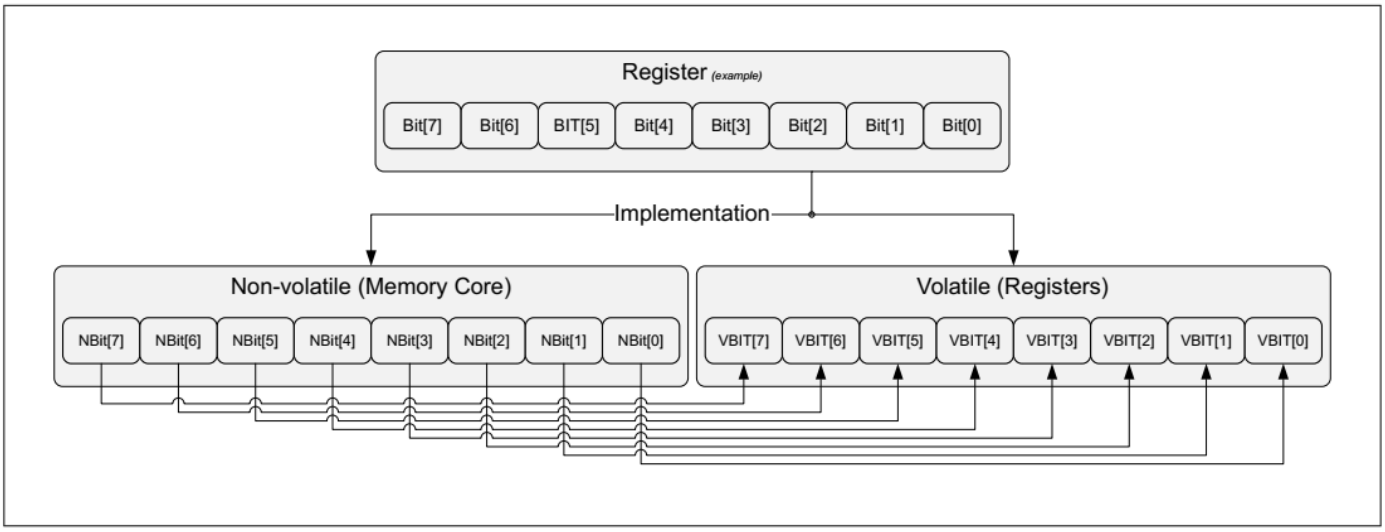

图 68　　寄存器结构

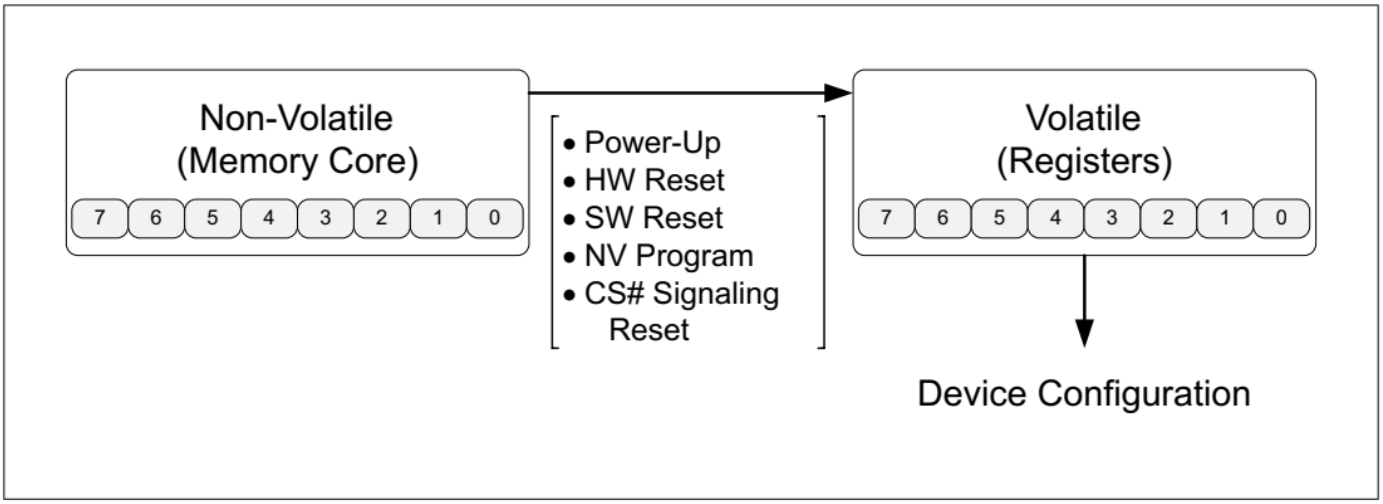

图 69　　寄存器组件内的数据移动

5.1 寄存器命名规则

表 46 寄存器位描述规则

Bit number	Name	Function	Read/Write	Factory default (binary)	Description
REGNAME#T[x] T = N, V, O Descending Order	–	–	Possible options: N/A - Not Applicable R - Readable Only R/W - Readable and Writable R/1 - Readable and One Time Programmable	Possible options: 0, 1	Format: Description of the Configuration bit 0 = Option '0' selection of the Bit 1 = Option '1' selection of the Bit Dependency: Is this Bit part of a function which requires multiple bits for implementation?

5.2 状态寄存器 1 (STR1x)

状态寄存器 1 包含状态位和控制位。 表 47描述了所支持的状态寄存器 1 类型的功能。

表 47 状态寄存器 1 [1)]

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR1N[7] STR1V[7]	STCFWR	Status Register 1 and Configuration Register 1, 2, 3, 4 Protection Selection against write (erase/program)	N->R/W V->R/W	0	Description: The STCFWR bit selects enabling and disabling writes (erase/program) to Status Register 1 and configuration registers 1, 2, 3, 4 based on WP# (Write Protect Pin) in Single SPI mode. When STCFWR bit is enabled with WP# LOW, any transaction that can change status or configuration registers is ignored, effectively locking the state of the device. If WP#/DQ[2] is HIGH (irrespective of STCFWR), Status and Configuration Registers can be changed. Selection options: 1 = WP# based protection is enabled 0 = WP# based protection is disabled Dependency: N/A

（表格续下页……）

表 47 （续）状态寄存器 1 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR1V[6]	PRGERR	Programming Error Status Flag	V -> R	0	Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a '1', it indicates that there was an error in the last programming operation. PRGERR bit is also set when a program operation is attempted within a protected memory region. When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/ software reset (see Table 48). ***Note**: The device will only go to standby mode once the PRGERR flag is cleared.* Selection options: 0 = Last programming operation was successful 1 = Last programming operation was unsuccessful Dependency: N/A
STR1V[5]	ERSERR	Erasing Error Status Flag	V -> R	0	Description: The ERSERR bit indicates erase operation success or failure. When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when a erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/software reset (see Table 49). Note The device will only go to standby mode once the ERSERR flag is cleared. Selection options: 0 = Last erase operation was successful 1 = Last erase operation was unsuccessful Dependency: N/A

（表格续下页……）

表 47 （续）状态寄存器 1 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR1N[4:2] STR1V[4:2]	LBPROT[2:0]	Legacy Block Protection based Memory Array size selection	If PLPROT = 0 N -> R/W V -> R/W If PLPROT = 1 N -> R V -> R	000	Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 1/64, 1/4, 1/2, etc. or bottom 1/64, 1/4, 1/2, etc., or up to the entire array is protected. Note If PLPROT bit - Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture (CFR1x[4]) is set to a '1', the LBPROT[2:0] bits cannot be erased or programmed. Selection options: 000 = Protection is disabled 001 = 1/64th of the (top/bottom) array protection is enabled 010 = 1/32nd of the (top/bottom) array protection is enabled ….. 111 = All sectors are protected Dependency: TBPROT (CFR1x[5])

（表格续下页……）

表 47 （续）状态寄存器 1 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	V -> R	0	Description: The WRPGEN bit must be set to ‘1’ to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable and Write Enable Volatile transactions set the WRPGEN bit to ‘1’ to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a ‘0’ to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to ‘0’ at the end of any successful program, erase or register write operation. After a power down/power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to ‘0’. Selection options: 0 = Program, erase or register write is disabled 1 = Program, erase or register write is enabled Dependency: N/A

（表格续下页……）

表 47 （续）状态寄存器 1 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	V -> R	0	Description: The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions. ***Note**: The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags transaction must be executed to return the device to standby mode.* Selection options: 0 = Device is in standby mode ready to receive new operation transactions 1 = Device is busy and unable to receive new operation transactions Dependency: N/A

1) POR、硬件复位、软件复位、DPD 退出和JEDEC串行闪存式器件复位信令协议期间的STR1x 值无效。

表 48 PRGERR 汇总

Error flag	Symbol	Conditions
Program Error	PRGERR	Bits cannot be programmed ‘1’ to ‘0’
		Trying to program in a protected region
		If ASP0[2] or ASP0[1] is 0, any nonvolatile register write attempting to change the value of CFR1N[6:2]/CFR1V[6:2]
		After the Password Protection Mode is selected and ASP Password Register update transaction executed
		SafeBoot Failure
		Configuration Failure

表 49 ERSERR 汇总

Error flag	Symbol	Conditions
Erase Error	ERSERR	Sector Device Erase - All bits cannot be erased to ‘1’s
		Trying to erase a protected region
		Register Erase - All bits cannot be erased to ‘1’s during Erase portion of Register Write
		SafeBoot Failure

5.3 状态寄存器 2 (STR2x)

状态寄存器 2 提供器件操作状态。表50描述了支持的状态寄存器2 类型的功能。

表 50 状态寄存器 2 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR2V[7:5]	RESRVD	Reserved for future use	V -> R	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
STR2V[4]	DICRCS	Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag	V -> R	0	Description: The DICRCS bit is used to determine when the device is in Memory Array Data Integrity Cyclic Redundancy Check suspend mode. Selection options: 0 = Memory Array Data Integrity Cyclic Redundancy Check is not in suspend mode 1 = Memory Array Data Integrity Cyclic Redundancy Check is in suspend mode Dependency: N/A

（表格续下页……）

表 50 （续）状态寄存器 2 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR2V[3]	DICRCA	Memory Array Data Integrity Cyclic Redundancy Check Abort Status Flag	V -> R	0	Description: The DICRCA bit indicates that the Memory Array Data Integrity Cyclic Redundancy Check calculation operation was aborted. The abort condition is based on ending address (ENDADD) and starting address (STRADD) relationship. If ENDADD < STRADD + 3, then DICRCA will be set and the device will return to the Standby state. DICRCA flag gets cleared at the next Data Integrity Cyclic Redundancy Check calculation operation when ENDADD ≥ STRADD + 3. Selection options: 0 = Memory Array Data Integrity Cyclic Redundancy Check calculation Is not aborted 1 = Memory Array Data Integrity Cyclic Redundancy Check calculation is aborted Dependency: N/A
STR2V[2]	SESTAT	Sector Erase Success/Failure Status Flag	V -> R	0	Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction must be executed prior to reading SESTAT bit which specifies the sector address. Selection options: 1 = Addressed sector was erased successfully 0 = Addressed sector was not erased successfully Dependency: N/A
STR2V[1]	ERASES	Erase operation Suspend Status Flag	V -> R	0	Description: The ERASES bit is used to indicate if the Erase operation is suspended. Selection options: 0 = Erase operation is not in suspend mode 1 = Erase operation is in suspend mode Dependency: N/A

（表格续下页……）

表 50 （续）状态寄存器 2 [1)]

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
STR2V[0]	PROGMS	Program operation Suspend Status Flag	V -> R	0	Description: The PROGMS bit is used to indicate if the Program operation is suspended. Selection options: 0 = Program operation is not in suspend mode 1 = Program operation is in suspend mode Dependency: N/A

1) POR、硬件复位、软件复位、DPD 退出和JEDEC串行闪存式器件复位信号协议期间的 STR2x 值无效。仅当 STR1V[0] / RDYBSY = 0 时，STR2x 位才有效。

5.4 配置寄存器 1 (CFR1x)

配置寄存器 1 控制接口和数据保护功能。

表 51 配置寄存器 1

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR1N[7] CFR1V[7]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR1N[6] CFR1V[6]	SP4KBS	Split 4KB Sectors selection between top and bottom address space	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The SP4KBS bit selects whether the 4 KB sectors are grouped together or evenly split between High and LOW address ranges (see Table 52). Selection options: 0 = 4 KB Sectors are grouped together 1 = 4 KB Sectors are split between High and Low Addresses Dependency: TB4KBS(CFR1N[2])

（表格续下页……）

表 51 （续）配置寄存器 1

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR1N[5] CFR1V[5]	TBPROT	Top or Bottom Protection selection for Legacy Protection Mode	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range. The bit also selects a memory address range (lowest or highest) to remain readable is available for reading during Read Password Protection mode even before a successful Password entry is completed (see Table 53). Selection options: 0 = Legacy Protection is applicable in the top half of the address range 1 = Legacy Protection is applicable in the bottom half of the address range Dependency: LBPROT[2:0] (STR1x[3:1])

（表格续下页……）

表 51 （续）配置寄存器 1

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR1N[4] CFR1V[4]	PLPROT	Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture	N -> R/1 V -> R	0	Description: The PLPROT bit permanently protects the Legacy Block Protection and 4KB Sector location. It thereby permanently protects the memory array protection scheme and sector architecture (see Table 53). ***Note**: PLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase. It is recommended to configure these bits before configuring the PLPROT bit.* Selection options: 0 = Legacy Block Protection and 4KB Sector Location are not protected 1 = Legacy Block Protection and 4KB Sector Location are protected Dependency: N/A
CFR1N[3] CFR1V[3]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

（表格续下页……）

表 51　　（续）配置寄存器 1

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR1N[2] CFR1V[2]	TB4KBS	Top or Bottom Address Range selection for 4KB Sector Block	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The TB4KBS bit defines the logical address location of the 4KB sector block. The 4KB sector block replaces the fitting portion of the highest or lowest address sector (see Table 52). Selection options: 0 = 4 KB Sector Block is in the bottom of the memory address space 1 = 4 KB Sector Block is in the top of the memory address space Dependency: SP4KBS (CFR1x[6])
CFR1N[1] CFR1V[1]	QUADIT	Quad SPI Interface Selection - I/O width set to 4 bits (1-1-4, 1-4-4)	N -> R/W V -> R/W	0	Description: The QUADIT bit selects the I/O width of the device. When configured to 4-bits (QUAD), WP# becomes DQ2 and DQ3_RESET# becomes DQ3. The QUADIT transactions require Opcode sent on a single I/O, Address either on a single or all four I/Os and Data always sent on all four I/Os. Selection options: 0 = Data Width set to 1 or 2 bits wide (1x - Single, 2x - Dual) 1 = Data Width set to 4 wide (4x - Quad) Dependency: N/A

（表格续下页……）

表 51 （续）配置寄存器 1

Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR1N[0] CFR1V[0]	TLPROT	Temporary Locking selection of Legacy Block Protection and Sector Architecture	N -> R V -> R/W	0	Description: The TLPROT bit temporarily protects the Legacy Block Protection and 4 KB Sector location. Upon power-up or a hardware reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme and sector architecture from any changes. ***Note**: TLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase.* Selection options: 0 = Legacy Block Protection and 4 KB Sector Location are not protected 1 = Legacy Block Protection and 4 KB Sector Location are temporarily protected Dependency: N/A

表 52 4 KB参数扇区位置选择

SP4KBS	TB4KBS	4 KB location
0	0	4 KB physical sectors at bottom (Low address)
0	1	4 KB physical sectors at top, (High address)
1	X	4 KB Parameter sectors are split between top (High Address) and bottom (Low Address)

表 53 PLPROT 和 TLPROT 保护

PLPROT	TLPROT	Array protection and 4K sector
0	0	Unprotected (Unlocked)
1	x	TBPROT, LBPROTx, SP4KBS, TB4KBS - Permanently Protected (Locked)
0	1	TBPROT, LBPROTx, SP4KBS, TB4KBS, Protected (Locked) till next Power-down

5.5 配置寄存器 2 (CFR2x)

配置寄存器 2 控制接口、存储器读取延迟和地址字节长度选择。

表 54 配置寄存器 2

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR2N[7] CFR2V[7]	ADRBYT	Address Byte Length selection between 3 or 4 bytes for Instructions	N -> R/W V -> R/W	0	Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes. Selection options: 0 = Instructions will use 3 Bytes for address1 = Instructions will use 4 Bytes for address Dependency: N/A
CFR2N[6] CFR2V[6]	QPI-IT	QPI Interface & Protocol Selection - I/O width set to 4 bits (4-4-4)	N -> R/W V -> R/W	0	Description: The QPI-IT bit selects the I/O width of the device to be 4-bits wide. When configured to 4-bits (QPI-IT, QUADIT), WP# becomes DQ2 and DQ3_RESET# becomes DQ3. The QPI-IT transactions require Opcode, Address and Data always sent on all four I/Os. Selection options: 0 = Data Width set to 1 or 2 bits wide (1x - Single, 2x - Dual) - Legacy Protocol 1 = Data Width set to 4 wide (4x - Quad) - QPI Protocol Dependency: N/A

（表格续下页……）

表 54　　（续）配置寄存器 2

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR2N[5] CFR2V[5]	DQ3RST	DQ3 and RESET Selection for DQ3 - Multiplexed operation on I/O #3	N -> R/W V -> R/W	0	Description: The DQ3RST bit controls the RESET# behavior on DQ3 signal. When enabled, a LOW on DQ3 will perform a hardware reset while CS# is HIGH. This multiplexed functionality on DQ3 is only available when QUADIT or QPI-IT interface modes are enabled. Disabling QUADIT or QPI-IT modes makes DQ3 a dedicated RESET# pin. Selection options: 0 = DQ3 has no multiplexed RESET# function 1 = DQ3 performs a hardware reset when LOW provided CS# is HIGH Dependency: N/A
CFR2N[4] CFR2V[4]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR2N[3:0] CFR2V[3:0]	MEMLAT[3:0]	Memory Array Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	1000	Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and nonvolatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see Table 55). Selection options: 0000 = 0 Latency Cycle Selection based on transaction opcodes ….. 1111 = 15 Latency Cycles Selection based on transaction opcodes Dependency: N/A

表 55 延迟编码（周期）与频率 [1], [2], [3], [4]

Latency code/ cycles	Read transaction maximum frequency (MHz)					
	RDAY2_C_0 (1-1-1) **RDSSR_C_0 (1-1-1)** **RDECC_C_0 (1-1-1)** **RDECC_4_0 (1-1-1)** **RDARG_C_0 (1-1-1)** [5] **RDAY4_C_0 (1-1-4)** **RDAY4_4_0 (1-1-4)** **RDPPB_C_0 (1-1-1)** **RDPPB_4_0 (1-1-1)**	**RDAY2_4_0 (1-1-1)**	**RDAY3_C_0 (1-2-2)** **RDAY3_4_0 (1-2-2)**	**RDAY2_4_0 (4-4-4)** **RDAY5_4_0 (4-4-4)** **RDAY5_C_0 (4-4-4)** **RDAY5_C_0 (1-4-4)** **RDAY5_4_0 (1-4-4)** **RDPPB_C_0 (4-4-4)** **RDPPB_4_0 (4-4-4)**	**RDSSR_C_0 (4-4-4)** [6] **RDARG_C_0 (4-4-4)** [5] **RDECC_C_0 (4-4-4)** **RDECC_4_0 (4-4-4)**	**RDAY7_C_0 (1-4-4)** **RDAY7_4_0 (1-4-4)** **RDAY7_C_0 (4-4-4)** **RDAY7_4_0 (4-4-4)**
	Mode Cycle = 0	**Mode Cycle = 8**	**Mode Cycle = 4**	**Mode Cycle = 2**	**Mode Cycle = 0**	**Mode Cycle = 1**
0	50	156	81	43	18	N/A
1	68	166	93	56	31	N/A
2	81	166	106	68	43	43
3	93	166	118	81	56	56
4	106	166	131	93	68	68
5	118	166	143	106	81	81
6	131	166	156	118	93	93
7	143	166	166	131	106	102
8 (Default)	156	166	166	143	118	102
9	166	166	166	156	131	102
10	166	166	166	166	143	102
11	166	166	166	166	156	102
12	166	166	166	166	166	102
13	166	166	166	166	166	102
14	166	166	166	166	166	102
15	166	166	166	166	166	102

1) 使用 ECC 错误报告机制时，读取的输出数据必须至少为 2 个字节才能正确进行 ECC 报告。
2) 该系列器件不支持 CK 频率 > 166 MHz的SDR或 > 102 MHz的DDR。
3) 快速读取 4 字节地址、QPI、双路 I/O、四线 I/O、QPI、DDR 四线 I/O 和 DDR QPI，协议包括地址后的连续读取模式位。这些位的时钟周期不计入表中所示的延时周期的一部分。例如，传统的四线 I/O 命令传输在地址之后有两个连续读取模式周期。因此，没有额外读取延迟的传统四线 I/O 命令传输仅支持表中所示的频率，以实现 0 周期的读取延迟。通过增加可变读

取延迟，可以增加四线 I/O 命令传输的频率，以允许操作达到最高支持 166MHz 频率。
4) 读取 SFDP 命令传输始终具有 8 个延迟周期，并且不同接口的最大频率与 8 个延迟周期相关。读取唯一 ID 有 32 个周期的延迟。
5) 读取任何寄存器命令传输使用这些延迟周期来读取非易失性寄存器。
6) 安全区域读取（4-4-4）延迟周期 > 0。

5.6 配置寄存器 3 (CFR3x)

配置寄存器 3 控制命令传输行为。

表 56 配置寄存器 3

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR3N[7:6] CFR3V[7:6]	VRGLAT[1:0]	Volatile Register Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	00	Description: The VRGLAT[1:0] bits control the read latency (dummy cycles) delay in all variable latency register read transactions. VRGLAT[1:0] selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see Table 57). Selection options: 00, 01, 10, 11 Latency Cycles Selection based on transaction opcodes Dependency: N/A
CFR3N[5] CFR3V[5]	BLKCHK	Blank Check selection during Erase operation for better endurance	N -> R/W V -> R/W	0	Description: When this feature is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally. Selection options: 0 = Blank Check is disabled before executing an erase operation 1 = Blank Check evaluation is enabled before executing an erase operation Dependency: N/A

（表格续下页……）

表 56　　（续）配置寄存器 3

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR3N[4] CFR3V[4]	PGMBUF	Program Buffer Size selection	N -> R/W V -> R/W	0	Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time. ***Note**: If programming data exceeds the program buffer size, data gets wrapped.* Selection options: 0 = 256 Byte Write Buffer Size 1 = 512 Byte Write Buffer Size Dependency: N/A
CFR3N[3] CFR3V[3]	UNHYSA	Uniform or Hybrid Sector Architecture selection	N -> R/W V -> R	0	Description: The UNHYSA bit selects between uniform (all 256 KB sectors) or hybrid (4 KB sectors and 256 KB sectors) sector architecture. If hybrid sector architecture is selected, 4 KB sector block is made part of the main flash array address map. The 4 KB sector block can overlay at either the highest or the lowest address range of the device. If uniform sector architecture is selected, 4 KB sector block is removed from the address map and all sectors are of uniform size. ***Note**: Hybrid sector architecture also enables 4 KB Sector Erase transaction (20 h). Otherwise, 4 KB Sector Erase transaction, if issued, is ignored by the device.* Selection options: 0 = Hybrid Sector Architecture (combination of 4 KB sectors and 256 KB sectors) 1 = Uniform Sector Architecture (all 256 KB sectors) Dependency: SP4KBS(CFR1N[6]), TB4KBS(CFR1N[2])

（表格续下页……）

表 56　　（续）配置寄存器 3

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR3N[2] CFR3V[2]	CLSRSM	Clear Status or Resume transaction 30 h selection	N -> R/W V -> R/W	0	Description: The CLSRSM bit selects how the 30 h transaction is used in the device. CLRRSM controls whether 30 h transaction is used as clear status transaction or as an alternate Program/Erase/Data Integrity Check resume transaction. Selection options: 0 = Clear Status Register transaction 1 = Program/Erase/Data Integrity Check Resume transaction Dependency: N/A
CFR3N[1] CFR3V[1]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR3N[0] CFR3V[0]	LSFRST	Legacy Software Reset transaction F0h selection	N -> R/W V -> R/W	0	Description: The LSFRST bit selects the software reset transaction. It allows the legacy F0h single transaction for software reset. Selection options: 0 = Legacy Software Reset is disabled 1 = Legacy Software Reset is enabled Dependency: N/A

表 57 寄存器延迟代码（周期）与频率[1), 2)]

Latency code	Fast read registers (No address) RDSR1_0_0 (1-1-1) RDSR1_0_0 (4-4-4) RDSR2_0_0 (1-1-1) RDCR1_0_0 (1-1-1) RDDLP_0_0 (1-1-1) RDIDN_0_0 (1-1-1) RDIDN_0_0 (4-4-4) RDPLB_0_0 (1-1-1) RDQID_0_0 (1-4-4, 4-4-4)		Regular read registers (No address) RDSR2_0_0 (4-4-4) RDCR1_0_0 (4-4-4) RDDLP_0_0 (4-4-4) RDPLB_0_0 (4-4-4)		Regular read registers (With address) RDDYB_C_0 (1-1-1) (4-4-4) RDDYB_4_0 (1-1-1) (4-4-4) RDARG_C_0[3)] (1-1-1) (4-4-4)	
	Frequency	Cycles	Frequency	Cycles	Frequency	Cycles
00 (Default)	50 MHz	0	50 MHz	0	50 MHz	0
01	133 MHz	0	133 MHz	0	133 MHz	1
10	133 MHz	1	133 MHz	1	133 MHz	1
11	166 MHz	2	166 MHz	2	166 MHz	2

1) 该系列器件不支持 CK 频率 > 166 MHz的SDR或 102 MHz的DDR。
2) 读取 SFDP 命令传输始终具有 8 个延迟周期，并且不同接口的最大频率与 8 个延迟周期相关。读取唯一 ID 有 32 个周期的延迟。
3) 读取任何寄存器命令传输使用这些延迟周期来读取易失性寄存器。

5.7 配置寄存器 4 (CFR4x)

配置寄存器4控制主要的闪存式存储器读取命令传输突发回卷行为和输出驱动阻抗。

表 58　　配置寄存器 4

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR4N[7:5] CFR4V[7:5]	IOIMPD[2:0]	I/O Driver Output Impedance selection	N -> R/W V -> R/W	000	Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements. Selection options: 000 = 45 Ω (Factory Default) 001 = 120 Ω 010 = 90 Ω 011 = 60 Ω 100 = 45 Ω 101 = 30 Ω 110 = 20 Ω 111 = 15 Ω Dependency: N/A
CFR4N[4] CFR4V[4]	RBSTWP	Read Burst Wrap Enable selection	N -> R/W V -> R/W	0	Description: The RBSTWP bit selects the read burst wrap feature. It allows the device to enter and exit burst wrapped read mode during normal operation. The wrap length is selected by RBSTWL[1:0] bits. Selection options: 0 = Read Wrapped Burst disabled 1 = Read Wrapped Burst enabled Dependency: RBSTWL[1:0] (CFR4x[1:0])

（表格续下页……）

表 58　　（续）配置寄存器 4

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR4N[3] CFR4V[3]	ECC12S	Error Correction Code (ECC) 1-bit or 1-bit/2-bit error correction selection	N -> R/W V -> R/W	1	Description: The ECC12S bit selects between 1-bit ECC error detection/ correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. This configuration option affects Address Trap Register and ECC Counter Register functionalities as well. The host needs to erase and reprogram the data in the SEMPER™ Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa). Selection options: 0 = 1-bit ECC Error Detection/Correction 1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection Dependency: N/A
CFR4N[2] CFR4V[2]	DPDPOR	Deep Power Down power saving mode entry selection upon POR	N -> R/W V -> R	0	Description: The DPDPOR bit selects if the device will be in either Deep Power Down (DPD) mode or the Standby mode after the completion of POR. If enabled, DPDPOR configures the device to start in DPD mode to reduce current consumption until the device is needed. If the device is in DPD, a pulse on CS# or a Hardware reset will return the device to Standby mode. Selection options: 0 = Standby mode is entered upon the completion of POR 1 = Deep Power Down Power mode is entered upon the completion of POR Dependency: N/A

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表 58 （续）配置寄存器 4

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR4N[1:0] CFR4V[1:0]	RBSTWL[1:0]	Read Burst Wrap Length selection	N -> R/W V -> R/W	00	Description: The RBSTWL[1:0] bits select the read burst wrap length and alignment during normal operation. It selects the fixed length/aligned group of 8-, 16-, 32-, or 64-bytes (see Table 59). Selection options: 00 = 8 Bytes Wrap length 01 = 16 Bytes Wrap length 10 = 32 Bytes Wrap length 11 = 64 Bytes Wrap length Dependency: RBSTWP (CFR4x[4])

表 59 输出数据回卷序列

Wrap boundary (Bytes)	Start address (Hex)	Address sequence (Hex)
Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18.
8	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02.
8	XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01.
16	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03.
16	XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E.
32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F.
32	XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00.
64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F 00, 01, 02.
64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D.

5.8 存储阵列数据完整性校验 CRC（循环冗余校验）寄存器 (DCRV)

存储阵列数据完整性检查CRC（循环冗余校验）寄存器（DCRV）存储对指定起始地址和结束地址之间包含的数据进行CRC（循环冗余校验）计算的结果。

表 60 存储阵列数据完整性校验 CRC（循环冗余校验）寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
DCRV[31:0]	DTCRCV[31:0]	Memory Array Data CRC Checksum Value	V -> R	0x00000000	Description: The DTCRCV[31:0 bits store the checksum value of the CRC process on the memory array data contained within the starting address and the ending address. Selection options: Checksum Value Dependency: N/A

5.9 ECC 状态寄存器 (ECSV)

ECC状态寄存器（ECSV）包含对单位数据执行的任何纠错操作的ECC状态，该数据的字节在上次读取期间被寻址。

注释： *单位数据定义为计算ECC字节数。HL-T/HS-T系列设备有16字节（128位）单位数据。*

表 61 ECC状态寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ECSV[7:5]	RESRVD	Reserved for future use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

（表格续下页.....）

表 61 （续）ECC 状态寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ECSV[4]	ECC2BT	ECC Error 2-bit Error Detection Flag	V -> R	0	Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT. ***Note**: ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.* ***Note**: ECC1BT is not valid if ECC2BT status flag is set.* Selection options: 0 = No 2-bit ECC Error was detected in the data unit (16 bytes)1 = 2-bit ECC Error was detected in the data unit (16 bytes) Dependency: CFR4x[3]
ECSV[3]	ECC1BT	ECC Error 1-bit Error Detection and Correction Flag	V -> R	0	Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT. ***Note**: ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.* Selection options: 0 = No 1-bit ECC Error was detected in the data unit (16 bytes)1 = 1-bit ECC Error was detected in the data unit (16 bytes) Dependency: N/A

（表格续下页……）

表 61　　（续）ECC 状态寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ECSV[2:0]	RESRVD	Reserved for future use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

5.10　　ECC 地址捕获寄存器 (EATV)

ECC 地址捕获寄存器 (EATV) 用于存储读操作期间发生 1 位/2 位错误或仅发生 1 位错误的ECC单位数据的地址。它存储自上次清除ECC命令传输以来在存储器读取操作期间捕获的第一个ECC错误的ECC单位数据地址。

表 62 ECC 地址捕获寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
EATV[31:0]	ECCATP[31:0]	ECC 1-bit and 2-bit Error Address Trap Register	V -> R	0x00000000	Description: The Address Trap Register (ECCATP[31:0]) stores the ECC unit data address where a 1-Bit/2-Bit error occurred during a read operation. ECCATP[31:0] stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC Status Register transaction (CLECC_0_0). ***Note**: ECCATP[31:0] is only updated during Read Instruction.* ***Note**: Mask non-valid upper ECCATP address bits from ECC unit address.* ***Note**: Clear ECC Status Register transaction (CLECC_0_0), POR or Hardware/ Software reset clears the EATV[31:0] to 0x00000000.* Selection options: ECC Error Data Unit Address Dependency: N/A

5.11 ECC 错误检测计数寄存器 (ECTV)

ECC 错误检测计数寄存器 (ECTV) 存储自上次 POR 或硬件/软件复位以来读取操作期间发生的 1 位/2 位或仅 1 位 ECC 错误的数量。

表 63 ECC 计数寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
ECTV[15:0]	ECCCNT[15:0]	ECC 1-bit and 2-bit Error Count Register	V -> R	0x0000	Description: The ECCCNT[15:0] stores the number of 1-bit/2-bit ECC errors occurred during read operations since the last POR or hardware/software reset. ***Note**: ECCCNT[15:0] is only updated during Read Instruction.* ***Note**: Only one ECC error is counted for each data unit. If multiple read transactions access the same unit data containing an ECC error, the ECCCNT[15:0] will increment each time the unit data is read.* ***Note**: Once the count reaches 0xFFFF, the ECCCNT[15:0] will stop incrementing* ***Note**: POR or Hardware/ Software reset clears the ECCNT[15:0] to 0x0000.* Selection options: ECC Error Count Dependency: N/A

5.12 高级扇区保护寄存器 (ASPO)

ASP 寄存器（ASPO）配置高级扇区保护方式的行为。

表 64 高级扇区保护寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ASPO[15:6]	RESRVD	Reserved for future use	N -> R/1	1111111111	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
ASPO[5]	ASPRDP	Read Password based Protection selection	N -> R/1	1	Description: The ASPRDP bit selects the Read Password Mode Protection mode. Read Password Protection mode works in conjunction with Password Protection mode to protect all sectors from Read/ Erase/Program. Based on TBPROT configuration bit (CFR1x[5]), either the top or bottom sector is available for reading. Selection options: 0 = Read Password Protection Mode is enabled 1 = Read Password Protection Mode is disabled Dependency: TBPROT (CFR1x[5])
ASPO[4]	ASPDYB	Dynamic Protection (DYB) for all sectors at power-up selection	N -> R/1	1	Description: The ASPDYB bit selects whether all DYB bits (sectors) are in the protected state following power-up or hardware reset. DYB bits will individually need to be reset to change sector protections. Selection options: 0 = DYB based sector protection enabled at power-up or hardware reset 1 = DYB based sector protection disabled at power-up or hardware reset Dependency: N/A

（表格续下页……）

表 64　　（续）高级扇区保护寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ASPO[3]	ASPPPB	Permanent Protection (PPB) bits for all sectors programmability selection	N -> R/1	1	Description: The ASPPPB bit selects whether all PPB bits are OTP making PPB sector protection permanent. ***Note**: ASPPPB disables PPB erase transaction (ERPPB_0_0).* Selection options: 0 = PPB bits are OTP 1 = PPB bits can be erased and programmed as desired Dependency: N/A
ASPO[2]	ASPPWD	Password Based Protection selection	N -> R/1	1	Description: The ASPPWD bit selects the Password Protection Mode. Password Protection mode protects all PPB bits till the correct password is entered. The ASPPWD can also be used in combination with the ASPRDP to protect all registers and all memory from erase/program and to protect sectors from being read as well till the correct password is provided - except for top or bottom sector which is available for reading based on TBPROT configuration bit (CFR1x[5]). ***Note**: When ASPPWD is selected, ASPO[15:0], CFR1N[7:2] and PWDO[63:0] are protected against Write operations.* Selection options: 0 = Password Protection Mode is enabled 1 = Password Protection Mode is disabled Dependency: N/A

（表格续下页……）

表 64　　（续）高级扇区保护寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ASPO[1]	ASPPER	Persistent Protection selection (Register Protection selection)	N -> R/1	1	Description: The ASPPER bit selects the Persistent Protection Mode. The Persistent Protection mode (ASPPER) protects the ASPO[15:0], CFR1x[6, 5, 4, 2] and CFR3x[3] registers from erase or program. Selection options: 0 = Persistent Protection Mode is enabled 1 = Persistent Protection Mode is disabled Dependency: N/A
ASPO[0]	ASPPRM	Permanent Protection selection	N -> R/1	1	Description: The ASPPRM bit selects the Permanent Protection Mode. The Permanent Protection mode (ASPPRM) permanently protects the PPB bits from erase or program. ASPPRM bit should be programmed once all the PPB based sector protections are finalized. ***Note***: *Permanent protection is independent of the PPBLOCK bit.* Selection options: 0 = Permanent Protection Mode is enabled 1 = Permanent Protection Mode is disabled Dependency: N/A

5.13　ASP 密码寄存器 (PWDO)

ASP 密码寄存器 (PWDO) 用于永久定义密码。

表 65　　密码寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
PWDO[63:0]	PASWRD[63:0]	Password Register	N -> R/1	0xFFFFFFFF FFFFFFFF	Description: The PASWRD[63:0] permanently stores a password used in password protected modes of operation. When the Password Protection Mode is enabled, this register will output the undefined data upon read password request. Selection options: Password Dependency: N/A

5.14　ASP PPB 锁定寄存器 (PPLV)

ASP PPB 锁定寄存器 (PPLV) 中的 PPBLCK 位用于保护 PPB 位。

表 66　　ASP PPB 锁定寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
PPLV[7:1]	RESVRD	Reserved for future use	V -> R	0000000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
PPLV[0]	PPBLCK	PPB Temporary Protection selection	V -> R/W	1, ASPO[2:1]	Description: The PPBLCK bit is used to temporarily protect all the PPB bits. Selection options: 1 = PPB Bits can be erased or programmed 0 = PPB bits are protected against erase or program till the next POR or hardware reset Dependency: N/A

5.15　ASP PPB 访问寄存器 (PPAV)

ASP PPB 访问寄存器 (PPAV) 用于提供每个扇区的 PPB 保护位的状态。

表 67 ASP PPB 访问寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
PPAV[7:0]	PPBACS[7:0]	Sector Based PPB Protection status	N -> R/W	11111111	Description: The PPBACS[7:0] bits are used to provide the state of the individual sector's PPB bit. Selection options: FF = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 1, not protecting that sector from program or erase operations 00 = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A

5.16 ASP 动态功能块访问寄存器 (DYAV)

ASP DYB访问寄存器 (DYAV) 用于提供每个扇区的DYB保护位的状态。

表 68 ASP DYB访问寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
DYAV[7:0]	DYBACS[7:0]	Sector Based DYB Protection status	V -> R/W	11111111	Description: The DYBACS[7:0] bits are used to provide the state of the individual sector's DYB bit. Selection options: FF = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 1, not protecting that sector from program or erase operations 00 = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 0, protecting that sector from program or erase operations Dependency: N/A

5.17 数据学习寄存器 (DLPx)

数据学习类型码寄存器（DLPx）包含 8 位数据学习类型码。

表 69 数据学习寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
DLPN[7:0] DLPV[7:0]	DTLRPT[7 :0]	Data Learning Pattern selection	N -> R/W V -> R/W	0x00	Description: The DTLRPT[7:0] bits provide the data pattern which is output during Read Latency cycles. This pattern is transferred to the host during SDR/DDR read transaction latency cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits. Selection options: Pattern Dependency: N/A

NOT YET CONVERTED: anchorline0

表 70 DLR 特点汇总

Interface type	SDR	DDR
1-1-1	N/A	N/A
1-2-2		
1-1-4	Yes	
1-4-4		Yes
4-4-4		
AutoBoot	N/A	N/A
Register Access		

表 71 数据学习类型码行为

Interface data type	Latency type 1	Latency type 2
SDR	Greater than or equal to 9; DLP on last 8 Clock Cycles	Less than 9; DLP is truncated
DDR	Greater than or equal to 5; DLP on last 4 Clock Cycles	Less than 5; DLP is truncated

5.18 自动启动寄存器 (ATBN)

自动启动寄存器 (ATBN) 提供了一种自动读取启动代码的方法，作为加电复位或硬件复位过程的一部分。

表 72 自动启动寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
ATBN[31:9]	STADR[22:0]	Starting Address Selection where AutoBoot will start reading data from	N -> R/W	00000000000000000000000	Description: The STADR[22:0] bits set the starting address from which the device will output the read data. Selection options: Address Bits Dependency: N/A
ATBN[8:1]	STDLY[7:0]	AutoBoot Read Starting Delay Selection	N -> R/W	00000000	Description: The STDLY[7:0] bits specify the initial delay (clock cycles) needed by the host before it can accept data. ***Note**: STDLY[7:0] = 0x00 is valid up to 50 MHz. STDLY[7:0] > 0x00 or higher is valid up to 166 MHz.* Selection options: Address Bits Dependency: N/A
ATBN[0]	ATBTEN	AutoBoot Feature Selection	N -> R/W	0	Description: The ATBTEN bit enables or disables the AutoBoot feature. Selection options: 0 = AutoBoot feature disabled 1 = AutoBoot feature enabled Dependency: N/A

5.19 扇区擦除计数寄存器（SECV）

扇区擦除计数寄存器 (SECV) 包含指定扇区已擦除的次数。

表 73　　扇区擦除计数寄存器

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (hex)	Description
SECV[23]	SECCPT	Sector Erase Count Corruption Status Flag	V -> R	0x0	Description: The SECCPT bit is used to determine if the reported sector erase count is corrupted and was reset. ***Note**: If SECCPT is set due to count corruption, it will reset to '0' on the next successful erase operation on the selected sector.* Selection options: 0 = Sector Erase Count is not corrupted and is valid 1 = Sector Erase Count is corrupted and is not valid Dependency: N/A
SECV[22:0]	SECVAL[22:0]	Sector Erase Count Value	V -> R	0x000000	Description: The SECVAL[22:0] bits store the number of times a sector has been erased. Selection options: Value Dependency: N/A

5.20　英飞凌 Endurance Flex 架构选择寄存器 (EFXx)

英飞凌 Endurance Flex 架构选择寄存器 (EFXx) 根据四个指针架构来定义长保留/高耐久性区域。

表 74　　英飞凌 Endurance Flex 架构选择寄存器（指针 4）

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EFX4O[10:2]	EPTAD4[8:0]	Infineon Endurance Flex architecture Pointer 4 Address Selection	N -> R/1	111111111	Description: The EPTAD4[8:0] bits define the 9-bit address of the beginning sector from where the long retention/high endurance region is defined. Selection options: Pointer Address Dependency: N/A
EFX4O[1]	ERGNT4	Infineon Endurance Flex architecture Pointer 4 based Region Type Selection	N -> R/1	1	Description: The ERGNT4 bit defines whether the region is long retention or high endurance. Selection options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX4O[0]	EPTEB4	Infineon Endurance Flex architecture Pointer 4 Enable# Selection	N -> R/1	1	Description: The EPTEN4 bit define whether the wear leveling pointer is enabled/disabled. Selection options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

表 75　　英飞凌 Endurance Flex 架构选择寄存器（指针 3）

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EFX3O[10:2]	EPTAD3[8:0]	Infineon Endurance Flex architecture Pointer 3 Address Selection	N -> R/1	111111111	Description: The EPTAD3[8:0] bits define the 9-bit address of the beginning sector from where the long retention/high endurance region is defined. Selection options: Pointer Address Dependency: N/A
EFX3O[1]	ERGNT3	Infineon Endurance Flex architecture Pointer 3 based Region Type Selection	N -> R/1	1	Description: The ERGNT3 bit defines whether the region is long retention or high endurance. Selection options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX3O[0]	EPTEB3	Infineon Endurance Flex architecture Pointer 3 Enable# Selection	N -> R/1	1	Description: The EPTEN3 bit define whether the wear leveling pointer is enabled/disabled. Selection options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

表 76　　英飞凌 Endurance Flex 架构选择寄存器（指针 2）

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EFX2O[10:2]	EPTAD2[8:0]	Infineon Endurance Flex architecture Pointer 2 Address Selection	N -> R/1	111111111	Description: The EPTAD2[8:0] bits define the 9-bit address of the beginning sector from where the long retention/high endurance region is defined. Selection options: Pointer Address Dependency: N/A
EFX2O[1]	ERGNT2	Infineon Endurance Flex architecture Pointer 2 based Region Type Selection	N -> R/1	1	Description: The ERGNT2 bit defines whether the region is long retention or high endurance. Selection options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX2O[0]	EPTEB2	Infineon Endurance Flex architecture Pointer 2 Enable# Selection	N -> R/1	1	Description: EPTEN2 bit define whether the wear leveling pointer is enabled/ disabled. Selection options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

表 77　　英飞凌 Endurance Flex 架构选择寄存器（指针 1）

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EFX1O[10:2]	EPTAD1[8:0]	Infineon Endurance Flex architecture Pointer 1 Address Selection	N -> R/1	111111111	Description: The EPTAD1[8:0] bits define the 9-bit address of the beginning sector from where the long retention/high endurance region is defined. Selection options: Pointer Address Dependency: N/A
EFX1O[1]	ERGNT1	Infineon Endurance Flex architecture Pointer 1 based Region Type Selection	N -> R/1	1	Description: The ERGNT1 bit defines whether the region is long retention or high endurance. Selection options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX1O[0]	EPTEB1	Infineon Endurance Flex architecture Pointer 1 Enable# Selection	N -> R/1	1	Description: The EPTEN1 bit define whether the wear leveling pointer is enabled/disabled. Selection options: 0 = Pointer Address Enabled 1 = Pointer Address Disabled Dependency: N/A

表 78　　英飞凌 Endurance Flex 架构选择寄存器 (指针 0)

Bit number	Name	Function	Read/ Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EFX0O[1]	GBLSEL	All Sectors based Region type Selection	N -> R/1	1	Description: The GBLSEL bit defines whether all sectors are defined as long retention region or high endurance region. ***Note**: If all other pointer registers are disabled, this bit defines the behavior of the entire memory space and is hardwired to start at Sector 0.* Selection options: 0 = Long Retention Sectors 1 = High Endurance Sectors Dependency: N/A
EFX0O[0]	WRLVEN	Wear Leveling Enable Selection	N -> R/1	1	Description: The WRLVEN bit enables/ disables the wear leveling feature. Selection options: 0 = Wear Leveling Disabled 1 = Wear Leveling Enabled Dependency: N/A

6 命令传输表

6.1 1-1-1 命令传输表

表79 → 1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read device ID	RDIDN_0_0	**Read manufacturer and device identification** transaction provides read access to manufacturer and device identification.	–	9F (CMD)	–	–	–	–	–	–	–	–	Figure 12	166	N/A
	RSFDP_3_0	**Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).	–	5A (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13	50	3
	RDUID_0_0	**Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device.	–	4C (CMD)	–	–	–	–	–	–	–	–	Figure 12	166	N/A

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表79 → （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Register access	RDSR1_0_0	**Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ1/SO.	–	05 (CMD)	–	–	–	–	–	–	–	–			
	RDSR2_0_0	**Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ1/SO.	–	07 (CMD)	–	–	–	–	–	–	–	–			
	RDCR1_0_0	**Read Configuration Register-1** transaction allows the Configuration Register-1 contents to be read from DQ1/SO.	–	35 (CMD)	–	–	–	–	–	–	–	–			

（表格续下页.....）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	RDARG_C_0	**Read Any Register** transaction provides a way to read all addressed nonvolatile and volatile device registers.	–	65 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	WRENB_0_0	**Write Enable** sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program, and erase transactions.	–	06 (CMD)	–	–	–	–	–	–	–	–	Figure 7		N/A
	WRENV_0_0	**Write Enable Volatile** enable write of volatile Registers.	–	50 (CMD)	–	–	–	–	–	–	–	–			

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表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Register access	WRDIS_0_0	**Write Disable** sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program, and erase transactions executaion.	–	04 (CMD)	–	–	–	–	–	–	–	–	Figure 11	166	N/A
	WRREG_0_1	**Write Register** transaction provides a way to write Status Register 1 and Configuration Registers 1 - 4	WRENB_0_0	01 (CMD)	Input STR1 data [7:0]	Input CFR1 data [7:0]	Input CFR2 data [7:0]	Input CFR3 data [7:0]	Input CFR4 data [7:0]	–	–	–			
	WRRSB_0_1	**SafeBoot Write Register** transaction to recover the device from configuration corruption.	WRENB_0_0	01 (CMD)	Input STR1 data [7:0]	Input CFR1 data [7:0]	Input CFR2 data [7:0]	Input CFR3 data [7:0]	Input CFR4 data [7:0]	Input 0x00	–	–			
	WRARG_C_1	**Write Any Register** transaction	WRENB_0_0	71 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	Figure 10		3

（表格续下页.....）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
		provides a way to write all addressed nonvolatile and volatile device registers.[1)]			ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			4
	CLPEF_0_0	**Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag)	–	30 (CMD)	–	–	–	–	–	–	–	–	Figure 7		N/A
			–	82 (CMD)	–	–	–	–	–	–	–	–			
	EN4BA_0_0	**Enter 4 Byte Address Mode** transaction sets the Address Legth bit CFR2V[7] to 1	–	B7 (CMD)	–	–	–	–	–	–	–	–			

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	EX4BA_0_0	**Exit 4-Byte Address Mode** transaction sets the Address Length bit CFR2V[7] to 0	–	B8 (CMD)	–	–	–	–	–	–	–	–			
	RDDLP_0_0	**Read Data Learning Pattern Register** transaction reads the DLP pattern.	–	41 (CMD)	–	–	–	–	–	–	–	–	Figure 12		
Register access	PRDLP_0_1	**Program Data Learning Pattern** transaction programs DLP pattern into the Nonvolatile registers	WRENB_0_0	43 (CMD)	Input DLP data [7:0]	–	–	–	–	–	–	–	Figure 11		

（表格续下页.....）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	WRDLP_0_1	**Write Data Learning Pattern** transaction writes DLP pattern into the Volatile register.	WRENB_0_0	4A (CMD)	Input DLP data [7:0]	–	–	–	–	–	–	–			
Register access	WRAUB_0_1	**AutoBoot Register Write** transaction writes AutoBoot pattern into the register.	WRENB_0_0	15 (CMD)	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	–	–	–	Figure 11	166	N/A
ECC	RDECC_C_0	**Read ECC Status** is used to determine the ECC status of the addressed data unit.	–	19 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDECC_4_0		–	18 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			

（表格续下页.....）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	CLECC_0_0	**Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter.	–	1B (CMD)	–	–	–	–	–	–	–	–	Figure 7		N/A
CRC	DICHK_4_1	**Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range.	–	5B (CMD)	Start ADDR [31:24]	Start ADDR [23:16]	Start ADDR [15:8]	Start ADDR [7:0]	End ADDR [31:24]	End ADDR [23:16]	End ADDR [15:8]	End ADDR [7:0]	Figure 9		4
Read flash array	RDAY1_C_0	**Read SDR** transaction reads out the memory	–	03 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 14	50	3

（表格续下页.....）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
		contents starting at the given address.	–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDAY1_4_0		–	13 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	RDAY2_C_0	**Read Fast SDR** transaction reads out the memory contents starting at the given address.	–	0B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13	166	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDAY2_4_0		–	0C (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			
Program flash array	PRPGE_C_1	**Program Page** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	02 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	Figure 10		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–			4
Program flash array	PRPGE_4_1	**Program Page** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	12 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	Figure 10	166	4

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Erase flash array	ER004_C_0	**Erase 4KB Sector** transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh).	WRENB_0_0	20 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 8		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	ER004_4_0		WRENB_0_0	21 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
Erase flash array	ER256_C_0	**Erase 256KB Sector** transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh).	WRENB_0_0	D8 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–			3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	ER256_4_0		WRENB_0_0	DC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	ERCHP_0_0	**Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	WRENB_0_0	60 or C7 (CMD)	–	–	–	–	–	–	–	–	Figure 7		N/A
	EVERS_C_0	**Evaluate Erase Status** transaction verifies that the last erase operation on the	–	D0 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 8		3

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
		addressed sector was completed successfully.	–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	SEERC_C_0	**Sector Erase Count** transaction outputs the number of erase cycles for the sector of the inputed address from the Sector Erase Count Register.	–	5D (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–			3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
Suspend/ resume	SPEPD_0_0	**Suspend Erase/ Program/Data Integrity Check** transaction allows the system to interrupt a programming, erase or data integrity check operation	–	75 (CMD	–	–	–	–	–	–	–	–	Figure 7		N/A

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表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	SPEPA_0_0	**Suspend Erase/ Program** alternate transaction allows the system to interrupt a programming or erase.	–	85 (CMD)	–	–	–	–	–	–	–	–			
			–	B0 (CMD)	–	–	–	–	–	–	–	–			
	RSEPD_0_0	**Resume Erase/ Program/Data Integrity Check** transaction allows the system to resume a programming, erase or data integrity check operation	–	7A (CMD)	–	–	–	–	–	–	–	–			
Suspend/ resume	RSEPA_0_0	**Resume Erase/ Program** alternate transaction allows the system to resume a programming,	–	8A (CMD)	–	–	–	–	–	–	–	–	Figure 7	166	N/A

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
		erase or data integrity check operation	–	30 (CMD)	–	–	–	–	–	–	–	–			
Secure silicon region array	PRSSR_C_1	**Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region	WRENB_0_0	42 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	Figure 10		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–			4
	RDSSR_C_0	**Read Secure Silicon Region** transaction reads data from the SSR.	–	4B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
Advanced sector protection	PRASP_0_1	ASP Register Write	WRENB_0_0	2F (CMD)	ASP Low Byte [7:0]	ASP High Byte [7:0]	–	–	–	–	–	–	Figure 11		N/A
	RDDYB_C_0	**Read Dynamic Protection Bit** transaction reads the contents of the DYB Access register.	–	FA (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDDYB_4_0		–	E0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	WRDYB_C_1	**Write Dynamic Protection Bit** transaction writes to the DYB Access register	WRENB_0_0	FB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	Figure 10		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			4
	WRDYB_4_1		WRENB_0_0	E1 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			
Advanced sector protection	RDPPB_C_0	**Read Persistent Protection Bit** transaction reads the contents of the PPB Access register	–	FC (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 13		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDPPB_4_0		–	E2 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
Advanced sector protection	PRPPB_C_0	**Program Persistent Protection Bit** transaction programs/writes the PPB register to enable the sector protection.	WRENB_0_0	FD (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 8	166	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	PRPPB_4_0		WRENB_0_0	E3 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	ERPPB_0_0	**Erase Persistent Protection Bit** transaction sets all persistent protection bits to 1.	WRENB_0_0	E4 (CMD)	–	–	–	–	–	–	–	–	Figure 7		N/A
	WRPLB_0_0	**Write PPB Protection Lock Bit** transaction clears the PPB Lock to 0.	WRENB_0_0	A6 (CMD)	–	–	–	–	–	–	–	–			
	RDPLB_0_0	**Read Program Persistent Protection Lock Bit** transaction shifts out the 8-bit PPB Lock register contents with MSb first	–	A7 (CMD)	–	–	–	–	–	–	–	–	Figure 12		
	PGPWD_0_1	**Program Password** transaction programs the 64-bit password to flash device.	WRENB_0_0	E8 (CMD)	Password [7:0]	Password [15:8]	Password [23:16]	Password [31:24]	Password [39:32]	Password [47:40]	Password [55:48]	Password [63:56]	Figure 11		

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	PWDUL_0_1	**Password Unlock** transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1.	–	E9 (CMD)	Password [7:0]	Password [15:8]	Password [23:16]	Password [31:24]	Password [39:32]	Password [47:40]	Password [55:48]	Password [63:56]			

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Reset	SRSTE_0_0	**Software Reset Enable** command is required immediately before a SFRST_0_0 transaction	–	66 (CMD)	–	–	–	–	–	–	–	–	Figure 7		
	SFRST_0_0	**Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from nonvolatile default values	SRSTE_0_0	99 (CMD)	–	–	–	–	–	–	–	–			

（表格续下页……）

表79 （续表）1-1-1命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Reset	SFRSL_0_0	**Legacy Software Reset** transaction restores the device to its initial power-up state, by reloading volatile registers from nonvolatile default values	–	F0 (CMD)	–	–	–	–	–	–	–	–	Figure 7		
Deep power down	ENDPD_0_0	**Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode	–	B9 (CMD)	–	–	–	–	–	–	–	–			

1) 此指令可以禁用，指令值将用于程序/擦除恢复指令。请参阅配置寄存器3（CFR3x）。

6.2 1-2-2 命令传输表

表 80　1-2-2 命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read flash array	RDAY3_C_0	**Read SDR Dual I/O** transaction reads out the memory contents starting at the given address.	–	BB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	Figure 16	166	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			4
	RDAY3_4_0		–	BC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			
	RDAY6_C_0	**Continuous Read SDR Dual I/O** transaction reads out the memory contents starting at the given address.	RDAY3_C_0	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	–	Figure 17		3
				ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			4
	RDAY6_4_0		RDAY3_4_0	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			

6.3 1-1-4 命令传输表

表 81　　1-1-4 命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read flash array	RDAY4_C_0	Read SDR Quad Output transaction reads out the memory contents starting at the given address.	–	6B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 18	166	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDAY4_4_0		–	6C (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			

6.4 1-4-4 命令传输表

表82 1-4-4·命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read manufacturer and device ID	RDQID_0_0	**Read Quad manufacturer and device identification** transaction provides read access to manufacturer and device identification.	–	AF (CMD)	–	–	–	–	–	–	–	–	Figure 23	166	N/A
Read flash array	RDAY5_C_0	**Read SDR Quad I/O** transaction reads out the memor	–	EB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	Figure 19		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			4

（表格续下页……）

表82 1-4-4·命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	RDAY5_4_0	y contents starting at the given address.	–	EC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			3
	RDAY6_C_0	Continuous Read SDR Quad I/O transaction reads out the memory contents starting at the given address.	RDAY5_C_0	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	–	Figure 20		4
				ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]							
	RDAY6_4_0		RDAY5_4_0	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			
	RDAY7_C_0	**Read DDR**	–	ED (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	Figure 21	102	3

（表格续下页……）

表82　1-4-4·命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
		Quad I/O transaction reads out the memory content starting at the given address.	–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	4			
			–												
	RDAY7_4_0		–	EE (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–				
	RDAY8_C_0	Continuous Read DDR Quad I/O transaction reads out the memory contents	RDAY7_C_0	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	–	Figure 22		4
				ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	4			3

（表格续下页……）

6 Transcation table

表82 1-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	RDAY8_4_0	starting at the given address.	RDAY7_4_0	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			4

6.5 4-4-4 命令传输表

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
Read·device·ID	RDIDN_0_0	**Read·manufacturer·and·device·identification·**transaction·provides·read·access·to·manufacturer·and·device·identification.	–	9F·(CMD)	–	–	–	–	–	–	–	–	Figure·27	166	N/A
	RSFDP_3_0	**Read·JEDEC·Serial·Flash·Discoverable·Parameters·**transaction·sequentially·accesses·the·Serial·Flash·Discovery·Parameters·(SFDP).	–	5A·(CMD)	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–	–	Figure·31	50	3

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	RDQID_0_0	**Read·Quad·manufacturer·and·device·identification·**transaction·provides·read·access·to·manufacturer·and·device·identification.	–	AF·(CMD)	–	–	–	–	–	–	–	–	Figure·27	166	N/A
	RDUID_0_0	**Read·Unique·ID·**accesses·a·factory·programmed·64-·bit·number·which·is·unique·to·each·device.	–	4C·(CMD)	–	–	–	–	–	–	–	–			
Register·access	RDSR1_0_0	**Read·Status·Register·1·**transaction·allows·the·Status·Register·1·contents·to·be·read·from·DQ1/SO.	–	05·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页.....）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	RDSR2_0_0	**Read·Status·Register-2·** transaction·allows·the·Status·Register-2·contents·to·be·read·from·DQ1/SO.	–	07·(CMD)	–	–	–	–	–	–	–	–			
	RDCR1_0_0	**Read·Configuration·Register-1·** transaction·allows·the·Configuration·Register-1·contents·to·be·read·from·DQ1/SO.	–	35·(CMD)	–	–	–	–	–	–	–	–			
	RDARG_C_0	**Read·Any·Register·** transaction·provides·a·way·to·read·all·addressed·nonvolatile·and·volatile·device·registers.	–	65·(CMD)	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–	–	Figure·31		3
			–		ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–			4

（表格续下页.....）

表83　4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	WRENB_0_0	**Write·Enable·** sets·the·Write·Enable·Latch·bit·of·the·Status·Register·1·to·1·to·enable·write,·program,·and·erase·transactions.	–	06·(CMD)	–	–	–	–	–	–	–	–	Figure·24		N/A
	WRENV_0_0	**Write·Enable·Volatile·** enable·write·of·volatile·Registers.	–	50·(CMD)	–	–	–	–	–	–	–	–			
	WRDIS_0_0	**Write·Disable·** sets·the·Write·Enable·Latch·bit·of·the·Status·Register·1·to·0·to·disable·write,·program,·and·erase·transactions·executaion.	–	04·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页.....）

表83 4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	WRREG_0_1	**Write Register** transaction provides a way to write Status Register 1 and Configuration Registers 1–4	WRENB_0_0	01 (CMD)	Input STR1 data [7:0]	Input CFR1 data [7:0]	Input CFR2 data [7:0]	Input CFR3 data [7:0]	Input CFR4 data [7:0]	–	–	–	Figure 29		
Register access	WRARG_C_1	**Write Any Register** transaction provides a way to write all addressed nonvolatile and volatile device registers.	WRENB_0_0	71 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	Figure 30	166	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			4
Register access	CLPEF_0_0	**Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag)	–	30 (CMD)	–	–	–	–	–	–	–	–	Figure 24		N/A

（表格续下页……）

表83　4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
		Note·This·command·may·be·disabled·and·the·instruction·value·instead·used·for·a·program/erase·resume·command.·See·"Configuration·Register·3·(CFR3x)"·on·page·92.	–	82·(CMD)	–	–	–	–	–	–	–	–			
	EN4BA_0_0	**Enter·4·Byte·Address·Mode**·transaction·sets·the·Address·Legth·bit·CFR2V[7]·to·1	–	B7·(CMD)	–	–	–	–	–	–	–	–			N/A
	EX4BA_0_0	**Exit·4·Byte·Address·Mode**·transaction·sets·the·Address·Legth·bit·CFR2V[7]·to·0	–	B8·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	RDDLP_0_0	**Read·Data·Learning·Pattern·Register·** transaction·reads·the·DLP·pattern.	–	41·(CMD)	–	–	–	–	–	–	–	–	Figure·27		
	PRDLP_0_1	**Program·Data·Learning·Pattern·** transaction·programs·DLP·pattern·into·the·Nonvolatile·registers	WRENB_0_0	43·(CMD)	Input·DLP data·[7:0]	–	–	–	–	–	–	–	Figure·29		
	WRDLP_0_1	**Write·Data·Learning·Pattern·** transaction·writes·DLP·pattern·into·the·Volatile·register.	WRENB_0_0	4A·(CMD)	Input·DLP data·[7:0]	–	–	–	–	–	–	–			

(表格续下页.....)

表83　4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
	WRAUB_0_1	**AutoBoot Register Write** transaction writes AutoBoot pattern into the register.	WRENB_0_0	15 (CMD)	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	–	–	–			
ECC	RDECC_C_0	**Read ECC Status** is used to determine the ECC status of the addressed data unit.	–	19 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 31	166	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDECC_4_0		–	18 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	CLECC_0_0	**Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter.	–	1B (CMD)	–	–	–	–	–	–	–	–	Figure 24		N/A

（表格续下页……）

表83 4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
CRC	DICHK_4_1	**Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range.	–	5B (CMD)	Start ADDR [31:24]	Start ADDR [23:16]	Start ADDR [15:8]	Start ADDR [7:0]	End ADDR [31:24]	End ADDR [23:16]	End ADDR [15:8]	End ADDR [7:0]	Figure 28		4
Read flash array	RDAY5_C_0	**Read QPI SDR** transaction reads out the memory contents starting at the given address.	–	EB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	Figure 32		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			4
	RDAY2_4_0		–	0C (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			
	RDAY5_4_0		–	EC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			
Read flash array	RDAY6_C_0	**Continuous Read QPI SDR** transaction reads out the memory contents starting at the given address.	RDAY5_C_0	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	–	Figure 33		3
				ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			4
	RDAY6_4_0		RDAY5_4_0	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	RDAY7_C_0	**Read·QPI·DDR·** transaction·reads·out·the·memory·contents·starting·at·the·given·address.	–	ED·(CMD)	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–	–	Figure·34		3
			–		ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–			4
	RDAY7_4_0		–	EE·(CMD)	ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–			
Read·flash·array	RDAY8_C_0	**Continuous·Read·QPI·DDR·** transaction·reads·out·the·memory·contents·starting·at·the·given·address.	RDAY7_C_0	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–	–	–	Figure·35	166	3
				ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–	–			4
	RDAY8_4_0		RDAY7_4_0	ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Mode·[7:0]	–	–	–	–			
Program·flash·array	PRPGE_C_1	**Program·Page·** programs·256B·or·512B·data·to·the·memory·array·in·one·transaction.	WRENB_0_0	02·(CMD)	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Input·Data·1 [7:0]	Input·Data·2 [7:0]	(Continue)	–	–	Figure·30		3
					ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Input·Data·1 [7:0]	Input·Data·2 [7:0]	(Continue)	–			4
	PRPGE_4_1		WRENB_0_0	12·(CMD)	ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	Input·Data·1 [7:0]	Input·Data·2 [7:0]	(Continue)	–			

（表格续下页……）

表83　4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Erase flash array	ER004_C_0	**Erase 4KB Sector** transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh).	WRENB_0_0	20 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 26		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	ER004_4_0		WRENB_0_0	21 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	ER256_C_0	**Erase 256KB Sector** transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh).	WRENB_0_0	D8 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–			3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	ER256_4_0		WRENB_0_0	DC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	ERCHP_0_0	**Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	WRENB_0_0	60 or C7 (CMD)	–	–	–	–	–	–	–	–	Figure 24		N/A
Erase flash array	EVERS_C_0	**Evaluate Erase Status** transaction verifies that the last erase operation on the	–	D0 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 26		3

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
		addressed·sector·was·completed·successfully.	–		ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–			4
	SEERC_C_0	**Sector·Erase·Count·** transactionoutputs·the·number·of·erase·cycles·for·the·sector·of·the·inputed·address·from·the·Sector·Erase·Count·Register.	–	5D·(CMD)	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–	–			3
			–		ADDR·[31:24]	ADDR·[23:16]	ADDR·[15:8]	ADDR·[7:0]	–	–	–	–			4
Suspend/·resume	SPEPD_0_0	**Suspend·Erase/·Program/Data·Integrity·Check·** transaction·allows·the·system·to·interrupt·a·programming,·erase·or·data·integrity·check·operation	–	75·(CMD	–	–	–	–	–	–	–	–	Figure·24	166	N/A
	SPEPA_0_0	**Suspend·Erase/·Program**	–	85·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
		alternate·transaction·allows·the·system·to·interrupt·a·programming·or·erase.	–	B0·(CMD)	–	–	–	–	–	–	–	–			
	RSEPD_0_0	**Resume·Erase/·Program/Data·Integrity·Check·** transaction·allows·the·system·to·resume·a·programming,·erase·or·data·integrity·check·operation	–	7A·(CMD)	–	–	–	–	–	–	–	–			
	RSEPA_0_0	**Resume·Erase/·Program·** alternatetransaction·allows·the·system·to·resume·a·programming,·erase·or·data·integrity·check·operation	–	8A·(CMD)	–	–	–	–	–	–	–	–			N/A
			–	30·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页.....）

表83　4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Secure silicon region array	PRSSR_C_1	**Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region	WRENB_0_0	42 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	–	Figure 30		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–			4
	RDSSR_C_0	**Read Secure Silicon Region** transaction reads data from the SSR.	–	4B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 31		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
Advanced sector protection	PRASP_0_1	ASP Register Write	WRENB_0_0	2F (CMD)	ASP Low Byte [7:0]	ASP High Byte [7:0]	–	–	–	–	–	–	Figure 29		N/A
	RDDYB_C_0	**Read Dynamic Protection Bit** transaction reads the contents of the DYB Access register.	–	FA (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 31		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDDYB_4_0		–	E0 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
Advanced sector	WRDYB_C_1	**Write Dynamic Protection Bit** transaction	WRENB_0_0	FB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	–	Figure 30	166	3

（表格续下页……）

表83 4-4-4命令传输表

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
protection		writes to the DYB Access register			ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			4
	WRDYB_4_1		WRENB_0_0	E1 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–			
	RDPPB_C_0	**Read Persistent Protection Bit** transaction reads the contents of the PPB Access register	–	FC (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 31		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	RDPPB_4_0		–	E2 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			
	PRPPB_C_0	**Program Persistent Protection Bit** transaction programs/writes the PPB register to enable the sector protection.	WRENB_0_0	FD (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	–	Figure 26		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			4
	PRPPB_4_0		WRENB_0_0	E3 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–			

（表格续下页.....）

表83　4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	ERPPB_0_0	**Erase·Persistent·Protection·Bit·**transaction·sets·all·persistent·protection·bits·to·'1'.	WRENB_0_0	E4·(CMD)	–	–	–	–	–	–	–	–	Figure·24		N/A
	WRPLB_0_0	**Write·PPB·Protection·Lock Bit·**transaction·clears·the·PPB·Lock·to·0	WRENB_0_0	A6·(CMD)	–	–	–	–	–	–	–	–			
	RDPLB_0_0	**Read·Program·Persistent·Protection·Lock Bit·**transaction·shifts·out·the·8-·bit·PPB·Lock·register·contents·with·MSb·first	–	A7·(CMD)	–	–	–	–	–	–	–	–	Figure·27		
	PGPWD_0_1	**Program·Password·**transaction·programs·the·64-bit·password·to·flash·device.	WRENB_0_0	E8·(CMD)	Password·[7:0]	Password·[15:8]	Password·[23:16]	Password·[31:24]	Password·[39:32]	Password·[47:40]	Password·[55:48]	Password·[63:56]	Figure·29		

（表格续下页……）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
	PWDUL_0_1	**Password·Unlock·** transaction·sends·the·64-bit·password·to·flash·device.·If·the·supplied·password·does·not·match·the·hidden·password·in·the·Password·Register,·the·device·is·locked·and·only·a·hardware·reset·or·POR·will·return·the·device·to·standby·state,·ready·for·new·transactions·such·as·a·retry·of·the·PWDUL_0_1.·If·the·password·does·match,·the·PPB·Lock·bit·is·set·to·'1'.	–	E9·(CMD)	Password·[7:0]	Password·[15:8]	Password·[23:16]	Password·[31:24]	Password·[39:32]	Password·[47:40]	Password·[55:48]	Password·[63:56]			

(表格续下页.....)

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
Reset	SRSTE_0_0	**Software·Reset·Enable·** command·is·required·immediately·before·a·SFRST_0_0 transaction	–	66·(CMD)	–	–	–	–	–	–	–	–	Figure·24	166	N/A
	SFRST_0_0	**Software·Reset·** transaction·restores·the·device·to·its·initial·power-up·state,·by·reloading·volatile·registers·from·nonvolatile·default·values	SRSTE_0_0	99·(CMD)	–	–	–	–	–	–	–	–			

（表格续下页.....）

表83 4-4-4·命令传输表

Function	Transaction·name	Description	Prerequisite·transaction	Byte·1·(Hex)	Byte·2·(Hex)	Byte·3·(Hex)	Byte·4·(Hex)	Byte·5·(Hex)	Byte·6·(Hex)	Byte·7 (Hex)	Byte·8 (Hex)	Byte·9 (Hex)	Transaction·format	Max·freq.·(MHz)	Address·length
Reset	SFRSL_0_0	**Legacy·Software·Reset·**transaction·restores·the·device·to·its·initial·power-up·state,·by·reloading·volatile·registers·from·nonvolatile·default·values	–	F0·(CMD)	–	–	–	–	–	–	–	–	Figure·24		
Deep·power-down	ENDPD_0_0	**Enter·Deep·Power·Down·Mode·**transaction·shifts·device·in·the·lowest·power·consumption·mode	–	B9·(CMD)	–	–	–	–	–	–	–	–			

7 电气特性

7.1 绝对最大额定值[1. - 3.]

Storage Temperature Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
V_{CC} (HL-T)	–0.5 V to +4.0 V
V_{CC} (HS-T)	–0.5 V to +2.5 V
Input voltage with respect to Ground (V_{SS})	–0.5 V to V_{CC} + 0.5 V
Output Short Circuit Current	100 mA

NOTES:

1. *信号传输期间允许的最大值请参阅“输入信号过冲”。*
2. *每一次只能有一个输出对地短接。短接时间不能超过一秒。*
3. *如果使用大于绝对最大额定值[1. -3.]中所列出的数值，可能对器件造成永久性损害。这只是压力额定值；并不意味器件在这些值或者在此数据手册操作部分所示值之上的任何其他情形下不能正常运行。如果让器件长时间在绝对最大额定值情况下运行，会影响器件的可靠性。*

7.2 工作范围

运行范围定义了一些限值，在这些限值之间可保证器件正常运行。

7.2.1 供电电压

V_{CC} (HL-T Devices)	2.7 V to 3.6 V
V_{CC} (HS-T Devices)	1.7 V to 2.0 V

7.2.2 温度范围

表 84 温度范围[1]

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient Temperature	TA	Industrial/Automotive AEC-Q100 Grade 3	–40	+85	°C
		Industrial Plus/Automotive AEC-Q100 Grade 2		+105	
		Automotive AEC-Q100 Grade 1		+125	

1) 扩展工业、汽车 2 级和汽车 1 级的工作和性能参数将由器件特性决定，并且可能与本规范中当前所示的标准工业或汽车 3 级温度范围设备有所不同。

7.3 热阻抗

表 85 热阻抗

Parameter	Description	Test condition	Device	24-ball BGA	16-lead SOIC	8-contact WSON	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal accordance with EIA/JESD51. With Still Air (0 m/s).	512T	40.4	35	32.7	°C/W
			01GT	37	28.3	–	
Theta JB	Thermal resistance (Junction to board)		512T	14.5	19	12.5	
			01GT	9.7	12	–	
Theta JC	Thermal resistance (Junction to case)		512T	8	9.9	13	
			01GT	7.5	7.6	–	

7.4 电容特性

表 86 电容

Package	Input capacitance		Output capacitance	
	Typ	Max	Typ	Max
24-ball BGA	3.0 pF	6.5 pF	7.0 pF	7.5 pF
16-lead SOIC	4.0 pF		7.5 pF	8.0 pF
8-contact WSON	3.0 pF		6.7 pF	7.5 pF

7.5 锁闭特性

表 87 锁闭参数[1]

Description	Min	Max	Unit
Input voltage with respect to VSS on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to VSS on all I/O connections			
V_{CC} Current	-100	+100	mA

1) 不包括电源 V_{CC}。测试条件：V_{CC} = 1.8 V/3.0 V，一次测试一个连接，未测试的连接处于 V_{SS}。

7.6 直流特性

7.6.1 输入信号过冲

在直流条件下，输入或 I/O 信号应保持等于或介于 V_{SS}和V_{CC}之间。在电压转换期间，输入或 I/O 可能会过冲 V_{SS}–1.0 V 或过冲至 V_{CC}+1.0 V，持续时间最长为 20 ns。

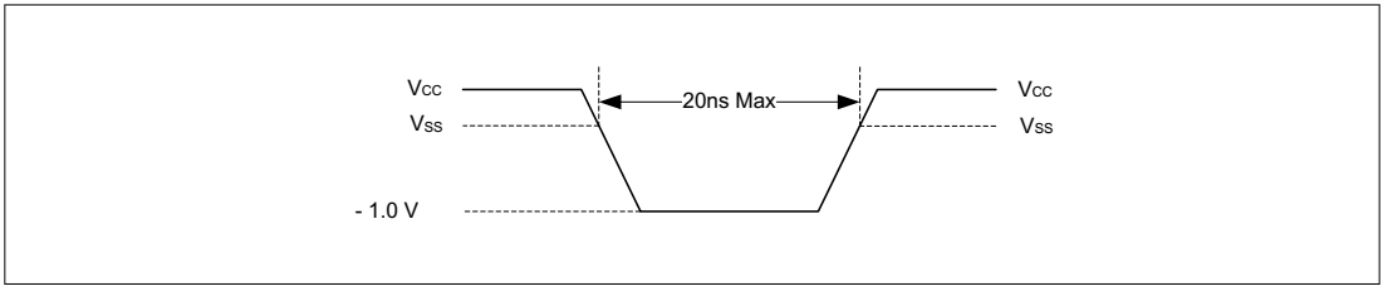

图 70　　最大负过冲波形

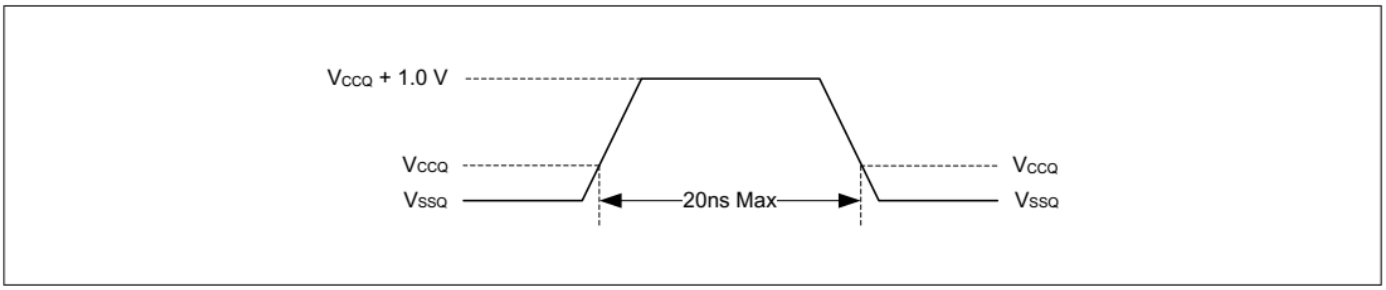

图 71　　最大正过冲波形

7.6.2　　直流特性（所有温度范围）

表 88　　直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
V_{IL}	Input Low Voltage (all V_{CC})	–	V_{CC} × -0.15	–	V_{CC} × 0.35	V	–
V_{IH}	Input High Voltage (all V_{CC})	–	V_{CC} × 0.65	–	V_{CC} × 1.15	V	–
V_{OL}	Output Low Voltage (all V_{CC})	At 0.1 mA	–	–	0.2	V	–
V_{OH}	Output High Voltage (all V_{CC})	At –0.1 mA	V_{CC} – 0.20	–	–	V	–

（表格续下页……）

表 88　　（续）直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
I_{LI}	Input Leakage Current	V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 85°C	–	–	±2	µA	–
		V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 105°C	–	–	±3	µA	–
		V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 125°C	–	–	±4	µA	–
I_{LO}	Output Leakage Current	V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 85°C	–	–	±2	µA	–
		V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 105°C	–	–	±3	µA	–
		V_{CC}= V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}, 125°C	–	–	±4	µA	–

（表格续下页……）

表 88　　（续）直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
I_{CC1}	Active Power Supply Current (READ[2)]	SDR @ 50 MHz (HL512T/ HS512T) (HL01GT/ HS01GT)	–	10/10 18/14	21/18 25/25	mA	–
		SDR @ 166 MHz (HL512T/ HS512T) (HL01GT/ HS01GT)	–	53 53	69/69 69/72	mA	–
		DDR @ 102 MHz	–	50	68	mA	–
I_{CC2}	Active Power Supply Current (Page Program) (512T/01GT)	V_{CC}= V_{CC} Max, CS# = V_{IH}	–	50	58/66	mA	–
I_{CC3}	Active Power Supply Current (Write Register and Write Any Register) (512T/01GT)	V_{CC}= V_{CC} Max, CS# = V_{IH}	–	50	55/66	mA	–
I_{CC4}	Active Power Supply Current (Sector Erase) (512T/01GT)	V_{CC}= V_{CC} Max, CS# = V_{IH}	–	50	55/66	mA	–
I_{CC5}	Active Power Supply Current (Chip Erase) (512T/01GT)	V_{CC}= V_{CC} Max, CS# = VIH	–	50	55/66	mA	–

（表格续下页……）

表 88　　（续）直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
I_{SB}	Standby Current (HS512T / HS01GT)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 85°C	–	11	113/160	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 105°C	–		188/220	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 125°C	–		340/510	µA	–
	Standby Current (HL512T/ HL01GT)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 85°C	–	14	126/160	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 105°C	–		188/425	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 125°C	–		340/560	µA	–
I_{DPD}	DPD Current (HS512T/ HS01GT)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 85°C	–	1.3	18/24	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 105°C	–		18/26	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 125°C	–		31/56	µA	–

（表格续下页……）

表 88　　（续）直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
I_{DPD}	DPD Current (HL512T/ HL01GT)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 85°C	–	2.2	18/26	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 105°C	–		18/26	µA	–
		RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}, 125°C	–		31/60	µA	–
I_{POR}	POR Current	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	–	80	mA	–
Power Up/Power Down Voltage							
V_{CC} (min)	V_{CC} (minimum operation voltage, HL-T)	–	2.7	–	–	V	Figure 66/ Figure 67
	V_{CC} (minimum operation voltage, HS-T)	–	1.7	–	–	V	
V_{CC} (cut-off)	V_{CC} (cut off where re-initialization is needed, HL-T)	–	2.4	–	–	V	Figure 67
	V_{CC} (cut off where re-initialization is needed, HS-T)	–	1.55	–	–	V	

（表格续下页……）

表 88　　（续）直流特性[1)]，[2)]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
V_{CC} (Low)	V_{CC} (low voltage for initialization to occur, HL- T)	–	0.7	–	–	V	
	V_{CC} (low voltage for initialization to occur, HS-T)	–	0.7	–	–	V	

1)　典型值为 T_{AI} = 25°C 和 V_{CC} = 1.8 V/3.0 V。
2)　读取数据返回期间输出未连接。不包括输出开关电流。

7.7　AC 测试条件

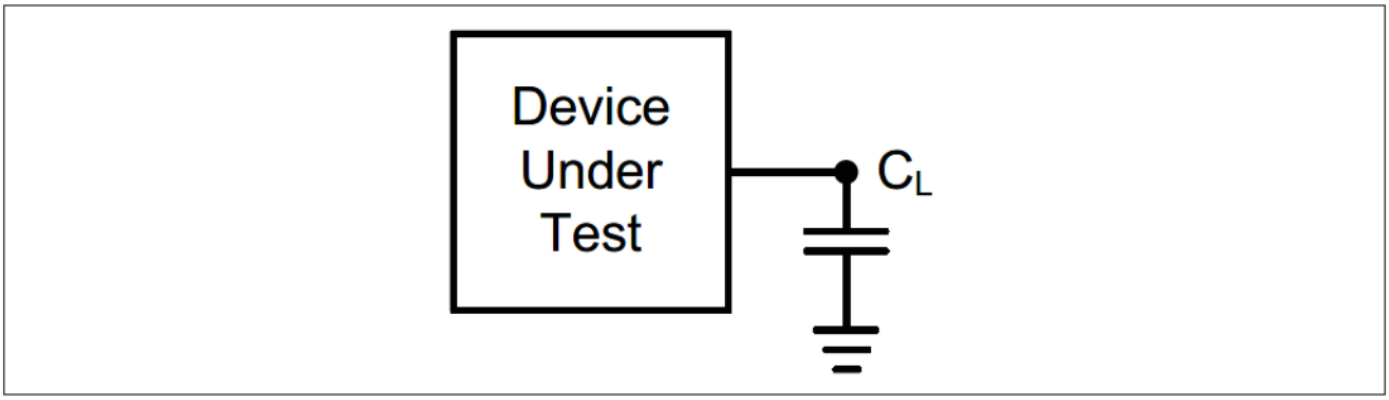

图 72　　测试设置

表 89　　交流测量条件[1)]

Parameter	Min	Max	Unit	Reference figure
Load Capacitance (C_L)	–	30	pF	Figure 72
Input Pulse Voltage	0	V_{CC}	V	–
Input Rise (t_{CRT}) and Fall (t_{CFT}) Slew Rates at 133 MHz (HL-T)[2)]	1.37	–	V/ns	Figure 78
Input Rise (t_{CRT}) and Fall (t_{CFT}) Slew Rates at 166 MHz (HL-T)[2)]	1.72			

（表格续下页……）

表 89 （续）交流测量条件[1)]

Parameter	Min	Max	Unit	Reference figure
Input Rise (t_{CRT}) and Fall (t_{CFT}) Slew Rates at 133 MHz (HS-T)[2)]	0.75			
Input Rise (t_{CRT}) and Fall (t_{CFT}) Slew Rates at 166 MHz (HS-T)[2)]	0.94			
$V_{IL(ac)}$	-0.30 × V_{CC}	0.30 × V_{CC}	V	–
$V_{IH(ac)}$	0.7 × V_{CC}	1.30 × V_{CC}		
$V_{OH(ac)}$	0.75 × V_{CC}	–		
$V_{OL(ac)}$	–	0.25 × V_{CC}		
Input Timing Ref Voltage	0.5 × V_{CC}			
Output Timing Ref Voltage				

1) AC特性表假设时钟和数据信号具有相同的斜率（斜率）。
2) 在 V_{CC} 最大时测量从输入脉冲最小值到最大值的输入斜率。

8 时序特性

表 90 时序特性[1)]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
SDR timing characteristics						
f_{CK}	Clock Frequency	DC	–	166	MHz	–
p_{CK}	CK Clock Period	$1/f_{CK}$	–	∞	ns	Figure 78
t_{CH}	Clock High Time	45% p_{CK}	–	55% p_{CK}	ns	
t_{CL}	Clock Low Time		–		ns	
t_{CS}	CS# High Time (Read transactions)	10	–	–	ns	Figure 79
	CS# High Time Between Transactions (Read transactions when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	
	CS# High Time (Program/ Erase transactions)	50	–	–	ns	
t_{CSS}	CS# Active Setup Time relative to CK (f_{CK} £ 50 MHz/f_{CK} > 50 MHz)	5/4	–	–	ns	
t_{CSH0}	CS# Active Hold Time (relative to CK in Mode 0)	4	–	–	ns	
t_{CSH3}	CS# Active Hold Time (relative to CK in Mode 3)	6	–	–	ns	
t_{SU}	Data Setup Time (all V_{CC})	2	–	–	ns	
t_{HD}	Data Hold Time (all V_{CC})				ns	
t_V[1)]	Clock Low to Output Valid (15 pF Loading, 3.0 V - 3.6 V, 30 Ω Output Impedance, 105°C) (HL-T[2)])	2	–	6.5	ns	Figure 80
	Clock Low to Output Valid (15pF Loading) (HS-T) (512T/ 01GT)	2/2	–	6/6	ns	
	Clock Low to Output Valid (15pF Loading) (HL-T)	2	–	8	ns	
	Clock Low to Output Valid (30pF Loading) (HS-T)(512T/ 01GT)	2/2	–	8/8	ns	
	Clock Low to Output Valid (30pF Loading) (HL-T)	2	–	9	ns	

（表格续下页……）

表 90 （续）时序特性[1)]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
t_{HO}	Output Hold Time (HL512T/HS512T) (HL01GT/HS01GT)	1.5/1.5 1.5/1.5	–	–	ns	
t_{DIS} [3)]	CS# Inactive to Output Disable Time (HS-T)	–	–	8	ns	
	CS# Inactive to Output Disable Time (HL-T)	–	–	9	ns	
	CS# Inactive to Output Disable Time (when Reset feature and Quad mode are both enabled)	–	–	20	ns	
t_{WPS}	WP# Setup Time (Applicable as a constraint for write register transactions when STCFWR is set to a 1)	20	–	–	ns	Figure 81
t_{WPH}	WP# Hold Time (Applicable as a constraint for write register transactions when STCFWR is set to a 1)	20	–	–	ns	
t_{IO_SKEW} [4)]	Data Skew (First Data Bit to Last Data Bit)	–	–	0.6	ns	–
DDR timing characteristics						
f_{CK}	CK Clock Frequency	DC	–	102	MHz	–
p_{CK}	CK Clock Period	$1/f_{CK}$	–	∞	ns	Figure 78
t_{CH}	Clock High Time	45% p_{CK}	–	55% p_{CK}	ns	
t_{CL}	Clock Low Time		–		ns	
t_{CS}	CS# High Time (Read transactions)	10	–	–	ns	Figure 83
	CS# High Time Between Transactions (Read transactions when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	
	CS# High Time (Program/ Erase transactions)	50	–	–	ns	
t_{CSS}	CS# Active Setup Time relative to CK (f_{CK} £ 50 MHz/f_{CK} > 50 MHz)	5/4	–	–	ns	

（表格续下页……）

表 90 （续）时序特性[1)]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
t_{CSH0}	CS# Active Hold Time (relative to CK in Mode 0)	4	–	–	ns ns	Figure 83
t_{SU}	Data Setup Time (all V_{CC})	2	–	–	ns	
t_{HD}	Data Hold Time (all V_{CC})	1.2	–	–	ns	
t_V	Clock Low to Output Valid (15 pF Loading, 3.0 V - 3.6 V, 30 W Output Impedance, 105°C) (HL-T)	2	–	6.5	ns	Figure 84
	Clock Low to Output Valid (15 pF Loading) (HS-T)(512T/01GT)	2/2	–	6/6	ns	–
	Clock Low to Output Valid (15 pF Loading) (HL-T)	2	–	8	ns	
t_{HO}	Output Hold Time (HL512T/HS512T) (HL01GT/HS01GT)	1.5/1.5 1.5/1.5	–	–	ns	
t_{DIS}	Output Disable Time (HS-T)	–	–	8	ns	
	Output Disable Time (HL-T)	–	–	9	ns	
	CS# Inactive to Output Disable Time (when Reset feature and Quad mode are both enabled)	–	–	20	ns	
t_{IO_SKEW} [5)]	Data Skew (First Data Bit to Last Data Bit)	–	–	0.6	ns	
Power up / power down timing						
t_{PU}	V_{CC}(min) to Read operation (HL512T/HS512T) (HL01GT/HS01GT)	–	–	450/500 450/500	µs	Figure 66
t_{PD}	V_{CC}(Low) time	25	–	–		Figure 67
t_{VR}	V_{CC}Power Up ramp rate	1	–	–	µs/V	–
t_{VF}	V_{CC}Power Down ramp rate	30	–	–		
Deep power down mode timing						
t_{ENTDPD} [6)]	Time to Enter DPD mode	–	–	3	µs	–
t_{EXTDPD}	Time to Exit DPD mode (HL512T/HS512T) (HL01GT/HS01GT)	–	–	380/430 380/430		Figure 65
t_{CSDPD}	Chip Select Pulse Width to Exit DPD	0.02	–	3		

表 90 （续）时序特性[1)]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
Reset timing[7)], [8)]						
t_{CSR}	CS# high before DQ3_RESET# Low	50	–	–	ns	Figure 60
t_{RS}	Reset Setup - RESET# High before CS# Low	50	–	–		Figure 56
t_{RH}	Reset Pulse Hold - RESET# Low to CS# Low (HL512T/HS512T) (HL01GT/HS01GT)	450/500 450/500	–	–	µs	
t_{RP}	RESET# Pulse Width	200	–	–	ns	Figure 56
t_{SR}	Internal Device Reset from Software Reset Transaction (512T/01GT)	–	–	83/83	µs	–
JEDEC serial flash reset signaling protocol timing						
t_{CSLW}	Chip Select Low	500	–	–	ns	Figure 63
t_{CSHG}	Chip Select High	500	–	–		
t_{RESET}	Internal device reset (HL512T/HS512T) (HL01GT/HS01GT)	–	–	450/500 450/500	µs	
t_{SUJ}	Data in Setup Time (w.r.t CS#)	50	–	–	ns	
t_{HDJ}	Data in Hold Time (w.r.t CS#)	50	–	–		
Embedded algorithm (erase, program, and data integrity check) performance[9)], [10)], [11)], [12)]						
t_W	Nonvolatile Register Write Time (512T/01GT)	–	44/44	357.5	ms	–
t_{PP}	256B Page Programming 4 KB Sector (512T/01GT)	–	430/430	2175	µs	–
	256B Page Programming 256 KB Sector (512T/01GT)	–	430/430	1700		–
	256B Page Programming 4 KB Sector (512T/01GT)	–	680/680	2175		–
	512B Page Programming 256 KB Sector (512T/01GT)	–	570/570	1700		–
t_{SE}	Sector Erase Time (4 KB physical sectors)	–	42	335	ms	–
	Sector Erase Time (256 KB Infineon Endurance Flex architecture disabled) (512T/01GT)	–	773/773	2677		–

表 90 （续）时序特性[1)]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
	Sector Erase Time (256 KB Infineon Endurance Flex architecture enabled) (512T/ 01GT)	–	773/773	5869		–
t_{BE}	Chip Erase Time (512 Mb)	–	201	696	sec	–
	Chip Erase Time (1 Gb)	–	398	1381		–
t_{EES}	Evaluate Erase Status Time for 4 KB physical sectors (HL512T/HS512T) (HL01GT/HS01GT)	–	45/45 45/45	51/51 50/54	µs	–
	Evaluate Erase Status Time for 256 KB physical sectors (HL512T/HS512T) (HL01GT/HS01GT)	–	45/45 45/45	51/51 50/54		–
t_{DIC_SETUP}	Data Integrity Check Calculation Setup Time (512T/ 01GT)	–	17/17	–	µs	–
t_{DIC_RATES}	Data Integrity Check Calculation Rate (Calculation rate over a large (>1024-byte) block of data) (512T/01GT)	55/55	65/65	–	MBps	–
t_{SEC}	Sector Erase Count Time (HL512T/HS512T) (HL01GT/HS01GT)	–	55/55 55/55	63/63 63/70	µs	–
t_{BEC1}	Blank Check single 256KB sector	–	15	17	ms	–
t_{BEC2}	Blank Check single 4KB sector	–	1	2		–
$t_{PASSWORD}$	Password Comparison Time	80	100	120	µs	–
Program, erase, or data integrity check suspend/resume timing						
t_{PEDS}	Program/Erase/Data Integrity Check Suspend	–	–	80	µs	–
t_{PEDRS}	Program/Erase/Data Integrity Check Resume to next Program/Erase/Data Integrity Check Suspend	–	100	–		–

1) 适用于所有工作温度选项。
2) 由设计保证
3) 输出 HI-Z 定义为数据不再驱动的点。
4) 这些值由特性保证，并未在生产中经过 100% 测试。
5) 这些值由特性保证，并未在生产中经过 100% 测试。
6) 由设计保证
7) 如果在 t_{PU} 结束时 Reset# 有效，则器件将保持在复位状态，并且 t_{RH} 将决定 CS# 何时可能变为低电平。

8) t_{RP} 和 t_{RH} 的总和不能小于t_{RPH}.
9) 典型写入和擦除时间假定以下条件：25°C，V_{CC}= 1.8 V 和 3.0 V；棋盘数据唤醒类型码。
10) 任何OTP 写入命令传输的写入时间与 t_{PP}相同。
11) PRPPB_4_0 和 PRPPB_C_0 命令传输的写入时间与 t_{PP} 相同。ERPPB_0_0 事务的擦除时间与 t_{SE} 相同。
12) 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

8.1 时序波形

8.1.1 时序波形

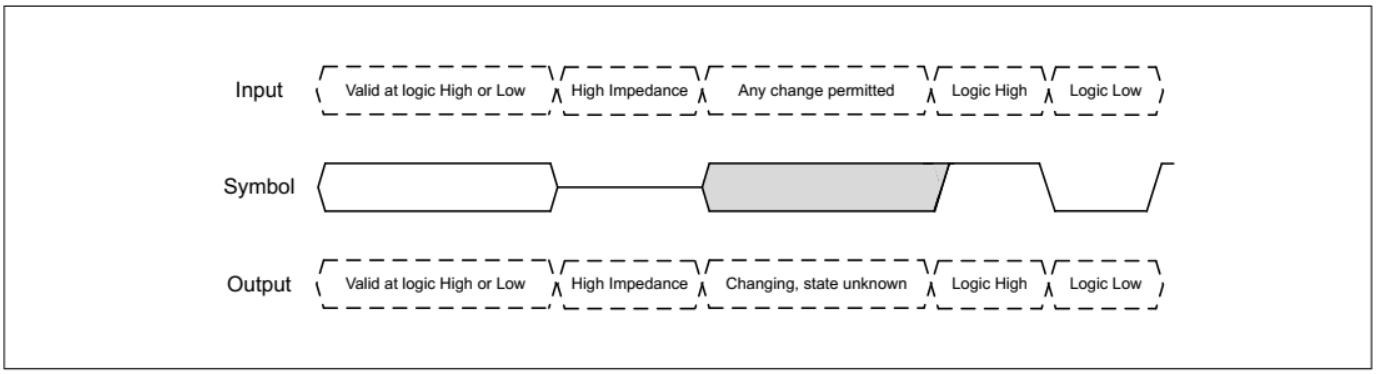

图 73 波形元素含义

8.1.2 时序参考电平

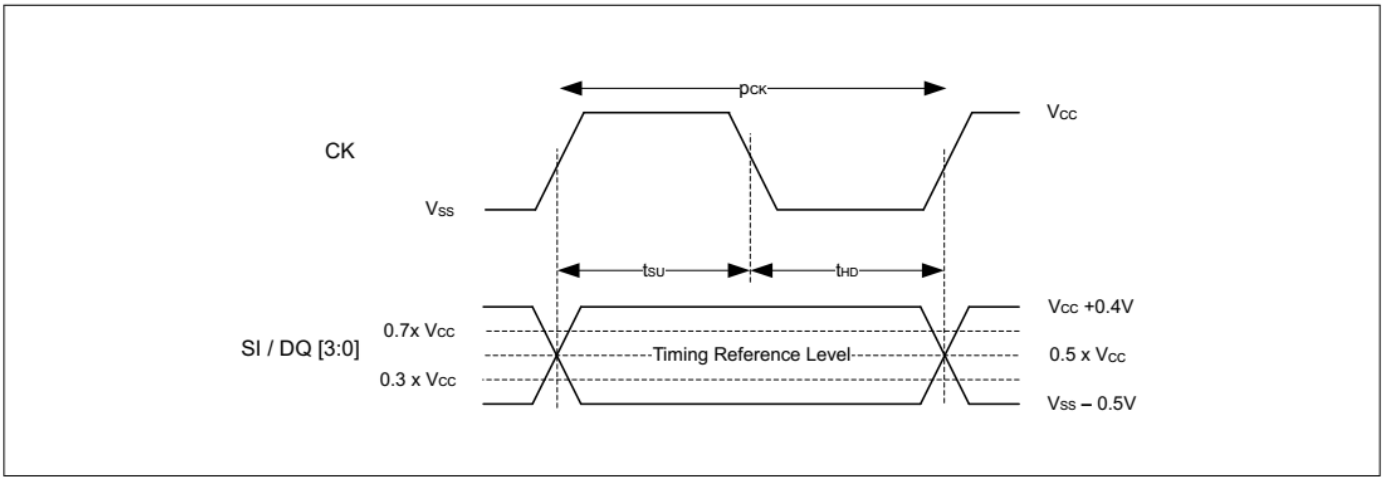

图 74 SDR输入参考电平

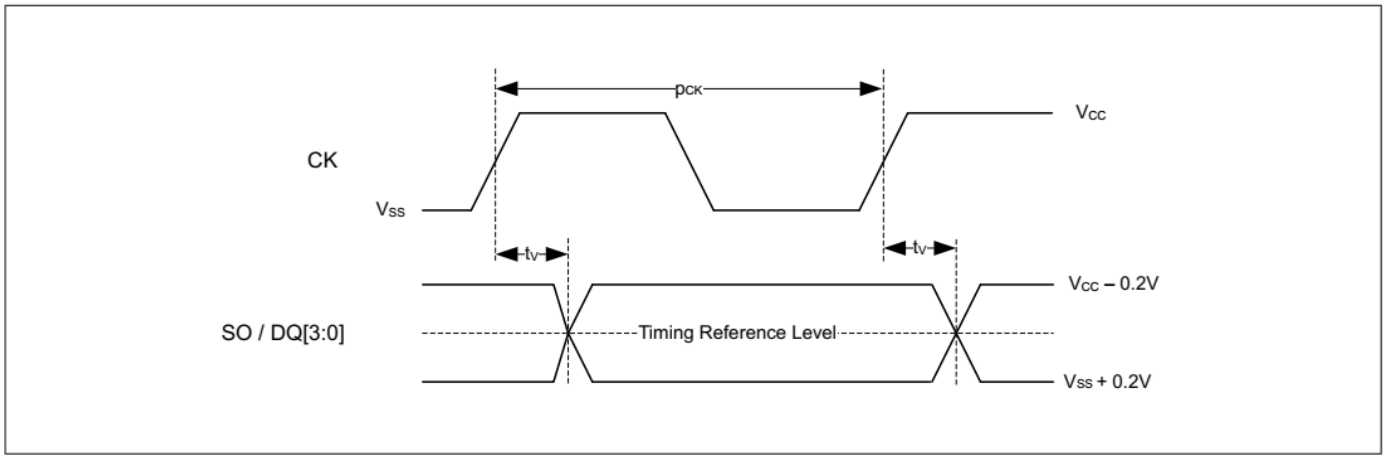

图 75　　SDR输出参考电平

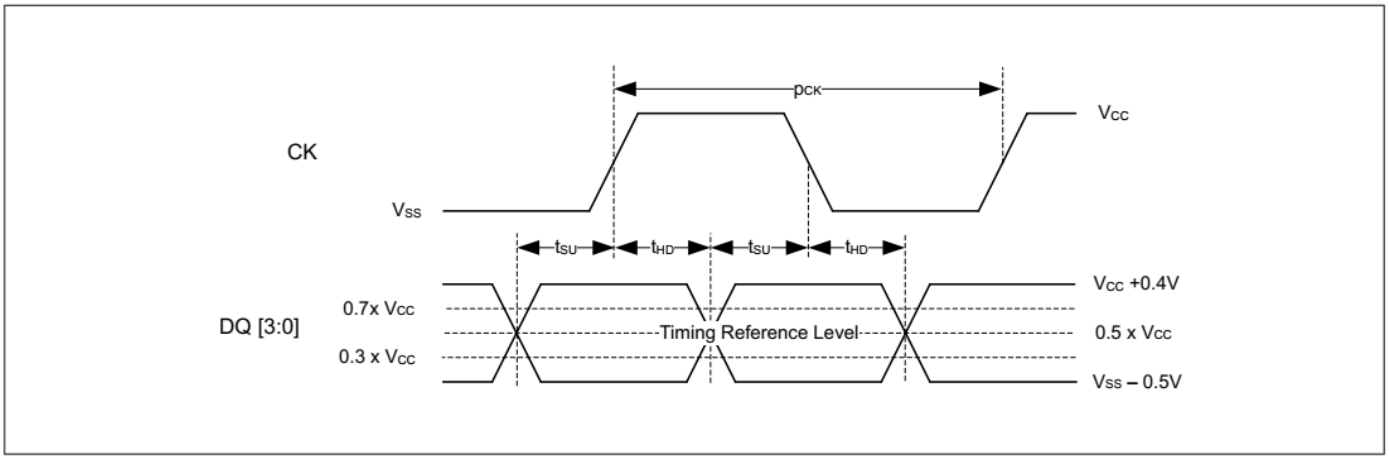

图 76　　DDR 输入参考电平

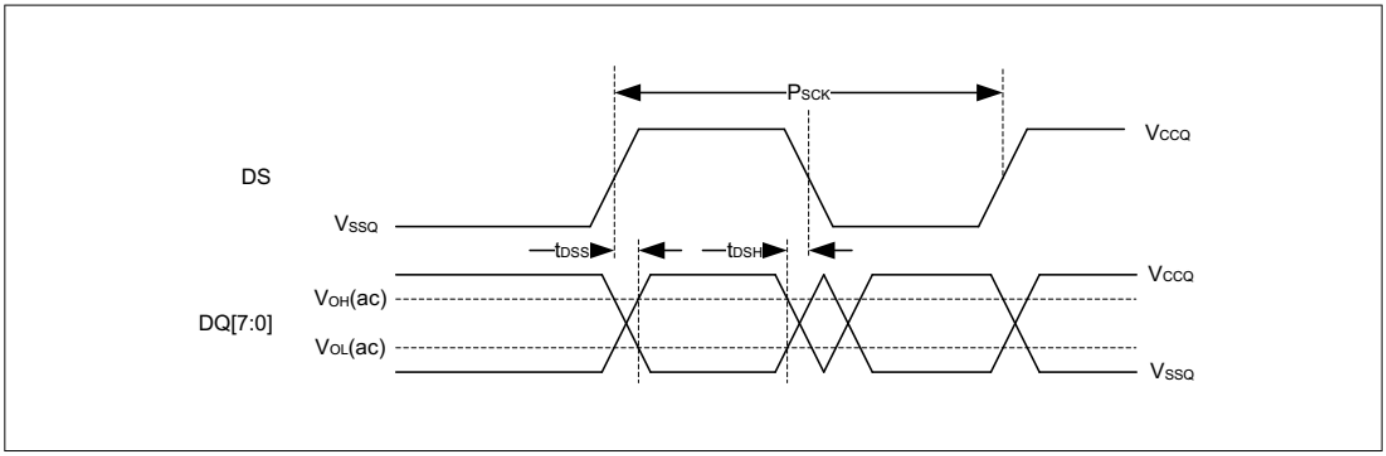

图 77　　DDR 输出参考电平

8.1.3 时钟时序

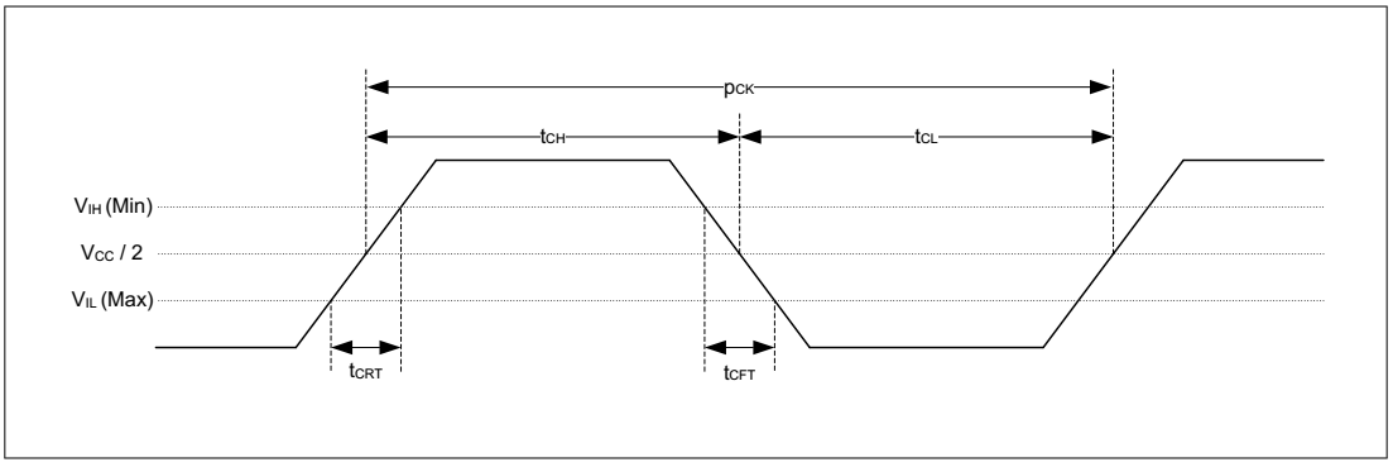

图 78 时钟时序

8.1.4 输入/输出时序

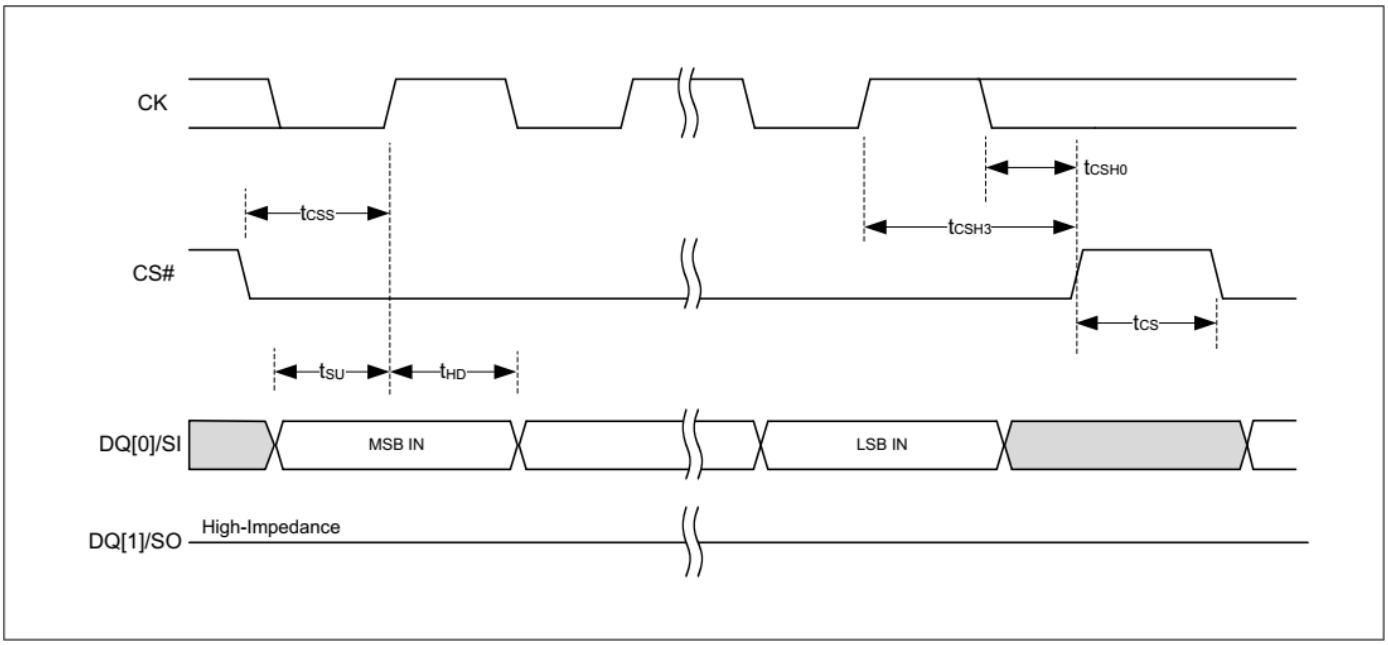

图 79 SPI输入时序

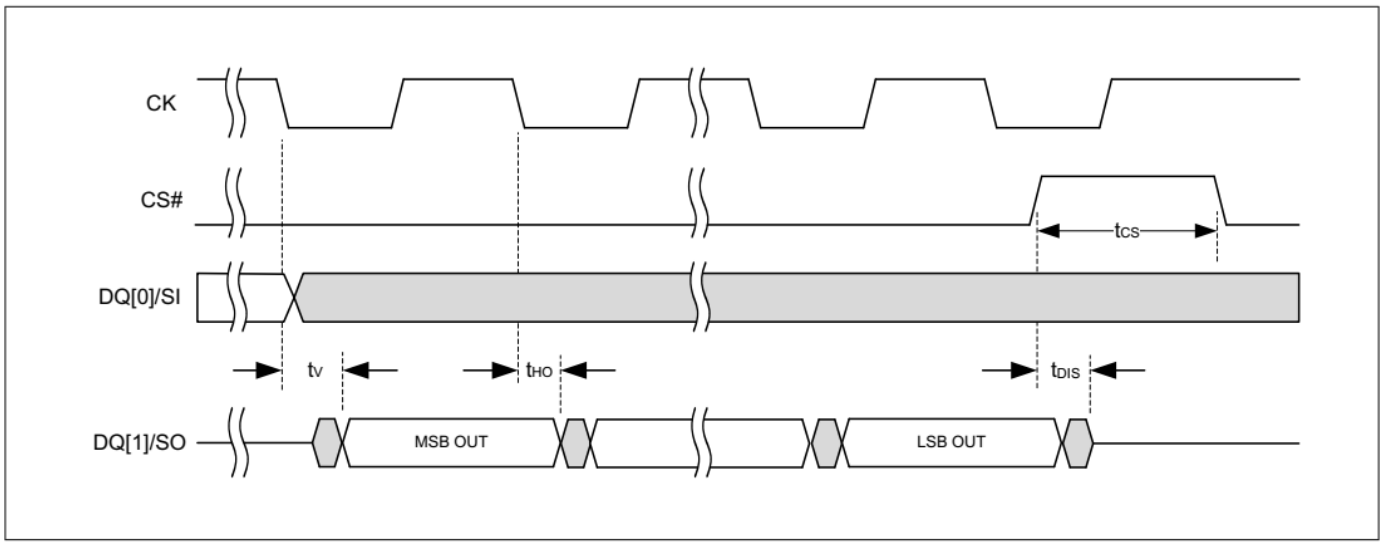

图 80　　SPI输出时序

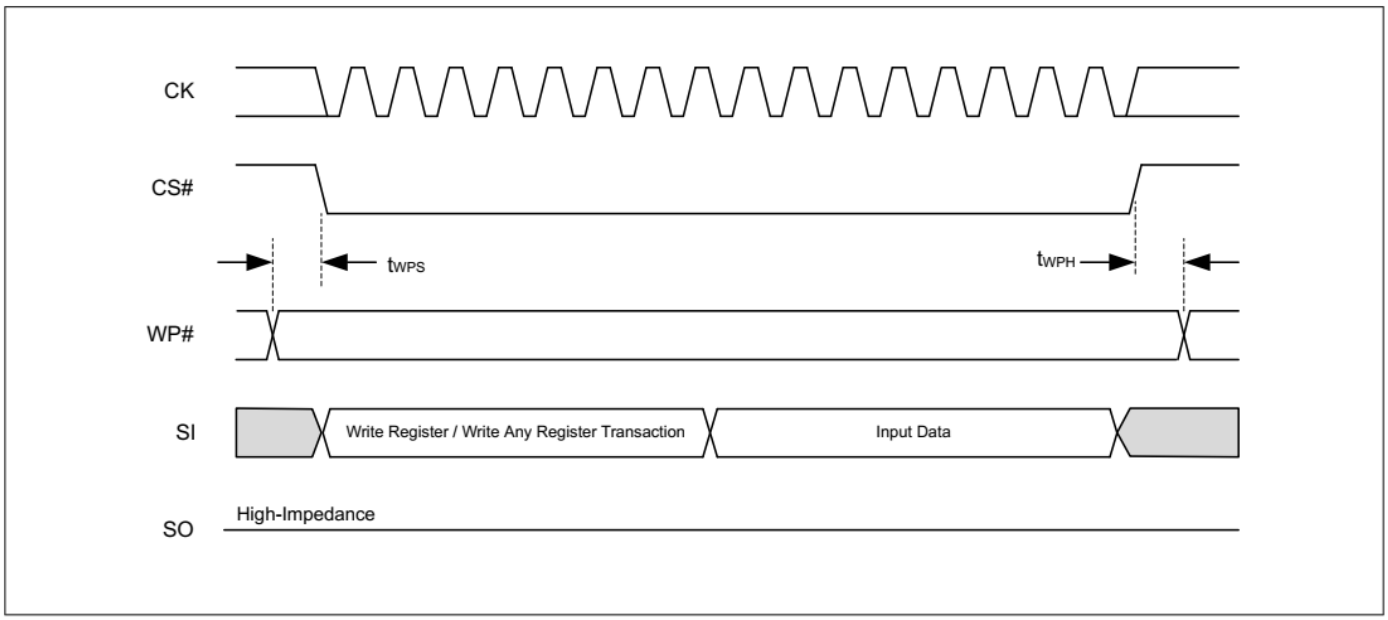

图 81　　WP#输入时序

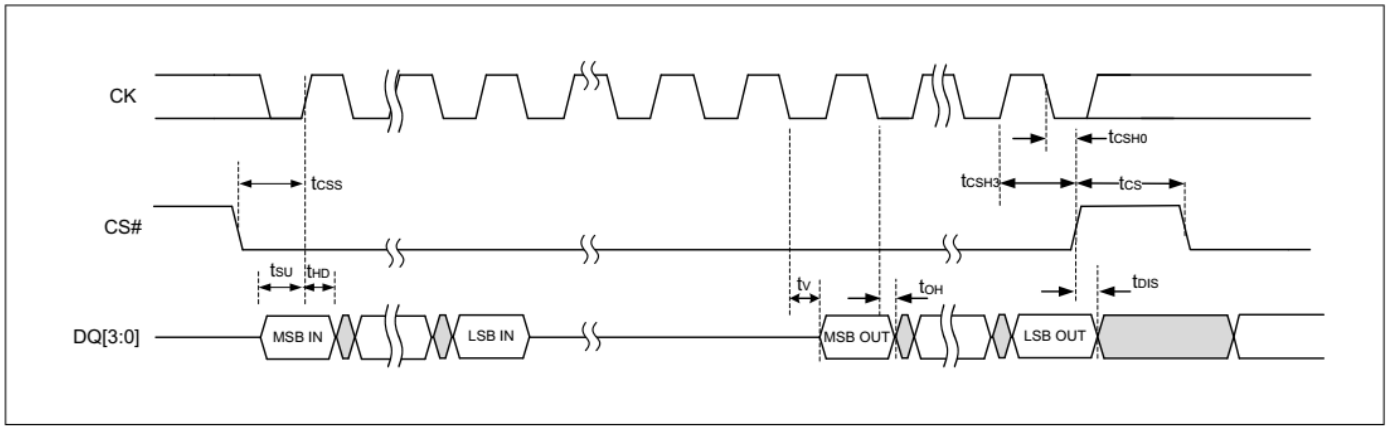

图 82　　Quad和QPI SDR输入输出时序

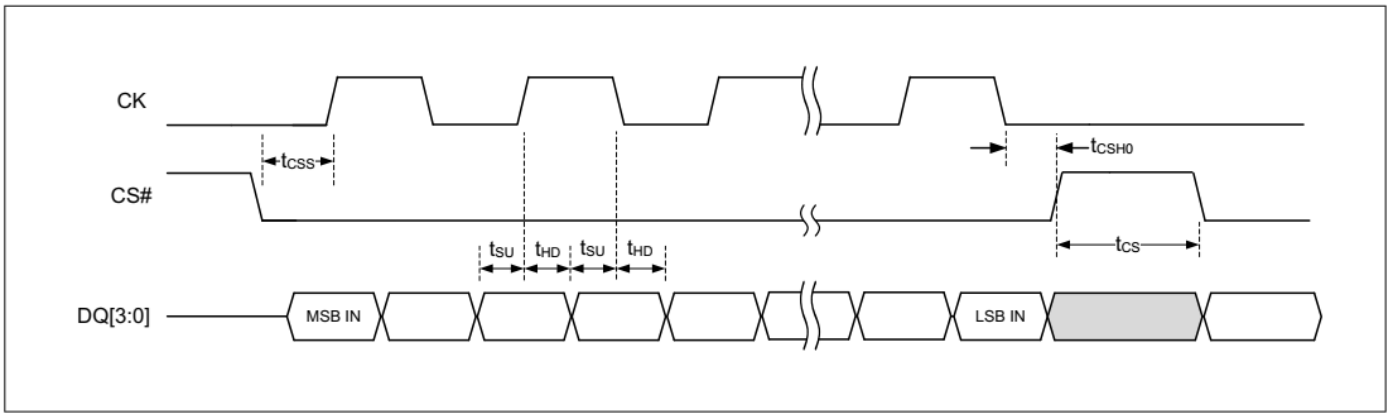

图 83　　Quad和QPI DDR输入时序

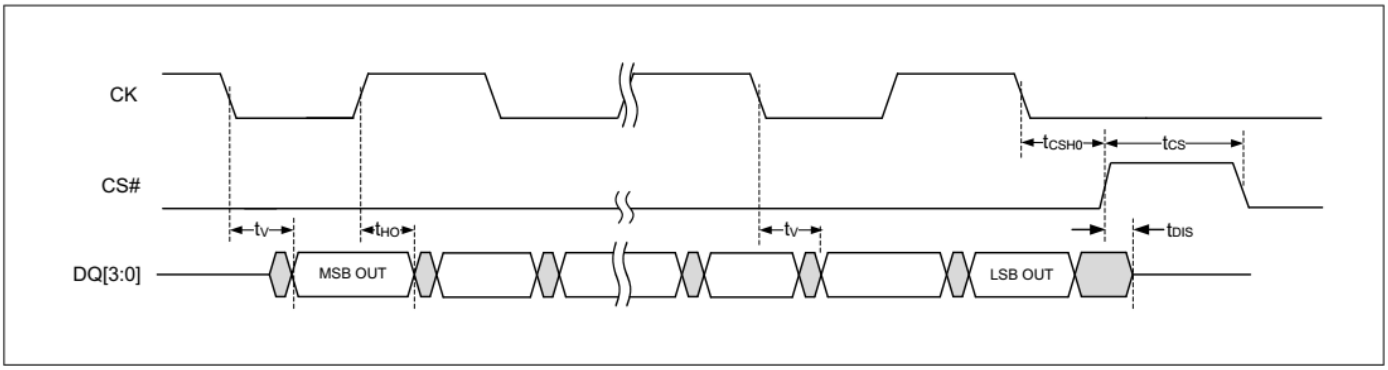

图 84　　Quad和QPI DDR输出时序

9 器件标识

9.1 JEDEC SFDP REV D

9.1.1 JEDEC SFDP Rev D 帧头表

表 91 JEDEC SFDP Rev D 帧头表

SFDP byte address	SFDP DWORD name	Data	Description
00 h	SFDP Header	53 h	This is the entry point for Read SFDP (5 Ah) command i.e., location zero within SFDP space ASCII “S”
01 h		46 h	ASCII “F”
02 h		44 h	ASCII “D”
03 h		50 h	ASCII “P”
04 h		08 h	SFDP Minor Revision (08 h = JEDEC JESD216 Revision D)
05 h		01 h	SFDP Major Revision (01 h = JEDEC JESD216 Revision D)This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06 h		03 h	Number of Parameter Headers (zero based, 03 h = 4 parameters)
07 h		FFh	SFDP Access Protocol (Backward Compatible)
08 h	1st Parameter Header	00 h	Parameter ID LSB (00 h = JEDEC SFDP Basic SPI Flash Parameter)
09 h		00 h	Parameter Minor Revision (00 h = JEDEC JESD216 Revision D)
0 Ah		01 h	Parameter Major Revision (01 h = The original major revision - all SFDP software is compatible with this major revision.
0 Bh		14 h	Parameter Table Length (14 h = 20 DWORDs are in the Parameter table)
0 Ch		00 h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned)JEDEC Basic SPI Flash parameter byte offset = 0100 h
0 Dh		01 h	Parameter Table Pointer Byte 1
0 Eh		00 h	Parameter Table Pointer Byte 2
0 Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)

（表格续下页……）

表 91　　（续） JEDEC SFDP Rev D 帧头表

SFDP byte address	SFDP DWORD name	Data	Description
10 h	2nd Parameter Header	84 h	Parameter ID LSB (84 h = 4-Byte Address Instruction Table)
11 h		00 h	Parameter Table Minor Revision (00 h = JEDEC JESD216 Revision D)
12 h		01 h	Parameter Table Major Revision (01 h = JEDEC JESD216 Revision D)
13 h		02 h	Parameter Table Length (2 h = 2 DWORDs are in the Parameter table)
14 h		50 h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned)4-Byte Address Instruction Table byte offset = 0150 h address
15 h		01 h	Parameter Table Pointer Byte 1
16 h		00 h	Parameter Table Pointer Byte 2
17 h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18 h	3rd Parameter Header	81 h	Parameter ID LSB (81 h = JEDEC Sector Map)
19 h		00 h	Parameter Table Minor Revision (00 h = JEDEC JESD216 Revision D)
1 Ah		01 h	Parameter Table Major Revision (01 h = JEDEC JESD216 Revision D)
1 Bh		16 h	Parameter Table Length (16 h = 22 DWORDs are in the Parameter table)
1 Ch		C8h	Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned)JEDEC Sector Map = 1C8h address
1 Dh		01 h	Parameter Table Pointer Byte 1
1 Eh		00 h	Parameter Table Pointer Byte 2
1 Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
20 h	4th Parameter Header	87 h	Parameter ID LSB (87 h = JEDEC Status, Control and Configuration Register Map)
21 h		00 h	Parameter Table Minor Revision (00 h = JEDEC JESD216 Revision D)
22 h		01 h	Parameter Table Major Revision (01 h = JEDEC JESD216 Revision D)
23 h		1 Ch	Parameter Table Length (1 Ch = 28 DWORDs are in the Parameter table)

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表 91　（续）JEDEC SFDP Rev D 帧头表

SFDP byte address	SFDP DWORD name	Data	Description
24 h		58 h	Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned)JEDEC Status, Control and Configuration Register Map = 158 h address
25 h		01 h	Parameter Table Pointer Byte 1
26 h		00 h	Parameter Table Pointer Byte 2
27 h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

9.1.2　JEDEC SFDP Rev D 参数表

对于 SFDP 数据结构，有三个独立的参数表。其中两个表具有固定长度，一个表具有可变结构和长度，具体取决于器件容量订购部件号 (OPN)。参数表见表 92。

表 92　JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
100 h	JEDEC Basic Flash Parameter DWORD-1	E7h	Bits 7:5 = unused = 111b Bit 4 = 50 h is Volatile Status Register write instruction and Status Register is default = 0b Bit 3 = Block Protect Bits are nonvolatile/volatile nonvolatile = 0b Bit 2 = Program Buffer > 64Bytes = 1b Bits 1:0 = Uniform 4 KB erase is unavailable = 11b
101 h		20 h	Bits 15:8 = 4KB erase opcode = 20 h
102 h		FAh	Bit 23 = Unused = 1b Bit 22 = Supports Quad Out (1-1-4) Read = Yes = 1b Bit 21 = Supports Quad I/O (1-4-4) Read = Yes =1b Bit 20 = Supports Dual I/O (1-2-2) Read = Yes = 1b Bit 19 = Supports DDR = Yes = 1b Bit 18:17 = Number of Address Bytes = 3- or 4-Bytes = 01b Bit 16 = Supports Dual Out (1-1-2) Read = No = 0b
103 h		FFh	Bits 31:24 = Unused = FFh
104 h	JEDEC Basic Flash Parameter DWORD-2	FFh20h	Density in bits, zero based, 512 Mb = 1FFFFFFFh
105 h		FFh00h	

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
106 h		FFh00h	Density in bits, zero based, 1 Gb = 3FFFFFFFh
107 h		1Fh (512 Mb) 3 Fh (1 Gb) 3 Fh(1 Gb) 7 Fh (2 Gb) 10 (4 Gb)	
108 h	JEDEC Basic Flash Parameter DWORD-3	48h	Bits 7:5 = number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = number of Quad I/O Dummy cycles = 01000b (Initial Delivery State)
109 h		EBh	Quad I/O instruction code
10 Ah		08 h	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b
10 Bh		6 Bh	1-1-4 Quad Out instruction code = 6 Bh
10 Ch	JEDEC Basic Flash Parameter DWORD-4	00 h	Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 00000b
10 Dh		FFh	Dual Out instruction code
10 Eh		88 h	Bits 23:21 = number of Dual I/O (1-2-2) Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 01000b (Initial Delivery State)
10 Fh		BBh	Dual I/O instruction code
110 h	JEDEC Basic Flash Parameter DWORD-5	FEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = Yes = 1b Bits 3:1 RFU = 111b Bit 0 = 2-2-2 not supported = 0b
111 h		FFh	Bits 15:8 = RFU = FFh
112 h		FFh	Bits 23:16 = RFU = FFh
113 h		FFh	Bits 31:24 = RFU = FFh
114 h	JEDEC Basic Flash Parameter DWORD-6	FFh	Bits 7:0 = RFU = FFh
115 h		FFh	Bits 15:8 = RFU = FFh

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
116 h		00 h	Bits 23:21 = number of 2-2-2 Mode cycles = 000b Bits 20:16 = number of 2-2-2 Dummy cycles = 00000b
117 h		FFh	2-2-2 instruction code
118 h	JEDEC Basic Flash Parameter DWORD-7	FFh	Bits 7:0 = RFU = FFh
119 h		FFh	Bits 15:8 = RFU = FFh
11 Ah		48 h	Bits 23:21 = Number of QPI Mode cycles = 010b Bits 20:16 = Number of QPI Dummy cycles = 01000b
11 Bh		EBh	QPI mode Quad I/O (4-4-4) instruction code
11 Ch	JEDEC Basic Flash Parameter DWORD-8	0 Ch	Erase type 1 size 2^N Bytes = 2^12 Bytes = 4 KB (Initial Delivery State)
11 Dh		20 h	Erase type 1 instruction
11 Eh		00 h	Erase type 2 size 2^N Bytes = Not Supported
11 Fh		FFh	Erase type 2 instruction = Not Supported = FFh
120 h	JEDEC Basic Flash Parameter DWORD-9	00 h	Erase type 3 size 2^N Bytes = Not Supported
121 h		FFh	Erase type 3 instruction = Not Supported = FFh
122 h		12 h	Erase type 4 size 2^N Bytes = 2^18 Bytes = 256KB
123 h		D8h	Erase type 4 instruction = D8h
124 h	JEDEC Basic Flash Parameter DWORD-10	23 h	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 29:25 = Erase type 4 Erase, Typical time count = 00101b (512M & 1G) Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU)
125 h		FAh	
126 h		FFh	

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表 92　　（续）JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
127 h		8 Bh	Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 15:11 = Erase type 2 Erase, Typical time count = 11111b (RFU) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16mS = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 00010b (typ erase time = count + 1 * units = 3 * 16 ms = 48 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) – 1 = 0011b
128 h	JEDEC Basic Flash Parameter DWORD-11	82 h	Bits 31 = Reserved = 1b Bits 30:29 = Chip Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b Bits 28:24 = Chip Erase Typical time count = 00011b (512M), and 00110b (1G) Bits 23:19 = Byte Program Typical Time, additional byte = 11111b Bits 18:14 = Byte Program Typical Time, first byte = 11111b Bits 13 = Page Program Typical Time unit (0: 8 µs, 1: 64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical Time Count = 00111 Bits 7:4 = Page Size (256B) = 2^N bytes = 1000h Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] – 1 = 0010b
129 h		E7	
12 Ah		FFh	
12 Bh		E3h for 512M E6h for 1G	
12 Ch	JEDEC Basic Flash Parameter DWORD-12	ECh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) = 64 µs = 8 µs = 10b (512M & 1Gb) Bits 28:24 = Suspend in-progress erase max latency count = 01001b Bits 23:20 = Erase resume to suspend interval count = 0001b
12 Dh		23 h	
12 Eh		19 h	

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
12 Fh		49 h	Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64µs) = 64 µs = 8 µs = 10b (512M & 1G) Bits 17:13 = Suspend in-progress program max latency count = 01001b Bits 12:9 = Program resume to suspend interval count = 0001b Bit 8 = Reserved = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b
130 h	JEDEC Basic Flash Parameter DWORD-13	8 Ah	Bits 31:24 = Erase Suspend Instruction = 75 h Bits 23:16 = Erase Resume Instruction = 7 Ah Bits 15:8 = Program Suspend Instruction = 85 h Bits 7:0 = Program Resume Instruction = 8 Ah
131 h		85 h	
132 h		7 Ah	
133 h		75 h	

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
134 h	JEDEC Basic Flash Parameter DWORD-14	F7h	Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). Bits 1:0 = RFU = 11b
135 h		66 h	Bit 31 = DPD Supported = supported = 0 Bits 30:23 = Enter DPD Instruction = B9h Bits 22:15 = Exit DPD Instruction not supported = 00 h Bits 14:13 = Exit DPD to next operation delay units = (00b: 128ns, 01b: 1µs, 10b: 8 µs, 11b: 64 µs) = 64 µs = 11b Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count+1) * units = (6 + 1) * 64 µs = 448 µs
136 h		80 h	
137 h		5 Ch	
138 h	JEDEC Basic Flash Parameter DWORD-15	8 Ch	Bits 31:24 = RFU = FFh Bit 23 =HOLD or RESET Disable = Supported = 1 Bits 22:20 = Quad Enable Requirements = 101b = 101b: QE is bit 1 of the Status Register-2. Status Register-1 is read using Read Status instruction 05 h. Status Register-2 is read using instruction 35 h. QE is set via Write Status instruction 01 h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 = 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0] = Axh + 1xxxb: RFU = 1101b
139 h		D6h	
13 Ah		DDh	

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表 92　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
13 Bh		FFh	Bits 15:10 = 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00 h will terminate this mode at the end of the current read operation + xx_x1xxb: RFU + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxxb: Mode Bit[7:0] != Axh + 1x_x1xxb: RFU = 11_0101b Bit 9 = 0-4-4 mode supported = 1b Bits 8:4 = 4-4-4 mode enable sequences = x_xx1xb: Issue instruction 38h. + x_1xxxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 01000 Bits 3:0 = 4-4-4 mode disable sequences = xxx1b: Issue FFh instruction + xx0xb: Issue F5h instruction + x1xxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65 h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. + 1xxxb: Issue the Soft Reset 66/99 sequence = 1100
13 Ch	JEDEC Basic Flash Parameter DWORD-16	F9h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b: issue instruction B7h (preceding write enable not required)
13 Dh		38 h	
13 Eh		F8h	

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
13 Fh		A1h	+ xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Refer to the vendor datasheet for the instruction set definition. + 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing = xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_1110_0000b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: Issue reset enable instruction 66h, then issue reset instruction 99 h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. + 1x_xxxxb: Exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 111000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Nonvolatile Register and Write Enable Instruction for Status Register 1 = xxx_xxx1b: Nonvolatile Status Register 1, powers-up to last written value, use instruction 06h to enable write. + xxx_1xxxb: Nonvolatile/Volatile Status Register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to nonvolatile status register. Volatile status register may be activated after power-up to override the nonvolatile status register, use instruction 50h to enable

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
			write and activate the volatile status register. + xx1_xxxxb: Status Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1111001b
140 h	JEDEC Basic Flash Parameter DWORD-17	00 h	Not Supported
141 h			
142 h			
143 h			
144 h	JEDEC Basic Flash Parameter DWORD-18	00 h	Bits 31: 24 = 00 h Bit 23 = 1b = JEDEC SPI Protocol Reset implemented as described in JESD252 Bits 22:18 = 01111b Bits 17:0 = 000 h
145 h		00 h	
146 h		BCh	
147 h		00 h	
148 h	JEDEC Basic Flash Parameter DWORD-19	00 h	Not Supported
149 h			
14 Ah			
14 Bh			
14 Ch	JEDEC Basic Flash Parameter DWORD-20	F7h	Bits 31:16 = Not Supported = 1111_1111_1111_1111b Bit 15:12 = 1111b = 4S-4D-4D Data Strobe is not supported Bit 11:8 = 0101b = 100 MHz 4S-4D-4D Bit 7:4 = 1111b = 4S-4S-4S Data Strobe is not supported Bit 0:3 = 0111b = 166 MHz 4S-4S-4S
14 Dh		F5h	
14 Eh		FFh	
14 Fh		FFh	
150 h	JEDEC 4-Byte Address Instructions Parameter DWORD-1	7 Bh	Supported = 1, Not Supported = 0 Bits 31:25 = Reserved = 1111_111b Bit 24 = Support for (1-8-8) Page Program Command, Instruction = 8Eh = 0b Bit 23 = Support for (1-1-8) Page Program Command, Instruction = 84 h = 0b
151 h		92 h	
152 h		0 Fh	

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
153 h		FEh	Bit 22 = Support for (1-8-8) DTR READ Command, Instruction = FDh = 0b Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7 Ch = 0b Bit 19 = Support for nonvolatile individual sector lock write command, Instruction = E3h = 1b Bit 18 = Support for nonvolatile individual sector lock read command, Instruction = E2h = 1b Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1b Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1b Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 1b Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b Bit 12 = Support for Erase Command – Type 4 = 1b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 0b Bit 9 = Support for Erase Command – Type 1 = 1b Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3 Eh = 0b Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34 h = 0b Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12 h = 1b

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
			Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 1b Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6 Ch = 1b Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 1b Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3 Ch = 0b Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0 Ch = 1b Bit 0 = Support for (1-1-1) READ Command, Instruction = 13 h = 1b
154 h	JEDEC 4-Byte Address Instructions Parameter DWORD-2	21 h	Bits 31:24 = D8h/DCh = Instruction fo Erase Type 4 Bits 23:16 = Instruction for Erase Type 3: RFU Bits 15:8 = Instruction for Erase Type 2: RFU Bits 7:0 = 20 h/21 h = Instruction for Erase Type 1
155 h		FFh	
156 h		FFh	
157 h		DCh	
158 h	Status, Control and Configuration Register Map DWORD-1	00 h	Bits 31:0 = Address offset for volatile registers = 00800000 h
159 h		00 h	
15 Ah		80 h	
15 Bh		00 h	
15 Ch	Status, Control and Configuration Register Map DWORD-2	00 h	Bits 31:0 = Address offset for nonvolatile registers = 00000000 h
15 Dh		00 h	
15 Eh		00 h	
15 Fh		00 h	
160 h	Status, Control and Configuration Register Map DWORD-3	C0h	Bit 31 = Generic Addressable Read Status/Control register command supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/ Write Status/Control register commands = 3 byte (default) = 10b
161 h		FFh	
162 h		C3h	

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表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
163 h		EBh	Bit 27:26 = Use the number of bits as defined in bits 3:0 in this DWORD = 10b Bit 25:22 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b Bit 21:18 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 0000b Bit 17:14 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode note supported = 1111b Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode note supported = 1111b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode note supported = 1111b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b
164 h	Status, Control and Configuration Register Map DWORD-4	C8h	Bit 31 = Generic Addressable Read Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for nonvolatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/ Write Status/Control register
165 h		FFh	
166 h		E3h	

（表格续下页.....）

表 92 （续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
167 h		EBh	commands for nonvolatile registers = 3 byte (default) = 10b Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for nonvolatile registers in (1S-1S-1S) mode not supported = 10b Bit 25:22 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b Bit 21:18 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 1000b Bit 17:14 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode note supported = 1111b Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode note supported = 1111b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode note supported = 1111b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non volatile registers in (1S-1S-1S) mode = 1000b
168 h	Status, Control and Configuration Register Map DWORD-5	00 h	Bits 7:0 = Command used for write access = read only = 00 h
169 h		65 h	Bits 15:8 = Command used for read access = 65 h
16 Ah		00 h	Bits 23:16 = Address of register where WIP is located = 00 h (status reg -1 volatile)

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
16 Bh		90 h	Bit 31 = Write In Progress (WIP) bit is supported = 1b Bit 30 = Write In Progress polarity, WIP = 1 means write is in progress = 0b Bits 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b
16 Ch	Status, Control and Configuration Register Map DWORD-6	06 h	Bits 7:0 = Command used for write access = 06 h
16 Dh		05 h	Bits 15:8 = Command used for read access = 05 h
16 Eh		00 h	Bits 23:16 = Address of register where WEL is located = 00h (status reg -1 volatile)
16 Fh		A1h	Bit 31 = Write Enable (WEL) bit is supported = 1b Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b Bits 29 = Write command is a direct command to set WEL bit = 1b Bits 28 = Bit is accessed by direct commands to set WEL bit = 0b Bit 27 = Local address for WEL bit is found in last byte of the address = 0b Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b
170 h	Status, Control and Configuration Register Map DWORD-7	00 h	Bits 7:0 = Command used for write access = read only = 00 h = Read Only
171 h		65 h	Bits 15:8 = Command used for read access = 65 h
172 h		00 h	Bits 23:16 = Address of register where Erase Error is located = 00 h

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表 92　　（续）JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
173 h		96 h	Bit 31 = Program Error bit supported = 1b Bit 30 = Positive polarity (Program Error = 0 means no error, Program Error = 1 means last Program operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = 0b Bits 26:24 = Bit location of Program Error bit in register = bit [6] = 110b
174 h	Status, Control and Configuration Register Map DWORD-8	00 h	Bits 7:0 = Command used for write access = read only = 00 h = Read Only
175 h		65 h	Bits 15:8 = Command used for read access = 65 h
176 h		00 h	Bits 23:16 = Address of register where Erase Error is located = 00 h
177 h		95 h	Bit 31 = Erase Error bit supported = 1b Bit 30 = Positive polarity Erase Error = 0 means no error, Erase Error = 1 means last erase operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Reserved = 0b Bits 26:24 = Bit location of erase Error bit in register = bit [5] = 101b
178 h	Status, Control and Configuration Register Map DWORD-9	71 h	Bits 7:0 = Command used for write access = 71 h
179 h		65 h	Bits 15:8 = Command used for read access = 65 h
17 Ah		03 h	Address of register where wait states bits are located = 800003 h (Configuration Reg - 2 volatile)

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
17 Bh		D0h	Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b
17 Ch	Status, Control and Configuration Register Map DWORD-10	71 h	Bits 7:0 = Command used for write access = 71 h
17 Dh		65 h	Bits 15:8 = Command used for read access = 65 h
17 Eh		03 h	Address of register where wait states bits are located = 03 h (Configuration Reg - 2 Nonvolatile)
17 Fh		D0h	Bit 31 = Variable number of dummy cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b
180 h	Status, Control and Configuration Register Map DWORD-11	00 h	Bit 31 = 30 dummy cycles supported = 0b Bit 30:26 = Bit pattern used to set 30 dummy cycles = 00000b Bit 25 = 28 dummy cycles supported = 0b Bit 24:20 = Bit pattern used to set 28 dummy cycles = 00000b Bit 19 = 26 dummy cycles supported = 0b Bit 18:14 = Bit pattern used to set 26 dummy cycles = 00000b
181 h		00 h	
182 h		00 h	

（表格续下页.....）

表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
183 h		00 h	Bit 13 = 24 dummy cycles supported = 0b Bit 12:8 = Bit pattern used to set 24 dummy cycles = 00000b Bit 7 = 22 dummy cycles supported = 0b Bit 6:2 = Bit pattern used to set 22 dummy cycles = 00000b Bits 1:0 = Reserved = 00b
184 h	Status, Control and Configuration Register Map DWORD-12	B0h	Bit 31 = 20 dummy cycles supported = 0b Bit 30:26 = Bit pattern used to set 20 dummy cycles = 00000b Bit 25 = 18 dummy cycles supported = 0b Bit 24:20 = Bit pattern used to set 18 dummy cycles = 00000b Bit 19 = 16 dummy cycles supported = 0b Bit 18:14 = Bit pattern used to set 16 dummy cycles = 00000b Bit 13 = 14 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 14 dummy cycles = 01110b Bit 7 = 12 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 12 dummy cycles = 01100b Bits 1:0 = Reserved = 00b
185 h		2 Eh	
186 h		00 h	
187 h		00 h	
188 h	Status, Control and Configuration Register Map DWORD-13	88 h	Bit 31 = 10 dummy cycles supported = 1b Bit 30:26 = Bit pattern used to set 10 dummy cycles = 01010b Bit 25 = 8 dummy cycles supported = 1b Bit 24:20 = Bit pattern used to set 8 dummy cycles = 01000b Bit 19 = 6 dummy cycles supported = 1b Bit 18:14 = Bit pattern used to set 6 dummy cycles = 00110b
189 h		A4h	
18 Ah		89 h	

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
18 Bh		AAh	Bit 13 = 4 dummy cycles supported = 1b Bit 12:8 = Bit pattern used to set 4 dummy cycles = 00100b Bit 7 = 2 dummy cycles supported = 1b Bit 6:2 = Bit pattern used to set 2 dummy cycles = 00010b Bits 1:0 = Reserved = 00b
18 Ch	Status, Control and Configuration Register Map DWORD-14	71 h	Bits 7:0 = Command used for write access = 71 h
18 Dh		65 h	Bits 15:8 = Command used for read access = 65 h
18 Eh		03 h	Address of register where wait states bits are located = 800003h (Configuration Reg - 2 Volatile)
18 Fh		96 h	Bit 31 = QPI Mode Enable Volatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [6] = 110b
190 h	Status, Control and Configuration Register Map DWORD-15	71 h	Bits 7:0 = Command used for write access = 71 h
191 h		65 h	Bits 15:8 = Command used for read access = 65 h
192 h		03 h	Address of register where wait states bits are located = 03 h (Configuration Reg - 2 Nonvolatile)

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表 92　　（续） JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
193 h		96 h	Bit 31 = QPI Mode Enable Nonvolatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [6] = 110b
194 h	Status, Control and Configuration Register Map DWORD-16	00 h	Not Supported
195 h		00 h	
196 h		00 h	
197 h		00 h	
198 h	Status, Control and Configuration Register Map DWORD-17	00 h	
199 h		00 h	
19 Ah		00 h	
19 Bh		00 h	
19 Ch	Status, Control and Configuration Register Map DWORD-18	00 h	
19 Dh		00 h	
19 Eh		00 h	
19 Fh		00 h	
1A0h	Status, Control and Configuration Register Map DWORD-19	00 h	Not Supported
1A1h		00 h	
1A2h		00 h	
1A3h		00 h	
1A4h	Status, Control and Configuration Register Map DWORD-20	00 h	
1A5h		00 h	
1A6h		00 h	
1A7h		00 h	
1A8h	Status, Control and Configuration Register Map DWORD-21	00 h	
1A9h		00 h	
1AAh		00 h	

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表 92　　（续）JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
1ABh		00 h	
1ACh	Status, Control and Configuration Register Map DWORD-22	00 h	
1ADh		00 h	
1AEh		00 h	
1AFh		00 h	
1B0h	Status, Control and Configuration Register Map DWORD-23	00 h	
1B1h		00 h	
1B2h		00 h	
1B3h		00 h	
1B4h	Status, Control and Configuration Register Map DWORD-24	00 h	
1B5h		00 h	
1B6h		00 h	
1B7h		00 h	
1B8h	Status, Control and Configuration Register Map DWORD-25	00 h	Not Supported
1B9h		00 h	
1BAh		00 h	
1BBh		00 h	
1BCh	Status, Control and Configuration Register Map DWORD-26	71 h	Bits 7:0 = Command used for write access = 71 h
1BDh		65 h	Bits 15:8 = Command used for read access = 65 h
1BEh		05 h	Address of register where Output Driver Strength volatile bits are located = 800005h (Configuration Reg - 4 Volatile)
1BFh		D5h	Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b
1C0h	Status, Control and Configuration Register Map DWORD-27	71 h	Bits 7:0 = Command used for write access = 71 h

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表 92　　（续）JEDEC SFDP Rev D 参数表

SFDP byte address	SFDP DWORD name	Data	Description
1C1h		65 h	Bits 15:8 = Command used for read access = 65 h
1C2h		05 h	Address of register where Output Driver Strength volatile bits are located = 05 h (Configuration Reg - 4 Nonvolatile)
1C3h		D5h	Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bits 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Not supported = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b
1C4h	Status, Control and Configuration Register Map DWORD-28	00 h	Bits 7:0 = Reserved = 00 h
1C5h		00 h	Bits 15:8 = Reserved = 00 h
1C6h		A0h	Bits 31:29 = Bit pattern to support Driver type 0 = 45 Ohm = 000b Bits 28:26 = Bit pattern to support Driver type 1 = 30 Ohm = 101b Bits 25:23 = Bit pattern to support Driver type 2 = 60 Ohm = 011b Bits 22:20 = Bit pattern to support Driver type 3 = 90 Ohm = 010b Bits 19:17 = Bit pattern to support Driver type 4 = Not supported = 000b Bit 16 = Reserved = 0b
1C7h		15 h	

扇区映射参数表说明

表 93 提供了一种方法来识别器件地址映射的配置方式，并为每个支持的配置提供扇区映射。这是通过定义一系列指令来读取影响地址映射选择的相关配置寄存器位来完成的。当必须读取多个配置位时，所有位都连接成一个索引值，用于选择当前地址映射。

为了识别器件中的扇区图配置，按以下 MSb 到 LSb 的顺序读取以下配置位，以形成配置图索引值：

- CFR3V[3] - 0 = 混合架构，1 = 统一架构
- CFR1V[6] - 0 = 4KB 参数组合在一起，1 = 4KB 扇区分为底部和顶部
- CFR1V[2] - 0 = 4KB 参数扇区位于底部，1 = 4KB 参数扇区位于顶部
- 某些配置位的值可能会使其他配置位的值变得无关紧要（无需考虑），因此并非所有可能的索引值

组合都能定义有效的地址映射。SFDP 扇区映射参数表仅支持选定的配置位组合（参见表 94）。使用此 SFDP 参数表确定扇区映射时，配置扇区地址映射时不得使用其他组合。支持以下索引值组合。

表 93　　扇区映射参数

CFR3V[3]	CFR1V[6]	CFR1V[2]	Index value	Description
0	0	0	00 h	4 KB sectors at bottom with remainder 256 KB sectors
0	0	1	01 h	4 KB sectors at top with remainder 256 KB sectors
0	1	0	02 h	4 KB sectors split between top and bottom with remainder 256 KB sectors
1	0	0	04 h	Uniform 256 KB sectors

表 94　　JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1C8h	JEDEC Sector Map Parameter DWORD-1 Config. Detect-1	FCh	Config. Detect -1 Uniform 256 KB Sectors or Hybrid Sectors Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for UNHYSA value 0 = Hybrid map with 4 KB parameter sectors 1 = Uniform map Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65 h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0
1C9h		65 h	
1CAh		FFh	
1CBh		08 h	
1CCh	JEDEC Sector Map Parameter DWORD-2 Config. Detect-1	04 h	Bits 31:0 = Address Value Configuration Register 3 (bit 3) = 00800004h
1CDh		00 h	
1CEh		80 h	
1CFh		00 h	
1D0h	JEDEC Sector Map Parameter DWORD-3 Config. Detect-2	FCh	Config. Detect-2 4 KB Hybrid Sectors Split between Top and Bottom Bits 31:24 = Read data mask = 0100_0000b: Select bit 6 of the data byte for SP4KBS value 0 = 4 KB parameter sectors are grouped together
1D1h		65h	
1D2h		FFh	

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表 94　　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1D3h		40 h	1 = 4 KB parameter sectors are split between High and Low Addresses Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = Not the end descriptor = 0
1D4h	JEDEC Sector Map Parameter DWORD-4 Config. Detect-2	02 h	Bits 31:0 = Address Value Configuration Register 1 (bit 6) = 00800002h
1D5h		00 h	
1D6h		80 h	
1D7h		00 h	
1D8h	JEDEC Sector Map Parameter DWORD-5 Config. Detect-3	FDh	Config Detect-3 4 KB Hybrid Sectors on Top or Bottom Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TB4KBS value 0 = 4 KB parameter sectors at bottom 1 = 4 KB parameter sectors at top Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65 h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = End of command descriptor = 1
1D9h		65 h	
1DAh		FFh	
1DBh		04 h	
1DCh	JEDEC Sector Map Parameter DWORD-6 Config. Detect-3	02 h	Bits 31:0 = Address Value Configuration Register 1 (bit 2) = 00800002h
1DDh		00 h	
1DEh		80 h	
1DFh		00 h	

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表 94　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1E0h	JEDEC Sector Map Parameter DWORD-7 Config-0 Header	FEh	Configuration Index 00h 4 KB sectors at bottom with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs - 1) = 02h: Three regions Bits 15:8 = Configuration ID = 00h, 4 KB sectors bottom with remainder 256 KB Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
1E1h		00 h	
1E2h		02 h	
1E3h		FFh	
1E4h	JEDEC Sector Map Parameter DWORD-8 Config-0 Region-0	F1h	Region 0 of 4 KB sectors Bits 31:8 = Region size (thirty-two 4 KB) = 0001FFh: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256 KB erase and is not supported in the 4 KB sector Bit 2 = Erase Type 3 support = 0b ---Is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
1E5h		FFh	
1E6h		01 h	
1E7h		00 h	
1E8h	JEDEC Sector Map Parameter DWORD-9 Config-0 Region-1	F8h	Region 1 of 128 KB sector Bits 31:8 = Region size = 0001FFh: Region size as count – 1 of 256 Byte units = 1 x 128 KB sectors = 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined
1E9h		FFh	
1EAh		01 h	

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表 94　　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1EBh		00 h	Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
1ECh	JEDEC Sector Map Parameter DWORD-10 Config-0 Region-2	F8h	Region 2 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value = count – 1 = 261,120 – 1 = 261119 = 03FBFFh Bits 31:8 = 1 Gb device Region size = 07FBFFh: Region size as count – 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count = 130,816 KB/256 = 523,364, value = count – 1 = 523,364 – 1 = 523263 = 07FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not definedBit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 256KB sector region
1EDh		FFh	
1EEh		FBh	
1EFh		03 h (512 Mb) 07 h (1 Gb)	
1F0h	JEDEC Sector Map Parameter DWORD-11 Config-3 Header	FEh	Configuration Index 01h 4 KB sectors at Top with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs – 1) = 02h: Three regions Bits 15:8 = Configuration ID = 01h: 4 KB sectors at top with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
1F1h		01 h	
1F2h		02 h	
1F3h		FFh	
1F4h	JEDEC Sector Map Parameter DWORD-12 Config-3 Region-0	F8h	Region 0 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value
1F5h		FFh	
1F6h		FBh	

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表 94　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1F7h		03h (512 Mb) 07h (1 Gb)	= count – 1 = 261,120 – 1 = 261119 = 03FBFFh Bits 31:8 = 1 Gb device Region size = 07FBFFh: Region size as count – 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count = 130,816 KB/256 = 523,264, value = count – 1 = 523,364 – 1 = 523263 = 07FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not definedBit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
1F8h	JEDEC Sector Map Parameter DWORD-13 Config-3 Region-1	F8h	Region 1 of 128 KB sector Bits 31:8 = Region size = 0001FFh: Region size as count – 1 of 256 Byte units = 1 x 128 KB sectors = 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not definedBit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
1F9h		FFh	
1FAh		01 h	
1FBh		00 h	
1FCh	JEDEC Sector Map Parameter DWORD-14 Config-3 Region-2	F1h	Region 2 of 4 KB sectors Bits 31:8 = Region size (thirty-two 4KB) = 0001FFh: Region size as count – 1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1
1FDh		FFh	
1FEh		01 h	

表 94　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
1FFh		00 h	Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256 KB erase and is not supported in the 4 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
200 h	JEDEC Sector Map Parameter DWORD-15 Config-1 Header	FEh	Configuration Index 02h 4KB sectors split between Bottom and Top with remainder 256 KB Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs – 1) = 04h: Five regions Bits 15:8 = Configuration ID = 02h: 4 KB sectors split between bottom and top with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = Not the end descriptor = 0
201 h		02 h	
202 h		04h	
203 h		FFh	
204 h	JEDEC Sector Map Parameter DWORD-16 Config-1 Region-0	F1h	Region 0 of 4 KB sectors Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256 = 256, value = count – 1 = 256 – 1 = 255 = FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is 256 KB erase and is not supported in the 4 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
205 h		FFh	
206 h		00 h	
207 h		00 h	
208 h	JEDEC Sector Map Parameter DWORD-17 Config-1 Region-1	F8h	Region 1 of 192 KB sector Bits 31:8 = Region size = 0002FFh: Region size as count-1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 =
209 h		FFh	
20 Ah		02 h	

表 94　　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
20 Bh		00h	768, value = count – 1 = 768 – 1 = 767 = 2 FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
20 Ch	JEDEC Sector Map Parameter DWORD-18 Config-1 Region-2	F8h	Region 2 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03F7FFh: Region size as count – 1 of 256 Byte units = 254 x 256 KB sectors = 65,024 KB Count = 65,024 KB/256 = 260,096 value = count – 1 = 260,096 – 1 = 260,095 = 03F7FFh Bits 31:8 = 1 Gb device Region size = 07F7FFh: Region size as count – 1 of 256 Byte units = 510 x 256 KB sectors = 130, 560 KB Count = 130,560 KB/256 = 522,240, value = count – 1 = 522,240 – 1 = 522,239 = 7F7FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector regionBit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region
20 Dh		FFh	
20 Eh		F7h	
20 Fh		03 h (512 Mb) 07 h (1 Gb)	
210 h	JEDEC Sector Map Parameter DWORD-19 Config-1 Region-3	F8h	Region 3 of 192 KB sector Bits 31:8 = Region size = 000FFh: Region size as count – 1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 = 768, value = count – 1 = 768 – 1 = 767 = 2FFh
211 h		FFh	
212 h		02 h	

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表 94　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
213 h		00 h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 22 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region
214 h	JEDEC Sector Map Parameter DWORD-20 Config-1 Region-5	F1h	Region 5 of 4 KB sectors Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256 = 256, value = count – 1 = 256 – 1 = 255 = FFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
215 h		FFh	
216 h		00 h	
217 h		00 h	
218 h	JEDEC Sector Map Parameter DWORD-21 Config-4 Header	FFh	Configuration Index 04h Uniform 256 KB sectors Bits 31:24 = RFU = FFh Bits 23:16 = Region count (DWORDs – 1) = 00 h: One region Bits 15:8 = Configuration ID = 04 h: Uniform 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = End of map descriptor = 1
219 h		04 h	
21 Ah		00 h	
21 Bh		FFh	
21 Ch	JEDEC Sector Map Parameter DWORD-22 Config-4 Region-0	F8h	Region 0 Uniform 256 KB sectors Bits 31:8 = 512 Mb device Region size = 03FFFFh: Region size as count – 1 of 256 Byte units = 256 x 256 KB sectors = 65,536
21 Dh		FFh	
21 Eh		FFh	

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表 94　（续）JEDEC SFDP rev D，扇区映射参数表

SFDP	SFDP DWORD name	Data	Description
21 Fh		03 h (512 Mb) 07 h (1 Gb)	KB Count = 65,536 KB/256 = 262,144 value = count – 1 = 262,144 – 1 = 262,143 = 3FFFFh Bits 31:8 = 1 Gb device Region size = 07FFFFh: Region size as count – 1 of 256 Byte units = 512 x 256 KB sectors = 131,072 KB Count = 131,072 KB/256 = 524,288, value = count – 1 = 524,288 – 1 = 524,287 = 7FFFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/supported = 1 Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region

9.2　制造商和器件 ID

表 95　制造商和器件ID

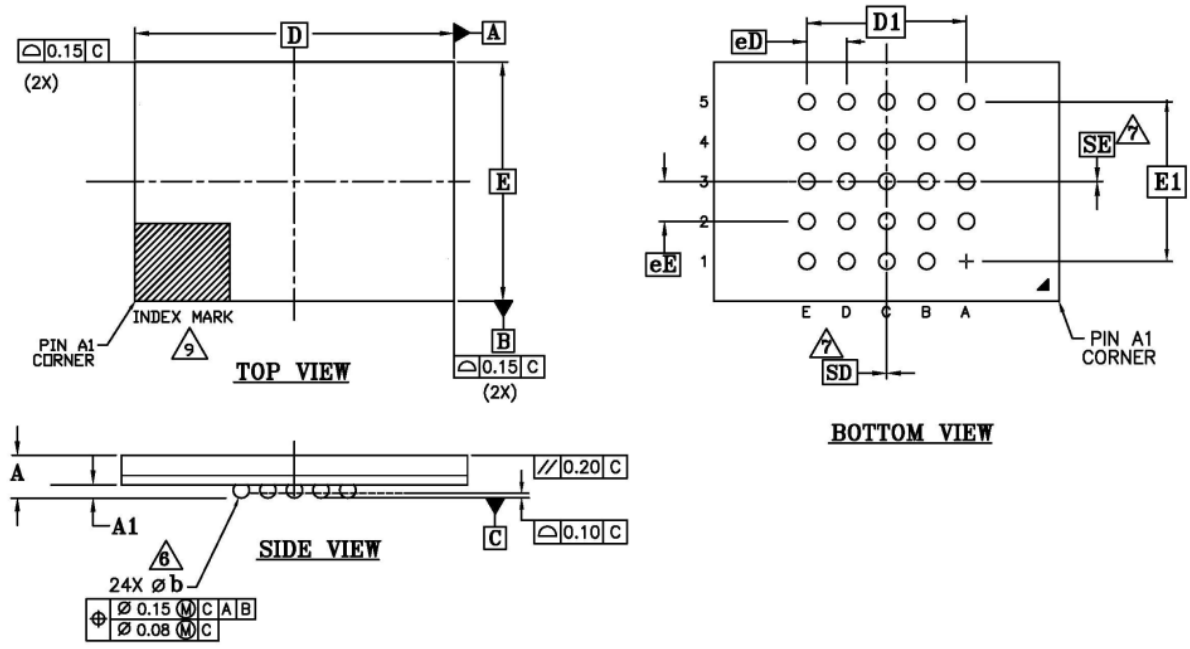
Byte address	Data	Description
00 h	34 h	Manufacturer ID for Infineon
01 h	2 Ah (HL-T) / 2 Bh (HS-T)	Device ID MSB - Memory Interface Type
02 h	1 Ah (512 Mb) / 1 Bh (1 Gb)	Device ID LSB - Density
03 h	0 Fh	ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map.
04 h	03 h (Default Configuration)	Physical Sector Architecture The HS/L-T family may be configured with or without 4 KB parameter sectors in addition to the uniform sectors. 03 h = Uniform 256 KB with thirty-two 4 KB Parameter Sectors)
05 h	90 h (HL-T/HS-T Family)	Family ID

9.3 唯一器件 ID

表 96 唯一器件ID

Byte address	Data	Description
00 h to 07 h	8-Byte Unique Device ID	64-bit unique ID number

10 封装图



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	4.00 BSC		
E1	4.00 BSC		
MD	5		
ME	5		
N	24		
Ø b	0.35	0.40	0.45
eE	1.00 BSC		
eD	1.00 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

NOTES:

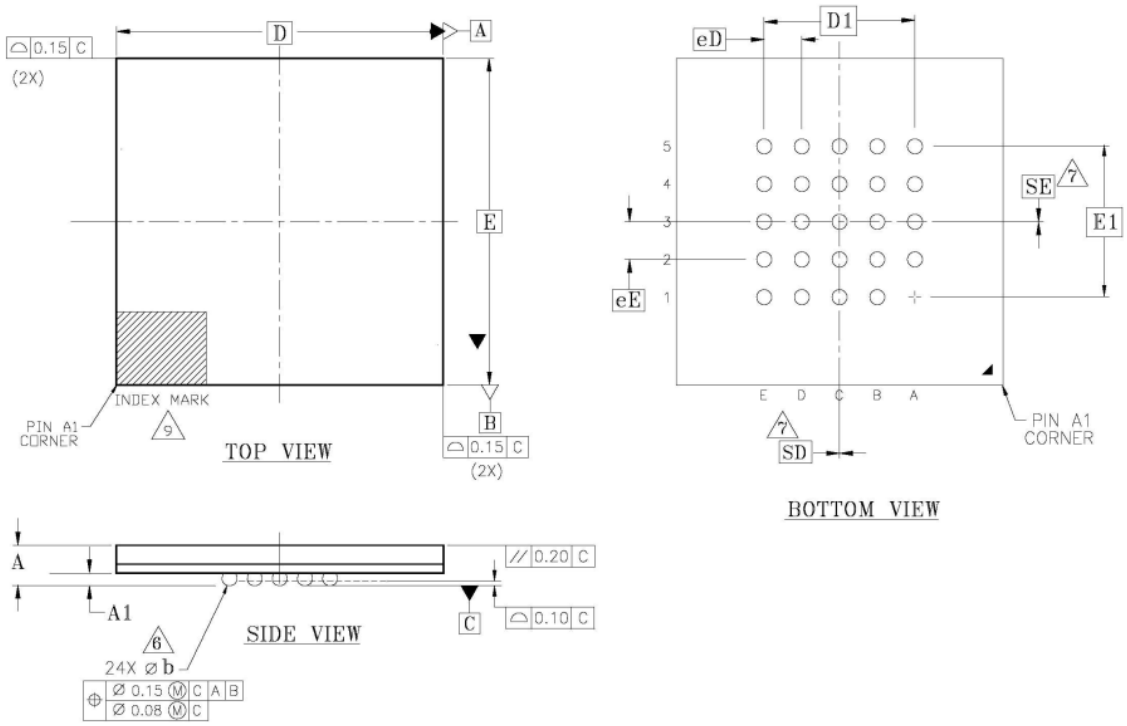
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: MO-234E

002-15550 *B

图 85 24 球 BGA（8 × 6 × 1 毫米）VAA024/ELA024/E2A024 封装外形（PG-BGA-24）

BOTTOM VIEW

10 Pakage diagrams



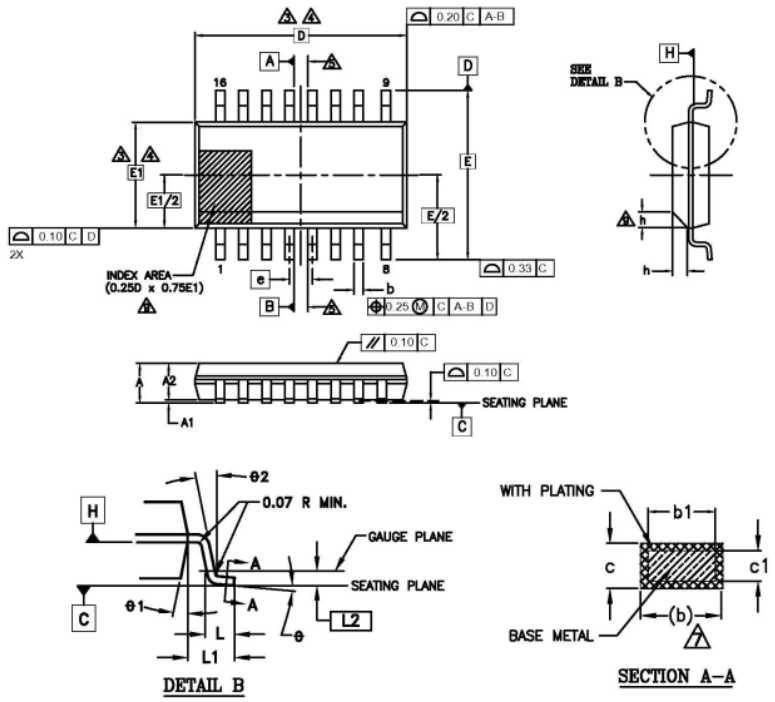
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		8.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
∅ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-22282 **

图 86 24 球 BGA (8 × 8 × 1 mm) VAC024 封装外形 (PG-BGA-24)



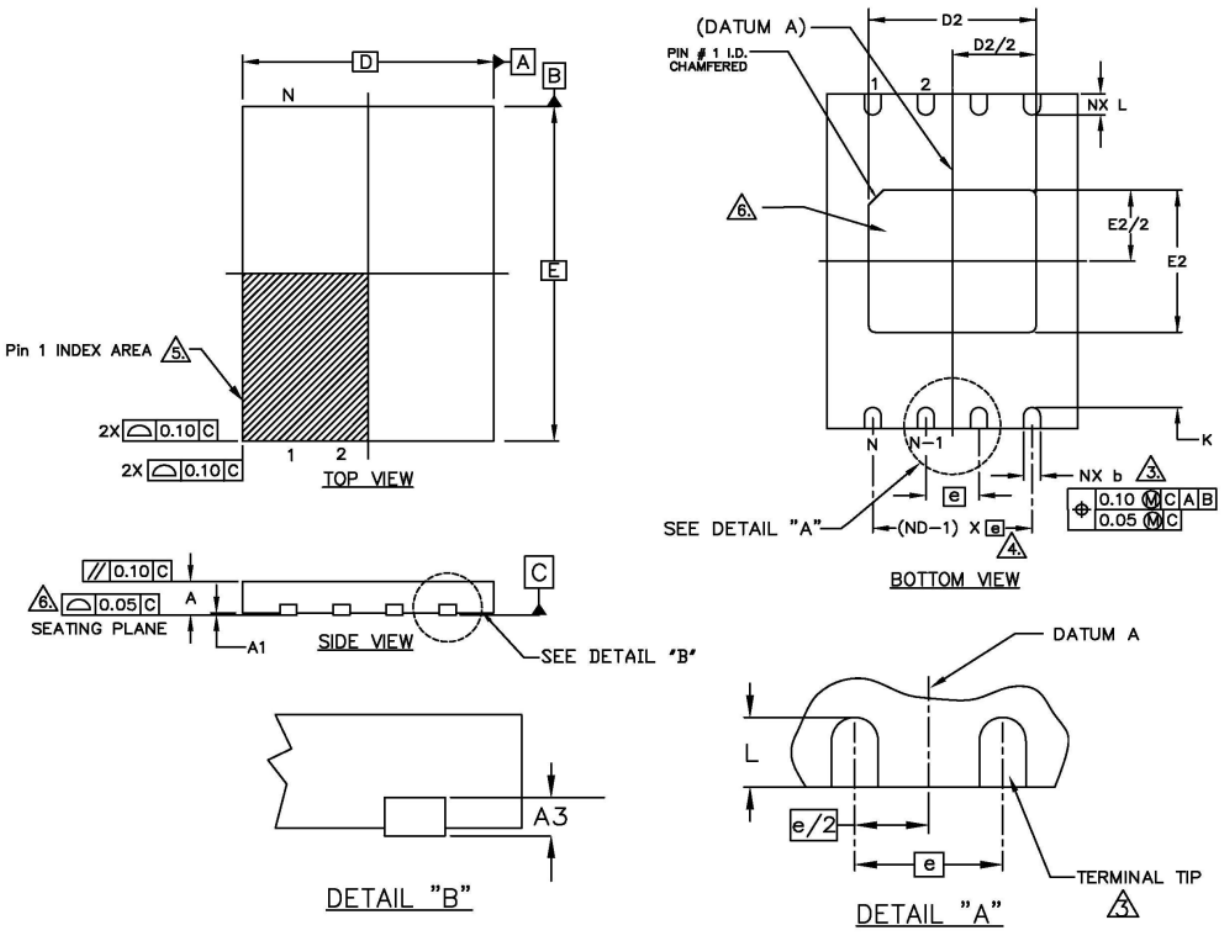
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-15547 *A

图 87　　16 引脚 SOIC (10.30 × 7.50 × 2.65 mm) SO3016/SL3016/SS3016 封装外形 (PG-DSO-16)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
K	0.20	-	-

NOTES:

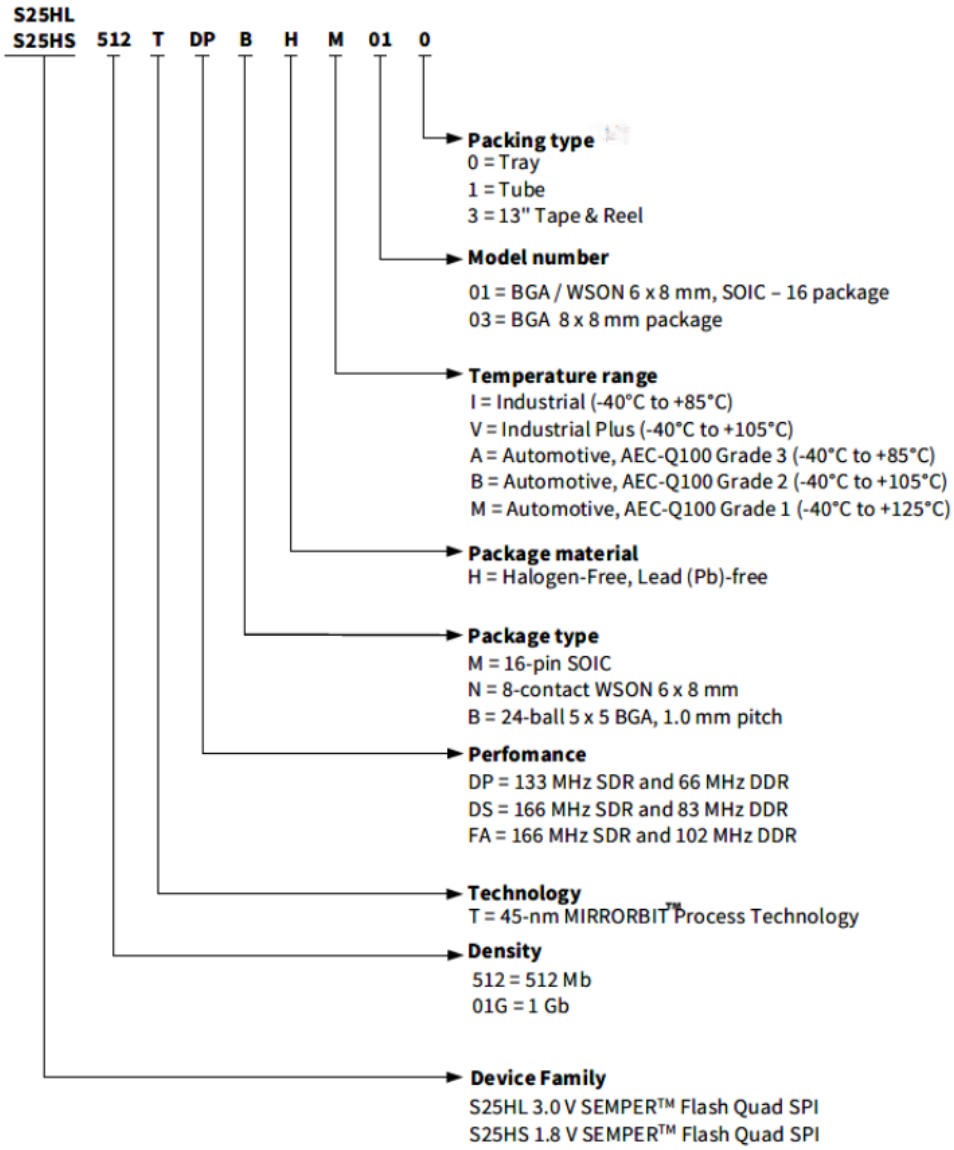
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A

002-15552 *A

图 88　　8 引脚 DFN (6.0 × 8.0 × 0.8 mm) WNH008 4.0 × 3.4 mm E-Pad (Sawn) 封装外形 (PG-WSON-8)

11 订购信息

订购部件编号由以下有效组合形成：



注释：

1. *请参阅https://www.infineon.cn/ 上的包装和封装手册以了解更多信息。*

11.1 有效组合 – 标准等级

表 97 列出计划批量支持的此器件的配置。联系当地销售办事处以确认特定的有效组合的可用性并检查新发布的组合。

表 97 有效组合 – 标准等级

Product family	Speed option	Package and materials	Temperature range	Model number	Packing type	Product (x = Packing type)	Package marking
S25HL512T	DP	BH	I, V	01	0, 3	S25HL512TDPBHI01x	25HL512TPI01
						S25HL512TDPBHV01x	25HL512TPV01
		MH	I, V	01	0, 1[1)], 3	S25HL512TDPMHI01x	25HL512TPI01
						S25HL512TDPMHV01x	25HL512TPV01
		NH	I, V	01	0, 1[1)], 3	S25HL512TDPNHI01x	2HL512TPI01
						S25HL512TDPNHV01x	2HL512TPV01
	FA	BH	I, V	01	0, 3	S25HL512TFABHI01x	25HL512TFI01
						S25HL512TFABHV01x	25HL512TFV01
		MH	I, V	01	0, 1[1)], 3	S25HL512TFAMHI01x	25HL512TFI01
						S25HL512TFAMHV01x	25HL512TFV01
		NH	I, V	01	0, 1[1)], 3	S25HL512TFANHI01x	2HL512TFI01
						S25HL512TFANHV01x	2HL512TFV01
S25HS512T	DP	BH	I, V	01	0, 3	S25HS512TDPBHI01x	25HS512TPI01
						S25HS512TDPBHV01x	25HS512TPV01
		MH	I, V	01	0, 1[1)], 3	S25HS512TDPMHI01x	25HS512TPI01
						S25HS512TDPMHV01x	25HS512TPV01
		NH	I, V	01	0, 1[1)], 3	S25HS512TDPNHI01x	2HS512TPI01
						S25HS512TDPNHV01x	2HS512TPV01
	DS	BH	V	01	0, 3	S25HS512TDSBHV01x	25HS512TSV01
		MH	V	01	0, 3	S25HS512TDSMHV01x	25HS512TSV01
	FA	BH	I, V	01	0, 3	S25HS512TFABHI01x	25HS512TFI01
						S25HS512TFABHV01x	25HS512TFV01
		MH	I, V	01	0, 1[1)], 3	S25HS512TFAMHI01x	25HS512TFI01
						S25HS512TFAMHV01x	25HS512TFV01
		NH	I, V	01	0, 1[1)], 3	S25HS512TFANHI01x	2HS512TFI01
						S25HS512TFANHV01x	2HS512TFV01
S25HL01GT	DP	BH	I, V	03	0, 3	S25HL01GTDPBHV03x	25HL01GTPV03
						S25HL01GTDPBHI03x	25HL01GTPI03

（表格续下页.....）

表 97　　（续）有效组合——标准等级

Product family	Speed option	Package and materials	Temperature range	Model number	Packing type	Product (x = Packing type)	Package marking
		MH	I, V	01	0, 1[1)], 3	S25HL01GTDPMHV01x	25HL01GTPV01
						S25HL01GTDPMHI01x	25HL01GTPI01
	FA	BH	I, V	03	0, 3	S25HL01GTFABHV03x	25HL01GTFV03
						S25HL01GTFABHI03x	25HL01GTFI03
		MH	I, V	01	0, 1[1)], 3	S25HL01GTFAMHI01x	25HL01GTFI01
						S25HL01GTFAMHV01x	25HL01GTFV01
S25HS01GT	DP	BH	I, V	03	0, 3	S25HS01GTDPBHI03x	25HS01GTPI03
						S25HS01GTDPBHV03x	25HS01GTPV03
		MH	I, V	01	0, 1[1)], 3	S25HS01GTDPMHI01x	25HS01GTPI01
						S25HS01GTDPMHV01x	25HS01GTPV01
S25HS01GT	FA	BH	I, V	03	0, 3	S25HS01GTFABHI03x	25HS01GTFI03
						S25HS01GTFABHV03x	25HS01GTFV03
		MH	I, V	01	0, 1[1)], 3	S25HS01GTFAMHI01x	25HS01GTFI01
						S25HS01GTFAMHV01x	25HS01GTFV01

1)　联系销售人员。

11.2 有效组合 – 汽车级/AEC-Q100

表 98列出了符合汽车级/AEC-Q100 认证并计划批量供货的配置。该表将随着新组合的发布而更新。如要确认特定组合的可用性并了解最新推出的组合，请咨询您当地的销售代表。

仅为 AEC-Q100 级产品提供生产部件批准程序（PPAP）支持。

用于需要符合 ISO/TS-16949 标准的端到端应用的产品必须是与 PPAP 结合使用的 AEC-Q100 级产品。非 AEC-Q100 级产品的制造或记录不完全符合 ISO/TS-16949 的要求。

对于不需要符合 ISO/TS-16949 标准的端到端应用，我们还提供不含 PPAP 支持的 AEC-Q100 级产品。

表 98 有效组合 – 汽车级/AEC-Q100

Product family	Speed option	Package and materials	Temperature range	Model number	Packing type	Ordering part number (x = packing type)	Package marking
S25HL512T	DP	BH	A[1], B, M	01	0, 3	S25HL512TDPBHA01x	25HL512TPA01
						S25HL512TDPBHB01x	25HL512TPB01
						S25HL512TDPBHM01x	25HL512TPM01
		MH	A[1], B, M	01	0, 1[1], 3	S25HL512TDPMHA01x	25HL512TPA01
						S25HL512TDPMHB01x	25HL512TPB01
						S25HL512TDPMHM01x	25HL512TPM01
		NH	A[1], B, M	01	0, 1[1], 3	S25HL512TDPNHA01x	2HL512TPA01
						S25HL512TDPNHB01x	2HL512TPB01
						S25HL512TDPNHM01x	2HL512TPM01
	FA	BH	A[1], B, M	01	0, 3	S25HL512TFABHA01x	25HL512TFA01
						S25HL512TFABHB01x	25HL512TFB01
						S25HL512TFABHM01x	25HL512TFM01
		MH	A[1], B, M	01	0, 1[1], 3	S25HL512TFAMHA01x	25HL512TFA01
						S25HL512TFAMHB01x	25HL512TFB01
						S25HL512TFAMHM01x	25HL512TFM01
		NH	A[1], B, M	01	0, 1[1], 3	S25HL512TFANHA01x	2HL512TFA01
						S25HL512TFANHB01x	2HL512TFB01
						S25HL512TFANHM01x	2HL512TFM01
S25HS512T	DP	BH	A[1], B, M	01	0, 3	S25HS512TDPBHA01x	25HS512TPA01
						S25HS512TDPBHB01x	25HS512TPB01
						S25HS512TDPBHM01x	25HS512TPM01
		MH	A[1], B, M	01	0, 1[1], 3	S25HS512TDPMHA01x	25HS512TPA01
						S25HS512TDPMHB01x	25HS512TPB01

（表格续下页……）

表 98　　（续）有效组合 - 汽车级/AEC-Q100

Product family	Speed option	Package and materials	Temperature range	Model number	Packing type	Ordering part number (x = packing type)	Package marking
						S25HS512TDPMHM01x	25HS512TPM01
		NH	A[1], B, M	01	0, 1[1], 3	S25HS512TDPNHA01x	2HS512TPA01
						S25HS512TDPNHB01x	2HS512TPB01
						S25HS512TDPNHM01x	2HS512TPM01
	FA	BH	A[1], B, M	01	0, 3	S25HS512TFABHA01x	25HS512TFA01
						S25HS512TFABHB01x	25HS512TFB01
						S25HS512TFABHM01x	25HS512TFM01
S25HS512T	FA	MH	A[1], B, M	01	0, 1[1], 3	S25HS512TFAMHA01x	25HS512TFA01
						S25HS512TFAMHB01x	25HS512TFB01
						S25HS512TFAMHM01x	25HS512TFM01
		NH	A[1], B, M	01	0, 1[1], 3	S25HS512TFANHA01x	2HS512TFA01
						S25HS512TFANHB01x	2HS512TFB01
						S25HS512TFANHM01x	2HS512TFM01
S25HL01GT	DP	BH	A, B, M	03	0, 3	S25HL01GTDPBHA03x	25HL01GTPA03
						S25HL01GTDPBHB03x	25HL01GTPB03
						S25HL01GTDPBHM03x	25HL01GTPM03
		MH	A, B, M	01	0, 1[1], 3	S25HL01GTDPMHA01x	25HL01GTPA01
						S25HL01GTDPMHB01x	25HL01GTPB01
						S25HL01GTDPMHM01x	25HL01GTPM01
	FA	BH	A, B, M	03	0, 3	S25HL01GTFABHA03x	25HL01GTFA03
						S25HL01GTFABHB03x	25HL01GTFB03
						S25HL01GTFABHM03x	25HL01GTFM03
		MH	A, B, M	01	0, 1[1], 3	S25HL01GTFAMHA01x	25HL01GTFA01
						S25HL01GTFAMHB01x	25HL01GTFB01
						S25HL01GTFAMHM01x	25HL01GTFM01
S25HS01GT	DP	BH	A, B, M	03	0, 3	S25HS01GTDPBHA03x	25HS01GTPA03
						S25HS01GTDPBHB03x	25HS01GTPB03
						S25HS01GTDPBHM03x	25HS01GTPM03
		MH	A, B, M	01	0, 1[1], 3	S25HS01GTDPMHA01x	25HS01GTPA01
						S25HS01GTDPMHB01x	25HS01GTPB01
						S25HS01GTDPMHM01x	25HS01GTPM01

（表格续下页.....）

表 98 （续）有效组合 - 汽车级/AEC-Q100

Product family	Speed option	Package and materials	Temperature range	Model number	Packing type	Ordering part number (x = packing type)	Package marking
	FA	BH	A, B, M	03	0, 3	S25HS01GTFABHA03x	25HS01GTFA03
						S25HS01GTFABHB03x	25HS01GTFB03
						S25HS01GTFABHM03x	25HS01GTFM03
		MH	A, B, M	01	0, 1[1)], 3	S25HS01GTFAMHA01x	25HS01GTFA01
						S25HS01GTFAMHB01x	25HS01GTFB01
						S25HS01GTFAMHM01x	25HS01GTFM01

1) 联系销售人员

修订记录

Document revision	Date	Description of changes
*P	2019-06-04	Finalizing document for S25HS512T devices.
*Q	2019-06-21	Finalizing document for S25HL512T devices.
*R	2019-07-03	Finalizing document for S25HL01GT devices.
*S	2019-09-13	Updated Transaction table Updated 4-4-4 transaction table Updated Table 83 Updated Ordering information Updated Valid combinations — standard grade Updated Table 97 Removed table “Valid Combinations — Standard Grade (In Production)”. Updated Valid combinations — automotive grade/ AEC-Q100 Updated Table 98 Removed “Valid Combinations — Automotive Grade/ AEC-Q100 (In Production)”.
*T	2019-11-26	Finalizing document for S25HS01GT devices.
*U	2019-12-20	Updated Features Updated Data protection schemes Updated Legacy block protection (LBP) Updated Configuration protection Updated Table 23 Updated Device identification Updated JEDEC SFDP Rev D: Updated JEDEC SFDP Rev D header table Updated Table 91 Updated JEDEC SFDP Rev D parameter table Updated Table 93
*V	2019-01-29	Updated Transaction table Updated 1-1-1 transaction table Updated Table 79 Updated to new template.
*W	2020-03-23	Updated Electrical characteristics Updated Latchup characteristics Updated Table 87. Completing Sunset Review.

Revision history

Document revision	Date	Description of changes
*X	2020-04-22	Updated Features Updated Error detection and correction Updated ECC error reporting Updated ECC data unit status (EDUS) Updated Table 15 Updated Registers Updated Configuration register 2 (CFR2x) Updated Table 54 Updated ECC status register (ECSV) Updated Table 61 Updated Device identification Updated JEDEC SFDP Rev D Updated JEDEC SFDP Rev D header table Updated Table 91 Updated JEDEC SFDP Rev D parameter table Updated Table 93
*Y	2020-12-01	Updated Features Updated Read Updated Read memory array transactions Updated Read SDR and DDR quad I/O transaction Updated description. Updated Read QPI SDR and DDR transaction Updated description Updated Read memory array related registers and transactions Updated Table 61 Updated Data learning pattern (DLP) Updated description Updated Registers Updated Configuration register 3 (CFR3x) Updated Table 56 Updated ECC address trap register (EATV) Updated Table 62 Updated Advanced sector protection register (ASPO) Updated Table 64. Updated Device identification Updated JEDEC SFDP Rev D Updated JEDEC SFDP Rev D parameter table Updated Table 92 Updated Sector map parameter table notes Updated description Updated Table 93

Revision history

Document revision	Date	Description of changes
*Z	2021-10-18	Updated Electrical characteristics Updated Thermal resistance Updated Table 85 Updated DC characteristics Updated DC characteristics (all temperature ranges) Updated Table 88 Updated Timing characteristics Updated Table 90 Updated Device identification Updated JEDEC SFDP Rev D Updated JEDEC SFDP Rev D parameter table Updated Table 92 Migrated to Infineon template. Completing Sunset Review.
AA	2022-01-18	Updated Address space maps Updated JEDEC JESD216 serial flash discoverable parameters (SFDP) space Updated Table 12 (Replaced JESD216C with JESD216D). Updated Features Updated Read Updated Read identification transactions Updated Read device identification transaction Replaced CFR3V[1:0] with CFR3V[7:6]. Updated Timing characteristics Updated Table 90 Updated Device identification Updated JEDEC SFDP Rev D Updated JEDEC SFDP Rev D parameter table Updated Table 92
AB	2022-12-08	Updated Features Updated Write Added Enter 4 byte address mode Added Exit 4 byte address mode Updated Write transactions related registers and transactions Updated Table 38 Updated Electrical characteristics Updated AC test conditions Updated Table 89 Updated Timing characteristics Updated Table 90 Completing Sunset Review.

Revision history

Document revision	Date	Description of changes
AC	2023-03-02	Updated Features Updated description Updated Features Updated Error detection and correction Updated ECC error reporting Updated ECC status register (ECSV) Updated description Updated ECC error address trap (EATV) Updated description Updated ECC error detection counter (ECTV) Updated description Updated Data protection schemes Updated Legacy block protection (LBP) Updated Configuration protection Updated description Updated Reset Updated description Updated JEDEC serial flash reset signaling protocol Replaced “CS# signaling reset” with “JEDEC serial flash reset signaling protocol” in heading. Updated description. Updated Figure 63 (Updated caption only). Updated Reset behavior Updated Table 44 Updated Power modes Updated Deep power down (DPD) mode Updated Enter DPD Updated description Updated Registers Updated Status register 1 (STR1x) Updated Note 24 referred in Table 47 Updated Status register 2 (STR2x) Updated Note 25 referred in Table 50 Updated Transaction table Updated 4-4-4 transaction table Updated Table 83 Updated Timing characteristics Updated Table 90 Updated to new template.
AD	2023-12-18	Updated Figure 19 Updated Figure 35 Updated Figure 85 Updated Table 98

Revision history

Document revision	Date	Description of changes
AE	2024-03-25	Updated “Data integrity” under Features. Updated “Packages” under Features. Updated “Program/erase (PE) endurance - high endurance (256 KB sectors)” under Data integrity. Updated waveform in QUAD output read SPI (QOR, 1S-1S-4S). Updated Table 57, Table 88, Table 90, and Table 92.
AF	2024-06-25	Removed 256 Mb device from datasheet. S25HL256T and S25HS256T created separate datasheet.
AG	2025-07-17	Template update; footnotes number updated. Footnotes added in Table 97 and Table 98. Updated the values of t_{SU} and t_{HD} in Table 90.

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