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CYTVII-B-H-8M-176-CPU

Evaluation Board User Guide

Document Number: 002-25907 Rev. *A

Cypress Semiconductor
An Infineon Technologies Company
198 Champion Court
San Jose, CA 95134-1709
www.cypress.com, www.infineon.com

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1. Introduction

This user guide provides instructions to handle the CYTVII-B-H-8M-176-CPU and CYTVII-B-H-176-SO evaluation boards, collectively referred to as 'CPU board' in this document. This is an evaluation platform for the CYT4BF8C Traveo™ II device. The board can be used as a standalone for basic validation or in combination with the CYTVII-B-E-BB Traveo II base board (available separately from Cypress). This document assumes that you will work with the combination (CPU board + base board), and provides guidance on how to use the features of the evaluation platform.

1.1 Precautions and Warnings

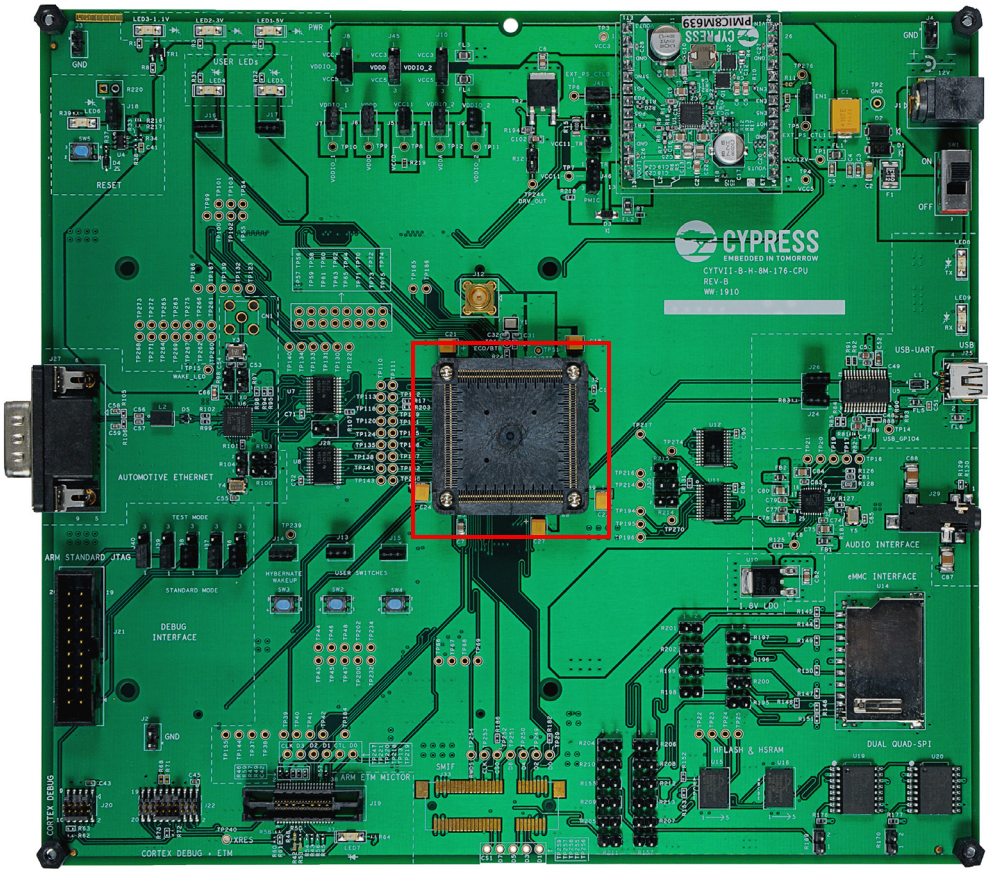
The board is a delicate PCB; make sure that the evaluation board is handled by qualified personnel who are aware of the capabilities of the board. Handle the board carefully and make sure it is not bent or subjected to stress. Ensure your own safety arising from electrical hazards and other sources.

The CPU board is shipped with a 12 V DC power adapter. This adapter can be plugged into the AC mains supply anywhere in the world and is designed to receive 100-240 V AC V @ 50/60 Hz. While powering the board, you must connect only the power adapter supplied with the evaluation board and not any other part.

2. Overview

Figure 2-1 shows the CYTVII-B-H-176-SO board. Insert a Traveo II device into the IC socket (highlighted in red) while the evaluation board is powered OFF.

Figure 2-1. CYTVII-B-H-176-SO Board



A variant of the CPU board (CYTVII-B-H-8M-176-CPU) is also available, where the Traveo II device is soldered directly onto the PCB. Functionally, the CYTVII-B-H-8M-176-CPU and CYTVII-B-H-176-SO boards are identical, except that the device can be easily replaced in the latter.

For CYTVII-B-H-176-SO kit open the four screws with a screwdriver, insert the device. Make sure that the device pin number 1 mark is facing the white arrow on the PCB, which is near C21. After inserting the device close the socket cover, tighten the screws. Make sure that the three holes on the socket cover are aligned as shown in Figure 2-1 for the proper working of the device.

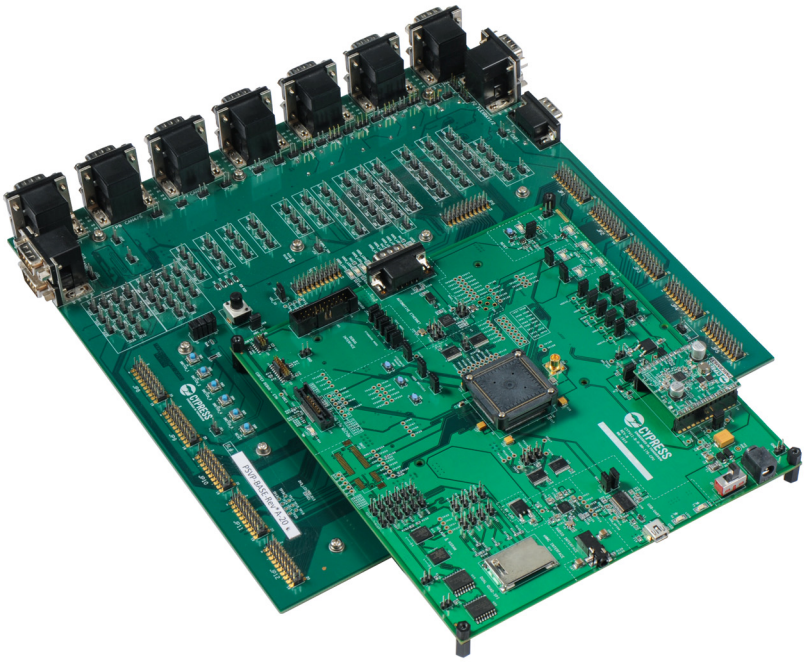
The CPU board is meant to be used along with a Traveo II base board (CYTVII-B-E-BB). The base board brings out all important interface connections such as CAN, LIN, SPI EEPROM, CXPI, and Flexray, and can be used in conjunction with several CPU boards of the Traveo II family. Figure 2-2 shows the base board.

Figure 2-2. Traveo II Base Board (CYTVII-B-E-BB)



Two Samtec connectors on the CPU board and corresponding mating connectors on the base board are used to connect signals across the two boards. When put together, the boards appear as shown in Figure 2-3.

Figure 2-3. Combination of CPU Board and Traveo II Base Board



2.1 Functional Overview

The CPU board has the following components:

1. One Traveo II device, either soldered or mounted on a socket (U3).
2. PMIC to generate the 5-V, 3.3-V, and 1.1-V output, which powers the CPU board and the base board (if connected).
3. Programming interface (Arm® Standard JTAG, Cortex® Debug, Cortex Debug + ETM and Arm ETM Mictor) to connect several programming tools such as IAR I-jet, Green Hills MULTI, also Cypress MiniProg.
4. USB-UART interface for terminal logging (J25).
5. Two user switches (SW2 and SW4) and two user LEDs (LED4 and LED5) for standalone operation without the base board.
6. One Hibernate Wakeup Switch. (SW3)
7. Reset controller with manual reset switch (SW5) and voltage supervision.
8. Measurement of device current on VCCD using jumper J5, VDDD using jumper J6, VDDIO_1 using jumper J7, VDDIO_2 using jumper J9, and VDDA using jumper J11 respectively.
9. Samtec connector interface (J34 and J35) for connecting to the base board CYTVII-B-E-BB.
10. SMIF connector (J33) so that the SMIF module can be mounted.

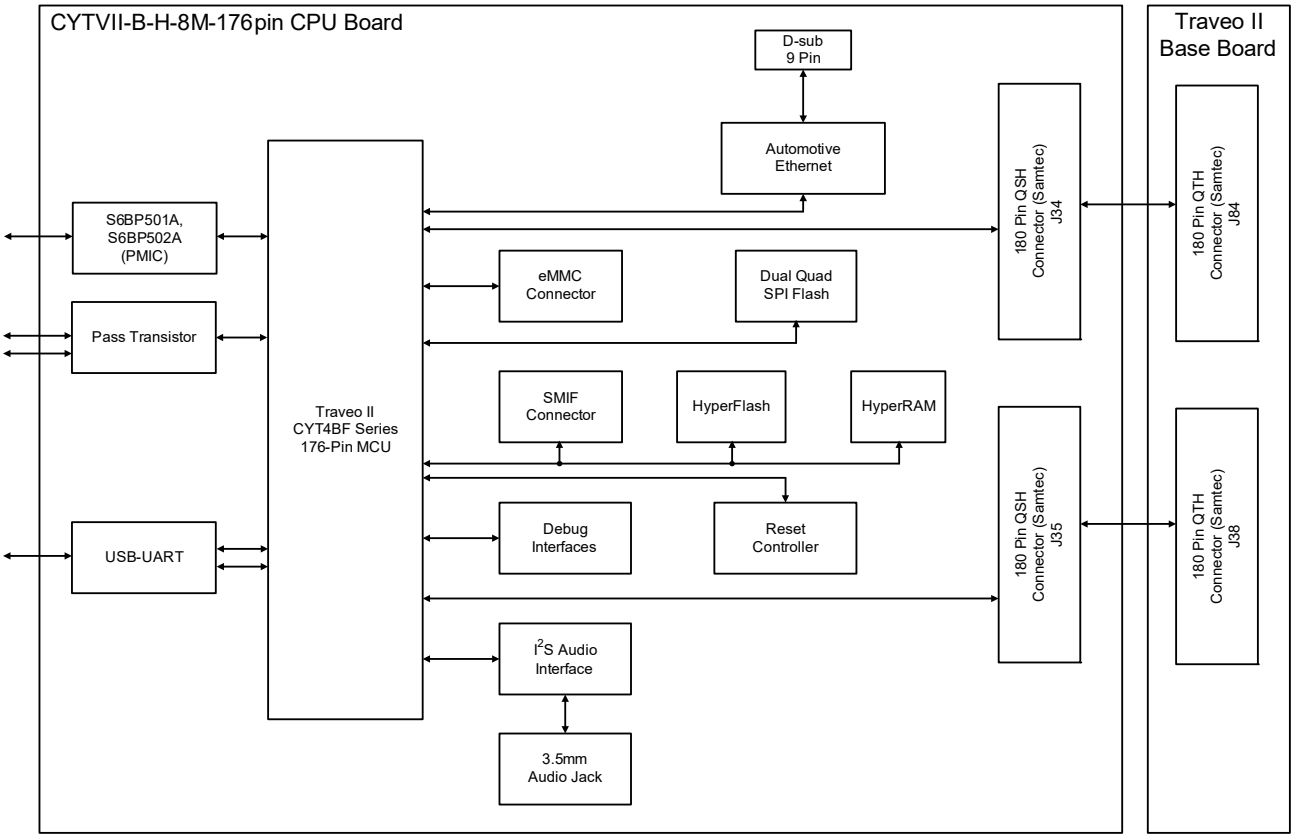
The Traveo II base board has the following components:

1. Six CAN-FD transceivers based on TJA1057GT (Dual connectors P6, P7, P8).
2. Four CAN-FD transceivers based on TJA1145T, with SPI-based transceiver configuration (Dual connectors P9, P10).
3. Six LIN transceivers based on TJA1021T (Dual connectors P3, P4, P5).
4. Two Flexray transceivers based on TJA1081TS (Dual connector P2).
5. One CXPI transceiver based on S6BT112A01 (Connector P1).
6. One SPI EEPROM 25LC320A (U9).
7. Five user switches (SW1 through SW5), 10 user LEDs (USER_LED0 through USER_LED9), and one potentiometer (POT1) for analog input.
8. Pin headers to access all I/Os of the Traveo II device (when a CPU board is connected to the base board).
9. Samtec connector interface (J38 and J84) for connecting to a CPU board.

2.1.1 Block Diagram

The Block Diagram is shown in Figure 2-4.

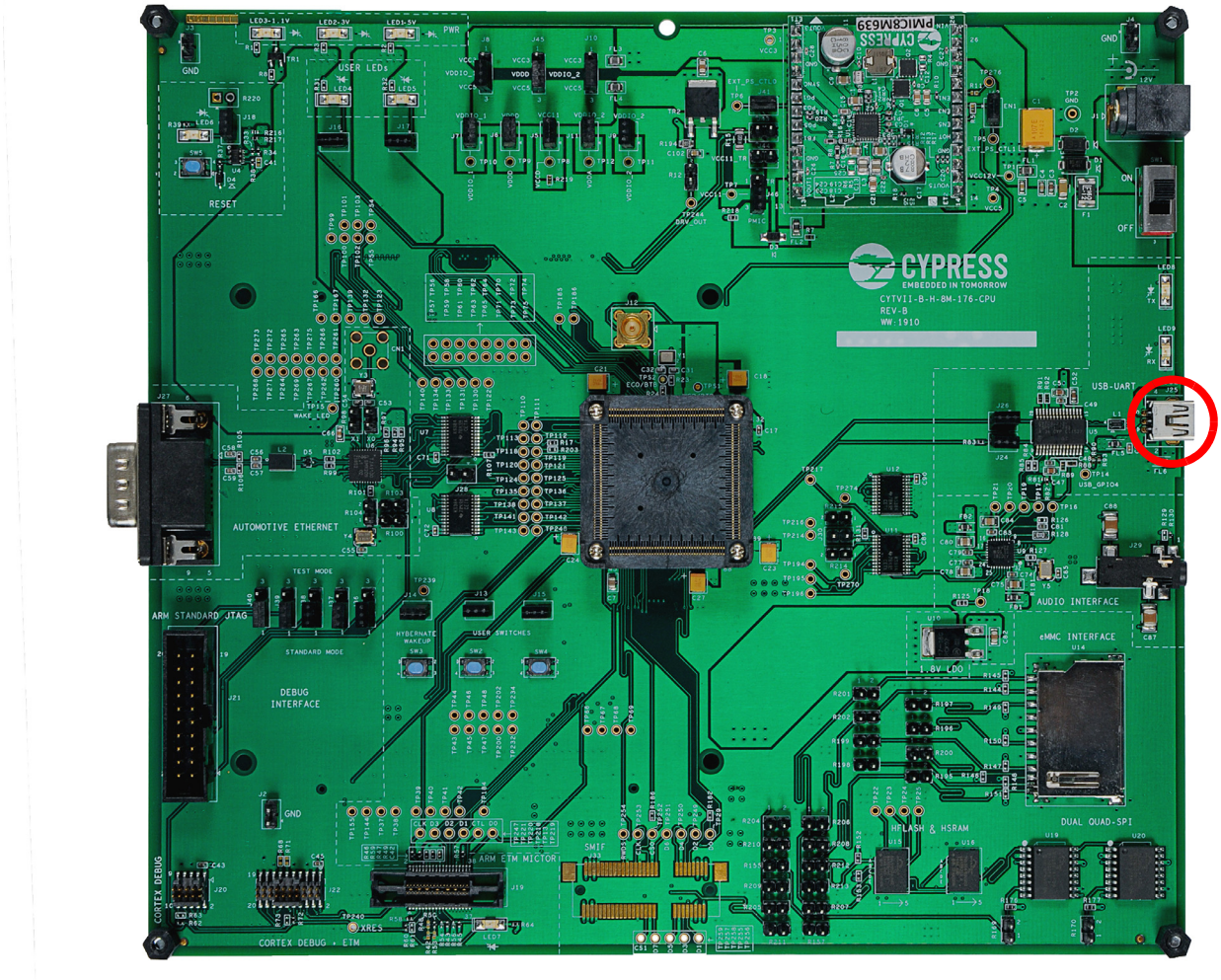
Figure 2-4. Block Diagram



2.1.2 USB Connector

The location of the USB Connector is shown in Figure 2-5.

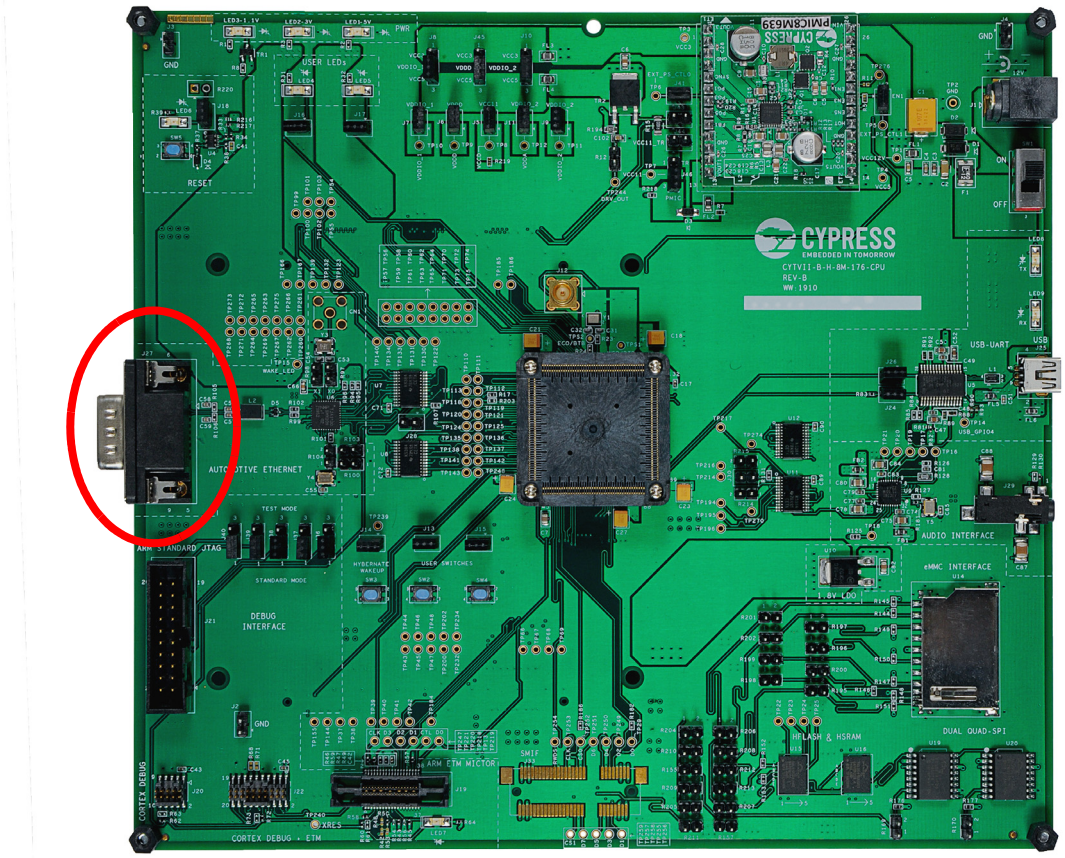
Figure 2-5. USB Connector



2.1.3 Ethernet Connector

The location of the Ethernet Connector is shown in Figure 2-6.

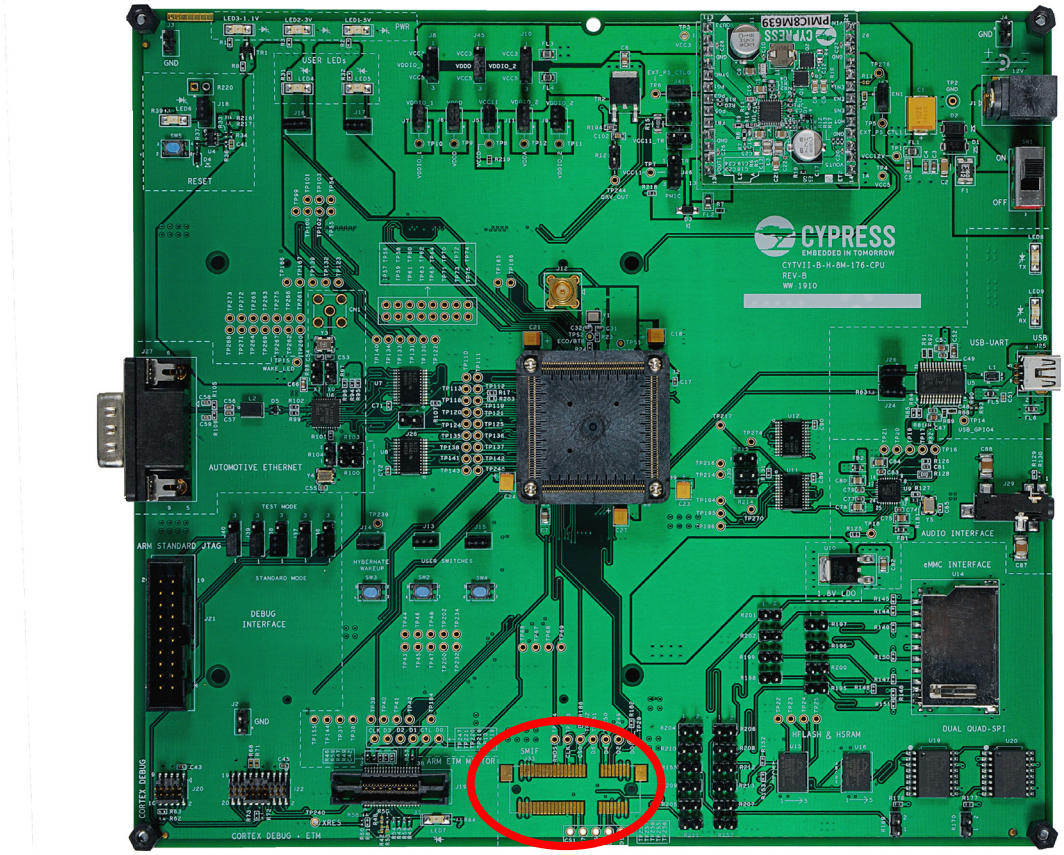
Figure 2-6. Ethernet Connector



2.1.4 SMIF Connector

The location of the SMIF Connector is shown in Figure 2-7.

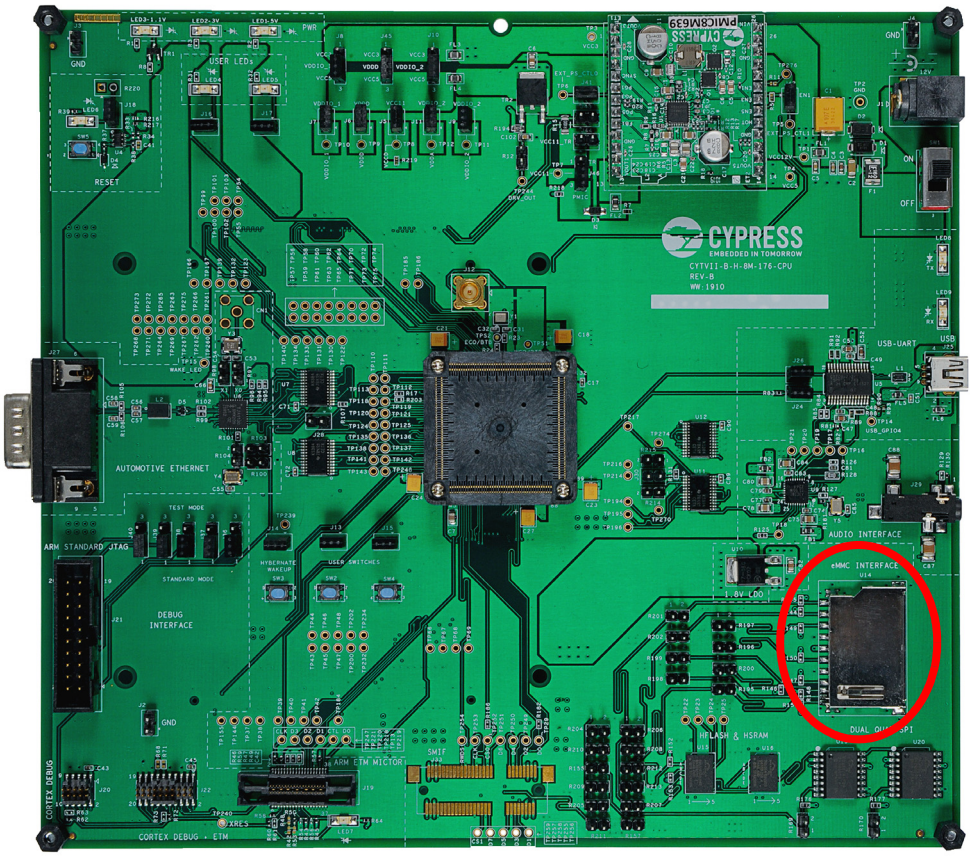
Figure 2-7. SMIF Connector



2.1.5 eMMC Connector

The location of the eMMC Connector is shown in Figure 2-8.

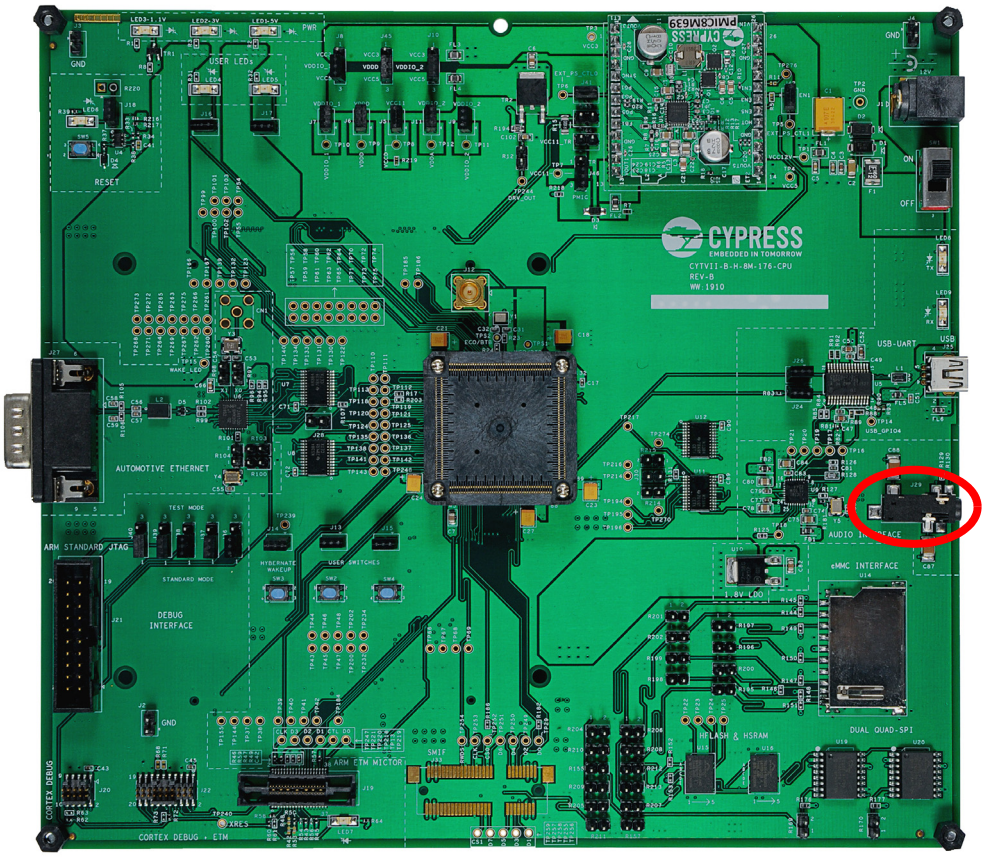
Figure 2-8. eMMC Connector



2.1.6 Audio Connector

The location of the Audio Connector is shown in Figure 2-9.

Figure 2-9. Audio Connector

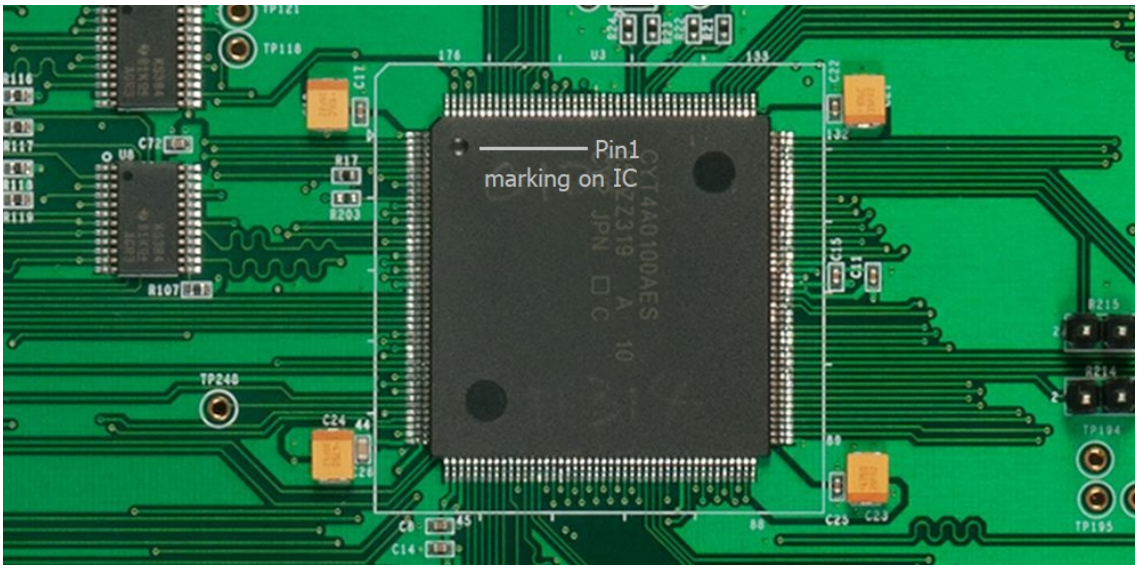


3. Operation

This section describes the operation of the CPU board and the base board. It is assumed that you have connected the CPU board to the base board using the Samtec interface and inserted a Traveo II device into the IC socket (applicable to CYTVII-B-H-176-SO boards only). Follow these steps to operate the CPU board and the base board:

1. For the socketed CPU board, ensure that the device is inserted into the socket. Remove the four screws on the socket using the screwdriver provided in the box and open the socket cover. If the device is not present, place one carefully using a vacuum picker or a pair of tweezers.
2. Ensure that pin 1 of the device is near the pin 1 marking on the PCB, as shown in Figure 3-1. Also, ensure that the device is placed in an angle such that the pins on all four sides of the LQFP package match well with the socket pins. Align the device slightly, if required.

Figure 3-1. Orientation of Device when Inserted in Socket



3. Replace the socket cover and fix the four screws so that the socket cover tightly sits on the socket base.
4. A 12 V wall adapter board is supplied along with the CPU board. Connect the 12 V wall adapter to the barrel connector marked "12V DC" on the CPU board. Connect its plug to a mains socket using one of the four plug adapters provided in the white box (depending on the geographical location and the socket type available).
5. Ensure that jumpers J45 (default “2-3”), J5, J6, J8, J7, J10, J9, J11 (current measurement jumpers) are inserted on the CPU board.
6. Turn ON the mains supply to the wall adapter. Turn ON the switch SW1 on the CPU board. The LED labeled PWR should light up.
7. Connect an appropriate programming tool to one of the programming interfaces (J19, J20, J21, J22). Programming tool options are:
   - Arm ETM MICTOR on J19
   - Cortex DEBUG on J20
   - Arm Standard JTAG on J21

- Cortex DEBUG and ETM on J22

8. Install the appropriate programming integrated design environment (IDE) on a PC. The programming IDE (GHS MULTI, IAR Embedded Workbench, Cypress Programmer, and so on) should be able to detect a device (read the device ID) and to load a firmware HEX file (*.srec*) into the device flash successfully.
   As part of the release package, various firmware examples compiled in *.srec* programming IDEs are available. Some examples use specific transceivers on the base board.
9. To start with, use the LED blink example provided with the release package to test the functioning of the board.
10. Connect a USB-mini cable to J25 and the other end to a PC. Open Tera Term or your preferred terminal logging application and set the appropriate port and baud rate (typically 115,200 baud, 8, N, 1). Ensure that jumpers J24 and J25 are inserted on the CPU board. Some firmware examples provide data logs from the device or ask for user inputs over the terminal.

4. Connections and Settings

4.1 Evaluation Board Connections

4.1.1 Base Board Connections

Make sure that the following jumpers are inserted on the base board, so that each transceiver on the base board can be used with the respective firmware example that activate each functionality of the device:

- CAN0.0 from the device uses the CAN0 transceiver on the base board (connect jumpers J70, J71, J72).
- CAN0.1 from the device uses the CAN1 transceiver on the base board (connect jumpers J66, J67, J68).
- CAN0.2 from the device uses the CAN2 transceiver on the base board (connect jumpers J81, J82, J83).
- CAN1.0 from the device uses the CAN3 transceiver on the base board (connect jumpers J76, J77, J78).
- CAN1.1 from the device uses the CAN4 transceiver on the base board (connect jumpers J91, J92, J93).
- CAN1.2 from the device uses the CAN5 transceiver on the base board (connect jumpers J86, J87, J88).
- LIN0 from the device uses the LIN0 transceiver on the base board (connect jumpers J58, J59, J60, J63).
- LIN1 from the device uses the LIN1 transceiver on the base board (connect jumpers J51, J52, J53, J56).
- LIN2 from the device uses the LIN2 transceiver on the base board (connect jumpers J37, J39, J40, J43).
- LIN3 from the device uses the LIN3 transceiver on the base board (connect jumpers J30, J31, J32, J35).
- LIN4 from the device uses the LIN4 transceiver on the base board (connect jumpers J22, J23, J24, J27).
- LIN5 from the device uses the LIN5 transceiver on the base board (connect jumpers J10, J16, J17, J20).
- EEPROM on the base board is enabled by connecting jumpers J47, J48, J49.
- The user switch functionality is enabled by connecting jumper J102.
- The potentiometer functionality is enabled by connecting jumper J89.

In addition, power is supplied to the base board by connecting jumper J80 to the 3 V or 5 V select jumper pin in the ‘5 V’ position. Make sure that jumper J80 is always connected. Once a specific functionality is chosen by connecting the jumpers listed above, ensure that the appropriate firmware is loaded onto the device. Incorrect firmware can result in port pins being configured incorrectly leading to bus contention and damage to hardware. For example, if you connect jumpers related to CAN0.0, you must ensure that firmware configures the related ports as CAN pins. Contact Cypress technical support for firmware examples.

Apart from these interface transceivers that can be used for specific functions, all pins of the device are also accessible on the base board using pin headers JP1 through JP12.

The device port pins are connected to pin headers on the base board as listed in Table 4-1.

Table 4-1. Device Port Pin Connections on Base Board

MCU Port Pin	Connection 1 Signal Name of Schematics	Connection 1 CPU Board Test Point	Connection 1 Base Board Test Point
VSSD	GND	TP2	Not applicable
P0.0	ETH_REFCLK	TP110	Not applicable
P0.1	ETH_TXEN	TP111	Not applicable
P0.2	ETH_TXER	TP112	Not applicable
P0.3	ETH_TXC	TP113	Not applicable
P1.0	BB_SPI0_MISO	Not applicable	JP3.18
P1.1	BB_SPI0_MOSI	Not applicable	JP3.16
P1.2	BB_SPI0_CLK	Not applicable	JP9.17
P1.3	BB_SPI0_SS0	Not applicable	JP9.18
P2.0	ETH_TXD0	TP118	Not applicable
P2.1	ETH_TXD1	TP119	Not applicable
P2.2	ETH_TXD2	TP120	Not applicable
P2.3	ETH_TXD3	TP121	Not applicable
P2.4	BB_SPI0_HOLD	TP122	JP12.4
P2.5	BB_SPI0_WP	TP123	JP2.3
P3.0	ETH_RXD0	TP124	Not applicable
P3.1	ETH_RXD1	TP125	Not applicable
P3.2	USER_LED1	J16.2	Not applicable
P3.3	USER_LED2	J17.2	Not applicable
P3.4	USER_SW1	J13.1	Not applicable
P3.5	USER_SW2	J15.1	Not applicable
VDDD	Not applicable	TP9	Not applicable
VSSD	GND	TP2	Not applicable
P4.0	BB_LIN1_RXD	TP130	JP6.15
P4.1	BB_LIN1_TXD	TP131	JP6.14
P4.2	BB_LIN1_SLP	TP132	JP6.3
P4.3	BB_CAN1_TXD	TP133	JP6.9
P4.4	BB_CAN1_RXD	TP134	JP6.8
P5.0	ETH_RXD2	TP135	Not applicable
P5.1	ETH_RXD3	TP136	Not applicable
P5.2	ETH_RXDV	TP138	Not applicable
P5.3	ETH_RXER	TP137	Not applicable
P5.4	GPIO_P5_4	TP140	JP6.10
P5.5	BB_LIN1_WAKE	TP139	JP6.4
P6.0	ETH_RXC	TP141	Not applicable
P6.1	ETH_MDIO	TP142	Not applicable
P6.2	ETH_MDC	TP143	Not applicable
P6.3	GPIO_P6_3	TP144	JP8.4
P6.4	SS_SPI0_SS1	Not applicable	Not applicable
P6.5	SDHC_CD	R198	Not applicable
P6.6	BB_CAN_SPI1_SS0	Not applicable	JP10.10
P6.7	BB_CAN_SPI1_SS1	Not applicable	JP10.9
VDDD	Not applicable	TP9	Not applicable

Table 4-1. Device Port Pin Connections on Base Board

MCU Port Pin	Connection 1 Signal Name of Schematics	Connection 1 CPU Board Test Point	Connection 1 Base Board Test Point
VDDIO_1	Not applicable	TP10	Not applicable
VSSD	GND	TP2	Not applicable
VCCD	Not applicable	TP8	Not applicable
VCCD	Not applicable	TP8	Not applicable
P7.0	SPIHB_CLK	R187.1,R195.1,R212.1	Not applicable
P7.1	SPIHB_RWDS	R188.1,R196.1,R213.1	Not applicable
P7.2	SPIHB_SEL0	R155.2,R169.1,R186.1,R197.1	Not applicable
P7.3	SPIHB_SEL1	R157.2,R170.1,R189.2	Not applicable
P7.4	SPIHB_DATA0	R182.1,R199.1,R204.1	Not applicable
P7.5	SPIHB_DATA1	R193.2,R200.1,R205.1	Not applicable
P7.6	BB_USER_LED0	TP155	JP7.18
P7.7	BB_USER_LED1	Not applicable	JP7.10
P8.0	SPIHB_DATA2	R183.1,R201.1,R206.1	Not applicable
P8.1	SPIHB_DATA3	R192.2,R202.1,R207.1	Not applicable
P8.2	SPIHB_DATA4	R184.1,R208.1	Not applicable
P8.3	BB_USER_LED2	Not applicable	JP7.13
P8.4	BB_USER_LED3	Not applicable	JP7.9
P9.0	BB_USER_LED4	Not applicable	JP7.14
P9.1	BB_USER_LED5	Not applicable	JP7.8
P9.2	BB_USER_LED6	Not applicable	JP7.15
P9.3	BB_USER_LED7	Not applicable	JP7.7
P10.0	BB_USER_LED8	TP166	JP6.7
P10.1	BB_USER_LED9	TP167	JP6.6
P10.2	BB_FRA_RXD	Not applicable	Not applicable
P10.3	BB_FRA_TXD	Not applicable	Not applicable
P10.4	BB_FRA_TXEN	Not applicable	Not applicable
P10.5	BB_FRB_RXD	Not applicable	Not applicable
P10.6	BB_FRB_TXD	Not applicable	Not applicable
P10.7	BB_FRB_TXEN	Not applicable	Not applicable
P11.0	SPIHB_DATA5	R191.2,R209.1	Not applicable
P11.1	SPIHB_DATA6	R185.1,R210.1	Not applicable
P11.2	SPIHB_DATA7	R190.2,R211.1	Not applicable
VREFL	VREFL_BB	R19.2	JP5.9
VSSA	Not applicable	R19.1	Not applicable
VDDA	Not applicable	R18.1	Not applicable
VREFH	VREFH_BB	R18.2	JP5.10
P12.0	BB_CAN2_TXD	Not applicable	JP10.8
P12.1	BB_CAN2_RXD	Not applicable	JP10.7
P12.2	GPIO_P12_2	Not applicable	JP10.11
P12.3	GPIO_P12_3	Not applicable	JP10.13
P12.4	BB_CAN4_TXD	Not applicable	JP11.8
P12.5	BB_CAN4_RXD	Not applicable	JP11.7
P12.6	BB_ADC_POT	Not applicable	JP7.11
P12.7	GPIO_P12_7	TP184	JP11.4
VDDIO_2	Not applicable	TP11	Not applicable

Table 4-1. Device Port Pin Connections on Base Board

MCU Port Pin	Connection 1 Signal Name of Schematics	Connection 1 CPU Board Test Point	Connection 1 Base Board Test Point
VSSD	GND	TP2	Not applicable
P13.0	UART_RX	TP185	JP10.4
P13.1	UART_TX	TP186	JP10.3
P13.2	BB_UART0_RTS	Not applicable	JP10.6
P13.3	BB_UART0_CTS	Not applicable	JP10.5
P13.4	BB_FRA_STBN	Not applicable	Not applicable
P13.5	BB_FRA_EN	Not applicable	Not applicable
P13.6	BB_FRA_ERRN	Not applicable	Not applicable
P13.7	BB_FRA_WAKE	Not applicable	Not applicable
P14.0	SS_MCLK	R214.1	Not applicable
P14.1	SS_TX_SCK	TP194	Not applicable
P14.2	SS_TX_WS	TP195	Not applicable
P14.3	SS_TX_SDO	TP196	Not applicable
P14.4	BB_FRB_STBN	Not applicable	Not applicable
P14.5	BB_FRB_EN	Not applicable	Not applicable
P14.6	BB_FRB_ERRN	Not applicable	Not applicable
P14.7	BB_FRB_WAKE	Not applicable	Not applicable
P15.0	BB_CAN6_TXD	TP200	Not applicable
P15.1	BB_CAN6_RXD	TP202	Not applicable
P15.2	BB_LIN0_WAKE	Not applicable	JP1.5
P15.3	BB_LIN2_WAKE	Not applicable	JP2.7
VDDD	Not applicable	TP9	Not applicable
VCCD	Not applicable	TP8	Not applicable
VCCD	Not applicable	TP8	Not applicable
VCCD	Not applicable	TP8	Not applicable
VSSD	GND	TP2	Not applicable
P16.3	BB_LIN3_WAKE	Not applicable	JP2.11
P17.0	BB_LIN4_RXD	Not applicable	JP2.13
P17.1	BB_LIN4_TXD	Not applicable	JP2.14
P17.2	BB_LIN4_SLP	Not applicable	JP2.16
P17.3	BB_LIN4_WAKE	Not applicable	JP2.15
P17.4	BB_LIN5_WAKE	Not applicable	JP1.11
P17.5	BB_LIN5_RXD	Not applicable	JP1.9
P17.6	BB_LIN5_TXD	Not applicable	JP1.10
P17.7	BB_LIN5_SLP	Not applicable	JP1.12
P18.0	SS_CLK_I2S_IF	R215.1	Not applicable
P18.1	SS_RX_SCK	TP214	Not applicable
P18.2	SS_RX_WS	TP216	Not applicable
P18.3	SS_RX_SDI	TP217	Not applicable
P18.4	TRACE_DATA_0	TP219	Not applicable
P18.5	TRACE_DATA_1	TP218	Not applicable
P18.6	TRACE_DATA_2	TP220	Not applicable
P18.7	TRACE_DATA_3	TP221	Not applicable
VDDD	Not applicable	TP9	Not applicable
VSSD	GND	TP2	Not applicable

Table 4-1. Device Port Pin Connections on Base Board

MCU Port Pin	Connection 1 Signal Name of Schematics	Connection 1 CPU Board Test Point	Connection 1 Base Board Test Point
P19.0	GPIO_P19_0	J36.3	Not applicable
P19.1	GPIO_P19_1	J37.3	Not applicable
P19.2	GPIO_P19_2	J38.3	Not applicable
P19.3	GPIO_P19_3	J39.3	Not applicable
P19.4	GPIO_P19_4	J40.3	Not applicable
P20.0	BB_LIN2_RXD	Not applicable	JP2.5
P20.1	BB_LIN2_TXD	Not applicable	JP2.6
P20.2	BB_LIN2_SLP	Not applicable	JP2.8
P20.3	BB_CAN5_TXD	Not applicable	JP11.6
P20.4	BB_CAN5_RXD	Not applicable	JP11.5
P20.5	BB_CAN5_S	Not applicable	JP10.16
P20.6	BB_CAN7_TXD	TP232	Not applicable
P20.7	BB_CAN7_RXD	TP234	Not applicable
P21.0	CPU_WCO_IN	R21.2	Not applicable
P21.1	CPU_WCO_OUT	R22.2	Not applicable
P21.2	CPU_ECO_IN	R23.2	Not applicable
P21.3	CPU_ECO_OUT	R24.2	Not applicable
P21.4	HIBERNATE_WAKEUP	J14.1	Not applicable
XRES	CPU_XRES	J18.1	Not applicable
VDDD	Not applicable	TP9	Not applicable
VSSD	GND	TP2	Not applicable
VSSD	GND	TP2	Not applicable
VCCD	Not applicable	TP8	Not applicable
P21.5	BB_LIN0_RXD	Not applicable	JP1.3
P21.6	BB_LIN0_TXD	Not applicable	JP1.4
P21.7	BB_LIN0_SLP	Not applicable	JP1.6
DRV_VOUT	DRV_VOUT	R9.1,R12.1,TP244	Not applicable
P22.1	EXT_PS_CTL0	J43.2,TP6	Not applicable
P22.2	EXT_PS_CTL1	J42.2,J44.2	Not applicable
P22.3	GPIO_P22_3	Not applicable	Not applicable
P22.4	TRACE_CLOCK	R46.2,TP247	Not applicable
P22.5	BB_LIN3_RXD	Not applicable	JP2.9
P22.6	BB_LIN3_TXD	TP251	JP2.10
P22.7	BB_LIN3_SLP	Not applicable	JP2.12
P23.0	BB_CAN3_TXD	TP250	JP3.12
P23.1	BB_CAN3_RXD	TP254	JP3.14
P23.2	GPIO_P23_2	Not applicable	JP10.14
P23.3	BB_CAN7_WAKE	Not applicable	JP11.3
P23.4	SWJ_SWO_TDO	J37.1	Not applicable
P23.5	SWJ_SWCLK_TCLK	J40.1	Not applicable
P23.6	SWJ_SWDIO_TMS	J39.1	Not applicable
P23.7	SWJ_SWDOE_TDI	J38.1	Not applicable
VDDD	Not applicable	TP9	Not applicable

The first column in Table 4-1 lists the pin number on the MCU, followed by the port pin name.

For each pin, the connected peripheral or net on the base board is depicted by the Netname of Schematics column.

The Base Board Test Point column indicates the place where the signal can be probed on the base board. For example, JP6.15 refers to the 15th pin on the JP6 header.

A value of #NA in the Test Point column indicates that the signal is unavailable on the JPx pin header on the base board. The signal might still be available on separate pin headers near the respective peripheral.

For details on the alternate functionality of each MCU pin, see the device datasheet.

Note: If there are pins with more than one connection to the base board, make sure that no two peripherals are driven at the same time. The unused peripheral jumpers must be disconnected before using the other connection.

4.1.2 Reset Switch

The correspondence between the Reset Switch and port number is given in Table 4-2.

Table 4-2. Reset Switch

Switch	Part No.	Port Name
Reset Switch	SW5	XRES

4.1.3 Hibernate Wakeup Switch

The correspondence between the Hibernate Wakeup Switch and port number is given in Table 4-3.

Table 4-3. Hibernate Wakeup Switch

Switch	Part No.	Port Name
Hibernate Wakeup Switch	SW3	P21.4

4.1.4 User Switches

The correspondence between the User Switches and port number is given in Table 4-4.

Table 4-4. User Switches

Switch	Part No.	Port Name
User SW1	SW2	P3.4
User SW2	SW4	P3.5

4.1.5 User LEDs

The correspondence between the User LEDs and port number is given in Table 4-5.

Table 4-5. User LEDs

Switch	Part No.	Port Name
User LED1	LED4	P3.2
User LED2	LED5	P3.3

4.1.6 JTAG Select Jumpers

The correspondence between the JTAG Select Jumpers and selected functions is given in Table 4-6.

Table 4-6. JTAG Select Jumpers

Jumpers Name	Part No.	Connection	Function
TRSTN	J36	1-2 (default)	SWJ_TRSTN
		2-3	GPIO_P19_0
SWO_TDO	J37	1-2 (default)	SWJ_SWO_TDO
		2-3	GPIO_P19_1
SWDOE_TDI	J38	1-2 (default)	SWJ_SWDOE_TDI
		2-3	GPIO_P19_2
SWDIO_TMS	J39	1-2 (default)	SWJ_SWDIO_TMS
		2-3	GPIO_P19_3
SWCLK_TCLK	J40	1-2 (default)	SWCLK_TCLK
		2-3	GPIO_P19_4

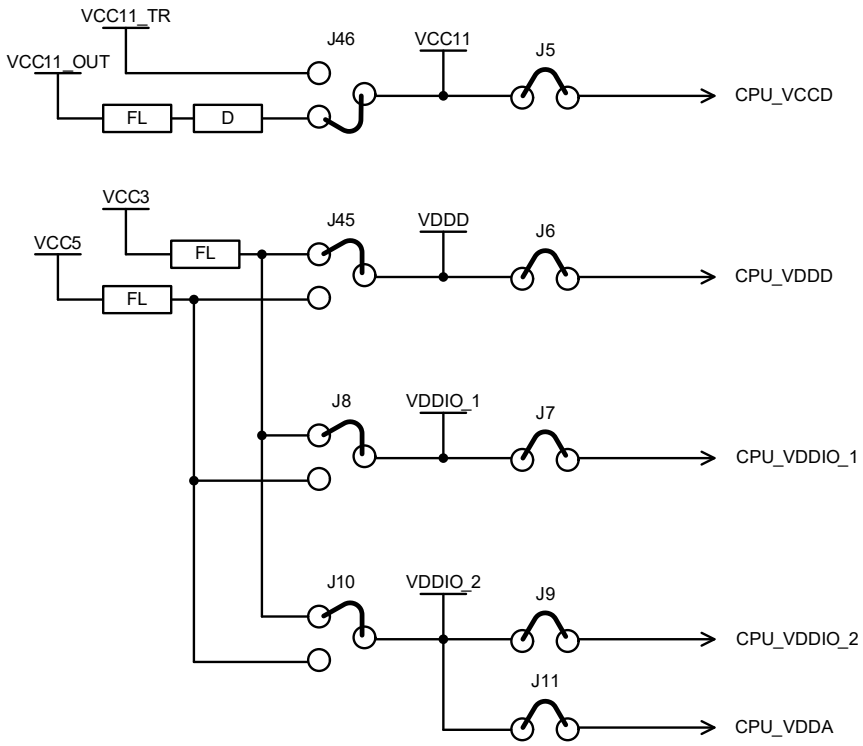
4.2 Power Supply Settings

Power Supply Settings are shown in Table 4-7 and Figure 4-1.

Table 4-7. Power Supply Jumpers Settings

Jumper	Pin	MCU Power	Remarks
J46	1-2	VCC11 = VCC11_TR	From PASS TRANSISTOR
	2-3 (default)	VCC11 = VCC11_PMIC	From S6BP501A
J45	1-2 (default)	VDDD = +3.3 V	Short Jumper - J6
	2-3	VDDD = +5.0 V	
J8	1-2 (default)	VDDIO_1 = +3.3 V	Short Jumper - J7
	2-3	VDDIO_1 = +5.0 V	
J10	1-2 (default)	VDDIO_2 = +3.3 V	Short Jumper - J9
	2-3	VDDIO_2 = +5.0 V	
	1-2 (default)	VDDA = +3.3 V	Short Jumper - J11
	2-3	VDDA = +5.0 V	

Figure 4-1. Power Supply Jumpers Settings



4.3 External Power Supply Control Signals Settings

Jumper Settings of the External Power Supply Control Signals from MCU are shown in Table 4-8.

Table 4-8. External Power Supply Control Signals Jumper Settings

Jumpers Name	PASS Transistor	S6BP501A	Remarks
EXT_PS_CTL0	J43	J41	J43 open (default)
			J41 close (default)
EXT_PS_CTL1	J44	J42	J44 open (default)
			J42 close (default)

4.4 Ethernet Settings

Ethernet Settings are shown in Table 4-9.

Table 4-9. Ethernet Settings

Function Status	Jumper	Settings	Remarks
Ethernet is enabled	J28	Closed	
Ethernet is disabled		Open	

4.5 Settings

Settings are shown in Table 4-10.

Table 4-10. Settings

Function Status	Jumper	Settings	Remarks
is enabled	J30	Closed	
is disabled		Open	

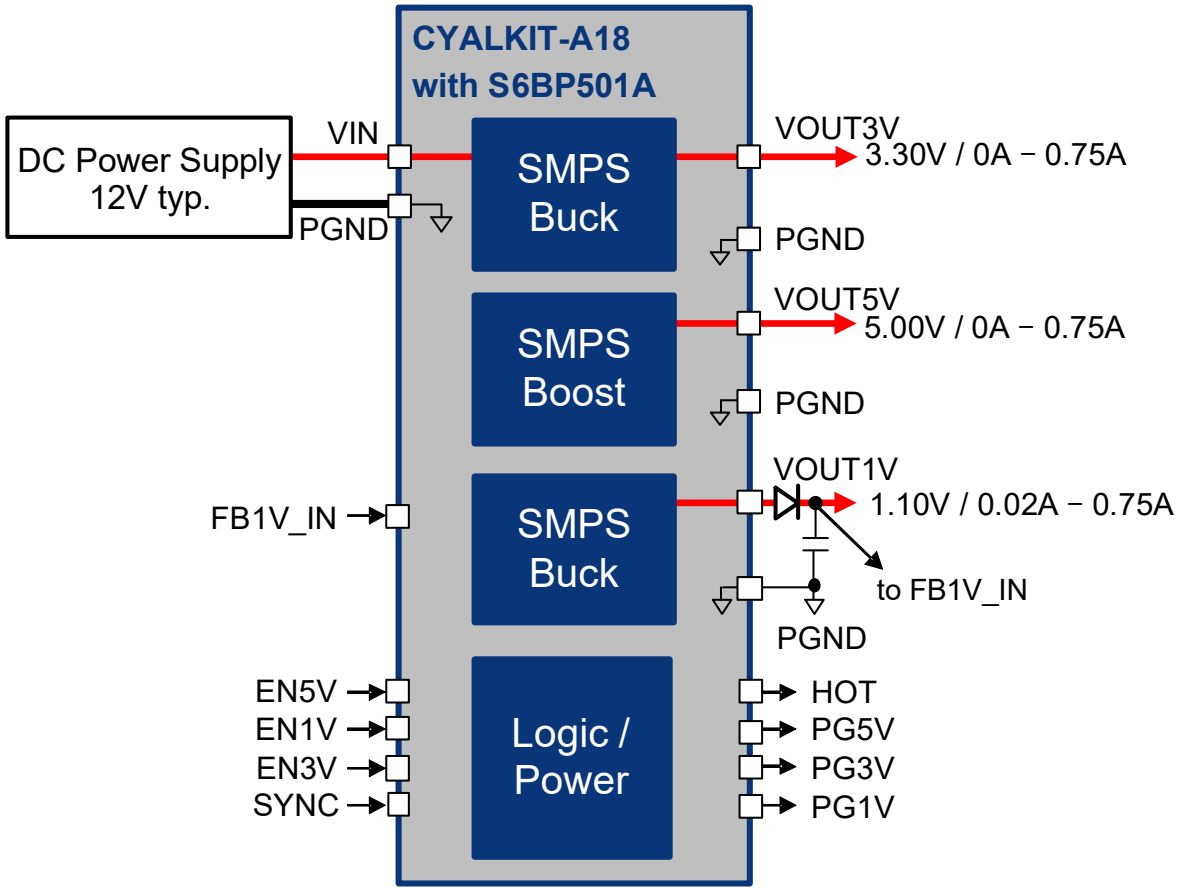
5. Power Management IC (PMIC)

5.1 Power Management IC (PMIC) Module

5.1.1 PMIC Module - CYALKIT-A18

CYALKIT-A18 is the PMIC module for the power block of an automotive application with CYT4B Series MCU. The PMIC Module implements the Cypress PMIC S6BP501A and is optimized for power supply of CYT4B Series MCU. 1.1 V output to supply to VCCD of CYT4B Series MCU needs external schottky barrier diode (SBD), output capacitor and constant load current no less than 20 mA.

Figure 5-1. Evaluation Board Block Diagram



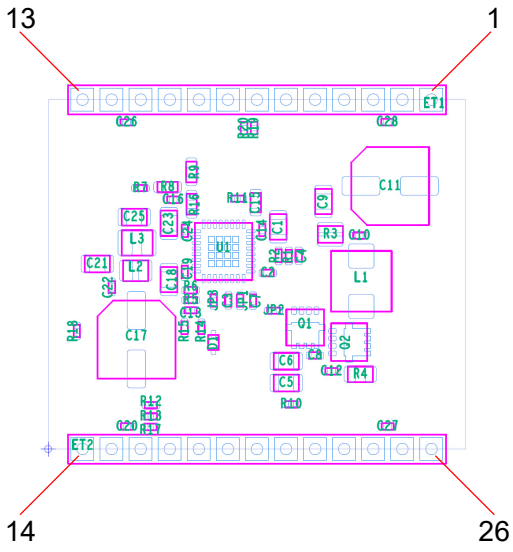
*SMPS: Switching Mode Power Supply

5.1.2 Input/Output Pin Descriptions

Table 5-1. Input/Output Pin Descriptions

Connector Symbol		I/O	Function Description
1, 2	VOUT3V	O	3.3 V power rail output terminal (0 A - 0.75 A)
3, 4	PGND	O	Ground terminal
5	SYNC	I	Mode setting or external clock input terminal Refer to the S6BP501A datasheet
6	PG1V	O	Power good terminal of 1.1 V power rail
7	PG3V	O	Power good terminal of 3.3 V power rail
8	PG5V	O	Power good terminal of 5 V power rail
9	FB1V_IN	I	Feed-back terminal for 1.1 V power rail
10, 11	PGND	–	Ground terminal
12, 13	VOUT1V	O	1.1 V output terminal (0 A - 0.75 A)
14, 15	VOUT5V	O	5 V output terminal (0 A - 0.75 A)
16, 17	PGND	–	Ground terminal
18	HOT	O	Thermal warning output terminal
19	EN5V	I	5 V power rail output enable terminal
20	EN3V	I	3.3 V power rail output enable terminal
21	EN1V	I	1.1 V power rail output enable terminal
22	N.C.	N.C.	No connection
23, 24	PGND	–	Ground terminal
25, 26	VIN	I	DC power supply terminal (4.5 V-42 V, 12 V typ.)

Figure 5-2. Pin Layout



A. Schematics of CPU Board

Figure A-1. Schematic (1/27)

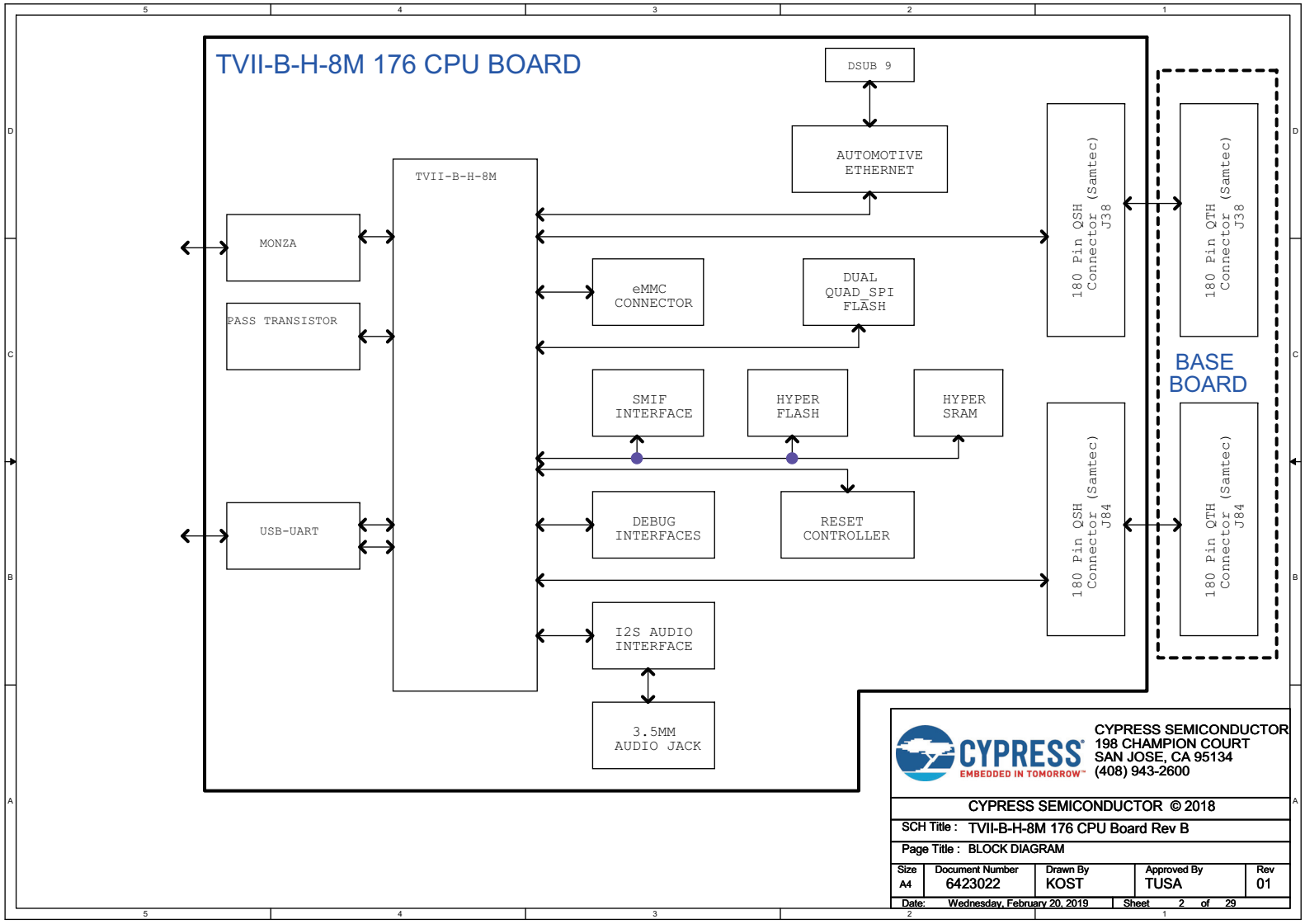


Figure A-2. Schematic (2/27)

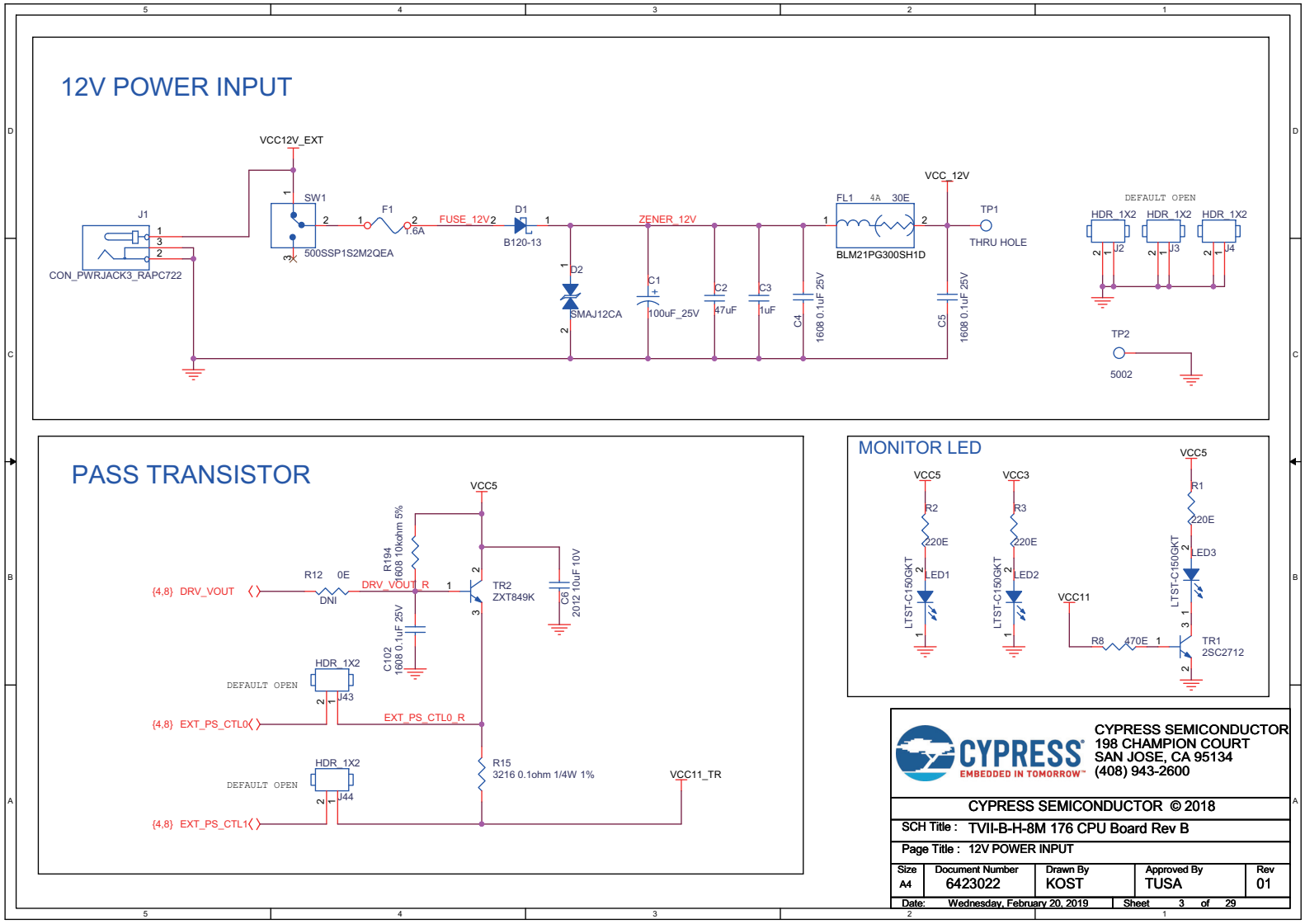


Figure A-3. Schematic (3/27)

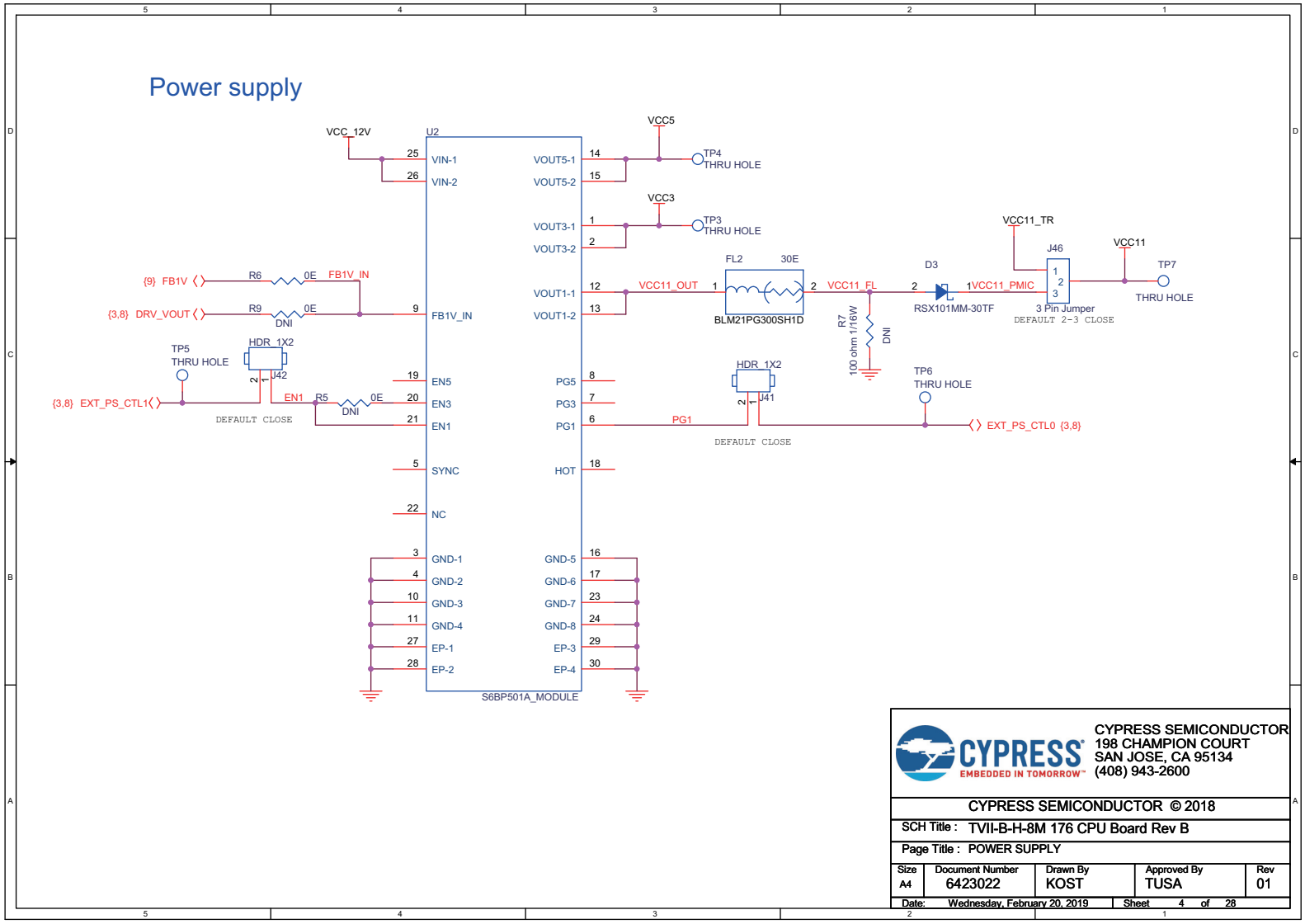


Figure A-4. Schematic (4/27)

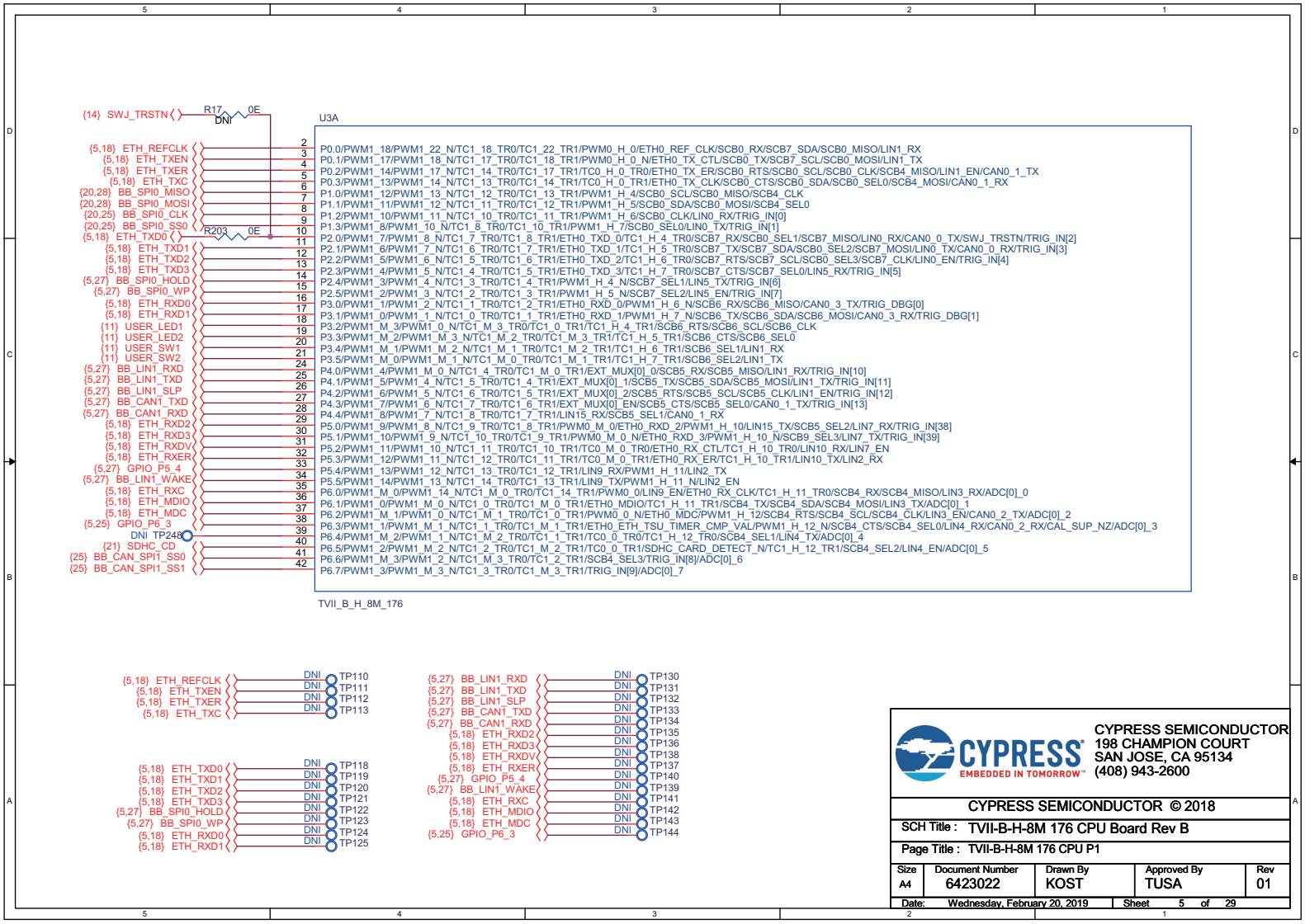


Figure A-5. Schematic (5/27)

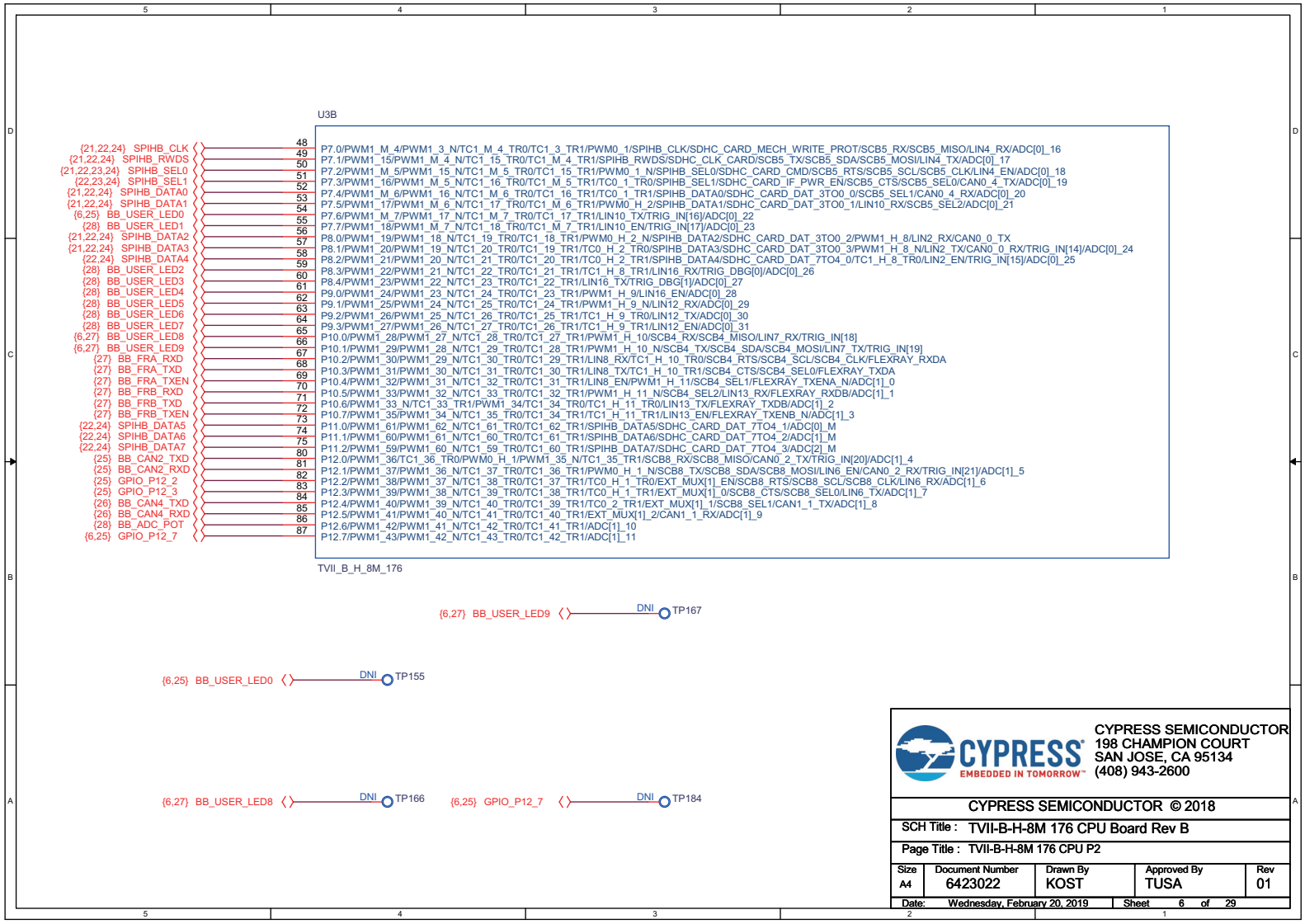


Figure A-6. Schematic (6/27)

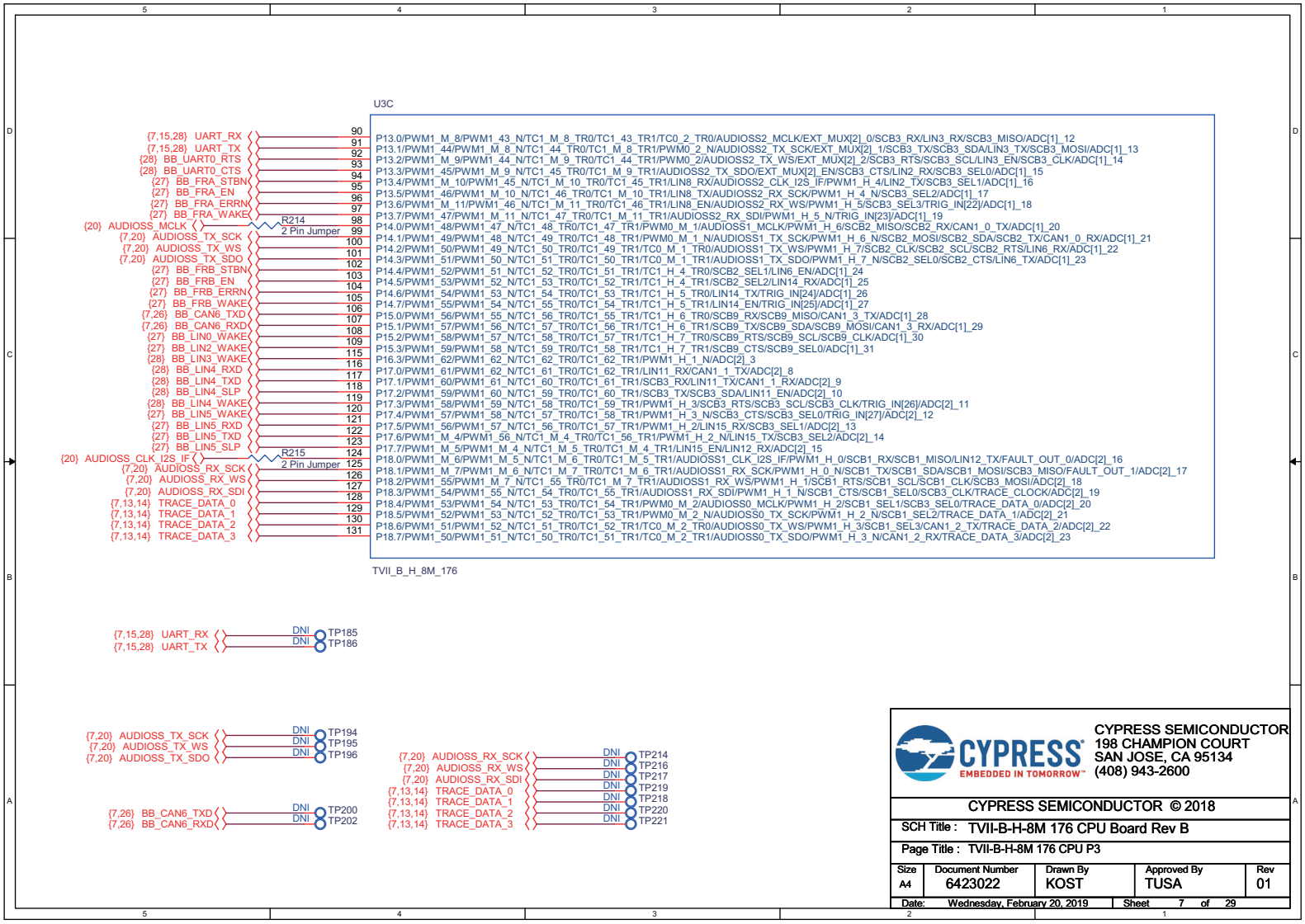


Figure A-7. Schematic (7/27)

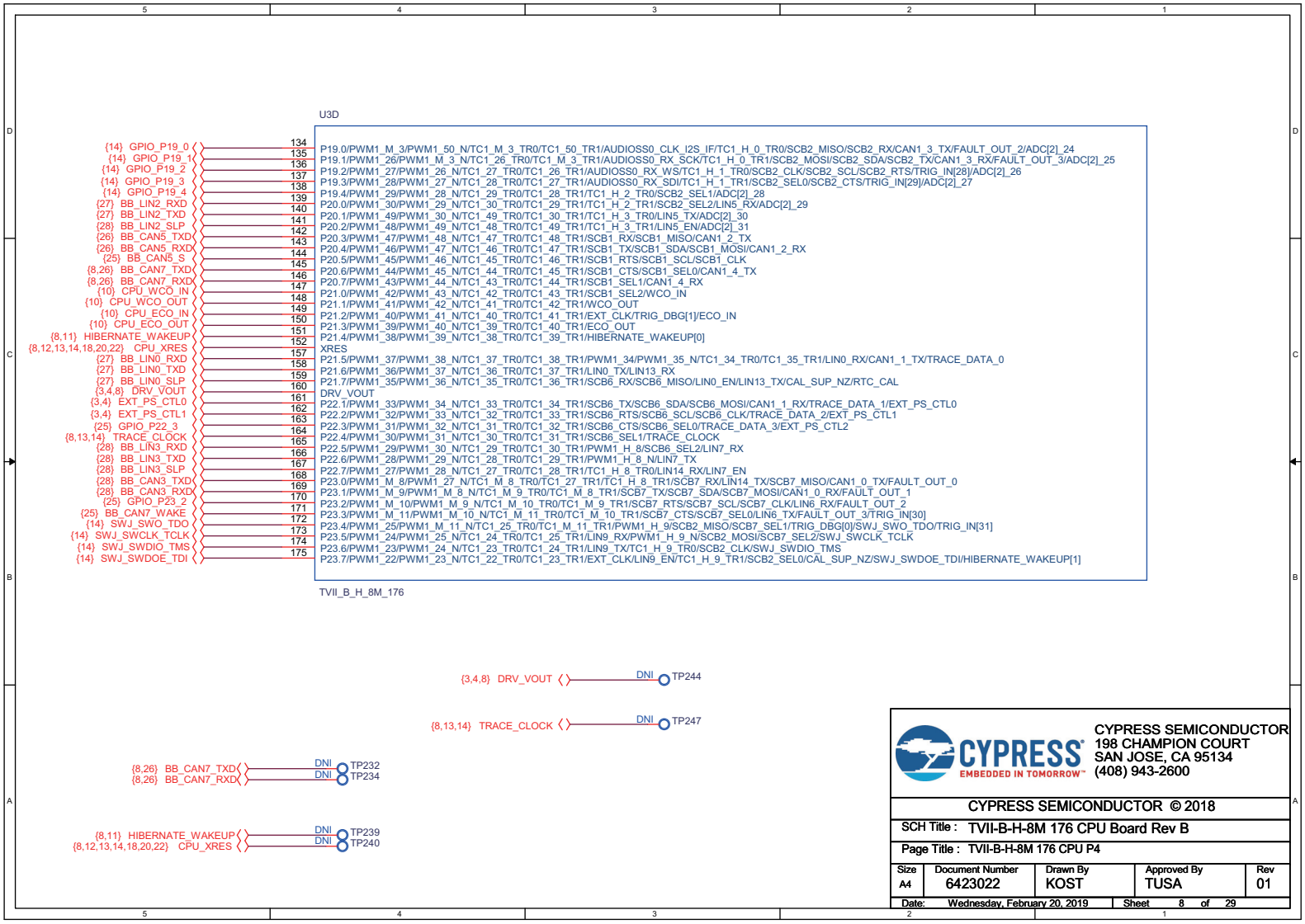


Figure A-8. Schematic (8/27)

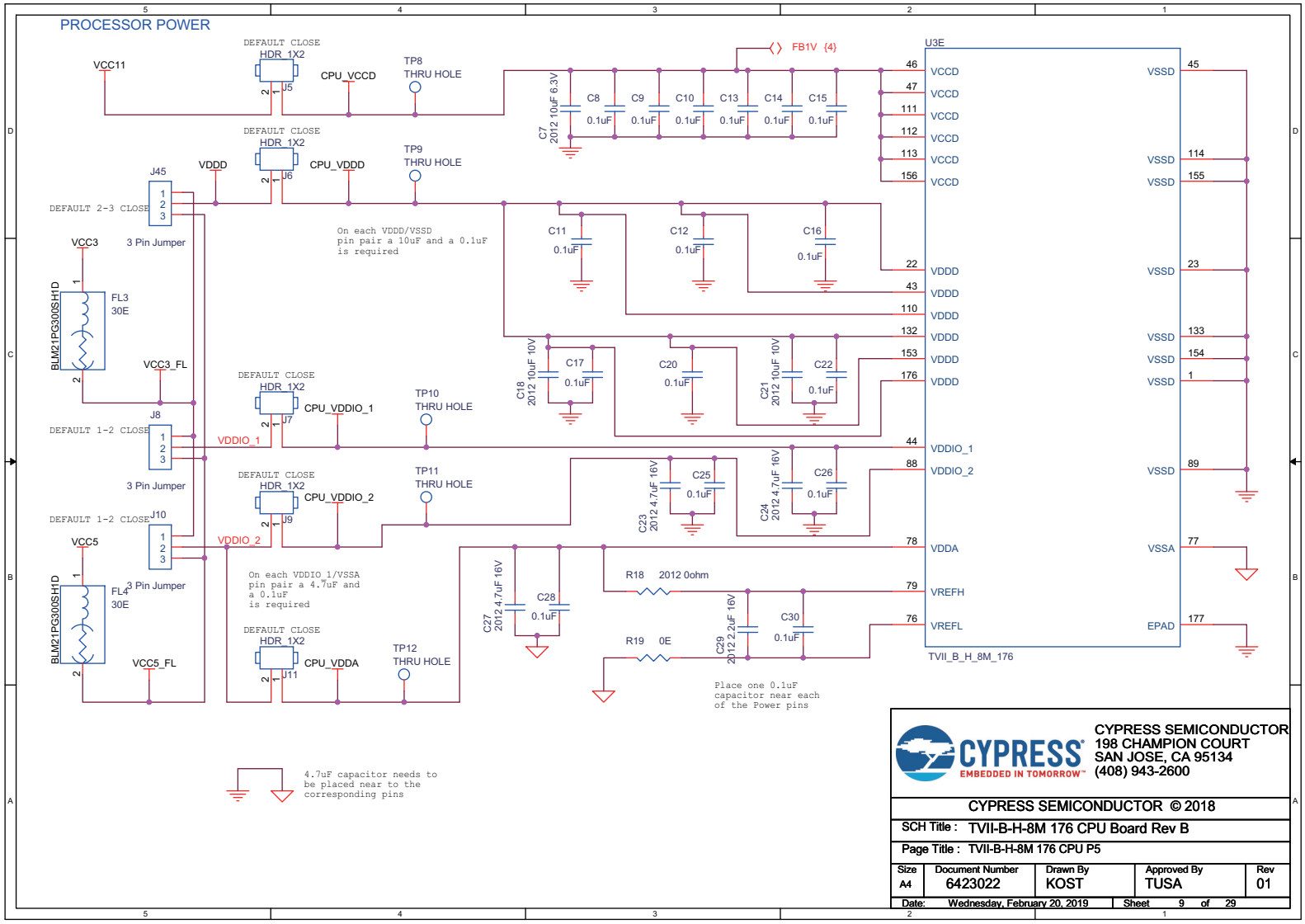


Figure A-9. Schematic (9/27)

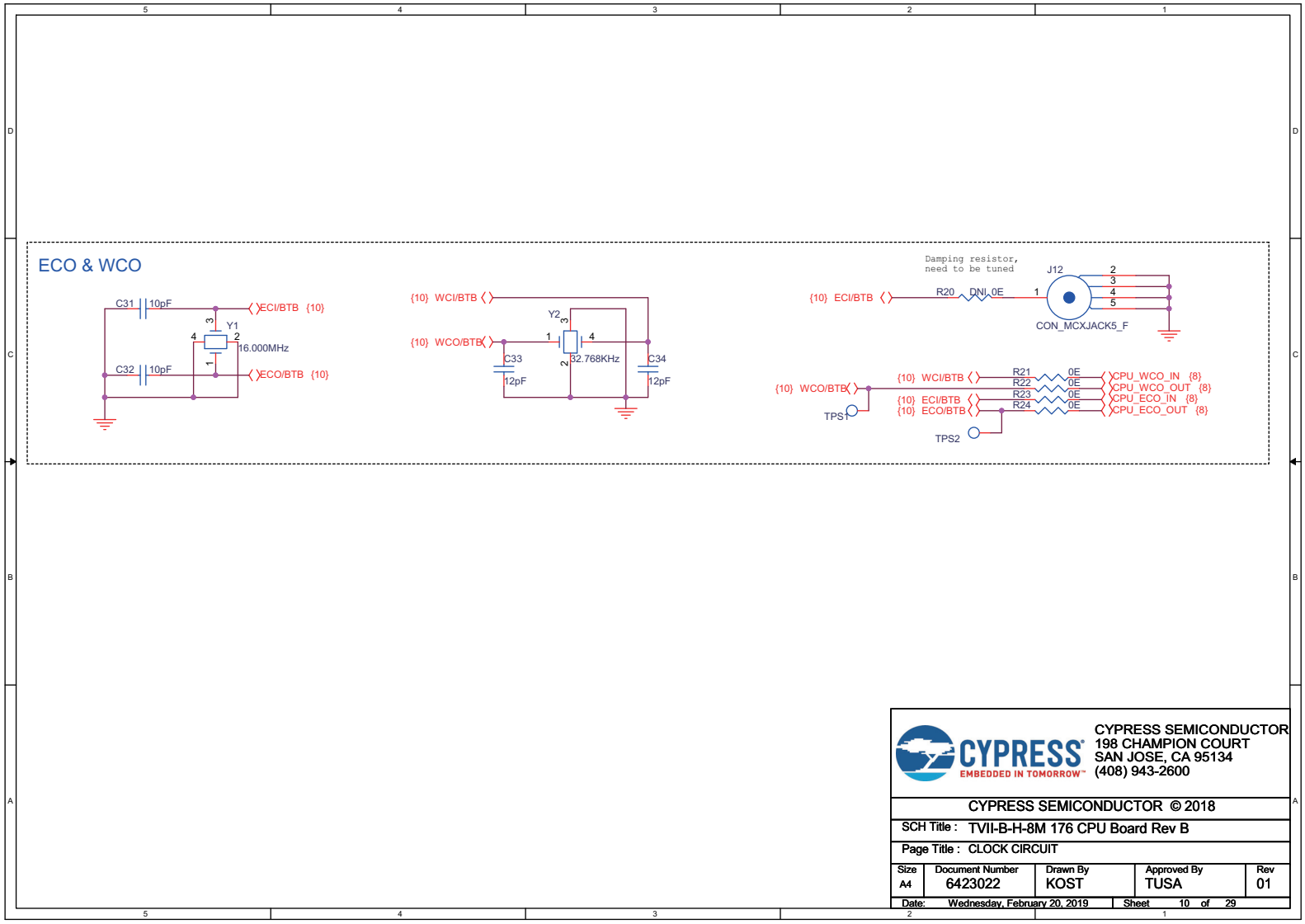


Figure A-10. Schematic (10/27)

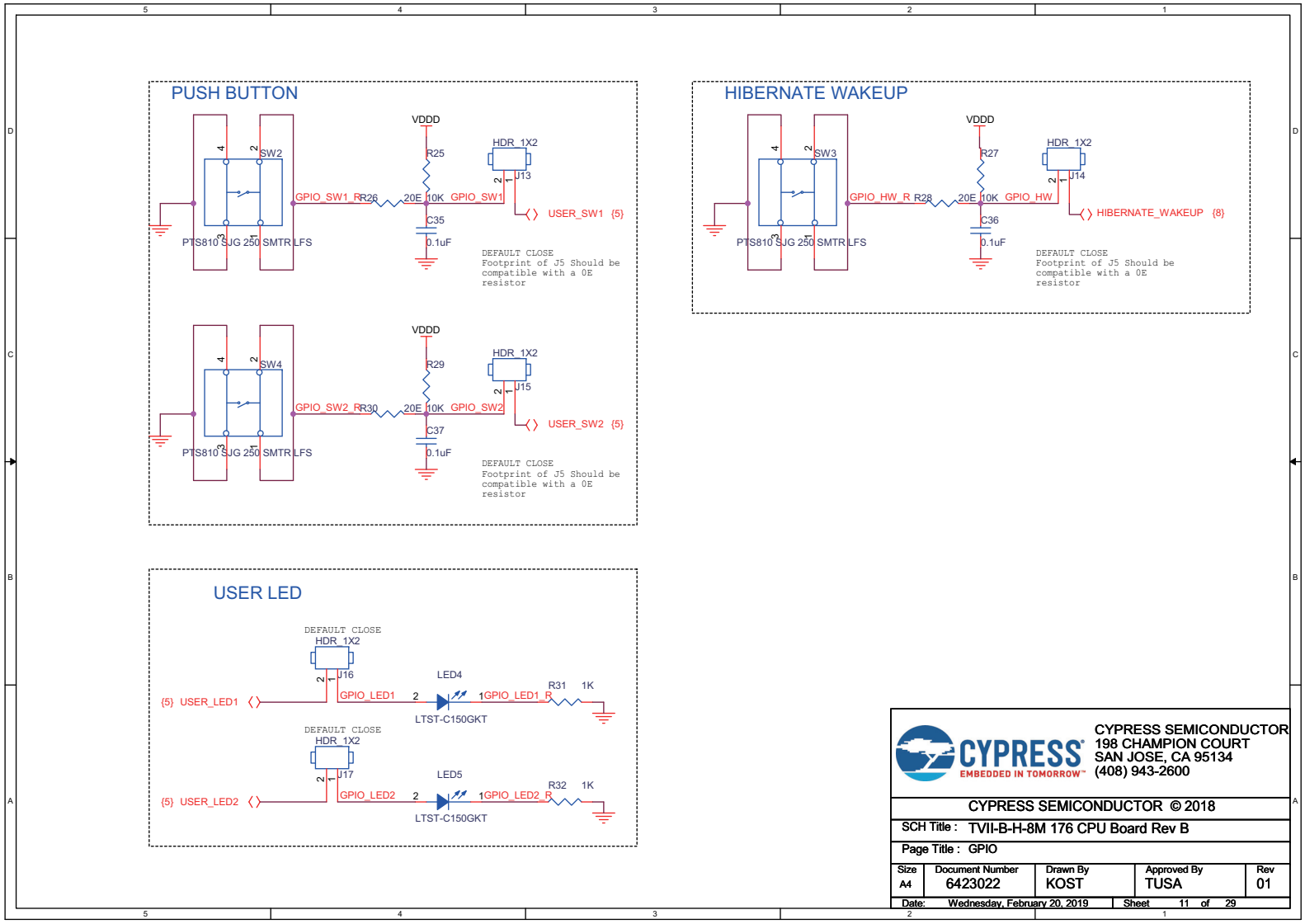


Figure A-11. Schematic (11/27)

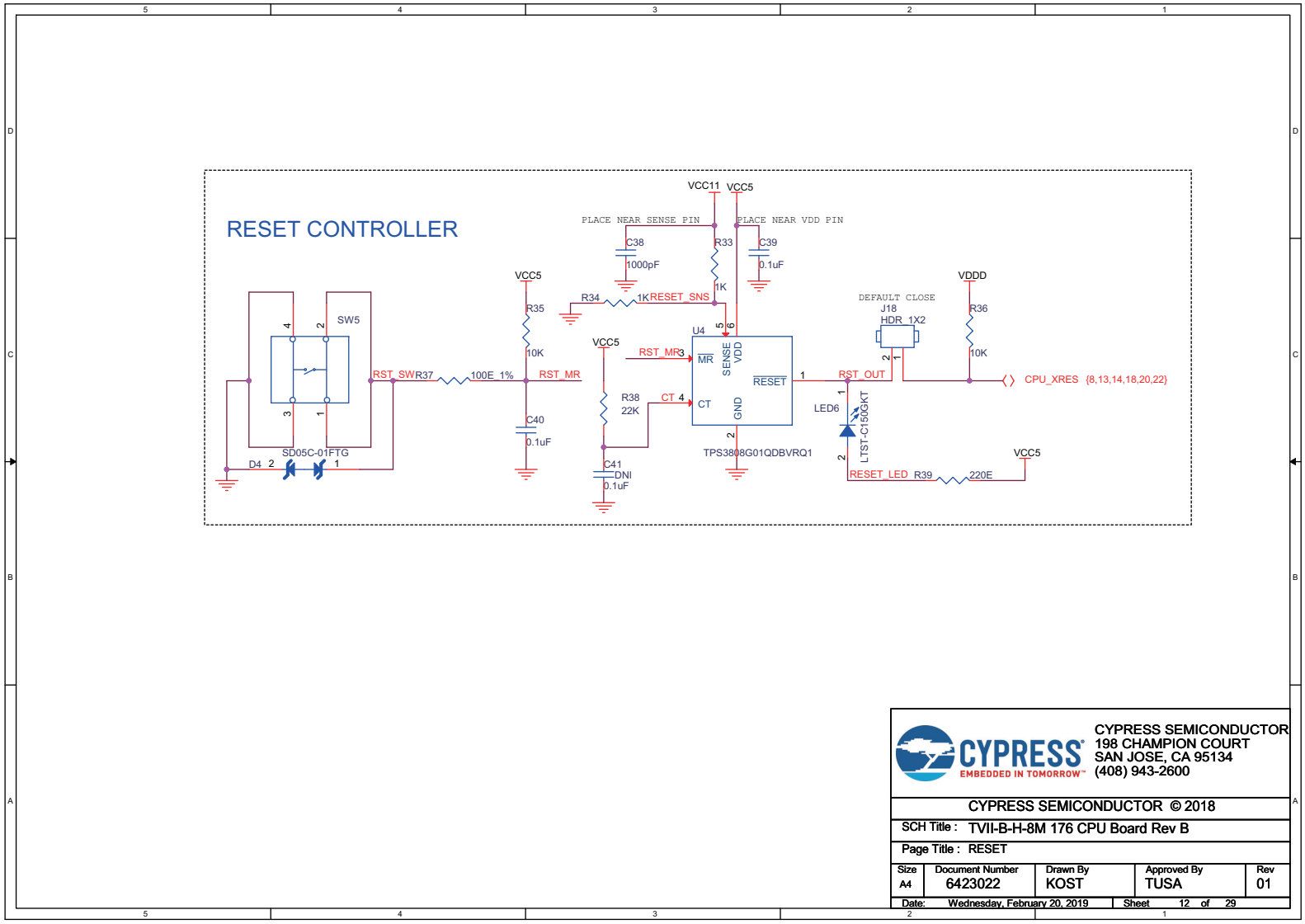


Figure A-12. Schematic (12/27)

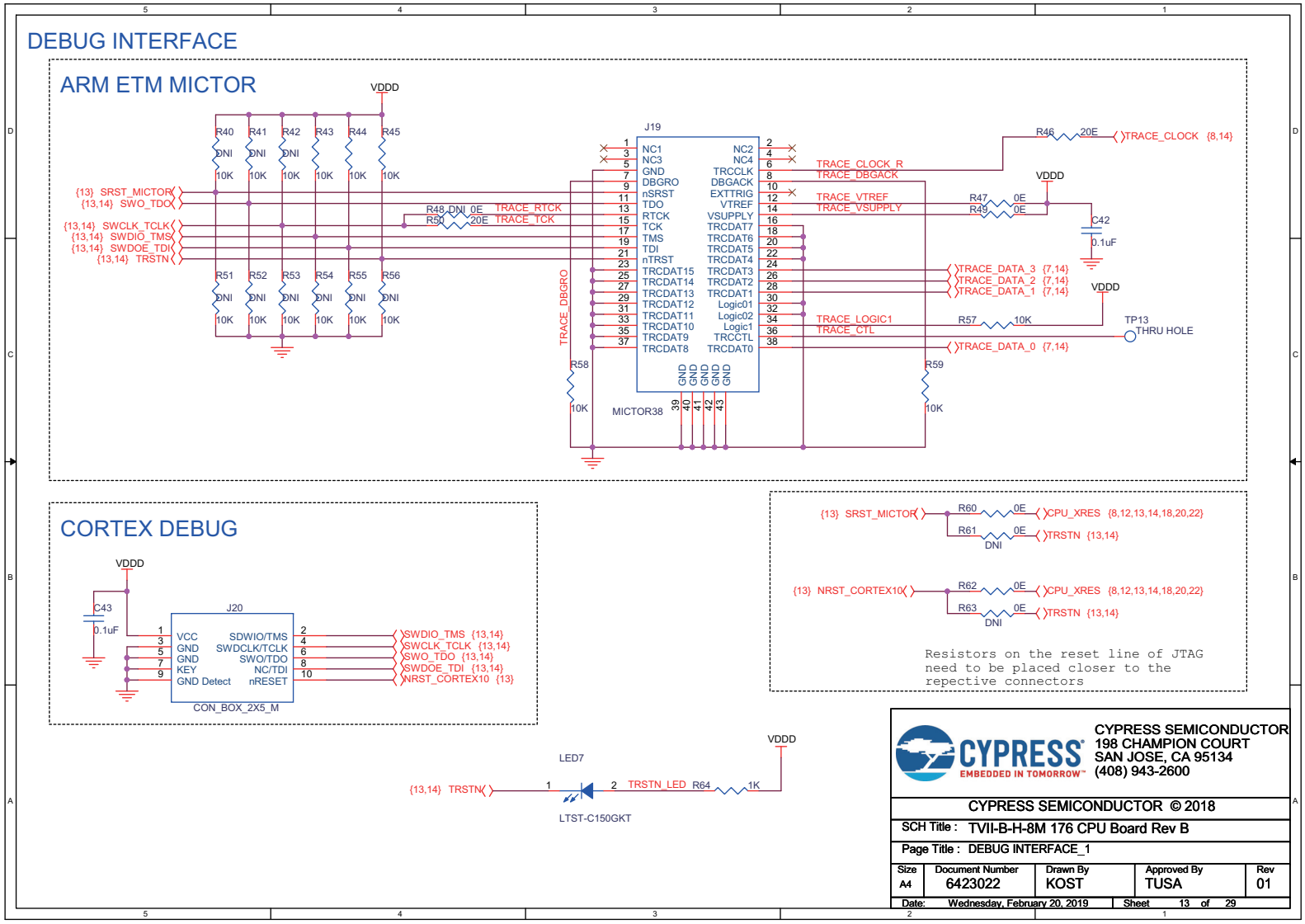


Figure A-13. Schematic (13/27)

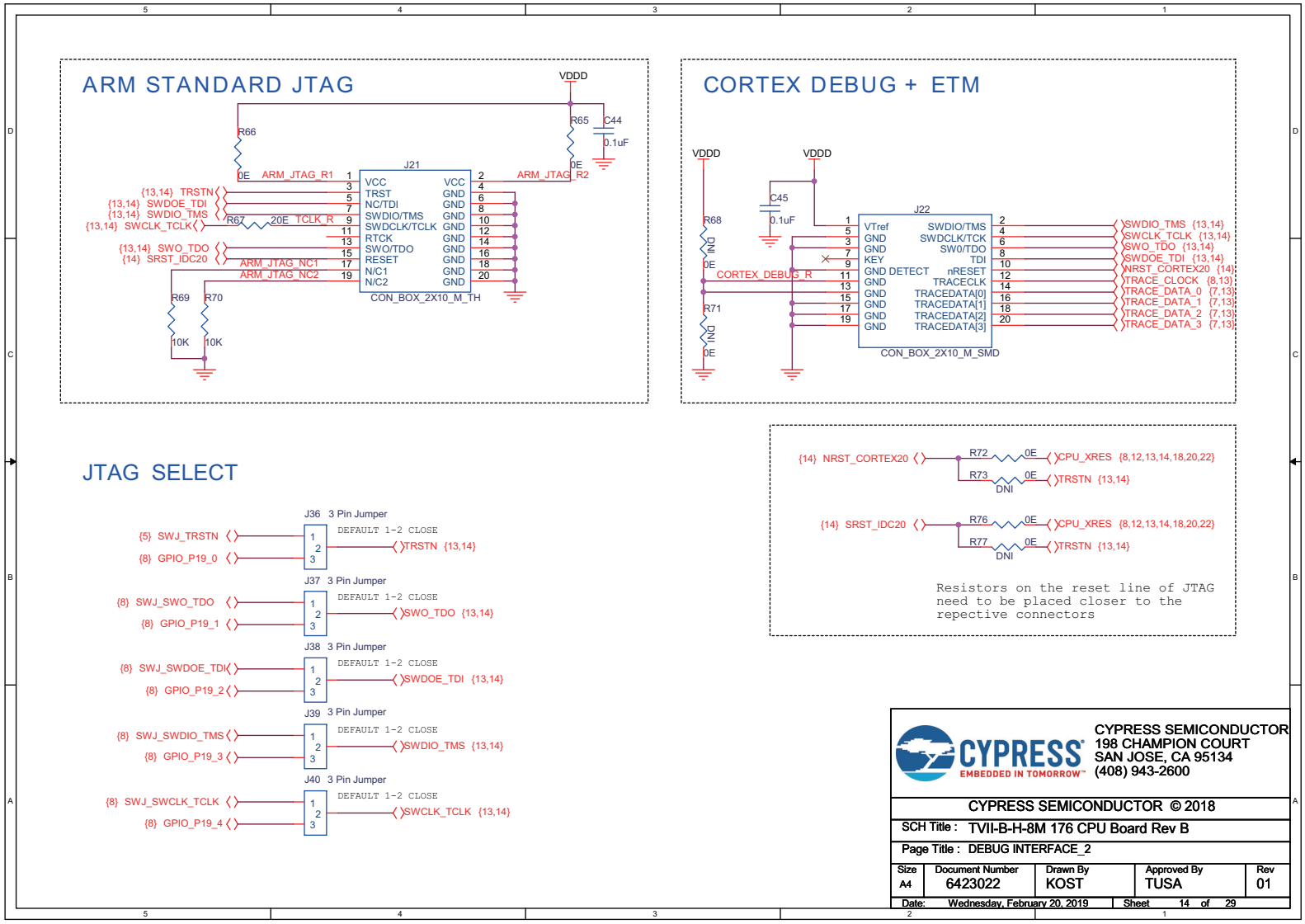


Figure A-14. Schematic (14/27)

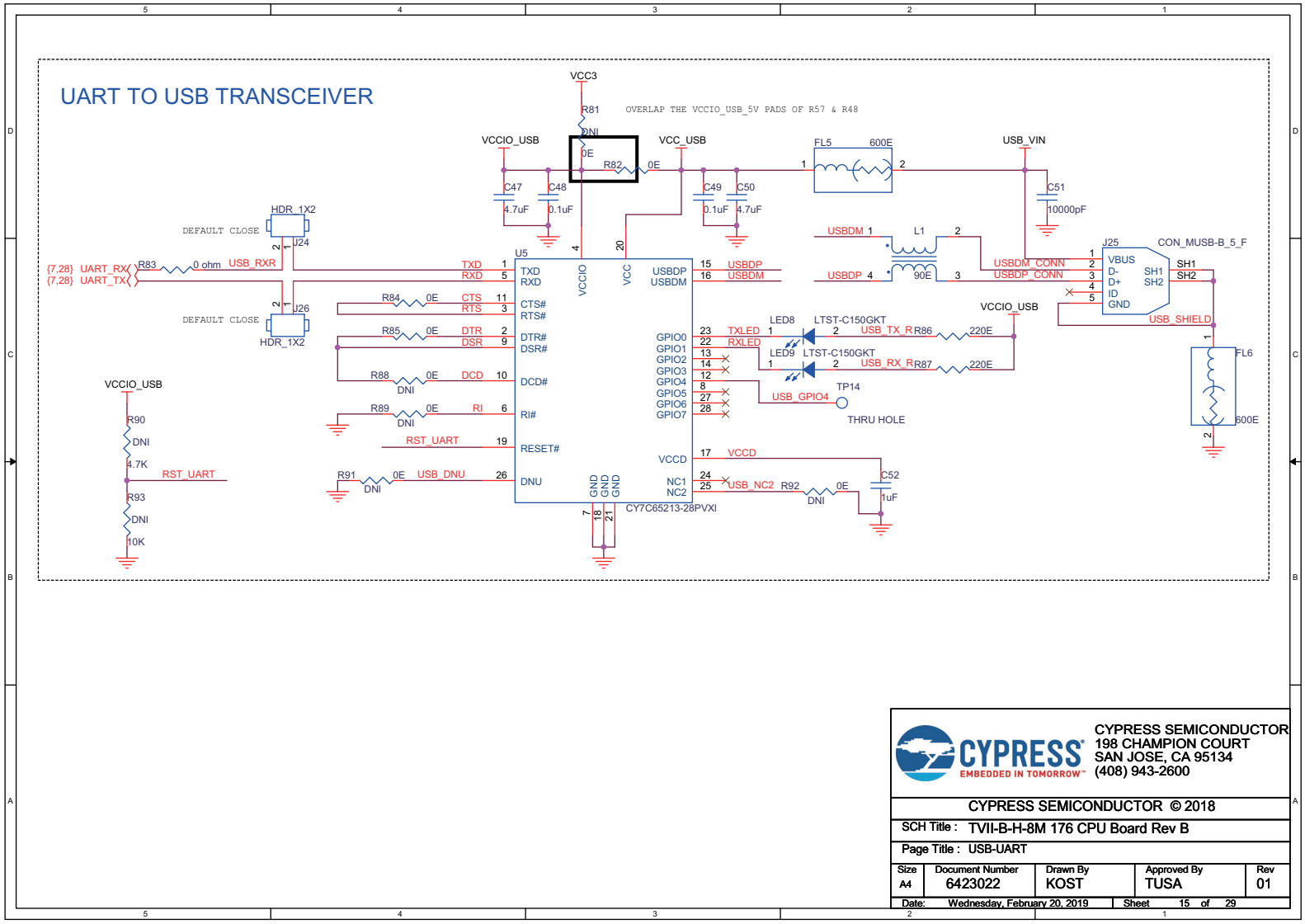


Figure A-15. Schematic (15/27)

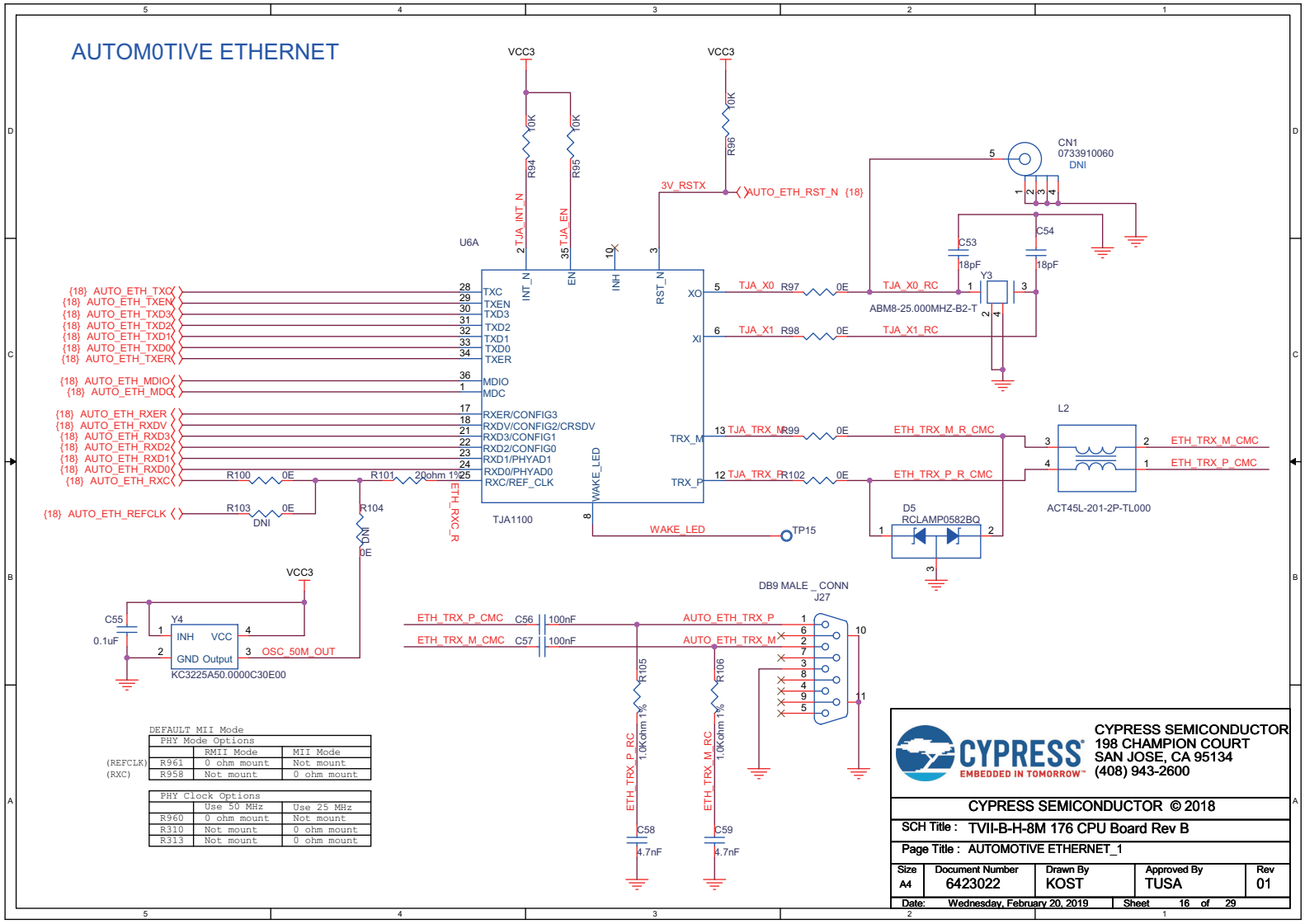


Figure A-16. Schematic (16/27)

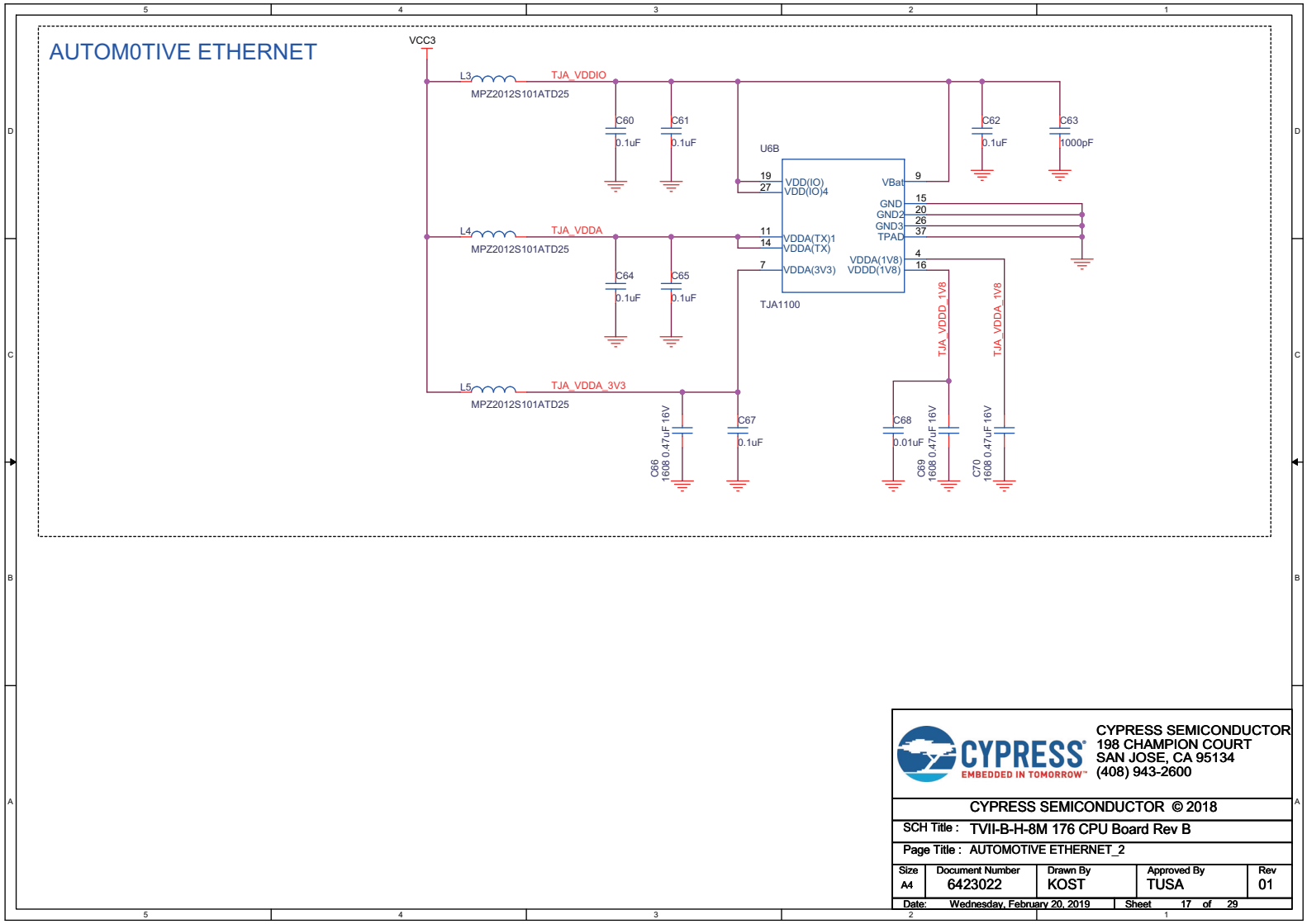


Figure A-17. Schematic (17/27)

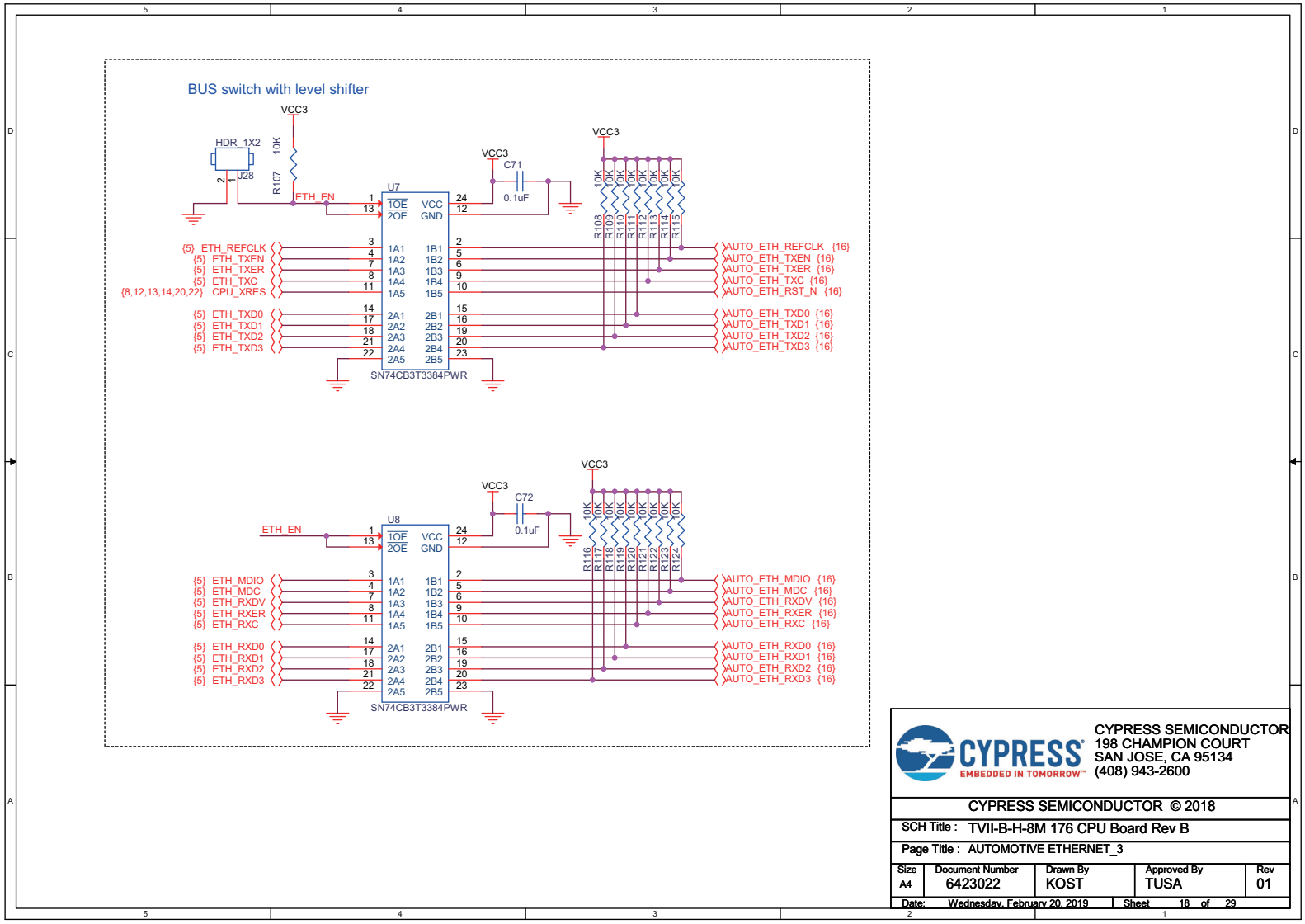


Figure A-18. Schematic (18/27)

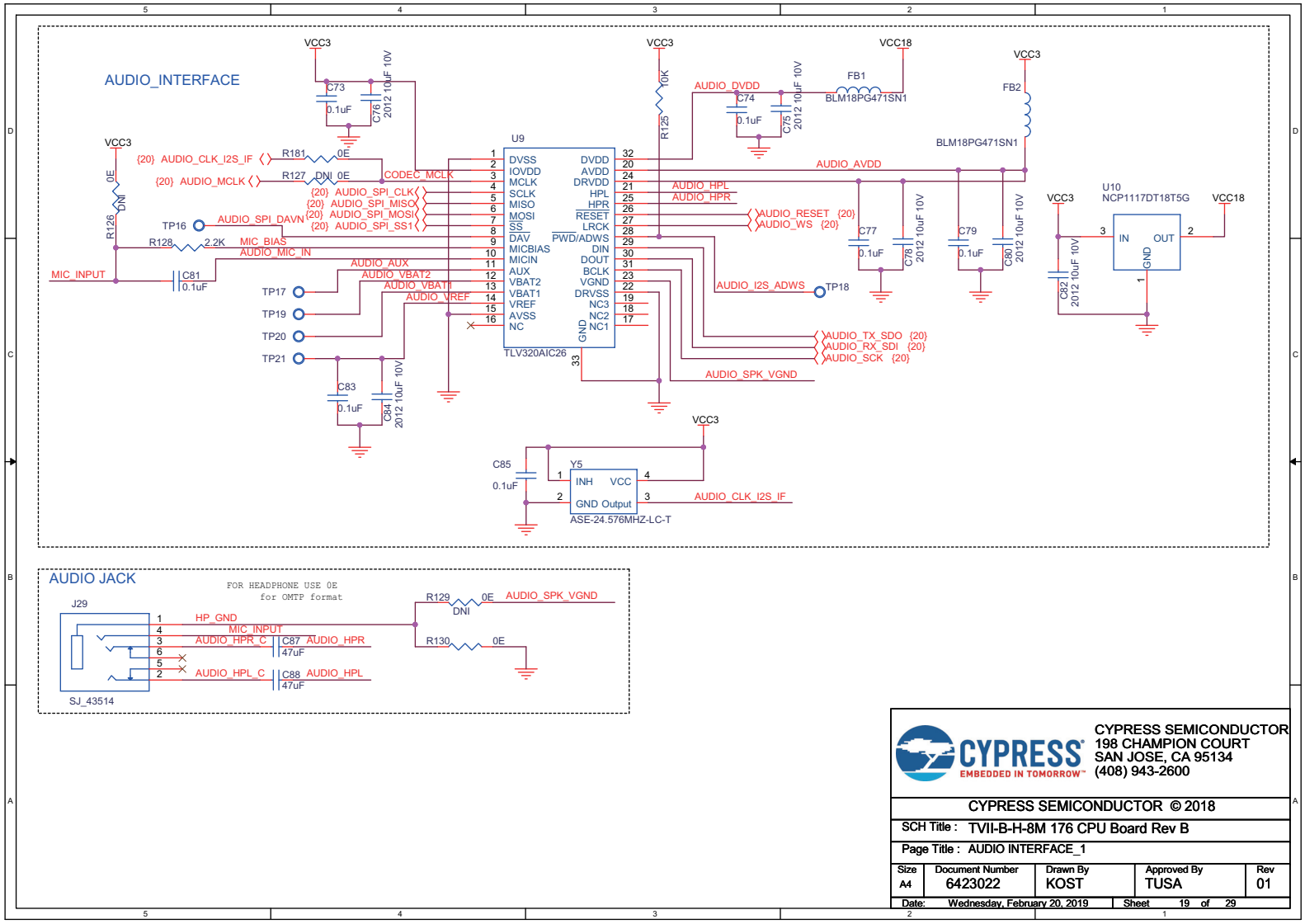


Figure A-19. Schematic (19/27)

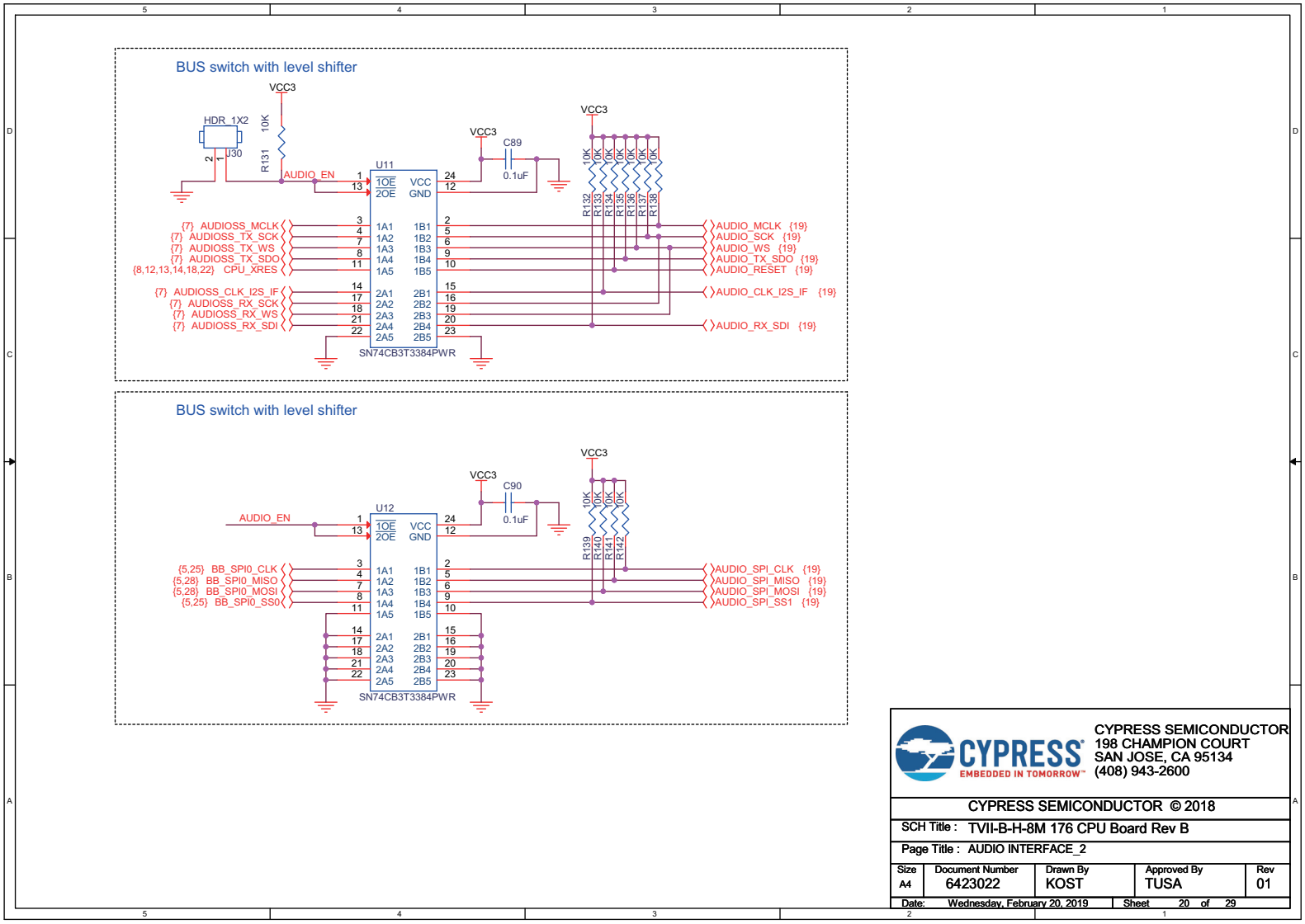


Figure A-20. Schematic (20/27)

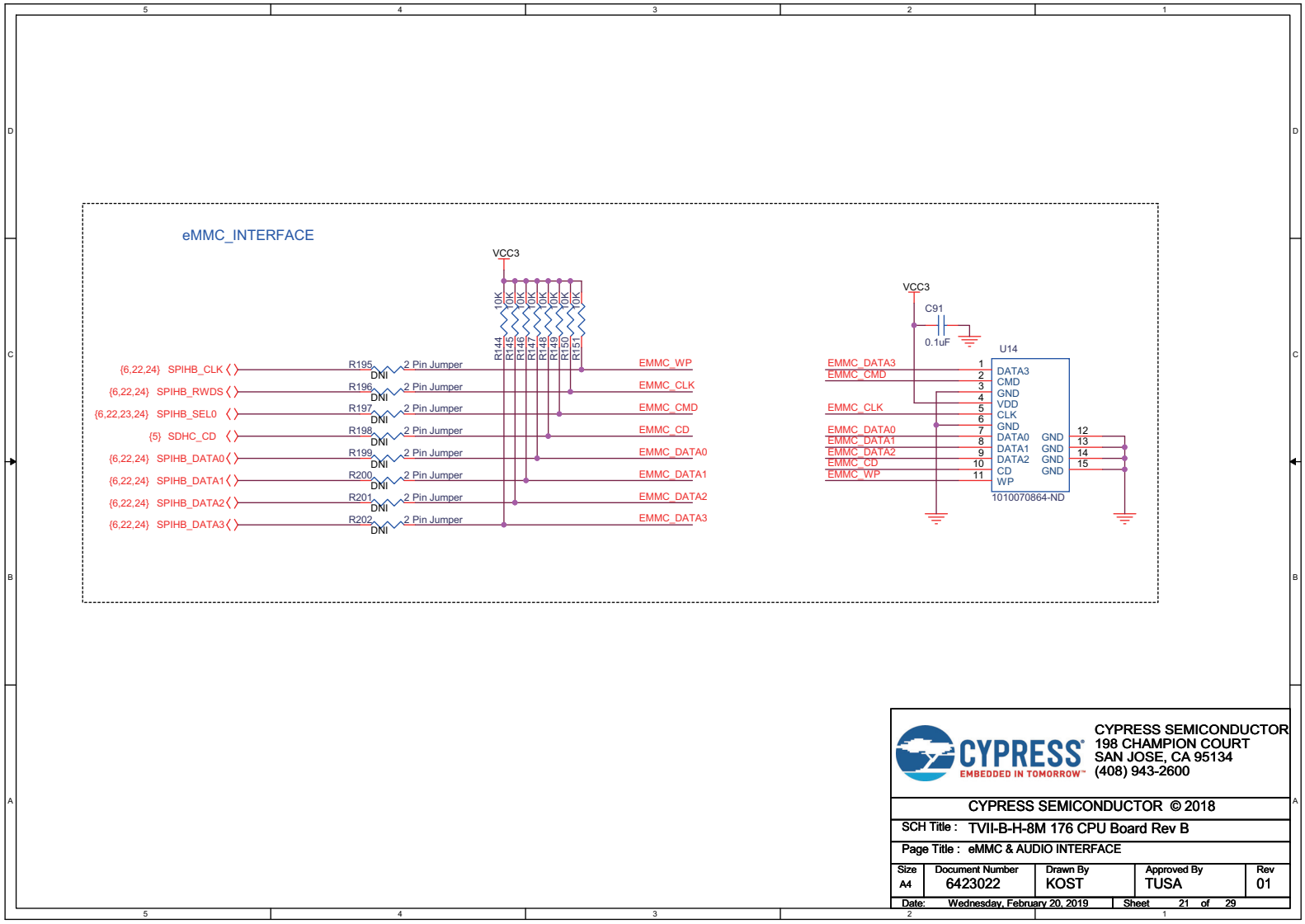


Figure A-21. Schematic (21/27)

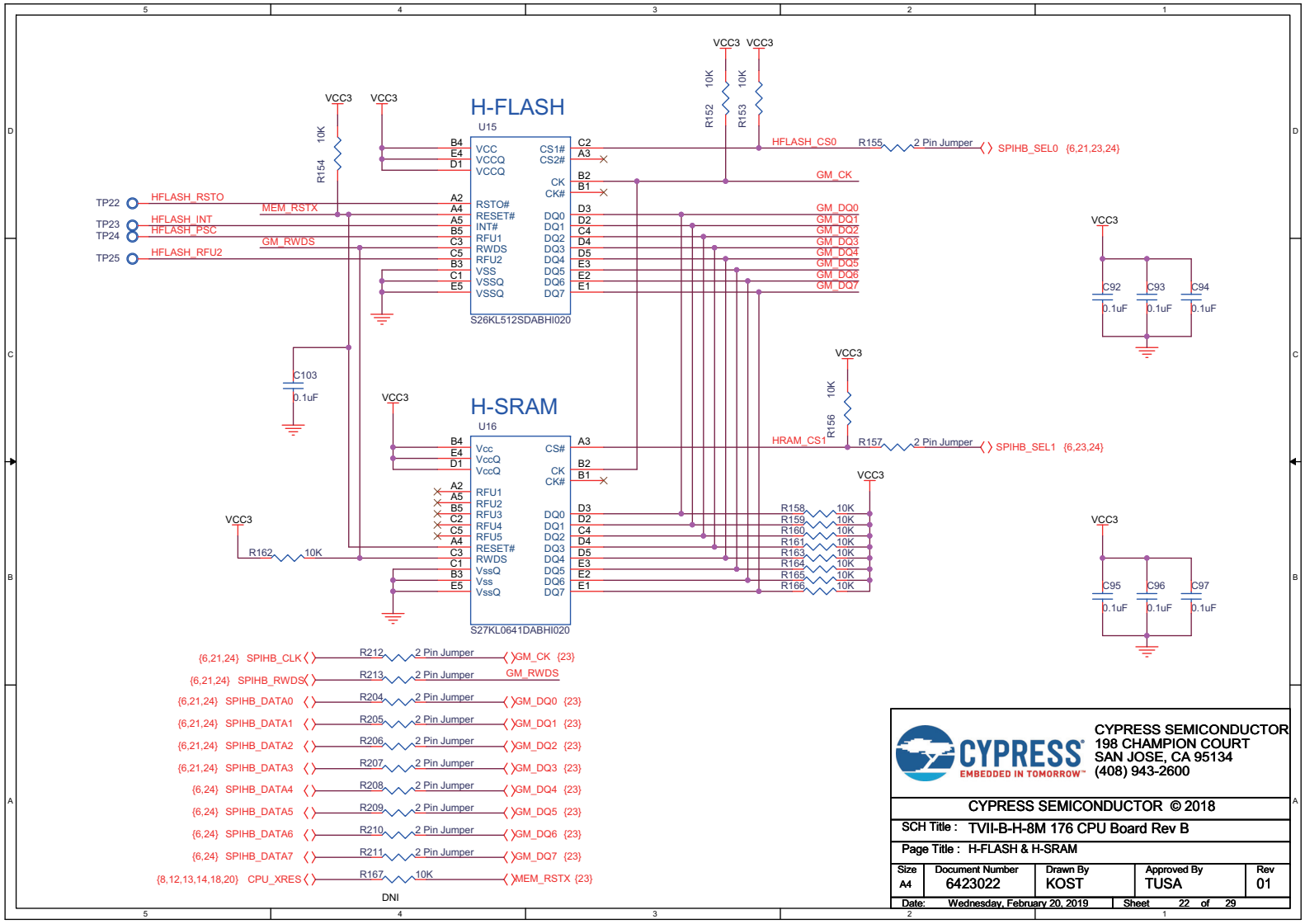


Figure A-22. Schematic (22/27)

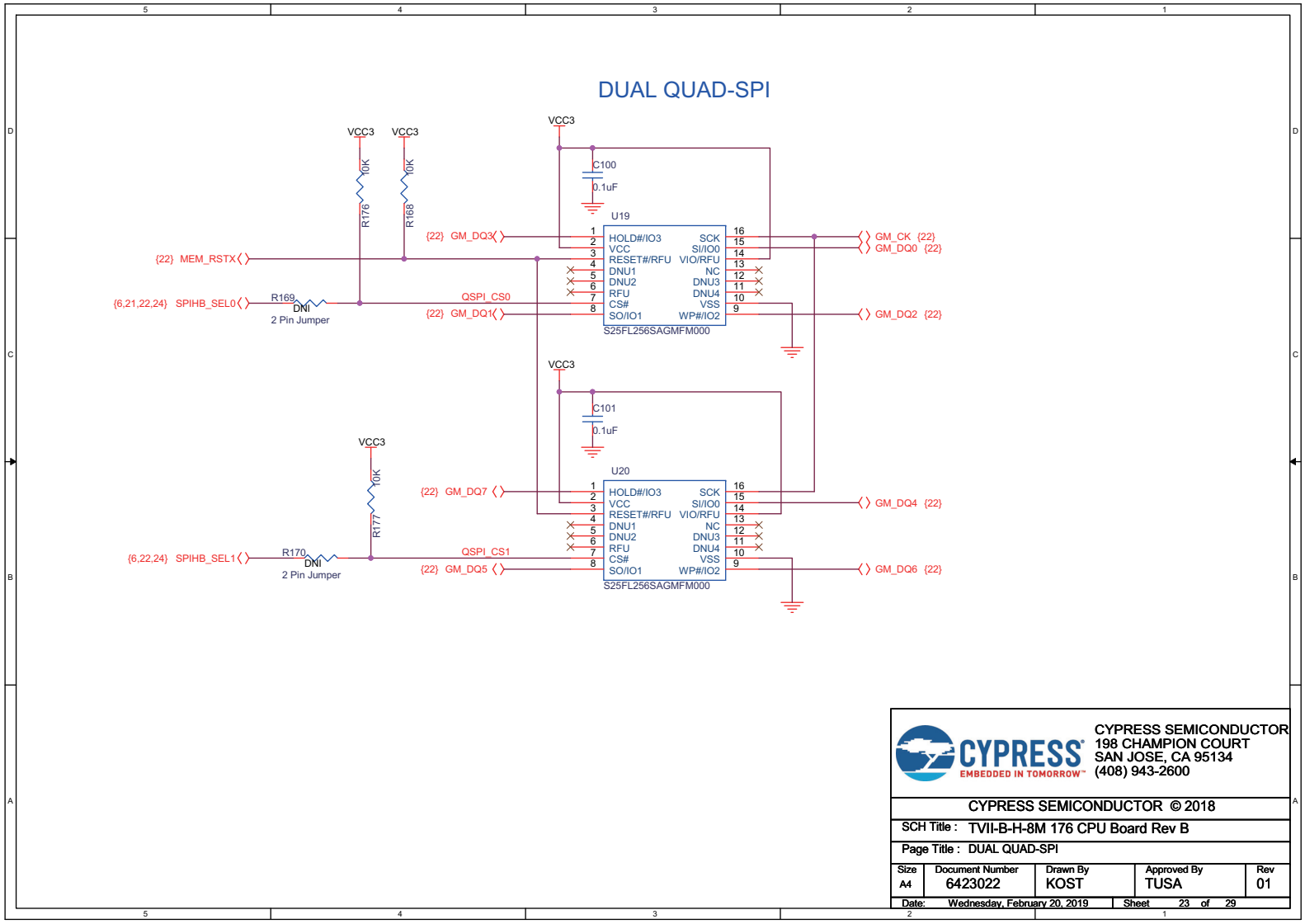


Figure A-23. Schematic (23/27)

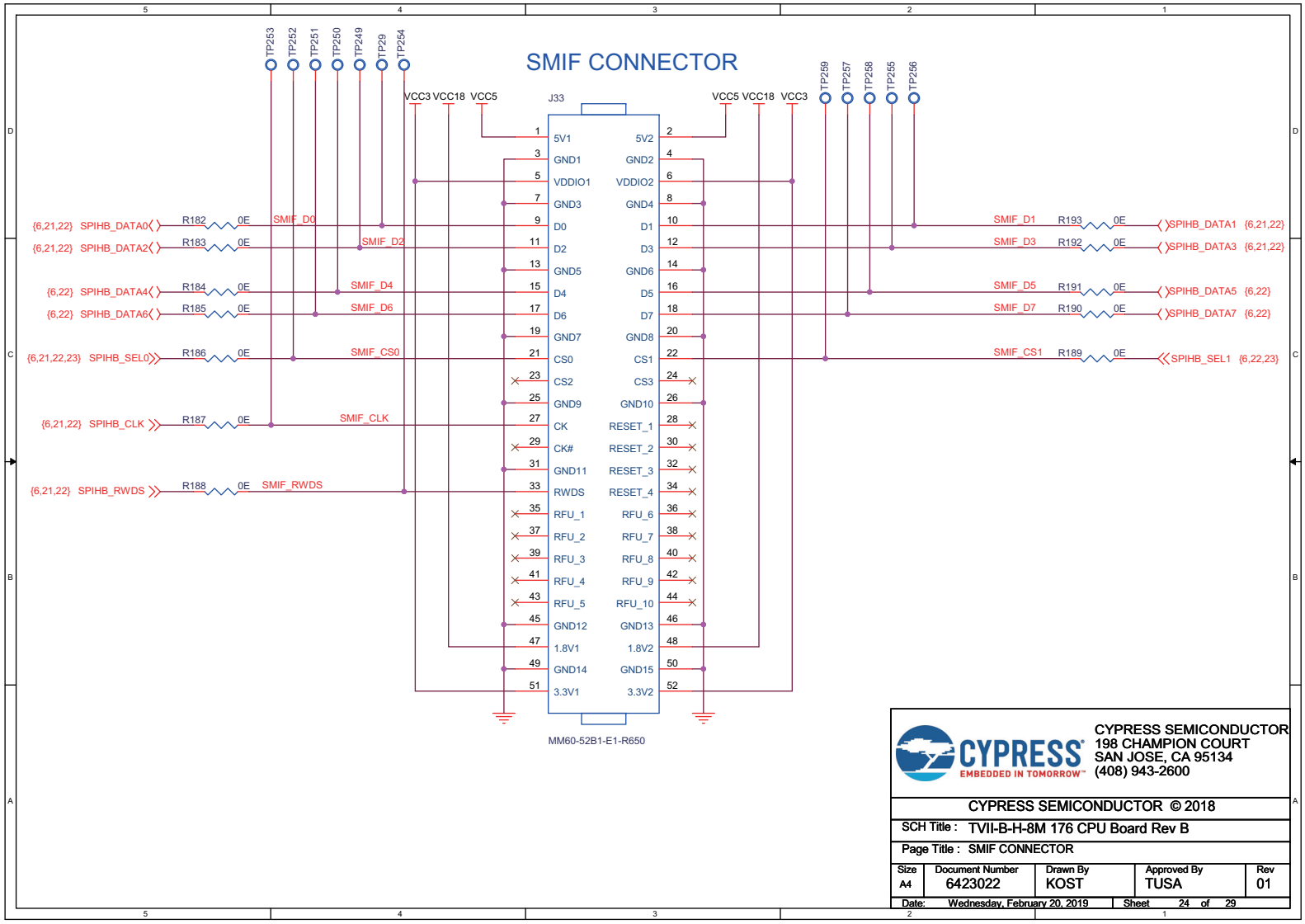


Figure A-24. Schematic (24/27)

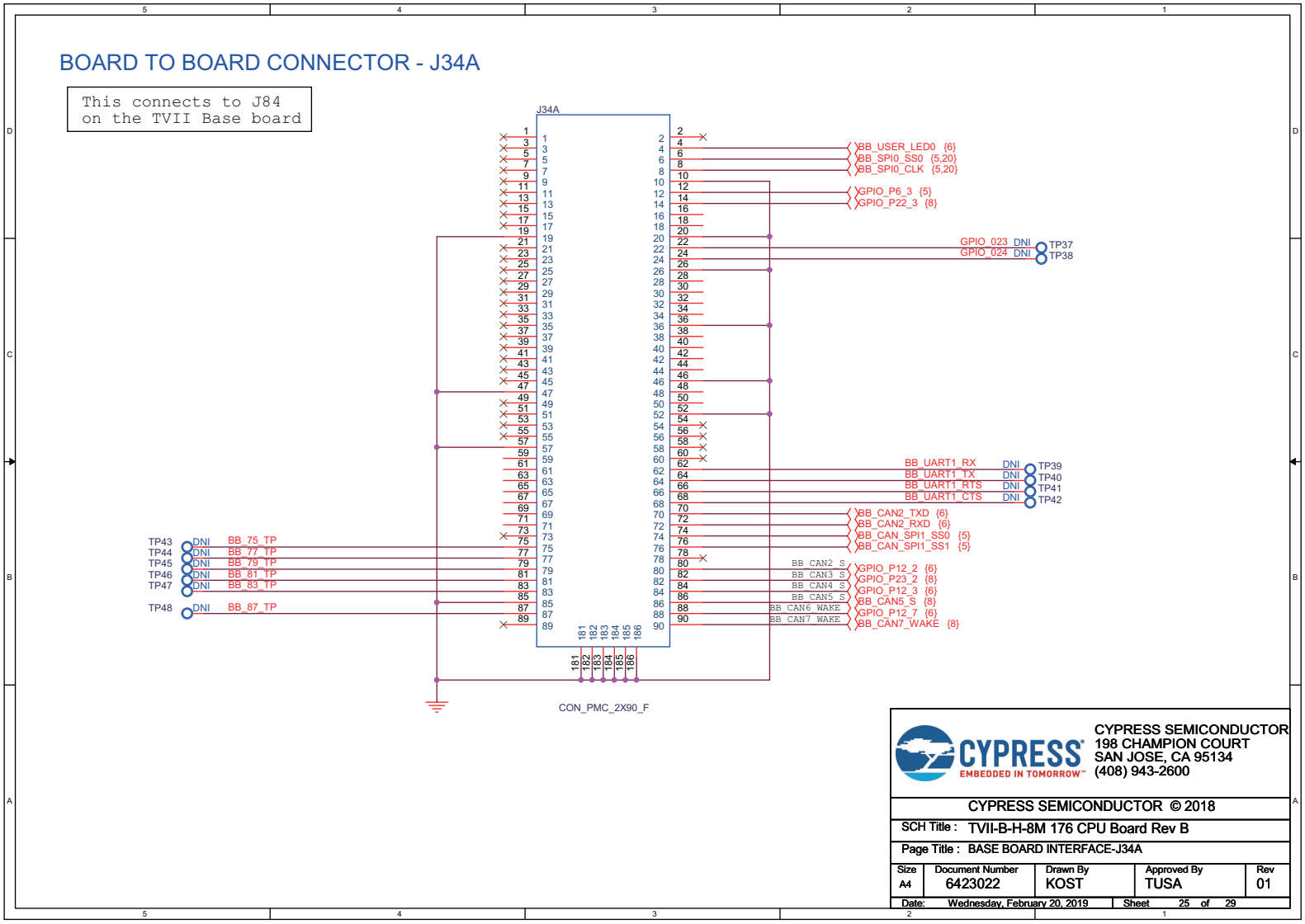


Figure A-25. Schematic (25/27)

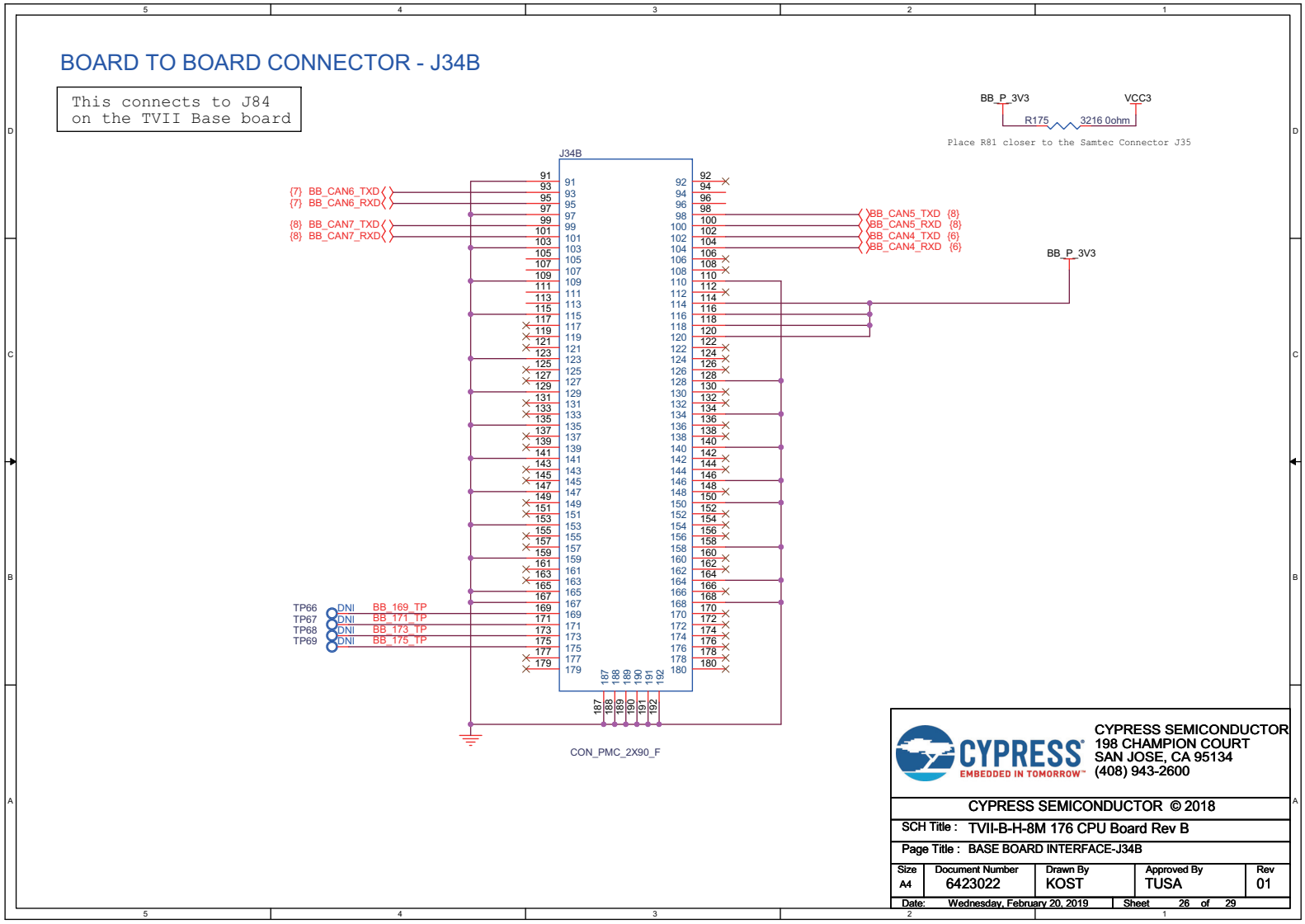


Figure A-26. Schematic (26/27)

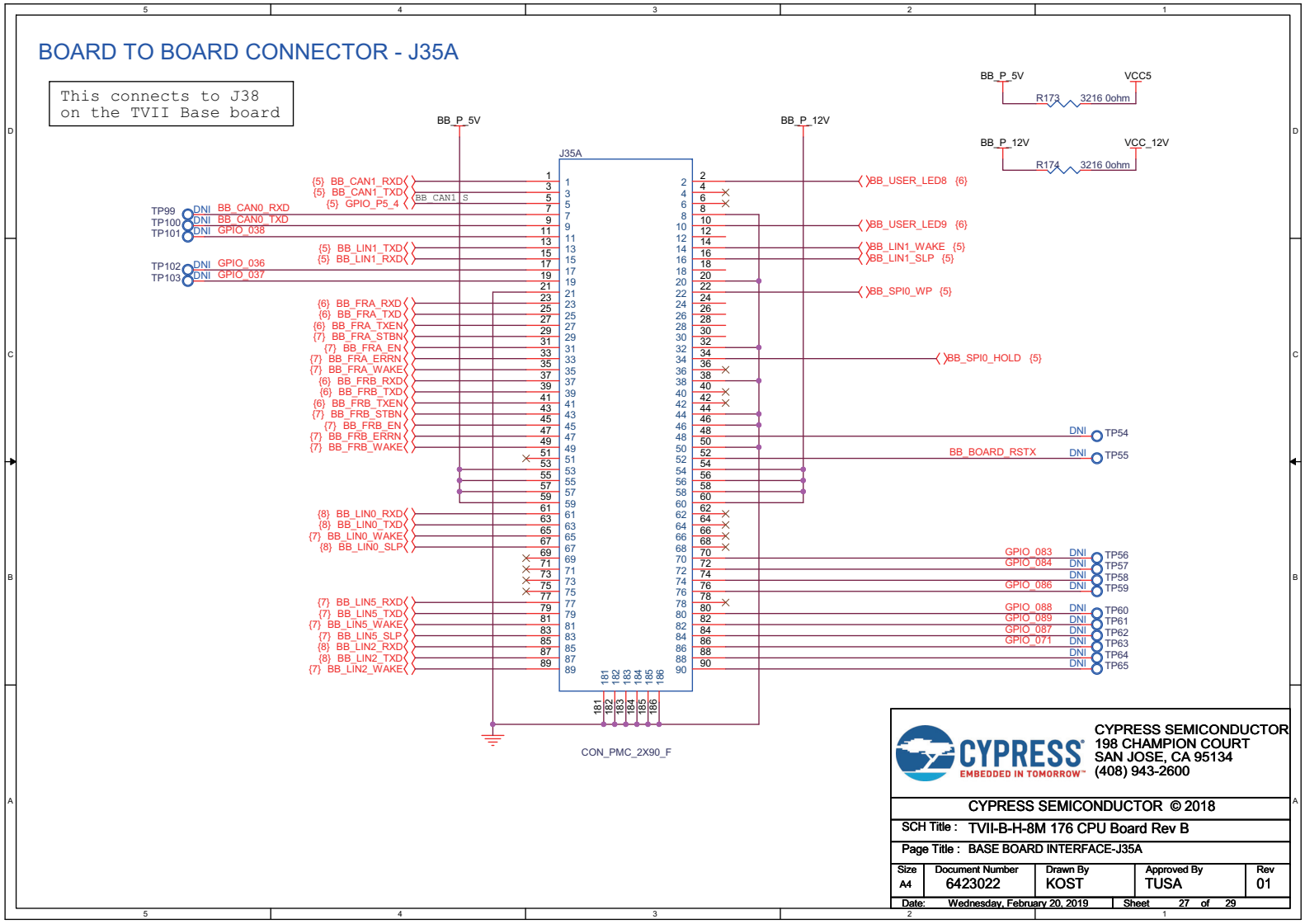
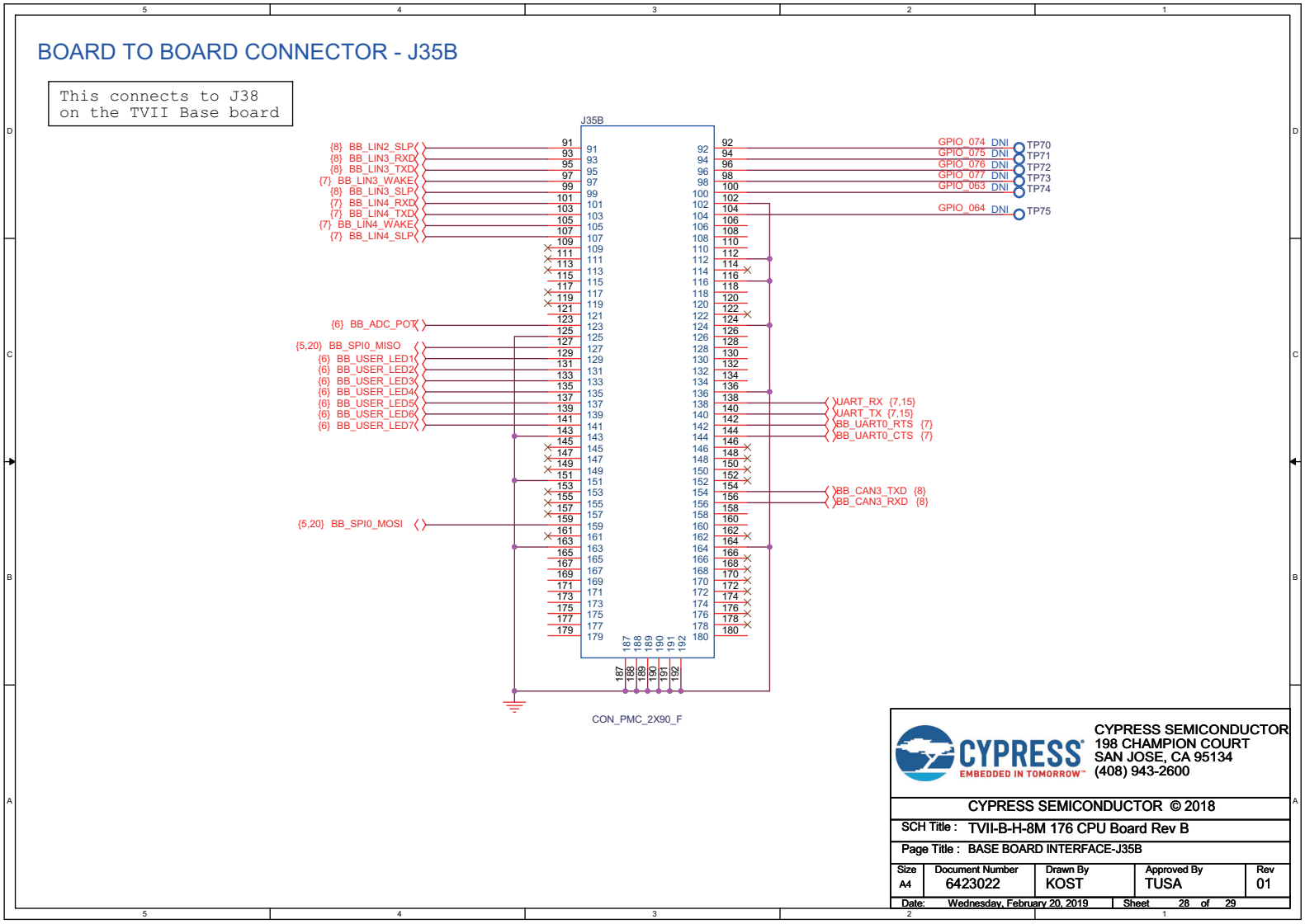


Figure A-27. Schematic (27/27)



B. Component Assembly on CPU Board

Figure B-1. Component Assembly (Top)

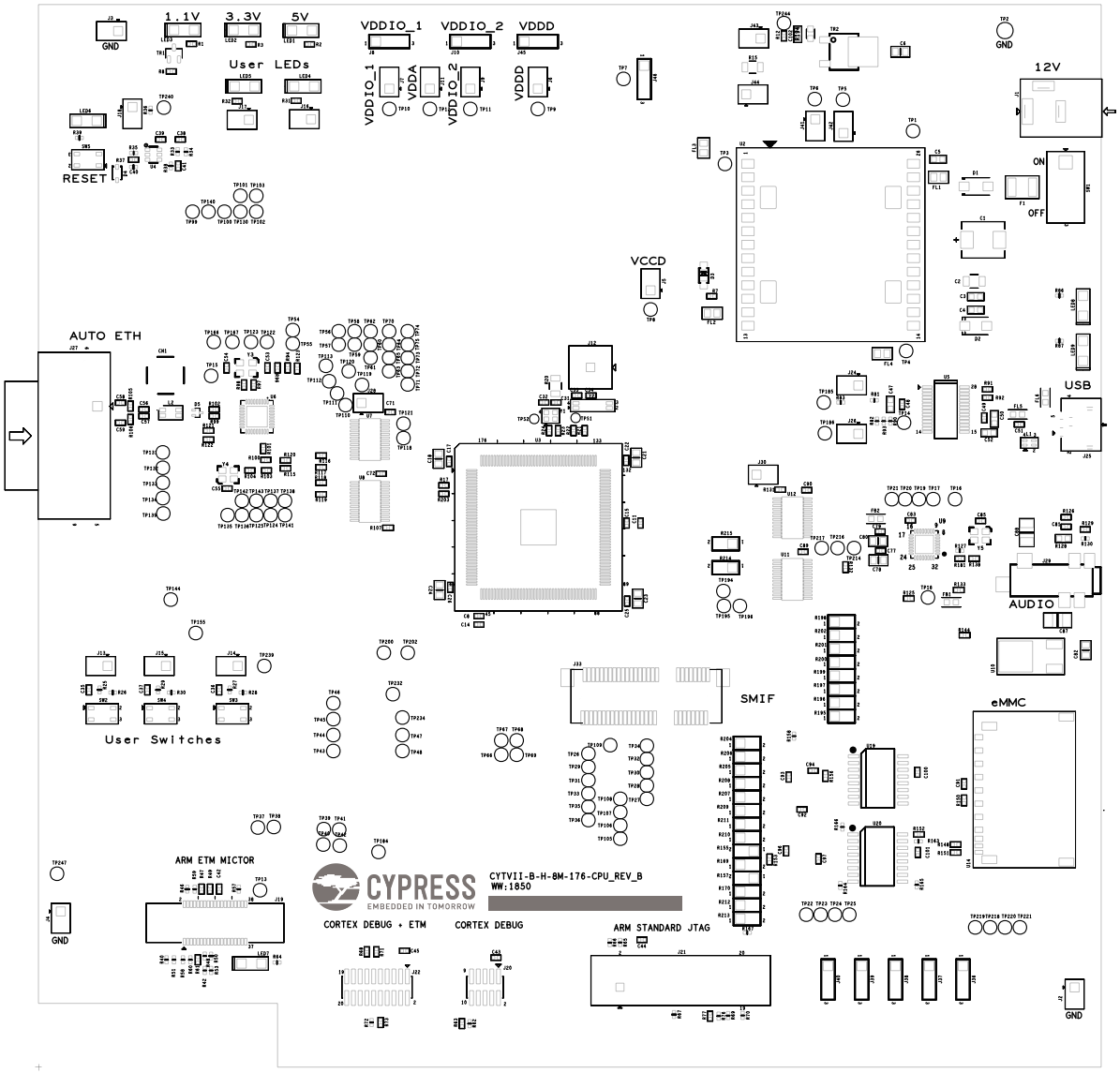
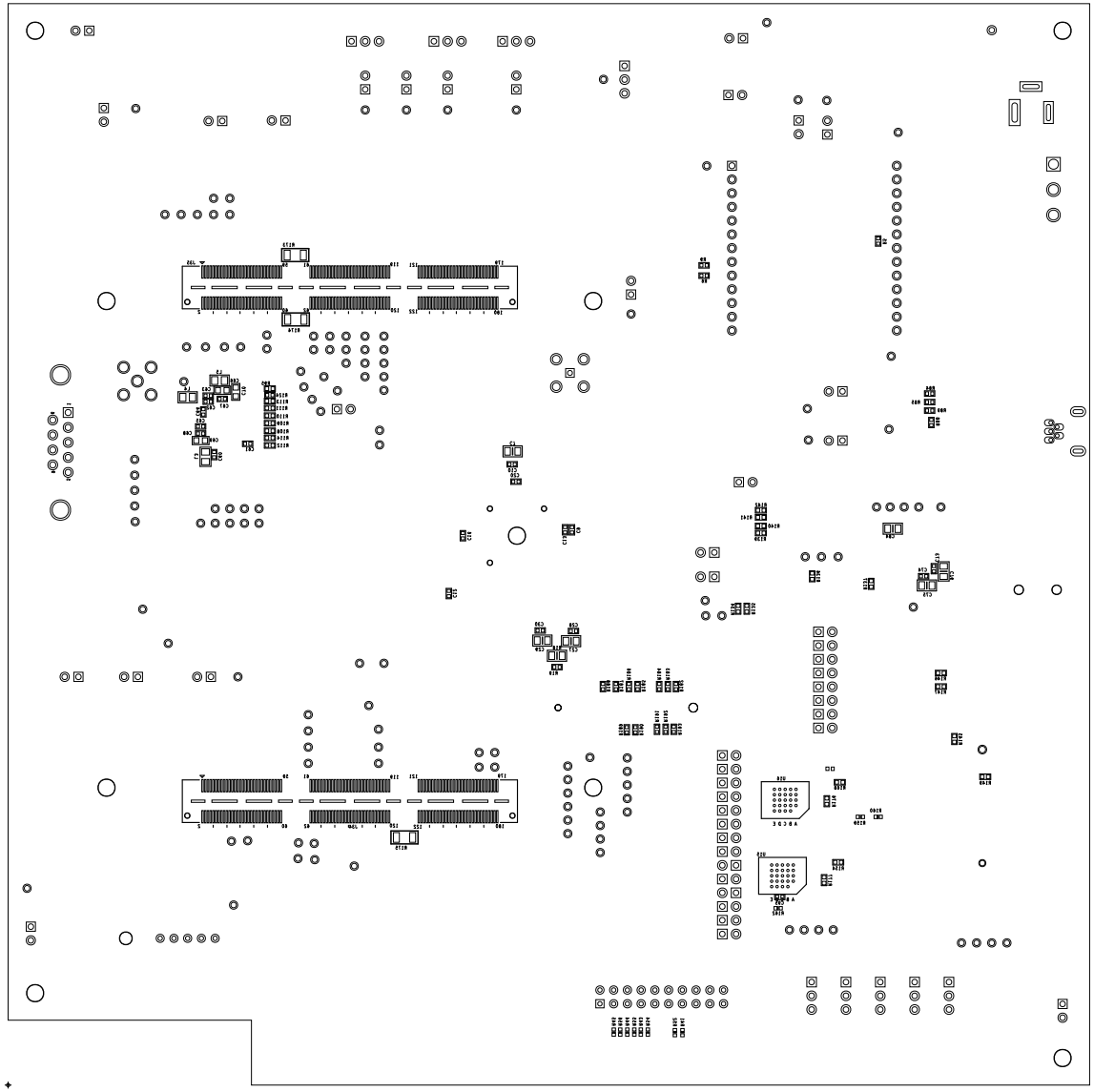


Figure B-2. Component Assembly (Bottom)



C. Schematics of Base Board

Figure C-1. Schematic (1/16)

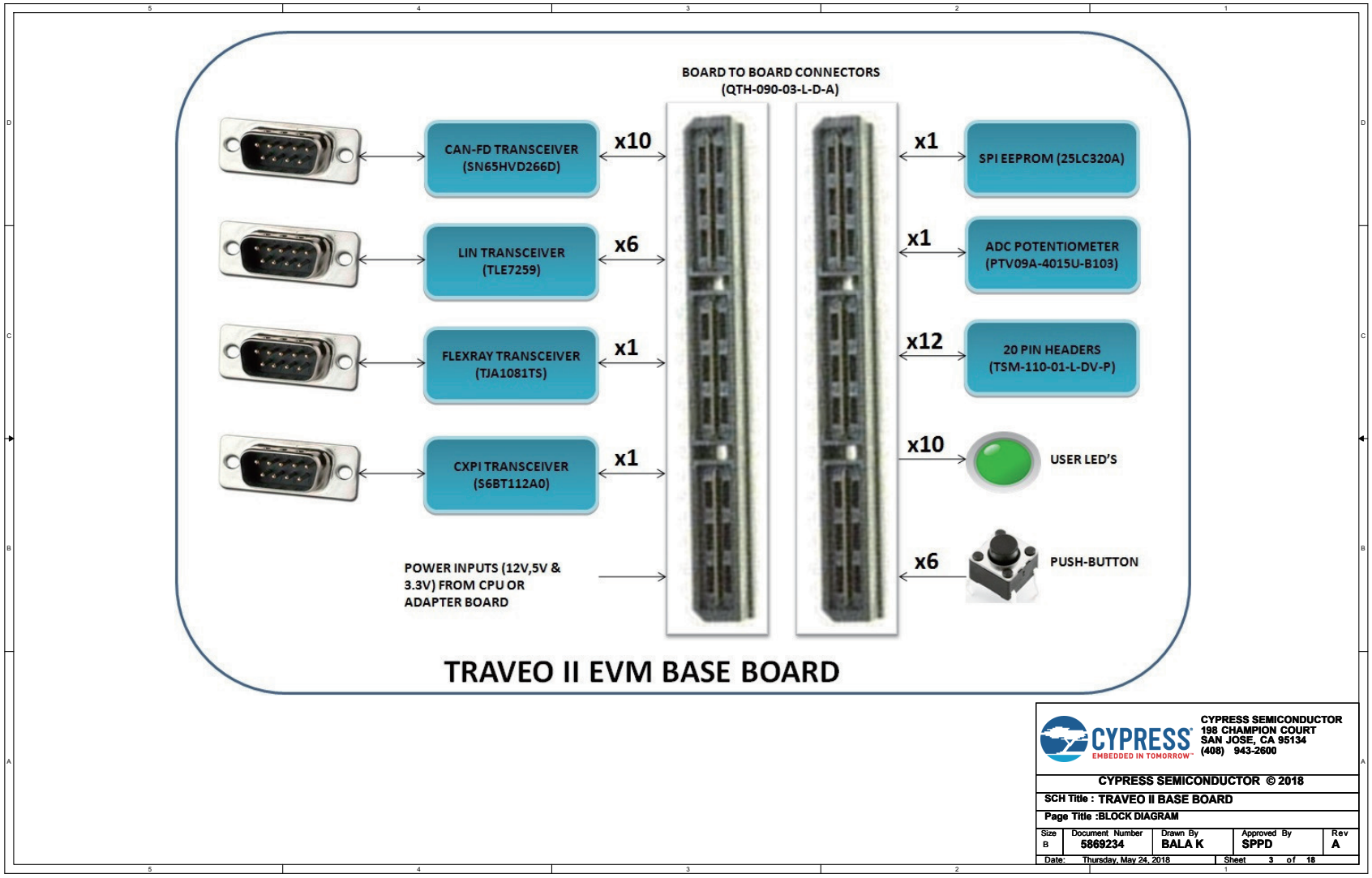


Figure C-2. Schematic (2/16)

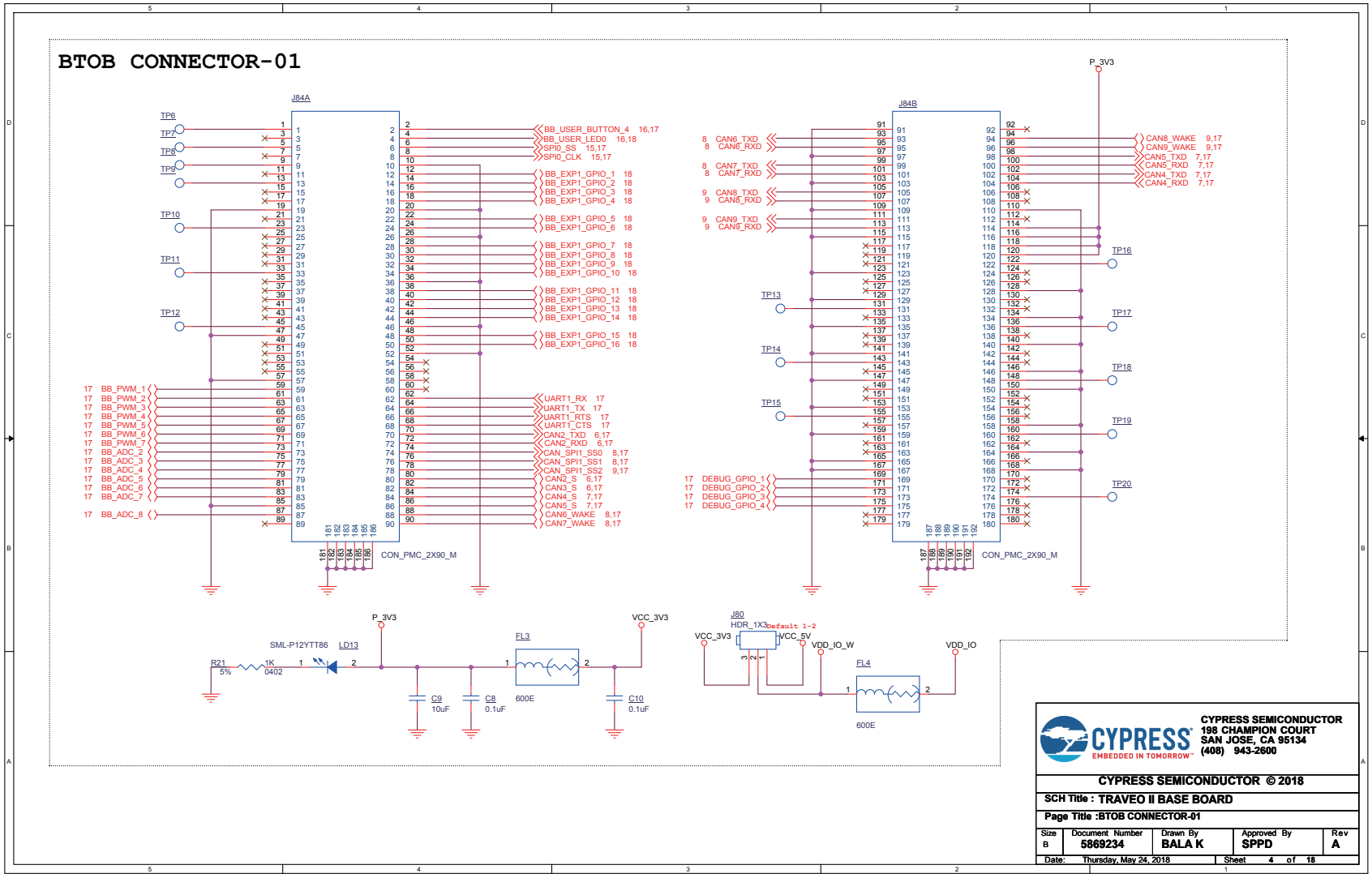


Figure C-3. Schematic (3/16)

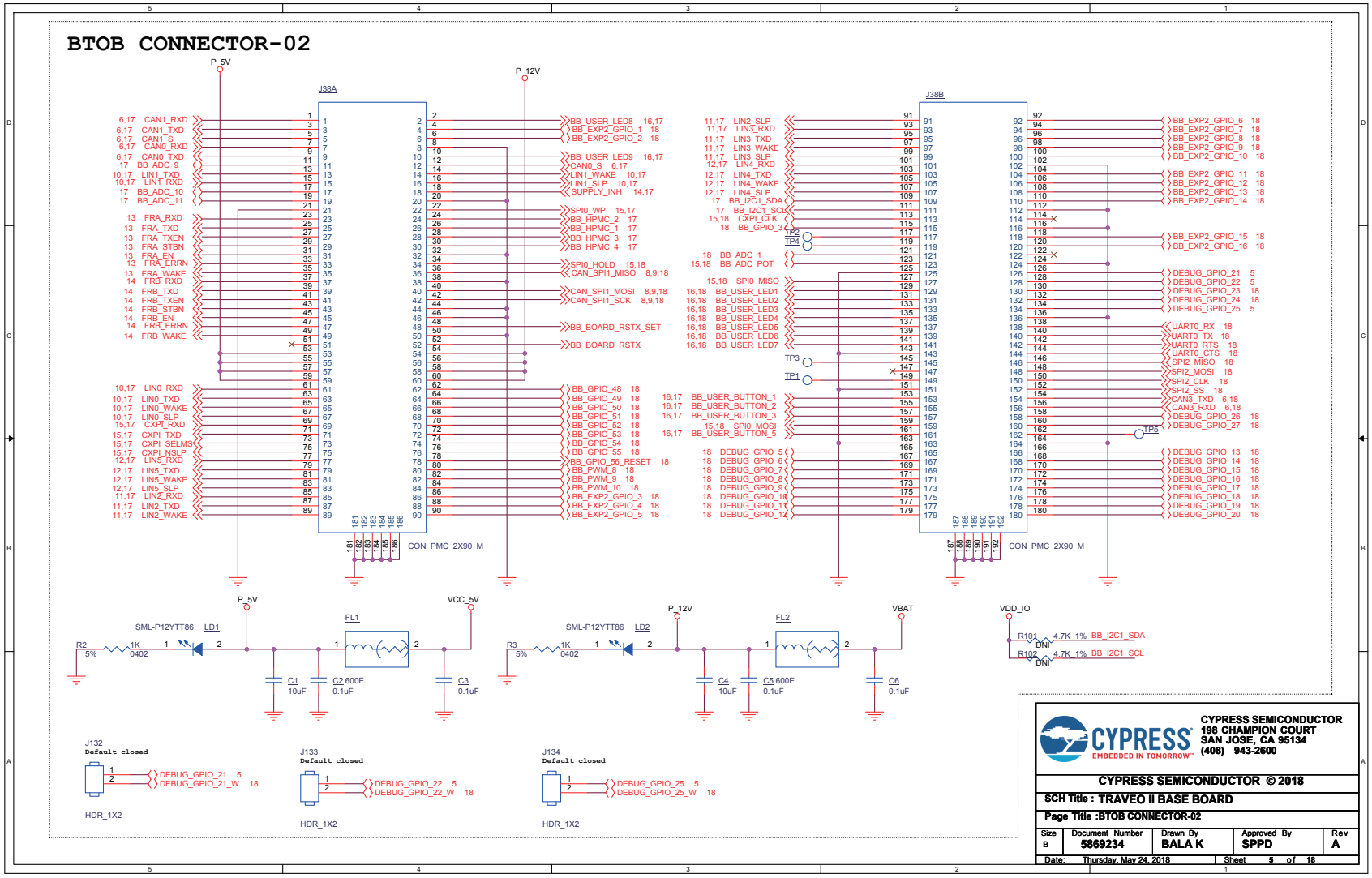


Figure C-4. Schematic (4/16)

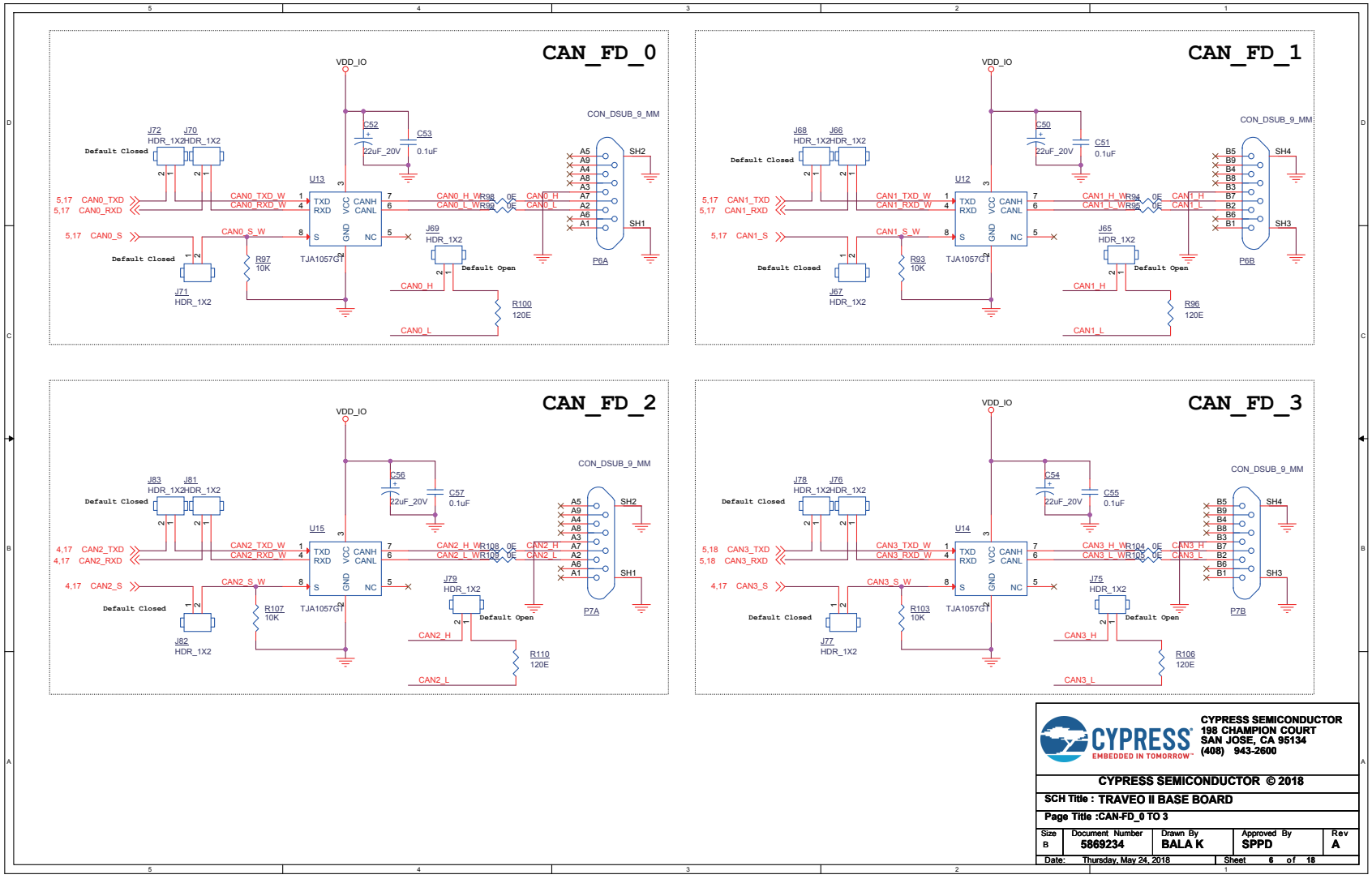


Figure C-5. Schematic (5/16)

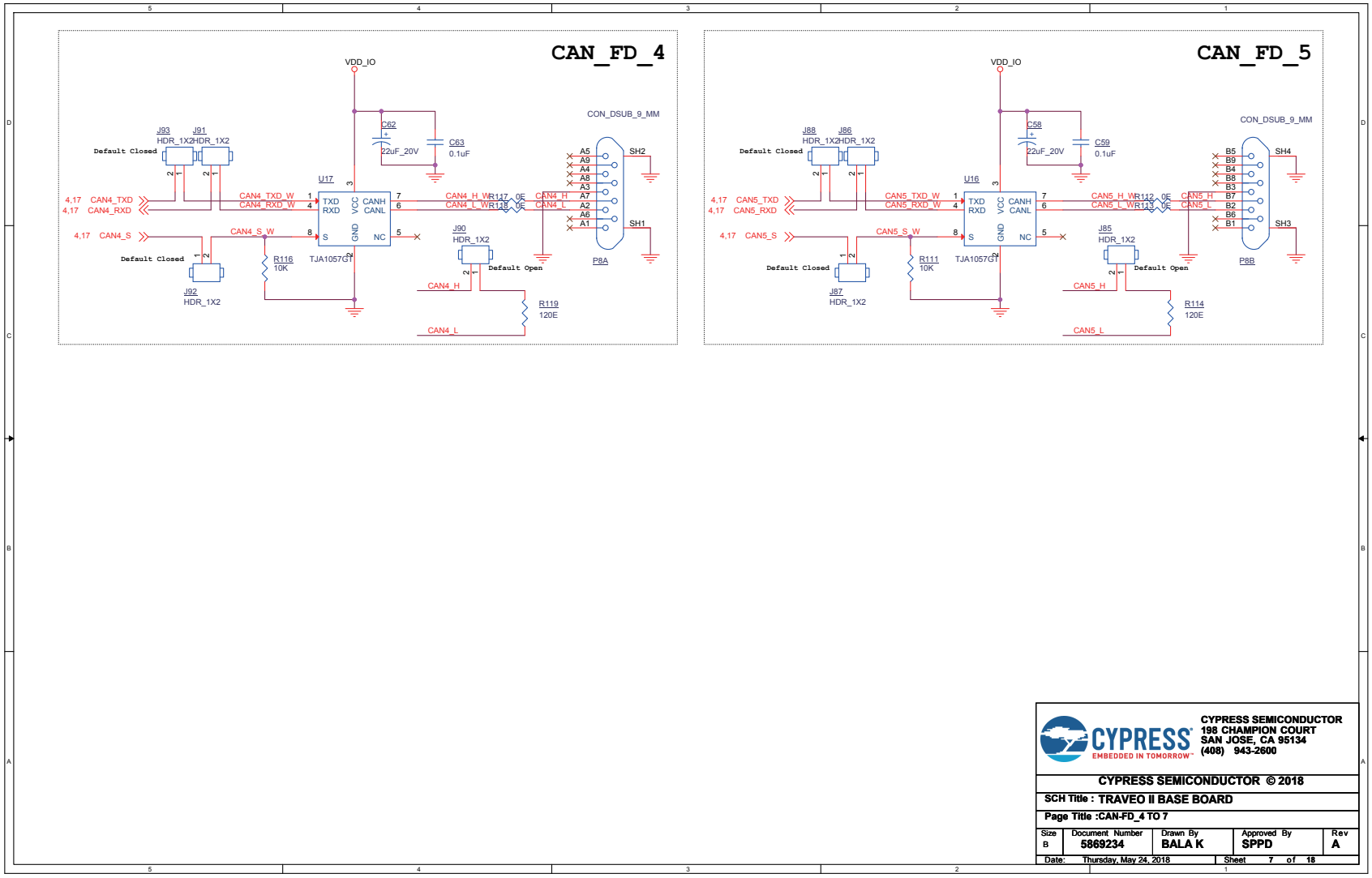


Figure C-6. Schematic (6/16)

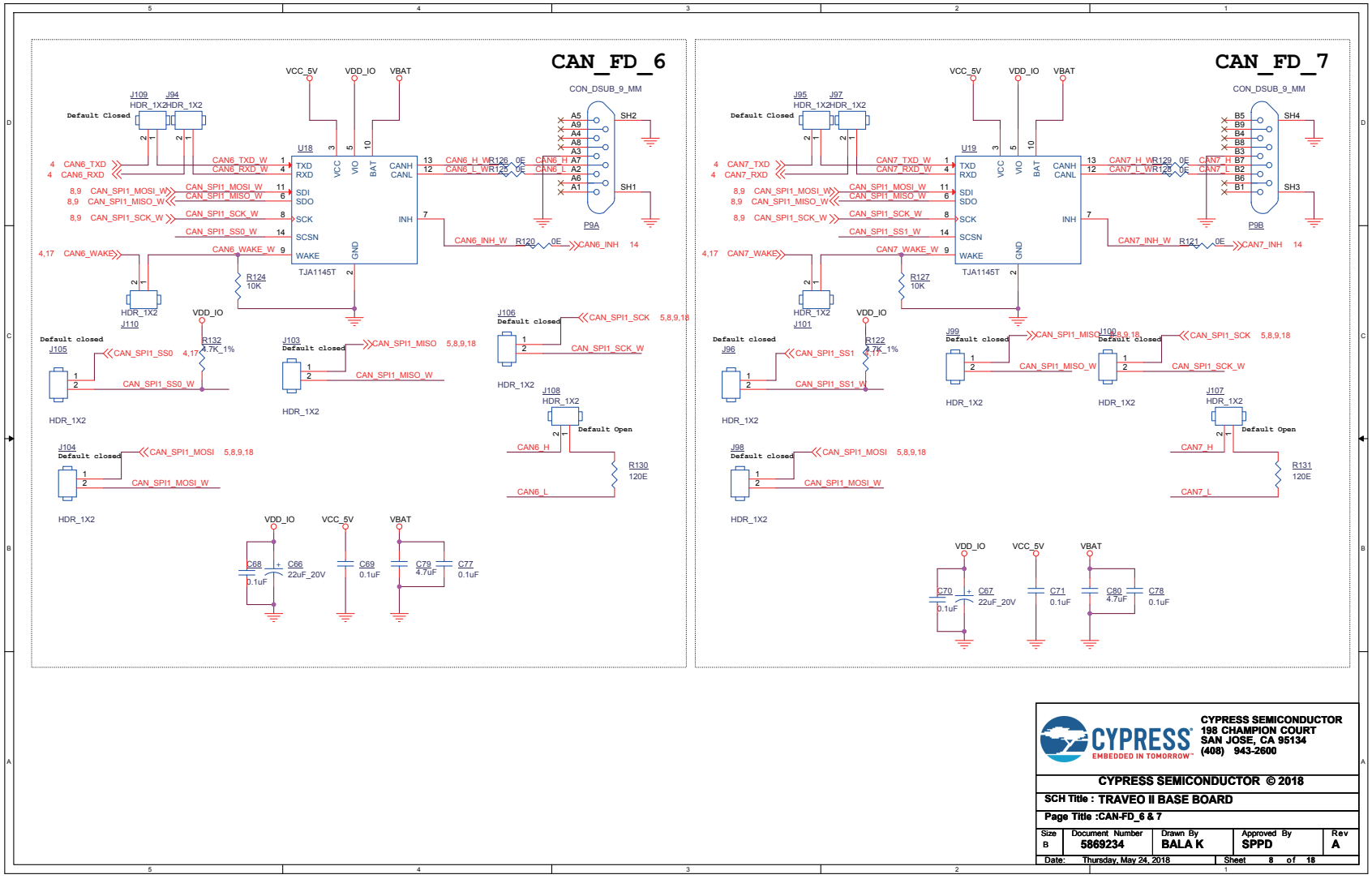


Figure C-7. Schematic (7/16)

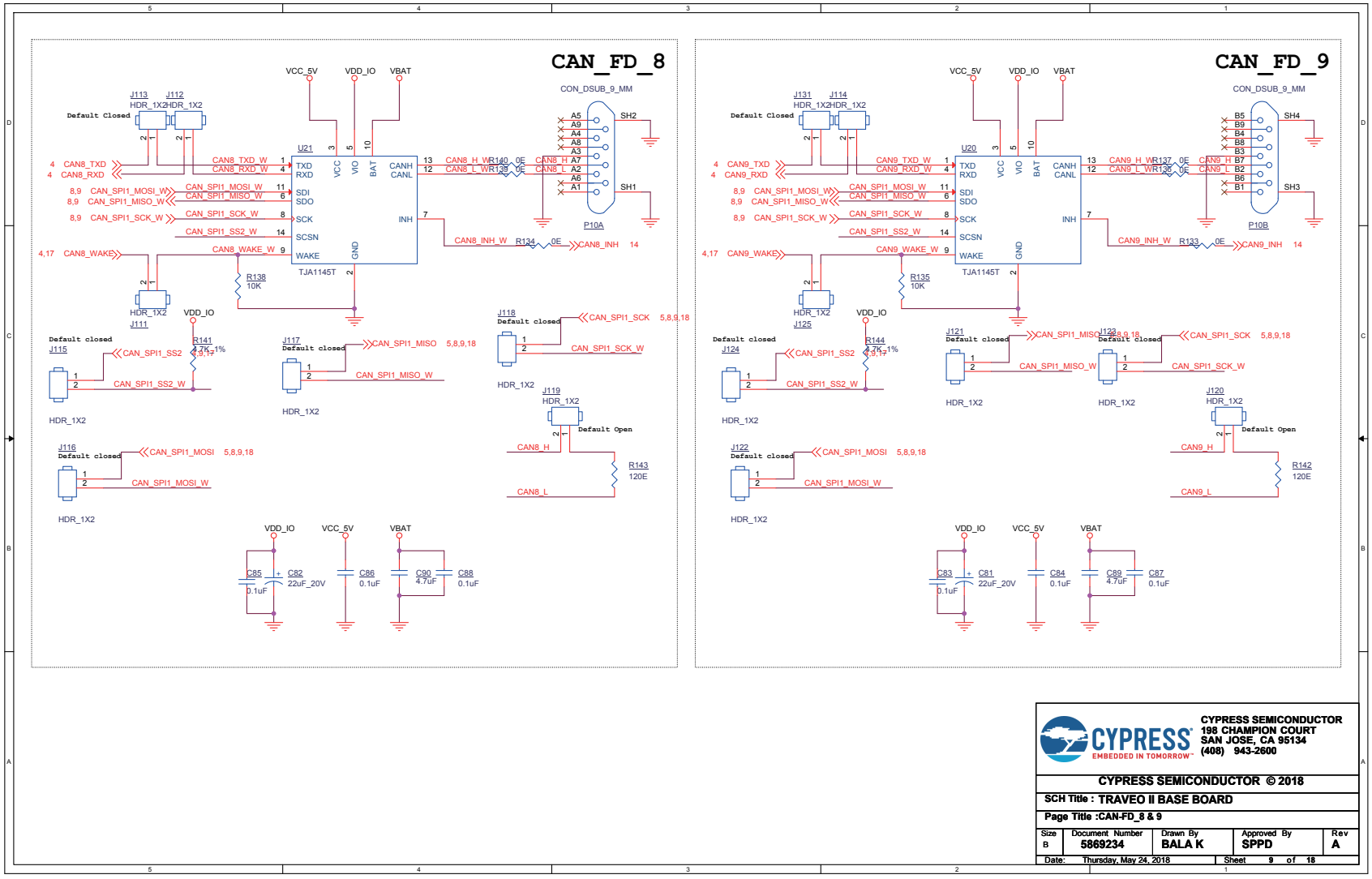


Figure C-8. Schematic (8/16)

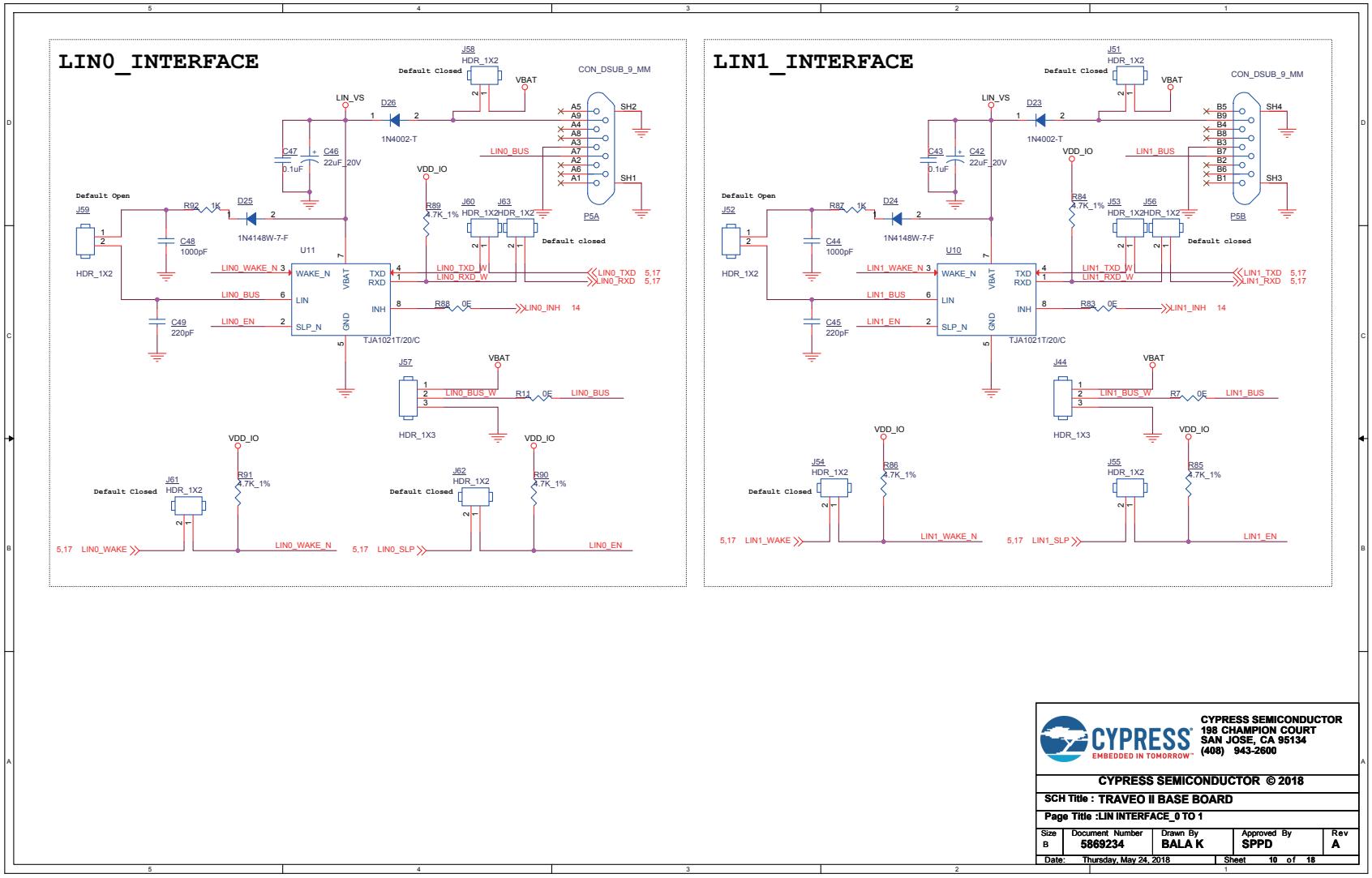


Figure C-9. Schematic (9/16)

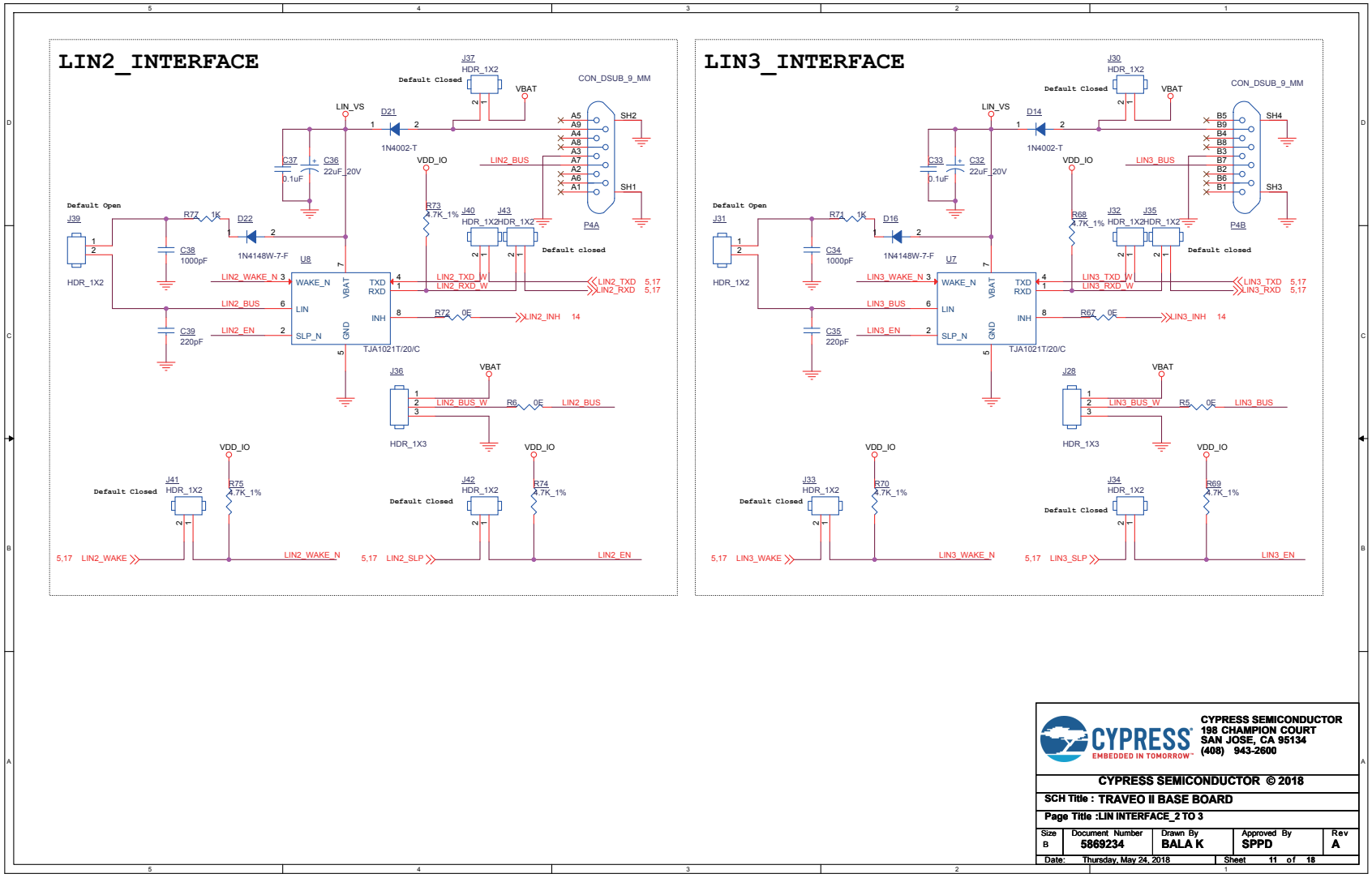


Figure C-10. Schematic (10/16)

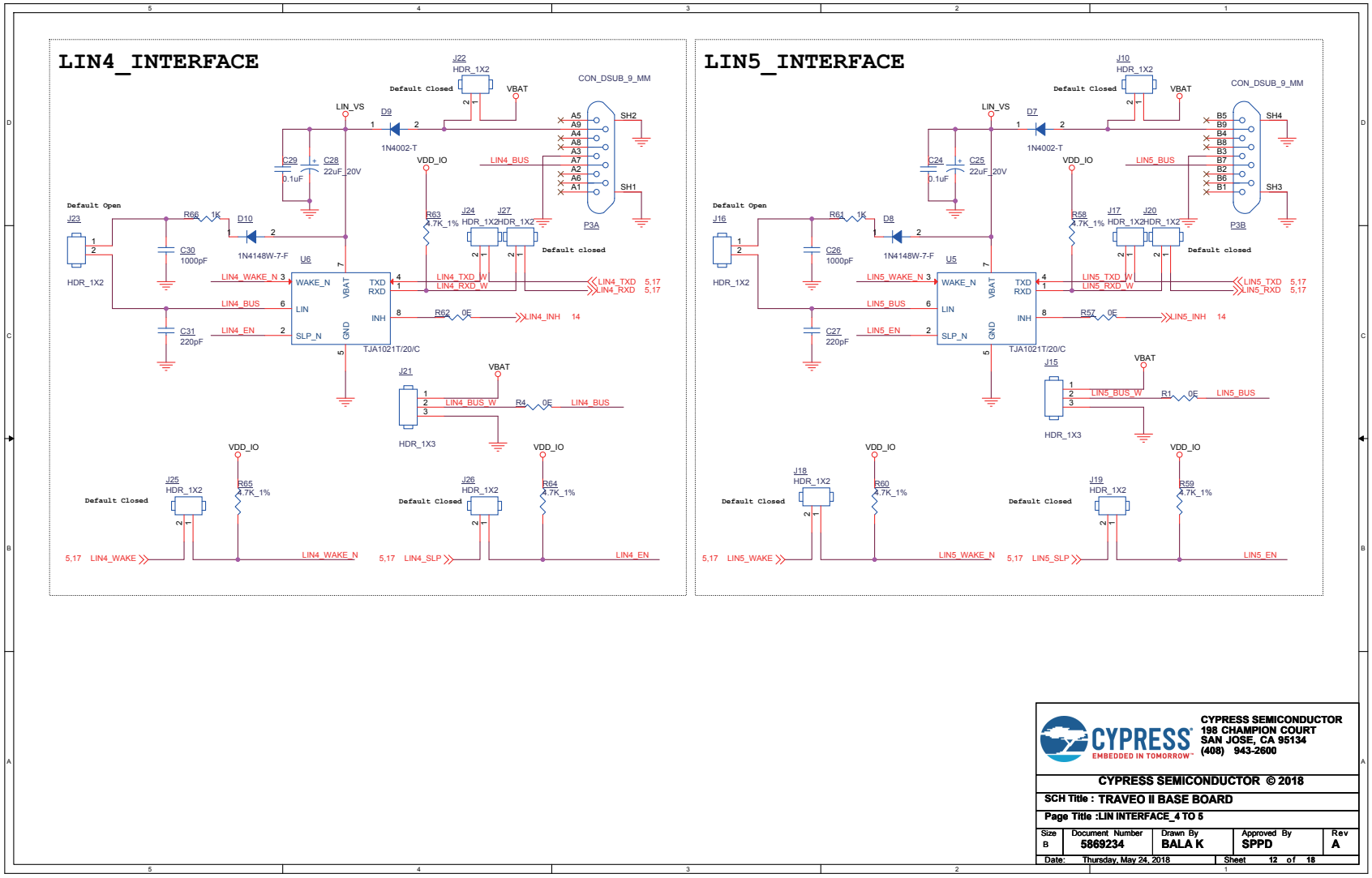


Figure C-11. Schematic (11/16)

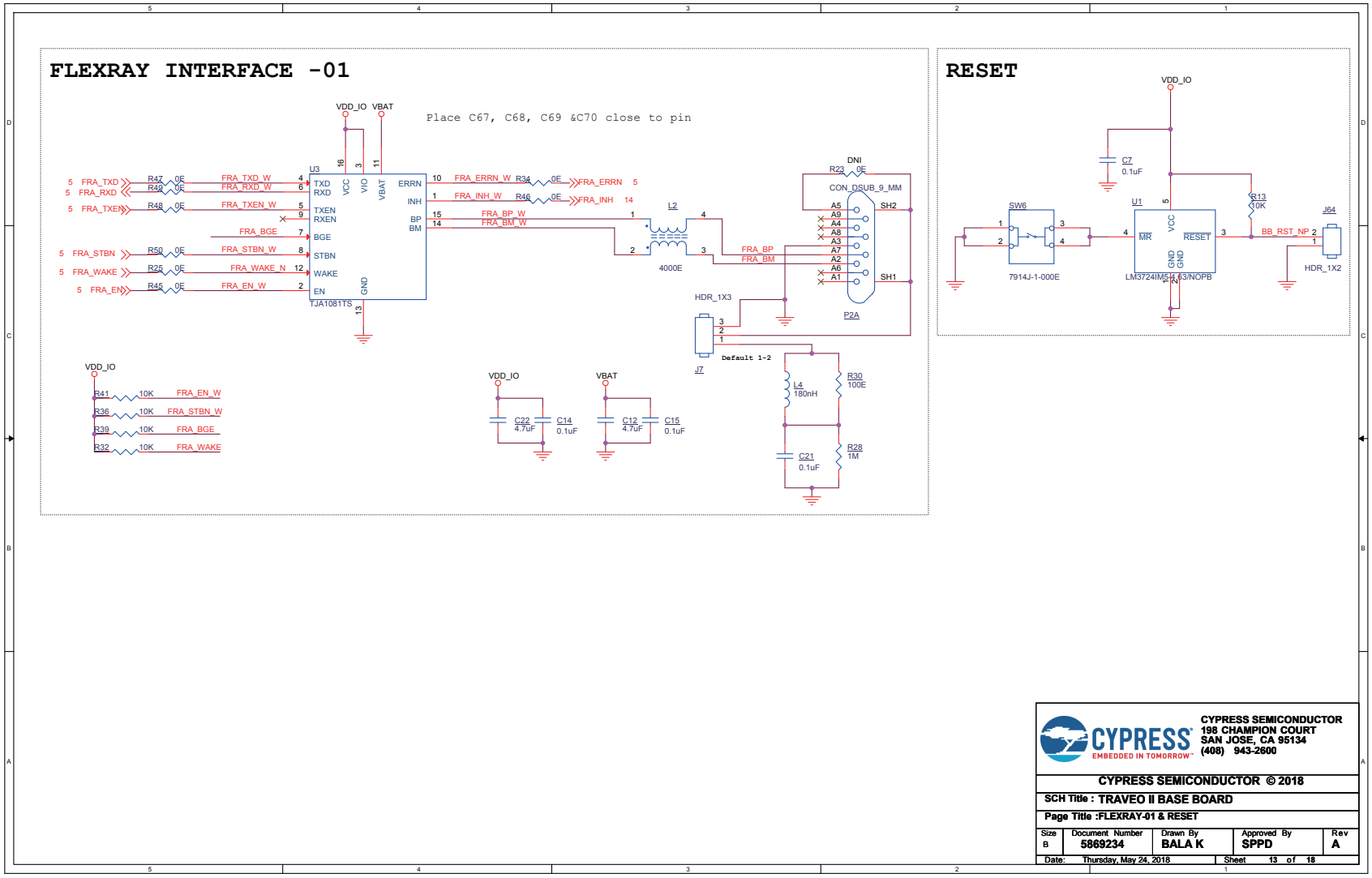


Figure C-12. Schematic (12/16)

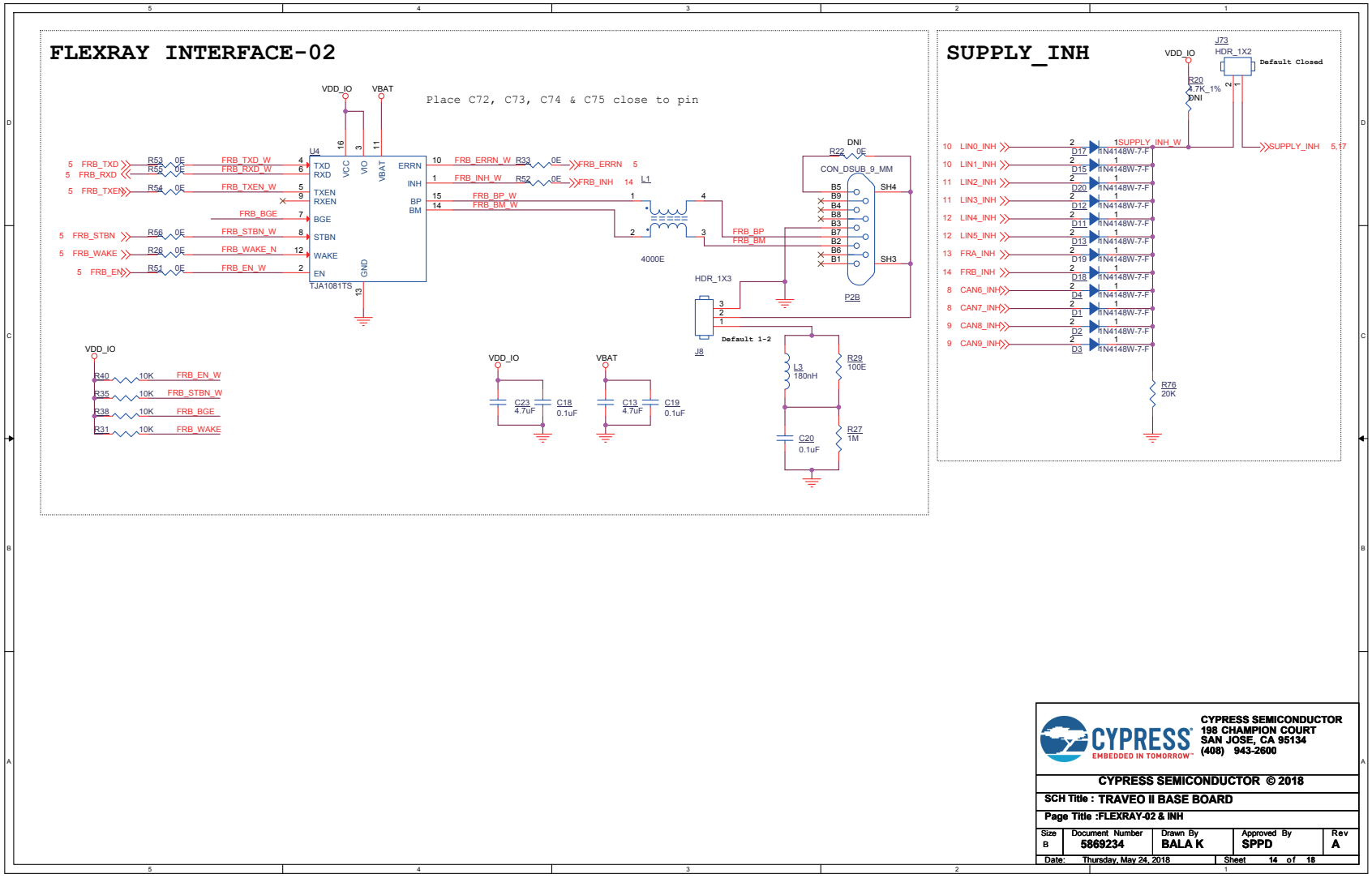


Figure C-13. Schematic (13/16)

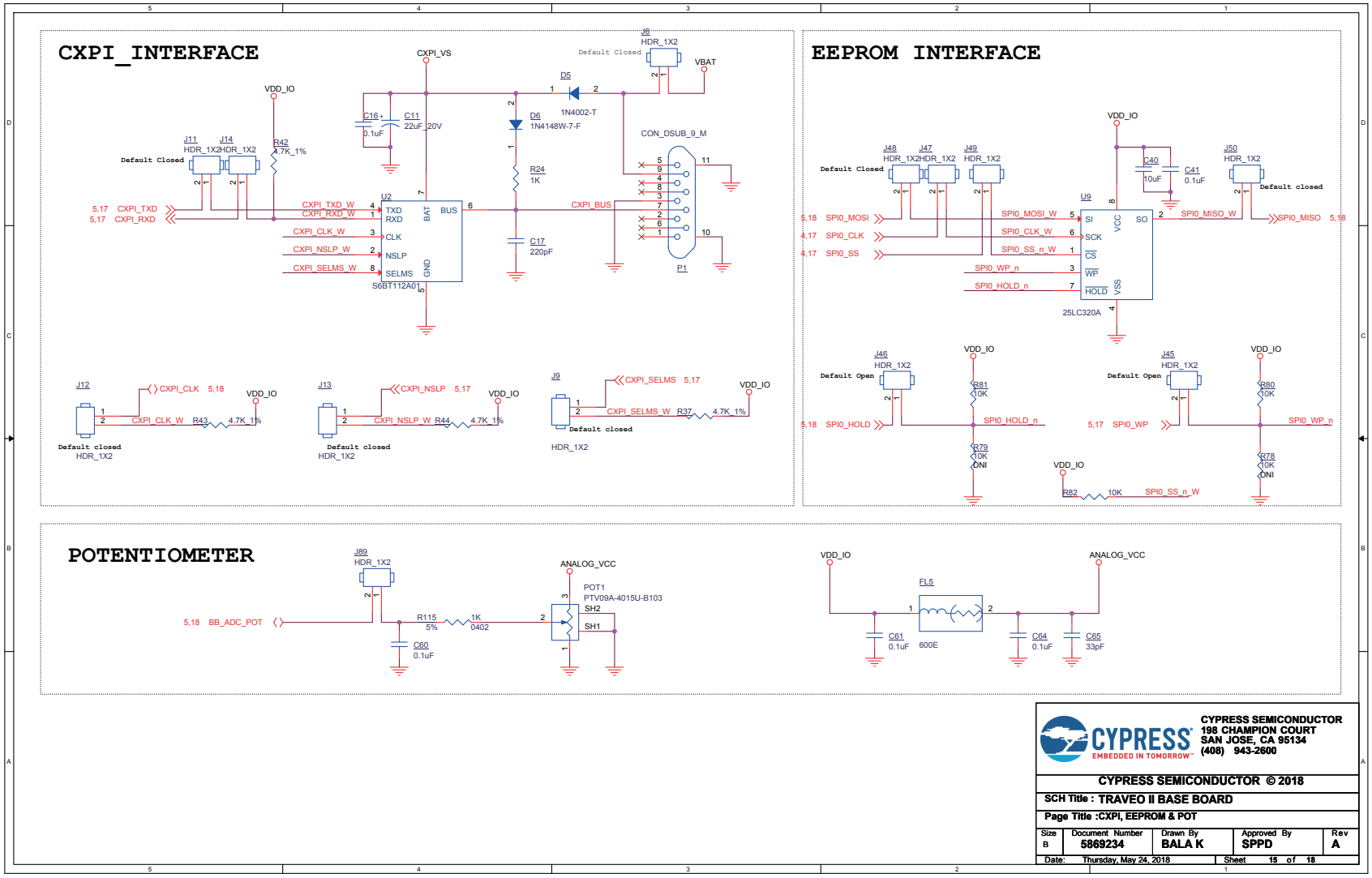


Figure C-14. Schematic (14/16)

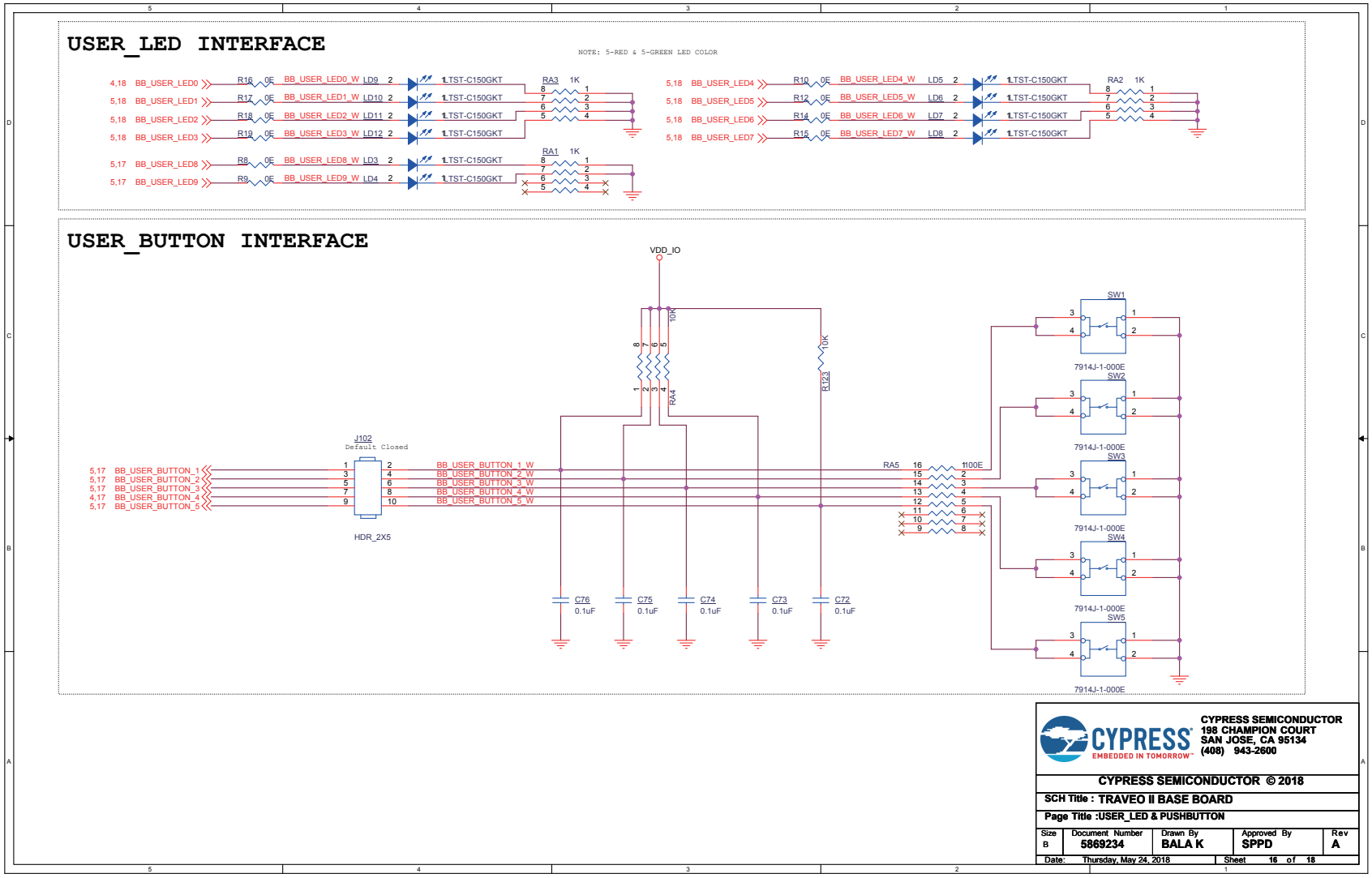


Figure C-15. Schematic (15/16)

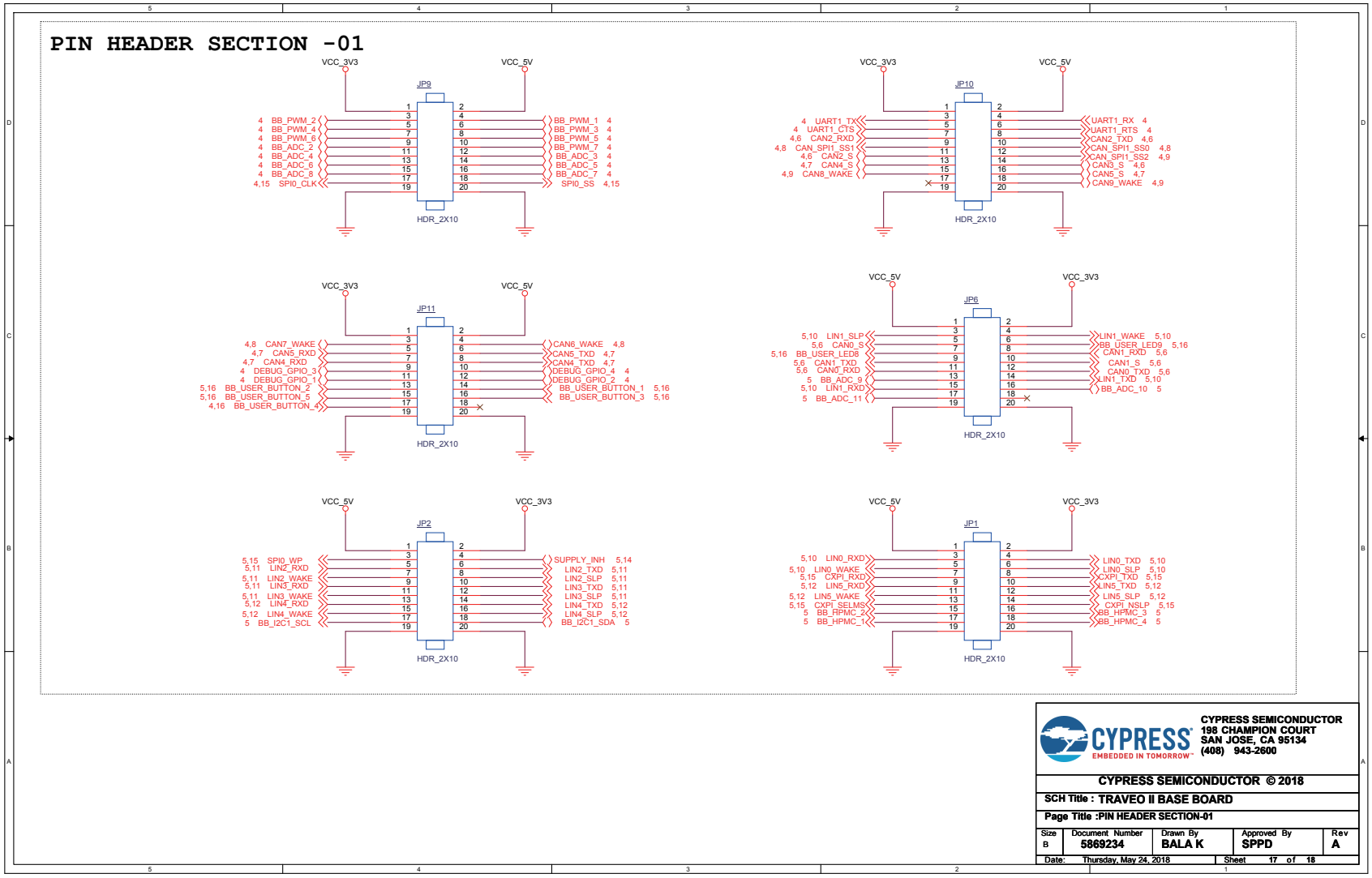
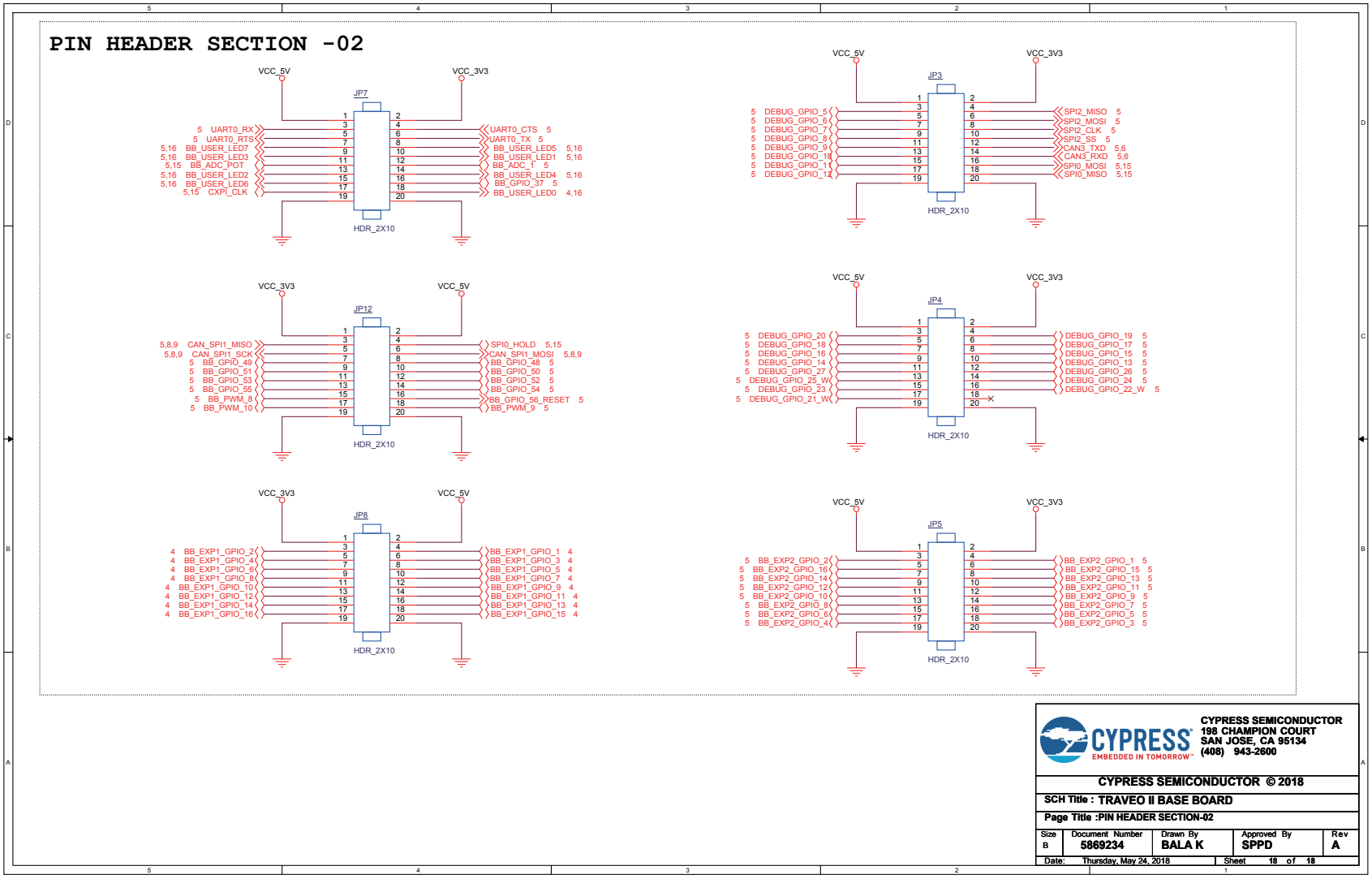


Figure C-16. Schematic (16/16)



D. Component Assembly on Base Board

Figure D-1. Component Assembly (Top)

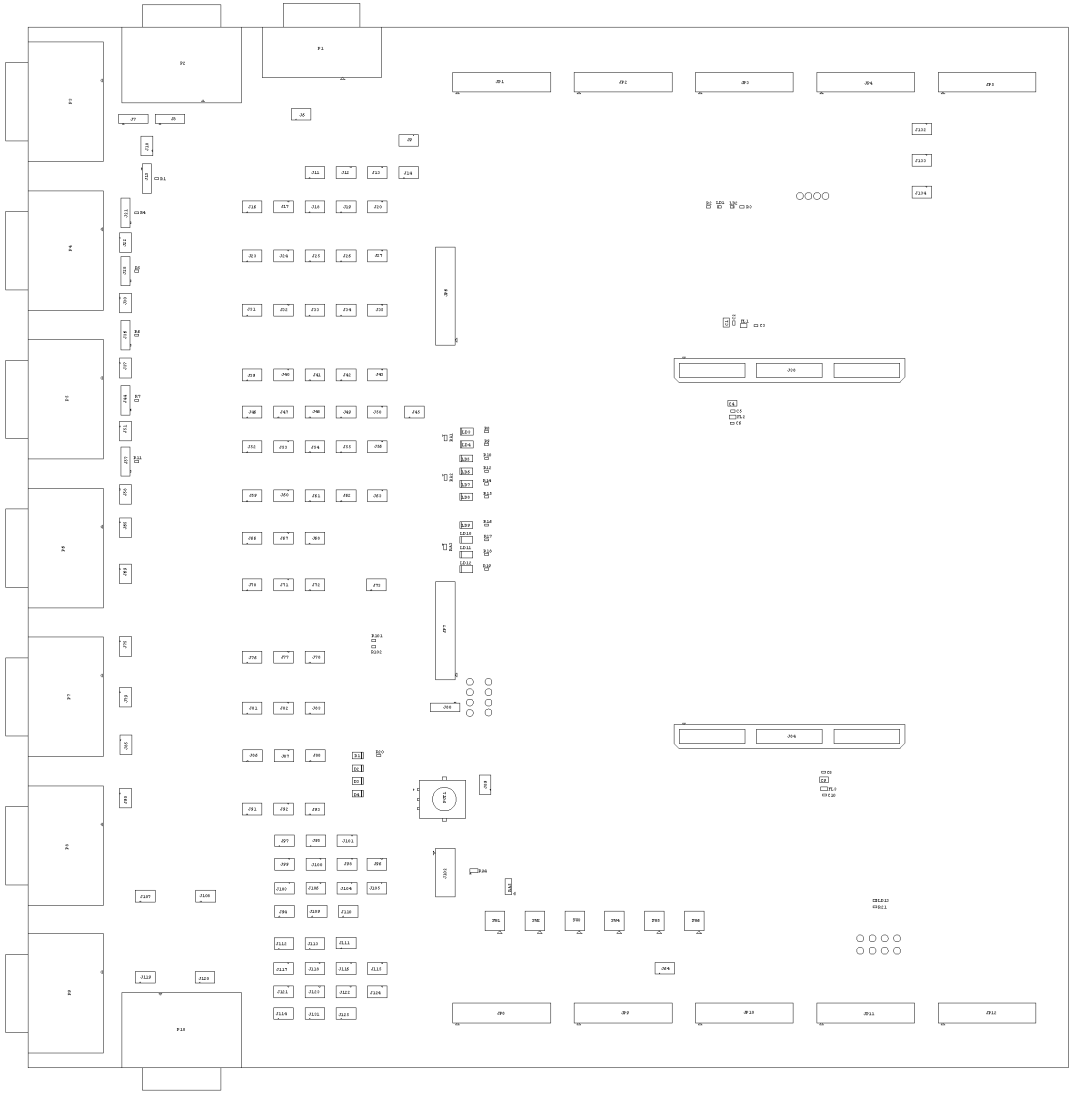
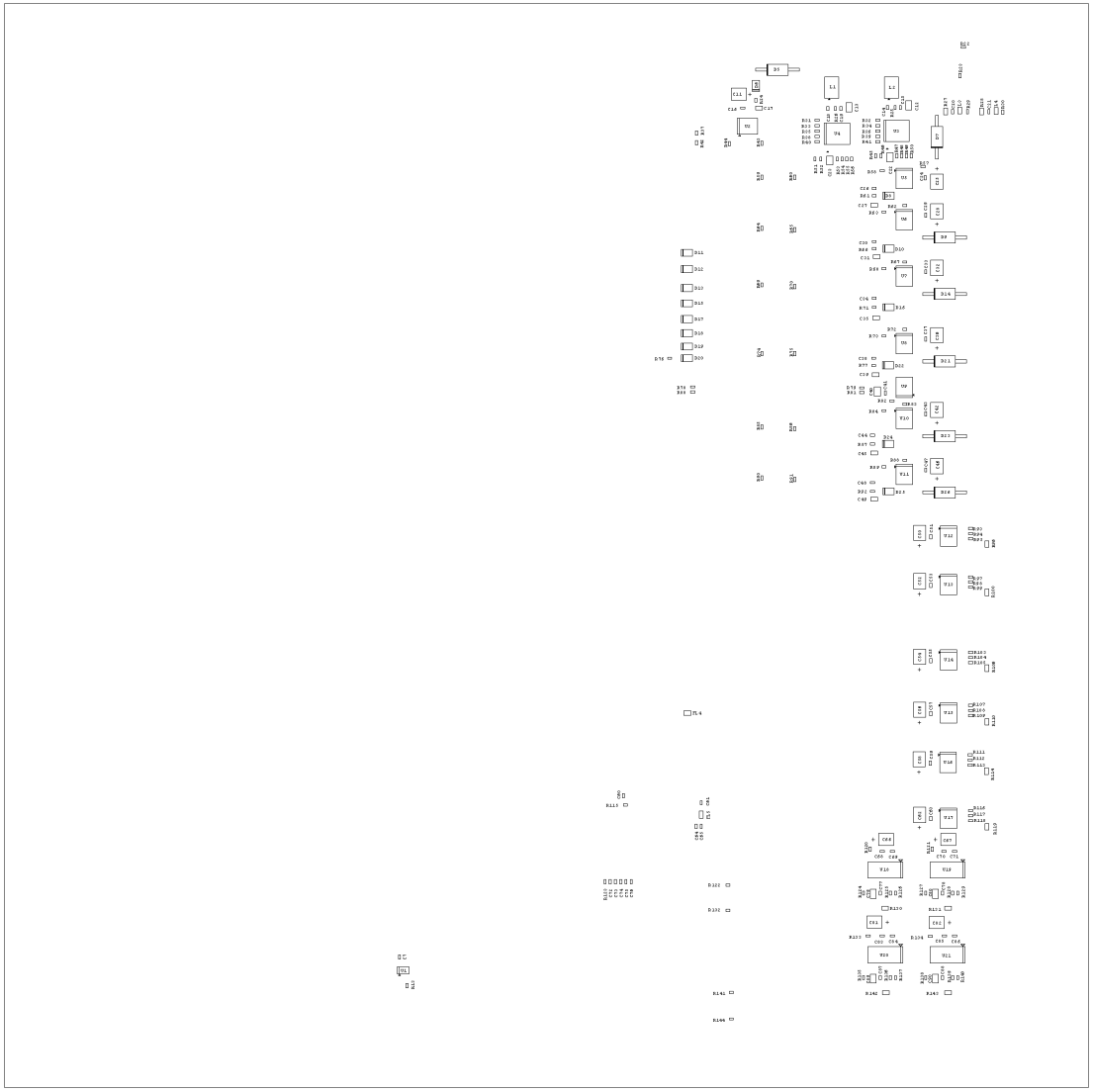


Figure D-2. Component Assembly (Bottom)



Revision History

Document Revision History

Document Title: CYTVII-B-H-8M-176-CPU Evaluation Board User Guide Document Number: 002-25907			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6493098	02/25/2019	New User Guide
*A	6923377	07/15/2020	Added content under Figure 2-1