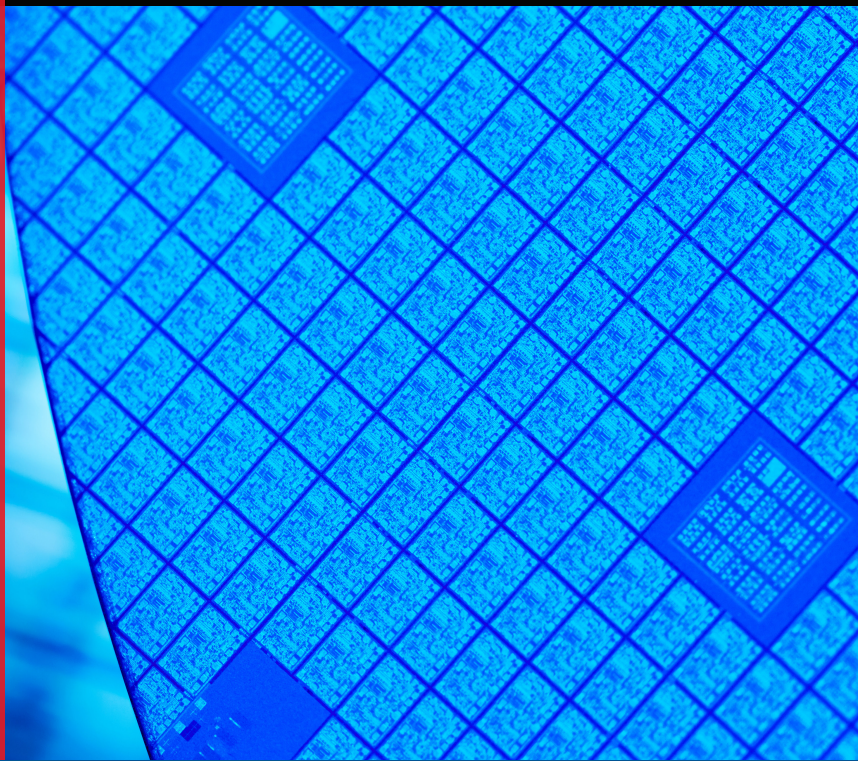CYPRESS

SONOS eFLASH

the Most Cost-Effective, Reliable Embedded Flash Solution for Next-Generation MCUs and IoT Devices

Cypress's SONOS (Silicon Oxide Nitride Oxide Silicon) is a patented and proprietary NOR Flash technology that Cypress developed for cost-effective MCUs. SONOS is a transistor with a polysilicon gate (S), an Oxide Nitride Oxide (ONO) gate dielectric and a Silicon substrate (S) whose threshold voltage (Vt) can be changed by adding or removing electric charge from the nitride (ONO) layer. Cypress's SONOS eFlash has been in production since 2001 and is now available on advanced nodes.

FEATURES

Cypress's SONOS eFlash:

• Requires only five extra masks beyond the standard CMOS process

• Requires no ECC, resulting in a smaller, less complex design

• Provides 25-ns access time with 100,000 Write Endurance cycles and 10 years of Data Retention

• Supports read operation at uLP minimum VDD of 0.81 V

• Is already proven down to the 28-nm node

• Leaves CMOS device characteristics unchanged, preserving existing transistor models and design IP
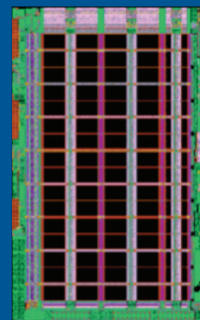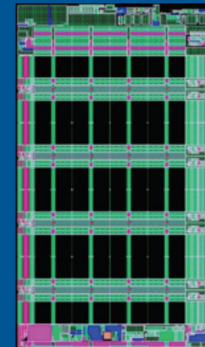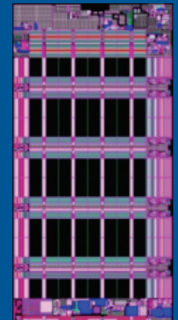
65-nm 4Mb   55-nm 8Mb   40-nm 8Mb

CELL OPERATION

Cypress's SONOS eFlash bit cell contains two transistors: a SONOS (Control Gate) and a MOS (Select Gate). One cell stores one bit of data for Flash or EEPROM. SONOS transistor is programmed by FN tunneling; threshold voltage is increased by injecting negative charges into the nitride layer. It is erased by FN tunneling as well; threshold voltage is decreased by ejecting negative charges from the nitride layer.
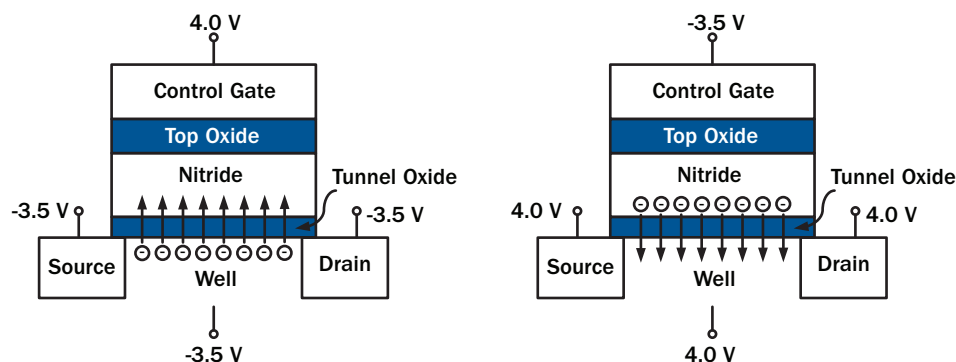
Program (left) and Erase (right) by FN Tunneling

CYPRESS
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SONOS EFLASH MACRO IP LIST

Node	Density	Output Width	Access Time
40-nm LP/uLP	1Mb to 16Mb	32, 64, 128, 256	25 to 50 ns
55-nm LP/uLP	1Mb to 16Mb	32, 64, 128	25 to 50 ns
65-nm	2Mb to 16Mb	128	25 ns

APPLICATIONS

Cypress's SONOS technology finds numerous uses in MCU, bank card, SIM card, ID card, EEPROM, FPGA, and nvSRAM products.

SONOS eFlash is scalable and proven in volume production. Cypress has:

- Shipped >2 billion PSoC units with SONOS eFlash over 15 years
- Introduced SONOS eFlash into volume production at the 350-nm node in 2001 and the 130-nm node in 2007
- Qualified SONOS eFlash at the 65-nm node in 2012
- Scaled SONOS eFlash to 55-nm, 40-nm and 28-nm nodes

The latest additions to the SONOS eFlash family provide ultralow-power and high-performance processing at attractive cost which makes them highly suitable for consumer and industrial applications such as wearable, factory automation, Industry 4.0, and IoT devices.
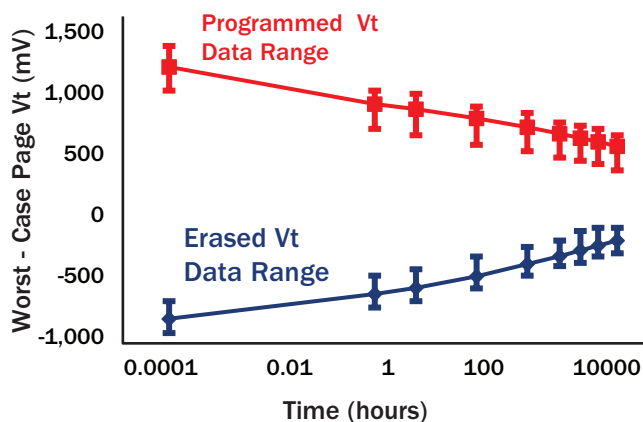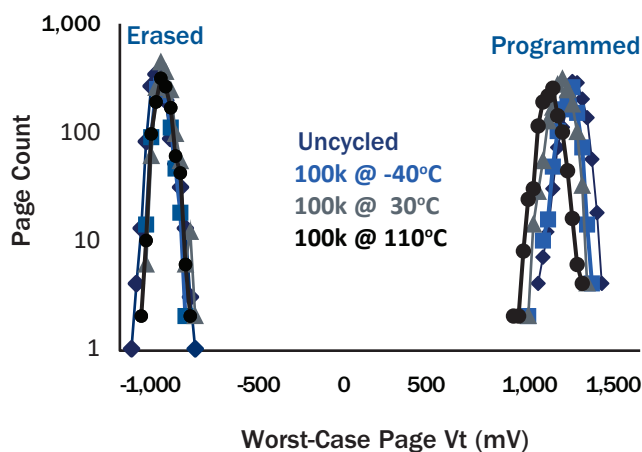
RELIABILITY

- Single-pulse Program/Erase operations of constant amplitude and duration
- Minimum 100,000 Program/Erase Endurance cycles across -40°C to 110°C temperature range
- Minimum 10 years of Data Retention
- SONOS eFlash passed 3,000 hours at 150°C without failure—three times longer than the 1,000-hour Automotive Grade 1 AEC Q100 requirement

HIGHLIGHTS

Cypress SONOS eFlash delivers:

- Low manufacturing cost
  - Low extra mask count (five)
  - No ECC requirement
  - Competitive bit cell and macro area
- High performance and robust reliability
  - 25-ns access time
  - Read operation at uLP minimum VDD of 0.81 V
  - 100,000 Write Endurance cycles
  - - 10 years of Data Retention
- Volume manufacturability and scalability

SONOS eFlash Write Endurance at -40°C, 30°C and 110°C

SONOS eFlash Data Retention at 150°C post 100k cycles