PRODUCT BRIEF

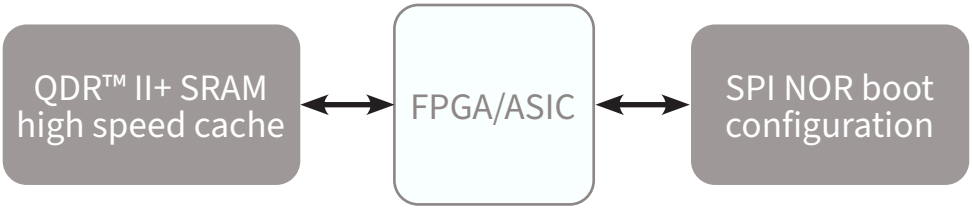
# 72-Mbit QDR® II+ Synchronous SRAM

## Infineon's HiRel memories perform in the most extreme environments

Infineon's 72-Mbit QDR™-II+, CYRS154X series, are Synchronous (Sync) SRAMs designed with Infineon's patented RadStop™ Technology that are optimized for space as well as other harsh environment applications. The 72-Mbit QDR-II+ SRAMs are available in x18/x36 and two-word/four-word data bus configurations and designed with a DDR address bus scheme. The QDR-II+ SRAM architecture provides a low latency and random memory access capability needed for high performance applications such as external cache memories. Infineon's QDR-II+ Sync SRAM family provides the Random Transaction Rate (RTR) necessary to break system bottlenecks.

Infineon's state-of-the art RadStop™ Technology is radiation hardened through propriety design and process hardening techniques. Our synchronous SRAM devices are of the highest reliability and performance and well suited for applications for payload processing and reconfigurable computing platforms for extreme environments. Well suited for radar implementations and image processing applications due to the low latency and random memory access capability.




### Key features

Certified reliability
- DLAM QML-V
- QCI, datapacks
- RHA, WLAT

Ultimate radiation performance
- >300 Krad TID
- >120 LET SEL immunity
- < $1.34e^{-7}$ Err/bit.day

Product features
- 250 MHz max frequency
- Concurrent R/W
- Throughput up to 36 Gbps
- Low latency (2 cycles)
- HSTL I/O
- SWaP optimized CCGA package with Six Sigma columns

Key applications
- Radar (SAR, LiDAR, SWOT)
- Satellite based networking
- Satellite imaging
- Command and data handling
- Telemetry and tracking
- Attitude and orbit control(AOC)

Differentiated memory portfolio
- Performance
- Density
- Reliability
- Longevity

Space

www.infineon.com/hirelmemory

## Key Features

- 250 MHz/36 Gbps maximum frequency of operation/ throughput
- 4-Mbit x18, 2-Mbit x36 bus-width configurations in two-word or four-word burst mode
- -55 to +125°C military temperature grade
- Two independent unidirectional data ports for concurrent read/write transactions
- Double Data Rate (DDR) address port
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Memory core bit-interleaving to eliminate multi-bit errors
- 1.5–1.8 V (HSTL) I/O signaling standards
- Controller RTL IP cores with embedded EDAC available for Xilinx and Microchip FPGAs
- QML-V qualified

## Product Table

| Density | Part Number | Description | Operating Temp | Qual Level | TID [krad (Si)] | SEL [LET] | SEU [err/ dev.day] | SEFI [LET] |
|---|---|---|---|---|---|---|---|---|
| 72 Mbit | CYPT1542AV18-250GCMB | 72M QDR II+ x18 BURST of 2 Prototype | -55°C to 125°C | Prototype | — | — | — | — |
| | 5962F1120101VXA | 72M QDR II+ x18 BURST of 2 DLAM QML V | -55°C to 125°C | QML-V | 300 | > 120 (125°C) | <1.34e-7 | Immune 120 |
| | CYPT1543AV18-250GCMB | 72M QDR II+ x18 BURST of 4 Prototype | -55°C to 125°C | Prototype | — | — | — | — |
| | 5962F1120102VXA | 72M QDR II+ x18 BURST of 4 DLAM QML V | -55°C to 125°C | QML-V | 300 | > 120 (125°C) | <1.34e-7 | Immune 120 |
| | CYPT1543AV18-1X24M | 72M QDR II+ Prototype DIE | -55°C to 125°C | Prototype | — | — | — | — |
| | CYPT1544AV18-250GCMB | 72M QDR II+ x36 BURST of 2 Prototype | -55°C to 125°C | Prototype | — | — | — | — |
| | 5962F1120201VXA | 72M QDR II+ x36 BURST of 2 DLAM QML V | -55°C to 125°C | QML-V | 300 | > 120 (125°C) | <1.34e-7 | Immune 120 |
| | CYPT1545AV18-250GCMB | 72M QDR II+ x36 BURST of 4 Prototype | -55°C to 125°C | Prototype | — | — | — | — |
| | 5962F1120202VXA | 72M QDR II+ x36 BURST of 4 DLAM QML V | -55°C to 125°C | QML-V | 300 | > 120 (125°C) | <1.34e-7 | Immune 120 |

1) Total Ionizing Dose [Krad (Si)]

2) Single Event Latchup [LET] @ 125°C

3) Single Event Upset [err/bit.dy] Geo sync-solar min; Note: SEU is <1e-12 with Controller EDAC

4) Single Event Functional Interrupt [err/dev.dy] geo sync-solar min

5) Prompt dose information available on request

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