# MOTIX™ Bridge

TLE9166EQ

## About this document

### Scope and purpose

This user manual gives recommendations on how to use the TLE9166EQ as well as a description of the SPI registers.

This document must be used in conjunction with the device datasheet, which contains the full device specification.

### Intended audience

This document is intended for developers designing with the TLE9166EQ.

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# 1 Supply and operation modes

This section provides information about the supply pins, the transition from fail safe mode to normal mode, the watchdog, and the thermal clusters.

## 1.1 Supplies

This section gives background information about the supply pins as well as recommendations for the external capacitors for the VS and VDD pins.

VS and VDD are two separated supply pins so that the information stored in the registers is kept during a VS undervoltage event, provided that $V_{DD}$ stays within the operating range. The system can therefore operate once $V_S$ has recovered, without any new initialization of the control registers.

It is recommended to place:

- An electrolytic capacitor at the VS pin
- A 100 nF ceramic capacitor at the VS pin
- A 100 nF ceramic capacitor at the VDD pin

The electrolytic capacitor must be dimensioned to prevent $V_S$ from exceeding the absolute maximum rating for example when the integrated half-bridges are turned off while a DC motor is running, or when the ISO/TR7637 pulses are applied.

The 100 nF ceramic capacitors are filters for high frequency emissions, for an improved EMC behavior. These capacitors must be placed as close as possible to the VS and VDD pins with short connections to GND for an optimal filtering.

## 1.2 Operation modes

This section gives additional information about the transition from fail safe mode to normal mode.

From fail safe mode, the device enters the normal mode when the microcontroller sends these two consecutive SPI frames:

1. Clear GENSTAT1
2. Trigger the watchdog by sending a write command to GENCTRL1

## 1.3 Timeout watchdog

This section gives information about the timeout watchdog.

### Purpose of the watchdog

It is highly recommended to keep the watchdog enabled.

When activated, this feature turns off the outputs in case of failure, such as:

- A malfunction of the microcontroller, preventing a retrigger of the watchdog
- A disconnection of one SPI signal
- A short circuit of one SPI signal to $V_{DD}$
- A short circuit of one SPI signal to GND

### Watchdog retrigger

The watchdog is retriggered when the device receives an SPI write command to the control register GENCTRL1.

### Disabling the watchdog

It is recommended to keep the watchdog enabled. However, it is possible to disable the watchdog for development purposes with the following sequence:

1. Set the WDUNLOCK bit
2. Reset the WDEN bit in the next SPI frame

This sequence of two consecutive SPI frames involving two different control registers avoids an unintended deactivation of the watchdog by a single erroneous SPI frame.

### Watchdog monitoring

The microcontroller can monitor the incrementation of WDMON[1:0] (Figure 1) without triggering a watchdog error, ensuring that the watchdog timer is not frozen.

If the watchdog is not retriggered within the configured watchdog period, then the device goes in fail safe mode.

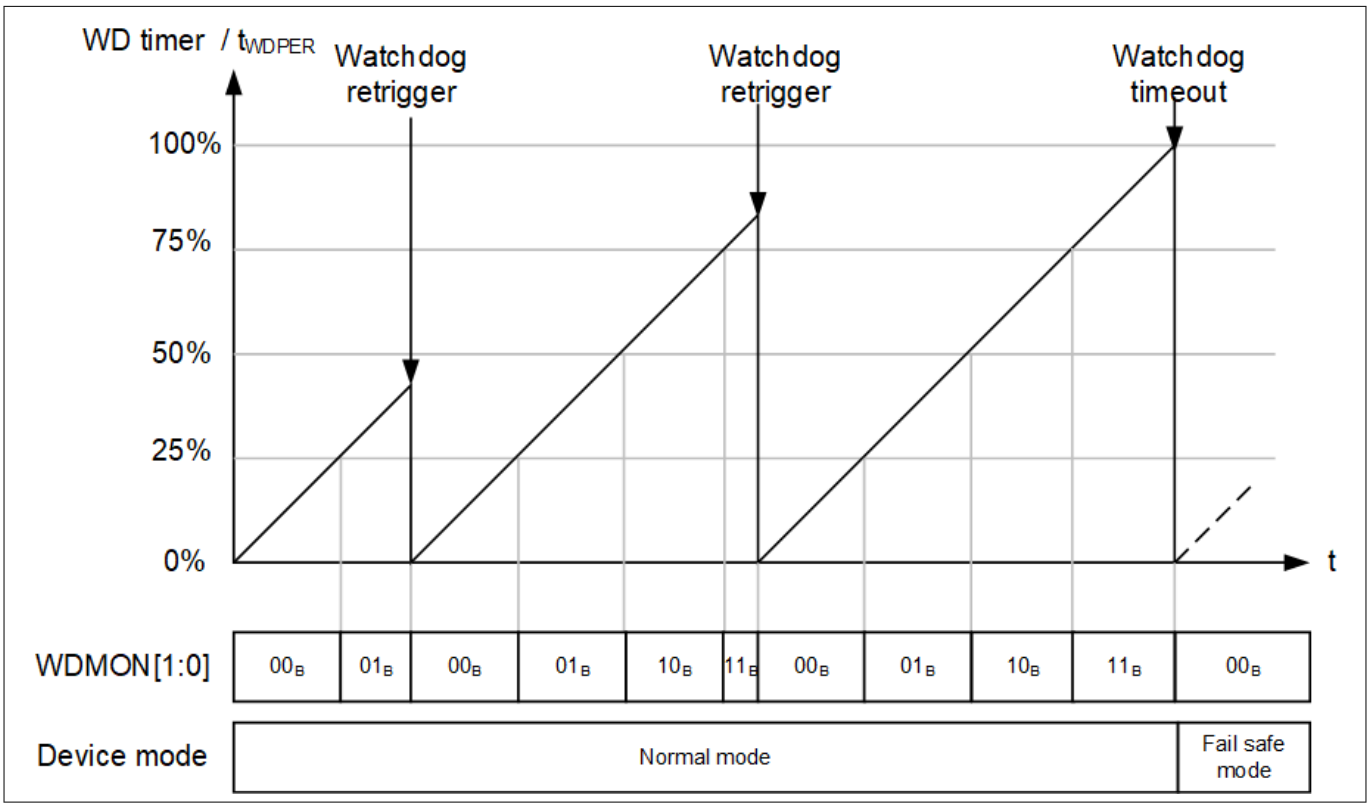



**Figure 1 Watchdog monitoring**

## 1.4 Temperature monitoring

This section gives additional information about the thermal clusters.

The thermal clusters allow a localization of the thermal warning and of the thermal shutdown events down to a group of outputs.

In case of a thermal shutdown event, only the outputs of the impacted thermal cluster are turned off. This does not affect the outputs of other thermal clusters.

# 2 Integrated power outputs

This chapter provides complementary information about the integrated half-bridges and the integrated high-sides.

## 2.1 Integrated half-bridges

### Body diodes

Thanks to the built-in body diodes of the high-side and low-side MOSFETs, the integrated half-bridges can control inductive loads without external diodes.

### Current monitoring in PWM operation

The device supports both high-side and low-side PWM up to 25 kHz, for example for the control of the speed of a motor.

It is also possible to monitor the current flowing through the high-sides with the CM pin.

If a monitoring of the load current during PWM operation is required, it is recommended to configure a low-side as PWM MOSFET, and to map the CM pin to the high-side which is permanently on. The current in this high-side is continuous and is equal to the load current, even during the PWM off-time.

For example, a DC motor is controlled by OUT1 and OUT2. The low-side of OUT1 is configured as PWM MOSFET. OUT1 can be configured either with passive freewheeling or active freewheeling.

The CM pin must be mapped to the high-side of OUT2 (Figure 2).

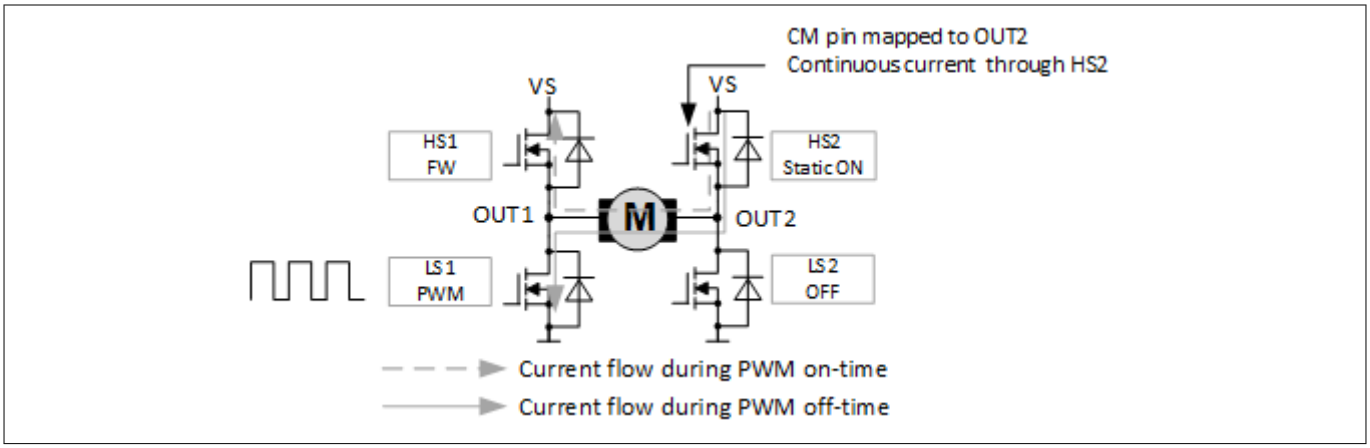



**Figure 2 Example of PWM operation with current monitoring**

### Pairing between half-bridges

It is possible to enable the so-called pairing between half-bridges in static mode with enabled overcurrent recovery. This function is implemented to control motors with significant parallel capacitors, up to 1 µF (Figure 3), which can trigger an overcurrent or a short circuit detection caused by:

- The charge of $C_{MOTOR}$
- The ringing caused by the switching of one MOSFET in combination with $C_{MOTOR}$ and the stray inductance of the cables to the motors

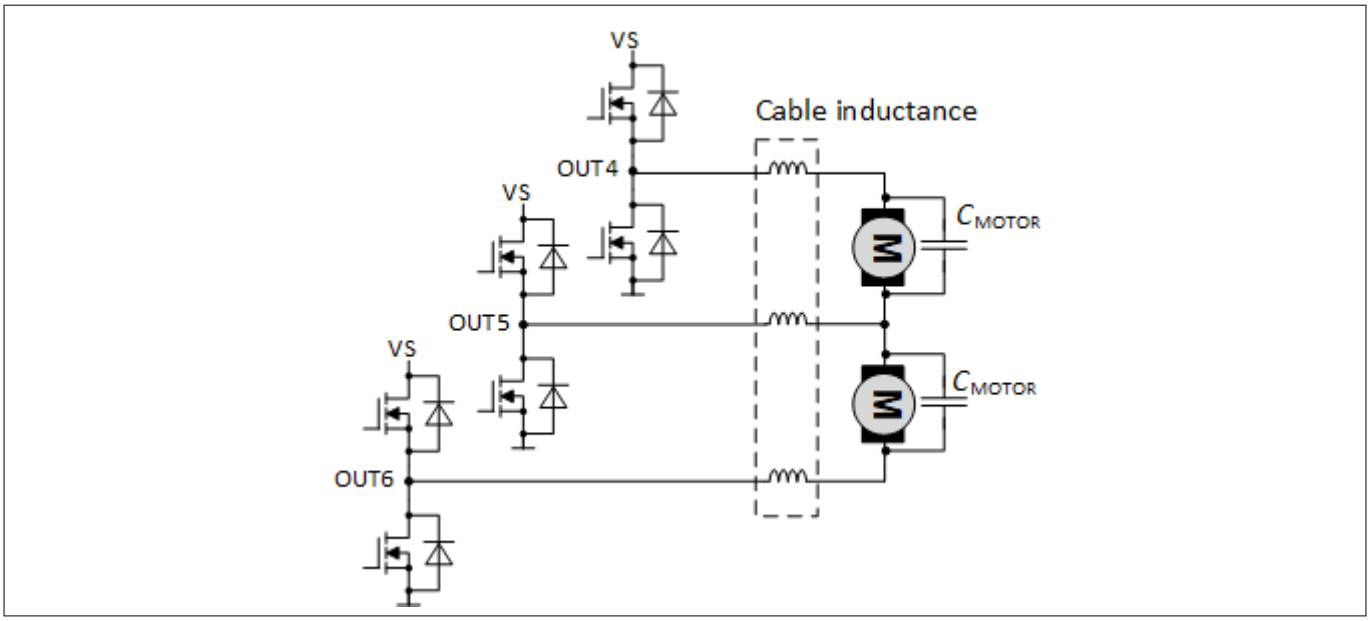



**Figure 3 Group of paired half-bridges**

When the pairing is enabled, the turn-on and the turn-off of one MOSFET can force (depending on the conditions) a blank time $t_{BLK_OCOL3}$ to an another paired half-bridge, avoiding an overcurrent or short circuit detection caused by the charge of $C_{MOTOR}$ or by ringings.

## 2.2 Integrated high-sides

This section provides complementary information about the constant current modes of the integrated high-sides.

The purpose of the constant current modes CCM1, CCM2 and CCM3 is to allow the integrated high-sides OUT7 to OUT12 to control capacitive loads while preventing an overcurrent detection in normal conditions:

- CCM1 and CCM2 are optimized for modules with significant input capacitors in the range of a few µF
- CCM3 is optimized for LED strings with a capacitor connected to OUTx in the range of a few hundreds of nF

Modules are in general not controlled in PWM by OUTx in contrast to LED strings.

If these capacitors are charged without constant current modes (CCM), the output may be switched off because of an overcurrent detection.

When the CCM is enabled, the output limits the current during $t_{CCMx}$ to a level which is lower than the overcurrent detection, in order to charge the capacitor. After $t_{CCMx}$, the output switches to $R_{DS(ON)}$ mode to lower the power dissipation in the high-side.

### Differences between CCM1 and CCM2

CCM1 has one single current limitation, while CCM2 has a two-step current limitation.

The first current limitation level of CCM2 when $V_{OUTx} \leq V_{OUT_LOW}$ is identical to that of CCM1.

For CCM2: the condition $V_{OUTx} \geq V_{OUT_LOW}$ indicates the absence of a short circuit, allowing to increase the current limitation to $I_{CCM2}$.

The second current limitation $I_{CCM2}$:

- Allows a faster charge of the input capacitor of the module
- Provides more current to the module, for example for a DC/DC converter operating at low supply voltage

#### CCM3

CCM3 also implements a two-step current limitation, similar to CCM2. However, since LED strings can be controlled using PWM, CCM3 has higher current limitation levels and a shorter duration compared to CCM2, to support the PWM operation.

## 2.3 Overcurrent recovery

The overcurrent recovery (OCR) feature allows the control of loads with inrush currents exceeding the overcurrent detection threshold of the respective outputs. This is particularly useful for DC motors connected to the integrated half-bridges and for a bulb connected to OUT7 in low $R_{DS(ON)}$ mode

***Note**: It is recommended to minimize the operation in OCR for reliability reasons, especially in short circuit conditions. Therefore, the OCR should be disabled when the inrush phase is over.*

#### Overcurrent recovery time

It is possible to extend the on-phase of the output when an overcurrent is detected with the overcurrent recovery time ( $t_{OCR}$ ) to increase the average current delivered to the load.

$t_{OCR}$ is longer for the integrated half-bridge because the inductance of the motor limits the rate of the current increase.

In contrast, $t_{OCR}$ is shorter for OUT7 in low $R_{DS(ON)}$ because the low resistance of the cold bulb filament allows a high increase rate of the load current. It is recommended to limit $t_{OCR}$ for a 10 W bulb to 6 µs to limit the increase of the junction temperature during each activation cycle.

#### OCR off-time

The OCR off-time $t_{OCR_OFF}$ allows a decrease of the output temperature between two activations.

#### Short circuit detection during OCR

The short circuit detection during OCR differs for half-bridges and OUT7 due to the different types of load.

For half-bridges: in normal conditions, the inductance of the motor limits the current increase. Therefore it is possible to detect short circuits by monitoring $I_{OUTx}$.

For OUT7: Monitoring $I_{OUT7}$ alone is not sufficient to distinguish between a cold filament of a 10 W bulb from a low ohmic short circuit to GND. Instead, the cold filament of a 10 W bulb has a higher resistance than a low ohmic short circuit. That is the reason why the short circuit diagnostic done by monitoring $V_{OUT7}$ at the end of $t_{OCR}$.

# 3 VCC2 voltage regulator

The configuration of OUT12_VCC2 as high-side, 5 V regulator or as 3.3 V regulator is latched at the start-up of the device, to avoid an unintentional wrong settings during the device operation.

When configured as a voltage regulator, OUT12_VCC2 is protected against short circuits to the battery, to avoid reverse current from the OUT12_VCC2 pin back to the VS pin. This allows the supply of off-boards sensors for example.

# 4 Electrochromic mirror control

When the electrochromic (EC) mirror control is activated by SPI settings, OUT10 supplies the external MOSFET controlling the EC mirror for diagnostic purposes. Indeed, the diagnostic functions of the OUT10 enables the detection of a short circuit or of an open load condition.

For stability reasons:

- $C_{ECDR}$, $C_{ECV}$ and Q1 must be placed close to each other
- The GND connection of TLE9166, $C_{ECDR}$ and $C_{ECV}$ must have star connection with low impedance

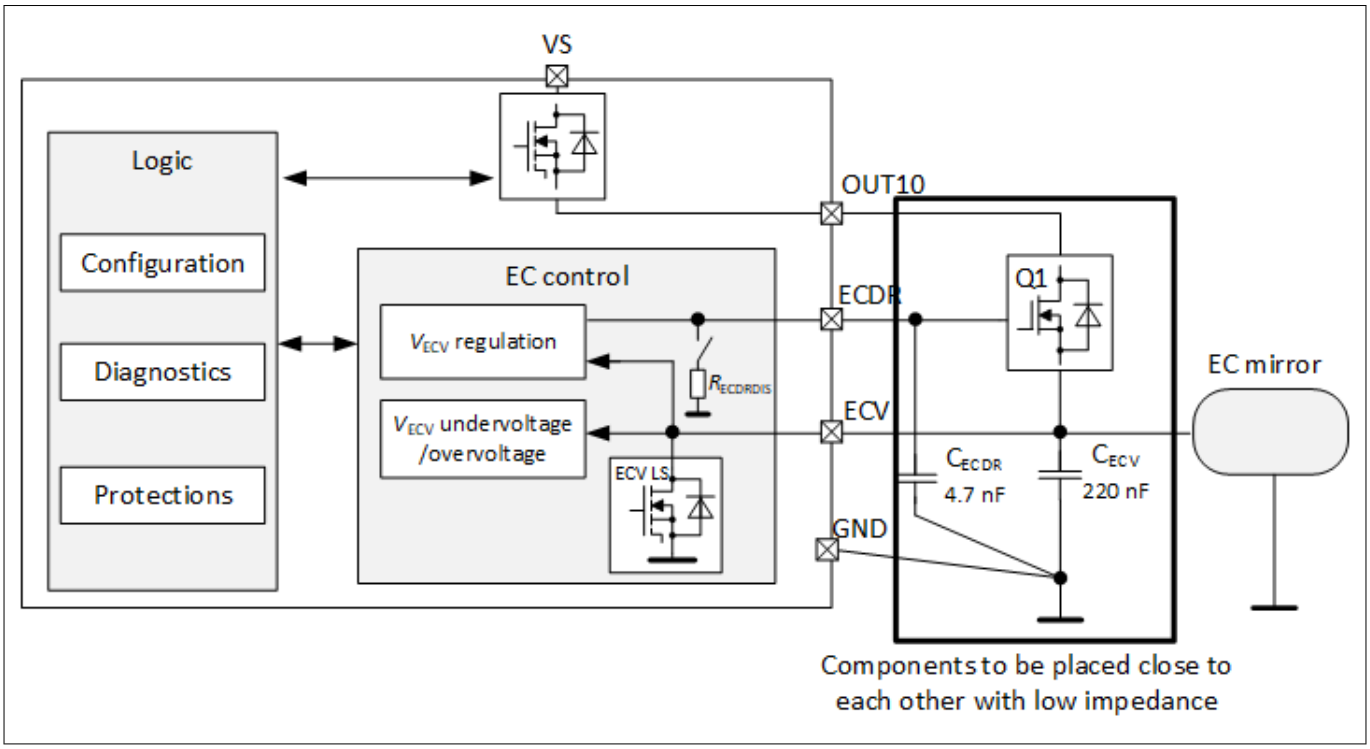



**Figure 4 Driver for electrochromic mirror**

# 5 High-side MOSFET driver for mirror heater

### Off-state diagnostic

The device supports diagnostics while the external MOSFET is off.

For that, the MOSFET driver must be in active off mode: The gate of the MOSFET is actively discharged and the pull-up diagnostic current ($I_{PUDIAG}$) is activated. A high threshold at the VSH pin indicates an open load condition or a short circuit of the VSH pin to the battery (Table 1).

**Table 1 $V_{SH}$ during off-state diagnostic**

| Conditions | Normal load | Short circuit SH to GND | Short circuit SH to VBAT | Open load |
|---|---|---|---|---|
| $V_{SH}$ | Low | Low | High | High |

***Note**: The drain-source overvoltage must be set to 2 V nom. for the off-state diagnostic.*

It is not possible to distinguish a short circuit of the SH pin to GND from a normal load with the off-state diagnostic. The short circuit to GND can only be detected with the drain-source overvoltage detection in on-state.

# 6 SPI protocol

This chapter provides complementary information about the SPI protocol.

### Global error flag

The global error flag (GEF) enables a fast diagnostic without sending a complete SPI frame.
To use the GEF without a complete SPI frame, the microcontroller must pull CSN to low while keeping SCLK low.

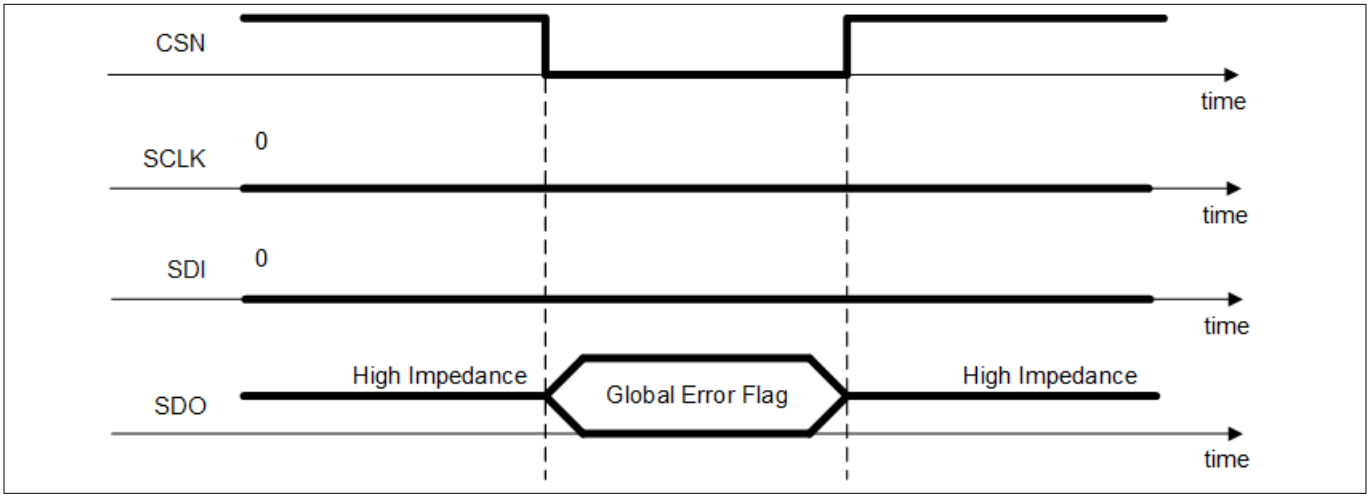



**Figure 5 Fast diagnostic with the global error flag**

### Polarity of the NPOR bit

Unlike the other status bits of the global status byte (GSB), the status bit for the power-on reset (NPOR) is active low.

After a successful clearing of GENSTAT1, NPOR is set. The microcontroller can therefore detect a short circuit of SDO to GND or to VDD.

In normal conditions (after clearing GENSTAT1), NPOR = 1 while the other bits of the GSB are reset. Therefore, a GSB with all bits reset means that SDO has a short circuit to GND.

It is very unlikely to have a the same time a thermal warning, a thermal shutdown, as supply error, a load error, a SPI error and a fail safe mode. Therefore, a GSB with all bits set can be interpreted as a short circuit of SDO to VDD.

### Detection of shorted SDO or of a device is in sleep mode

The SPI protocol has been defined so that:

- At least one bit is 0: Bit0 of the global status byte is reset in normal conditions.
- At least one bit is 1. Bit3 of the global status byte NPOR is set after a clear command to GENSTAT1 has been received by the TLE9166.

As a result, once GENSTAT1 has been cleared, a SPI frame will all bits of the global status byte set or reset can be excluded, except in the following cases:

- SDO has a short circuit
- The device is in sleep mode (SDO is in high impedance)

# 7 SPI register information

## 7.1 Register overview - DOORIC (ascending offset address)

**Table 2 Register overview - DOORIC (ascending offset address)**

| Short name | Long name | Offset address | Page number |
|---|---|---|---|
| GENCTRL1 | Data control register 1 | $01_H$ | 13 |
| GENCTRL2 | Data control register 2 | $02_H$ | 16 |
| GENCTRL3 | Data control register 3 | $03_H$ | 18 |
| GENCTRL4 | Data control register 4 | $04_H$ | 20 |
| GENCTRL5 | Data control register 5 | $05_H$ | 22 |
| GENCTRL6 | Data control register 6 | $06_H$ | 25 |
| GENCTRL7 | Data control register 7 | $07_H$ | 27 |
| GENCTRL8 | Data control register 8 | $08_H$ | 30 |
| GENCTRL9 | Data control register 9 | $09_H$ | 31 |
| GENCTRL10 | Data control register 10 | $0A_H$ | 32 |
| GENSTAT1 | General status register 1 | $0B_H$ | 33 |
| GENSTAT2 | General status register 2 | $0C_H$ | 36 |
| GENSTAT3 | General status register 3 | $0D_H$ | 38 |
| GENSTAT4 | General status register 4 | $0E_H$ | 40 |

## 7.2 Data control register 1

**GENCTRL1** Offset address: $01_H$

Data control register 1 Reset values see: Table 3

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | OUT12_VCC2_EN | OUT12_VCC2_CFG | | OUT12_VCC2_FS | ECDR_GM | ECVLS | ECV_FS | ECDR_DAC |
| r | | | | | | | | rwh | rw | | rwh | rwh | rwh | rwh | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ECDR_DAC | | | | | ECV_OUT10_CFG | | MASKTW | MASKOL | CMSEL | | | | WDPER | WDEN | EN |
| rwh | | | | | rwh | | rwh | rwh | rwh | | | | rwh | rwh | rwh |

| Field | Bits | Type | Description |
|---|---|---|---|
| EN | 0 | rwh | **Device enable bit**<br>$0_B$ **Setting1**: The device is in sleep mode(default)<br>$1_B$ **Setting2**: The device is in normal mode |
| WDEN | 1 | rwh | **Watchdog enable bit**<br>$0_B$ **Setting1**: The watchdog is disabled<br>$1_B$ **Setting2**: The watchdog is enabled(default) |
| WDPER | 2 | rwh | **Watchdog period selection**<br>$0_B$ **Setting1**: Watchdog period=50 m(default)<br>$1_B$ **Setting2**: Watchdog period=250 ms |
| CMSEL | 6:3 | rwh | **Current or VS ratio multiplexer selection**<br>$0_H$ **Setting1**: CM pin in HZ(default)<br>$1_H$ **Setting2**: OUT1(HS) current monitoring is selected<br>$2_H$ **Setting3**: OUT2(HS) current monitoring is selected<br>$3_H$ **Setting4**: OUT3(HS) current monitoring is selected<br>$4_H$ **Setting5**: OUT4(HS) current monitoring is selected<br>$5_H$ **Setting6**: OUT5(HS) current monitoring is selected<br>$6_H$ **Setting7**: OUT6(HS) current monitoring is selected<br>$7_H$ **Setting8**: OUT7 current monitoring is selected<br>$8_H$ **Setting9**: OUT8 current monitoring is selected<br>$9_H$ **Setting10**: OUT9 current monitoring is selected<br>$A_H$ **Setting11**: OUT10 current monitoring is selected<br>$B_H$ **Setting12**: OUT11 current monitoring is selected<br>$C_H$ **Setting13**: OUT12(HS) current monitoring is selected<br>$D_H$ **Setting14**: VS ratio 0.2*VS is selected<br>$E_H$ **Setting15**: VS ratio 0.13*VS is selected<br>$F_H$ **Setting16**: CM pin in HZ(default) |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| MASKOL | 7 | rwh | **Open load mask bit**<br>$0_B$ **Setting1**: Open load conditions are reported in GEF(default)<br>$1_B$ **Setting2**: Open load conditions are not reported in GEF |
| MASKTW | 8 | rwh | **Temperature warning mask bit**<br>$0_B$ **Setting1**: Temperature warning conditions are reported in GEF(default)<br>$1_B$ **Setting2**: Temperature warning conditions are not reported in GEF |
| ECV_OUT10_CFG | 10:9 | rwh | **ECV and OUT10 configutation**<br>$00_B$ **Setting1**: ECV is configured as standalone low-side switch controled by ECVLS bit. The pasive pull down resistor RECDRDIS is connected if ECVLS=0b(default)<br>$01_B$ **Setting2**: ECV and OUT10 are configured in half-bridge mode controled by ECVLS bit respective OUT10EN bit( cross current protection is implemented). The passive pulldown resistor RECDRDIS is disconnected.<br>$10_B$ **Setting3**: ECV regulation is enabled for electrochromic mirror control.<br>$11_B$ **Setting4**: The low-side switch can be control by ECVLS bit during ECV regulation independent of ECV overvoltage filtered signal |
| ECDR_DAC | 16:11 | rwh | **ECV VTARGET DAC setting** |
| ECV_FS | 17 | rwh | **ECV Vtarget full scale range**<br>$0_B$ **Setting1**: VTARGET values = 0....VTARGET_MAX1(default)<br>$1_B$ **Setting2**: VTARGET values = 0....VTARGET_MAX2. VTARGET is clamped to VTARGET_MAX2. |
| ECVLS | 18 | rwh | **Enable ECV low-side**<br>$0_B$ **Setting1**: ECV low-side is deactivated(default)<br>$1_B$ **Setting2**: ECV low-side is activated |
| ECDR_GM | 19 | rwh | **ECDR error amplifier current capability**<br>$0_B$ **Setting1**: IECDR_source1 and IECDR_sink1 are selected(default)<br>$1_B$ **Setting2**: IECDR_source2 and IECDR_sink2 are selected |
| OUT12_VCC2_FS | 20 | rwh | **OUT12_VCC2 fail safe mode enable bit**<br>$0_B$ **Setting1**: OUT12_VCC2 is disabled in fail safe mode(default)<br>$1_B$ **Setting2**: OUT12_VCC2 is enabled in fail safe mode according with the OUT12_VCC2_EN bit setting |
| OUT12_VCC2_CFG | 22:21 | rw | **OUT12_VCC2 configuration bits**<br>$00_B$ **Setting1**: VCC2 with 3.3 V regulated output voltage(default)<br>$01_B$ **Setting2**: VCC2 with 5 V regulated output voltage<br>$10_B$ **Setting3**: High Side<br>$11_B$ **Setting4**: VCC2 with 3.3 V regulated output voltage |
| OUT12_VCC2_EN | 23 | rwh | **OUT12_VCC2 enable bit**<br>$0_B$ **Setting1**: OUT12_VCC2 disabled(default)<br>$1_B$ **Setting2**: OUT12_VCC2 enabled |

## 7 SPI register information

**Table 3 Reset values of GENCTRL1**

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX00 $0002_H$ | Reset value at power-on |
| Soft_reset | ---- ----<br>---- 0000<br>0000 0000<br>0000 001$-_B$ | Reset the regs when enter FS |

## 7.3 Data control register 2

**GENCTRL2** Offset address: $02_H$

Data control register 2 Reset values see: Table 4

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | RES | OUT5PAIR | | OUT1PAIR | | | OUT 11EN | OUT 10EN |
| r | | | | | | | | r | rwh | | rwh | | | rwh | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUT9 EN | OUT 8EN | OUT7EN | | OUT6EN | | OUT5EN | | OUT4EN | | OUT3EN | | OUT2EN | | OUT1EN | |
| rwh | rwh | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1EN | 1:0 | rwh | **OUT1 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT1 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT1 ON<br>$10_B$ **Setting3**: High-side of OUT1 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT1 OFF |
| OUT2EN | 3:2 | rwh | **OUT2 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT2 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT2 ON<br>$10_B$ **Setting3**: High-side of OUT2 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT2 OFF |
| OUT3EN | 5:4 | rwh | **OUT3 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT3 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT3 ON<br>$10_B$ **Setting3**: High-side of OUT3 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT3 OFF |
| OUT4EN | 7:6 | rwh | **OUT4 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT4 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT4 ON<br>$10_B$ **Setting3**: High-side of OUT4 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT4 OFF |
| OUT5EN | 9:8 | rwh | **OUT5 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT5 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT5 ON<br>$10_B$ **Setting3**: High-side of OUT5 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT5 OFF |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT6EN | 11:10 | rwh | **OUT6 enable**<br>$00_B$ **Setting1**: Low-side and high-side of OUT6 OFF(default)<br>$01_B$ **Setting2**: Low-side of OUT6 ON<br>$10_B$ **Setting3**: High-side of OUT6 ON<br>$11_B$ **Setting4**: Low-side and high-side of OUT6 OFF |
| OUT7EN | 13:12 | rwh | **OUT7 enable**<br>$00_B$ **Setting1**: OUT7 OFF(default)<br>$01_B$ **Setting2**: OUT7 ON with low RDSON<br>$10_B$ **Setting3**: OUT7 ON with high RDSON<br>$11_B$ **Setting4**: OUT7 OFF |
| OUT8EN | 14 | rwh | **OUT8 enable**<br>$0_B$ **Setting1**: OUT8 OFF(default)<br>$1_B$ **Setting2**: OUT8 ON |
| OUT9EN | 15 | rwh | **OUT9 enable**<br>$0_B$ **Setting1**: OUT9 OFF(default)<br>$1_B$ **Setting2**: OUT9 ON |
| OUT10EN | 16 | rwh | **OUT10 enable**<br>$0_B$ **Setting1**: OUT10 OFF(default)<br>$1_B$ **Setting2**: OUT10 ON |
| OUT11EN | 17 | rwh | **OUT11 enable**<br>$0_B$ **Setting1**: OUT11 OFF(default)<br>$1_B$ **Setting2**: OUT11 ON |
| OUT1PAIR | 20:18 | rwh | **OUT1 paired settings**<br>$000_B$ **Setting1**: no pairing (default)<br>$001_B$ **Setting2**: OUT1 paired with OUT2<br>$010_B$ **Setting3**: OUT1 paired with OUT3<br>$011_B$ **Setting4**: OUT1 paired with OUT2 and OUT3<br>$100_B$ **Setting5**: OUT1 paired with OUT6<br>$101_B$ **Setting6**: OUT1 paired with OUT2 and OUT6<br>$110_B$ **Setting7**: OUT1 paired with OUT3 and OUT6<br>$111_B$ **Setting8**: OUT1 paired with OUT2, OUT3 and OUT6 |
| OUT5PAIR | 22:21 | rwh | **OUT5 paired settings**<br>$00_B$ **Setting1**: no pairing (default)<br>$01_B$ **Setting2**: OUT5 paired with OUT4<br>$10_B$ **Setting3**: OUT5 paired with OUT6<br>$11_B$ **Setting4**: OUT5 paired with OUT4 and OUT6 |
| RES | 23 | r | |

**Table 4 Reset values of** GENCTRL2

| Reset type | Reset value | Note |
|---|---|---|
| Reset | $XX00\ 0000_H$ | |
| Soft_reset | $--00\ 0000_H$ | Reset the regs when enter FS |

## 7.4 Data control register 3

**GENCTRL3** Offset address: $03_H$

Data control register 3 Reset values see: Table 5

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | GDRV | | ICHG_DSCHG | | | | OUT12CCM | |
| r | | | | | | | | rwh | | rwh | | | | rwh | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUT11CCM | | OUT10CCM | | OUT9CCM | | OUT8CCM | | OUT7CCM | | OCTH_OUT5 | | OCTH_OUT6 | | OCTH_OUT1 | |
| rwh | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OCTH_OUT1 | 1:0 | rwh | **Overcurrent high-side/low-side threshold**<br>$00_B$ **Setting1**: \|IOC_OUT1\|=2 A(default)<br>$01_B$ **Setting2**: \|IOC_OUT1\|=3 A<br>$10_B$ **Setting3**: \|IOC_OUT1\|=4 A<br>$11_B$ **Setting4**: \|IOC_OUT1\|=2 A |
| OCTH_OUT6 | 3:2 | rwh | **Overcurrent high-side/low-side threshold**<br>$00_B$ **Setting1**: \|IOC_OUT6\|=2 A(default)<br>$01_B$ **Setting2**: \|IOC_OUT6\|=3 A<br>$10_B$ **Setting3**: \|IOC_OUT6\|=4 A<br>$11_B$ **Setting4**: \|IOC_OUT6\|=2 A |
| OCTH_OUT5 | 5:4 | rwh | **Overcurrent high-side/low-side threshold**<br>$00_B$ **Setting1**: \|IOC_OUT5\|=4 A(default)<br>$01_B$ **Setting2**: \|IOC_OUT5\|=6 A<br>$10_B$ **Setting3**: \|IOC_OUT5\|=7.5 A<br>$11_B$ **Setting4**: \|IOC_OUT5\|=4 A |
| OUT7CCM | 7:6 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |
| OUT8CCM | 9:8 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |
| OUT9CCM | 11:10 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT10CCM | 13:12 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |
| OUT11CCM | 15:14 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |
| OUT12CCM | 17:16 | rwh | **Selection between constant current modes or RDSON mode**<br>$00_B$ **Setting1**: RDSON mode(default)<br>$01_B$ **Setting2**: Constant current mode 1<br>$10_B$ **Setting3**: Constant current mode 2<br>$11_B$ **Setting4**: Constant current mode 3 |
| ICHG_DSCHG | 21:18 | rwh | **Mirror heater GH charge and discharge currents**<br>$0_H$ **Setting1**: Ichg=0.5 mA , Idchg=-0.5 mA<br>$1_H$ **Setting2**: Ichg=1 mA , Idchg=-1 mA<br>$2_H$ **Setting3**: Ichg=1.5 mA , Idchg=-1.5 mA<br>$3_H$ **Setting4**: Ichg=2 mA , Idchg=-2 mA(default)<br>$4_H$ **Setting5**: Ichg=2.5 mA , Idchg=-2.5 mA<br>$5_H$ **Setting6**: Ichg=3 mA , Idchg=-3 mA<br>$6_H$ **Setting7**: Ichg=4 mA , Idchg=-4 mA<br>$7_H$ **Setting8**: Ichg=5 mA , Idchg=-5 mA<br>$8_H$ **Setting9**: Ichg=7 mA , Idchg=-7 mA<br>$9_H$ **Setting10**: Ichg=10 mA , Idchg=-10 mA<br>$A_H$ **Setting11**: Ichg=12.5 mA , Idchg=-12.5 mA<br>$B_H$ **Setting12**: Ichg=2 mA , Idchg=-2 mA<br>…<br>$F_H$ **Setting16**: Ichg=2 mA , Idchg=-2 mA |
| GDRV | 23:22 | rwh | **Heater gate driver control**<br>$00_B$ **Setting1**: The MOSFET gate is discharged to GND through the RGHDIS(default)<br>$01_B$ **Setting2**: The MOSFET gate is actively discharged by the MOSFET driver<br>$10_B$ **Setting3**: The MOSFET gate is charged by the MOSFET driver<br>$11_B$ **Setting4**: The MOSFET gate is discharged to GND through the RGHDIS |

**Table 5 Reset values of GENCTRL3**

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX0C $0000_H$ | |
| Soft_reset | –-0C $0000_H$ | Reset the regs when enter FS |
| Soft_reset_s9144 | –-00 $0000_H$ | Reset the regs for s9144 variant |

## 7.5 Data control register 4

**GENCTRL4** Offset address: $04_H$

Data control register 4 Reset values see: Table 6

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Res** | | | | | | | | | | **IHOLD** | **OUT9PWM** | | | **OUT8PWM** | |
| r | | | | | | | | | | rwh | rwh | | | rwh | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OUT8PWM** | **OUT7PWM** | | | **OUT6PWM** | | **OUT5PWM** | | **OUT4PWM** | | **OUT3PWM** | | **OUT2PWM** | | **OUT1PWM** | |
| rwh | rwh | | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1PWM | 1:0 | rwh | **OUT1 external PWM control**<br>$00_B$ **Setting1**: OUT1 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT1 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT1 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT1 not mapped to external PWM |
| OUT2PWM | 3:2 | rwh | **OUT2 external PWM control**<br>$00_B$ **Setting1**: OUT2 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT2 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT2 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT2 not mapped to external PWM |
| OUT3PWM | 5:4 | rwh | **OUT3 external PWM control**<br>$00_B$ **Setting1**: OUT3 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT3 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT3 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT3 not mapped to external PWM |
| OUT4PWM | 7:6 | rwh | **OUT4 external PWM control**<br>$00_B$ **Setting1**: OUT4 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT4 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT4 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT4 not mapped to external PWM |
| OUT5PWM | 9:8 | rwh | **OUT5 external PWM control**<br>$00_B$ **Setting1**: OUT5 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT5 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT5 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT5 not mapped to external PWM |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT6PWM | 11:10 | rwh | **OUT6 external PWM control**<br>$00_B$ **Setting1**: OUT6 not mapped to external PWM(default)<br>$01_B$ **Setting2**: OUT6 mapped to external PWM with passive FW<br>$10_B$ **Setting3**: OUT6 mapped to external PWM with active FW<br>$11_B$ **Setting4**: OUT6 not mapped to external PWM |
| OUT7PWM | 14:12 | rwh | **OUT7 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT7 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT7 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT7 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT7 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT7 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT7 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT7 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT7 not mapped to internal PWM channels |
| OUT8PWM | 17:15 | rwh | **OUT8 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT8 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT8 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT8 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT8 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT8 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT8 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT8 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT8 not mapped to internal PWM channels |
| OUT9PWM | 20:18 | rwh | **OUT9 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT9 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT9 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT9 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT9 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT9 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT9 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT9 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT9 not mapped to internal PWM channels |
| IHOLD | 21 | rwh | **Mirror heater Gx hold current**<br>$0_B$ **Setting1**: 5 mA(default)<br>$1_B$ **Setting2**: 12.5 mA |

**Table 6 Reset values of** GENCTRL4

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX00 $0000_H$ | |
| Soft_reset | –-00 $0000_H$ | Reset the regs when enter FS |

## 7.6 Data control register 5

**GENCTRL5** Offset address: $05_H$

Data control register 5 Reset values see: Table 7

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | RES | OUTx_SC_CFG | OUT7CL | OUT7_TOCR_OFF | | OUT7_TOCR | | OUT7SR |
| r | | | | | | | | r | rwh | rwh | rwh | | rwh | | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUT7OCR | OUT6OCR | OUT5OCR | OUT4OCR | OUT3OCR | OUT2OCR | OUT1OCR | OUT12PWM | | | OUT11PWM | | | OUT10PWM | | |
| rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | | | rwh | | | rwh | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT10PWM | 2:0 | rwh | **OUT10 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT10 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT10 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT10 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT10 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT10 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT10 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT10 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT10 not mapped to internal PWM channels |
| OUT11PWM | 5:3 | rwh | **OUT11 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT11 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT11 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT11 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT11 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT11 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT11 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT11 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT11 not mapped to internal PWM channels |
| OUT12PWM | 8:6 | rwh | **OUT12 internal PWM or current mode control**<br>$000_B$ **Setting1**: OUT12 not mapped to internal PWM channels(default)<br>$001_B$ **Setting2**: OUT12 mapped to internal PWM1 channel<br>$010_B$ **Setting3**: OUT12 mapped to internal PWM2 channel<br>$011_B$ **Setting4**: OUT12 mapped to internal PWM3 channel<br>$100_B$ **Setting5**: OUT12 mapped to internal PWM4 channel<br>$101_B$ **Setting6**: OUT12 mapped to internal PWM5 channel<br>$110_B$ **Setting7**: OUT12 mapped to internal PWM6 channel<br>$111_B$ **Setting8**: OUT12 not mapped to internal PWM channels |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1OCR | 9 | rwh | **OUT1 overcurrent recovery**<br>$0_B$ **Setting1**: OUT1 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT1 overcurrent recovery enable |
| OUT2OCR | 10 | rwh | **OUT2 overcurrent recovery**<br>$0_B$ **Setting1**: OUT2 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT2 overcurrent recovery enable |
| OUT3OCR | 11 | rwh | **OUT3 overcurrent recovery**<br>$0_B$ **Setting1**: OUT3 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT3 overcurrent recovery enable |
| OUT4OCR | 12 | rwh | **OUT4 overcurrent recovery**<br>$0_B$ **Setting1**: OUT4 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT4 overcurrent recovery enable |
| OUT5OCR | 13 | rwh | **OUT5 overcurrent recovery**<br>$0_B$ **Setting1**: OUT5 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT5 overcurrent recovery enable |
| OUT6OCR | 14 | rwh | **OUT6 overcurrent recovery**<br>$0_B$ **Setting1**: OUT6 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT6 overcurrent recovery enable |
| OUT7OCR | 15 | rwh | **OUT7 overcurrent recovery**<br>$0_B$ **Setting1**: OUT7 overcurrent recovery disable(default)<br>$1_B$ **Setting2**: OUT7 overcurrent recovery enable |
| OUT7SR | 16 | rwh | **OUT7 low RON in overcurrent slew rate control**<br>$0_B$ **Setting1**: OUT7 low RON in overcurrent slew rate=10 V/us(default)<br>$1_B$ **Setting2**: OUT7 low RON in overcurrent slew rate=0.5 V/us |
| OUT7_TOCR | 18:17 | rwh | **OUT7 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT7 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT7 overcurrent recovery ON time=3 us<br>$10_B$ **Setting3**: OUT7 overcurrent recovery ON time=6 us<br>$11_B$ **Setting4**: OUT7 overcurrent recovery ON time=9 us |
| OUT7_TOCR_OFF | 20:19 | rwh | **OUT7 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT7 overcurrent recovery OFF time=100 us<br>$01_B$ **Setting2**: OUT7 overcurrent recovery OFF time=200 us(default)<br>$10_B$ **Setting3**: OUT7 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT7 overcurrent recovery OFF time=600 us |
| OUT7CL | 21 | rwh | **OUT7 low RON current limitation config**<br>$0_B$ **Setting1**: OUT7 low RON current limitation=3.6 A<br>$1_B$ **Setting2**: OUT7 low RON current limitation=4.6 A(default) |

(table continues...)

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUTx_SC_CFG | 22 | rwh | **OUT1 to OUT6 short circuit events configuration when the OCR function is activated.**<br>$0_B$ **Setting1**: First short circuit event latch-off the OUTx(default)<br>$1_B$ **Setting2**: Second consecutive short circuit event lached-off the OUTx |
| RES | 23 | r | **Reserved bit** |

**Table 7 Reset values of** GENCTRL5

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX28 $0000_H$ | |
| Soft_reset | –-28 $0000_H$ | Reset the regs when enter FS |

## 7.7 Data control register 6

**GENCTRL6** Offset address: $06_H$

Data control register 6 Reset values see: Table 8

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Res** | | | | | | | | **OUT6_TOCR_OFF** | | **OUT6_TOCR** | | **OUT5_TOCR_OFF** | | **OUT5_TOCR** | |
| r | | | | | | | | rwh | | rwh | | rwh | | rwh | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OUT4_TOCR_OFF** | | **OUT4_TOCR** | | **OUT3_TOCR_OFF** | | **OUT3_TOCR** | | **OUT2_TOCR_OFF** | | **OUT2_TOCR** | | **OUT1_TOCR_OFF** | | **OUT1_TOCR** | |
| rwh | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | | rwh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1_TOCR | 1:0 | rwh | **OUT1 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT1 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT1 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT1 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT1 overcurrent recovery ON time=48 us |
| OUT1_TOCR_OFF | 3:2 | rwh | **OUT1 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT1 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT1 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT1 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT1 overcurrent recovery OFF time=600 us |
| OUT2_TOCR | 5:4 | rwh | **OUT2 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT2 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT2 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT2 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT2 overcurrent recovery ON time=48 us |
| OUT2_TOCR_OFF | 7:6 | rwh | **OUT2 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT2 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT2 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT2 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT2 overcurrent recovery OFF time=600 us |
| OUT3_TOCR | 9:8 | rwh | **OUT3 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT3 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT3 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT3 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT3 overcurrent recovery ON time=48 us |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT3_TOCR_OFF | 11:10 | rwh | **OUT3 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT3 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT3 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT3 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT3 overcurrent recovery OFF time=600 us |
| OUT4_TOCR | 13:12 | rwh | **OUT4 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT4 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT4 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT4 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT4 overcurrent recovery ON time=48 us |
| OUT4_TOCR_OFF | 15:14 | rwh | **OUT4 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT4 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT4 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT4 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT4 overcurrent recovery OFF time=600 us |
| OUT5_TOCR | 17:16 | rwh | **OUT5 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT5 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT5 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT5 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT5 overcurrent recovery ON time=48 us |
| OUT5_TOCR_OFF | 19:18 | rwh | **OUT5 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT5 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT5 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT5 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT5 overcurrent recovery OFF time=600 us |
| OUT6_TOCR | 21:20 | rwh | **OUT6 overcurrent recovery ON time**<br>$00_B$ **Setting1**: OUT6 overcurrent recovery ON time=0 us(default)<br>$01_B$ **Setting2**: OUT6 overcurrent recovery ON time=24 us<br>$10_B$ **Setting3**: OUT6 overcurrent recovery ON time=32 us<br>$11_B$ **Setting4**: OUT6 overcurrent recovery ON time=48 us |
| OUT6_TOCR_OFF | 23:22 | rwh | **OUT6 overcurrent recovery OFF time**<br>$00_B$ **Setting1**: OUT6 overcurrent recovery OFF time=200 us(default)<br>$01_B$ **Setting2**: OUT6 overcurrent recovery OFF time=300 us<br>$10_B$ **Setting3**: OUT6 overcurrent recovery OFF time=400 us<br>$11_B$ **Setting4**: OUT6 overcurrent recovery OFF time=600 us |

**Table 8 Reset values of** GENCTRL6

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX00 $0000_H$ | |
| Soft_reset | –-00 $0000_H$ | Reset the regs when enter FS |

## 7.8 Data control register 7

**GENCTRL7** Offset address: $07_H$

Data control register 7 Reset values see: Table 9

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | WDUNLOCK | VDS_BLK | VDSMON | | | | PWM6PHSH | |
| r | | | | | | | | rwh | rwh | rwh | | | | rwh | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWM6PHSH | PWM5PHSH | | | PWM4PHSH | | | PWM3PHSH | | | PWM2PHSH | | | PWM1PHSH | | |
| rwh | rwh | | | rwh | | | rwh | | | rwh | | | rwh | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| PWM1PHSH | 2:0 | rwh | **PWM1 generator phase shift**<br>$000_B$ **Setting1**: PWM1 generator phase shift =0 deg.(default)<br>$001_B$ **Setting2**: PWM1 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM1 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM1 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM1 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM1 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM1 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM1 generator phase shift=315 deg. |
| PWM2PHSH | 5:3 | rwh | **PWM2 generator phase shift**<br>$000_B$ **Setting1**: PWM2 generator phase shift=0 deg.(default)<br>$001_B$ **Setting2**: PWM2 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM2 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM2 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM2 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM2 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM2 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM2 generator phase shift=315 deg. |
| PWM3PHSH | 8:6 | rwh | **PWM3 generator phase shift**<br>$000_B$ **Setting1**: PWM3 generator phase shift=0 deg.(default)<br>$001_B$ **Setting2**: PWM3 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM3 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM3 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM3 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM3 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM3 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM3 generator phase shift=315 deg. |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| PWM4PHSH | 11:9 | rwh | **PWM4 generator phase shift**<br>$000_B$ **Setting1**: PWM4 generator phase shift=0 deg.(default)<br>$001_B$ **Setting2**: PWM4 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM4 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM4 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM4 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM4 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM4 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM4 generator phase shift=315 deg. |
| PWM5PHSH | 14:12 | rwh | **PWM5 generator phase shift**<br>$000_B$ **Setting1**: PWM5 generator phase shift=0 deg.(default)<br>$001_B$ **Setting2**: PWM5 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM5 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM5 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM5 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM5 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM5 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM5 generator phase shift=315 deg. |
| PWM6PHSH | 17:15 | rwh | **PWM6 generator phase shift**<br>$000_B$ **Setting1**: PWM6 generator phase shift=0 deg.(default)<br>$001_B$ **Setting2**: PWM6 generator phase shift=45 deg.<br>$010_B$ **Setting3**: PWM6 generator phase shift=90 deg.<br>$011_B$ **Setting4**: PWM6 generator phase shift=135 deg.<br>$100_B$ **Setting5**: PWM6 generator phase shift=180 deg.<br>$101_B$ **Setting6**: PWM6 generator phase shift=225 deg.<br>$110_B$ **Setting7**: PWM6 generator phase shift=270 deg.<br>$111_B$ **Setting8**: PWM6 generator phase shift=315 deg. |
| VDSMON | 21:18 | rwh | **Drain-source overvoltage threshold**<br>$0_H$ **Setting1**: VDSOV_TH=0.1 V<br>$1_H$ **Setting2**: VDSOV_TH=0.15 V<br>$2_H$ **Setting3**: VDSOV_TH=0.2 V(default)<br>$3_H$ **Setting4**: VDSOV_TH=0.25 V<br>$4_H$ **Setting5**: VDSOV_TH=0.3 V<br>$5_H$ **Setting6**: VDSOV_TH=0.35 V<br>$6_H$ **Setting7**: VDSOV_TH=0.4 V<br>$7_H$ **Setting8**: VDSOV_TH=0.5 V<br>$8_H$ **Setting9**: VDSOV_TH=2 V<br>$9_H$ **Setting10**: VDSOV_TH=0.2 V<br>…<br>$F_H$ **Setting16**: VDSOV_TH=0.2 V |
| VDS_BLK | 22 | rwh | **VDS monitoring blank time**<br>$0_B$ **Setting1**: tVDS_BLK/tVDS_BLK_OFF=8 us /37 us(default)<br>$1_B$ **Setting2**: tVDS_BLK/tVDS_BLK_OFF=50 us / 124 us |

(table continues...)

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| WDUNLOCK | 23 | rwh | **Watchdog unlock bit**<br>$0_B$ **Setting1**: 0b - watchdog functionality is locked(default)<br>$1_B$ **Setting2**: 1b- watchdog functionality is unlocked |

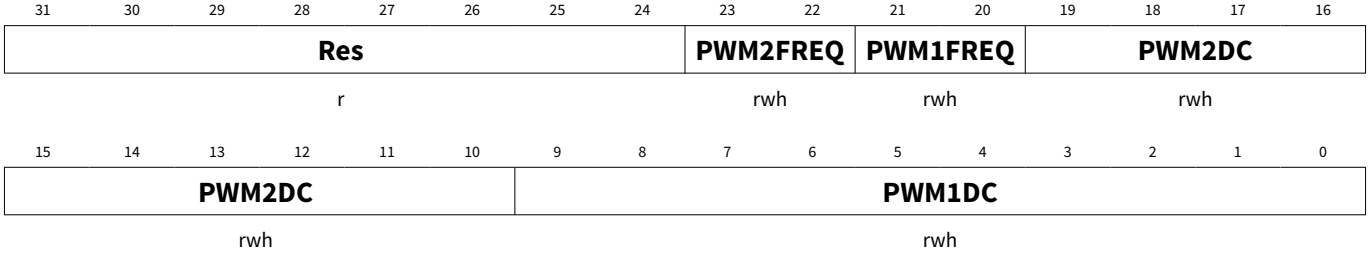
**Table 9 Reset values of** GENCTRL7

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX08 $0000_H$ | |
| Soft_reset | –-08 $0000_H$ | Reset the regs when enter FS |
| Soft_reset_s9144 | –-00 $0000_H$ | Reset the chip for s9144 variant |

## 7.9 Data control register 8

**GENCTRL8** Offset address: $08_H$

Data control register 8 Reset values see: Table 10




| Field | Bits | Type | Description |
|---|---|---|---|
| PWM1DC | 9:0 | rwh | **PWM channel 1 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 1 duty cycle =0 %(default)<br>$3FF_H$ **Setting1024**: PWM channel 1 duty cycle =100 % |
| PWM2DC | 19:10 | rwh | **PWM channel 2 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 2 duty cycle =0 %(default)<br>$3FF_H$ **Setting1024**: PWM channel 2 duty cycle =100 % |
| PWM1FREQ | 21:20 | rwh | **PWM channel 1 frequency**<br>$00_B$ **Setting1**: PWM channel 1 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 1 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 1 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 1 frequency=400 Hz |
| PWM2FREQ | 23:22 | rwh | **PWM channel 2 frequency**<br>$00_B$ **Setting1**: PWM channel 2 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 2 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 2 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 2 frequency=400 Hz |

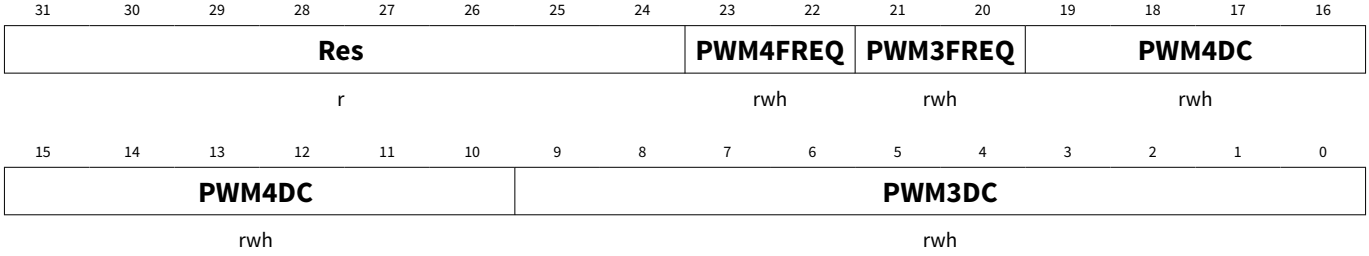
**Table 10 Reset values of GENCTRL8**

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX00 $0000_H$ | |
| Soft_reset | ––00 $0000_H$ | Reset the regs when enter FS |

## 7.10 Data control register 9

**GENCTRL9** Offset address: $09_H$

Data control register 9 Reset values see: Table 11




| Field | Bits | Type | Description |
|---|---|---|---|
| PWM3DC | 9:0 | rwh | **PWM channel 3 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 3 duty cycle=0 % (default)<br>$3FF_H$ **Setting1024**: PWM channel 3 duty cycle=100 % |
| PWM4DC | 19:10 | rwh | **PWM channel 4 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 4 duty cycle=0 %(default)<br>$3FF_H$ **Setting1024**: PWM channel 4 duty cycle=100 % |
| PWM3FREQ | 21:20 | rwh | **PWM channel 3 frequency**<br>$00_B$ **Setting1**: PWM channel 3 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 3 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 3 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 3 frequency=400 Hz |
| PWM4FREQ | 23:22 | rwh | **PWM channel 4 frequency**<br>$00_B$ **Setting1**: PWM channel 4 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 4 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 4 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 4 frequency=400 Hz |

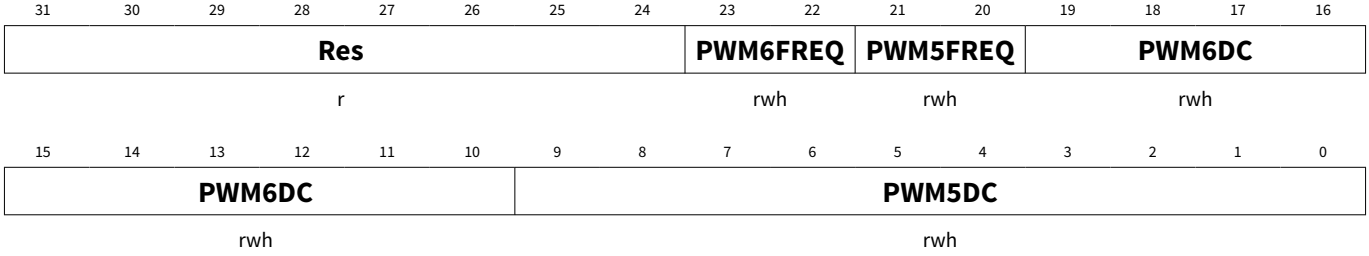
**Table 11 Reset values of** GENCTRL9

| Reset type | Reset value | Note |
|---|---|---|
| Reset | XX00 $0000_H$ | |
| Soft_reset | ––00 $0000_H$ | Reset the regs when enter FS |

## 7.11 Data control register 10

**GENCTRL10** Offset address: $0A_H$

Data control register 10 Reset values see: Table 12




| Field | Bits | Type | Description |
|---|---|---|---|
| PWM5DC | 9:0 | rwh | **PWM channel 5 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 5 duty cycle=0 % (default)<br>$3FF_H$ **Setting1024**: PWM channel 5 duty cycle=100 % |
| PWM6DC | 19:10 | rwh | **PWM channel 6 duty cycle = (Dec[xx xxxx xxxx]/1023)*100%**<br>$000_H$ **Setting1**: PWM channel 6 duty cycle=0 % (default)<br>$3FF_H$ **Setting1024**: PWM channel 6 duty cycle=100 % |
| PWM5FREQ | 21:20 | rwh | **PWM channel 5 frequency**<br>$00_B$ **Setting1**: PWM channel 5 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 5 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 5 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 5 frequency=400 Hz |
| PWM6FREQ | 23:22 | rwh | **PWM channel 6 frequency**<br>$00_B$ **Setting1**: PWM channel 6 frequency=100 Hz(default)<br>$01_B$ **Setting2**: PWM channel 6 frequency=200 Hz<br>$10_B$ **Setting3**: PWM channel 6 frequency=320 Hz<br>$11_B$ **Setting4**: PWM channel 6 frequency=400 Hz |

**Table 12 Reset values of GENCTRL10**

| Reset type | Reset value | Note |
|---|---|---|
| Reset | $XX00\ 0000_H$ | |
| Soft_reset | $--00\ 0000_H$ | |

## 7.12 General status register 1

**GENSTAT1** Offset address: $0B_H$

General status register 1 Reset value: $XXXX\ XXXX_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | HBE | VCC2_SC_VS | VCC2_SC_GND | OUT7_SC | OUT6HS_SC | OUT6LS_SC | OUT5HS_SC | OUT5LS_SC |
| r | | | | | | | | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUT4HS_SC | OUT4LS_SC | OUT3HS_SC | OUT3LS_SC | OUT2HS_SC | OUT2LS_SC | OUT1HS_SC | OUT1LS_SC | WDMON | | CPUV | VSUV | VSOV | ECVUV | ECVOV | SHST |
| rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rw | | rwh | rwh | rwh | rwh | rwh | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| SHST | 0 | rw | **SH level status bit**<br>$0_B$ **Setting1**: SHST=0b ( VS - VSH > VDSOV_TH)<br>$1_B$ **Setting2**: SHST=1b ( VS - VSH < VDSOV_TH) |
| ECVOV | 1 | rwh | **ECV overvoltage**<br>$0_B$ **Setting1**: ECVOV=0b -No ECV overvoltage detected<br>$1_B$ **Setting2**: ECVOV=1b -ECV overvoltage detected |
| ECVUV | 2 | rwh | **ECV undervoltage**<br>$0_B$ **Setting1**: ECVUV=0b -No ECV undervoltage detected<br>$1_B$ **Setting2**: ECVOV=1b -ECV undervoltage detected |
| VSOV | 3 | rwh | **VS overvoltage**<br>$0_B$ **Setting1**: VSOV=0b -No VS overvoltage detected<br>$1_B$ **Setting2**: VSOV=1b -VS ovevoltage detected |
| VSUV | 4 | rwh | **VS undervoltage**<br>$0_B$ **Setting1**: VSUV=0b -No VS undervoltage detected<br>$1_B$ **Setting2**: VSUV=1b -VS undervoltage detected |
| CPUV | 5 | rwh | **Charge pump undervoltage**<br>$0_B$ **Setting1**: CPUV=0b -No CP undervoltage detected<br>$1_B$ **Setting2**: CPUV=1b -CP undervoltage detected |
| WDMON | 7:6 | rw | **Watchdog timer monitoring**<br>$00_B$ **Setting1**: WDMON=00b - WD timer is between [0%; 25%] of tWDPER<br>$01_B$ **Setting2**: WDMON=01b - WD timer is between [25%; 50%] of tWDPER<br>$10_B$ **Setting3**: WDMON=10b - WD timer is between [50%; 75%] of tWDPER<br>$11_B$ **Setting4**: WDMON=11b - WD timer is between [75%; 100%] of tWDPER |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1LS_SC | 8 | rwh | **OUT1 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT1LS_SC=0b - no short circuit detected<br>$1_B$ **Setting2**: OUT1LS_SC=1b -short circuit detected |
| OUT1HS_SC | 9 | rwh | **OUT1 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT1HS_SC=0b -no short circuit detected<br>$1_B$ **Setting2**: OUT1HS_SC=1b -short circuit detected |
| OUT2LS_SC | 10 | rwh | **OUT2 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT2LS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT2LS_SC=1b -short circuit detected |
| OUT2HS_SC | 11 | rwh | **OUT2 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT2HS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT2HS_SC=1b -short circuit detected |
| OUT3LS_SC | 12 | rwh | **OUT3 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT3LS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT3LS_SC=1b -short circuit detected |
| OUT3HS_SC | 13 | rwh | **OUT3 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT3HS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT3HS_SC=1b -No short circuit detected |
| OUT4LS_SC | 14 | rwh | **OUT4 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT4LS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT4LS_SC=1b -short circuit detected |
| OUT4HS_SC | 15 | rwh | **OUT4 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT4HS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT4HS_SC=1b -short circuit detected |
| OUT5LS_SC | 16 | rwh | **OUT5 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT5LS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT5LS_SC=1b -short circuit detected |
| OUT5HS_SC | 17 | rwh | **OUT5 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT5HS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT5HS_SC=1b -short circuit detected |
| OUT6LS_SC | 18 | rwh | **OUT6 low-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT6LS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT6LS_SC=1b -short circuit detected |
| OUT6HS_SC | 19 | rwh | **OUT6 high-side short circuit status when OCR function is enabled**<br>$0_B$ **Setting1**: OUT6HS_SC=0b -No short circuit detected<br>$1_B$ **Setting2**: OUT6HS_SC=1b -short circuit detected |
| OUT7_SC | 20 | rwh | **OUT7 short circuit status- valid only when OUT7 is selected in low RDSON mode and the OCR function is enabled**<br>$0_B$ **Setting1**: OUT7_SC=0b -no short circuit detected<br>$1_B$ **Setting2**: OUT7_SC=1b -short circuit detected |

(table continues...)

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| VCC2_SC_GND | 21 | rwh | **VCC2 short-circuit to GND**<br>$0_B$ **Setting1**: VCC2_SC_GND =0b -No VCC2 short-circuit to GND detected<br>$1_B$ **Setting2**: VCC2_SC_GND =1b -VCC2 short-circuit to GND detected |
| VCC2_SC_VS | 22 | rwh | **VCC2 short-circuit to VS**<br>$0_B$ **Setting1**: VCC2_SC_VS =0b -No VCC2 short-circuit to VS detected<br>$1_B$ **Setting2**: VCC2_SC_VS =1b -VCC2 short-circuit to VS detected |
| HBE | 23 | rwh | **Input error status bit valid for the half-brige configuration if the enable bits of OUT10 and of ECV low-side are both set**<br>$0_B$ **Setting1**: HBE =0b -No half-bridge configuration error between ECV LS and OUT10<br>$1_B$ **Setting2**: HBE =1b -half-bridge configuration error between ECV LS and OUT10 |

## 7.13 General status register 2

**GENSTAT2** Offset address: $0C_H$

General status register 2 Reset value: $XXXX\ XXXX_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Res** | | | | | | | | **RES** | | | | **PAIRE** | **ECVLS_OL** | **OUT12_OL** | **OUT11_OL** |
| r | | | | | | | | r | | | | rwh | rwh | rwh | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OUT10_OL** | **OUT9_OL** | **OUT8_OL** | **OUT7_OL** | **OUT6HS_OL** | **OUT6LS_OL** | **OUT5HS_OL** | **OUT5LS_OL** | **OUT4HS_OL** | **OUT4LS_OL** | **OUT3HS_OL** | **OUT3LS_OL** | **OUT2HS_OL** | **OUT2LS_OL** | **OUT1HS_OL** | **OUT1LS_OL** |
| rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1LS_OL | 0 | rwh | **OUT1 low-side open load**<br>$0_B$ **Setting1**: OUT1LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT1LS_OL=1b -Open load detected |
| OUT1HS_OL | 1 | rwh | **OUT1 high-side open load**<br>$0_B$ **Setting1**: OUT1HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT1HS_OL=1b -Open load detected |
| OUT2LS_OL | 2 | rwh | **OUT2 low-side open load**<br>$0_B$ **Setting1**: OUT2LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT2LS_OL=1b -Open load detected |
| OUT2HS_OL | 3 | rwh | **OUT2 high-side open load**<br>$0_B$ **Setting1**: OUT2HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT2HS_OL=1b -Open load detected |
| OUT3LS_OL | 4 | rwh | **OUT3 low-side open load**<br>$0_B$ **Setting1**: OUT3LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT3LS_OL=1b -Open load detected |
| OUT3HS_OL | 5 | rwh | **OUT3 high-side open load**<br>$0_B$ **Setting1**: OUT3HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT3HS_OL=1b -Open load detected |
| OUT4LS_OL | 6 | rwh | **OUT4 low-side open load**<br>$0_B$ **Setting1**: OUT4LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT4LS_OL=1b -Open load detected |
| OUT4HS_OL | 7 | rwh | **OUT4 high-side open load**<br>$0_B$ **Setting1**: OUT4HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT4HS_OL=1b -Open load detected |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT5LS_OL | 8 | rwh | **OUT5 low-side open load**<br>$0_B$ **Setting1**: OUT5LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT5LS_OL=1b -Open load detected |
| OUT5HS_OL | 9 | rwh | **OUT5 high-side open load**<br>$0_B$ **Setting1**: OUT5HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT5HS_OL=1b -Open load detected |
| OUT6LS_OL | 10 | rwh | **OUT6 low-side open load**<br>$0_B$ **Setting1**: OUT6LS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT6LS_OL=1b -Open load detected |
| OUT6HS_OL | 11 | rwh | **OUT6 high-side open load**<br>$0_B$ **Setting1**: OUT6HS_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT6HS_OL=1b -Open load detected |
| OUT7_OL | 12 | rwh | **OUT7 open load**<br>$0_B$ **Setting1**: OUT7_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT7_OL=1b -Open load detected |
| OUT8_OL | 13 | rwh | **OUT8 open load**<br>$0_B$ **Setting1**: OUT8_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT8_OL=1b -Open load detected |
| OUT9_OL | 14 | rwh | **OUT9 open load**<br>$0_B$ **Setting1**: OUT9_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT9_OL=1b -Open load detected |
| OUT10_OL | 15 | rwh | **OUT10 open load**<br>$0_B$ **Setting1**: OUT10_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT10_OL=1b -Open load detected |
| OUT11_OL | 16 | rwh | **OUT11 open load**<br>$0_B$ **Setting1**: OUT11_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT11_OL=1b -Open load detected |
| OUT12_OL | 17 | rwh | **OUT12 open load**<br>$0_B$ **Setting1**: OUT12_OL=0b -No open load detected<br>$1_B$ **Setting2**: OUT12_OL=1b -Open load detected |
| ECVLS_OL | 18 | rwh | **ECV low-side open load**<br>$0_B$ **Setting1**: ECVLS_OL=0b -No open load detected<br>$1_B$ **Setting2**: ECVLS_OL=1b -Open load detected |
| PAIRE | 19 | rwh | **Pair error status bit shows a wrong configuration for pairing of OUT6(OUT6 paired with OUT1 and OUT5)**<br>$0_B$ **Setting1**: PAIRE=0b -No paired error detected<br>$1_B$ **Setting2**: PAIRE=1b - paired error detected |
| RES | 23:20 | r | **Reserved bit** |

## 7.14 General status register 3

**GENSTAT3** Offset address: $0D_H$

General status register 3 Reset value: $XXXX\ XXXX_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Res** | | | | | | | | **RES** | | | | **VDSOV** | **ECVLS_OC** | **OUT12_OC** | **OUT11_OC** |
| r | | | | | | | | r | | | | rwh | rwh | rwh | rwh |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OUT10_OC** | **OUT9_OC** | **OUT8_OC** | **OUT7_OC** | **OUT6HS_OC** | **OUT6LS_OC** | **OUT5HS_OC** | **OUT5LS_OC** | **OUT4HS_OC** | **OUT4LS_OC** | **OUT3HS_OC** | **OUT3LS_OC** | **OUT2HS_OC** | **OUT2LS_OC** | **OUT1HS_OC** | **OUT1LS_OC** |
| rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT1LS_OC | 0 | rwh | **OUT1 low-side overcurrent - valid**<br>$0_B$ **Setting1**: OUT1LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT1LS_OC=1b -Overcurrent detected |
| OUT1HS_OC | 1 | rwh | **OUT1 high-side overcurrent**<br>$0_B$ **Setting1**: OUT1HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT1HS_OC=1b -Overcurrent detected |
| OUT2LS_OC | 2 | rwh | **OUT2 low-side overcurrent**<br>$0_B$ **Setting1**: OUT2LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT2LS_OC=1b -Overcurrent detected |
| OUT2HS_OC | 3 | rwh | **OUT2 high-side overcurrent**<br>$0_B$ **Setting1**: OUT2HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT2HS_OC=1b -Overcurrent detected |
| OUT3LS_OC | 4 | rwh | **OUT3 low-side overcurrent**<br>$0_B$ **Setting1**: OUT3LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT3LS_OC=1b -Overcurrent detected |
| OUT3HS_OC | 5 | rwh | **OUT3 high-side overcurrent**<br>$0_B$ **Setting1**: OUT3HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT3HS_OC=1b -Overcurrent detected |
| OUT4LS_OC | 6 | rwh | **OUT4 low-side overcurrent**<br>$0_B$ **Setting1**: OUT4LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT4LS_OC=1b -Overcurrent detected |
| OUT4HS_OC | 7 | rwh | **OUT4 high-side overcurrent**<br>$0_B$ **Setting1**: OUT4HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT4HS_OC=1b -Overcurrent detected |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| OUT5LS_OC | 8 | rwh | **OUT5 low-side overcurrent**<br>$0_B$ **Setting1**: OUT5LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT5LS_OC=1b -Overcurrent detected |
| OUT5HS_OC | 9 | rwh | **OUT5 high-side overcurrent**<br>$0_B$ **Setting1**: OUT5HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT5HS_OC=1b -Overcurrent detected |
| OUT6LS_OC | 10 | rwh | **OUT6 low-side overcurrent**<br>$0_B$ **Setting1**: OUT6LS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT6LS_OC=1b -Overcurrent detected |
| OUT6HS_OC | 11 | rwh | **OUT6 high-side overcurrent**<br>$0_B$ **Setting1**: OUT6HS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT6HS_OC=1b -Overcurrent detected |
| OUT7_OC | 12 | rwh | **OUT7 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT7_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT7_OC=1b -Overcurrent detected |
| OUT8_OC | 13 | rwh | **OUT8 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT8_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT8_OC=1b -Overcurrent detected |
| OUT9_OC | 14 | rwh | **OUT9 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT9_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT9_OC=1b -Overcurrent detected |
| OUT10_OC | 15 | rwh | **OUT10 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT10_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT10_OC=1b -Overcurrent detected |
| OUT11_OC | 16 | rwh | **OUT11 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT11_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT11_OC=1b -Overcurrent detected |
| OUT12_OC | 17 | rwh | **OUT12 overcurrent in RDSON or CCM modes**<br>$0_B$ **Setting1**: OUT12_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: OUT12_OC=1b -Overcurrent detected |
| ECVLS_OC | 18 | rwh | **ECV low-side overcurrent**<br>$0_B$ **Setting1**: ECVLS_OC=0b -No overcurrent detected<br>$1_B$ **Setting2**: ECVLS_OC=1b -Overcurrent detected |
| VDSOV | 19 | rwh | **Heater drain-source overvoltage**<br>$0_B$ **Setting1**: VDSOV=0b- No drain-source overvoltage detected<br>$1_B$ **Setting2**: VDSOV=1b -Drain-source overvoltage detected |
| RES | 23:20 | r | **Reserved bit** |

## 7.15 General status register 4

**GENSTAT4** Offset address: $0E_H$

General status register 4 Reset value: $XXXX\ XXXX_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | RES | | | | | | | Res |
| r | | | | | | | | r | | | | | | | r |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | TSDC6 | TSDC5 | TSDC4 | TSDC3 | TSDC2 | TSDC1 | TWC6 | TWC5 | TWC4 | TWC3 | TWC2 | TWC1 |
| r | | | | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

| Field | Bits | Type | Description |
|---|---|---|---|
| TWC1 | 0 | rwh | **Thermal warning cluster 1**<br>$0_B$ **Setting1**: TWC1=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC1=1b -Thermal warning detected |
| TWC2 | 1 | rwh | **Thermal warning cluster 2**<br>$0_B$ **Setting1**: TWC2=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC2=1b -Thermal warning detected |
| TWC3 | 2 | rwh | **Thermal warning cluster 3**<br>$0_B$ **Setting1**: TWC3=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC3=1b -Thermal warning detected |
| TWC4 | 3 | rwh | **Thermal warning cluster 4**<br>$0_B$ **Setting1**: TWC4=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC4=1b -Thermal warning detected |
| TWC5 | 4 | rwh | **Thermal warning cluster 5**<br>$0_B$ **Setting1**: TWC5=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC5=1b -Thermal warning detected |
| TWC6 | 5 | rwh | **Thermal warning cluster 6**<br>$0_B$ **Setting1**: TWC6=0b -No thermal warning detected<br>$1_B$ **Setting2**: TWC6=1b -thermal warning detected |
| TSDC1 | 6 | rwh | **Thermal shutdown cluster 1**<br>$0_B$ **Setting1**: TSDC1=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC1=1b -thermal shutdown detected |
| TSDC2 | 7 | rwh | **Thermal shutdown cluster 2**<br>$0_B$ **Setting1**: TSDC2=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC2=1b -thermal shutdown detected |
| TSDC3 | 8 | rwh | **Thermal shutdown cluster 3**<br>$0_B$ **Setting1**: TSDC3=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC3=1b -thermal shutdown detected |

**(table continues...)**

(continued)

| Field | Bits | Type | Description |
|---|---|---|---|
| TSDC4 | 9 | rwh | **Thermal shutdown cluster 4**<br>$0_B$ **Setting1**: TSDC4=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC4=1b -thermal shutdown detected |
| TSDC5 | 10 | rwh | **Thermal shutdown cluster 5**<br>$0_B$ **Setting1**: TSDC5=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC5=1b -thermal shutdown detected |
| TSDC6 | 11 | rwh | **Thermal shutdown cluster 6**<br>$0_B$ **Setting1**: TSDC6=0b -No thermal shutdown detected<br>$1_B$ **Setting2**: TSDC6=1b -thermal shutdown detected |
| RES | 23:17 | r | **Reserved bit** |

# Revision history

| Revision | Date | Description of changes |
|---|---|---|
| Rev. 1.01 | 2025-02-17 | • Document confidentiality updated |
| Rev. 1.00 | 2024-09-12 | • Initial release |

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**Edition 2025-02-17**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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**Document reference**
**IFX-hwj1661951235055**

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