MCP+ SBC Family

User’s Guide

About this document

The intention of this User's Guide is to provide relevant design-in information for automotive applications with the Infineon MCP+ SBC family. The document is complementary to the datasheet.

Scope and purpose

This User’s Guide covers the following products of the MCP+ SBC device family (with/without CAN Partial Networking, with 5 V or 3.3 V main supply output):

- TLE9278BQX
- TLE9278BQXV33
- TLE9278-3BQX
- TLE9278-3BQXV33

Intended audience

This document is aimed at hardware engineers integrating devices of the MCP+ SBC family into their applications.

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1 Hardware configuration

1.1 Introduction and initial setup

The MCP+ SBC includes a dedicated pin (VIO) for externally supplying the internal digital I/O stages for communication with the µC as well as for supervision purposes. This is usually done using VCC1 or VEXT. It also includes the PCFG pin for storing the VIO supply voltage level during power-up. The configuration is stored for all conditions and can be changed only by powering down ($V_S < V_{POR,f}$) and restarting the device. Depending on the configuration, supervision functions refer to VCC1 or VEXT.

VIO must not be larger than VCC1.

The available configuration options and the device behavior they cause are shown in ***Table 1*** on page 4. Configurations not listed are unsupported.

Table 1 Supply and power-up configurability

VCC1 output voltage	PCFG pin	VIO supply	µC supply	VEXT output voltage	VEXT behavior	Supervision functions
3.3V	Open	VCC1	VCC1	Configurable via SPI using VEXT_VCFG	Configurable via SPI, OFF after power-up	Supervision functions of VIO with 3.3V level, VREG_UV SPI status bit active
3.3V	GND	VCC1	VCC1	Configurable via SPI using VEXT_VCFG	Configurable via SPI, OFF after power-up	Supervision functions of VIO with 3.3V level, VREG_UV SPI status bit active
5V	Open	VCC1	VCC1	Configurable via SPI using VEXT_VCFG	Configurable via SPI, OFF after power-up	Supervision functions of VIO with 5V level, VREG_UV SPI status bit active
5V	GND	VEXT	VEXT	VEXT=3.3V (fixed)	Follow VCC1 (ON at power-up, SBC normal, stop, sleep, fail-safe mode)	Supervision functions of VIO with 3.3V level, VREG_UV SPI status bit not active and rerouted to VCC1

The response to a watchdog trigger failure or VIO overvoltage can be configured for four different cases. They are selected using the INTN pin and the CFG2 bit in the HW_CTRL_0 SPI register:

- A watchdog trigger failure enters the SBC Restart Mode (configurations 1 and 3). Depending on the setting of CFG2, the Fail Output (FO) is activated after the first or the second watchdog trigger failure. If VIO_OV_RST is set in configurations 1 or 3, VIO_OV enters the SBC Restart Mode and activates FO.
- A watchdog trigger failure enters the SBC Fail-Safe Mode (configurations 2 and 4). Depending on the setting of CFG2, the Fail Output (FO) is activated after the first or the second watchdog trigger failure. The first watchdog trigger failure in configuration 4 enters the SBC Restart Mode. If VIO_OV_RST is set in configurations 2 or 4 , VIO_OV enters the SBC Fail-Safe Mode and activates FO.

The device configuration can be identified by reading the CFG2_STATE and CFG1_STATE bits in the WK_LVL_STAT SPI register.

Table 2 Watchdog trigger failure configuration

Config.	Event	FO activation	SBC mode entered	CFG2 setting	INTN pin (CFG1_STATE)
1	One watchdog failure	After first WD failure	SBC Restart Mode	1	External pull-up (HIGH)
2	One watchdog failure	After first WD failure	SBC Fail-Safe Mode	1	No external pull-up (LOW)
3	Two watchdog failures	After second WD failure	SBC Restart Mode	0	External pull-up (HIGH)
4	Two watchdog failures	After second WD failure	SBC Fail-Safe Mode	0	No external pull-up (LOW)

Table 3 SBC configuration

Config.	Description	FO/TEST pin	INTN pin (CFG1_STATE)	CFG2_STATE	CFG2_STATE
0	Software development mode: Watchdog trigger failures do not trigger a reset. After power-up one arbitrary SPI command must be sent.	0	-	X	X
1	If the WD trigger is missed for the first time, V_{CC1} remains unchanged, the FO pin is activated (HIGH), SBC Restart Mode is entered.	Open or > $V_{Test,H}$	External pull-up to V_{IO}	1	1
2	If the WD trigger is missed for the first time, V_{CC1} turns off, the FO pin is activated (HIGH), SBC Fail-Safe Mode is entered.	Open or > $V_{Test,H}$	Open or GND	1	0
3	If the WD trigger is missed for the second time, V_{CC1} remains unchanged, the FO pin is activated (HIGH), SBC Restart Mode is entered.	Open or > $V_{Test,H}$	External pull-up to V_{IO}	0	1
4	If the WD trigger is missed for the second time, V_{CC1} turns off, the FO pin is activated (HIGH), SBC Fail-Safe Mode is entered.	Open or > $V_{Test,H}$	Open or GND	0	0

See also ***Chapter 1.3.1*** on page 9.
See also ***Chapter 1.3.2*** on page 10.

1.2 Pin structures

Table 4 Pin overview

Pin	Symbol	Input / output structure
1	CANH0	CAN0 high bus pin. High-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
2	CANL0	CAN0 low bus pin. Low-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
3	GND	CAN0 and CAN1 common ground.
4	CANL1	CAN1 low bus pin. Low-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
5	CANH1	CAN1 high bus pin. High-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
6	GND	Analog ground.
7	CANH2	CAN2 high bus pin. High-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
8	CANL2	CAN2 low bus pin. Low-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
9	GND	CAN2 and CAN3 common ground.
10	CANL3	CAN3 low bus pin. Low-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
11	CANH3	CAN3 high bus pin. High-side switch with biasing and termination according to ISO 11898-2. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
12	PCFG	Configuration pin. For power-up hardware configuration (see ***Introduction and initial setup***). 5 kΩ pull-up to internal 5 V during POR and SBC Init Mode.
13	TXDCAN0	Transmit CAN0. Permanent 40 kΩ pull-up to VCC1. Not influenced by register settings. (See also P_8.3.28 in the TLE9278BQX data sheet.)
14	RXDCAN0	Receive CAN0. Push-pull output stage. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
15	TXDCAN1	Transmit CAN1. Permanent 40 kΩ pull-up to VCC1. Not influenced by register settings. (See also P_8.3.28 in the TLE9278BQX data sheet.)
16	RXDCAN1	Receive CAN1. Push-pull output stage. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
17	TXDCAN2	Transmit CAN2. Permanent 40 kΩ pull-up to VCC1. Not influenced by register settings. (See also P_8.3.28 in the TLE9278BQX data sheet.)
18	RXDCAN2	Receive CAN2. Push-pull output stage. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)
19	VCAN	Power supply input for internal HS-CAN modules
20	TXDCAN3	Transmit CAN3. Permanent 40 kΩ pull-up to VCC1. Not influenced by register settings. (See also P_8.3.28 in the TLE9278BQX data sheet.)
21	RXDCAN3	Receive CAN3. Push-pull output stage. (See also the block diagram in chapter 8.1 of the TLE9278BQX data sheet.)

Table 4 Pin overview (continued)

Pin	Symbol	Input / output structure
22	VCC1	Buck voltage regulator feedback input. Connect to the buck regulator output voltage. Pull-down structure to prevent a floating output voltage if VCC1 is in SBC Sleep Mode or Fail-Safe Mode.
23	VIO	I/O voltage supply. Reference voltage for over- and undervoltage monitoring (see ***Introduction and initial setup***). I/O structure supply input.
24	RSTN	Reset output. Active LOW, internal pull-up. 20 kΩ pull-up to VCC1, open-drain output stage. Not influenced by register settings.
25	INTN	Interrupt output. Active LOW. 250 kΩ pull-down to GND during reset delay time and SBC Init Mode, push-pull output stage afterwards. Not influenced by register settings.
26	GND	Buck regulator ground.
27	BCKSW	Buck regulator switch node output. Push-pull output stage. (See also chapter 8.1 of the TLE9278BQX data sheet.)
28	n.c.	Not connected (not bonded internally)
29	VS	Buck regulator supply voltage. Connected to battery voltage or boost output voltage with reverse protection diode. If the boost is not used, use a filter for improved EMC. Device supply input and sensing structure for boost output voltage.
30	VS	Buck regulator supply voltage. Connected to battery voltage or boost output voltage with reverse protection diode. If the boost is not used, use a filter for improved EMC. Device supply input and sensing structure for boost output voltage.
31	n.c.	Not connected (not bonded internally)
32	GND	Boost regulator ground.
33	GND	Boost regulator ground.
34	n.c.	Not connected (not bonded internally)
35	BSTD	Boost transistor drain. Connected between inductor and diode for boost functionality. If the boost regulator is not used, connect to ground. Low-side switch in open-drain configuration.
36	BSTD	Boost transistor drain. Connected between inductor and diode for boost functionality. If the boost regulator is not used, connect to ground. Low-side switch in open-drain configuration.
37	CSN	SPI chip select input. Permanent 40 kΩ pull-up to VCC1. Not influenced by register settings.
38	SDO	SPI data output. Out of SBC (=MISO). Push-pull output stage. Not influenced by register settings.
39	SDI	SPI data input. Into SBC (=MOSI). Permanent 40 kΩ pull-down to VCC1. Not influenced by register settings.
40	CLK	SPI clock input. Permanent 40 kΩ pull-down to VCC1. Not influenced by register settings.
41	GND	Common digital ground.
42	WK	Wake input. High-ohmic after POR; configurable type. 10 µA pull-up/pull-down to internal 5 V or GND; configurable via SPI register WK_PUPD_CTRL.

Table 4 Pin overview (continued)

Pin	Symbol	Input / output structure
43	VBSENSE	Battery voltage monitoring input. 5 kΩ pull-up to VS to prevent unintended floating of VBSENSE.
44	VEXTIN	Input supply voltage for VEXT. Connected to battery voltage with reverse protection diode and filter for improved EMC. 150 kΩ base-to-emitter resistor integrated to VEXTB.
45	VEXTSH	Emitter connection of the external PNP; shunt connection to VEXTIN. 5 kΩ pull-up to VS to prevent an unintended floating of VEXTSH. Not influenced by register settings (antiparallel diodes between VS and VEXTSH).
46	VEXTB	Base connection of the external PNP. Pull-up structure to VS to prevent an unintended switch-on behavior of the external PNP in case of parasitic traces of the PNP base to GND.
47	VEXTREF	Collector connection of the external PNP; reference input. Pull-down structure to prevent a floating output voltage if VEXT is OFF; additional pull-down structure to be activated in case of 0 V to prevent damage.
48	FO/TEST	FO: Fail output. Active LOW, open drain. TEST: Connect to GND to activate SBC Software Development Mode. 5 kΩ pull-up to internal 5 V during POR and SBC Init Mode; low-side switch in open-drain configuration. Activation via error or via SPI bit FO_ON.
Cooling tab	GND	Exposed die pad. For cooling purposes only: Connect to the tab, but do not use as electrical ground. Noother internal structure.

1.3 Response on system failures

1.3.1 Watchdog trigger failure

The four different configurations (depending on the state of the INTN pin and the CFG2 bit setting) are described in ***Table 2*** on page 5. A watchdog trigger failure leads to either an SBC Restart of Fail-Safe Mode entry (after the first or after the second trigger failure). The Failure Output (FO) is activated.

The specific behavior is illustrated in the following timing diagrams.

1.3.1.1 Watchdog trigger failure, Config1

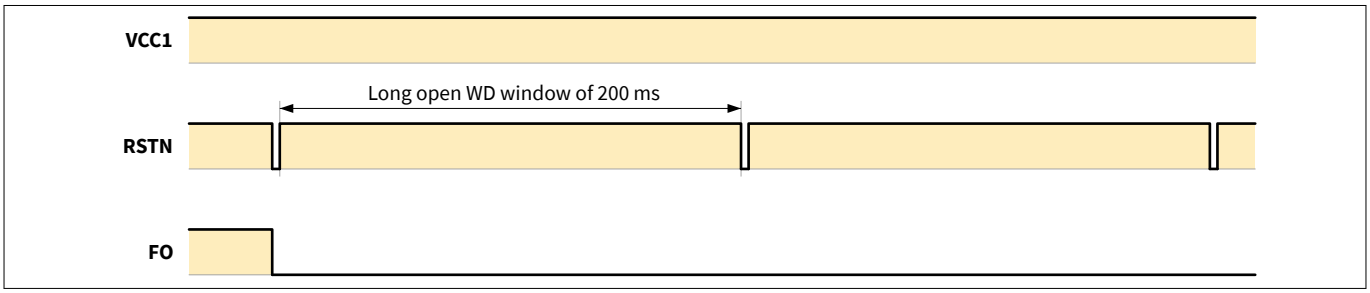


Figure 1 SBC Restart Mode entry and FOx activation after first watchdog trigger failure

1.3.1.2 Watchdog trigger failure, Config2

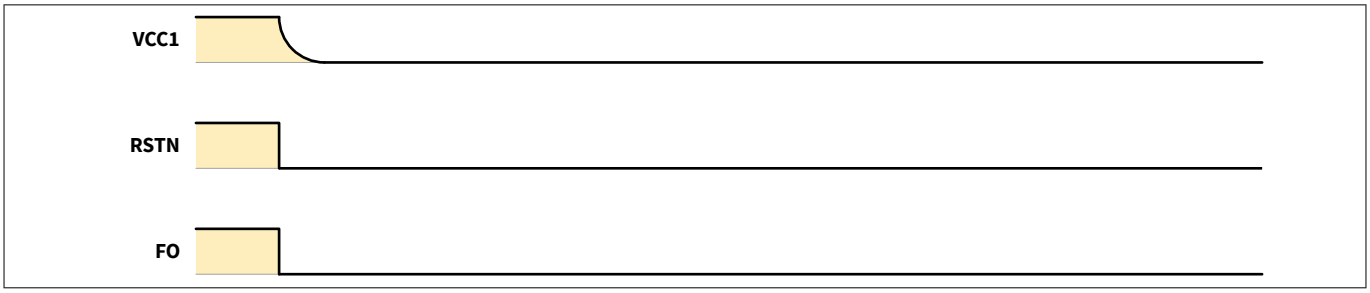


Figure 2 SBC Fail-Safe Mode entry and FOx activation after first watchdog trigger failure

1.3.1.3 Watchdog trigger failure, Config3

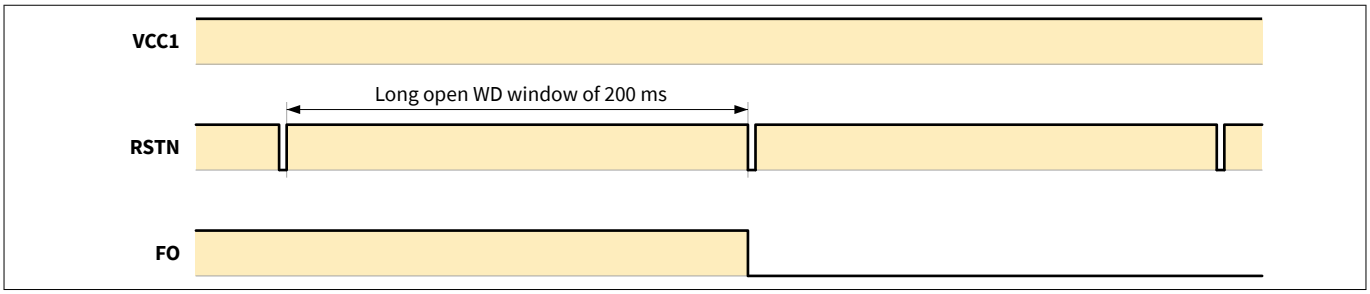


Figure 3 SBC Restart Mode entry due to watchdog failure and FO activation after second watchdog trigger failure

1.3.1.4 Watchdog trigger failure, Config4

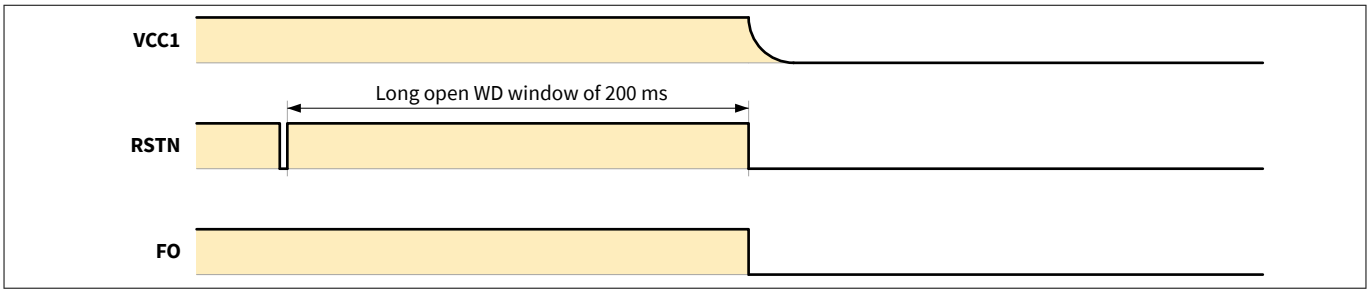


Figure 4 SBC Fail-Safe Mode entry and FOx activation after second watchdog trigger failure

1.3.2 Behavior in case of VIO overvoltage

The behavior in case of VIO overvoltage differs from the response on watchdog trigger failure (see ***Table 2*** on page 5).

Strategy of VIO overvoltage signalization:

- Level 1: SPI flag (VIO_OV) activation only.
- Level 2: SPI flag (VIO_OV) + Restart Mode entry (FO activation).
- Level 3: SPI flag (VIO_OV) + SBC Fail-Safe Mode entry (FO activation).

Selection via SPI bit VIO_OV_RST in register M_S_CTRL (default value after POR/Soft Reset/Restart = 0):

- If VIO_OV_RST = 0 (default), a VIO overvoltage condition is flagged with the SPI status bit VIO_OV (SUP_STAT_2).
- If VIO_OV_RST = 1, a VIO overvoltage condition sets the VIO_OV bit and in addition, depending on the hardware configuration, an additional action is triggered:
  - If CFG0_STATE = 1, the SBC Restart Mode is entered in case of VIO_OV.
    The fail output (FO) is activated if configured as fail output. VIO_OV_RST is cleared when the SBC enters the Restart Mode.
  - If CFG0_STATE = 0, the SBC Fail-Safe Mode is entered in case of VIO_OV.
    The fail output (FO) is activated if configured as fail output. A wake event is needed to exit the SBC Fail-Safe Mode. VIO_OV_RST is cleared when the SBC enters the Restart Mode.

1.3.2.1 VIO overvoltage, Config1/3

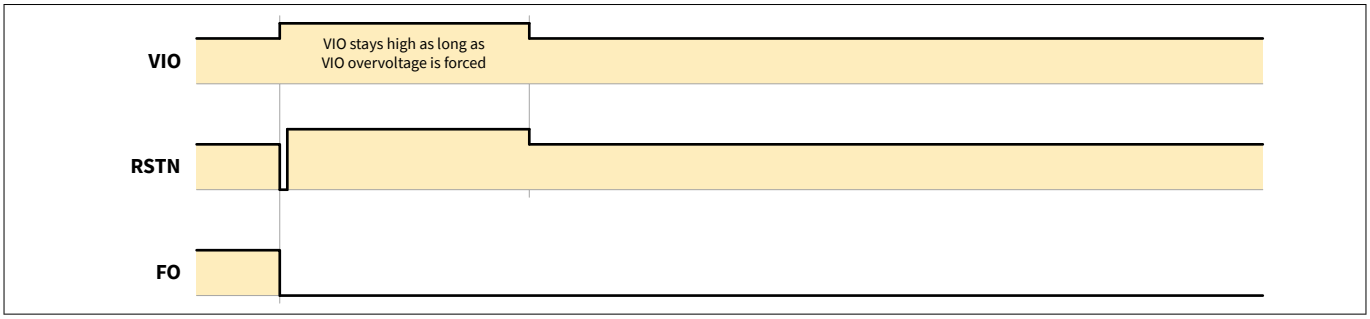


Figure 5 SBC Restart Mode entry due to VIO overvoltage

1.3.2.2 VIO overvoltage, Config2/4

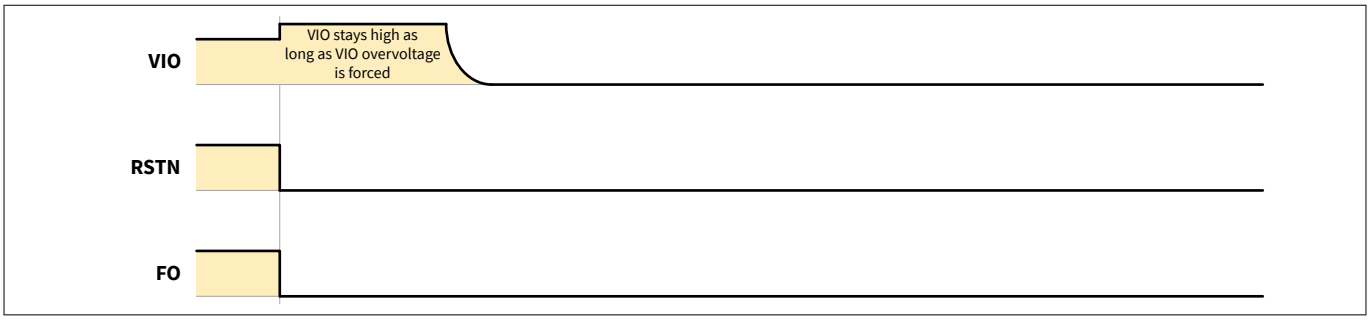


Figure 6 Fail-Safe mode entry due to VIO OV

1.3.2.3 VIO overvoltage and CFG=0 configuration

If the device has been triggered by a VIO overvoltage event in the CFG=0 configuration, it exits the SBC Restart Mode after a delay time, t_{RD1}, of typ. 10 ms. This time can be reduced to typ. 2 ms (t_{RD2}).

At the same time, VIO_OV_RST is automatically cleared. The device stays in SBC Normal Mode, even if the overvoltage condition is still present. Though, the VIO_OV bit remains set and must be cleared actively.

The SBC enters the Restart Mode again only if the VIO_OV_RST bit is set again.

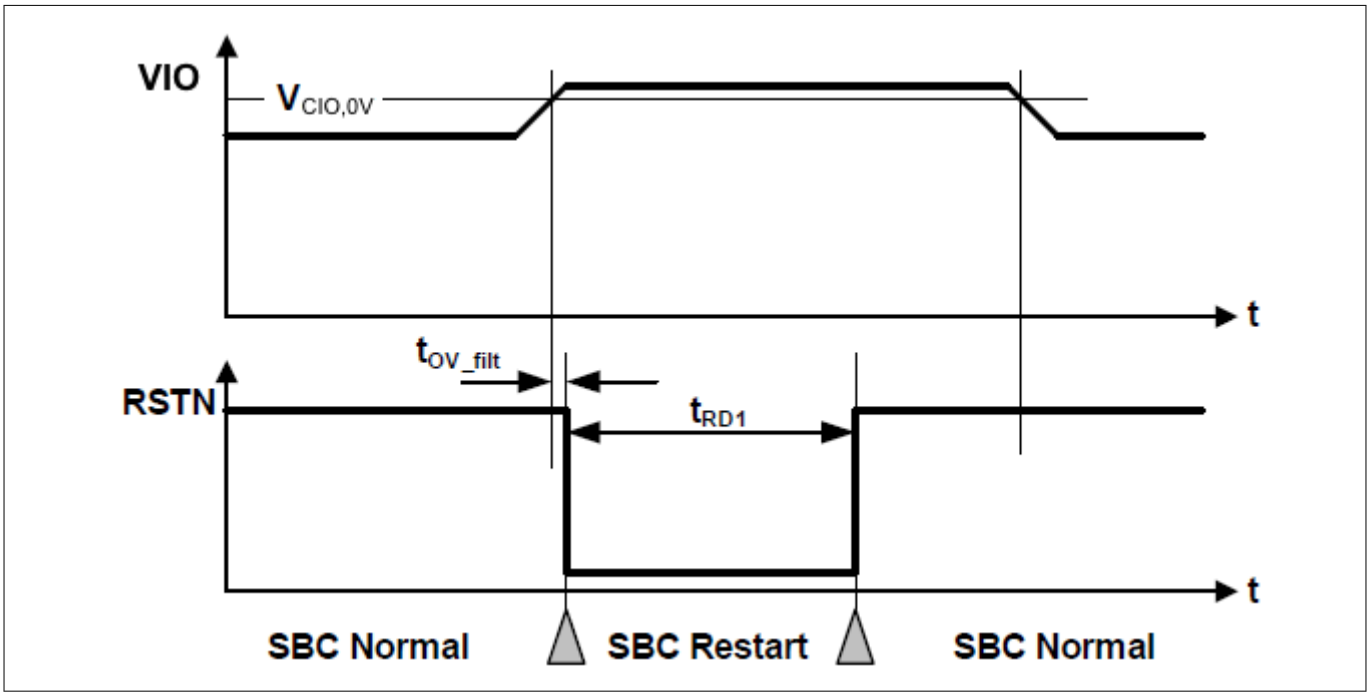


Figure 7 VIO Overvoltage Timing Diagram

This behavior differs from the undervoltage response, as shown below.

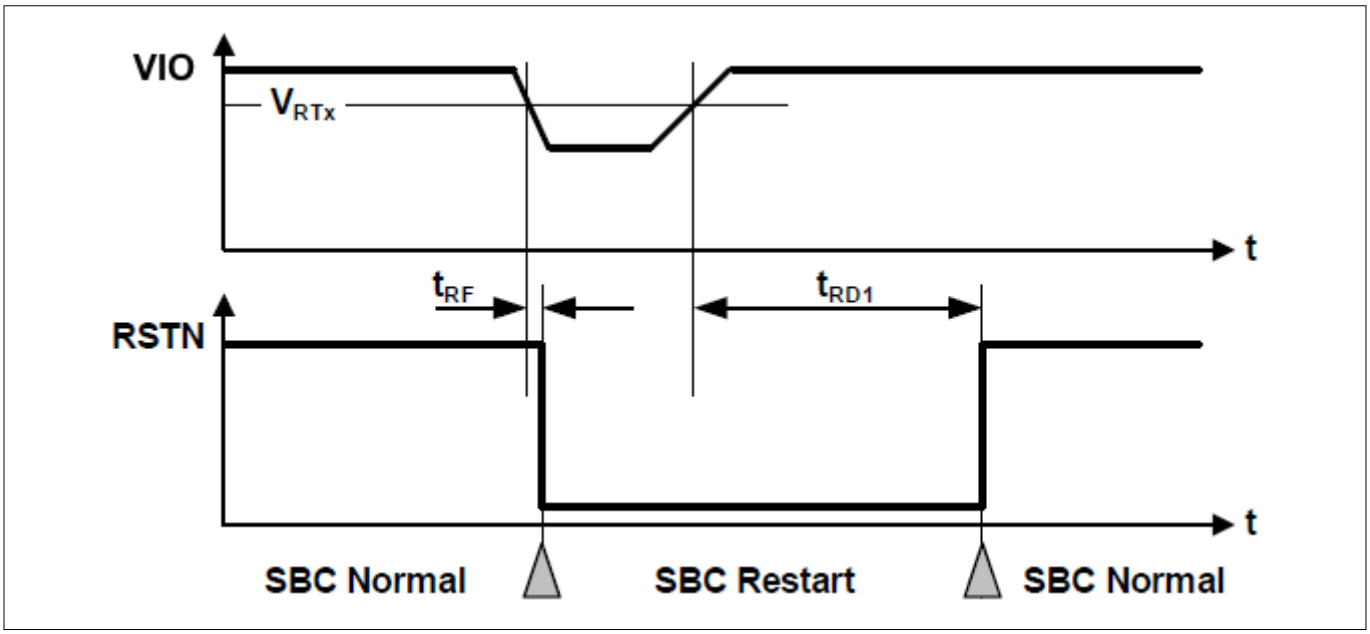


Figure 8 VIO Undervoltage Timing Diagram

1.4 Layout and BOM guidelines

1.4.1 Grounding concept, BOM proposal, and general layout recommendations

The power system of the TLE9278 is separated into multiple power domains:

- CAN power
- Boost regulator
- Buck regulator
- External PNP regulator
- Analog ground
- Digital ground

For proper grounding and good EMC behavior, dedicated power grounds for buck, boost, and CAN should be used.

In particular, these supplies are represented by switching events, causing high voltage and current slew rates in the system.

1.4.1.1 Grounding concept for the buck converter

We recommend using a dedicated ground domain for the buck converter. It connects the GND of the internal output power stage of the buck converter, the buck input bypass capacitor, and the buck output capacitors. This plane provides a low-impedance connection of all high-frequency current paths of the buck converter and connects them to the main GND plane with some VIAs.

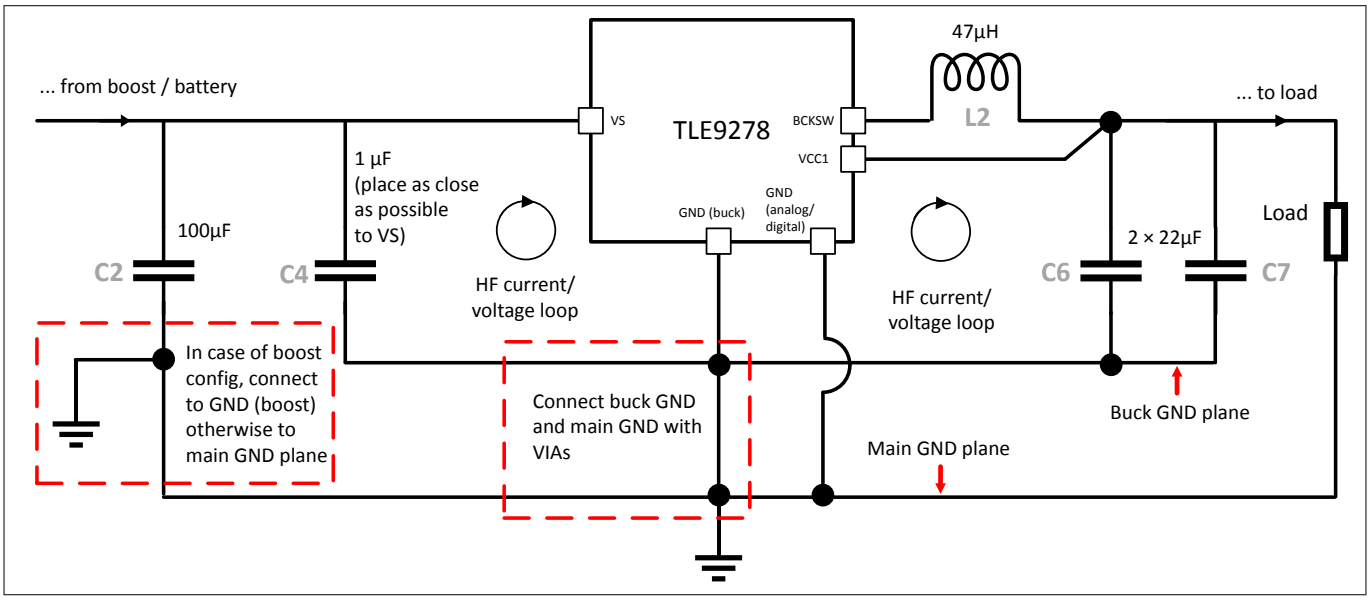


Figure 9 Grounding concept and BOM proposal for the VCC1 buck regulator

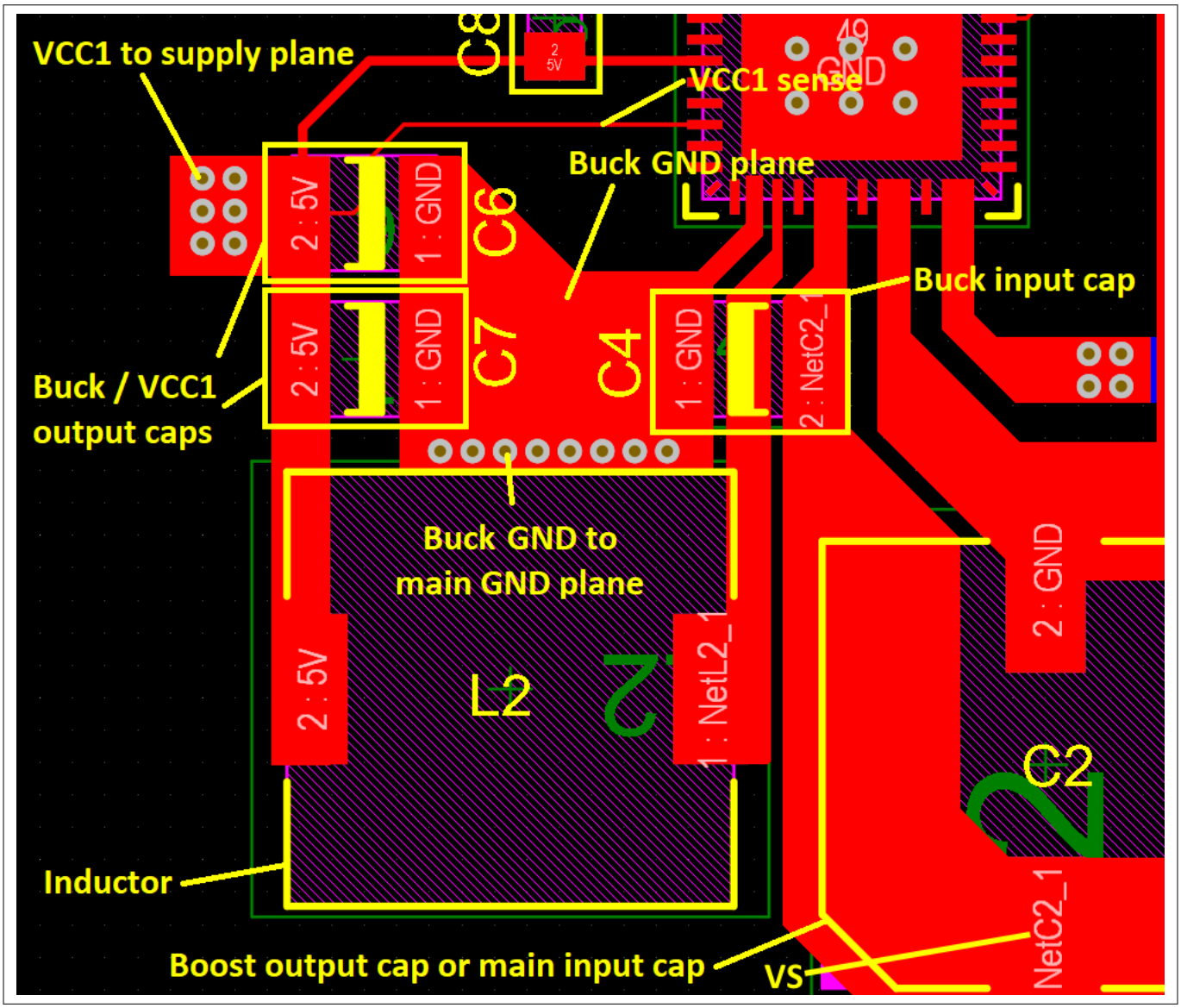


Figure 10 Recommended VCC1 buck converter layout

1.4.1.2 Grounding concept for the boost converter

The boost converter is handled in a similar way to the buck converter: A dedicated GND domain connects the GND of the boost low-side MOSFET with the boost input and output capacitors to provide low-impedance paths for alternating currents and voltages. The load is connected to GND connection to the load is provided using vias to the GND plane (see ***Figure 11***).

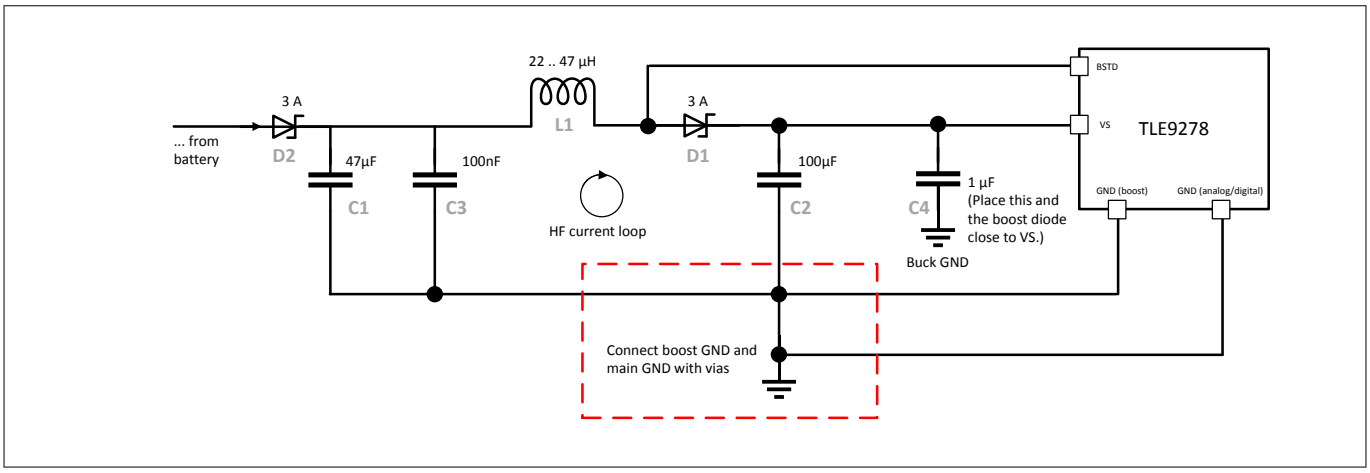


Figure 11 Grounding concept and BOM proposal for the boost converter

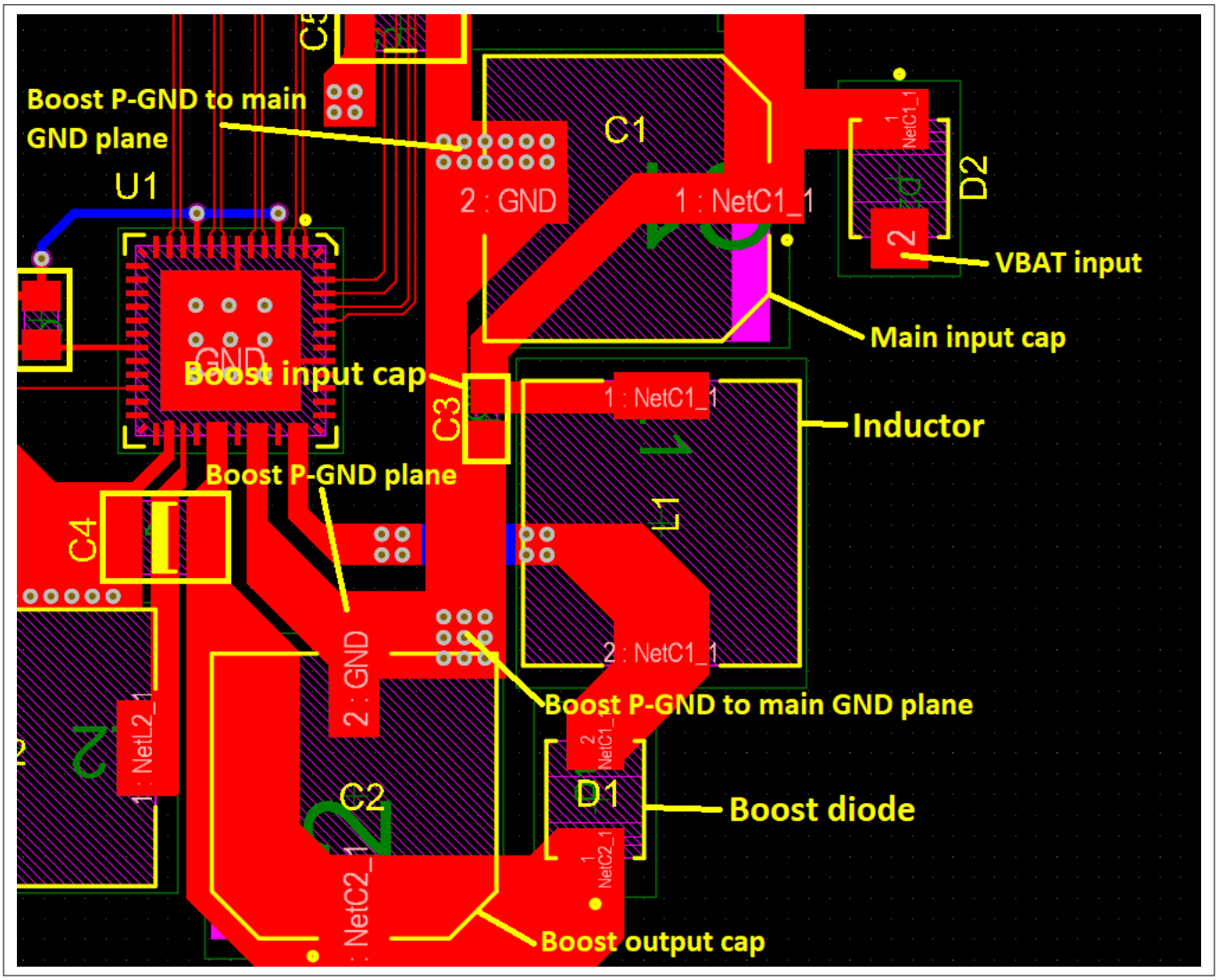


Figure 12 Recommended layout for the boost regulator converter

The area directly underneath the inductors must be kept free from signals that are not related to the switching signals inside the inductor, especially the GND planes. Otherwise, the inductor can inject switching noise into those signals, which creates bad EMC behavior.

1.4.1.3 Grounding concept for the CAN transceiver

The GND connection of the CAN transceiver should not be connected directly to the GNDs of either the buck or the boost converter. Otherwise, the switching noise of the DC/DC converter can be injected into the CAN lines or, conversely, the switching noise of the CAN transceiver into other GNDs and lead to emission problems.

We recommend connecting the CAN GND to the main GND plane, as shown in this example:

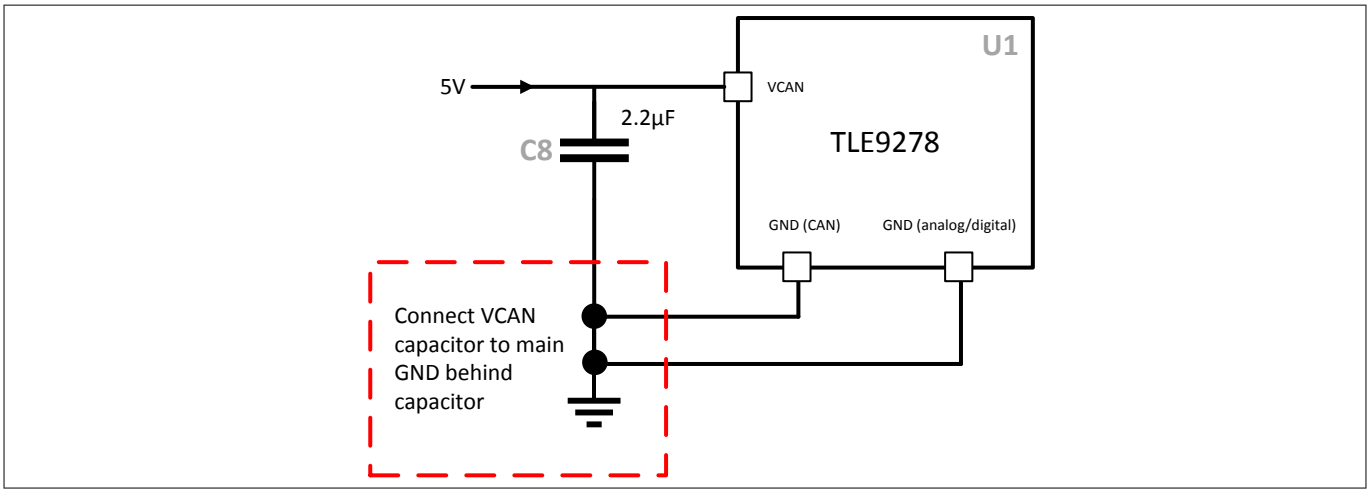


Figure 13 Grounding concept and BOM proposal for the CAN transceivers

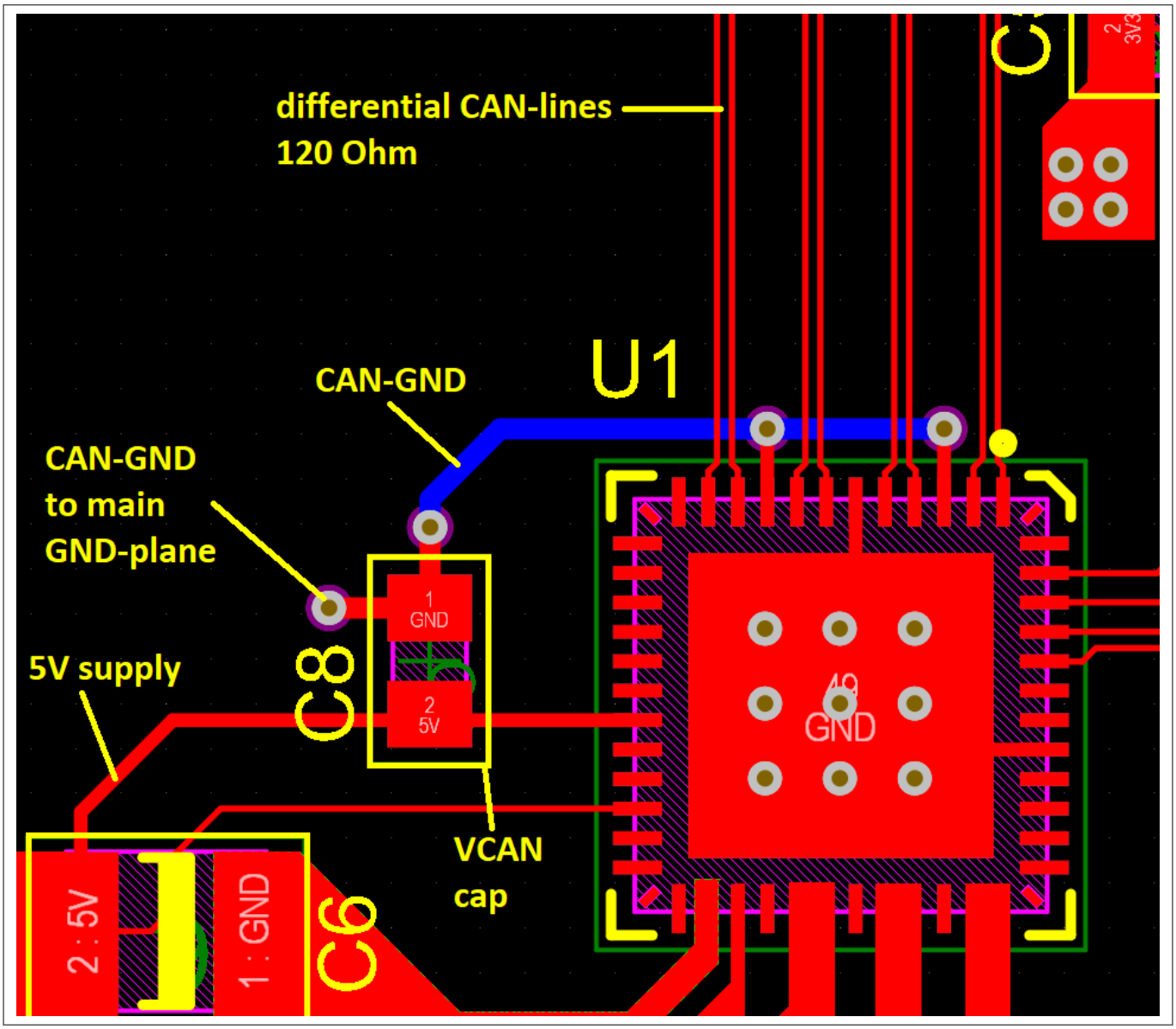


Figure 14 Recommended layout for the CAN transceiver GND connection

1.4.1.4 Grounding concept for the external regulator

The layout of the external PNP linear regulator is less critical than the layouts of the buck and boost converters. However, the output capacitor should be placed close to the PNP transistor to ensure stability. Also, the current sensing lines of the shunt resistor must be routed differentially.

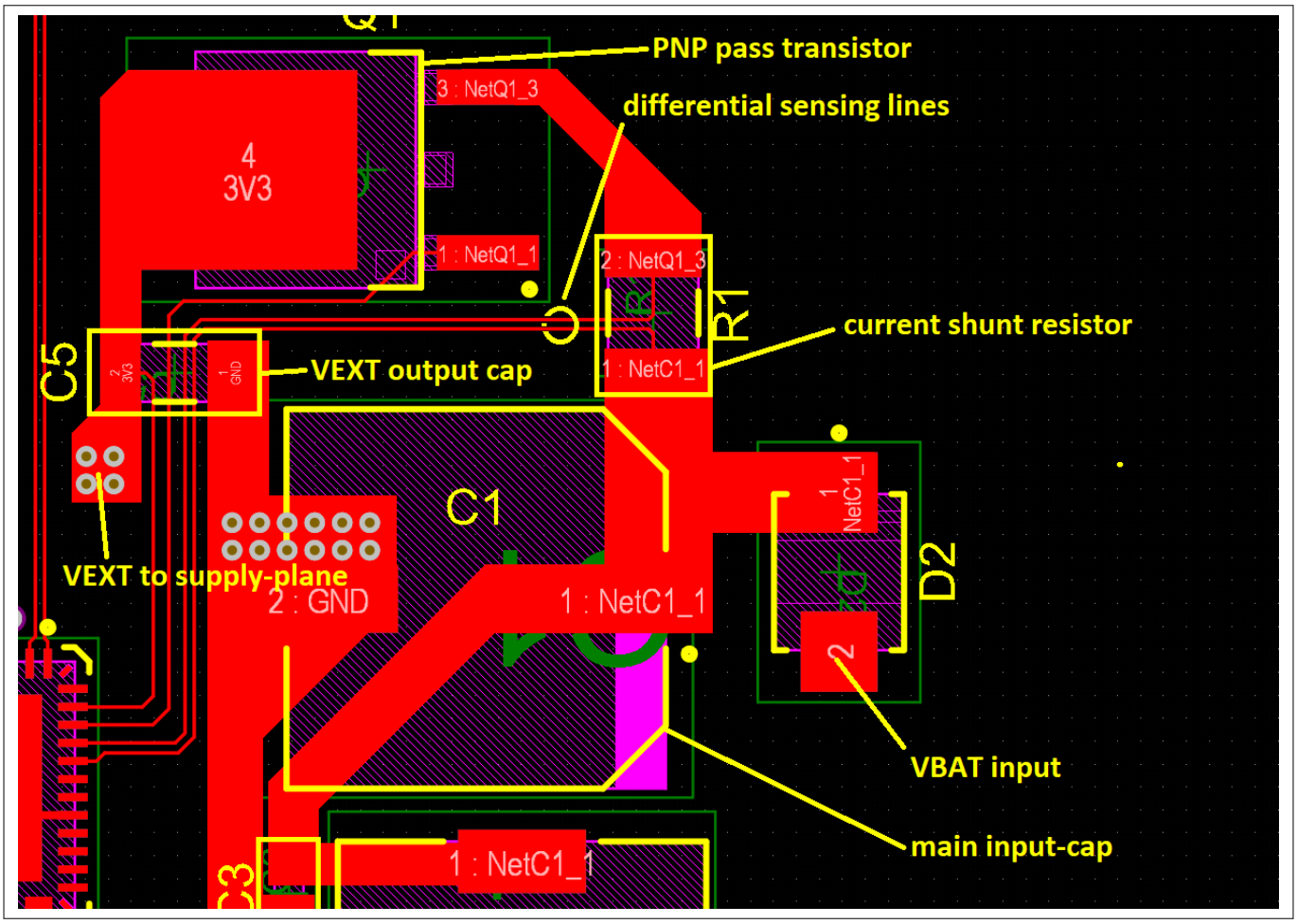


Figure 15 Recommended layout for the VEXT regulator

This recommended layout does not include dedicated thermal cooling areas, which are not needed for lower output currents. For larger output currents, we recommend placing a copper area underneath the PNP transistor.

The input of the VEXT can also be connected to the VCC1 output instead of to VBAT. This results in a lower voltage drop and, therefore, lower power dissipation.

1.4.2 ESD considerations

- All ground (GND) pins of the SBC should be connected together at the PCB (as star ground connection).
- Route CAN bus lines separated or shielded from other lines with alternating signals.
- Place SBC and microcontroller next to each other, as close as possible (focus on digital I/O).
- Pins that are directly connected to VBAT (e.g. VBSENSE) should get a serial resistor and bypass capacitor to limit ESD pulse effects.

1.4.3 EMC considerations

- All connections are preferably short for a low impedance.
- Place capacitors at VS, VCAN, VCC1 and VEXT as close as possible to these pins and the belonging ground.
- Connect bypass capacitors close to the pins to lower the reactance and limit electromagnetic emissions.
- All ground (GND) pins of the SBC should be connected together at the PCB (as star ground connection).
- Route CAN bus lines separated or even shielded.

- Place a bypass capacitor between VCAN and CAN GND (100 nF classical CAN, 1 µF CAN FD).
- Place SBC and microcontroller next to each other, as close as possible (focus on digital I/O).

1.4.4 Thermal considerations

- For improved thermal performance, a 4-layer PCB is recommended.
- The copper thickness and connection of high current nodes should be wide and thick (e.g. 35/70 µm).
- Thermal vias are recommended (as many as possible, preferably under the hot spots like Exposed Pads).
- Consider cooling areas as follows:
  - Connect all GND layers with thermal vias and use them for cooling (connect to Exposed Pad and common ground).
  - Form a quadratic copper area on the bottom side of the SBC with ≥ 300 mm^2.
  - Form a cooling area for the external high-side power transistor, if used (Note: connect to V_S).
- Avoid placing the SBC at the edge of the PCB, which could lead to increased mechanical stress.

1.5 VBSENSE

If the WK/VBSENSE pin is used as VBSENSE, a direct high-voltage monitoring (for example, VBAT) is possible. The VBSENSE pin must be protected against VBAT (unbuffered) pulses. For ESD protection, it is recommended to put a 10 kΩ series resistor and a bypass capacitor of 22 nF close to the VBSENSE pin.

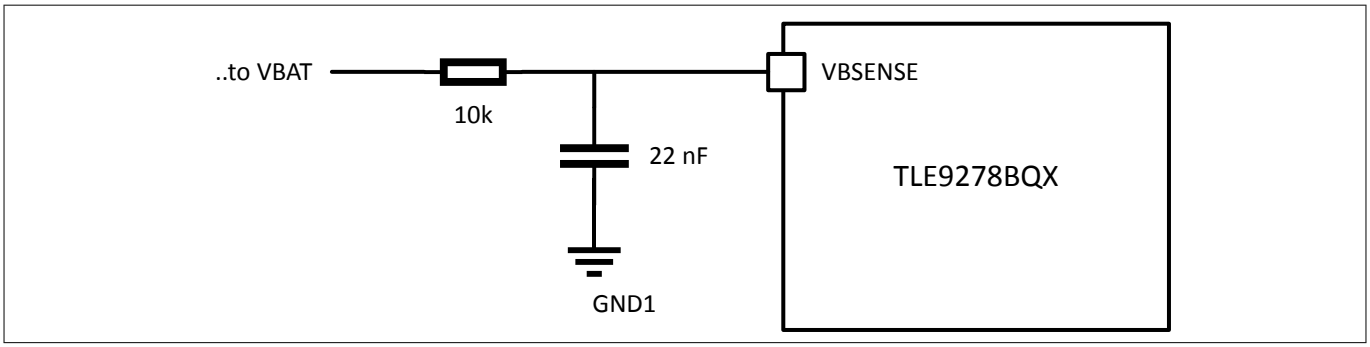


Figure 16 Sample VBSENSE configuration

2 Power dissipation and thermal measurements

2.1 Junction temperature measurement

2.1.1 Background

In order to verify the System Basis Chip (SBC) in the application properly, the maximum junction temperature must be determined to derive max. operating conditions and to ensure proper operation.

However, the device junction temperature cannot be directly determined for the SBC family in the application.

The solution is to measure the device temperature on the top of the package, and then to calculate the junction temperature by using the thermal correlation factor Ψ_{JT} (Psi).

The following pages show the boundary conditions and the results with an example.

2.1.2 Boundary conditions for Ψ_{JT} value calculation

Ψ calculation was performed with following conditions and variations:

- Two different PCB designs with 16 thermal vias each.
- Cooling area on bottom of PCB with 0 mm^2, 300 mm^2, and 600 mm^2.
- Ambient temperature: 85 °C and 105 °C.

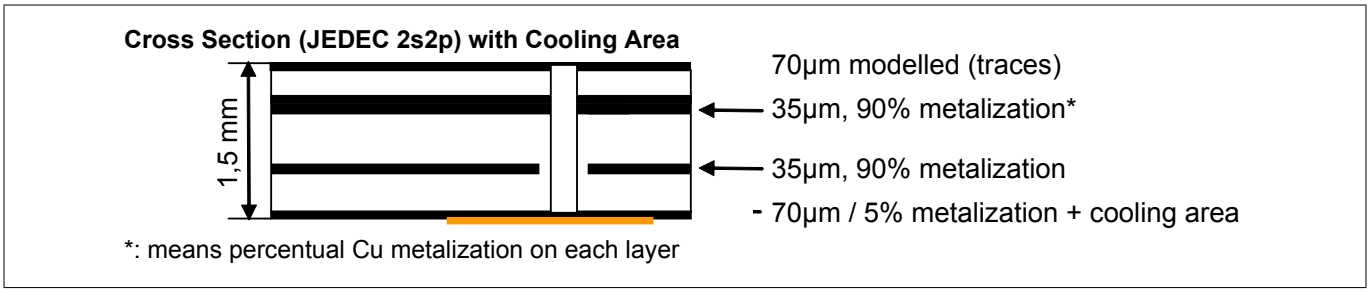


Figure 17 PCB stackup (JEDEC 2s2p) with cooling area

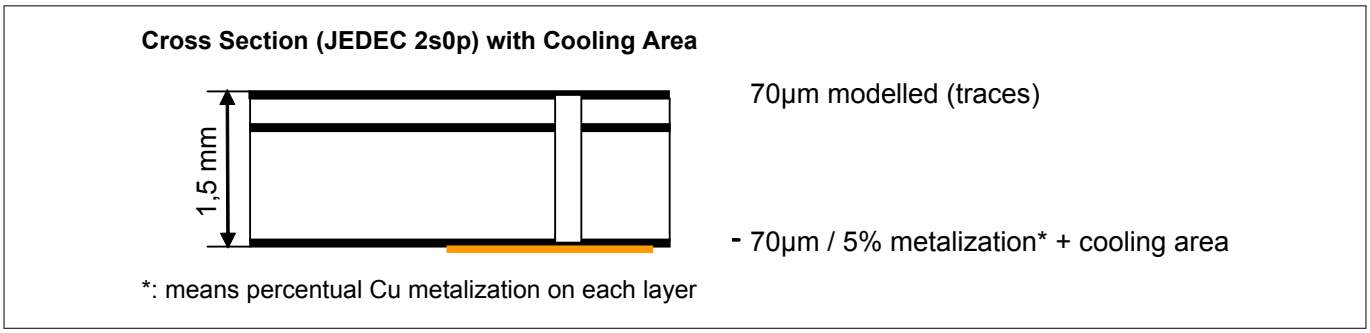


Figure 18 PCB stackup (JEDEC 2s0p) with cooling area

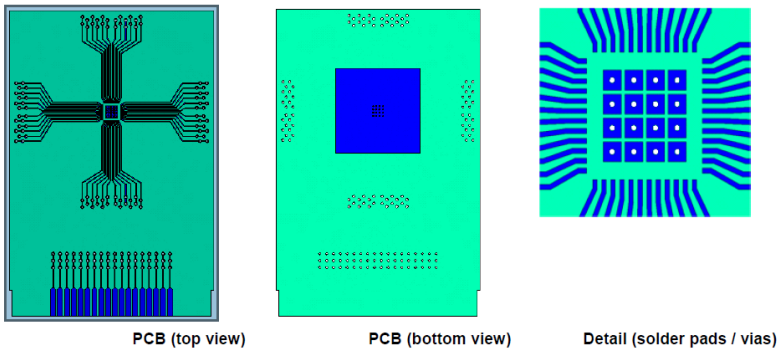


Figure 19 JEDEC PCB Layout

Table 5 Assumption for a nominal power dissipation per power module

Power module	Nominal power dissipation (W)
VCC1	0.51
Boost	1.10
Internal	0.08
CAN	0.14
Total	**1.83**

2.1.3 Ψ calculation results

The following figure shows the R_{thJA} results with the equivalent Ψ_{JT} values. From these Ψ_{JT} results, the chip temperature can be calculated if the package top temperature and the applied power is known (see ***Chapter 2.1.4***).

2s0p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	48.2	54.6	73.2
	Psi- jt [K/W]	7.51	7.78	8.59
2s2p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	31.0	31.7	34.8
	Psi- jt [K/W]	6.87	6.90	7.03

Rth-ja / Psi- jt for Tamb = 85°C

2s0p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	46.93	53.17	71.63
	Psi- jt [K/W]	7.79	8.05	8.89
2s2p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	30.63	31.31	34.42
	Psi- jt [K/W]	7.15	7.17	7.31

Rth-ja / Psi- jt for Tamb = 105°C

Figure 20 R_{thJA}/Ψ_{JT} results for both PCB designs

2.1.4 Calculation of the device junction temperature (T_J)

Natural convection thermal resistance R_{thJA} was determined in accordance with JEDEC JESD51-1 specifications and is calculated with the formula:

$$R_{thJA} = \frac{T_{junction} - T_{ambient}}{P_{dissipation}}$$

Ψ_{JT} is derived under natural convection conditions and provides a correlation between the junction temperature and the temperature on the package's top surface. Because temperature differences are driven by heat flow, the package's top temperature is close to the junction temperature. Ψ_{JT} is calculated with the formula:

$$\Psi_{JT} = \frac{T_{junction} - T_{top}}{P_{dissipation}}$$

The device junction temperature can be calculated by rearranging the formula accordingly:

$$T_{junction} = (\Psi_{JT} \cdot P_{dissipation}) + T_{top}$$

Example calculation

- Conditions
  - T_{top} = 110 °C
  - $P_{dissipation}$ = 1.83 W
  - PCB type: 2s2p
  - Cooling Area = 300 mm²
  - T_a = 85 °C
  - Resulting: R_{thJA} = 31.7 K/W, Ψ_{JT} = 6.9 K/W
- $T_{junction}$ = (6.9 K/W * 1.83 W) + 110 °C = 122.6 °C

3 Buck and boost converter application hints

3.1 Buck conversion efficiency

The diagram below displays the efficiency of the buck converter for a variety of source voltages and operating temperatures.

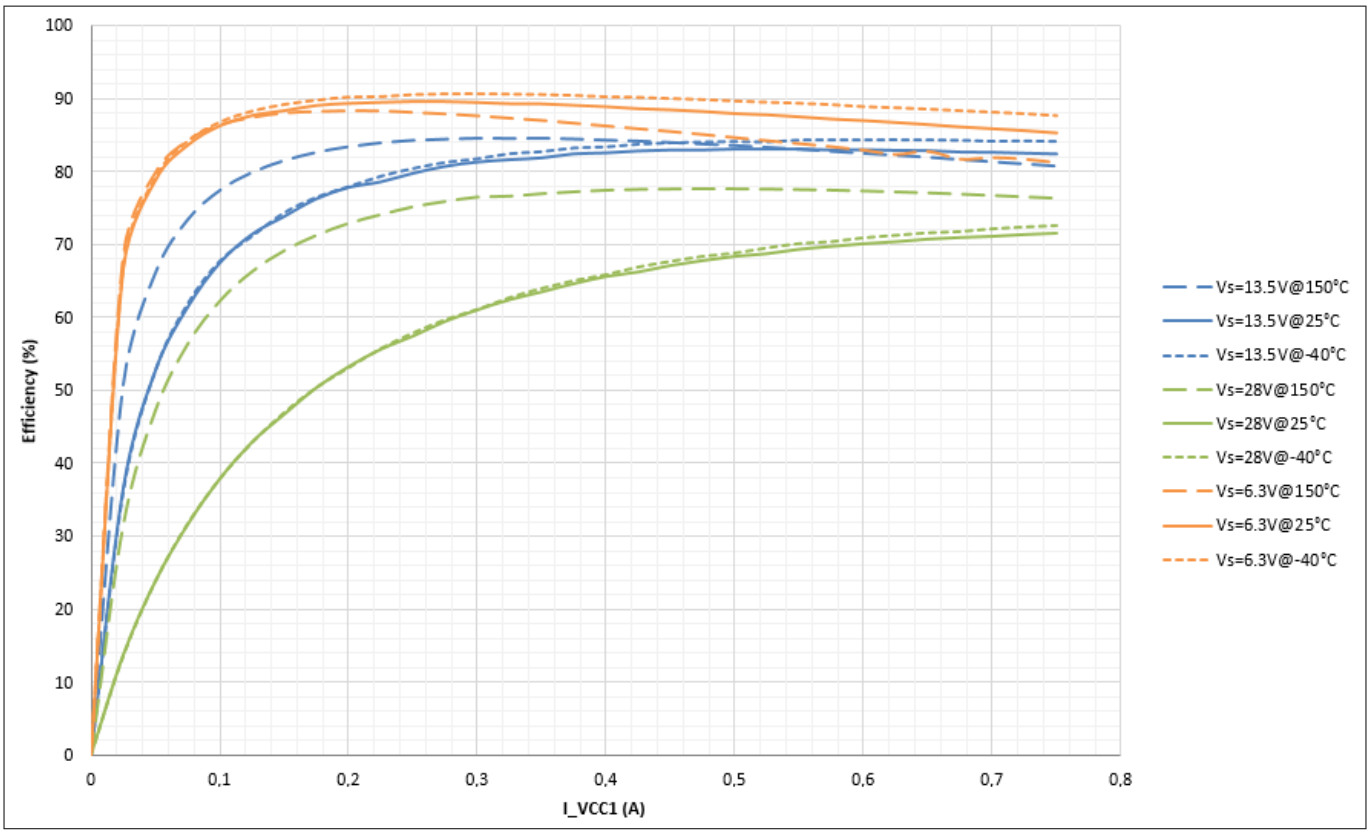


Figure 21 Buck conversion efficiency

3.2 Boost conversion efficiency

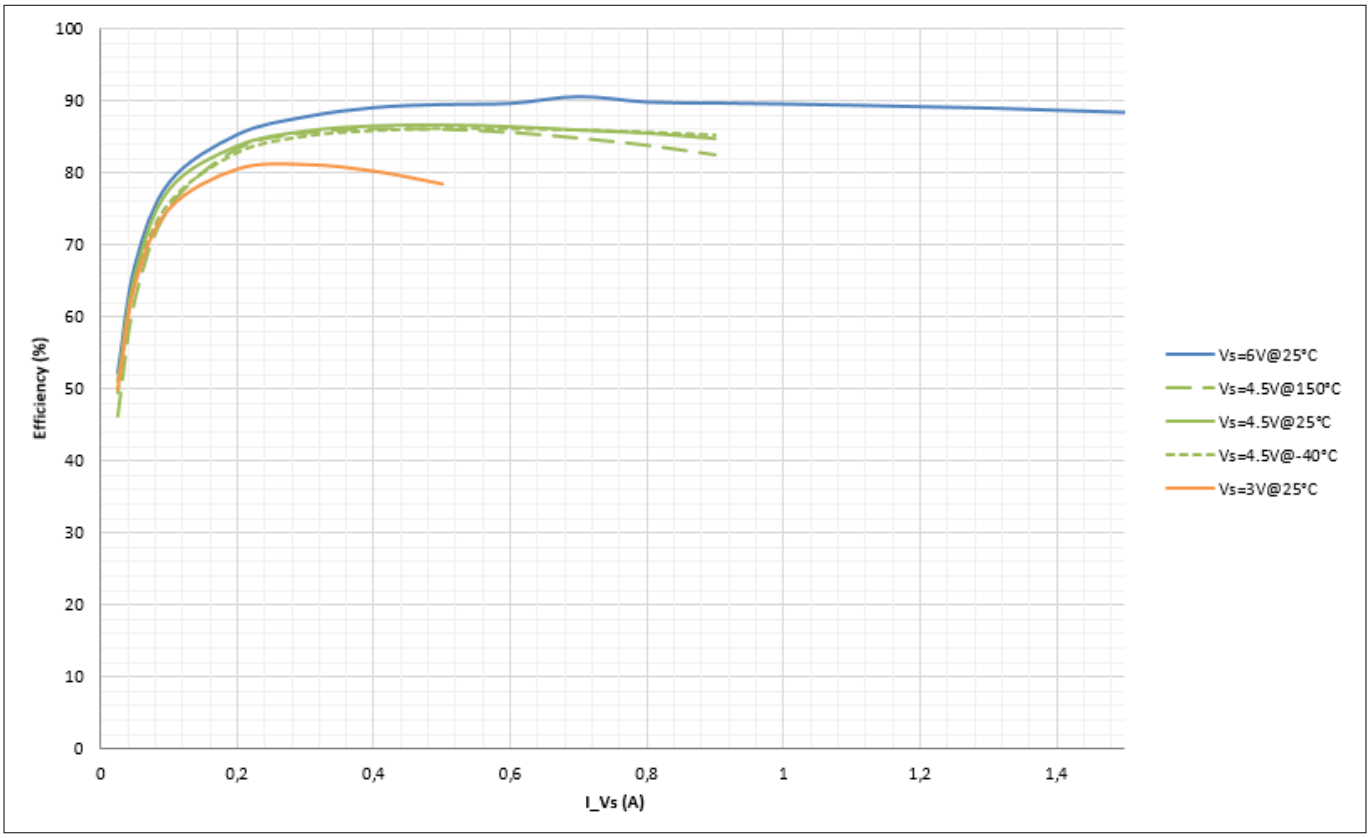


Figure 22 Boost conversion efficiency for 6.7V output

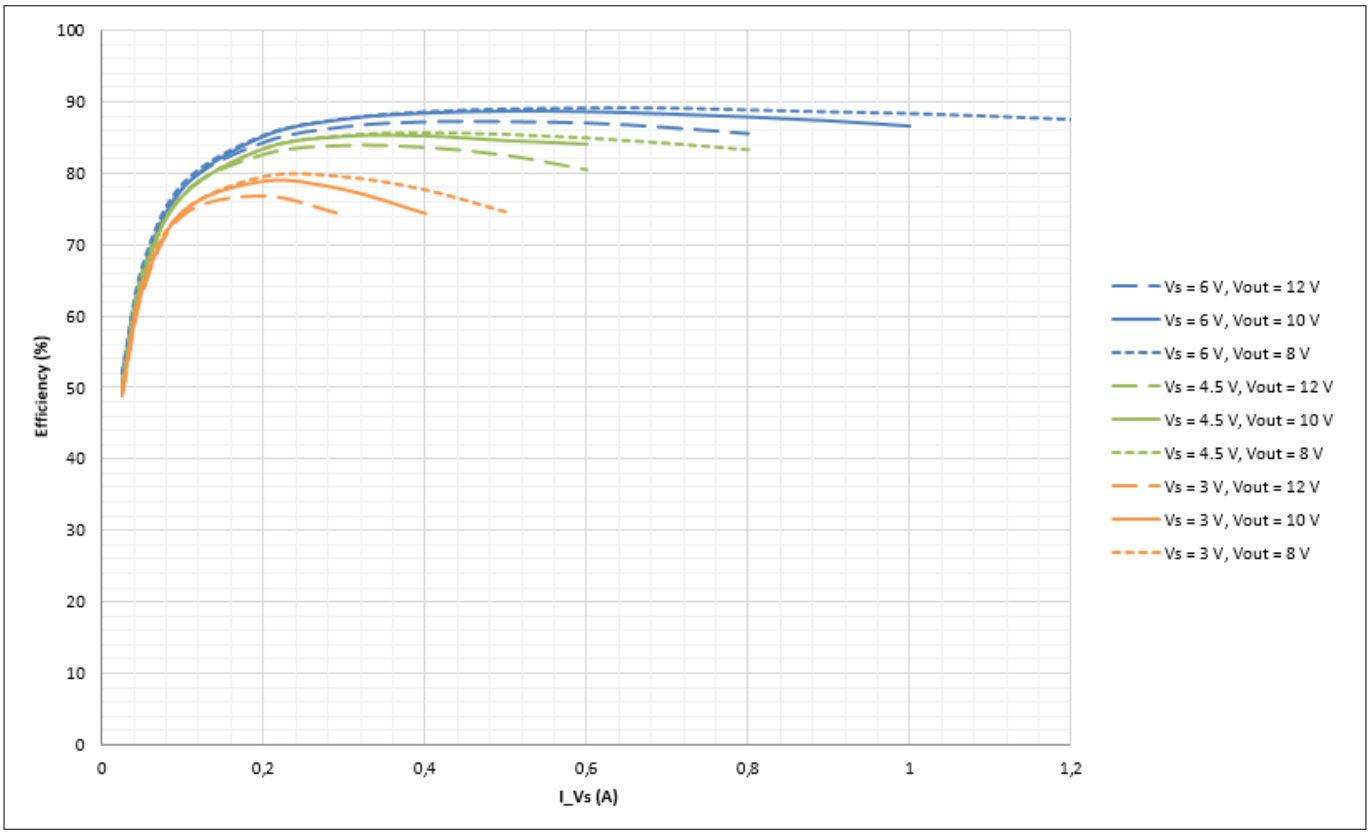


Figure 23 Boost conversion efficiency at 25 °C

3.3 Automatic PFM-PWM transition in SBC Stop Mode

To decrease power consumption in the SBC Stop Mode, the buck converter automatically operates in PFM mode if the load current is typically below 110 mA when the Stop Mode is entered. When the load current exceeds 110 mA, the device automatically re-enters PWM mode. As a precondition, the PWM_AUTO bit in the HW_CTRL_0 register must be set to 1.

4 VEXT application hints

4.1 Increasing the VEXT nominal output voltage with external components

VEXT can be set internally to a nominal voltage of 5 V, 3.3 V (default), 1.8 V, or 1.2 V via SPI.

If the PCFG pin is connected to GND, VEXT is activated by default without requiring an SPI command, providing 3.3 V (default).

Alternately, any output voltage between 3.3 V and 5 V can be set before enabling SPI, using an external resistive divider. The example below shows a 5 V output voltage generation for a 3.3 V type.

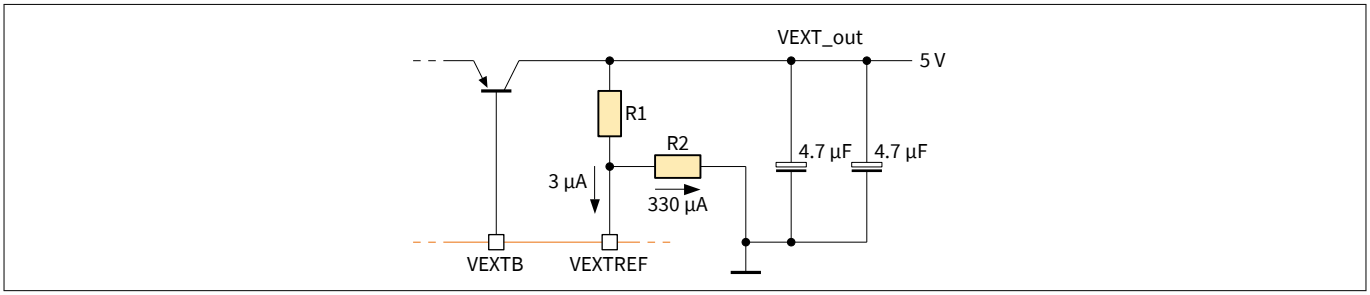


Figure 24 Increasing the default VEXT output voltage

Calculation

Input current on VEXTREF:

$$R1 = \frac{VEXT_{out} - VEXT_{ref}}{I_{R2} + I_{VEXT_ref}} = \frac{5\,V - 3.3V}{330\mu A + 3\mu A} = 5.11\,k\Omega$$

assuming a typical base current of 3 µA at ambient temperature.

The resulting 330 µA are assumed to be a balanced choice between circuit robustness and current consumption (see also next page):

$$R2 = \frac{VEXT_{ref}}{I_{R2}} = \frac{3.3\,V}{330\,\mu A\,\cdot} = 10\,k\Omega$$

The following recommendations should be considered:

- Use 1% (or better) SMD resistors placed very close to the VEXTREF pin.
- Use in parallel 2 x 4.7 µF ceramic, low ESR capacitors (or 1 x 10 µF) to achieve a good regulation performance and place it close to the collector of the PNP.
- Recommended current through R2: 330 µA (a balanced choice between current consumption and circuit robustness).
- Additional tests are required in the real application board to verify the circuit performance for all boundary conditions of the application.

The VEXT output voltage is estimated as max. additional +/-2% error to the specified output voltage tolerance, using 1% tolerance resistors. It can be improved by using resistors with 0.1% tolerance.

4.2 VEXT robustness hints - short circuit of VEXT against GND for external supplies

VEXT can be used in the stand-alone configuration to supply external loads. In the event of a short circuit to GND, negative voltage undershoot can occur due to resonance of the output capacitor/wire inductance combination. The absolute maximum ratings of the device (for example, VEXTREF pin) can be exceeded. In order to limit such effect, the load should be connected close or a resistor R_{Lim} of about 100 Ohm can be inserted (see ***Figure 25***). The electrical functionality of the regulator remains unchanged.

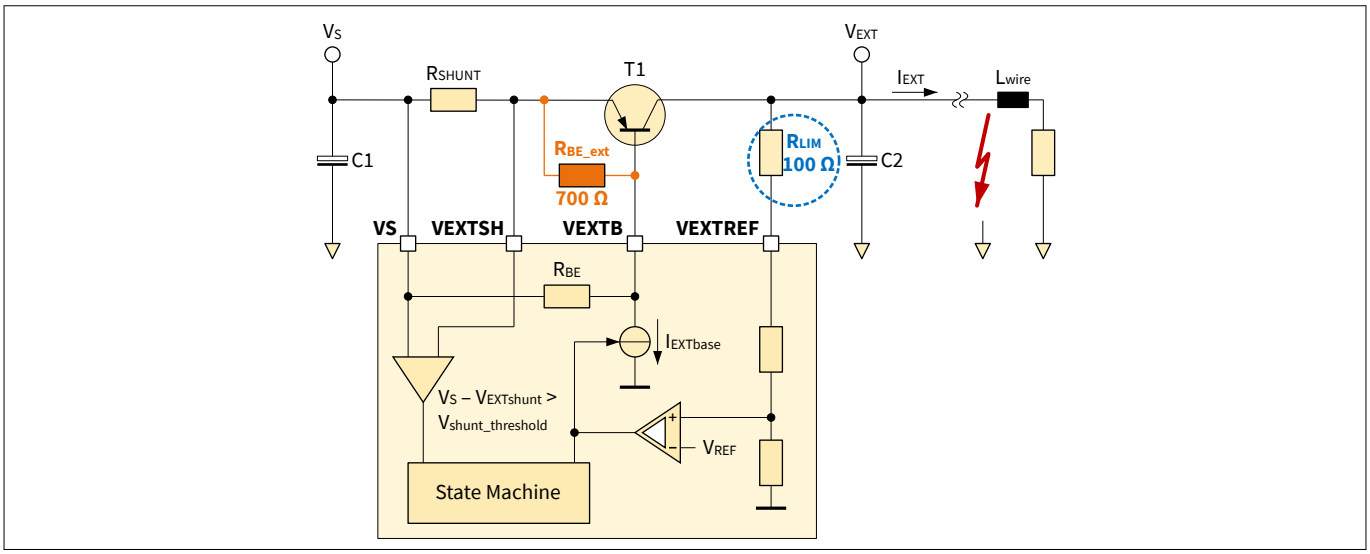


Figure 25 VEXT external supply with robustness for short circuit against GND

4.3 VEXT robustness hints - protection against increased VEXT output voltage

In adverse environmental conditions (dirt, humidity, icing, …), an external leakage path from the base of the PNP (VEXTB) to GND may occur. A respective leakage current causes an increased output voltage when VEXTB is on, which could violate the max. ratings of VEXTB. Also, the output voltage could rise when VEXTB is OFF. The device has an internal protection circuitry which prevents the above mentioned behavior. It can compensate a leakage current of ~200 µA on VEXTB, and can sink 2.5 mA on VEXTREF (see ***Figure 25***).

If a leakage current on VEXTB may exceed the value stated above, an external resistor R_{BE_EXT} of about 700 Ohm can be inserted to further compensate excessive leakage currents. This applies to VEXTB stand-alone configurations. The functionality of the regulator remains unchanged. However, additional currents contribute to the SBC overall current consumption.

5 CAN partial networking hints - SWK configuration and activation

5.1 Background

CAN Partial Networking (PN) allows to reduce the current consumption of the CAN network significantly by putting selected nodes into a sleep mode, and waking them up only if needed. The MCP+ SBC family offers devices with CAN PN according to ISO11898-2:2016. The respective feature is named Selective Wake (SWK).

In the following sections, all configuration and activation tasks, needed to properly use this feature, are described.

A MCP+ device has four integrated CAN transceivers and, therefore, four separate SWK modules. All descriptions in the following sections apply only to a single SWK module. In each case, you must select the desired module first using the CAN_SWK field in the BUS_CTRL_3 register.

5.2 SWK configuration and activation sequence

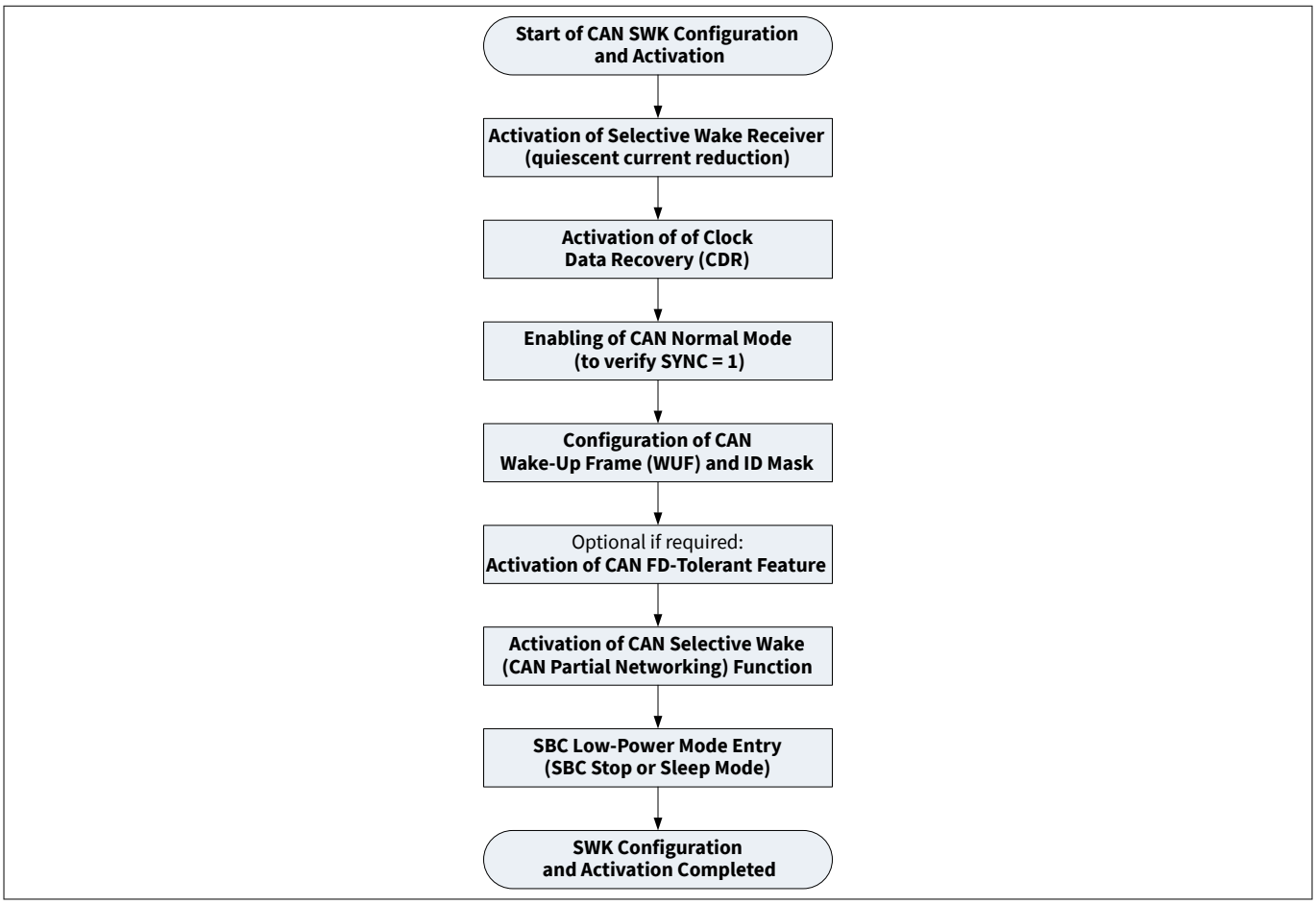


Figure 26 Overall SWK configuration & activation sequence

For a detailed explanation of the different sequence steps, see below:

- Activation of Selective Wake Receiver, see ***Chapter 5.3*** on page 29.
- Activation of Clock Data Recovery (CDR), see ***Chapter 5.4*** on page 29.
- Configuration of CAN Wake-Up Frame (WUF), see ***Chapter 5.5*** on page 30.
- Activation of CAN FD tolerant feature, see ***Chapter 5.6*** on page 31.
- Activation of CAN Selective Wake function, see ***Chapter 5.7*** on page 31.
- SBC Low-Power Mode entry, see ***Chapter 5.8*** on page 32.

5.3 Activation of the Selective Wake Receiver

When the Selective Wake Receiver is activated, the quiescent current is increased by typically 750 µA plus 250 µA per additional CAN module (after the first). When partial networking is deactivated on the device and regular CAN communications resume, we recommend that the Normal Mode Receiver is activated again.

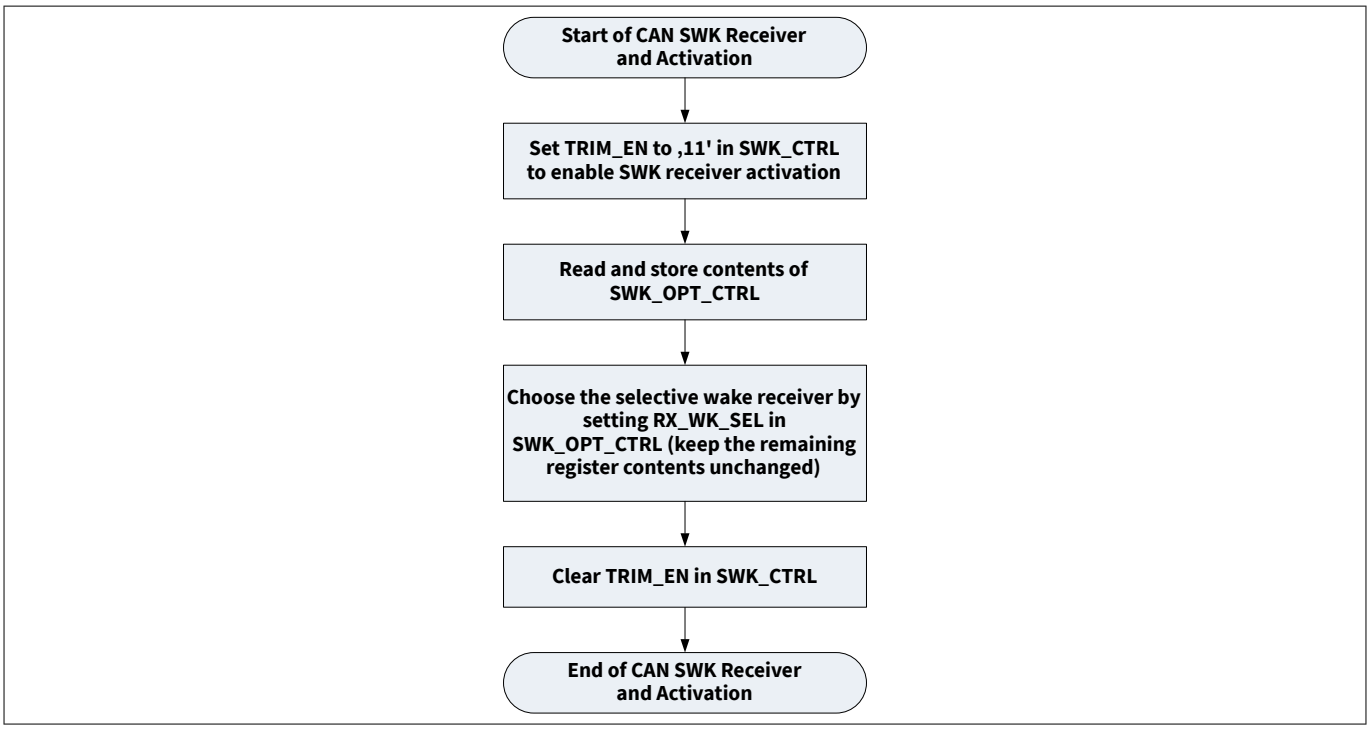


Figure 27 Activation of the Selective Wake Receiver

5.4 Activation of the Clock Data Recovery (CDR)

It is strongly recommended to enable the Clock Data Recovery (CDR) to compensate for drift effects (lifetime, temperature).

The CDR settings of the registers SWK_CDR_CTRL2, SWK_BTL0_CTRL1_CTRL, SWK_CDR_LIMIT_High_CTRL, SWK_CDR_LIMIT_LOW_CTRL need to be chosen depending on the CAN baud rate. Please also refer to *Recommended CDR Settings for Different Baud Rates* in the datasheet.

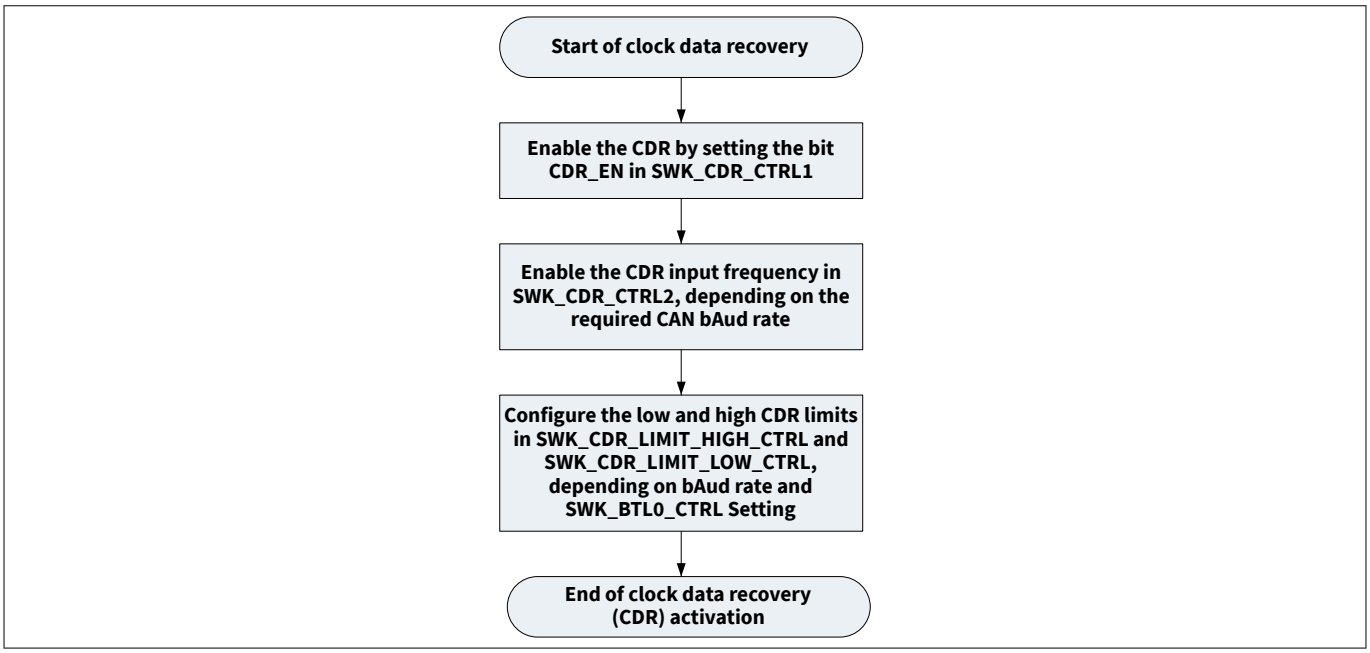


Figure 28 Activation of the Clock Data Recovery (CDR)

5.5 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

The ID configuration depends on standard or extended frame format. In both cases, the configuration is done from the end of the registers, e.g. in SWK_ID3_CTRL and SWK_ID2_CTRL.

The DLC content must match exactly the number of data bytes.

It is not possible to mask the IDE bit (Identifier Extension bit).

The data bytes start from SWK_DATA7_CTRL, e.g., if two data bytes are sent, they have to be configured in SWK_DATA7_CTRL and SWK_DATA6_CTRL.

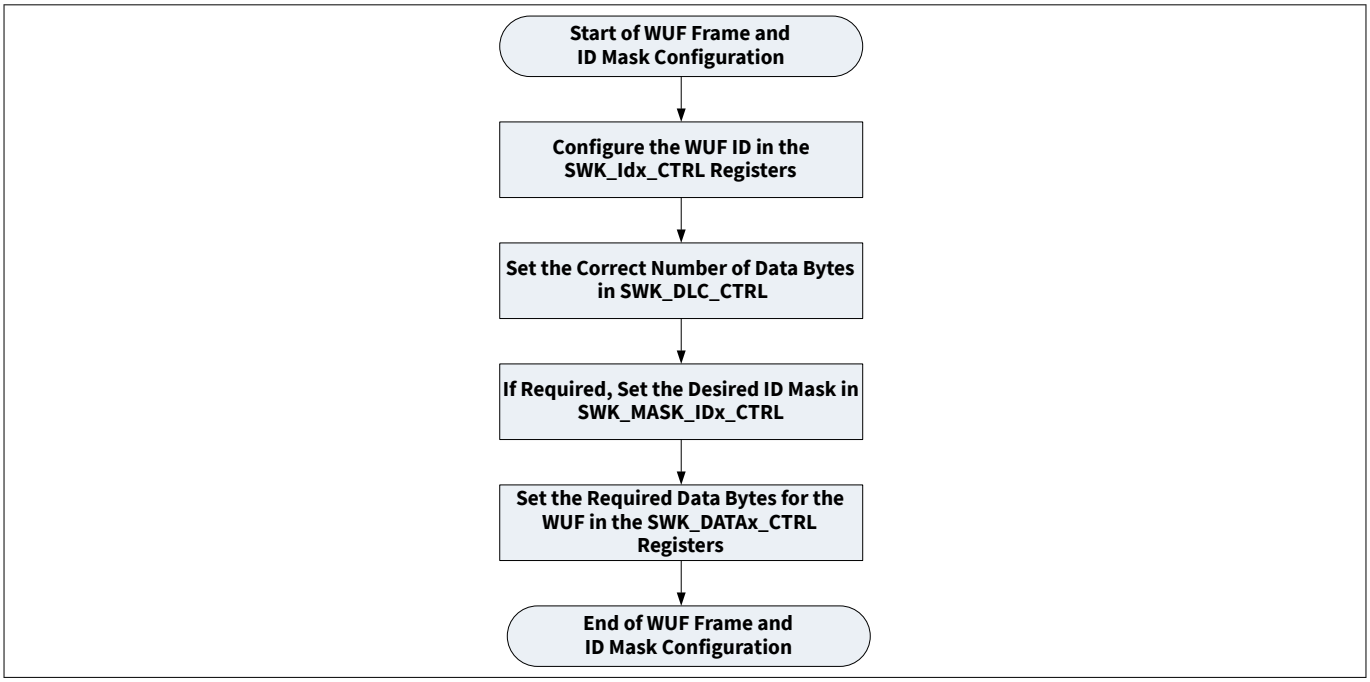


Figure 29 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

5.6 Activation of the CAN FD-tolerant feature (optional)

This is an optional feature and should only be used if the CAN FD tolerance is needed for the respective ECU (mixed classical and CAN FD networks).

The recommended settings apply for an arbitration rate of 500 kBit/s and a 2 MBit/s CAN FD communication.

For more information, please refer to chapter 5.6.7 of the datasheet, and to the SPI register SWK_CAN_FD_CTRL.

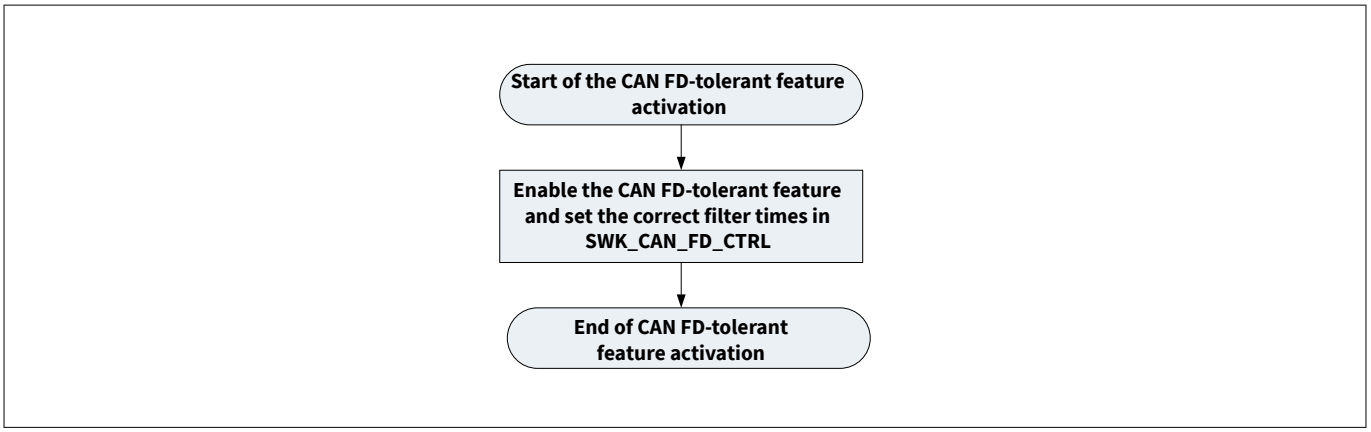


Figure 30 Activation of the CAN FD-tolerant feature

SWK_CAN_FD_CTRL
CAN FD Configuration Control Register (Address 011 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN
r	r	rwh	rw	rw	rw	rw	rw

Figure 31 SWK_CAN_FD_CTRL register

5.7 Activation of the CAN Selective Wake (SWK) function

The synchronization of the protocol handler must be ensured for the Selective Wake operation, to ensure a wake-up via WUF.

The CFG_VAL bit is cleared by the SBC in case the SWK configuration is changed, or in case of a configuration error.

SWK_STAT content must be: SWK_SET = 1, SYNC = 1, WUP = 0, WUF = 0.

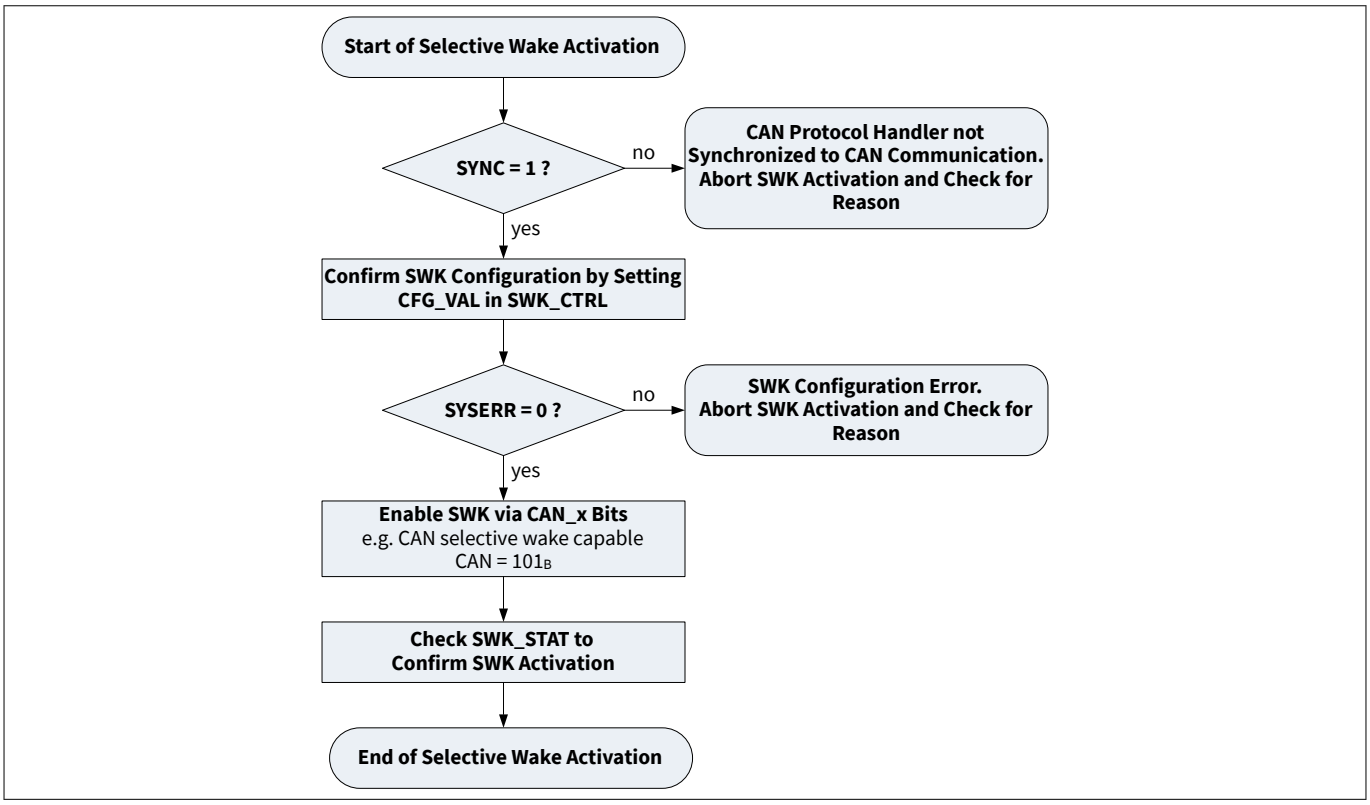


Figure 32 Activation of the CAN Selective Wake (SWK = CAN partial networking) function

5.8 SBC Low-Power Mode (SBC Stop or Sleep Mode) entry

Right after enabling SWK, this sequence should be executed.

Before entering SBC Sleep Mode, it is mandatory to check pending wake events and to clear the wake status register.

Wake events lead to disabling the SWK function.

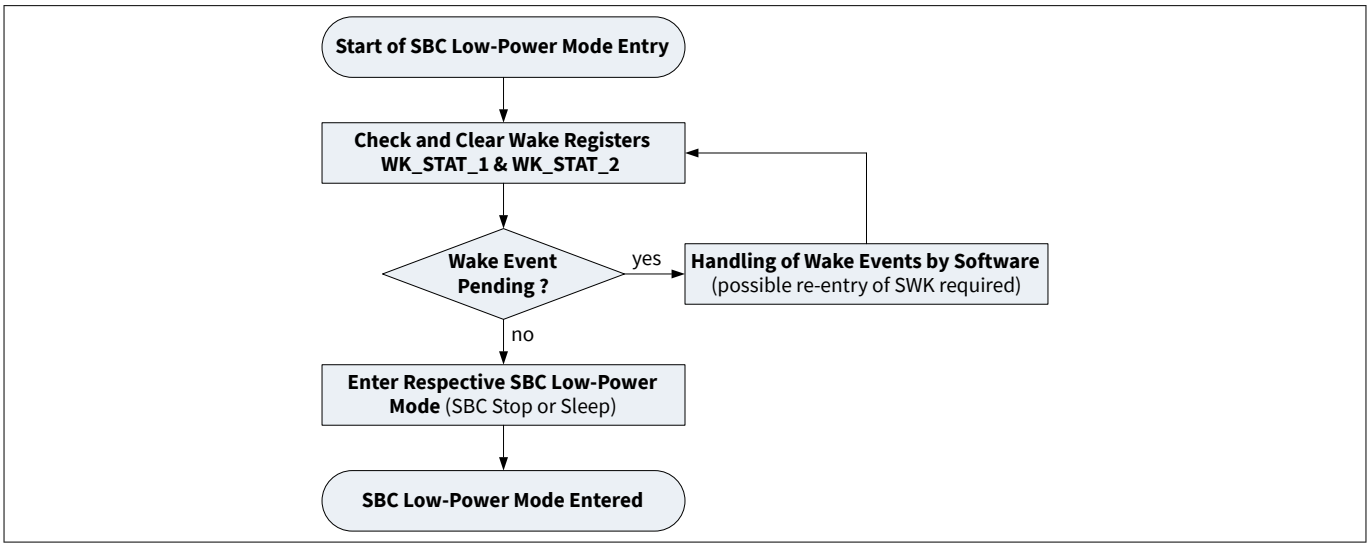


Figure 33 SBC Low-Power Mode entry

6 SPI interface

6.1 MCP+ System Basis Chip (MCP+ SBC) family

The MCP+ SBC family features an in-depth diagnosis and failure signalization in the SPI registers (status registers). These diagnosis and failure bits are intended to support a system and failure diagnosis of the ECU, which is typically required by the system and by functional safety.

The diagnosis functions are in general required by OEMs, but vary in detail, depending on the partitioning and implementation. There are also prewarning bits (e.g., thermal prewarning or VCC1 under-voltage prewarning) which can be used to react early enough to perform emergency savings, to disregard incorrect measurements, or to shut down functions, avoiding a thermal shutdown.

6.2 SPI configuration

6.2.1 Timing

The SPI command is executed, at the latest, 5 µs after the CSN is set to HIGH. In general, care must be taken about the minimum CSN High time, and the minimum time between two SPI commands, which is 3 µs (see P_13.7.23 and P_13.7.24 in the datasheet).

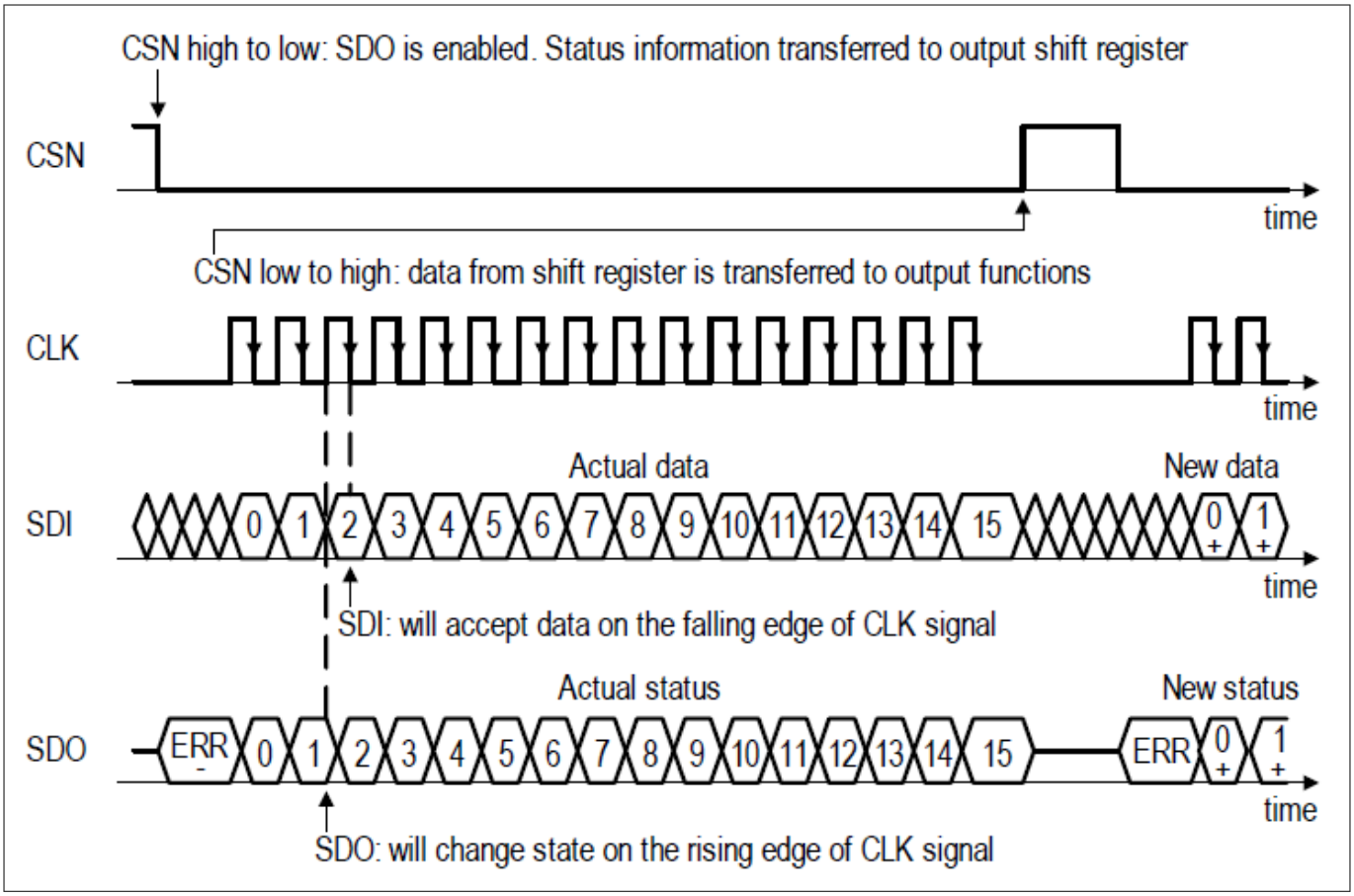


Figure 34 SPI timing diagram

The data is sampled with the falling edge of the clock, therefore, the clock polarity from the microcontroller usually must be set to inverted phase.

6.2.2 Status information field

The status information field immediately shows whether there was a change in status flags (avoids unnecessary polling). The bit in the status information field is set, if any bit in the respective register is set.

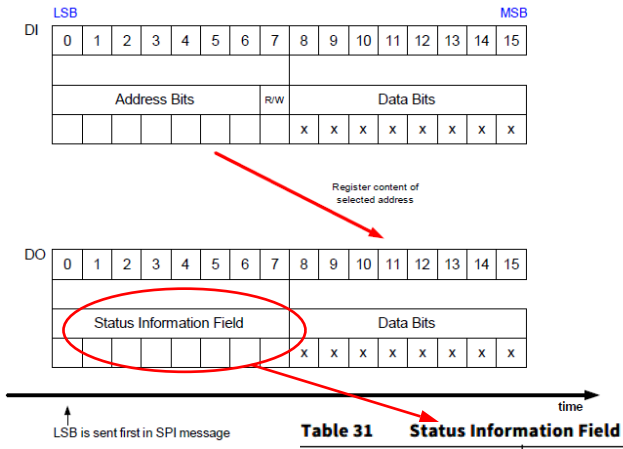


Table 31 Status Information Field

Status Information Bit	Symbol Address Bit	Status Register
0	100 0001	**SUP_STAT_0** & **SUP_STAT_1** (Combinational OR): Supply Status (VCC1 and VEXT), POR
1	100 0010	**THERM_STAT**: Thermal Protection Status
2	100 0011	**DEV_STAT**: Device Status - Mode before Wake, WD Fail, SPI Fail, Failure
3	100 0100	**BUS_STAT_0**: Bus Failure Status: CAN0, VCAN
4	100 0101	**BUS_STAT_2** & **BUS_STAT_3** (Combinational OR): Bus Failure Status: CAN1, CAN2 and CAN3
5	100 0110	**WK_STAT_0**: Wake Source Status for CAN0, WK, Timer and PFM-to-PWM transition
6	100 0111	**WK_STAT_2**: Wake Source Status for CAN1, CAN2, CAN3, and VBAT_UV
7	100 1100	**SMPS_STAT**: SMPS Status

Figure 35 SPI interface – status information field

For example, the SBC might return "00001000" as the status information field's content. In this example, bit 3 is set to 1 and all other bits to 0. (The most significant bit is the first; the least significant bit is the last.) This indicates that at least one bit of the BUS_STAT_0 register is 1.

For more detailed information about the error, send a read request for the BUS_STAT_0 register to find out which bits are 1. This lets you determine whether the failure is related to VCAN undervoltage, a thermal shutdown of the transceiver cell, a bus-dominant timeout, or a TXD-dominant timeout.

6.2.3 Register mapping structure

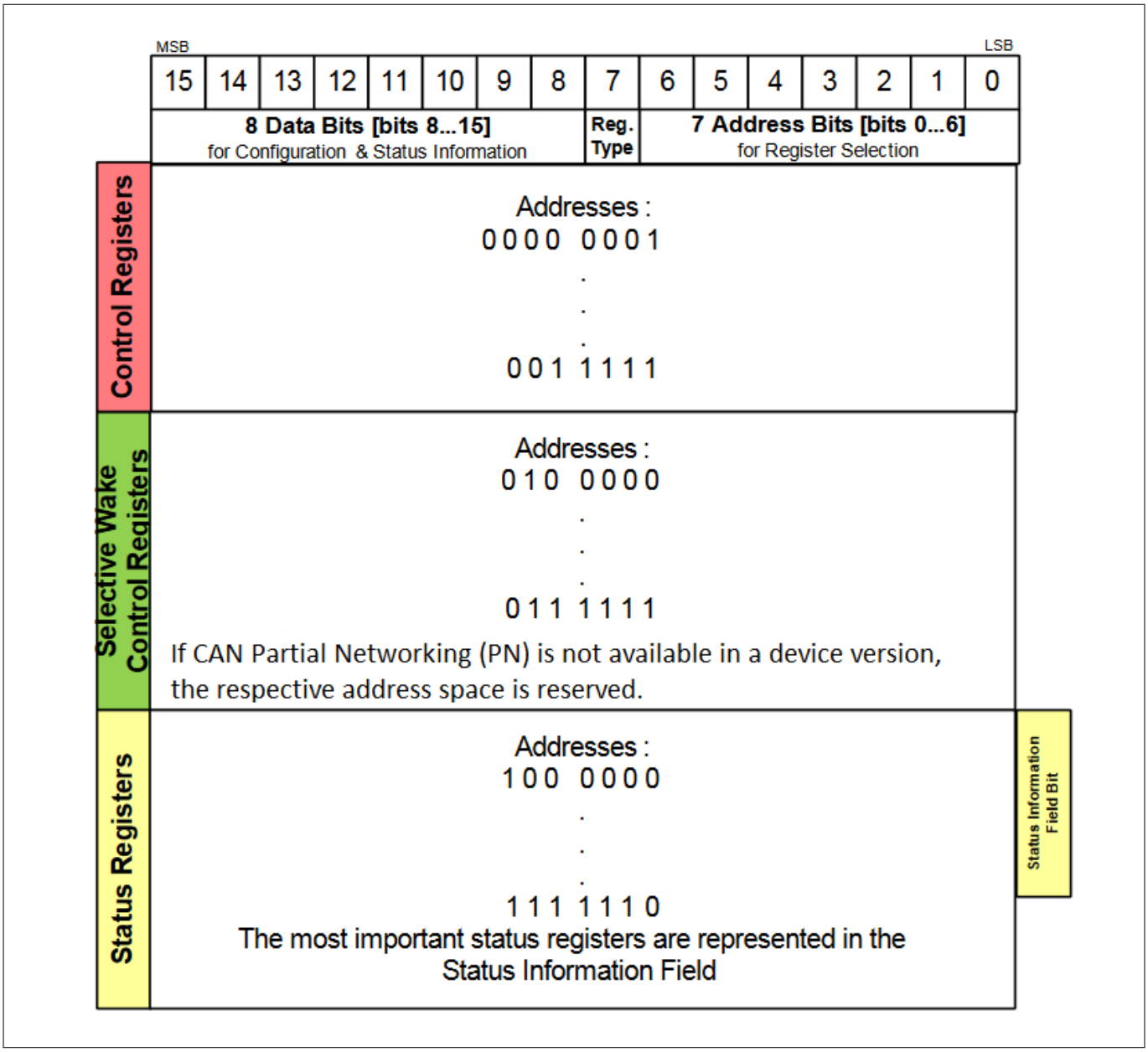


Figure 36 SPI register mapping overview

The register mapping includes:

- Control registers to configure all SBC contents in SBC Normal Mode.
- SYS_STAT_CTRL is a freely usable 8-bit RAM register – not changed by SBC.
- Selective wake registers only visible in -3BQX variants.
- Status registers for wake and failure signalization and diagnosis (keep content until actively cleared).

6.3 SPI diagnosis

6.3.1 Prewarning examples

- Thermal prewarning

TPW	0	rc	**Thermal Pre Warning** 0B , No Thermal Pre warning 1B , Thermal Pre warning detected

  - Provides early warning that the SBC is close to the critical junction temperature.
- VIO undervoltage prewarning

VIO_ WARN	0	rc	**VIO Undervoltage Prewarning ($V_{PW,f}$)** 0_B No VIO undervoltage prewarning 1_B VIO undervoltage prewarning detected

  - Provides early warning in case the VIO undervoltage threshold is set to a lower level, and the VIO voltage is not sufficient anymore.
  - Possible actions: Emergency saving of RAM data, refusing ADC measurements, disabling communication.

6.3.2 Determining the source of a restart or reset

Description
Power-On Reset Detection 0_B No POR 1_B POR occurred
Reserved, always reads as 0
VIO Short to GND Detection 0_B No short 1_B VIO short to GND detected
VIO UV-Detection (due to VRTx reset) 0_B No Fail-Safe Mode entry due to 4th consecutive VIO_UV 1_B Fail-Safe Mode entry due to 4th consecutive VIO_UV
VIO UV-Detection (due to VRTx reset) 0_B No VIO_UV detection 1_B VIO UV-Fail detected

Wake up via CAN_0 Bus 0_B No Wake up 1_B Wake up
Wake up via cyclic wake 0_B No Wake up 1_B Wake up
Reserved, always reads as 0
Wake up via WK 0_B No Wake up 1_B Wake up

TSD2 Thermal Shut-Down Detection 0_B No TSD2 event 1_B TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1 Thermal Shut-Down Detection 0_B No TSD1 fail 1_B TSD1 OT detected
Thermal Pre Warning 0_B No Thermal Pre warning 1_B Thermal Pre warning detected

Device Status before Restart Mode 00_B Cleared (Register must be actively cleared) 01_B Restart due to failure described in Table 8 and Table 9. 10_B Sleep Mode 11_B Reserved
Reserved, always reads as 0
Number of WD-Failure Events (1/2 WD failures depending on INTN) 00_B No WD Fail 01_B 1x WD Fail, FOx activation- Config 1/2 10_B 2x WD Fail, FOx activation- Config 3/4 11_B Reserved (never reached)
SPI Fail Information 0_B No SPI fail 1_B Invalid SPI command detected
Activation of Fail Output FO 0_B No Failure 1_B Failure occurred, FO is activated

Figure 37 Status registers signalize the potential source of wake-up and failure events

7 Reset behavior during power-up/down

7.1 Possible VCC1 undervoltage reset toggling due to dynamic load changes

If V_S is close to the VCC1 undervoltage threshold (VRTx), a dynamic variation of the load current can generate a reset toggling. (See ***Figure 38***.)

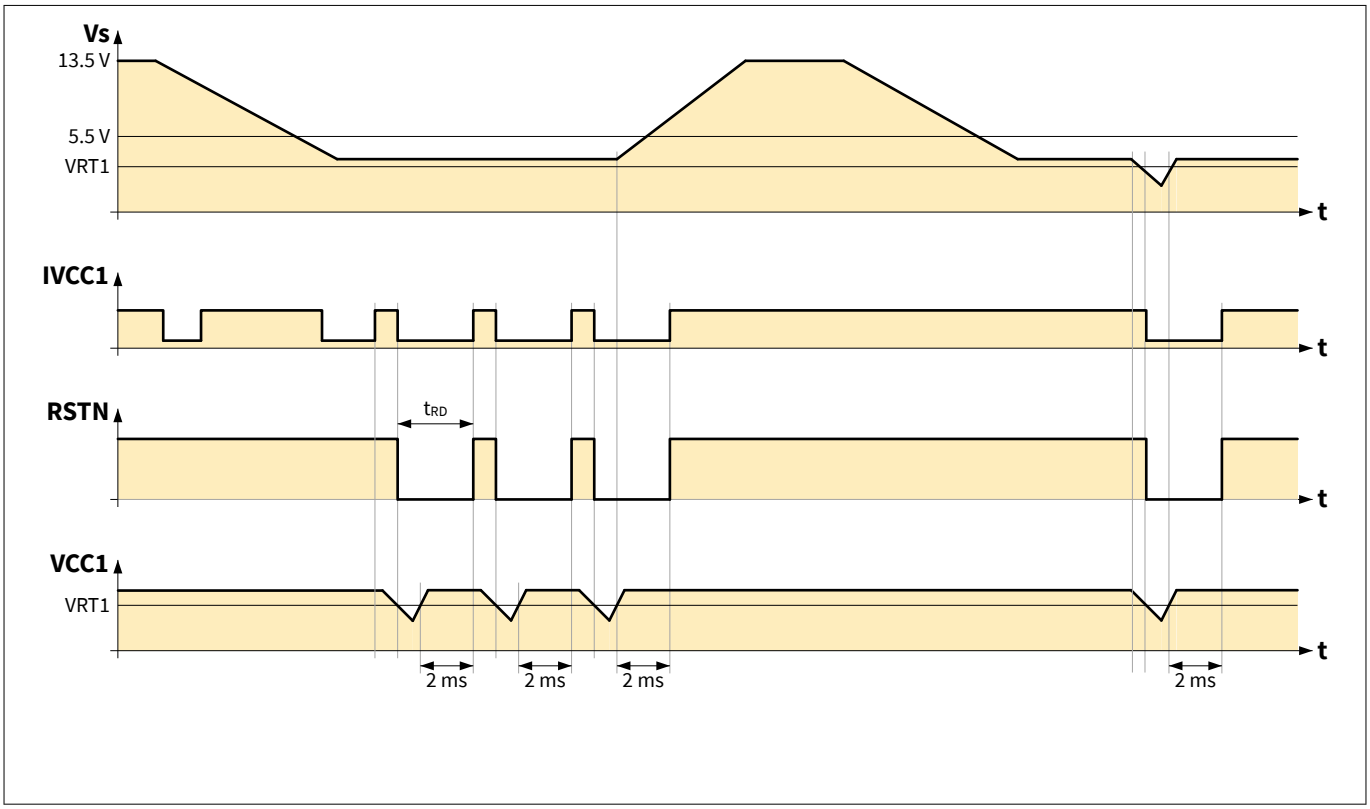


Figure 38 Simplified timing diagram of reset behavior at low supply voltage

- If V_S is close to the VCC1 undervoltage threshold level, the voltage regulator already operates in the linear region ($V_{drop} = R_{on} * I_{load}$).
- A VCC1 undervoltage reset forces the microcontroller into reset state as well, and the load current on VCC1 drops immediately.
- Therefore, VCC1 increases and could rise again above the undervoltage threshold (and the SBC reset is released).
- The startup of the microcontroller applies the load again, and V_S triggers the undervoltage level again.
- The behavior can repeat (toggling) as long as V_S stays at this sensitive level.
- Also a load step on VEXT, influencing the V_S level, could cause the same behavior of VCC1 undervoltage reset toggling.

7.2 Use case LV124-E07

The LV124-E07 test is a typical use case to check for potential reset toggling caused by low supply voltage, which can be triggered for any device with an integrated undervoltage reset if a dynamic load (for example, a microcontroller) is supplied by VCC1.

4.7.2 Test

Table 17: Test Parameter E-07: Slow ramp-down and ramp-up of power supply voltage

Operating modes of the DUT	**Test 1:** KL 30 ON and KL 15 ON **Test 2:** KL 30 ON
Initial voltage	U_{Bmax}
Rate of voltage ramp-down/ramp-up	0.5 V/min
Hold time at U_{Bmax}	Until error memory completely read out
Minimum voltage	0 V
Final voltage	U_{Bmax}
Number of cycles	1 cycle in operating mode II.c 1 cycle in operating mode II.a
Number of DUT	minimum 6

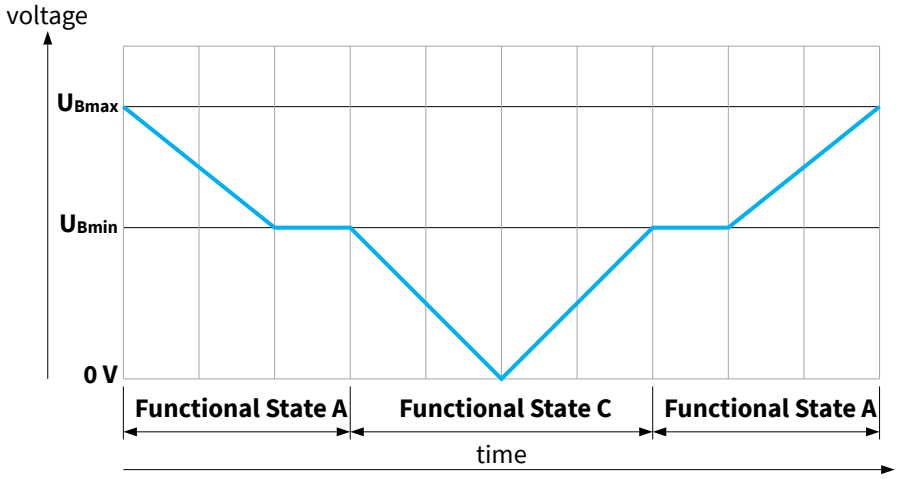


Figure 39 Voltage ramp for testing low supply voltage according to LV124

Reset behavior during power-up/down

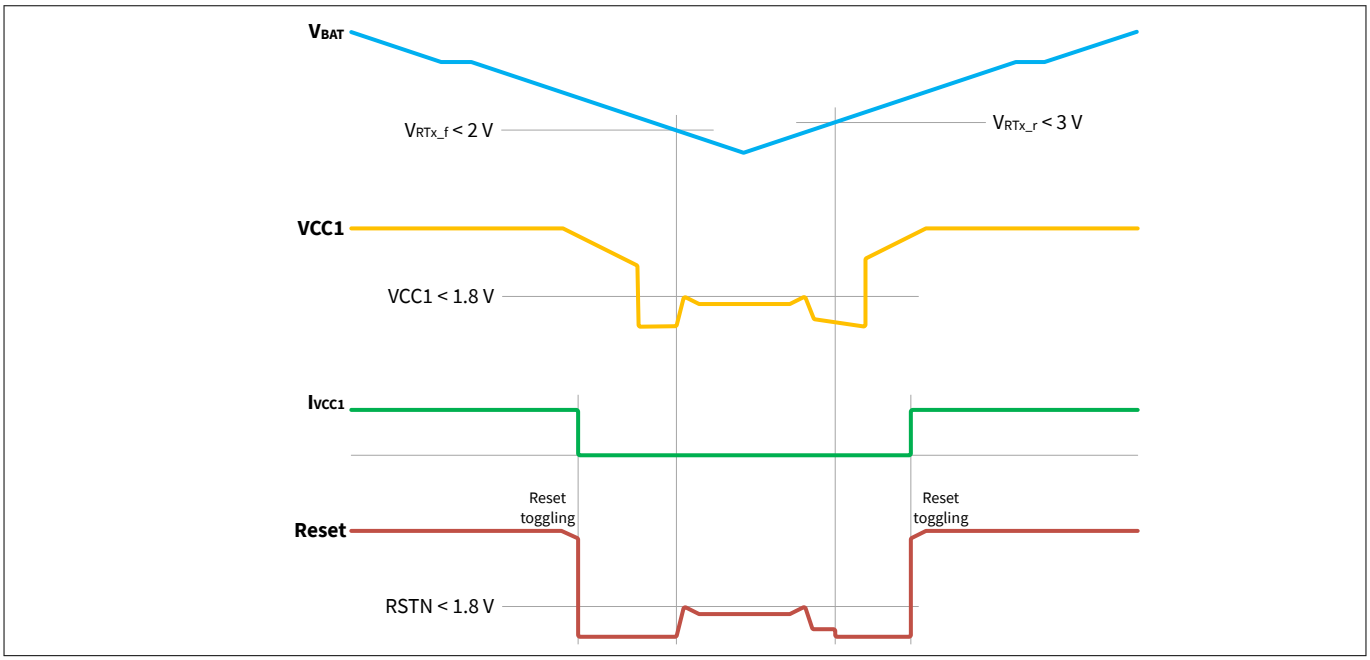


Figure 40 VCC1 undervoltage reset toggling at low V_S, expected system behavior

8 Pin FMEA

8.1 Abstract

Note: The following information shall be considered as a basis for an FMEA on application level. It is not a description or warranty of a certain functionality, condition, or quality of the device.

The section shows the results of considerations taken during the pin FMEA. In addition, the effect of the potential failure on the Fail Output (FO) function is stated.

The devices of the MCP+ SBC family covered by this Pin FMEA are listed below:

- TLE9278BQX
- TLE9278-3BQX
- TLE9278BQX V33
- TLE9278-3BQX V33

Note: If the NC pin is left floating, it can be ignored in the FMEA (internally not bonded).

8.2 Introduction

8.2.1 General information about FMEA

A failure modes and effects analysis (FMEA) is a procedure in operations management for the analysis of potential failure modes within a system, for classification by severity or determination of the effect of failures on the system.

Failure modes are any errors or defects in a process, design, or item, and can be potential or actual. Effects analysis refers to studying the consequences of those failures.

8.2.2 Implementation

In an FMEA, failures are usually prioritized according to how serious their consequences are, how frequently they occur and how easily they can be detected. The purpose of the FMEA is to take actions to eliminate or reduce failures, starting with the highest-priority ones. It may be used to evaluate risk management priorities for mitigating known threat vulnerabilities.

This document is intended to provide a basis for an application-level FMEA at the customer side. A quantification on the severity, occurrence and detection levels is not given and needs to be done by the developer for each application individually.

8.3 Classification of Failure Effects

Table 6 Classes of Failure Effects

Class	Failure Effects
A	Damage to device affects application functionality
B	No damage to device, but thermal damage must be considered
C	No damage to device, but can affect application functionality

Table 6 Classes of Failure Effects (continued)

Class	Failure Effects
D	No damage to device, and no affect to application functionality

8.4 Pin FMEA table

Table 7 Potential Failure Mode and Effects Analysis

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
1	CANH0	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible	FO unchanged	C
		Pin shorted to VS	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to neighbor pin (CANL0)	No CAN communication possible	FO unchanged	C
2	CANL0	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VS	No CAN communication possible	FO unchanged	C
		Pin shorted to neighbor pin (GNDCAN)	CAN communication disturbed and generates EMC	FO unchanged	C
3	GNDCAN	Pin open	Ground connection over pin 9	FO unchanged	C
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Not functional	B
		Pin shorted to neighbor pin (CANL1)	CAN communication disturbed and generates EMC	FO unchanged	C
3,9	GNDCAN	Both pins open	No low ohmic ground for CAN. Ground connection over substrate contacts and antiparallel diodes, increased EM emission and disturbance of other functions possible.	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
4	CANL1	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VS	No CAN communication possible	FO unchanged	C
		Pin shorted to neighbor pin (CANH1)	No CAN communication possible	FO unchanged	C
5	CANH1	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible	FO unchanged	C
		Pin shorted to VS	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to neighbor pin (GND)	No CAN communication possible	FO unchanged	C
6	GND	Pin open	Disturbance or parameter shift possible due to parasitic metal resistance	FO unchanged	C
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Not functional	B
		Pin shorted to neighbor pin (CANH2)	No CAN communication possible	FO unchanged	C
7	CANH2	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible	FO unchanged	C
		Pin shorted to VS	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to neighbor pin (CANL2)	No CAN communication possible	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
8	CANL2	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VS	No CAN communication possible	FO unchanged	C
		Pin shorted to neighbor pin (GNDCAN)	CAN communication disturbed and generates EMC	FO unchanged	C
9	GNDCAN	Pin open	Ground connection over pin 3	FO unchanged	C
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to neighbor pin (CANL3)	CAN communication disturbed and generates EMC	FO unchanged	C
3,9	GNDCAN	Both pins open	No low ohmic ground for CAN. Ground connection over substrate contacts and antiparallel diodes, increased EM emission and disturbance of other functions possible.	FO unchanged	C
10	CANL3	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VS	No CAN communication possible	FO unchanged	C
		Pin shorted to neighbor pin (CANH3)	No CAN communication possible	FO unchanged	C
11	CANH3	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible	FO unchanged	C
		Pin shorted to VS	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to neighbor pin (PCFG)	No CAN communication possible when PCFG = GND	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
12	PCFG)	Pin open	Normal application case	FO unchanged	D
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (TXDCAN0); the pins are not real neighbors	No CAN communication possible, TXD timeout failure shown on SPI	FO unchanged	C
13	TXDCAN0	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, TXD timeout failure shown on SPI	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (RXDCAN0)	No CAN communication possible	FO unchanged	C
14	RXDCAN0	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, large pin current	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (TXDCAN1)	No CAN0 communication possible, CAN1 communication may be disturbed depending on strength of TDXCAN driver in µC	FO unchanged	C
15	TXDCAN1	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, TXD timeout failure shown on SPI	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (RXDCAN1)	No CAN communication possible	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
16	RXDCAN1	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, large pin current	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (TXDCAN2)	No CAN1 communication possible, CAN2 communication may be disturbed depending on strength of TDXCAN driver in µC	FO unchanged	C
17	TXDCAN2	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, TXD timeout failure shown on SPI	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (RXDCAN2)	No CAN communication possible	FO unchanged	C
18	RXDCAN2	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, large pin current	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (VCAN)	No CAN2 communication possible	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
19	VCAN	Pin open	CAN is not supplied, no CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN is not supplied, no CAN communication possible, large current flowing on PCB	FO activated in case connected to VIO, otherwise FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (TXDCAN3)	No CAN3 communication possible	FO unchanged	C
20	TXDCAN3	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, TXD timeout failure shown on SPI	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (RXDCAN3)	No CAN communication possible	FO unchanged	C
21	RXDCAN3	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, large pin current	FO unchanged	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (VCC1)	No CAN communication possible	FO unchanged	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
22	VCC1	Pin open	Load may be destroyed due to high voltage from uncontrolled Buck operation. SBC can be destroyed if VCC1 connected to VIO.	FO activated in case VCC1 connected to VIO, otherwise FO unchanged	A
		Pin shorted to GND	Load not supplied, large current flowing (limited internally)	FO activated in case VCC1 connected to VIO	B
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (VIO)	Large current may flow on PCB when when VIO is set to 3.3V and PCFG=GND, µC may be destroyed. Nominal operation if PCFG open in 5V or 3.3 variant (PCFG not relevant)	FO unchanged	B
23	VIO	Pin open	IO pins not supplied, application not working	FO activated	C
		Pin shorted to GND	µC not supplied, application not working, large current flowing (limited internally)	FO activated	B
		Pin shorted to VS	Destruction of pin (and possibly of the connected µC)	Not functional	A
		Pin shorted to neighbor pin (RTSN)	No reset is generated, large pin current	FO activated	B
24	RTSN	Pin open	The reset signal does not reach the µC	FO unchanged	C
		Pin shorted to GND	Always reset for µC, application not working	FO unchanged	C
		Pin shorted to VS	Destruction of pin (and possibly of the connected µC)	Not functional	A
		Pin shorted to neighbor pin (INTN); the pins are not real neighbors	Each interrupt creates reset of the µC	FO unchanged. Depending on startup time of µC, a watchdog trigger can be missed which leads to fail-safe mode (FO active).	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
25	INTN	Pin open	The interrupt signal does not reach the µC	FO unchanged	C
		Pin shorted to GND	Permanent INTN low signaled to the µC	FO unchanged	C
		Pin shorted to VS	Destruction of pin (and possibly of the connected µC)	Not functional	A
		Pin shorted to neighbor pin (GNDBACK)	No wake-up is shown, large pin current	FO unchanged	B
26	GNDBACK	Pin open	Freewheeling over ESD diode (will probably be destroyed)	FO unchanged	A
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to neighbor pin (BCKSW)	µC not supplied, application not working, large current flowing (limited internally)	FO activated	B
27	BCKSW	Pin open	µC not supplied, application not working	FO unchanged	C
		Pin shorted to GND	µC not supplied, application not working, large current flowing (limited internally)	FO activated in case VCC1 connected to VIO, otherwise FO unchanged	B
		Pin shorted to VS	µC may be destroyed due to high voltage, large current flowing (limited internally)	FO activated in case VCC1 connected to VIO, otherwise FO unchanged	B
		Pin shorted to neighbor pin (n.c.)	No effect	FO unchanged	D
29	VS	Pin open	Chip only supplied by one bond wire, fusing of remaining bond wire possible	FO unchanged	A
		Pin shorted to GND	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to VS	Normal application case	FO unchanged	D

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
30	VS	Pin open	Chip only supplied by one bond wire, fusing of remaining bond wire possible	FO unchanged	A
		Pin shorted to GND	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to VS	Normal application case	FO unchanged	D
		Pin shorted to neighbor pin (n.c.)	No effect	FO unchanged	D
32	GNDBST	Pin open	Boost only connected to GND by one pin or bond wire, fusing of remaining bond wires possible	FO unchanged	A
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B
33	GNDBST	Pin open	Boost only connected to GND by one pin or bond wire, fusing of remaining bond wires possible	FO unchanged	A
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to neighbor pin (n.c.)	No effect	FO unchanged	D
35	BSTD	Pin open	Boost not working	FO unchanged	C
		Pin shorted to GND	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to VS	Boost not working	FO unchanged	C
36	BSTD	Pin open	Boost not working	FO unchanged	C
		Pin shorted to GND	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to VS	Boost not working	FO unchanged	C
		Pin shorted to neighbor pin (CSN); the pins are not real neighbors	Destruction of pin (and possibly of the connected µC)	Not functional	A

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
37	CSN	Pin open	SPI failure	FO activated after WDT failure	C
		Pin shorted to GND	SPI failure	FO activated after WDT failure	C
		Pin shorted to VS	Destruction of pin, additional failures possible	Not functional	A
		Pin shorted to neighbor pin (SDO)	SPI failure or wrong SPI output to µC	FO activated after WDT failure	C
38	SDO	Pin open	Wrong SPI output to µC	FO activated after WDT failure	C
		Pin shorted to GND	Wrong SPI output to µC	FO activated after WDT failure	C
		Pin shorted to VS	Destruction of pin, additional failures possible	FO activated after WDT failure	A
		Pin shorted to neighbor pin (SDI)	SPI failure or wrong SPI output	FO activated after WDT failure	C
39	SDI	Pin open	SPI failure	FO activated after WDT failure	C
		Pin shorted to GND	SPI failure	FO activated after WDT failure	C
		Pin shorted to VS	Destruction of pin, additional failures possible	FO activated after WDT failure	A
		Pin shorted to neighbor pin (CLK)	SPI failure	FO activated after WDT failure	C
40	CLK	Pin open	SPI failure	FO activated after WDT failure	C
		Pin shorted to GND	SPI failure	FO activated after WDT failure	C
		Pin shorted to VS	Destruction of pin, additional failures possible	FO activated after WDT failure	A
		Pin shorted to neighbor pin (GND)	SPI failure	FO activated after WDT failure	C

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
41	GND	Pin open	Disturbance or parameter shift possible due to parasitic metal resistance	FO unchanged	C
		Pin shorted to GND	Normal application case	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to neighbor pin (WK)	No wake-up possible	FO unchanged	C
42	WK	Pin open	No wake-up possible	FO unchanged	C
		Pin shorted to GND	No wake-up possible	FO unchanged	C
		Pin shorted to VS	No wake-up possible	FO unchanged	C
		Pin shorted to neighbor pin (VBSENSE)	No wake-up possible	FO unchanged	C
43	VBSENSE	Pin open	Low voltage always detected on VBSENSE	FO unchanged	C
		Pin shorted to GND	In case of a nominal application (like DS chapter 14) where VBAT=VSENSE with input filter (R and C), low battery voltage always detected	FO unchanged	C
		Pin shorted to VS	Low voltage never detected on VBSENSE before VS drops	FO unchanged	C
		Pin shorted to neighbor pin (VEXTIN)	Low voltage maybe never detected on VBSENSE before VS drops	FO unchanged	C
44	VEXTIN	Pin open	VEXT load not supplied	FO activated if VIO is connected to VEXT, otherwise FO unchanged	C
		Pin shorted to GND	VEXT load not supplied	FO activated if VIO is connected to VEXT, otherwise FO unchanged	C
		Pin shorted to VS	Normal operation	FO unchanged	D
		Pin shorted to neighbor pin (VEXTSH)	VEXT current limitation not working,external PNP not protected	FO unchanged	B

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
45	VEXTSH	Pin open	VEXT current limitation always active, VEXT load not supplied, SPI status bits VEXT_OC and VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	C
		Pin shorted to GND	VEXT load no supplied, large current flowing (not limited), SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
		Pin shorted to VS	VEXT current limitation not working,external PNP not protected	FO unchanged	B
		Pin shorted to neighbor pin (VEXTB)	VEXT load no supplied, large current flowing into pin, SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
46	VEXTB	Pin open	VEXT load no supplied, SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	C
		Pin shorted to GND	VEXT load no supplied, large current flowing through PNP emitter-base junction (not limited), SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
		Pin shorted to VS	VEXT load no supplied, large current flowing into pin, SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
		Pin shorted to neighbor pin (VEXTREF)	Load supplied by VEXT may be damaged by high voltage	Not functional	B

Table 7 Potential Failure Mode and Effects Analysis (continued)

Pin number	Pin name	Potential failure mode	Potential effects of failure	Effects of failure on Fail Output (FO) function	Class
47	VEXTREF	Pin open	VEXT regulator forces output voltage near to VS, load supplied by VEXT may be damaged by high voltage, SPI status bit VEXT_UV set	Not functional	B
		Pin shorted to GND	VEXT load no supplied, large current flowing (limited), SPI status bit VEXT_UV set	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
		Pin shorted to VS	Load supplied by VEXT may be damaged by high voltage	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
		Pin shorted to neighbor pin (FO/ TEST)	Load supplied by VEXT may be damaged by high voltage	FO activated if VIO is connected to VEXT, otherwise FO unchanged	B
48	FO/TEST	Pin open	FO never signaled	Not functional	C
		Pin shorted to GND	FO always signaled, SBC Development Mode active when short is present at power-up	Not functional	C
		Pin shorted to VS	FO never signaled, current flowing in case of FO activation	Not functional	C
		Pin shorted to neighbor pin (CANH0); the pins are not real neighbors	CAN0 control circuits connected to FO CAN0 communication disturbed and generates EMI	Not functional	C
EP	Exposed pad	Pin open	Worse thermal behavior, thermal shutdown with smaller dissipated power	FO activated by thermal shutdown	C
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	FO unchanged	B

Revision History

Revision	Date	Changes
1.0	2019-04-12	Initial release

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