LinearFET 40V – 12V PDU switch
Board introduction

IFAG ATV MOS
30.03.2026

OptiMOS™ 7 - 40V – LinearFET

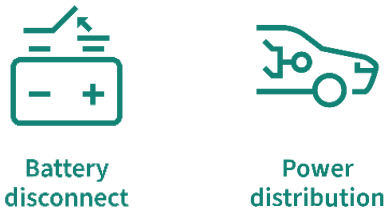
Lead product

Group	Product	V_{DS}	max $R_{DS(on)}$ at V_{GS} = 12 V [mΩ]	I_D (DC current) [A]	I_D (chip limitation) [A]	R_{thJC} [K/W]	package
1	IAUAN04S7S004	40 V	0.43	280 A	536	0.63	sTOLL

Old sales-name: IAUAN04S7N004L

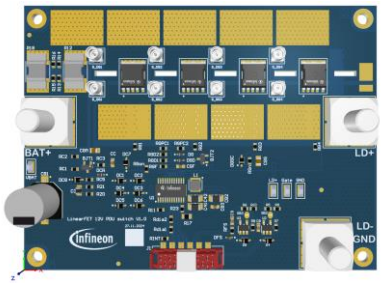
- **The best of 2 MOSFET types in 1 device:**
  - **Very low $R_{DS(on)}$** OptiMOS™ 7 Technology for steady state operation
  - **Significantly increased SOA** compared to standard MOSFETs for linear mode operation
- **sTOLL** – robust Automotive power package
- **Excellent paralleling** characteristics
- **Perfect fit** for
  - **Capacitor charging, over-voltage clamping** – e.g. disconnect switch
  - **Board-net stabilization** (slow switching, EMC improvement) – e.g. PWM switches for heaters

Application examples:



Evaluation Board:

12V PDU single switch



sTOLL

L x W x H 7.0 x 8.0 x 2.3 mm³
Cu-Clip soldered

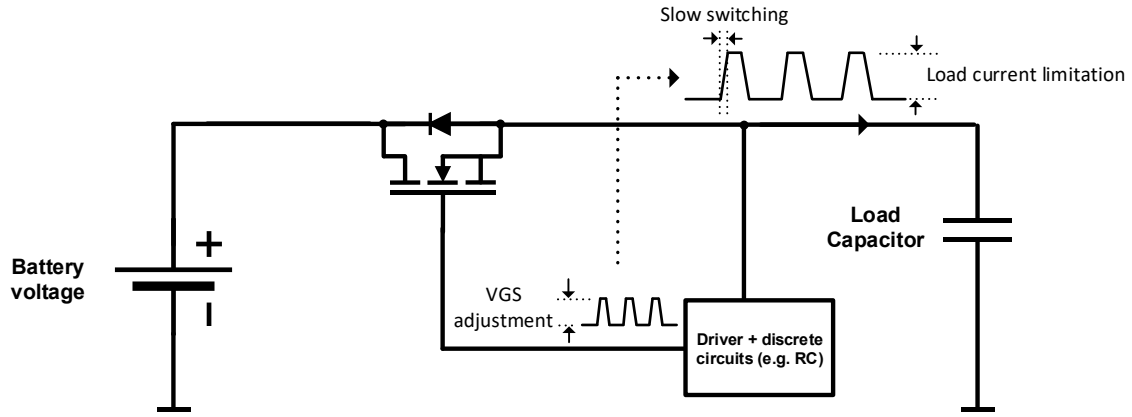
	Group 1
EES	available
ES	available
QS	Q2 2026
SOP	Q3 2026

Preliminary Information. Subject to change.

Target applications and use cases

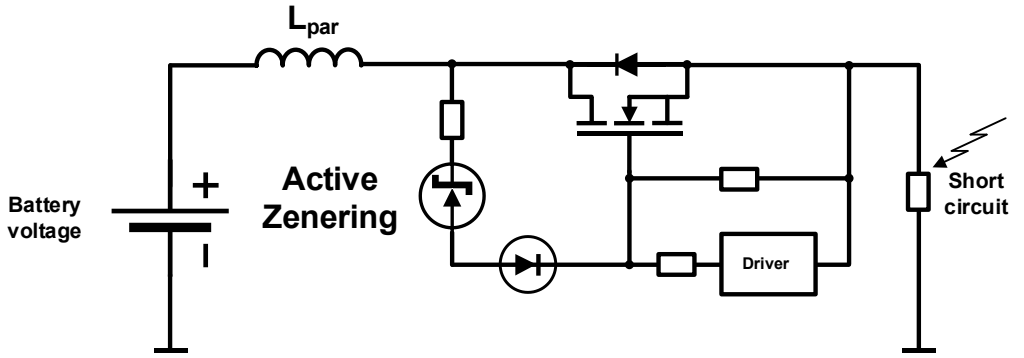
Capacitor charging

- Limit in-rush current via V_{GS} adjustment in linear mode operation.
- Pulsing to limit self-heating for large capacitors.
- Slow switching to minimize board-net voltage fluctuations and under-/overvoltage.

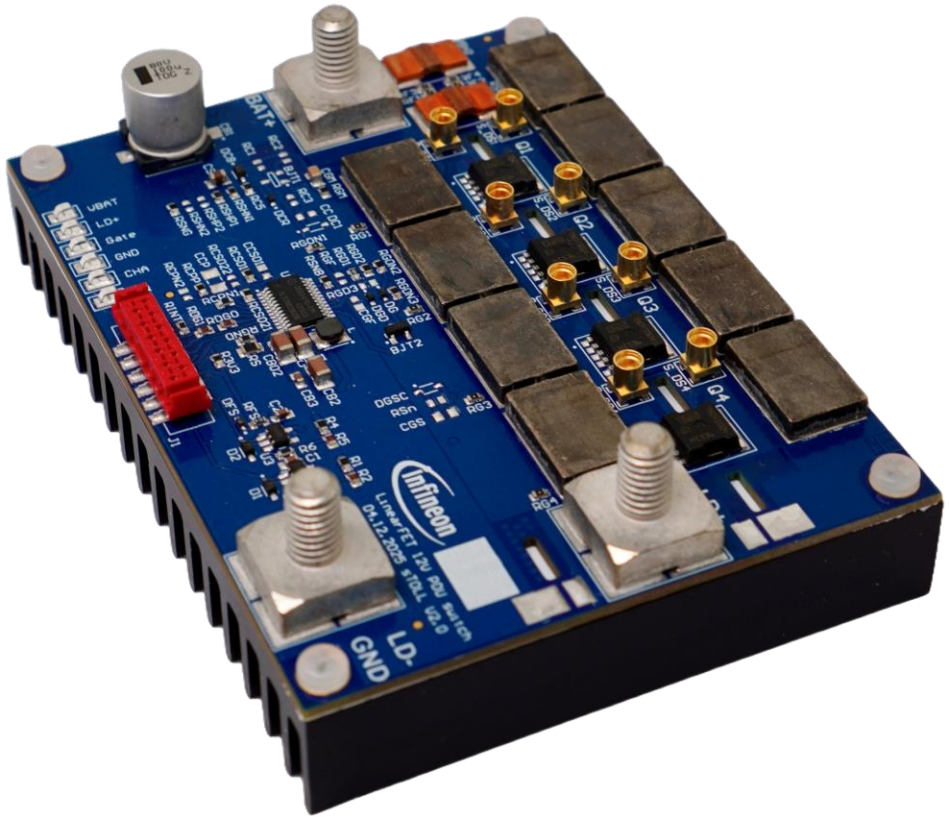


Short circuit clamping

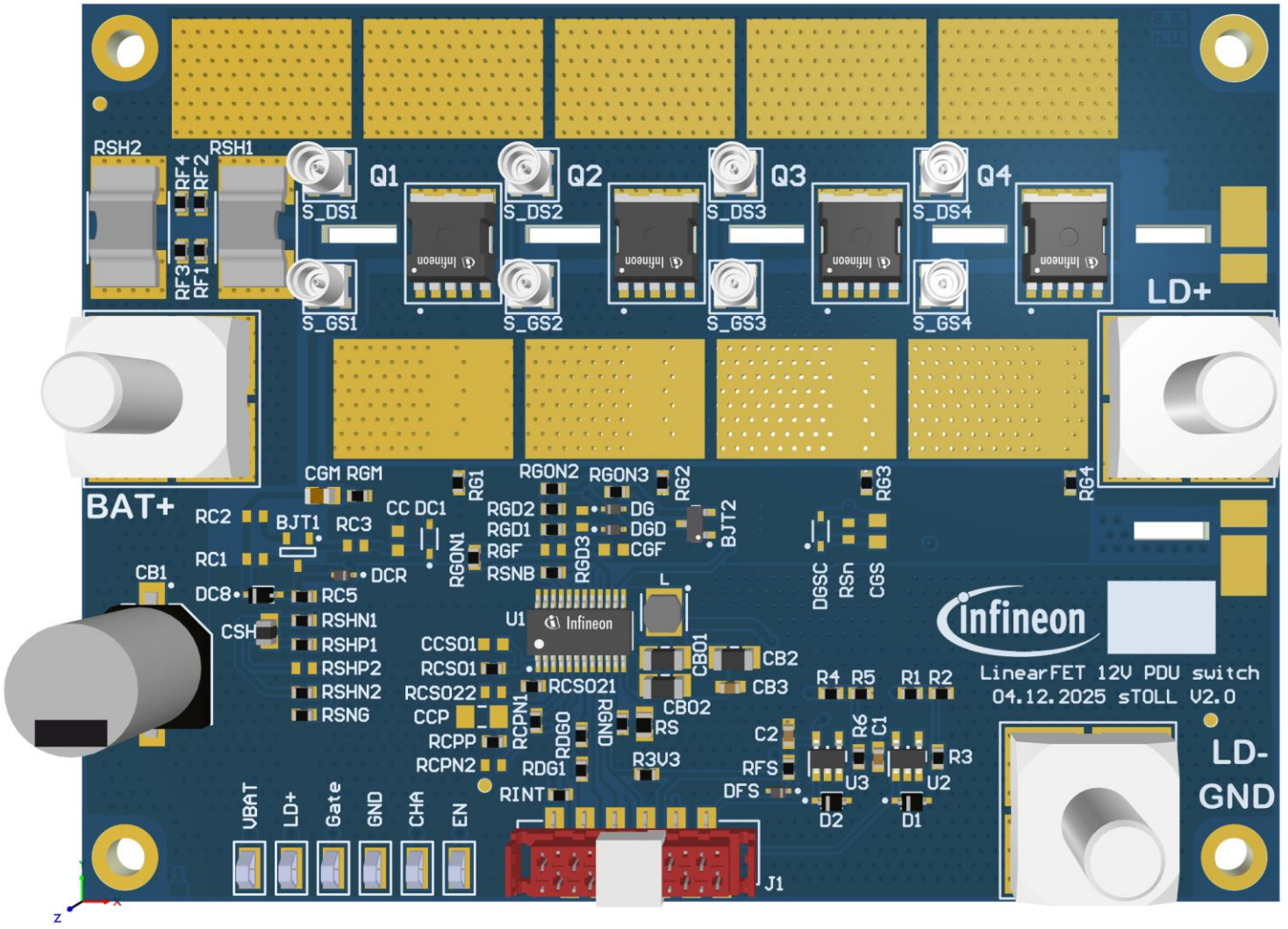
- System over-voltage protection via active clamping to limit V_{DS}.
- Avoidance of avalanche (reduced degradation).
- High energy capability due to improved SOA and enablement of paralleling in linear mode.



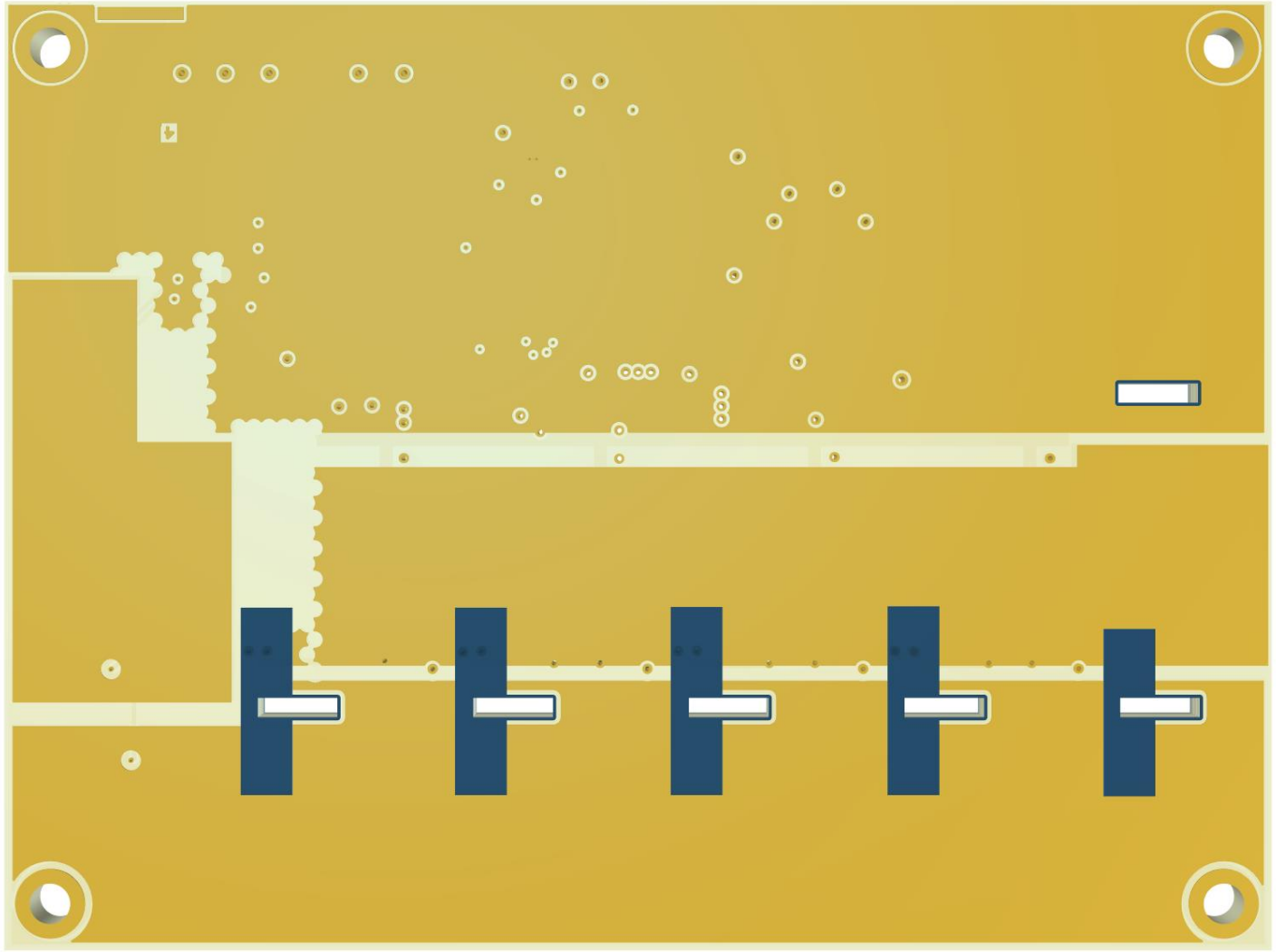
LinearFET 40V – 12V PDU switch



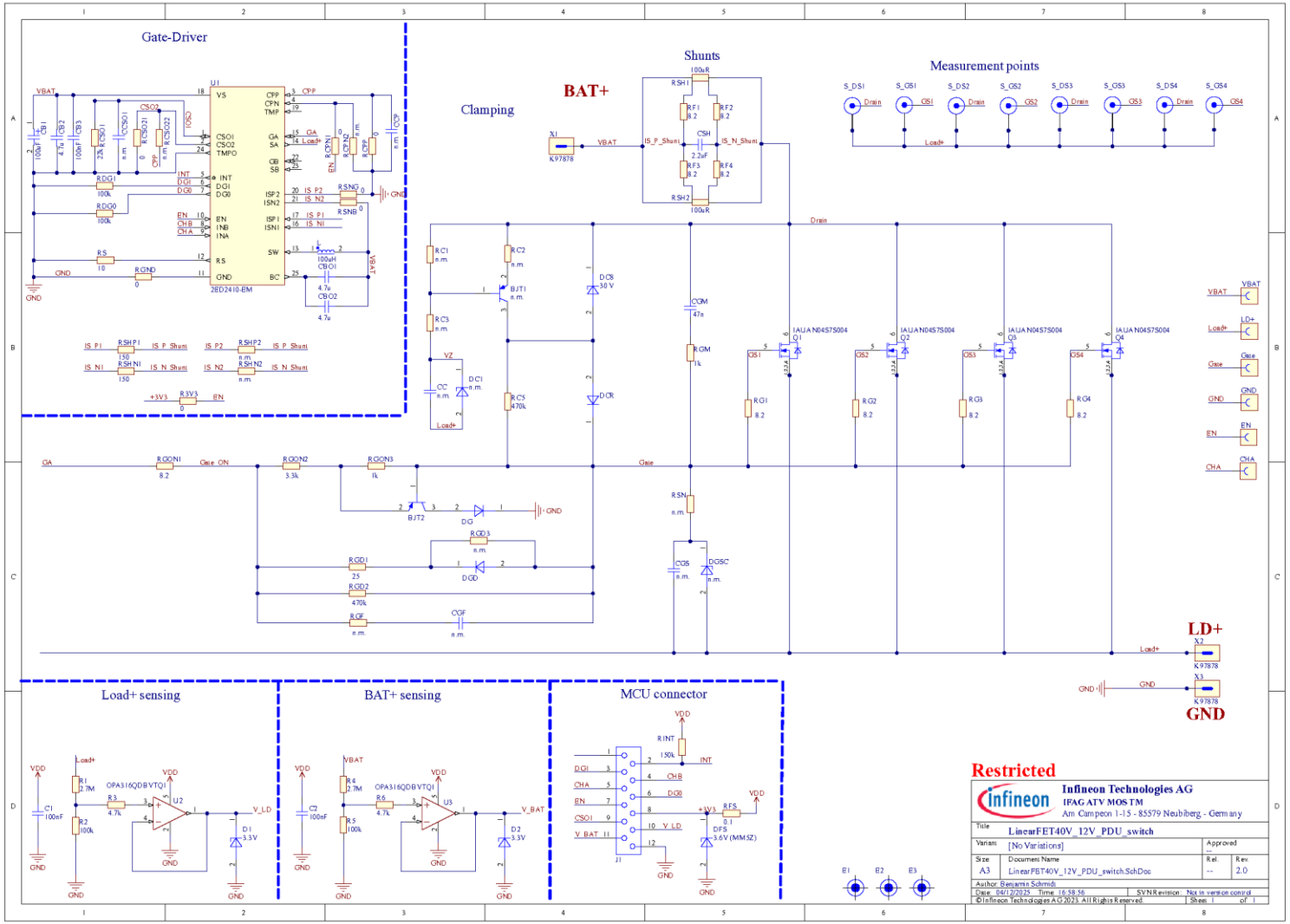
LinearFET 40V – 12V PDU switch



LinearFET 40V – 12V PDU switch

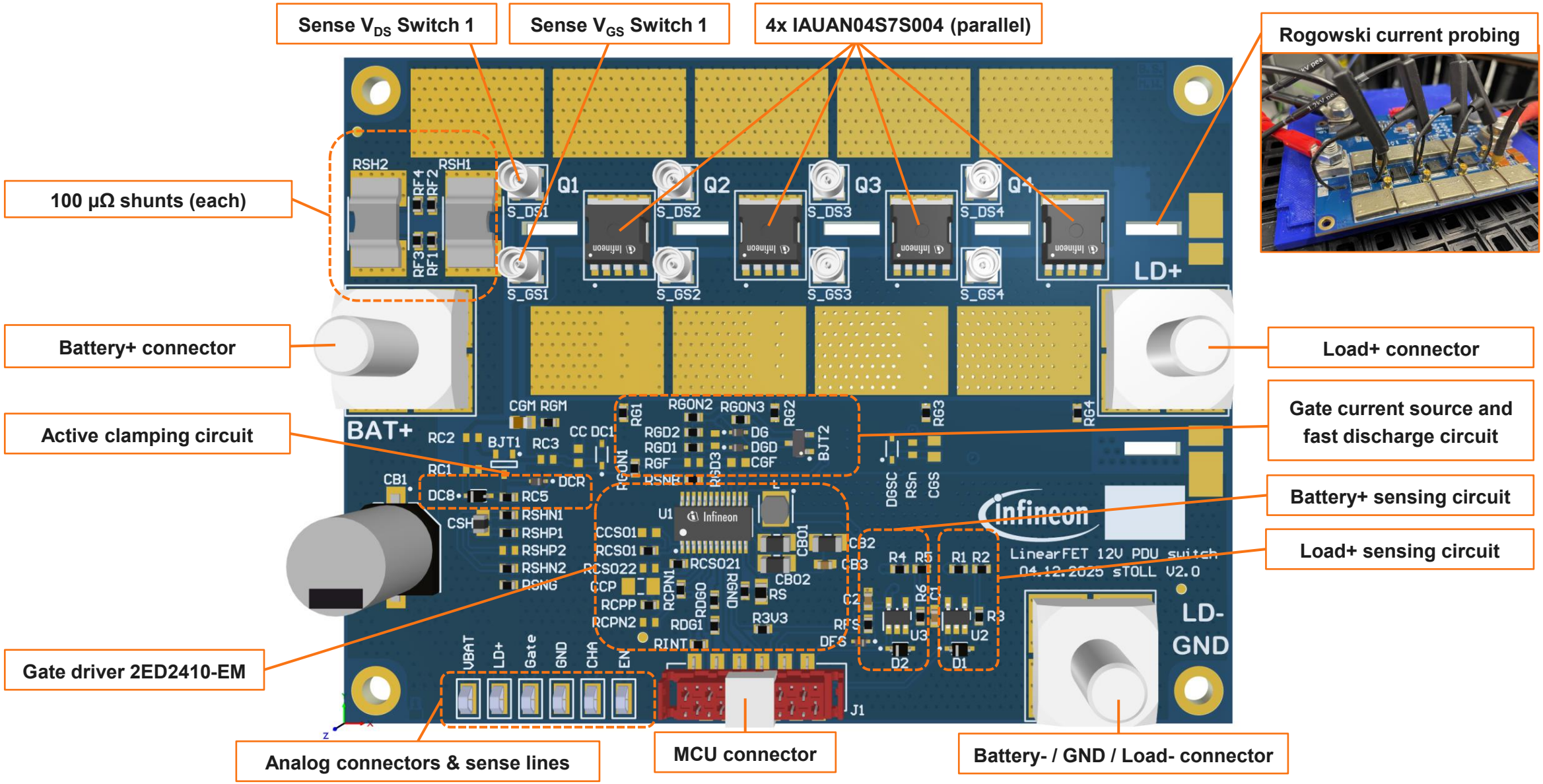


Board schematic



Bill of Materials

Board overview



Simplified schematic

Active Zener clamp circuit:

- Zener diode (30V) to clamp V_{DS} at typically 35V…40V
- Reverse diode blocks reverse current during on-state of the MOSFET (V_{GS} high)

Gate current control

- BJT circuit used as a constant gate current source:

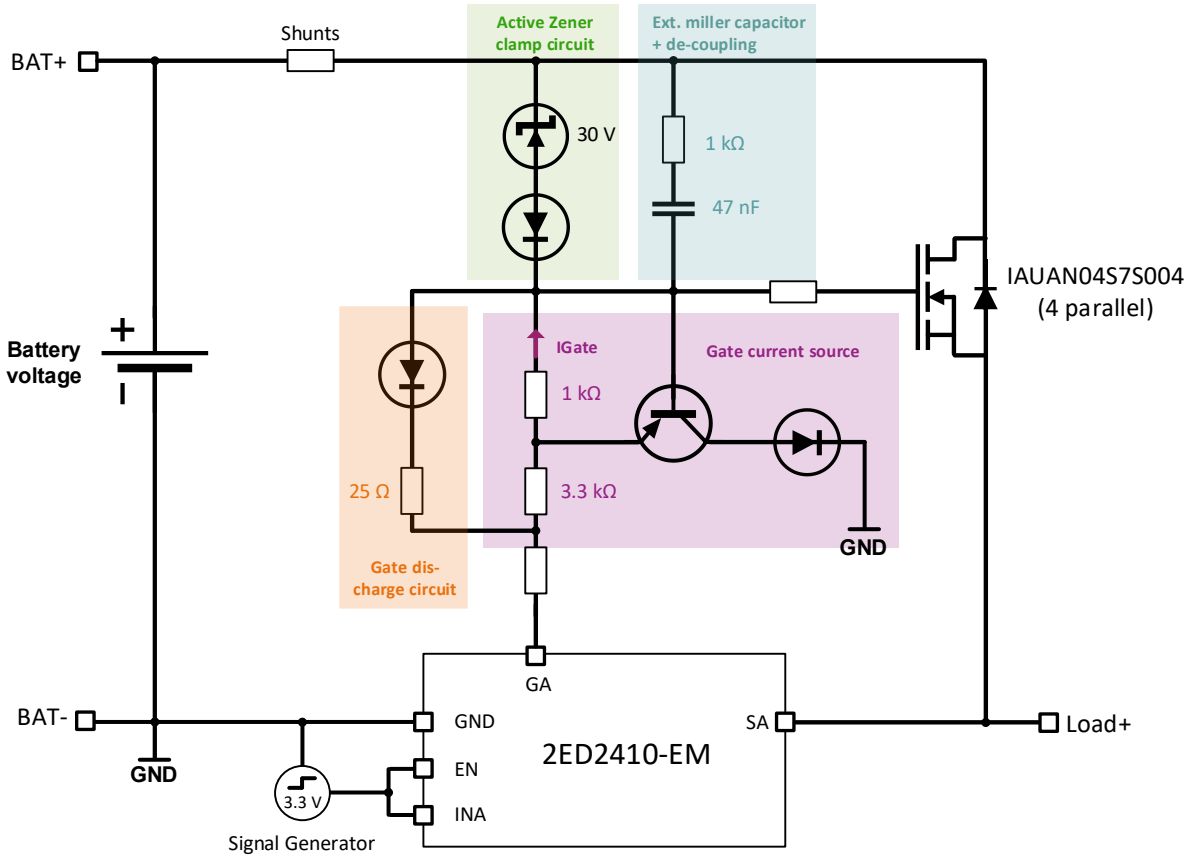
$I_{GATE} \approx \frac{V_{BE}}{1k\Omega} \approx 600\mu A$

External miller capacitor + de-coupling

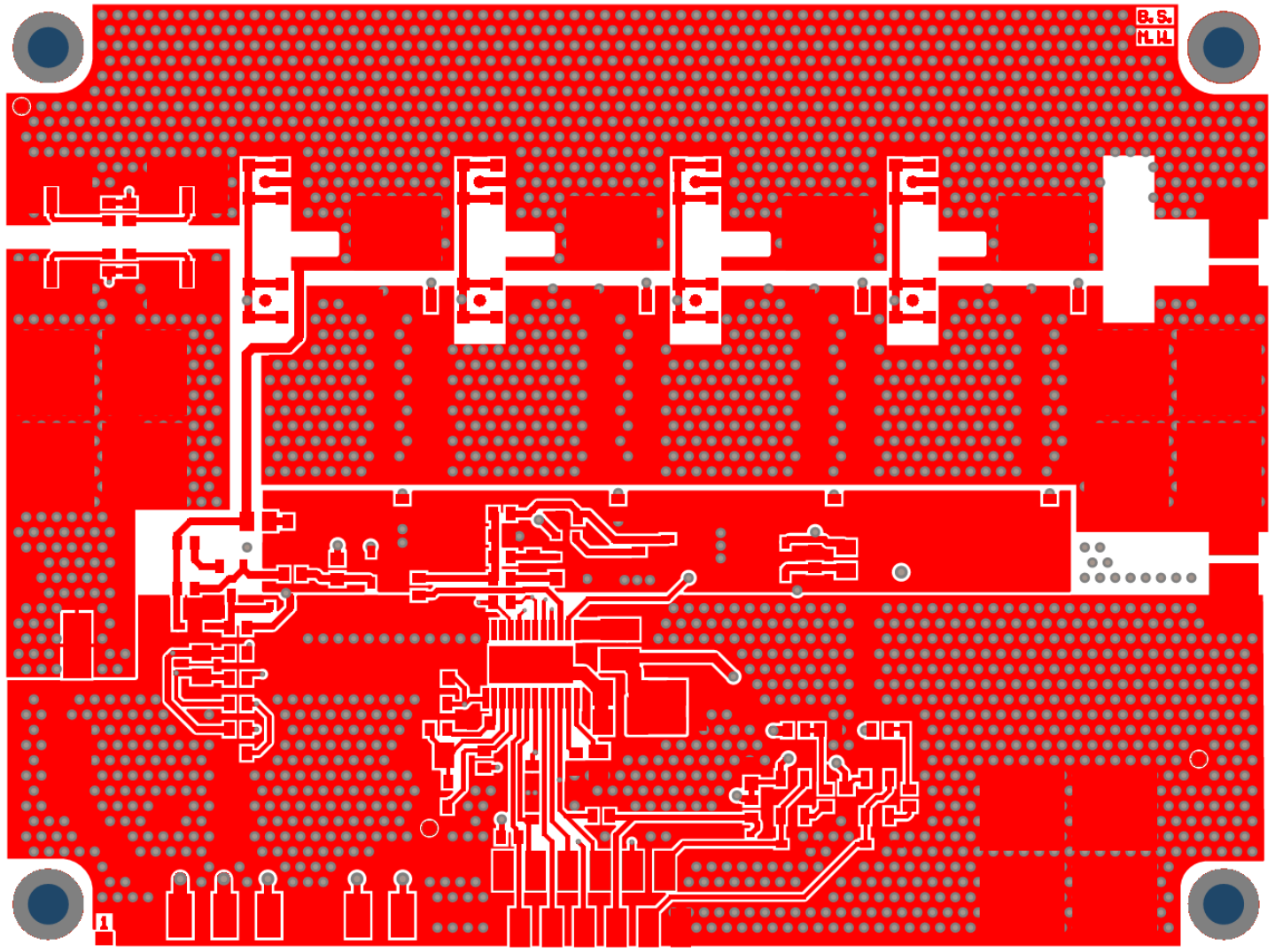
- 47 nF external miller capacitor for soft-start (10 V/ms) capacitor charging in combination with low I_{Gate}
- De-coupling series resistance reduces sensitivity towards battery voltage variation

Discharge circuit

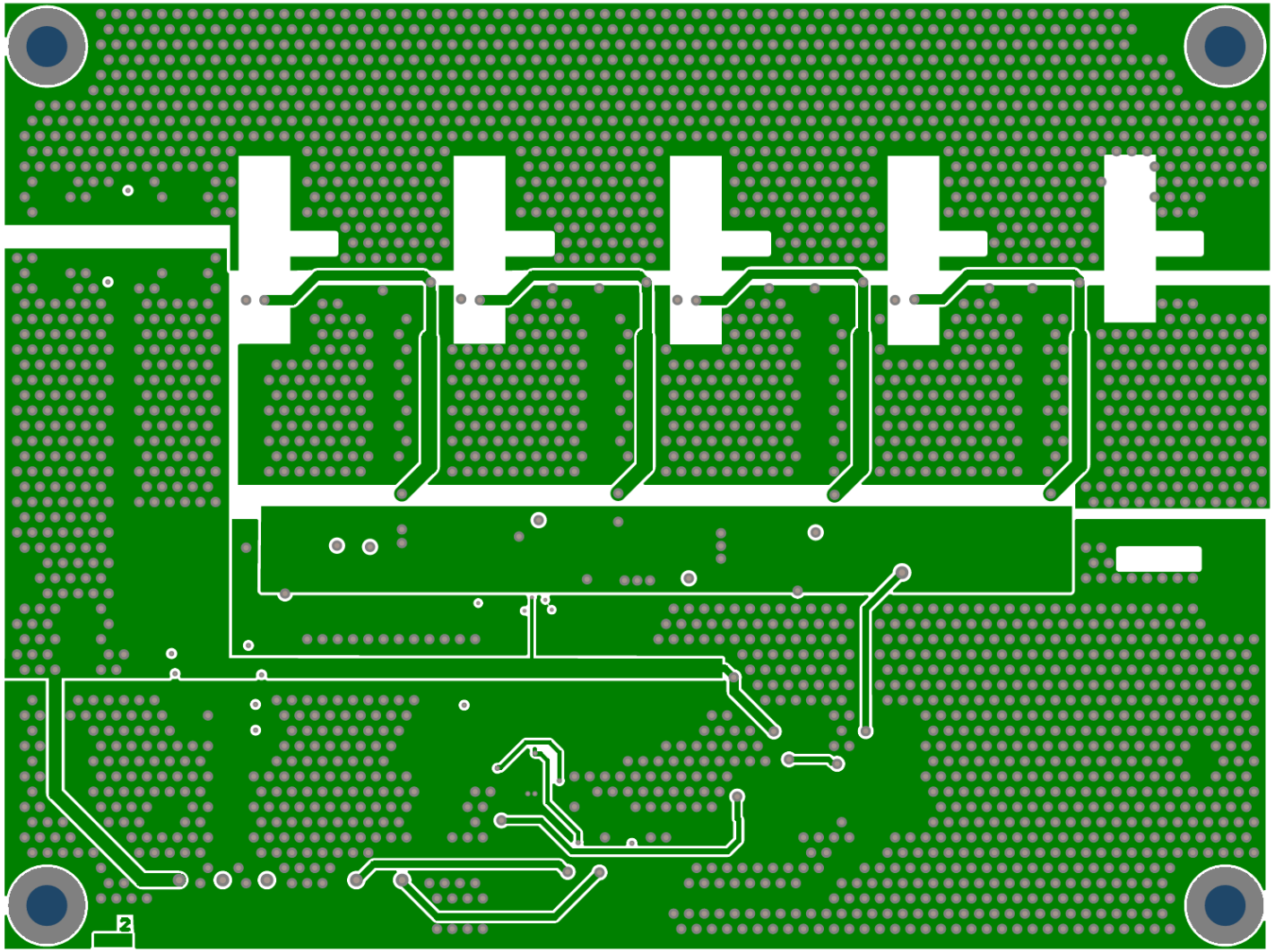
- Gate dis-charge circuit to ensure fast disconnection in case of faults such as over-current or short circuits
- Ensures pull-down of the gate in off-state via the driver active pull-down stage in case of fast battery voltage transients coupling into the gate.



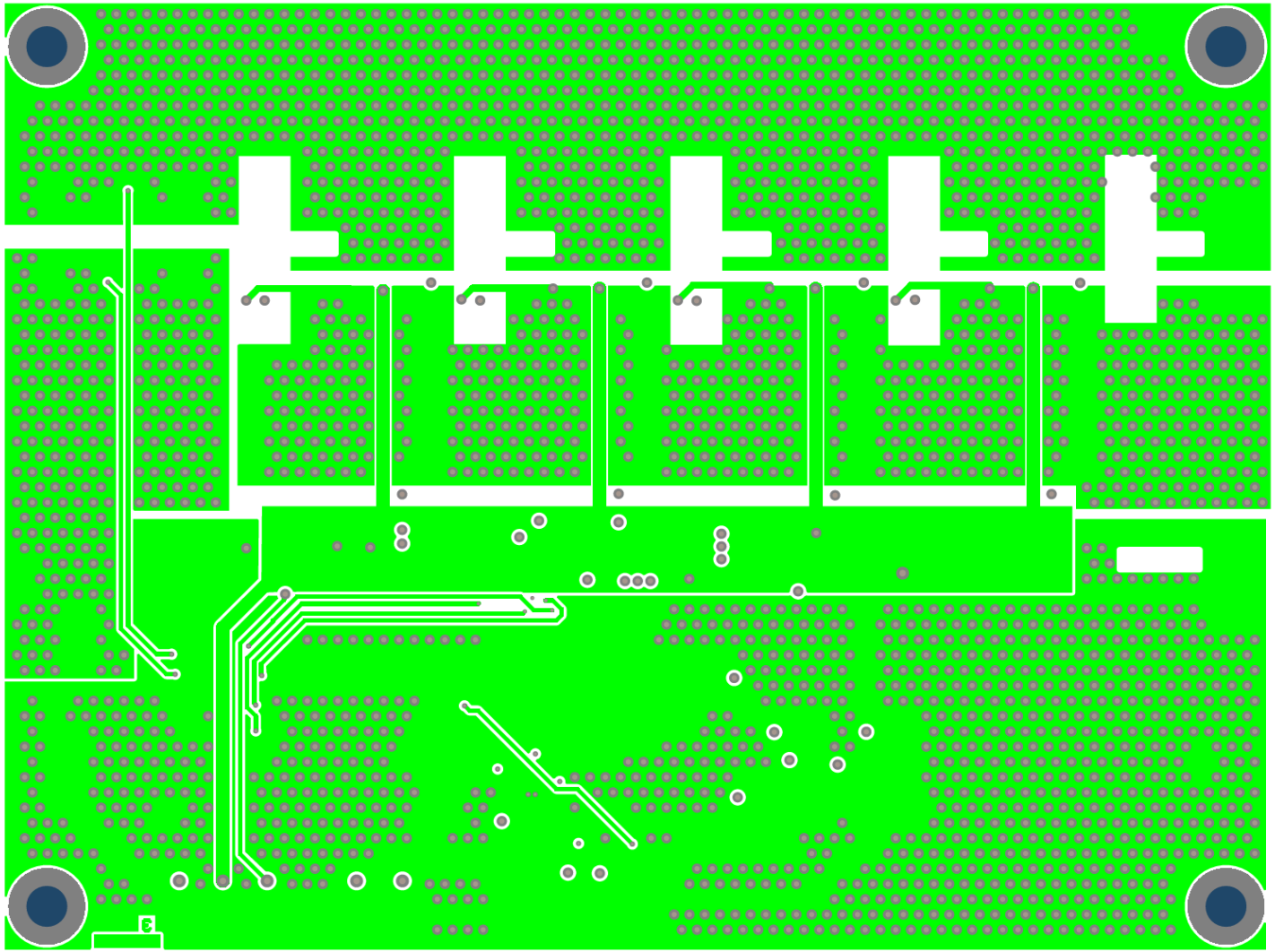
Top layer



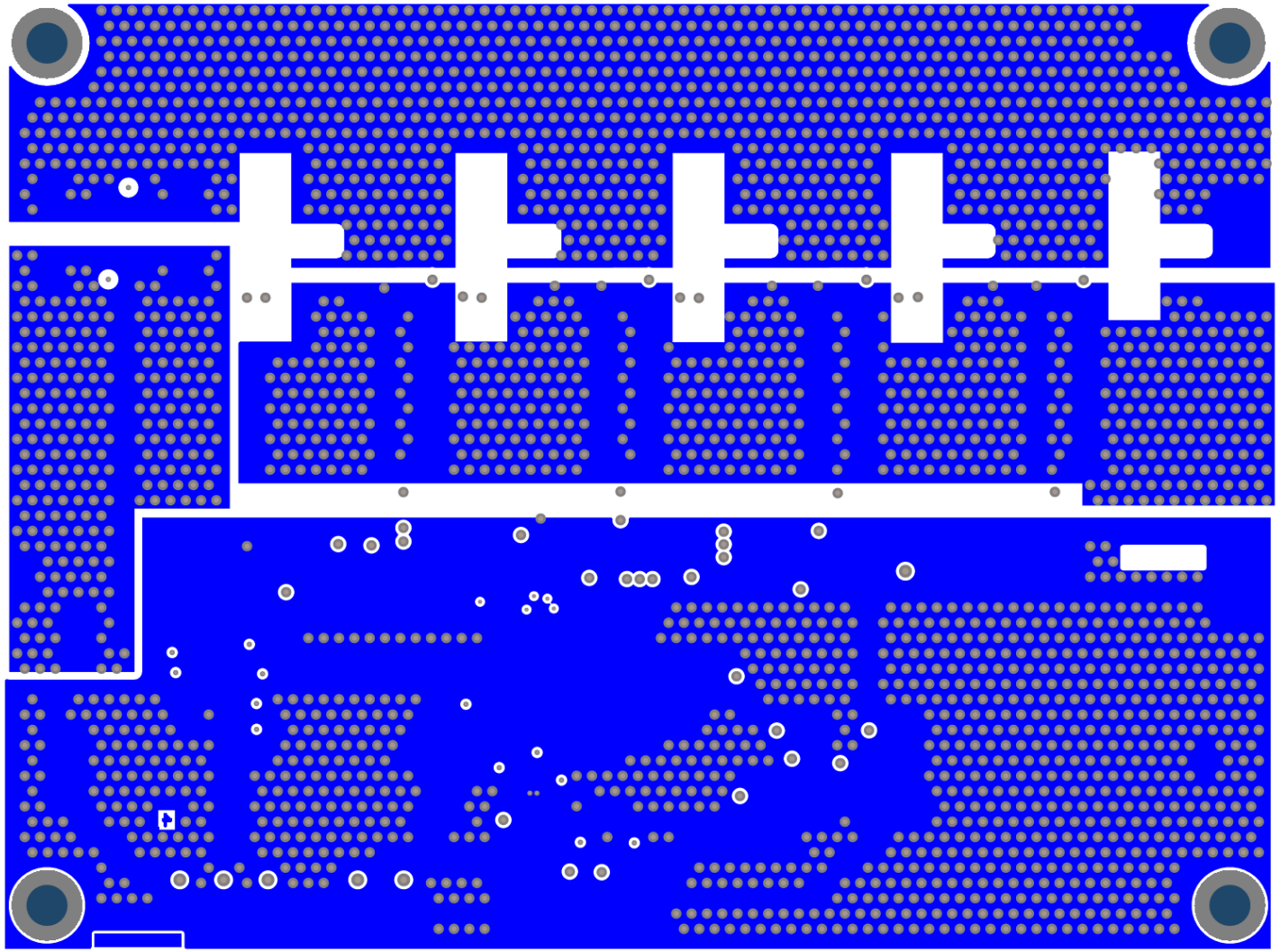
Middle layer 1



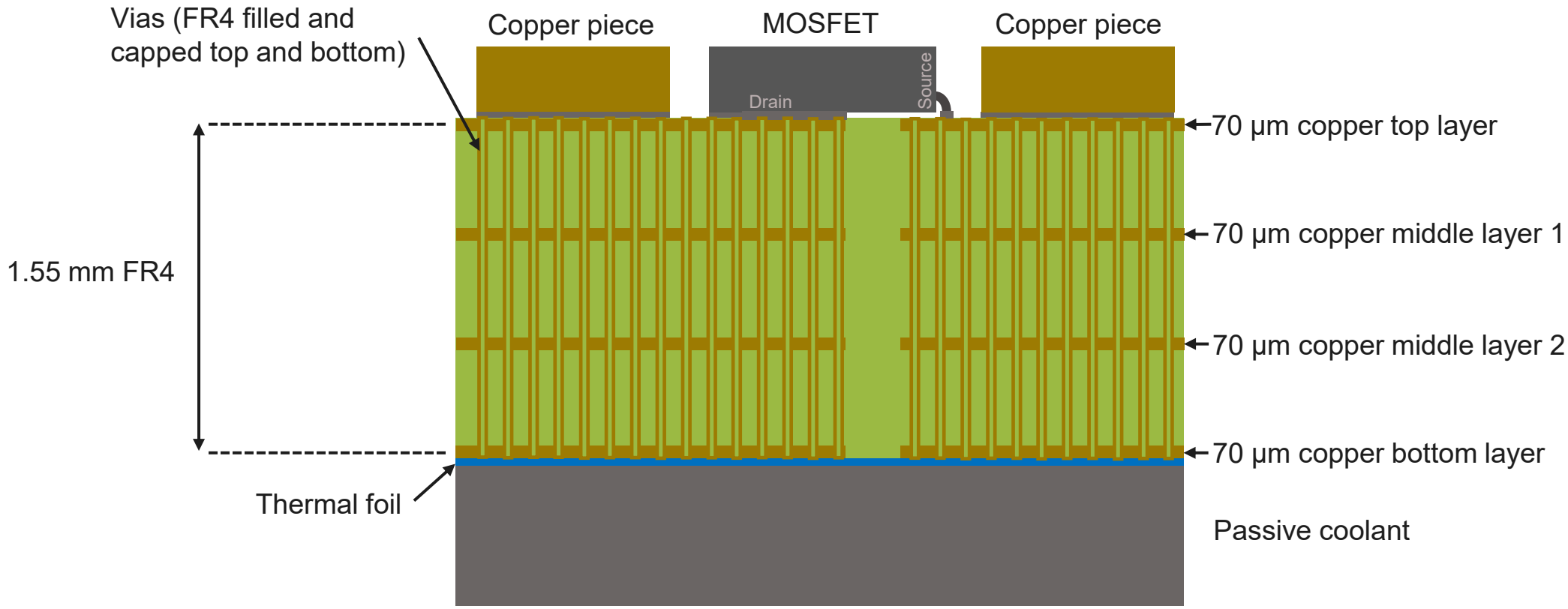
Middle layer 2



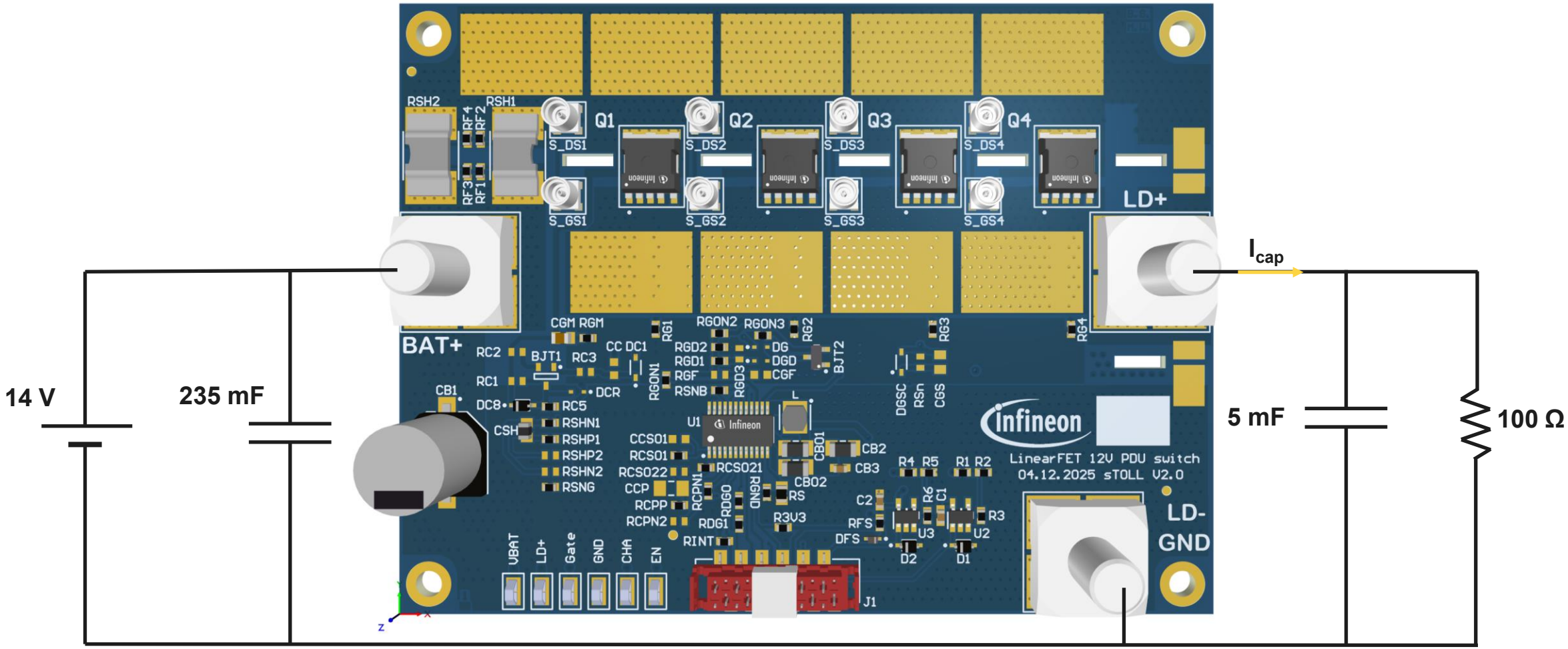
Bottom layer



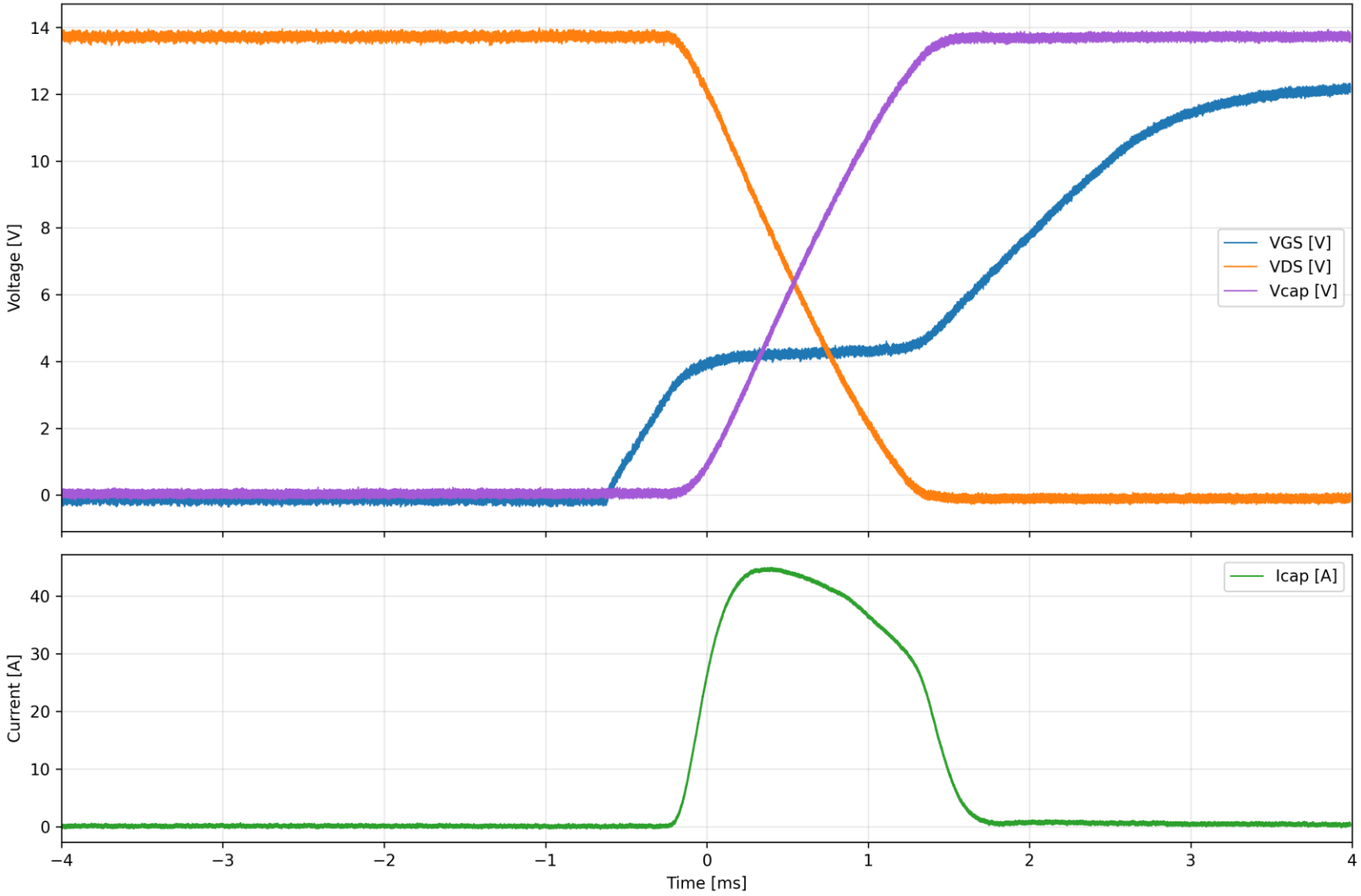
PCB stack and thermal design



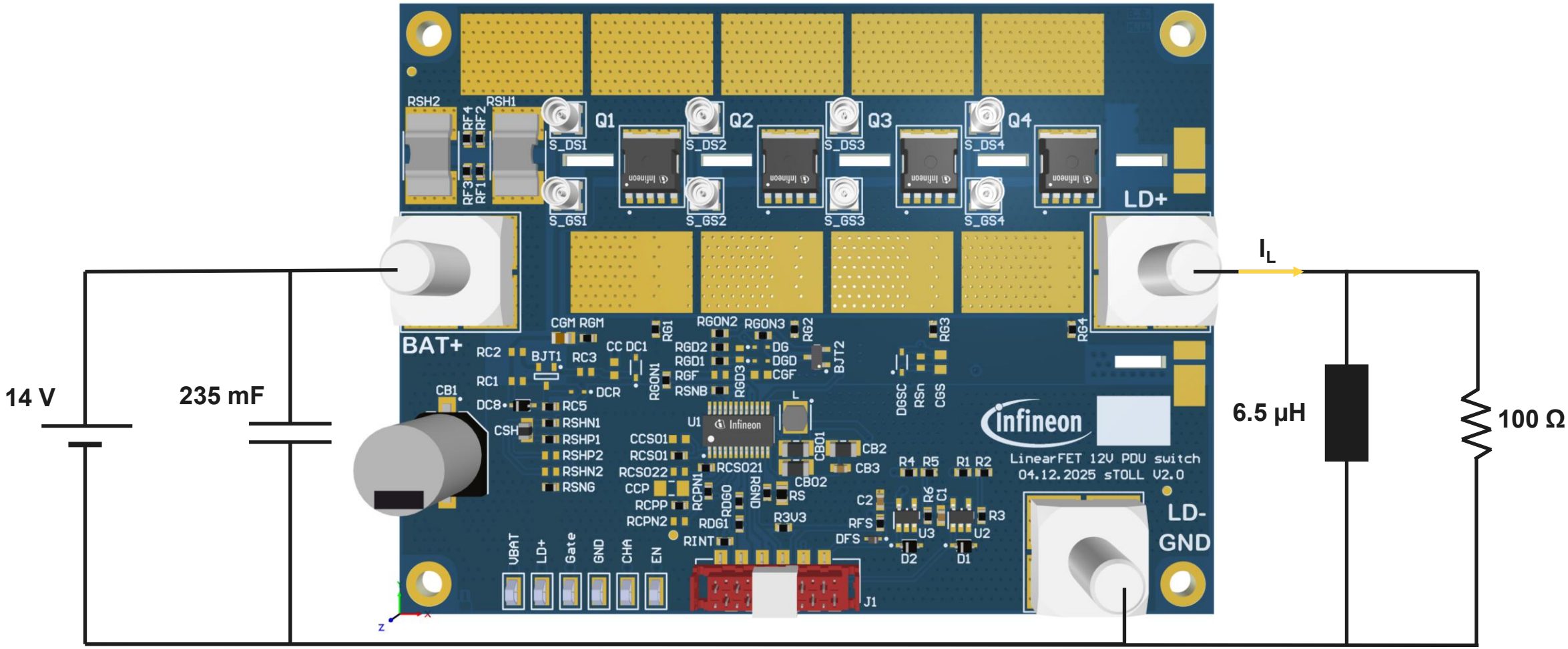
Capacitor charging – example



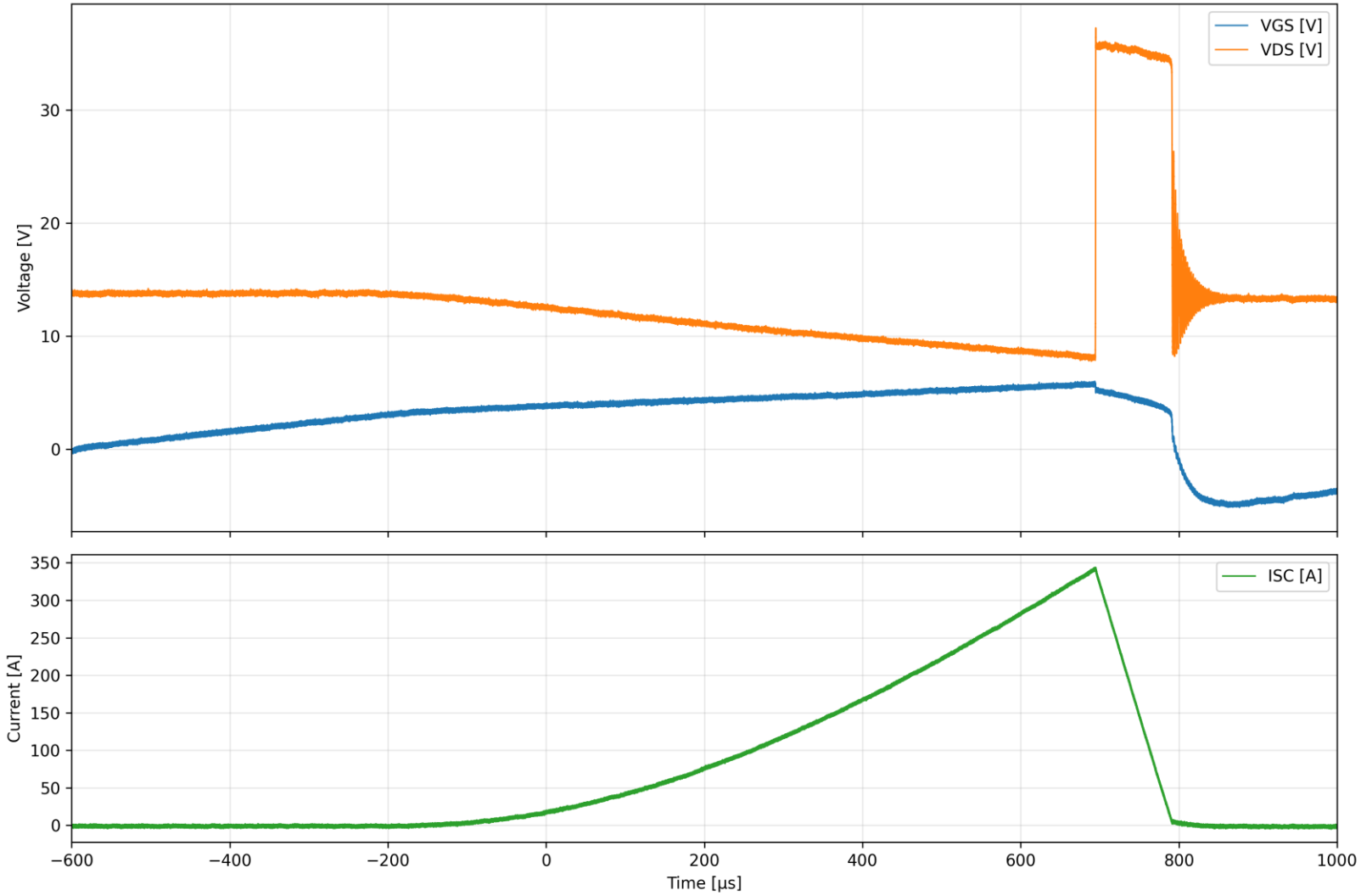
Capacitor charging – measurements



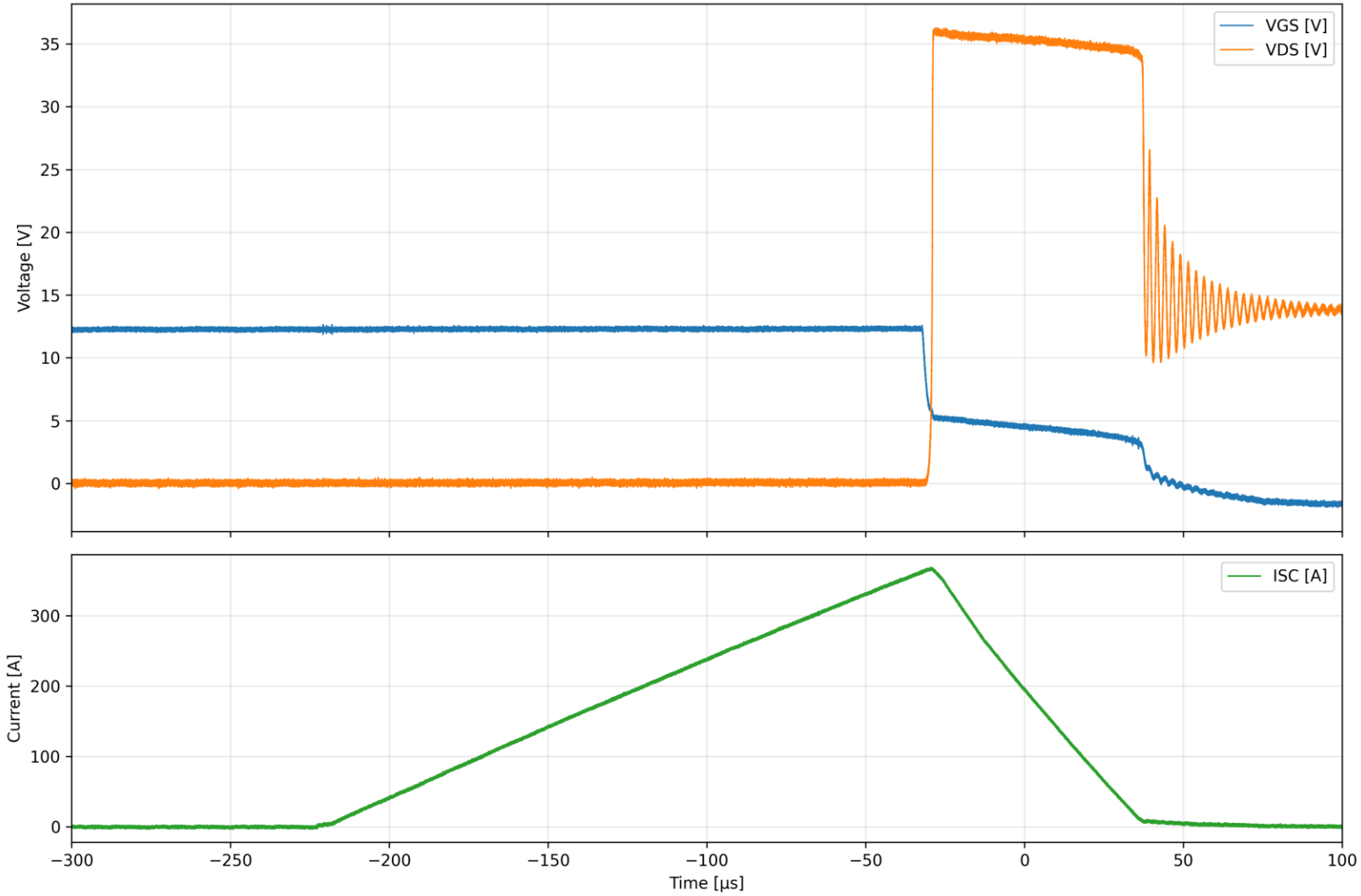
Short circuit clamping – example



Short circuit clamping (type 1) – measurements



Short circuit clamping (type 2) – measurements




Infineon