KIT_TRAVEO_T2G_B_H_MC1 Motor Control Evaluation Kit guide

About this document

About this document

The document describes the features and hardware details of the KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit, which is designed to serve as an evaluation platform for motor control applications with the TRAVEO™ T2G Body High dual-core Arm® Cortex® M7-based microcontroller. This board is a part of Infineon's motor control evaluation platform kits.

Intended audience

This document is intended for KIT_TRAVEO_T2G_B_H_MC1 users. This board is intended to be used under laboratory conditions.

Reference board/kit

Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

***Note**: Boards do not necessarily meet safety, EMI, or quality standards (e.g., UL, CE) requirements.*

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Safety precautions

Table 1	Safety precautions
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Introduction

The KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit allows for the evaluation and development of motor control applications using the TRAVEO™ T2G CYT4BF microcontroller (TRAVEO™ T2G CYT4BF).

CYT4BF is a family of TRAVEO™ T2G microcontrollers targeted at automotive systems such as high-end body-control units. CYT4BF has two Arm® Cortex®-M7 CPUs for primary processing, and an Arm® Cortex®-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting Controller Area Network with Flexible Data rate (CAN FD), Local Interconnect Network (LIN), Gigabit Ethernet, and FlexRay. TRAVEO™ T2G devices are manufactured on an advanced 40-nm process. CYT4BF incorporates a low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit includes a power stage inverter card, adapter card, BLDC motor, and TRAVEO_T2G_B_H_DC_V1 drive card featuring two potentiometers, a push button, and two user LEDs for easy interaction and visual feedback. It incorporates a USB Type-C connector for convenient USB device connectivity. Onboard debugger based on J-Link simplifies programming and debugging tasks. Additionally, it offers a Trace box and ETM header. With four hall sensor headers, four encoder headers, a mikroBUS header, and a high-density connector, it provides flexibility and expandability for sensor integration and connectivity options. The board supports operating voltages from 3.3 V to 5.0 V for TRAVEO™ T2G CYT4BF.

ModusToolbox™ is used to develop and debug TRAVEO™ T2G CYT4BF projects. It is a set of tools that enables integration of these devices into existing development methodology.

For additional information about TRAVEO™ T2G CYT4BF, see AN235305 - Getting started with TRAVEO™ T2G family MCUs in ModusToolbox™ software, which assists in creating custom designs using the Eclipse IDE for ModusToolbox™ software.

1.1 Kit contents

The kit includes the following contents:

- KIT_TRAVEO_T2G_B_H_DC_V1 motor control card
- Drive adapter card
- KIT_MOTOR_DC_250W_24V_T2G power board
- USB Type-A to USB Type-C cable
- Nanotec DB42M03 24 V BLDC motor
- 24V/1A AC/DC power adapter
- Quick start guide

1.2 Getting started

This guide aims to familiarize you with the evaluation kit.

- The Kit operation section describes the major features and functionalities such as programming, debugging, and USB-UART bridges of the KIT_TRAVEO_T2G_B_H_DC_V1 motor control card
- The Hardware section provides a detailed hardware description
- Application development using the KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit is supported in ModusToolbox™. ModusToolbox™ is a free development ecosystem that includes the Eclipse IDE for ModusToolbox™ and the TRAVEO™ T2G CYT4BF SDK along with TRAVEO™ T2G CYT4BF MCU. Using ModusToolbox™, you can enable and configure device resources, middleware libraries, write C/assembly source codes, and program or debug the device. For more information, see the ModusToolbox™ software installation guide
- Code examples are available for evaluating the KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit. These examples help you become familiar with the TRAVEO™ T2G CYT4BF MCU and create your own

designs. These examples can be accessed through the ModusToolbox™ Project Creator tool. Additionally, see Infineon code examples for ModusToolbox™ software to access these examples

1.3 Key features

The KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit features:

- An Infineon TRAVEO™ T2G CYT4BF dual-core (Arm® Cortex® M7-based) microcontroller **TRAVEO™ T2G CYT4BF8CDE**, 350 MHz, 8 MB flash/1 MB SRAM, TEQFP-176
- Connection to MADK boards (M1/M3/M5) and Samtec 2x30 pins HSEC8 connector for LV15W card via a 100-pin HD connector connected to the T2G drive adapter card
- Five LEDs
  - 1 Power LED
  - 2 USER LED: User-controlled LED
  - 2 DEBUG LED & AUX LED: Debugger-controlled LEDs
- Isolated debug options (default)
  - Onboard debugger (SEGGER J-Link LITE) via a USB connector
  - Isolation must be built between this connector and the computer side to prevent overvoltage in the computer
- Isolated connectivity
  - UART channel of on-board debugger (SEGGER J-Link LITE) via USB connector
  - CAN interface on a 4-pin header X14
- 2 non-isolated debug options
  - SWD/JTAG via 10-pin 1.27 mm header
  - ETM trace via 20-pin 1.27 mm header
- Power supply of TRAVEO™ T2G CYT4BF MCU
  - Via 100-pin expansion board (5 V or 24 V) converted to 3.3 V or 5 V
  - Via debug USB connector, 5 V isolated DC-DC converted to 3.3 V or 5 V
- Power supply of XMC4200 MCU in isolated debug domain
  - Via debug USB connector
- KIT_MOTOR_DC_250W_24V_T2G power board
  - Rated voltage: 24 V and rated power: 250 W
  - Three shunt and single shunt operation
- DB42M03 brushless DC motor
- 24 V/1 A AC/DC power adapter

2 Kit operation

The KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit serves as an evaluation board to aid engineers in developing TRAVEO™ T2G Body High-based motor control solutions in combination with suitable power stage evaluation boards featuring the MADK connector (M1/M3/M5). The board is equipped with an isolated onboard debugger for programming and debugging via a USB interface. Additionally, it features a USB VCOM functionality using the same USB connection utilized for the debugger.

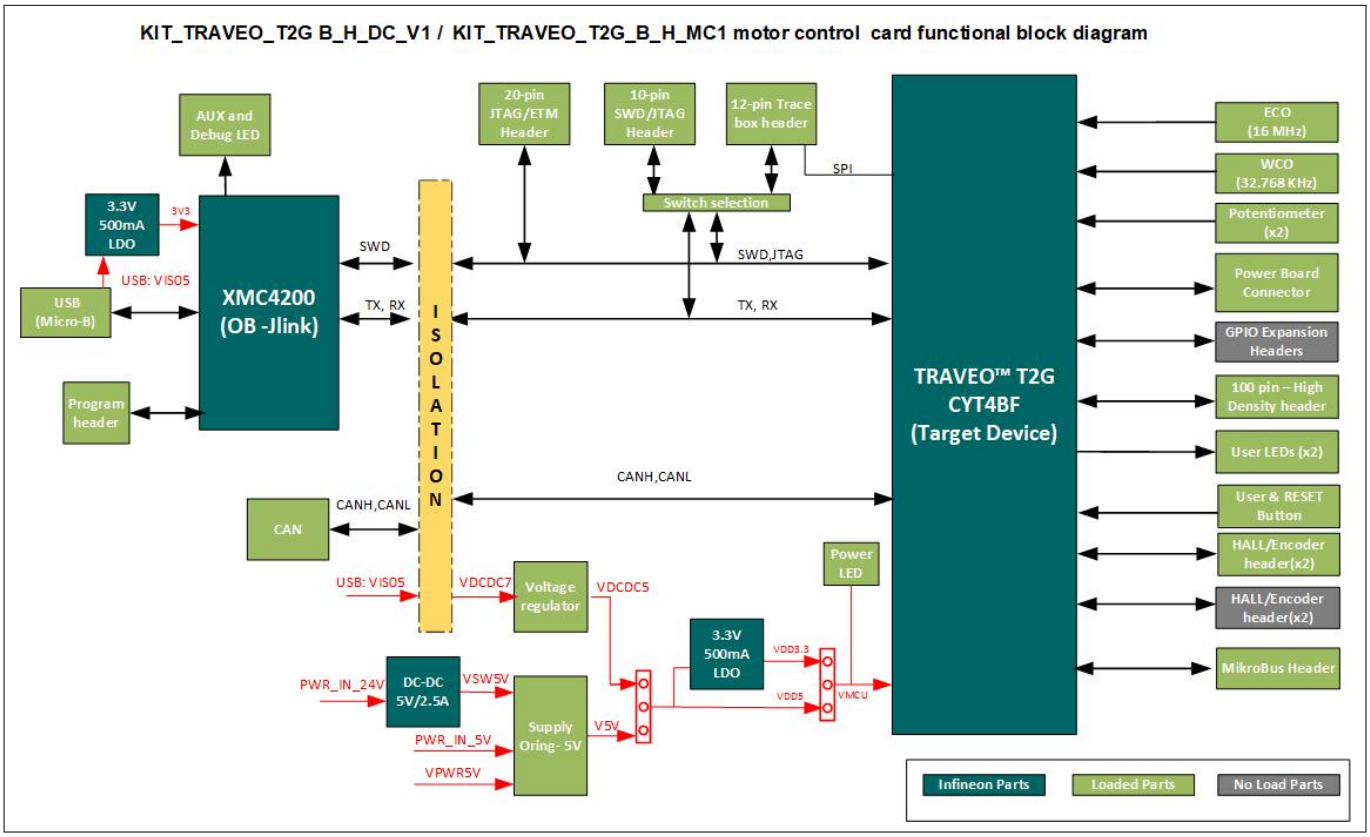

Figure 1 KIT_TRAVEO_T2G_B_H_DC_V1 motor control card block diagram

2 Kit operation

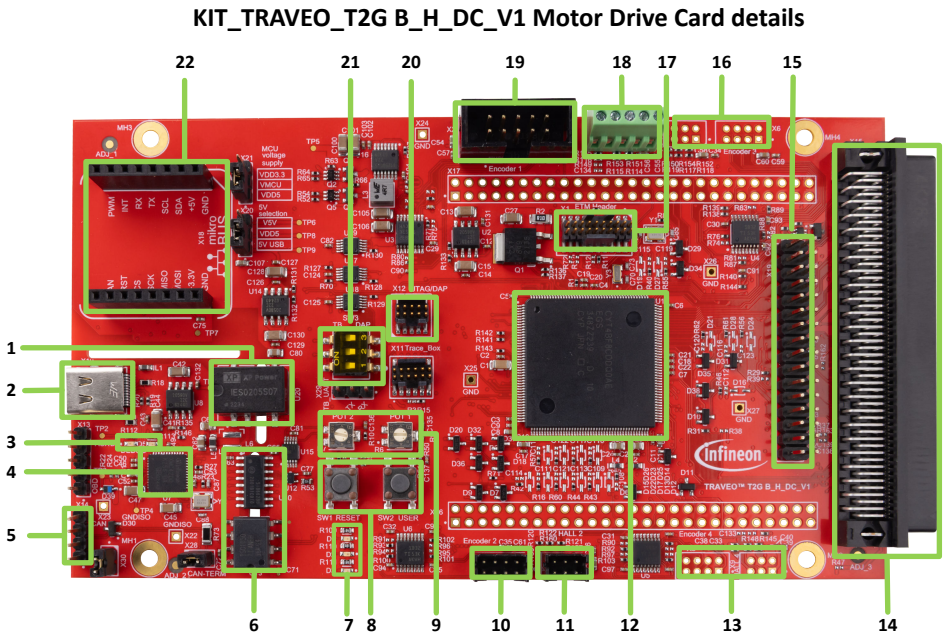

Figure 2 KIT_TRAVEO_T2G_B_H_DC_V1 motor control card details

2 Kit operation

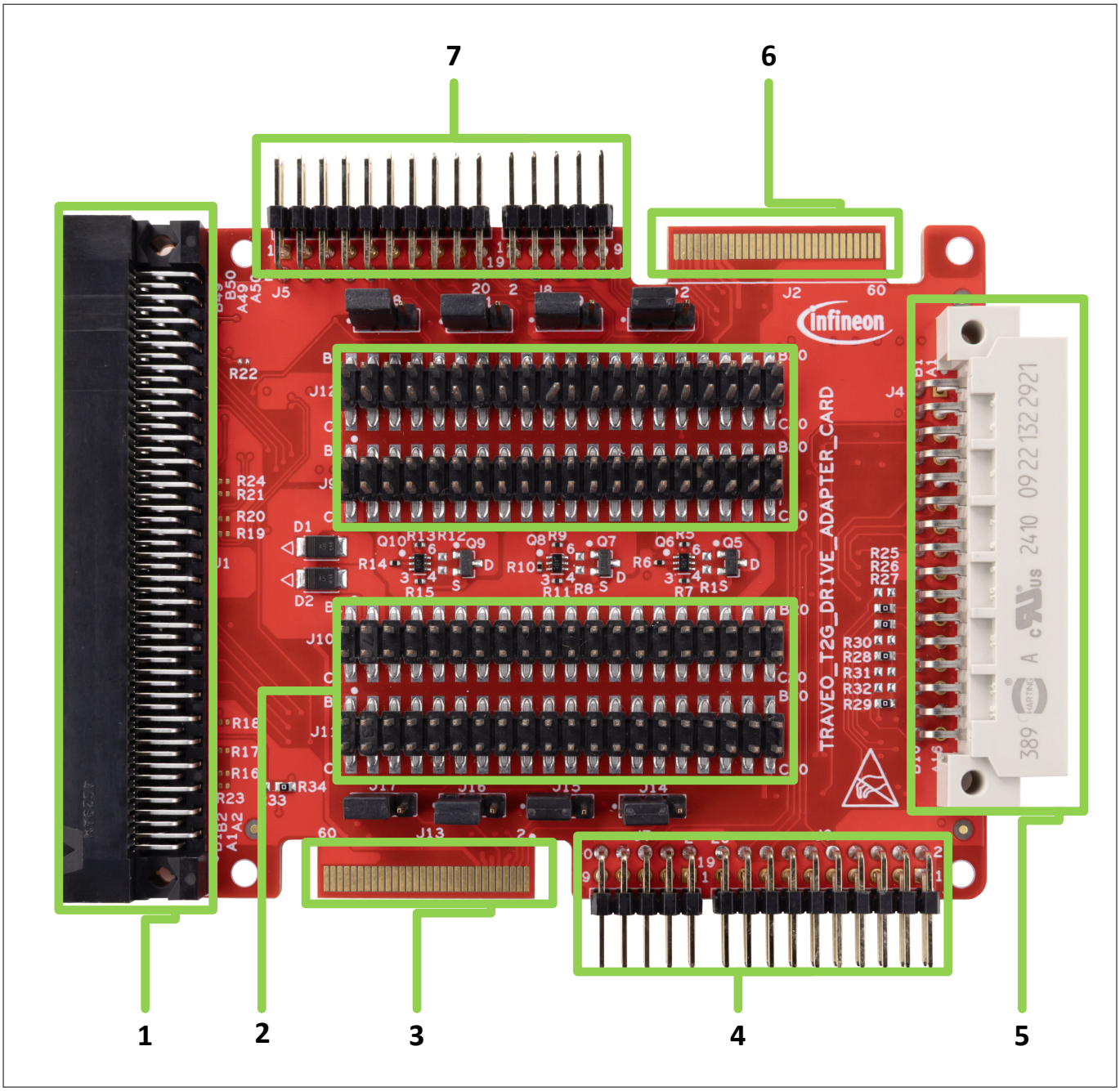

Figure 3 Drive adapter card details

The components present in the drive adapter card are:

1. 100-pin HD connector (J1)
2. 2x20 headers (J9, J10, J11, J12)
3. Samtec connector (J13)
4. MADK M1 connector (J6) and MADK M3 connector (J6 + J7)
5. MADK M5 connector (J4)
6. Samtec connector (J2)
7. MADK M1 connector (J5) and MADK M3 connector (J5 + J8)

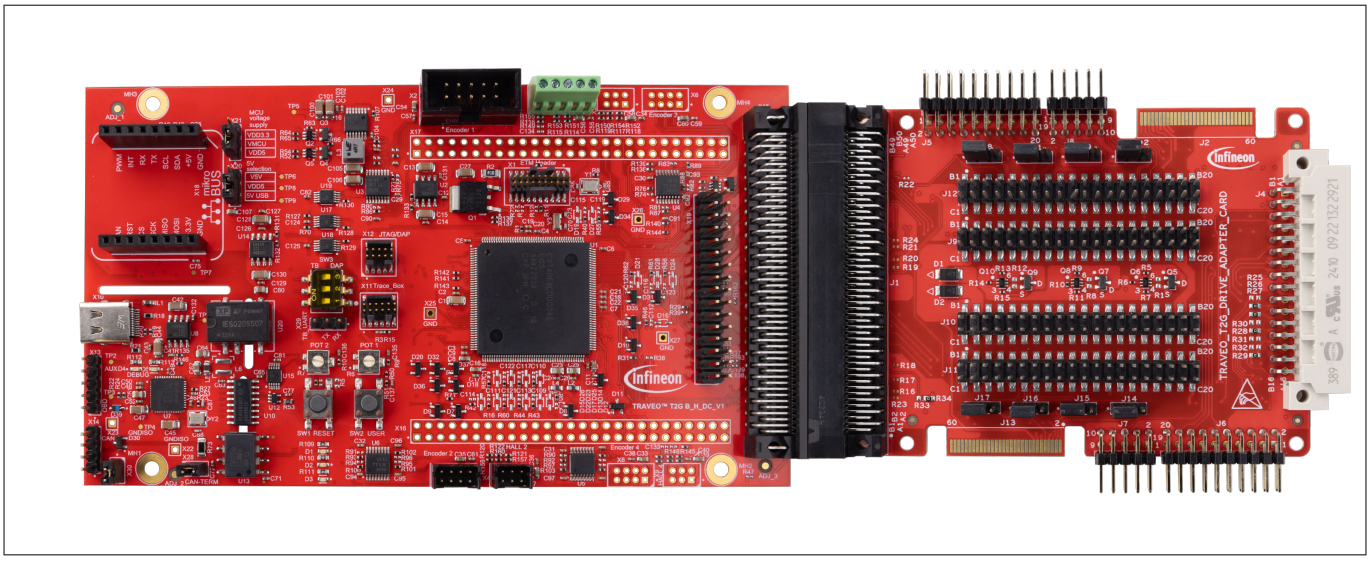

Figure 4 KIT_TRAVEO_T2G_B_H_DC_V1 motor control card connected to the drive adapter card

2.1 Using the OOB example

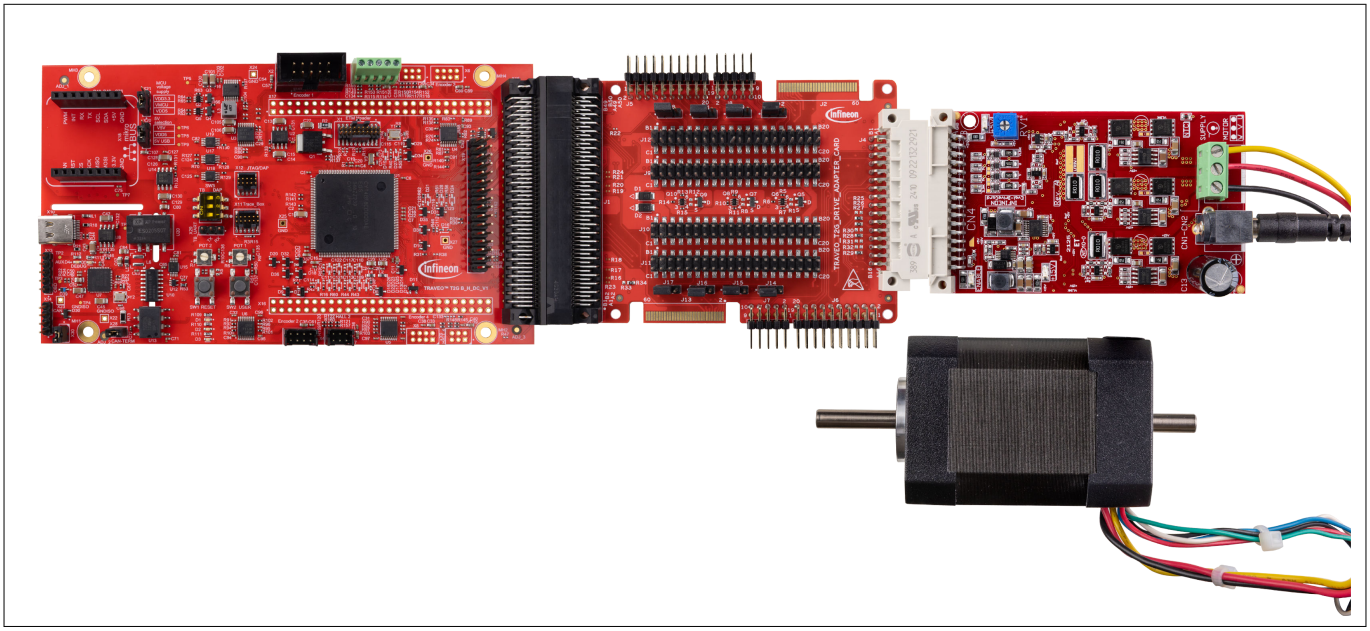

Figure 5 KIT_TRAVEO_T2G_B_H_MC1 complete setup with motor

2.1.1 Standalone operation

The MCU is pre-programmed with the out-of-box (OOB) firmware, configured to run the included motor in sensorless field-oriented control (FOC) three-shunt mode. To ensure proper operation:

1. Set the input voltage selection jumper (X20) to position 2-3 (V5V)
2. Set the VMCU voltage selection jumper (X21) to position 1-2 (VDD5)
3. Connect the control and power board using the adapter board as shown in Figure 5
4. Connect the motor wires to the motor screw terminal connector (CN3) on the power board as follows:
   - **Yellow**: U

- **Red**: V
- **Black**: W

5. Connect the 24 V/1 A power adapter to the DC input barrel jack (CN1) on the power board and turn on the power supply
6. The motor shaft spins in a clockwise direction (with respect to the motor front side)
7. The motor speed is controlled by the potentiometer POT1 (R6). Use the provided screwdriver to adjust the potentiometer setting
8. The user button (SW2) is used to change the motor direction. When pressed, the motor speed ramps down to '0' and stops. To restart the motor in the reverse direction, set the potentiometer (R6) to zero speed and then increase the speed
9. User LED1 (yellow) indicates the following motor directions:
   - On: For clockwise direction
   - Off: For counter-clockwise direction

***Note**: The motor speed depends on the potentiometer setting. If the potentiometer is set to '0' (fully turned in a clockwise direction), the motor will not run.*

2.1.2 GUI operation

2.1.2.1 Create a new project

1. Install ModusToolbox™ Motor Suite GUI from Infineon Developer Center (IDC)

   ***Note**: Use ModusToolbox™ Setup tool as an alternative to download and install ModusToolbox™ Motor Suite.*

2. Ensure that all the micro switches of SW3 are on the right side for proper operation
3. Follow steps 1 to 5 as described in the standalone operation section to set up the hardware
4. Connect the USB cable to the PC and the control card USB socket
5. Open the ModusToolbox™ Motor Suite GUI
6. Navigate to KIT_TRAVEO_T2G_B_H_DC_V1 Motor Control Drive Kit, select RFO, and click **New Project** to open the configurator view

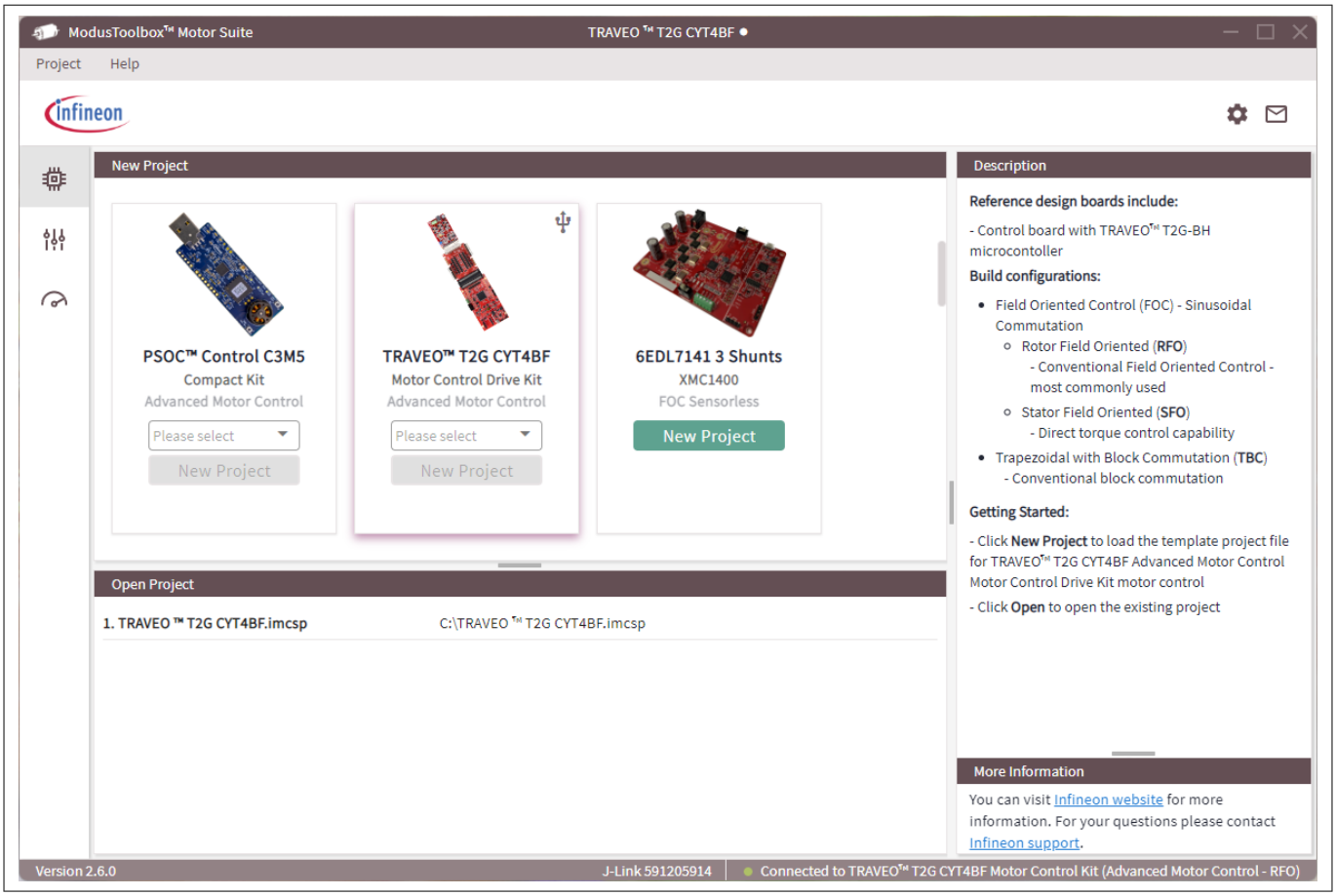

Figure 6 GUI: Open new project

2.1.2.2 Configurator view

1. A green color at the bottom of the suite indicates a successful connection
2. Configure the static parameters in the configurator view
3. Click **Flash Firmware** to reprogram the default firmware
4. Click the **Test bench** button to switch to the test bench view

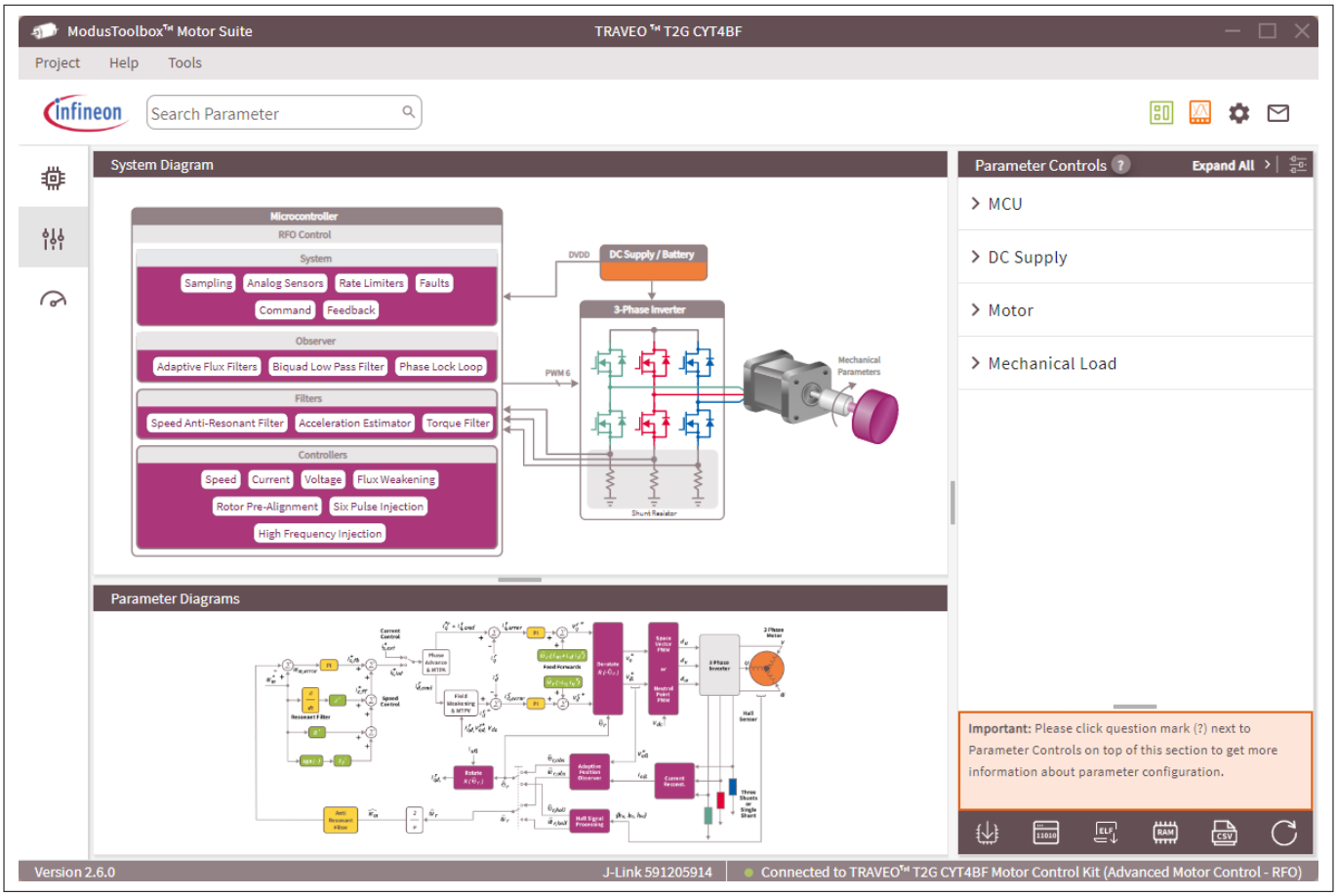

Figure 7 GUI: Configurator view

2.1.2.3 Test bench view

1. In the command panel, use the drive switch to enable or disable the drive
2. To set the motor speed using the target set slider in the command panel, turn off the potentiometer control switch in the GUI. If the potentiometer control switch is on, the potentiometer (R6) on the kit controls the motor speed
3. Use the emergency stop to halt or restart the motor and clear faults
4. The control panel and command panel sections display various parameters, including:
   - Voltage applied
   - Currents flowing
   - DC bus voltage
   - Faults
   - Control scheme
   - State of the state machine
   - Motor direction
5. Select the oscilloscope view to stream these parameters. For more details, see the user manual located in the top left corner of the oscilloscope window

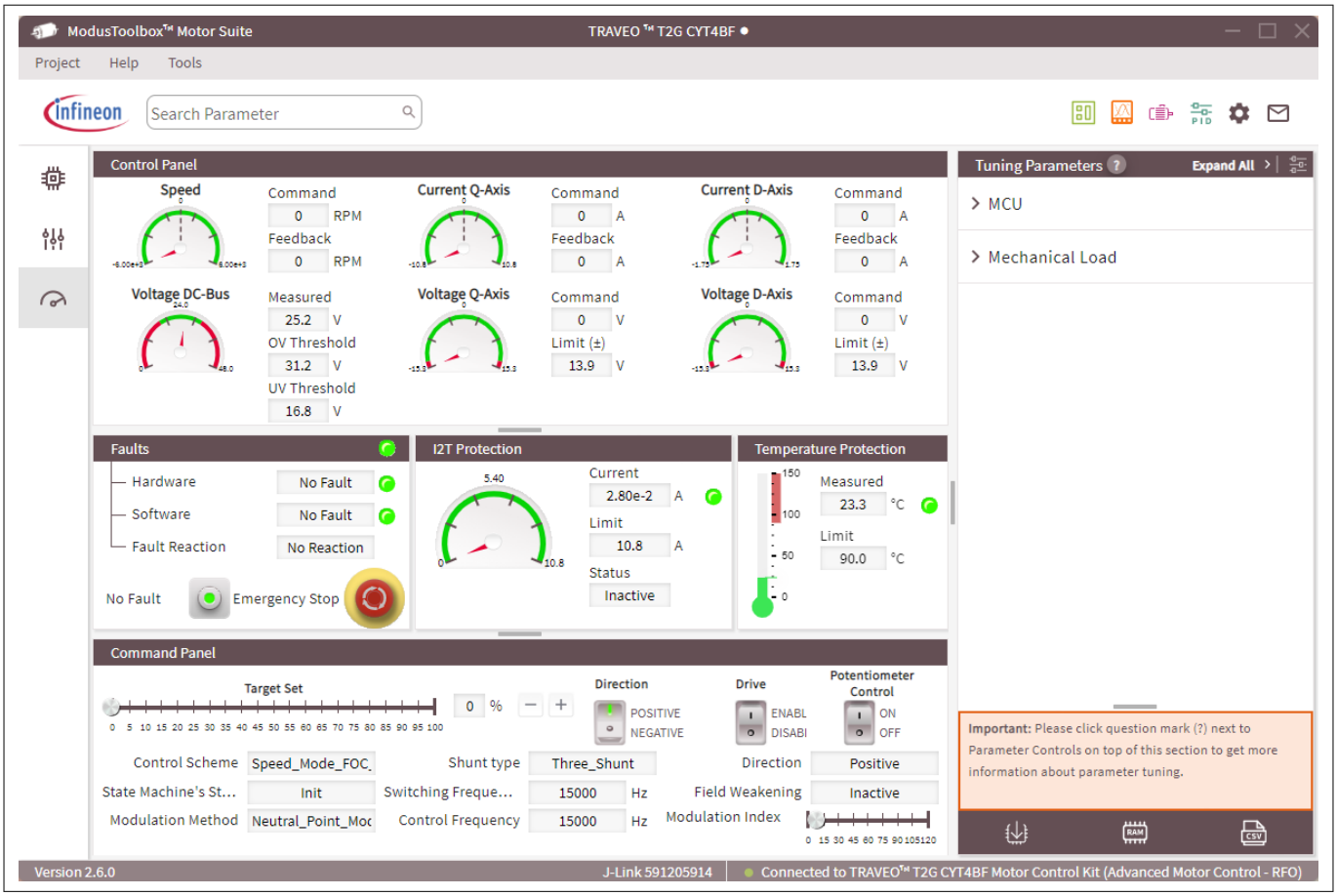

Figure 8 GUI: Test bench view

2.2 Creating a project and programming/debugging using ModusToolbox™

The KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit can be programmed and debugged using the onboard J-Link debugger, which also supports USB-UART bridge functionality. An XMC4200 device is used to implement the J-Link functionality. See the J-Link user guide for more details.

The following steps provide an overview of project creation, programming, and debugging using ModusToolbox™. For more information, go to **Help** > **ModusToolbox™ general documentation** > **ModusToolbox™ user guide.**

1. Connect the board to the PC using the provided USB cable through the J-Link USB connector (X10), as shown in Figure 9. It will enumerate as a USB composite device if the board is being connected to the PC for the first time. Ensure to install the latest J-Link drivers from the Segger website.

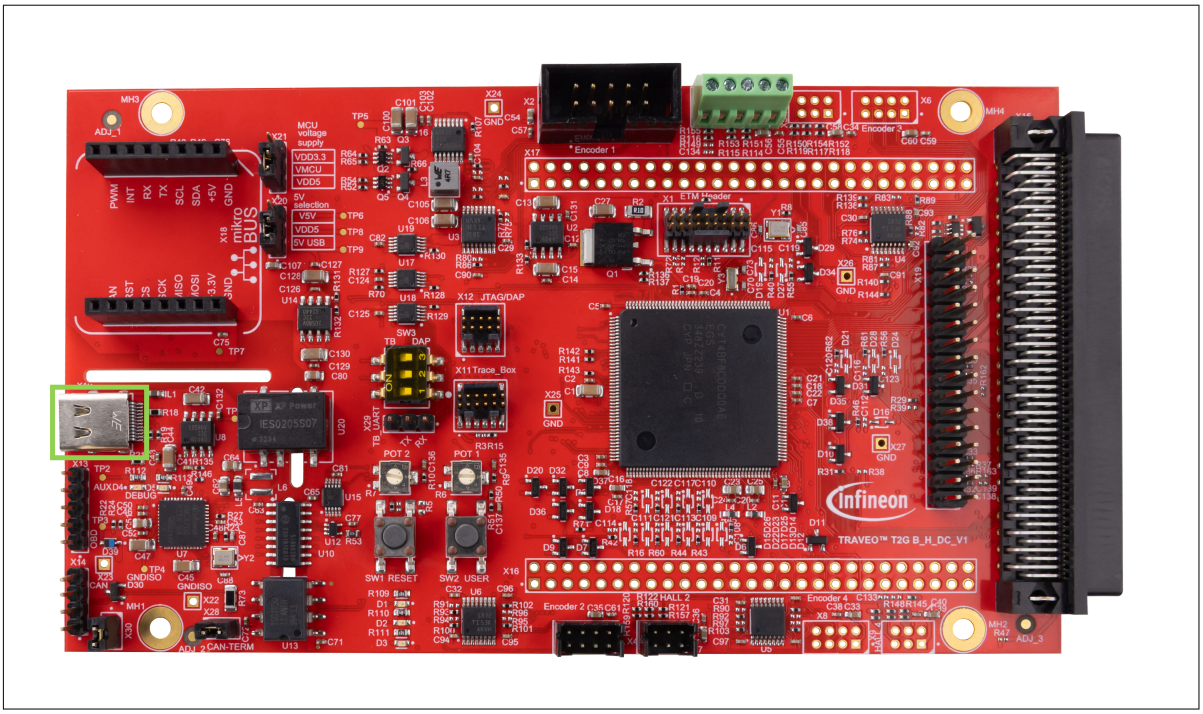

Figure 9 Connect USB cable to the USB connector on board

2. The debugger on this kit features the J-Link LITE with UART. The debug LED (green) is always ON if the USB is connected

***Note**: Programming can be done either with the onboard J-Link debugger (isolated) or by attaching an external debugger to the connector X12 (non-isolated) on the board. It is recommended to use the onboard J-Link debugger*

3. In the Eclipse IDE for ModusToolbox™, import the desired code example (application) into a new workspace

a. Click on **New Application** from the Quick Panel tab

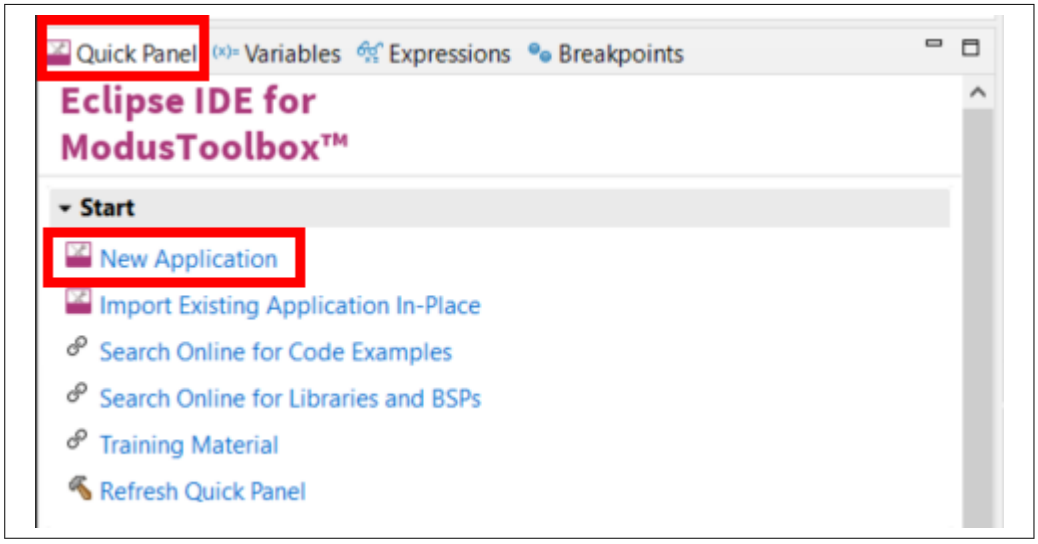

Figure 10 Create new application

b. Select the BSP -KIT_TRAVEO_T2G_B_H_MC1 in the Choose Board Support Package window and click **Next**

2 Kit operation

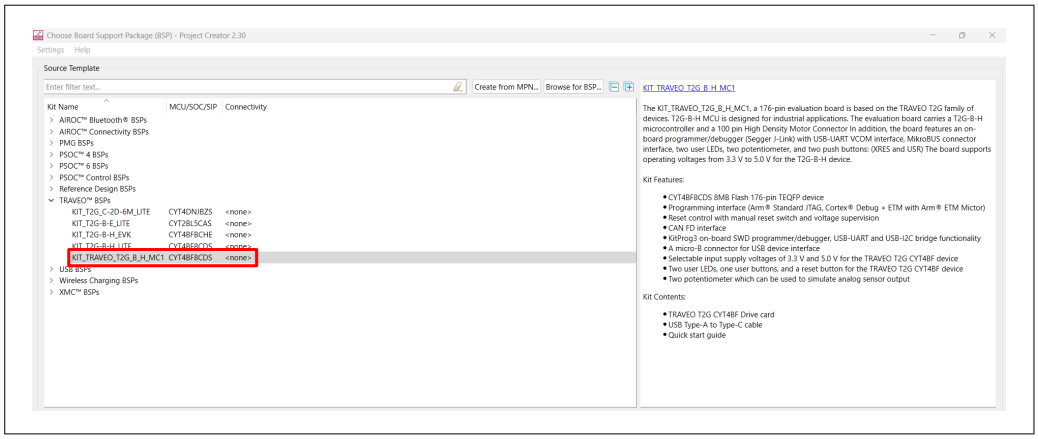

Figure 11 Choose Board Support Package

c. Select the application in the Select Application window and click **Create**

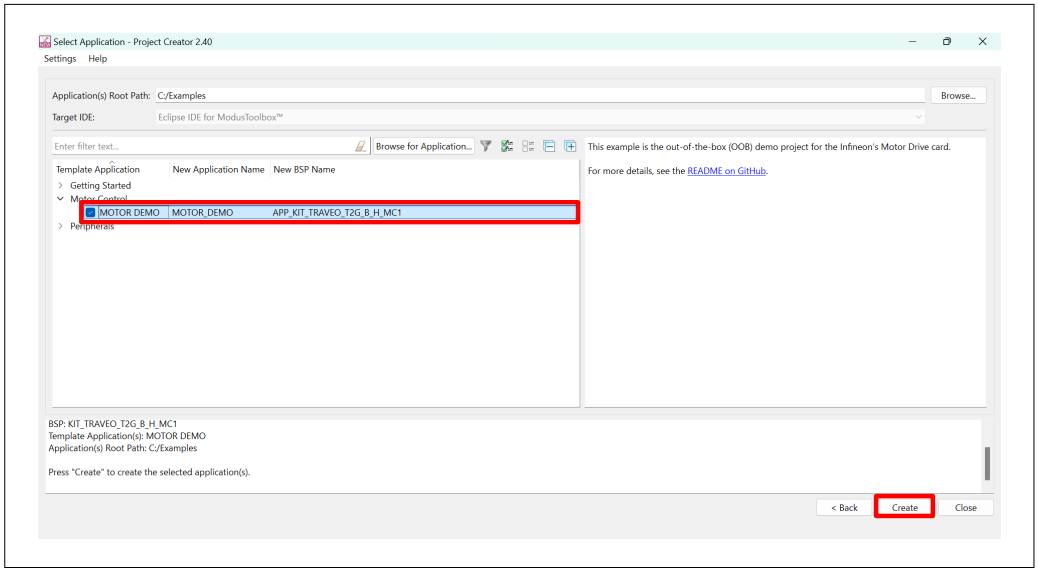

Figure 12 Select application

4. To build and program TRAVEO™ T2G CYT4BF MCU application, in the Project Explorer, select the **<App_Name>** project. In the Quick Panel tab, scroll to the **Launches** section and click the **<App_Name> Program** (J-Link) configuration

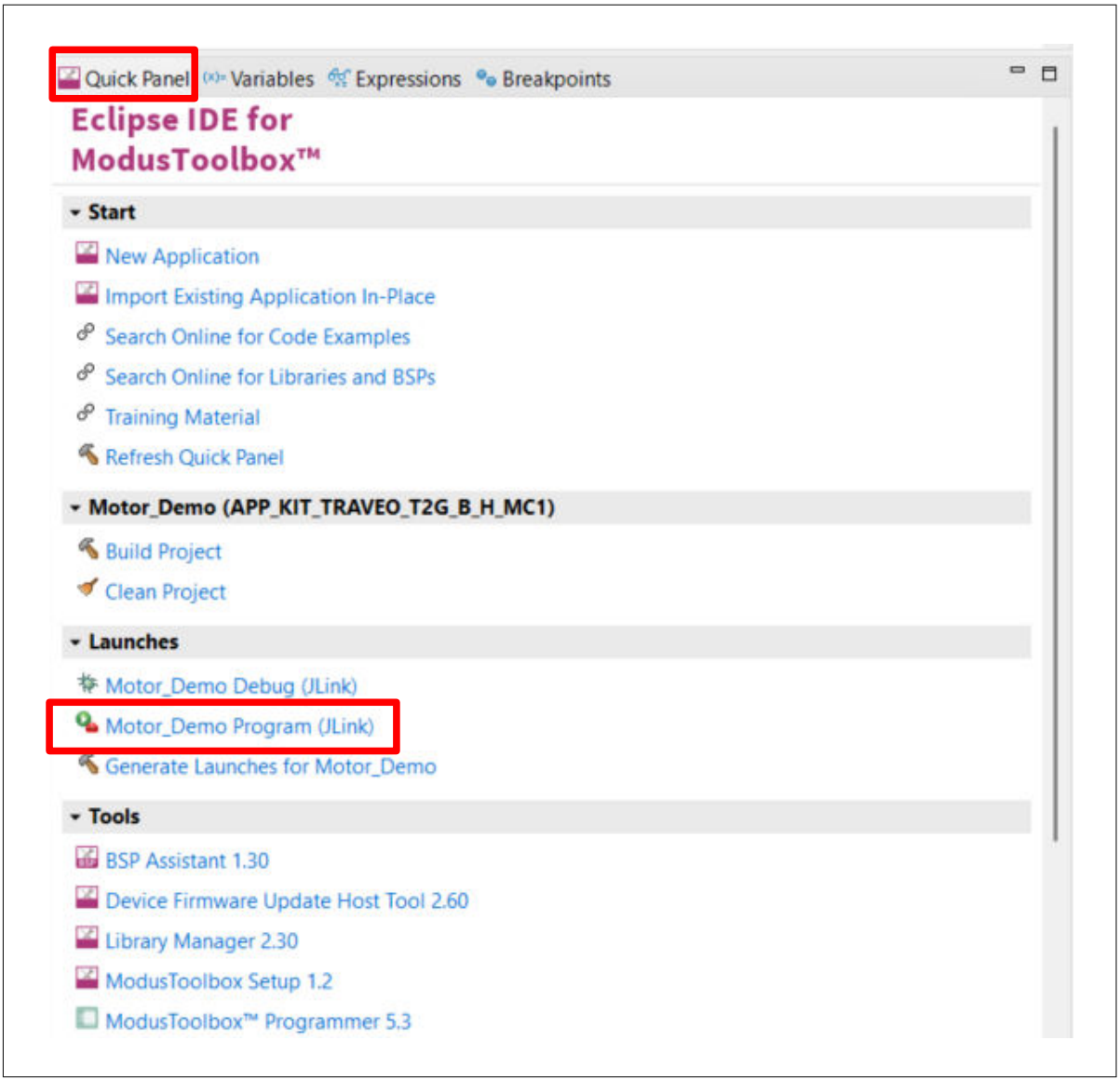

Figure 13 Programming in ModusToolbox™

5. ModusToolbox™ includes an integrated debugger. To debug an TRAVEO™ T2G CYT4BF MCU application, in the Project Explorer, select the **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Debug** (J-Link) configuration. For more details, see the Program and debug section in the Eclipse IDE for ModusToolbox™ user guide

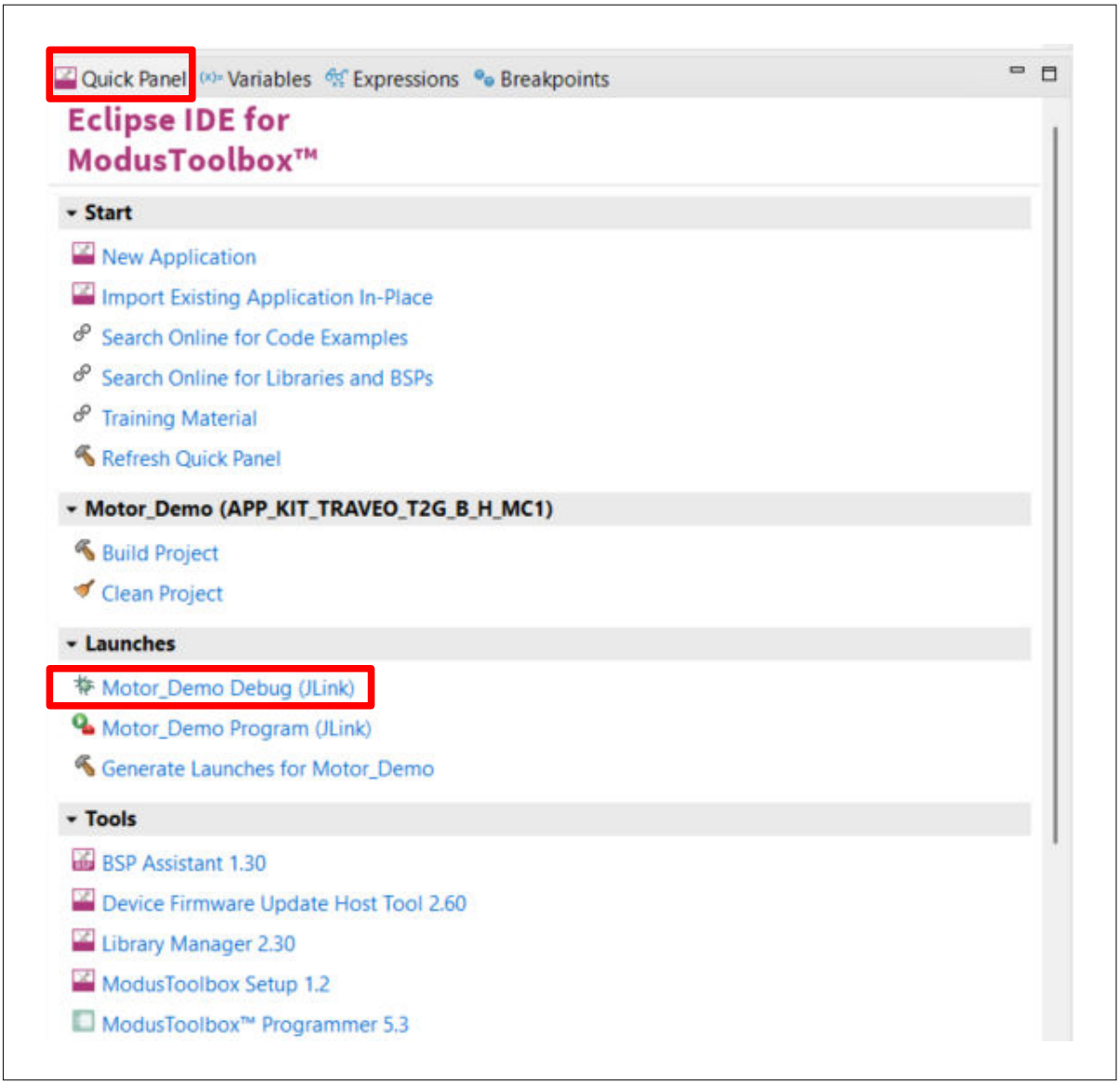

Figure 14 Debugging in ModusToolbox™

3 Hardware

3.1 Hardware and functional description

This section provides a detailed explanation of the individual hardware blocks used in this kit.

3.2 KIT_TRAVEO_T2G_B_H_DC_V1 motor control card

The control card is designed for the TRAVEO™ T2G CYT4BF microcontroller in a TEQFP-176 package. It features an onboard isolated J-Link debugger with the XMC4200 microcontroller. All the I/Os from the TRAVEO™ T2G CYT4BF MCU are routed out to the 100-pin high-density (HD) connector, and the resources are mapped to support up to four motor controls. The HD connector can be inserted into a mating connector on the included adapter board, which in turn facilitates connectivity to the various MADK motor control power boards.

3.3 TRAVEO™ T2G CYT4BF MCU

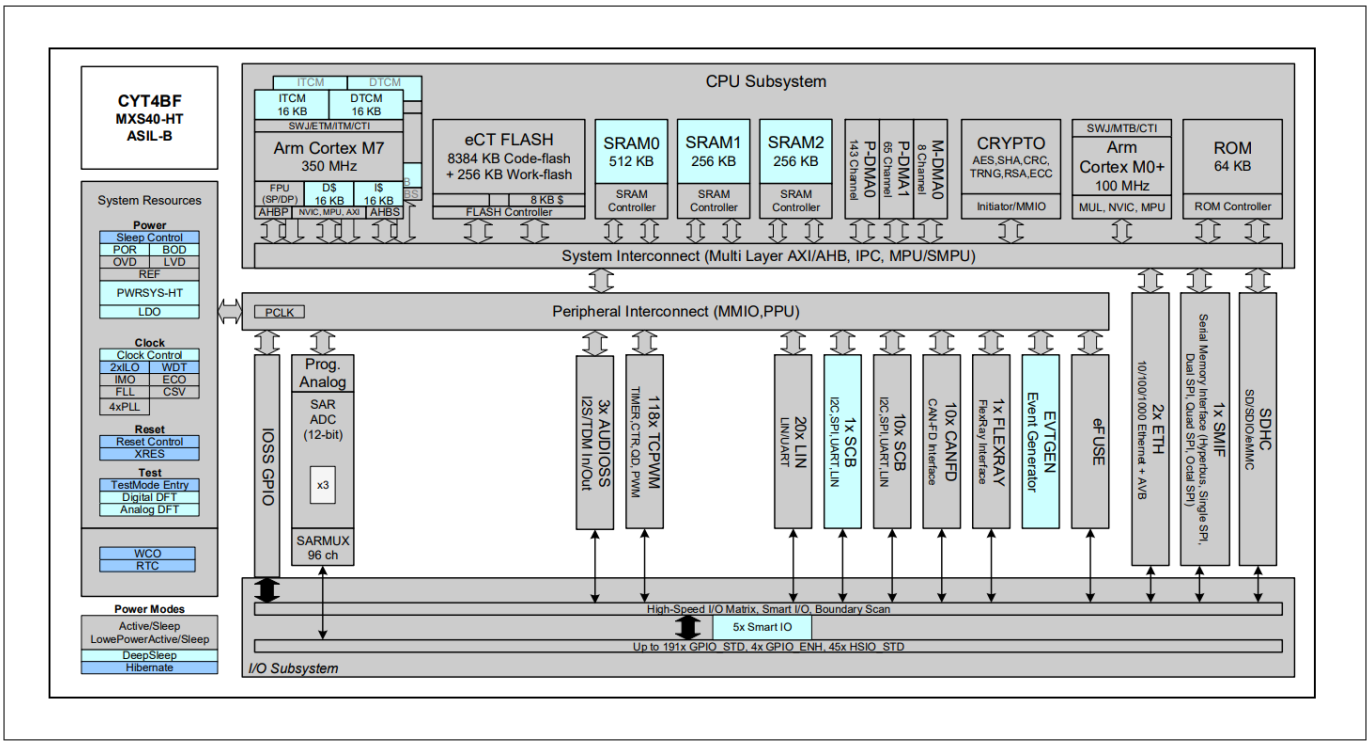

Figure 15 TRAVEO™ T2G CYT4BF MCU block diagram

The KIT_TRAVEO_T2G_B_H_DC_V1 motor control kit is built around TRAVEO™ T2G CYT4BF. It incorporates Infineon's low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

Features

- CPU subsystem
  - Two 350-MHz 32-bit Arm® Cortex®-M7 CPUs, each with
    - Single-cycle multiply
    - Single/double-precision floating point unit (FPU)
    - 16-KB data cache, 16-KB instruction cache

    - Memory protection unit (MPU)
    - 16-KB instruction and 16-KB data tightly-coupled memories (TCM)
  - 100-MHz 32-bit Arm® Cortex® M0+ CPU with
    - Single-cycle multiply
    - Memory protection unit (MPU)
  - Inter-processor communication in hardware
  - Three DMA controllers
    - Peripheral DMA controller #0 (P-DMA0) with 143 channels
    - Peripheral DMA controller #1 (P-DMA1) with 65 channels
    - Memory DMA controller (M-DMA0) with 8 channels
- Integrated memories
  - 8384 KB of code-flash with an additional 256 KB of work-flash
    - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing from it
    - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
    - Flash programming through SWD/JTAG interface - 1024-KB of SRAM with selectable retention granularity
- Cryptography engine
  - Supports Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
  - Secure boot and authentication
    - Using digital signature verification
    - Using fast secure boot
  - AES: 128-bit blocks, 128-/192-/256-bit keys
  - 3DES: 64-bit blocks, 64-bit key
  - Vector unit supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
  - SHA-1/2/3: SHA-512, SHA-256, SHA-160 with variable length input data
  - CRC: supports CCITT CRC16 and IEEE-802.3 CRC32
  - True random number generator (TRNG) and pseudo random number generator (PRNG)
  - Galois/Counter Mode (GCM)
- Functional safety for ASIL-B
  - Memory protection unit (MPU)
  - Shared memory protection unit (SMPU)
  - Peripheral protection unit (PPU)
  - Watchdog timer (WDT)
  - Multi-counter watchdog timer (MCWDT)
  - Low-voltage detector (LVD)
  - Brown-out detection (BOD)
  - Over-voltage detection (OVD)
  - Clock supervisor (CSV)
  - Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash, TCM)

- Low-Power 2.7-V to 5.5-V operation
  - Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
  - Configurable options for robust BOD
    - Two threshold levels (2.7 V and 3.0 V) for BOD on V_{DDD} and VDDA
    - One threshold level (1.1 V) for BOD on VCCD
- Wakeup
  - Up to two pins to wake from Hibernate mode
  - Up to 240 GPIO pins to wake from Sleep modes
  - Event Generator, SCB, watchdog timer, RTC alarms to wake from DeepSleep modes
- Clocks
  - Internal main oscillator (IMO)
  - Internal low-speed oscillator (ILO)
  - External crystal oscillator (ECO)
  - Watch crystal oscillator (WCO)
  - Phase-locked loop (PLL)
  - Frequency-locked loop (FLL)
- Communication interfaces
  - Up to 10 CAN FD channels
    - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
    - Compliant to ISO 11898-1:2015
    - Supports all the requirements of Bosch CAN FD Specification V1.0 for non-ISO CAN FD
    - ISO 16845:2015 certificate available
  - Up to 11 runtime-reconfigurable SCB (serial communication block) channels, each configurable as I^2C, SPI, or UART
  - Up to 20 independent LIN channels
    - LIN protocol compliant with ISO 17987
  - Up to two 10/100/1000 Mbps Ethernet MAC interfaces conforming to IEEE-802.3az
    - Supports the following PHY interfaces:
      - Media-independent interface (MII)
      - Reduced media-independent interface (RMII)
      - Gigabit media-independent interface (GMII)
      - Reduced gigabit media-independent interface (RGMII)
    - Compliant with IEEE-802.1BA Audio Video Bridging (AVB)
    - Compliant with IEEE-1588 Precision Time Protocol (PTP)
  - FlexRay interface (V2.1) configurable for single or dual data-channels for fault tolerance, supporting data rates up to 10 Mbps
- External memory interface
  - One SPI (single, dual, quad, or octal) or HYPERBUSTM interface
  - On-the-fly encryption and decryption
  - Execute-In-Place (XIP) from external memory

- SDHC interface
  - One Secure Digital High Capacity (SDHC) interface supporting embedded MultiMediaCard (eMMC), Secure Digital (SD), or SDIO (Secure Digital Input Output)
    - Compliant to eMMC 5.1, SD 6.0, and SDIO 4.10 specifications
  - Data rates up to SD High Speed 50 MHz, or eMMC 52 MHz DDR
- Audio interface
  - Three Inter-IC Sound (I^2S) Interfaces for connecting digital audio devices
  - I^2S, left justified, or time division multiplexed (TDM) audio formats
  - Independent transmit or receive operation, each in master or slave mode
- Timers
  - Up to 102 16-bit and 16 32-bit timer/counter pulse-width modulator (TCPWM) blocks
    - Up to 15 16-bit counters for motor control
    - Up to 87 16-bit counters and 16 32-bit counters for regular operations
    - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PWM_DT), pseudo-random PWM (PWM_PR), and shift-register (SR) modes
  - Up to 16 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
    - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)
- Real time clock (RTC)
  - Year/Month/Date, Day-of-week, Hour:Minute:Second fields
  - 12- and 24-hour formats
  - Automatic leap-year correction
- I/O
  - Up to 240 programmable I/Os
  - Three I/O types
    - GPIO Standard (GPIO_STD)
    - GPIO Enhanced (GPIO_ENH)
    - High-Speed I/O Standard (HSIO_STD)
- Regulators
  - Generates a 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
  - Three regulators:
    - DeepSleep
    - Core internal
    - Core external
- Programmable analog
  - Three SAR A/D converters with up to 99 external channels (96 I/Os + 3 I/Os for motor control)
    - Each ADC supports 32 logical channels, with 32 + 1 physical connections. Any external channel can be connected to any logical channel in the respective SAR.
  - Each ADC supports 12-bit resolution and sampling rates of up to 1 Msps
  - Each ADC also supports six internal analog inputs like
    - Bandgap reference to establish absolute voltage levels
    - Calibrated diode for junction temperature calculations
    - Two AMUXBUS inputs and two direct connections to monitor supply levels
  - Each ADC supports addressing of external multiplexers

  - Each ADC has a sequencer supporting autonomous scanning of configured channels
  - Synchronized sampling of all ADCs for motor-sense applications
- Smart I/O
  - Up to five Smart I/O blocks, which can perform Boolean operations on signals going to and from I/Os
  - Up to 36 I/Os (GPIO_STD) supported
- Debug interface
  - JTAG controller and interface compliant to IEEE-1149.1-2001
  - Arm® SWD (serial wire debug) port
  - Supports Arm® Embedded Trace Macrocell (ETM) Trace
    - Data trace using SWD
    - Instruction and data trace using JTAG
- Compatible with industry-standard tools
  - GHS MULTI or IAR EWARM for code development and debugging
- Packages
  - 176-TEQFP, 24 × 24 × 1.7 mm (max), 0.5-mm lead pitch
  - 272-BGA, 16 × 16 × 1.7 mm (max), 0.8-mm ball pitch
  - 320-BGA, 17 × 17 × 1.7 mm (max), 0.8-mm ball pitch
- Certification
  - Qualified for automotive application according to AEC-Q100

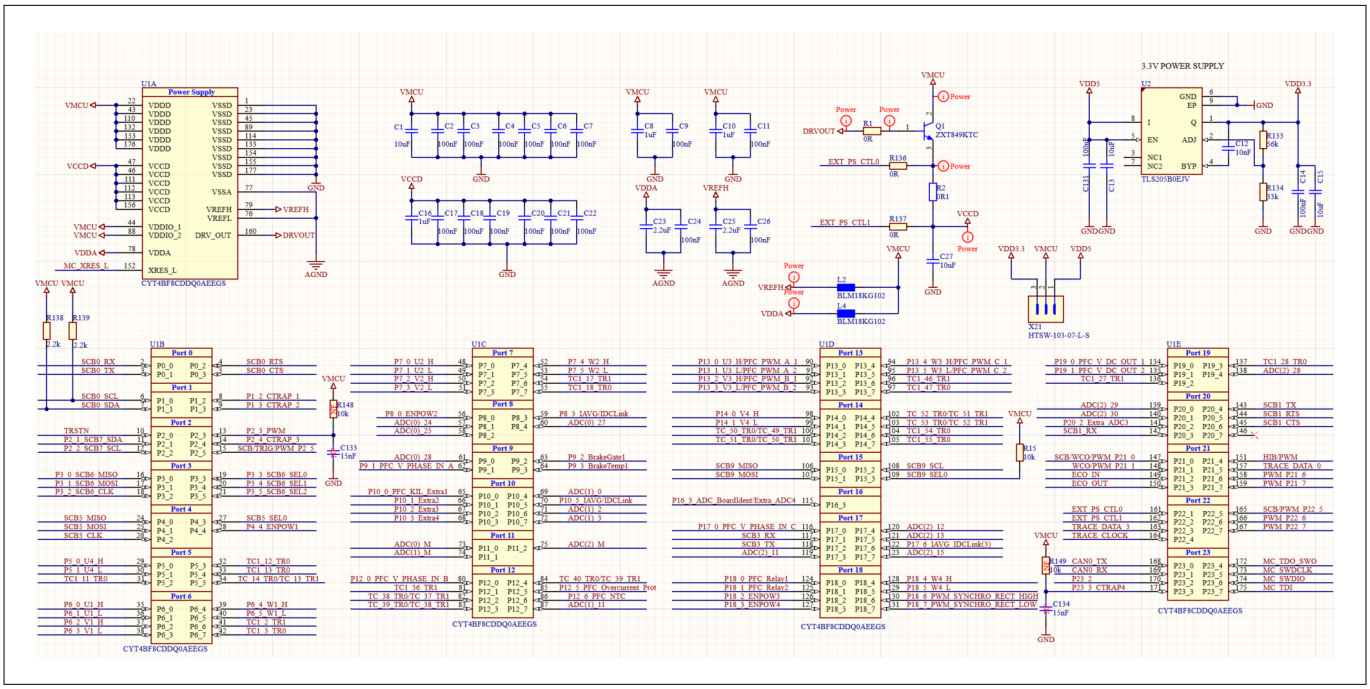

Figure 16 TRAVEO™ T2G CYT4BF MCU pin connections

3.4 TRAVEO™ T2G CYT4BF MCU power supply system

The TRAVEO™ T2G CYT4BF MCU operates using a single regulated VDDD supply within the range of 2.7 V to 5.5 V. It contains three regulators that provide power to the low-voltage core transistors: Deep Sleep, core internal, and core external. These regulators accept a 2.7 V to 5.5 V VDDD supply and provide a low-noise 1.1 V supply to various parts of the device. They are automatically enabled and disabled by hardware and firmware when

switching between power modes. The core internal and core external regulators operate in Active mode and provide power to the CPU subsystem and associated peripherals.

The core internal regulator supports load currents up to 300 mA and is operational during device start-up (boot process) and in Active/Sleep modes.

To support worst-case loading, with both M7 CPUs and the M0+ CPU at their maximum clock frequency and all integrated peripherals operating, a core external regulator is required, capable of loading currents up to 600 mA. The KIT_TRAVEO_T2G_B_H_DC_V1 motor control card implements an NPN pass transistor (Q1) for the core external regulator, reducing the overall power dissipation within the TRAVEO™ T2G CYT4BF package while maintaining a well-regulated core supply.

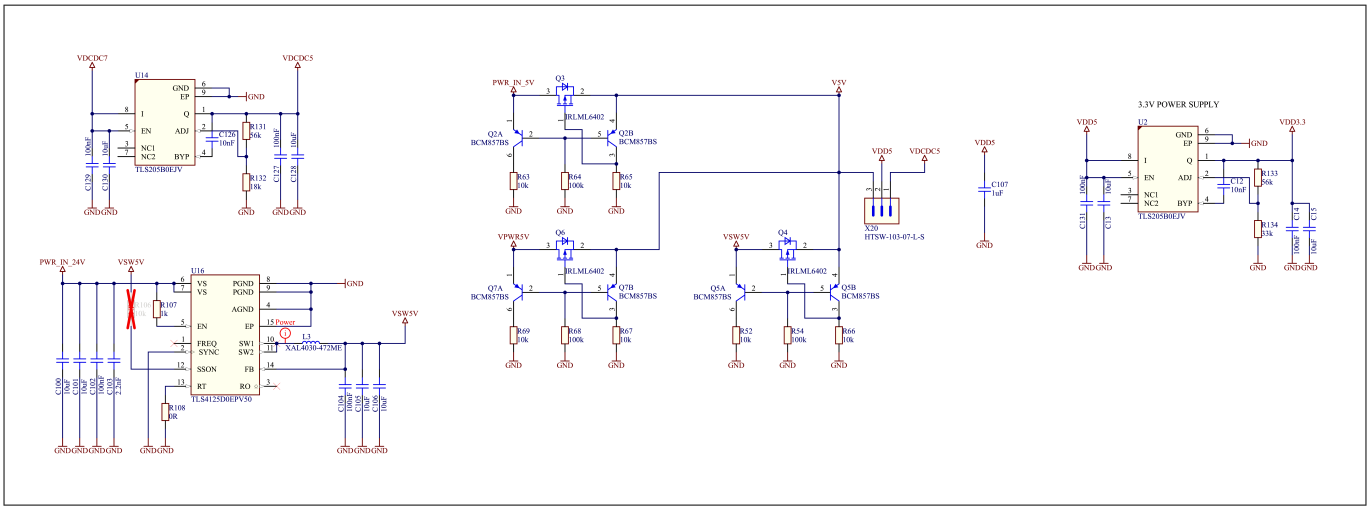

Figure 17 TRAVEO™ T2G CYT4BF MCU power supply scheme

The TRAVEO™ T2G CYT4BF MCU can be operated at 3.3 V or 5.0 V using the voltage selection from the X21 jumper header. The rest of the board is also supported with both 3.3 V and 5 V supplies. VMCU is the supply voltage that goes to the MCU and other parts of the board. If the X21 jumper is in the 1-2 position, VMCU is 5.0 V; if it is in the 2-3 position, VMCU is 3.3 V. VDD3.3 is generated using the U2 low-dropout regulator.

The VDD5 rail, which powers the U2 regulator as well as the rest of the circuits running on 3.3 V or 5 V, can be sourced from any of the following options:

1. **Isolated USB supply**: The USB 5 V supply is used to power a 5 V to 7 V DC-DC isolated converter, which in turn generates a 5 V supply (VDCDC5) using U14. This supply can be used to power the board when the X20 jumper is set to the 1-2 position
2. **5 V or 24 V supply from the power board**: When the X20 jumper is set to the 2-3 position, the board can be powered by any of the following sources:
   a. **High-density HD connector (X15)**: Either a 24 V supply on pin B41, converted to 5 V using U16, or a 5 V supply on pins B5/B10 of the 100-pin high-density connector
   b. **MADK5 power board header (X19)**: A 5 V supply on pin 2 of the X19 header can be used to power the board

Multiple 5 V sources, which come from the power stage (either direct 5 V or 24 V regulated to 5 V), are ORed using low-drop rectifiers based on the Q3, Q4, and Q6 MOSFETs.

3.5 TRAVEO™ T2G CYT4BF MCU I/O connectors

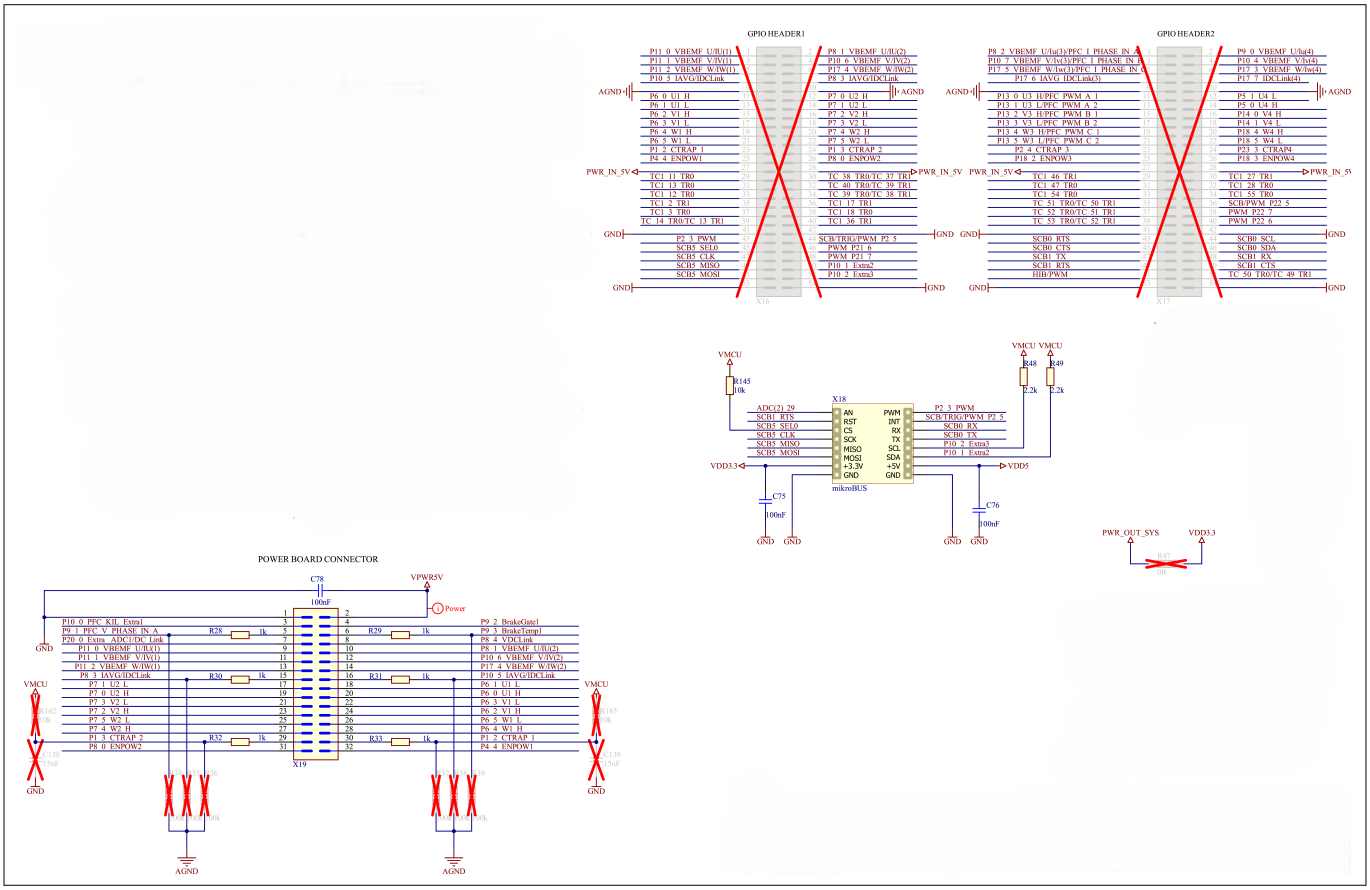

Figure 18 MADK M5 header, expansion header, and mikroBUS header

MADK M5 header (X19): The MADK M5 header offers the same pinout available in the MADK M5 connector on the drive adapter card, using a 16x2 male header with a standard 2.54 mm pitch. This header can be used for hardware debugging or probing the signals.

Table 2 MADK M5 header pin out details

Pin no.	Signal name	TRAVEO™ T2G CYT4BF pin	Description
1	GND	GND	Ground
2	VPWR5V	NA	Power input
3	P10_0_PFC_KILL_Extra1	P10.0	PFC KILL extra digital signal
4	P9_2_BrakeGate1	P9.2	Output brake gate signal
5	P9_1_PFC_V_PHASE_IN_A	P9.1	Analog-PFC input for phase voltage or current
6	P9_3_BrakeTemp1	P3.1	Temperature feedback for motor 1 power stage
7	P20_0_Extra_ADC1/ DC_Link	P20.0	Analog-PFC input for phase voltage or current

(table continues...)

Table 2 (continued) MADK M5 header pin out details

Pin no.	Signal name	TRAVEO™ T2G CYT4BF pin	Description
8	P8_4_VDCLink	P8.4	Power stage VDC link sensing signal
9	P11_0_VBEMF_U/IU(1)	P11.0	Motor 1 BEMF U or Current U sense
10	P8_1_VBEMF_U/IU(2)	P8.1	Motor 2 BEMF U or Current U sense
11	P11_1_VBEMF_V/IV(1)	P11.1	Motor 1 BEMF V or Current V sense
12	P10_6_VBEMF_V/IV(2)	P10.6	Motor 2 BEMF V or Current V sense
13	P11_2_VBEMF_W/IW(1)	P11.2	Motor 1 BEMF W or Current W sense
14	P17_4_VBEMF_W/IW(2)	P17.4	Motor 2 BEMF W or Current W sense
15	P8_3_IAVG/IDCLink	P8_3	Motor 1 DC link shunt current
16	P10_5_IAVG/IDCLink	P10_5	Motor 2 DC link shunt current
17	P7_1_U2_L	P7.1	Motor 2 PWM UL
18	P6_1_U1_L	P6.1	Motor 1 PWM UL
19	P7_0_U2_H	P7.0	Motor 2 PWM UH
20	P6_0_U1_H	P6.0	Motor 1 PWM UH
21	P7_3_V2_L	P7.3	Motor 2 PWM VL
22	P6_3_V1_L	P6.3	Motor 1 PWM VL
23	P7_2_V2_H	P7.2	Motor 2 PWM VH
24	P6_2_V1_H	P6.2	Motor 1 PWM VH
25	P7_5_W2_L	P7.5	Motor 2 PWM WL
26	P6_5_W1_L	P6.5	Motor 1 PWM WL
27	P7_4_W2_H	P7.4	Motor 2 PWM WH
28	P6_4_W1_H	P6.4	Motor 1 PWM WH
29	P1_3_CTRAP2	P1.3	Motor 2 kill feedback
30	P1_2_CTRAP1	P1.2	Motor 1 kill feedback
31	P8_0_ENPOW2	P8.0	Motor 2 power stage enable
32	P4_4_ENPOW1	P4.4	Motor 1 power stage enable

mikroBUS header (X18): The mikroBUS header provides a standardized interface for connecting compatible Click boards, which can expand the kit's functionality with sensors, actuators, communication modules, and more. Note that some interfaces may require rework, as the same pins are used for multiple functionalities.

Table 3 mikroBUS header pinout details

Pin	Signal name	Connected to signal	TRAVEO™ T2G CYT4BF MCU pin	Rework required
1	AN	ADC(2)_29	P20.0	Y
2	RST	SCB_RTS	P20.5	Y
3	CS	SCB5_SEL0	P4.3	
4	SCK	SCB5_CLK	P4.2	
5	MISO	SCB5_MISO	P4.0	
6	MOSI	SCB5_MOSI	P4.1	
7	+3.3 V	VDD3.3	VDDD	
8	GND	GND	EPAD	
9	GND	GND	EPAD	
10	+5 V	VDD5	-	
11	SDA	P10_1_Extra2	P10.1	
12	SCL	P10_2_Extra3	P10.2	
13	TX	SCB0_TX	P0_1	
14	RX	SCB0_RX	P0_0	
15	INT	SCB/TRIG/ PWM_P2_5	P0.0	
16	PWM	P2_3_PWM	P0.1	

***Note**: mikroBus header pin 1 AN input is also connected to POT1. Remove R55 to use this pin for external analog input. RST pin(2) is not connected to MCU XRES_L so mikroBus based click boards cannot Reset TRAVEO™ T2G CYT4BF MCU.*

3.6 100-pin HD connector interface

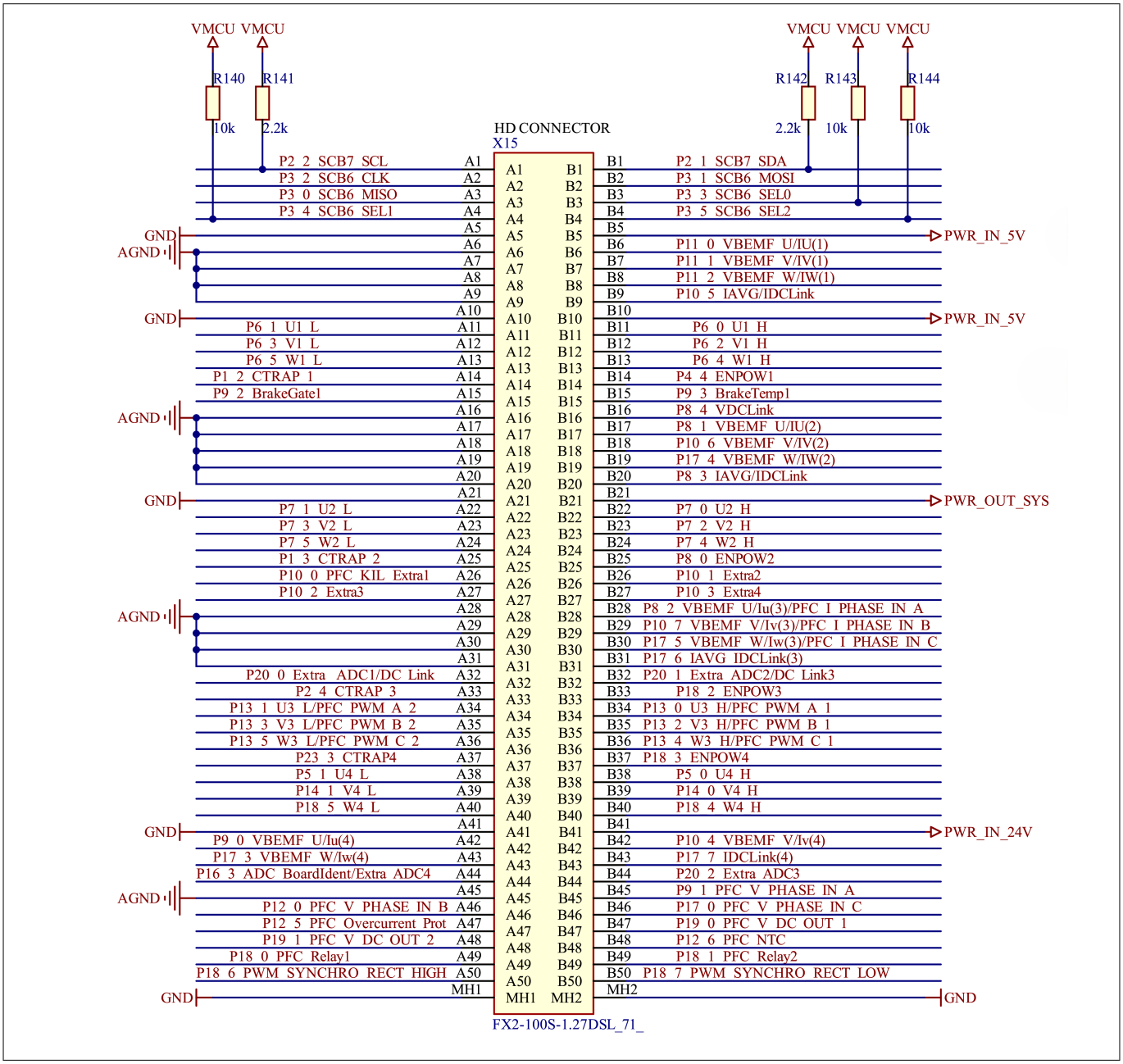

Figure 19 100-pin HD connector

The 100-pin high-density connector interfaces with the drive adapter card, facilitating connectivity for MADK motor power stages. It supports single, dual, and triple motors, as well as an optional power factor correction (PFC) control or a fourth motor.

Table 4 X15 HD connector peripheral details

X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals	X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals
A1	P2.2	SCB7 SCL	B1	P2.1	SCB7 SDA
A2	P3.2	SCB6 CLK	B2	P3.1	SCB6 MOSI

(table continues...)

Table 4 (continued) X15 HD connector peripheral details

X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals	X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals
A3	P3.0	SCB6 MISO	B3	P3.3	SCB6 SEL0
A4	P3.4	SCB6 SEL1	B4	P3.5	SCB6 SEL2
A5	GND	Ground	B5	PWR_IN_5V	5 V Input from power board
A6	AGND	Analog ground	B6	P11.0	VBEMFU/IU(1)
A7	AGND	Analog ground	B7	P11.1	VBEMFV/IV(1)
A8	AGND	Analog ground	B8	P11.2	VBEMFW/IW(1)
A9	AGND	Analog ground	B9	P10.5	IAVG/IDCLink(1)
A10	GND	Ground	B10	PWR_IN_5V	5 V Input from power board
A11	P6.1	U1L	B11	P6.0	U1H
A12	P6.3	V1L	B12	P6.2	V1H
A13	P6.5	W1L	B13	P6.4	W1H
A14	P1.2	CTRAP_1	B14	P4.4	ENPOW1
A15	P9.2	BrakeGate1	B15	P9.3	BrakeTemp1
A16	AGND	Analog ground	B16	P8_4	VDCLink
A17	AGND	Analog ground	B17	P8.1	VBEMFU/IU(2)
A18	AGND	Analog ground	B18	P10.6	VBEMFV/IV(2)
A19	AGND	Analog ground	B19	P17.4	VBEMFW/IW(2)
A20	AGND	Analog ground	B20	P8.3	IAVG/IDCLink(2)
A21	GND	Ground	B21	PWR_OUT_SYS	3.3 V output from control board
A22	P7.1	U2L	B22	P7.0	U2H
A23	P7.3	V2L	B23	P7.2	V2H
A24	P7.5	W2L	B24	P7.4	W2H
A25	P1.3	CTRAP2	B25	P8.0	ENPOW2
A26	P10.0	PFC KIL Extra1	B26	P10.1	Extra2 digital GPIO
A27	P10.2	Extra3 Digital GPIO	B27	P10.3	Extra4 digital GPIO
A28	AGND	Analog ground	B28	P8.2	VBEMFU/ IU(3)/PFC I PHASE IN A

(table continues...)

Table 4 (continued) X15 HD connector peripheral details

X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals	X15 HD pin	TRAVEO™ T2G CYT4BF pin	Peripherals
A29	AGND	Analog ground	B29	P10.7	VBEMFV/ IV(3)/PFC I PHASE IN B
A30	AGND	Analog ground	B30	P17.5	VBEMFW/ IW(3)/PFC I PHASE IN C
A31	AGND	Analog ground	B31	P17.6	IAVG/IDCLink(3)
A32	P20.0	Extra ADC1/DC LINK	B32	P20.1	Extra ADC2/DC LINK3
A33	P2.4	CTRAP3	B33	P18.2	ENPOW3
A34	P13.1	U3L/ PFC_PWM_A_2	B34	P13.0	U3H/ PFC_PWM_A_1
A35	P13.3	V3L/ PFC_PWM_B_2	B35	P13.2	V3H/ PFC_PWM_B_1
A36	P13.5	W3L/ PFC_PWM_C_2	B36	P13.4	W3H/ PFC_PWM_C_1
A37	P23.3	CTRAP4	B37	P18.3	ENPOW4
A38	P5.1	U4L	B38	P5.0	U4H
A39	P14.1	V4L	B39	P14.0	V4H
A40	P18.5	W4L	B40	P18.4	W4H
A41	GND	Ground	B41	PWR_IN_24V	24 V supply input from power board
A42	P9.0	VBEMFU/IU(4)	B42	P10.4	VBEMFV/IV(4)
A43	P17.3	VBEMFW/IW(4)	B43	P17.7	IDCLINK(4)
A44	P16.3	ADC BoardIdent/ EXTRA ADC4	B44	P20.2	EXTRA ADC3
A45	AGND	Analog ground	B45	P9.1	PFC V PHASE IN A
A46	P12.0	PFC V PHASE IN B	B46	P17.0	PFC V PHASE IN C
A47	P12.5	PFC_Overcurrent _Prot	B47	P19.0	PFC V DC OUT 1
A48	P19.1	PFC V DC OUT 2	B48	12.6	PFC NTC
A49	P18.0	PFC_Relay1	B49	P18.1	PRC_Relay2
A50	P18.6	PWM SYNCHRO RECT HIGH	B50	P18.7	PWM SYNCHRO RECT LOW

3.7 ADC input buffers

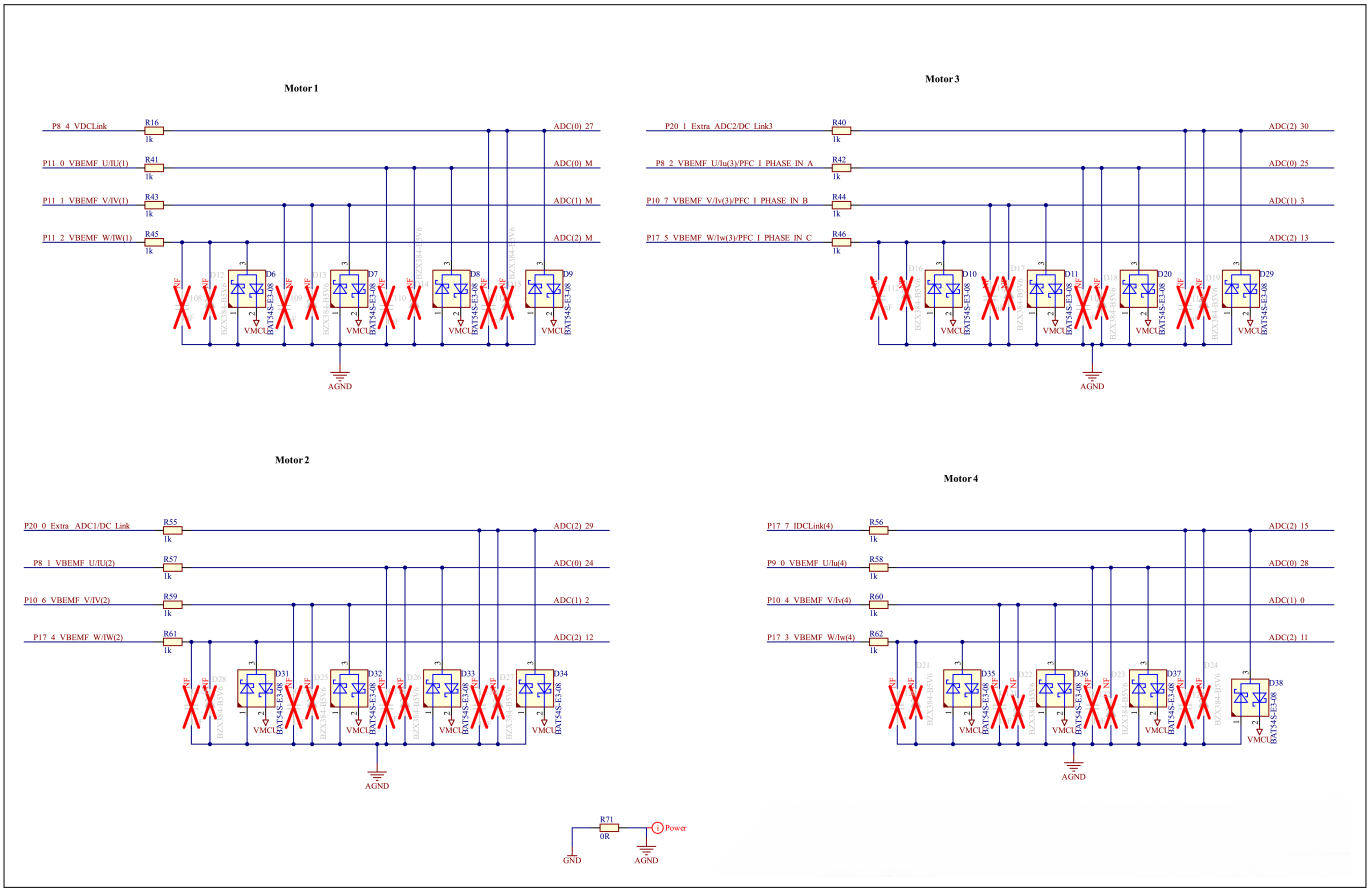

Figure 20 ADC signal input buffers and scaling circuit

The analog signals from power stages, such as phase currents, back electromotive force (BEMF) voltages, DC link current, and bus voltage, are protected by a circuit that includes a Schottky diode. This protection circuit is designed to prevent damage to the MCU analog pins. The analog pins of the MCU can sense ADC signals from the power board within the range of 0 to 5 V.

3.8 Reset and user buttons

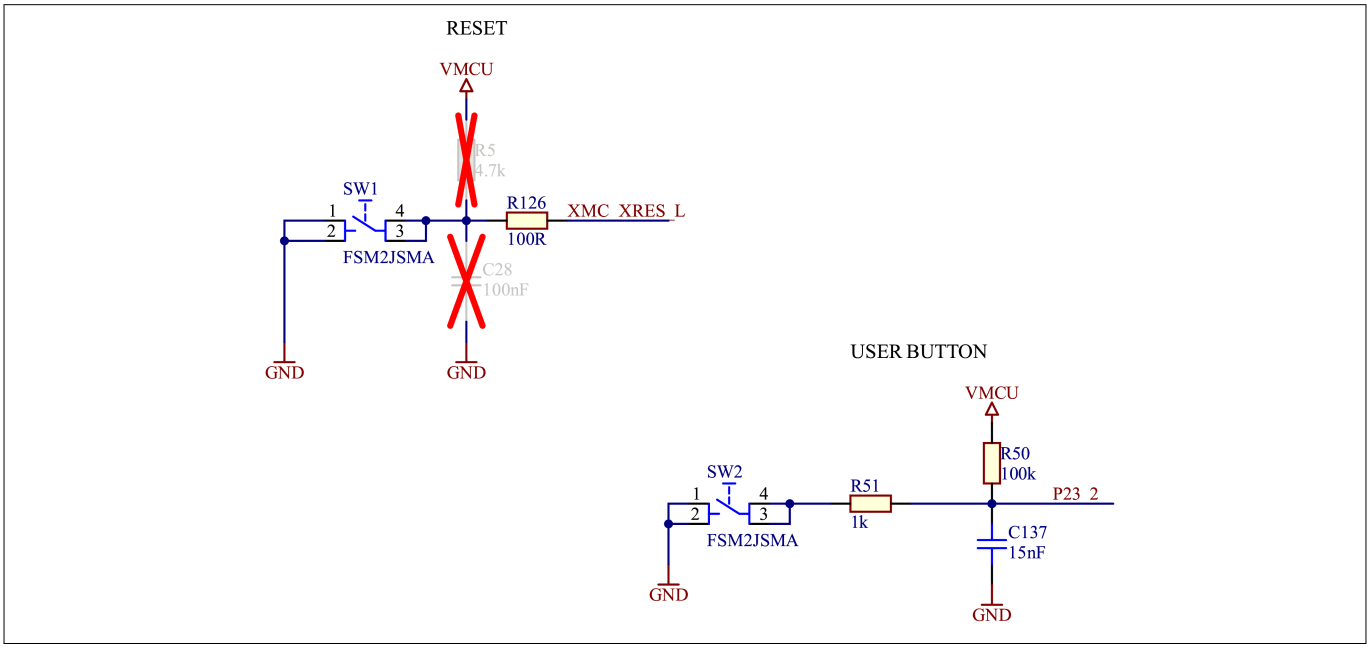

Figure 21 Reset and user buttons

The board is equipped with a reset button (SW1) connected to the TRAVEO™ T2G CYT4BF MCU XRES_L pin. Additionally, it includes a user button (SW2) that can be utilized to alter the motor's direction of rotation or for other user-defined operations.

Table 5 Reset and user button connection details

Designator	Name	Connected to signal	TRAVEO™ T2G CYT4BF pin
SW1	RESET	XRES_L	XRES_L
SW2	USER BUTTON	User_switch	P23.2

3.9 Potentiometers and user LEDS

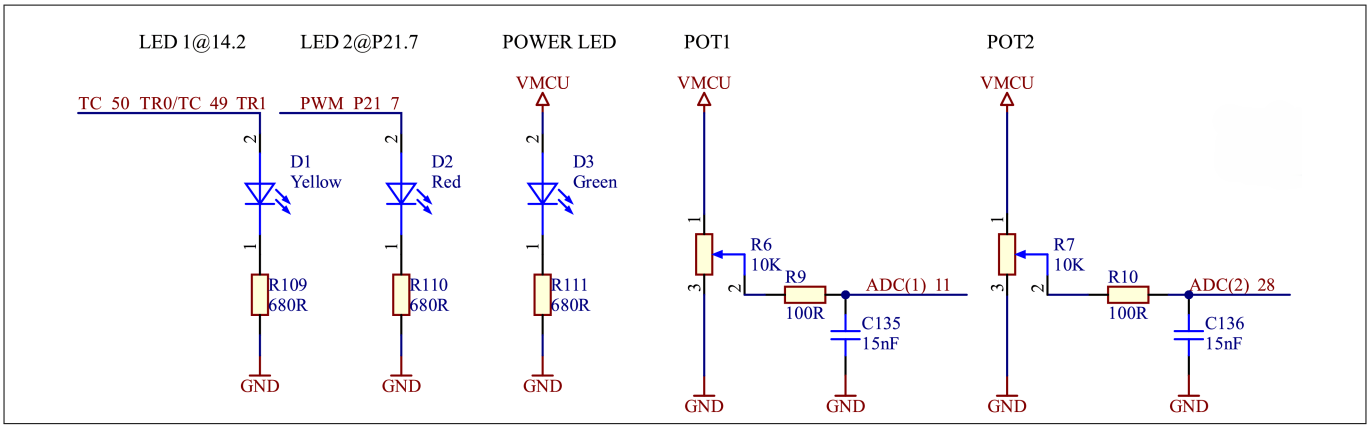

Figure 22 Potentiometers and user LEDs

The board features two potentiometers connected to the ADC inputs, allowing for precise control of the motor's speed. Furthermore, two user LEDs (D1 and D2) can be controlled using the MCU GPIOs. When a current of 3.3 V or 5.0 V is supplied through the VMCU power line, the green power LED (D3) switches on.

Table 6 Potentiometer and user LED connection details

Designator	Name	Connected to signal	TRAVEO™ T2G CYT4BF pin
POT1	Potentiometer 1	ADC(1)_11	P12.7
POT2	Potentiometer 2	ADC(2)_28	P19.4
D1	User LED1	TC_50_TR0/TC_49_TR1(X17)	P14.2
D2	User LED2	PWM_P21_7(X16)	P21.7

3.10 Digital isolators and CAN interface

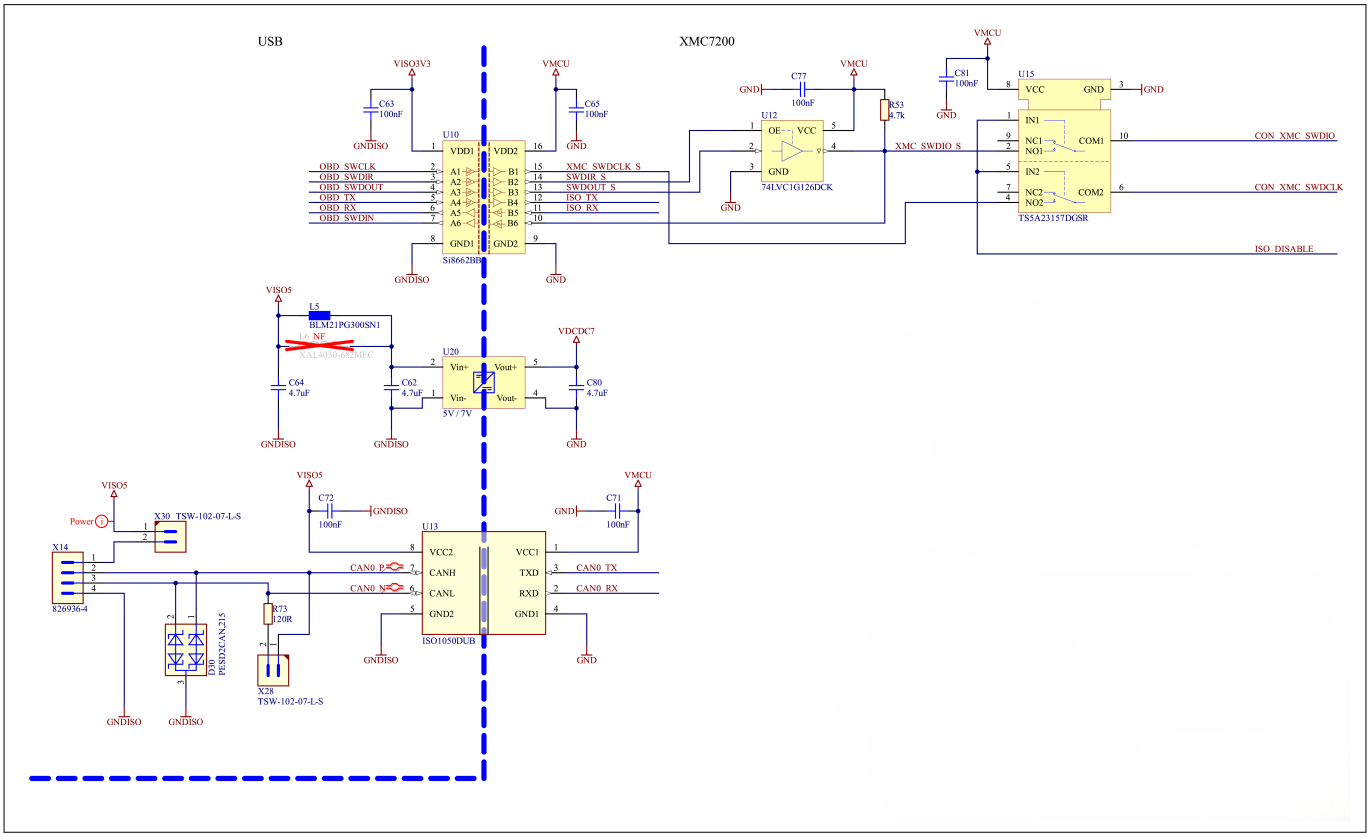

Figure 23 Digital isolators and CAN interface

Isolation for the SWD and UART lines is achieved using a digital isolator (U10). The CAN signal uses a dedicated isolator (U13), and the USB power supply is isolated from the target side using an isolated DC-DC converter (U20). An isolated CAN interface is available on the X14 header. Additionally, by mounting the X28 jumper, a 120 Ω termination resistor can be enabled on the CAN_P and CAN_N lines.

Table 7 CAN header (X14) pinout details

Pin	Signal name	TRAVEO™ T2G CYT4BF Pin	Description
1	VISO5	-	+5 V supply
2	CAN0_P	CAN0_TX (P23.0)	CAN0_TX signal from the MCU
3	CAN0_N	CAN0_RX (P23.1)	CAN0_RX signal to the MCU
4	GND	GND	Power

3.11 TRAVEO™ T2G CYT4BF MCU clock architecture

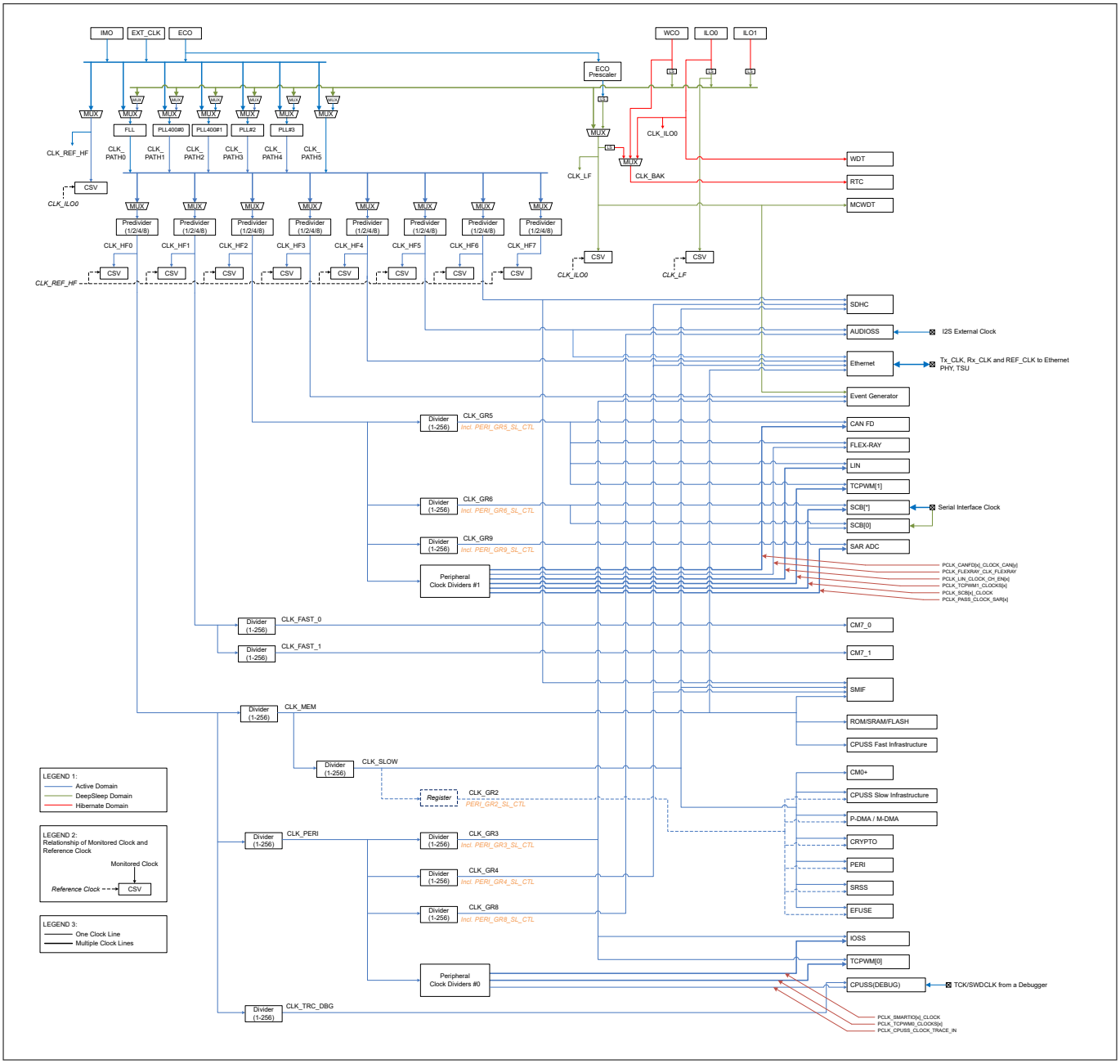

Figure 24 TRAVEO™ T2G CYT4BF MCU clock architecture

Figure 24 shows the MCU clocking scheme. A 16 MHz external clock oscillator (ECO) serves as the source for PLL400M0 and PLL400M1. PLL400M0 is configured to 200 MHz and supplies the clock to CLK_HF0 and CLK_HF2 via CLK_PATH1. Peripheral Group 0 is configured to 100 MHz using CLK_HF0, while Peripheral Group 1 is configured to 100 MHz via CLK_HF2. The TCPWM and ADC utilize the Peripheral clock from Group 1, running at 100 MHz. PLL400M1 is configured to 350 MHz and supplies the clock to CLK_HF1 via CLK_PATH2. The CPU core CM7_0 operates at 350 MHz using CLK_FAST0.

3.12 TRAVEO™ T2G CYT4BF MCU external programming/debugging headers

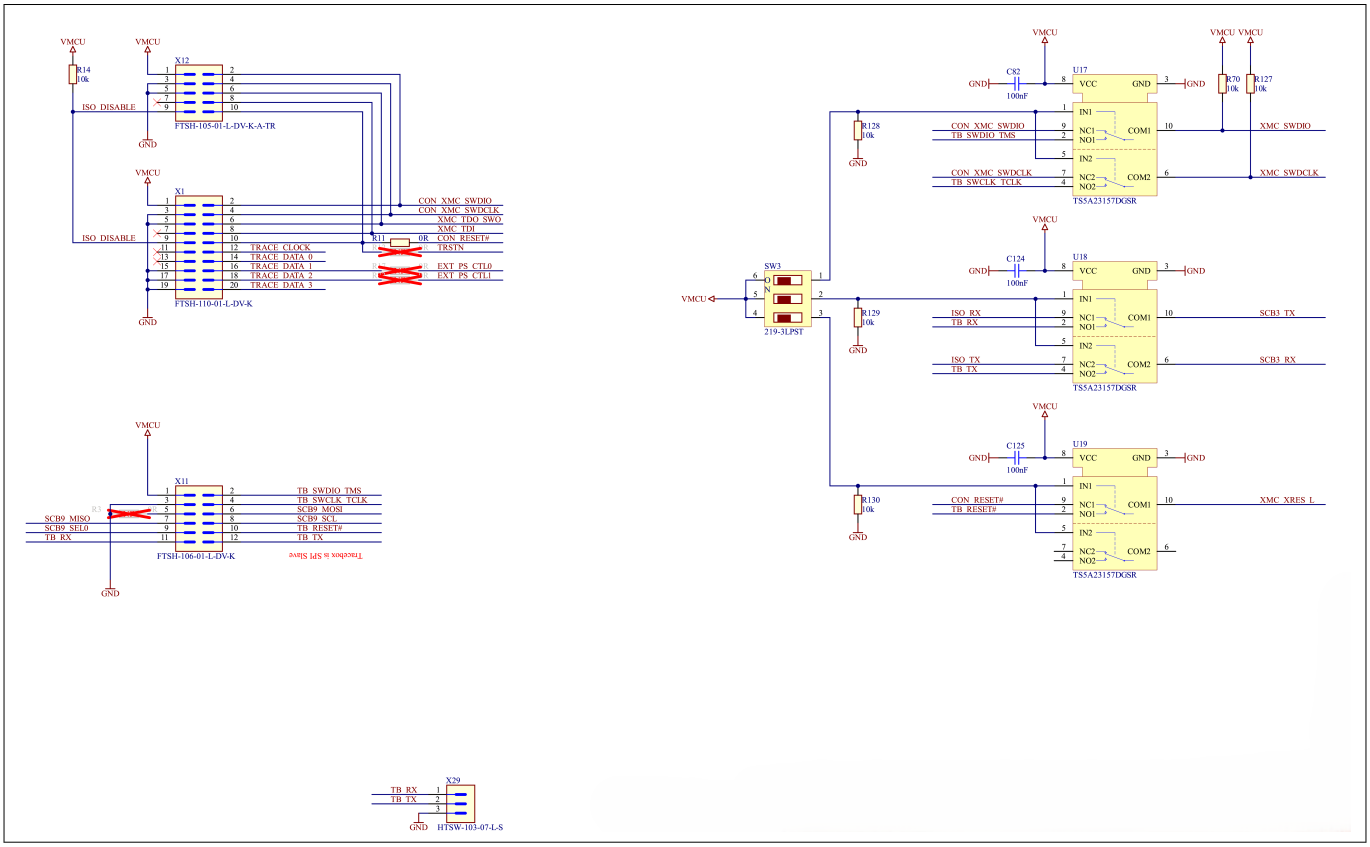

Figure 25 External debugger connections

The board features a 10-pin Cortex® header (X12) and a 20-pin ETM Trace header (X1). Additionally, it features a proprietary 12-pin header with SWD, UART, and SPI interfaces (X11). All headers have a 1.27 mm pitch.

The selection between the onboard debugger or the Cortex® 10-pin header (X12) and the proprietary 12-pin header (X11) is managed using SW3 DIP switches.

SW3 DIP switches should be in the default position where all switches are towards 1,2,3 for using an external debugger on X1 or X12 headers. The Low ISO DISABLE signal coming from the external debugger on pin 9 of the X12 or X1 headers will automatically disconnect the onboard debugger.

***Note**: The external debugger or serial interface is not isolated.*

3.13 XMC4200 as an onboard programmer/debugger

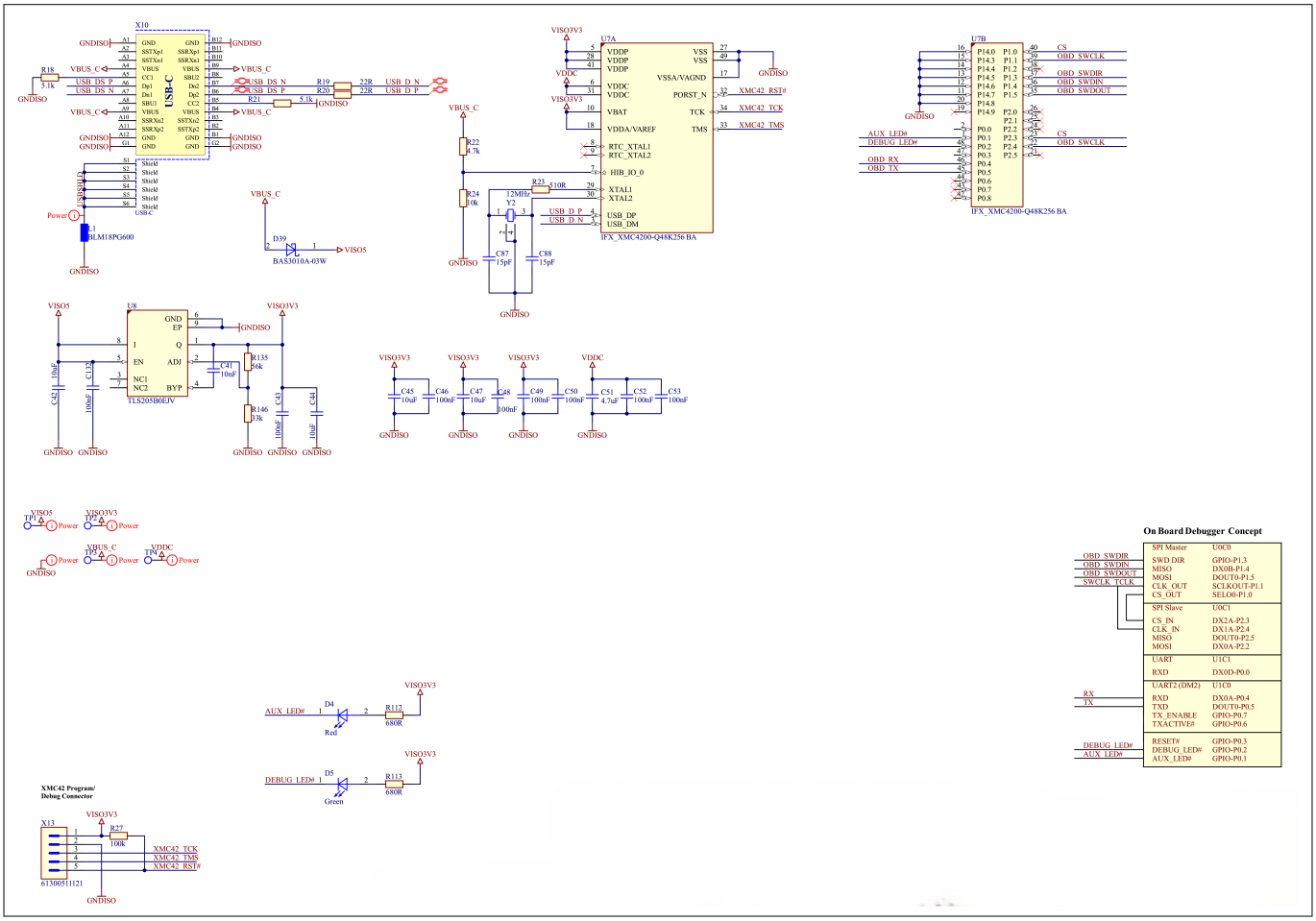

Figure 26 XMC4200-based J-Link lite programmer/debugger

The onboard J-Link LITE programmer or debugger based on XMC4200 (U7) provides the SWD interface as well as a UART interface over USB for the target MCU. The XMC4200 MCU is powered using a 5 V USB supply converted to 3.3 V using the (U8) voltage regulator. The Debug LED (D5) switches on when the USB interface is connected to the PC. Additionally, the Aux LED (D4) blinks during active communication between the debugger and the target MCU. Test points TP1, TP2, TP3, and TP4 can be used to measure the different power rail voltages. X13 is a factory programming header for the XMC4200 MCU that hosts the J-link firmware to enable the J-link interface with the TRAVEO™ T2G CYT4BF MCU.

3.14 Hall sensor and encoder interface

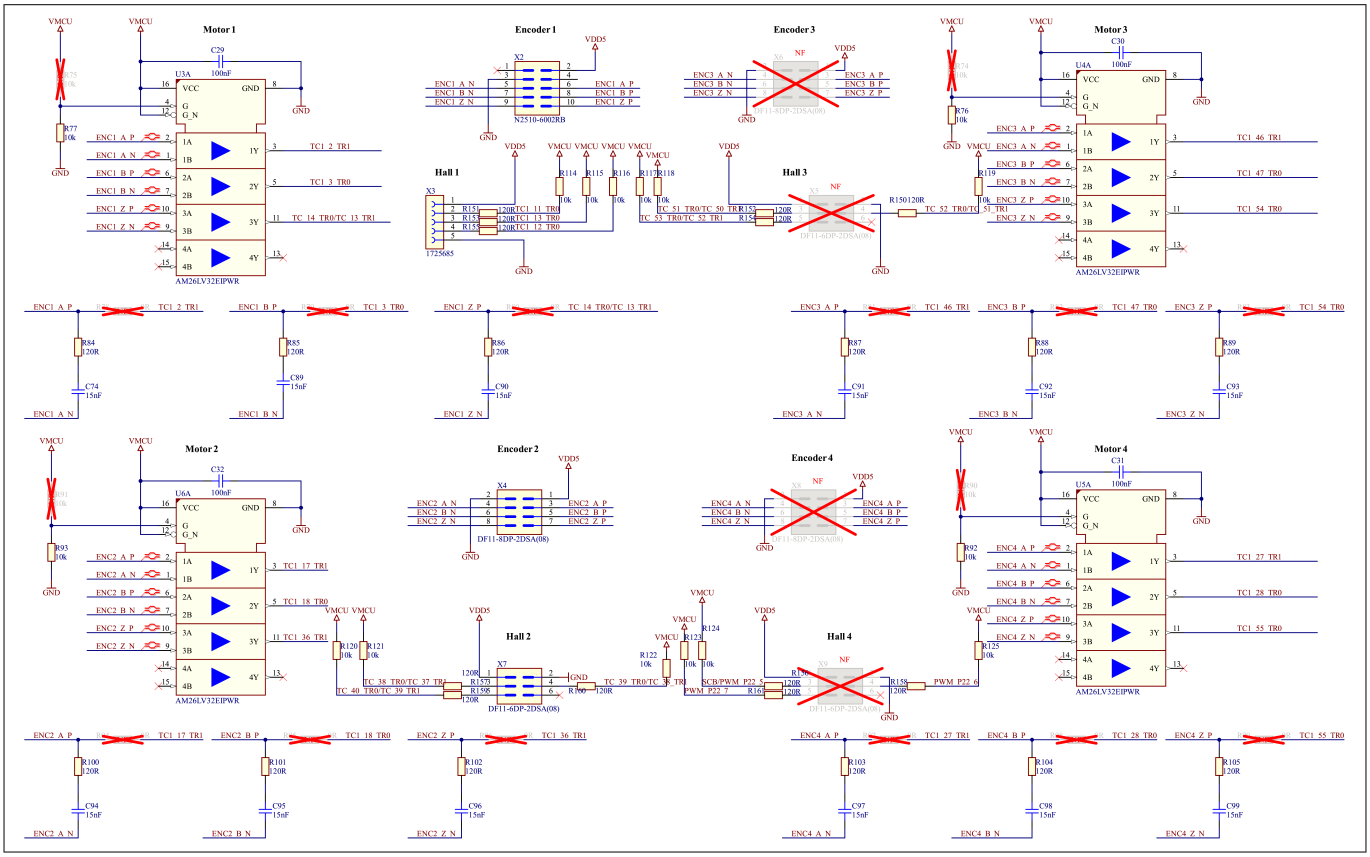

Figure 27 Hall sensor and encoder interface

The Hall sensor (X3, X7, X5, and X9) and encoder interface (X2, X4, X6, and X8) allow users to connect motors with Hall sensors or incremental encoders for sensor-based motor control applications. The board supports both differential as well as single-ended ABZ encoders. When using single-ended encoders, the input signal is connected to ENCx_A_P, ENCx_B_P, and ENCx_Z_P pins of X2, X4, X6, and X8 connectors, while the corresponding N lines are connected to GND.

***Note**: For Motor 3 and Motor 4 headers, the Encoder and Hall sensors are not mounted as default on the board.*

Table 8 Hall 1 (X3) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	P5.2	Hall 1 input for motor 1
3	P5.4	Hall 2 input for motor 1
4	P5.3	Hall 3 input for motor 1
5	GND	Ground

Table 9 Hall 2 (X7) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P12.2	Hall 1 input for motor 2
4	P12.3	Hall 2 input for motor 2
5	P12.4	Hall 3 input for motor 2
6	-	-

Table 10 Hall 3 (X5 - not mounted) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P14.3	Hall 1 input for motor 3
4	P14.4	Hall 2 input for motor 3
5	P14.5	Hall 3 input for motor 3
6	-	-

Table 11 Hall 4 (X9 - not mounted) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P22.5	Hall 1 input for motor 4
4	P22.6	Hall 2 input for motor 4
5	P22.7	Hall 3 input for motor 4
6	-	-

Table 12 Encoder 1 (X2) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	-
2	-	+5 V supply VDD5
3	GND	Ground
4	-	-
5	-	ENC1_A_N for motor 1
6	P6.6	ENC1_A_P for motor 1
7	-	ENC1_B_N for motor 1
8	P6.7	ENC1_B_P for motor 1

(table continues...)

Table 12 (continued) Encoder 1 (X2) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
9	-	ENC1_Z_N for motor 1
10	P5.5	ENC1_Z_P for motor 1

Table 13 Encoder 2 (X4) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P7.6	ENC2_A_P for motor 2
4	-	ENC2_A_N for motor 2
5	P7.7	ENC2_B_P for motor 2
6	-	ENC2_B_N for motor 2
7	P12.1	ENC2_Z_P for motor 2
8	-	ENC2_Z_N for motor 2

Table 14 Encoder 3 (X6 - not mounted) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P13.6	ENC3_A_P for motor 3
4	-	ENC3_A_N for motor 3
5	P13.7	ENC3_B_P for motor 3
6	-	ENC3_B_N for motor 3
7	P14.6	ENC3_Z_P for motor 3
8	-	ENC3_Z_N for motor 3

Table 15 Encoder 4 (X8 - not mounted) pinout details

Pin	TRAVEO™ T2G CYT4BF pin	Description
1	-	+5 V supply VDD5
2	GND	Ground
3	P19.2	ENC4_A_P for motor 4
4	-	ENC4_A_N for motor 4
5	P19.3	ENC4_B_P for motor 4
6	-	ENC4_B_N for motor 4
7	P14.7	ENC4_Z_P for motor 4
8	-	ENC4_Z_N for motor 4

3.15 Drive adapter card

The drive adapter card provides the following interfaces:

- 100-pin HD connector for the control card
- 2x M1/M3 connectors for compatible MADK power boards
- 1x M5 connector for compatible MADK power boards
- 2x Samtec connectors for compatible power boards
- Expansion header interface with standard 2.54 mm pitch

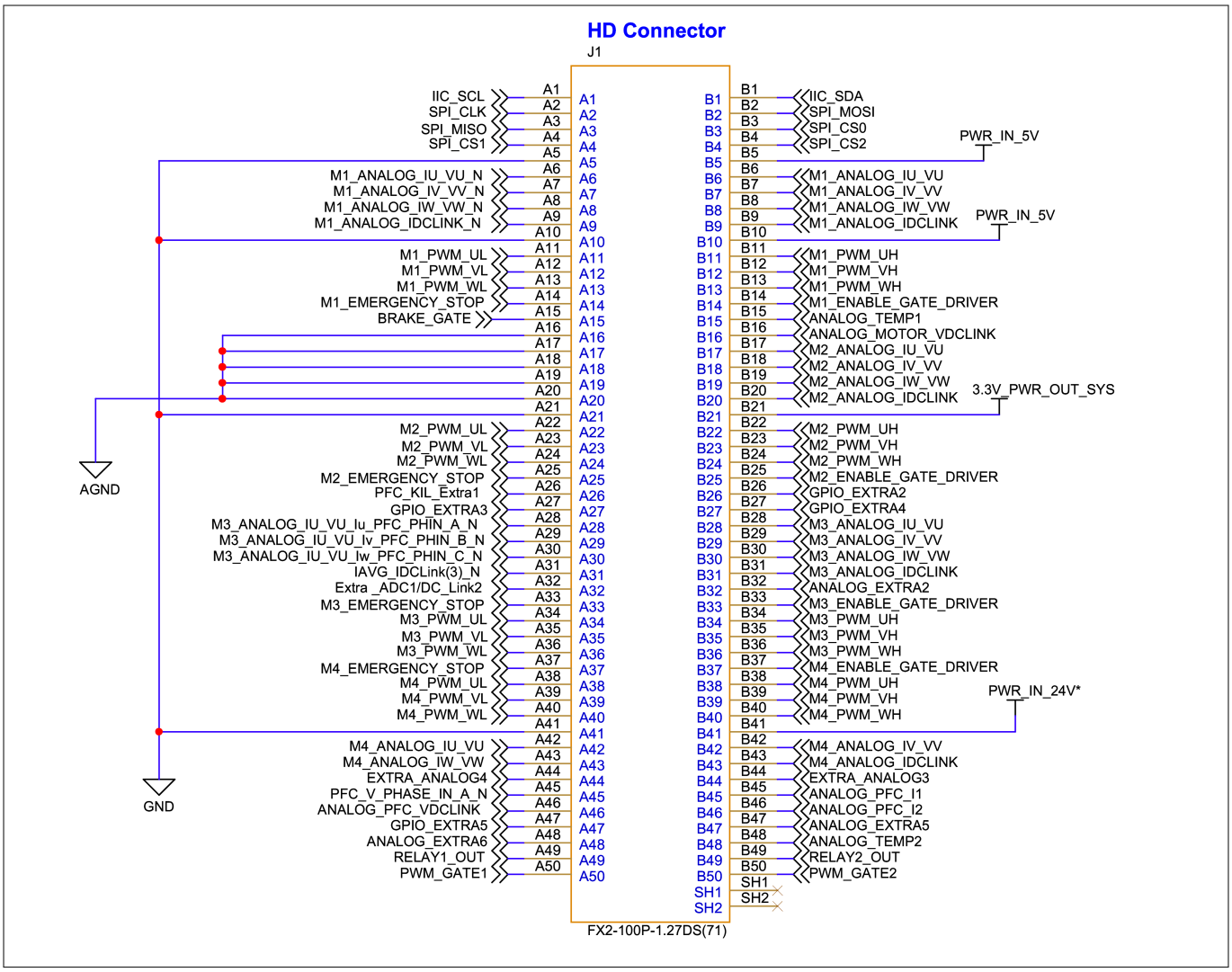

Figure 28 Drive adapter card 100-pin HD connector

3 Hardware

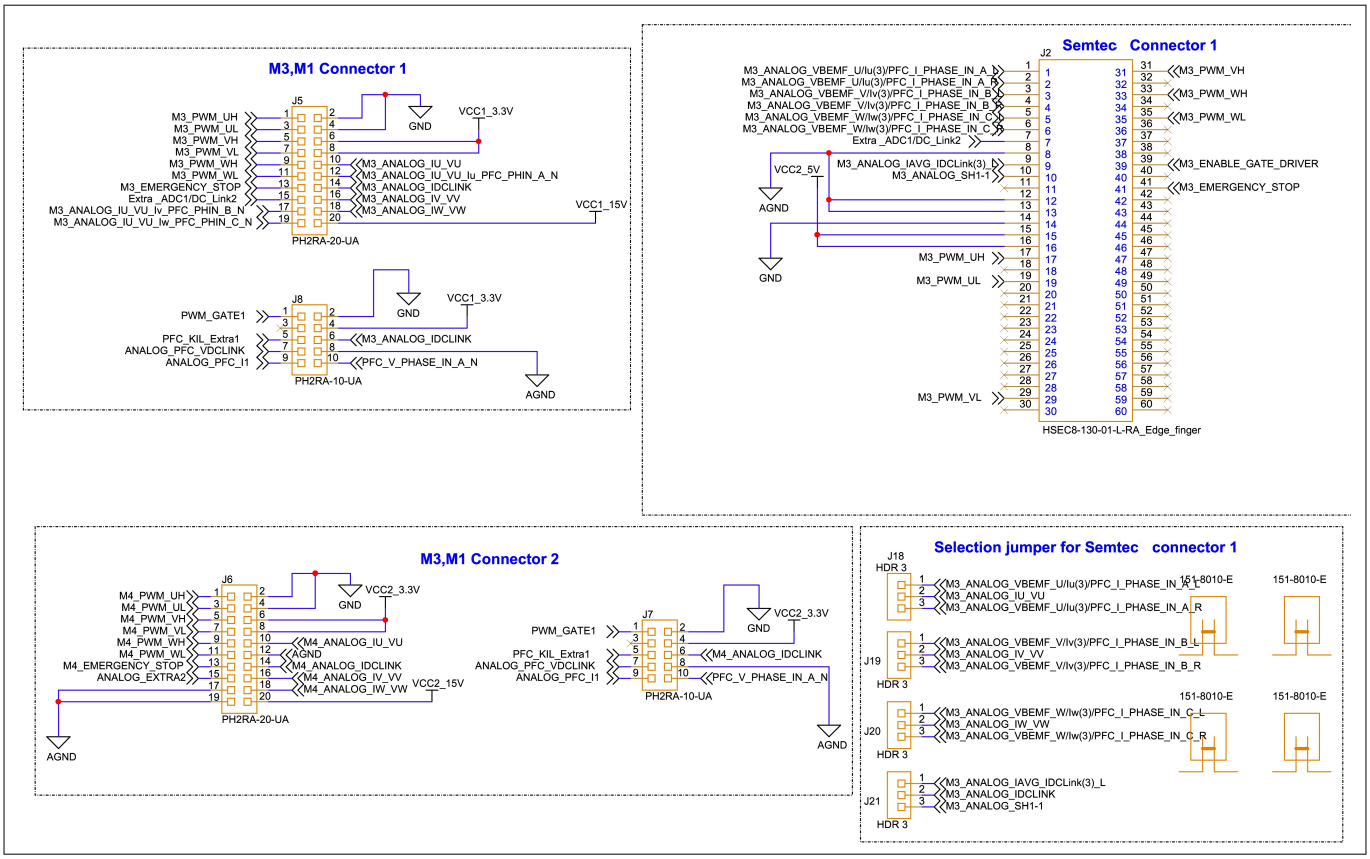

Figure 29 M3, M1 connectors, and Samtec connector 1

3 Hardware

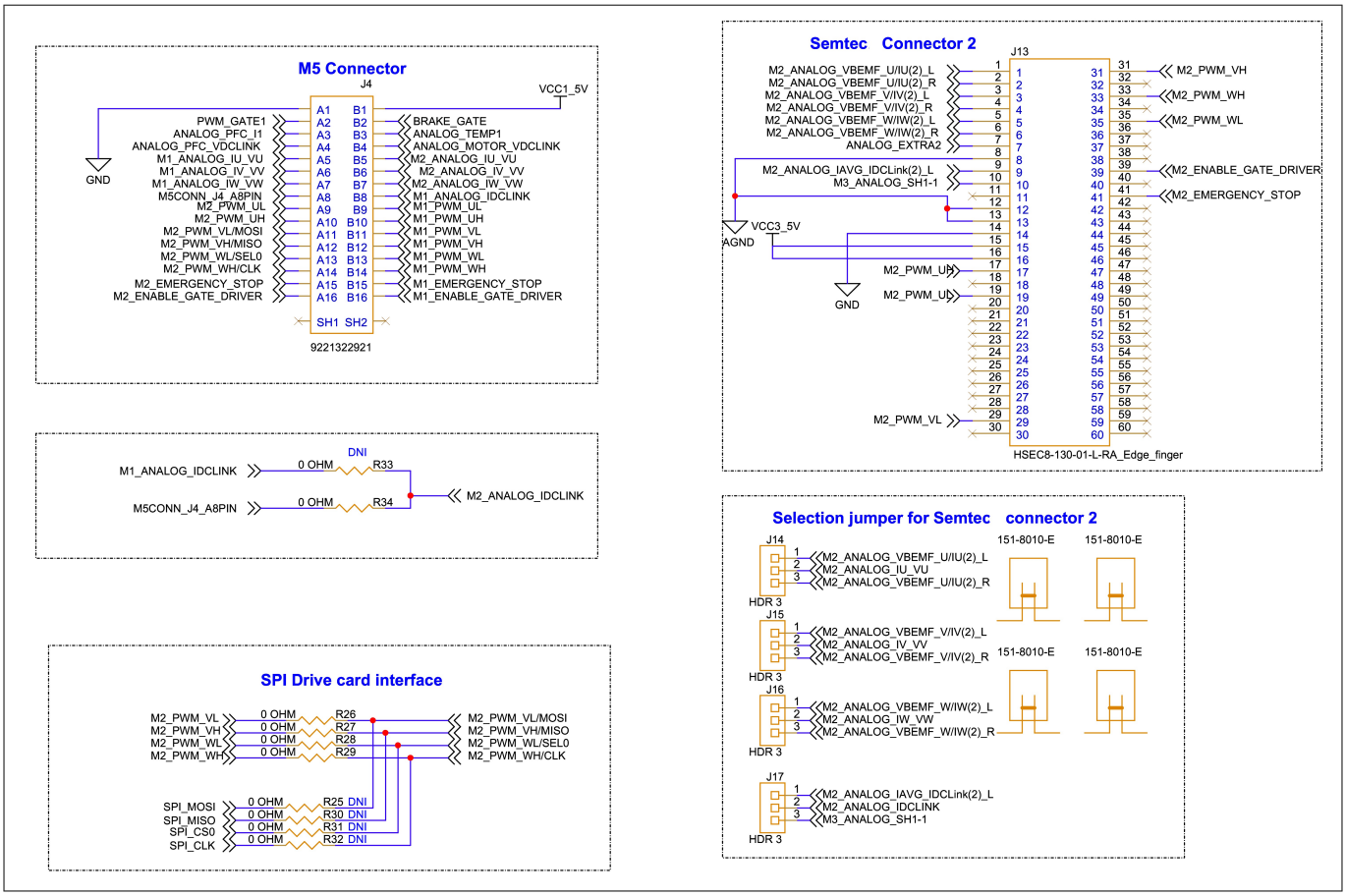

Figure 30 M5 connector and Samtec connector 2

3 Hardware

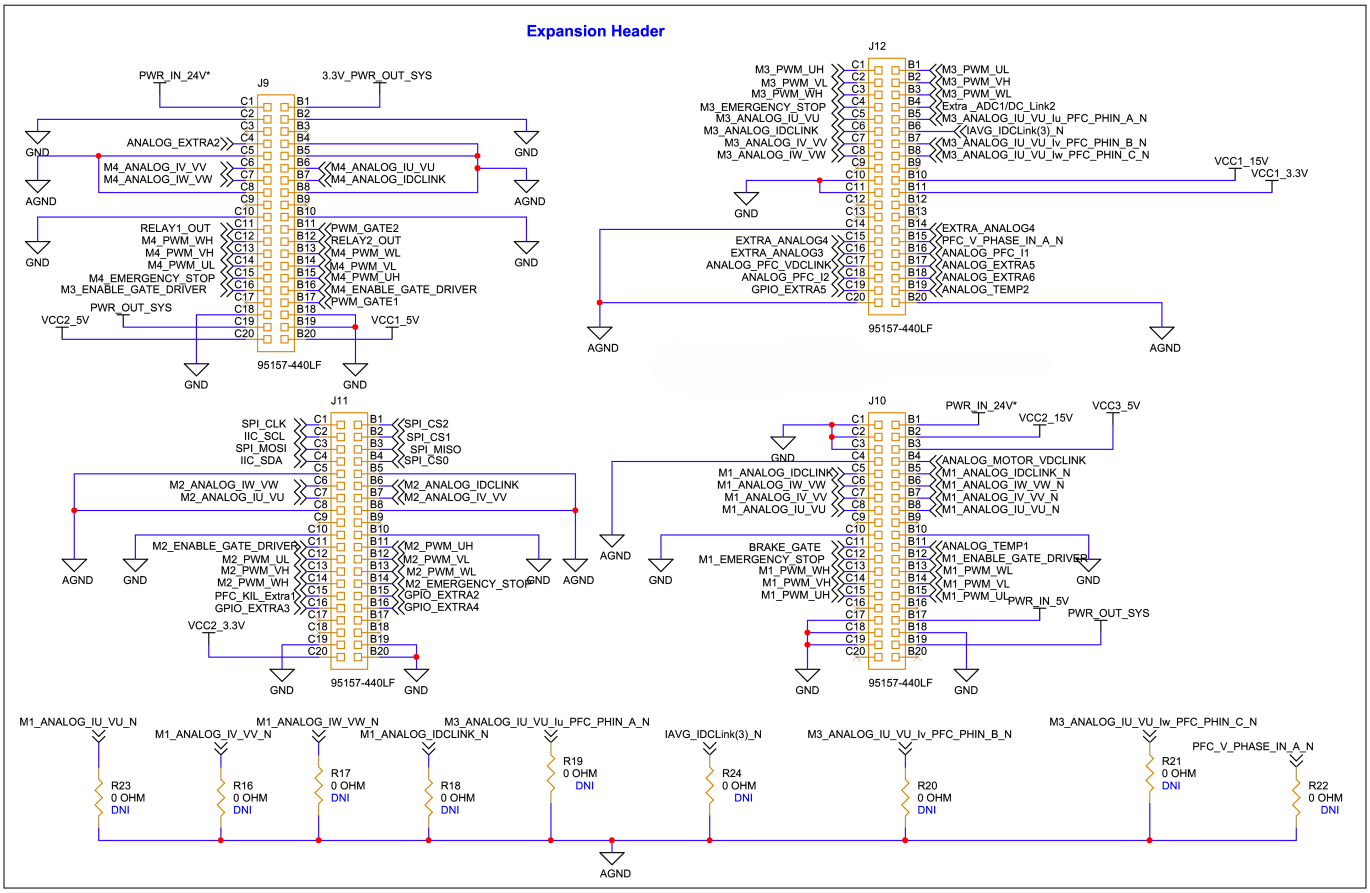

Figure 31 Drive adapter card expansion headers

3.16 KIT_MOTOR_DC_250W_24V_T2G power board

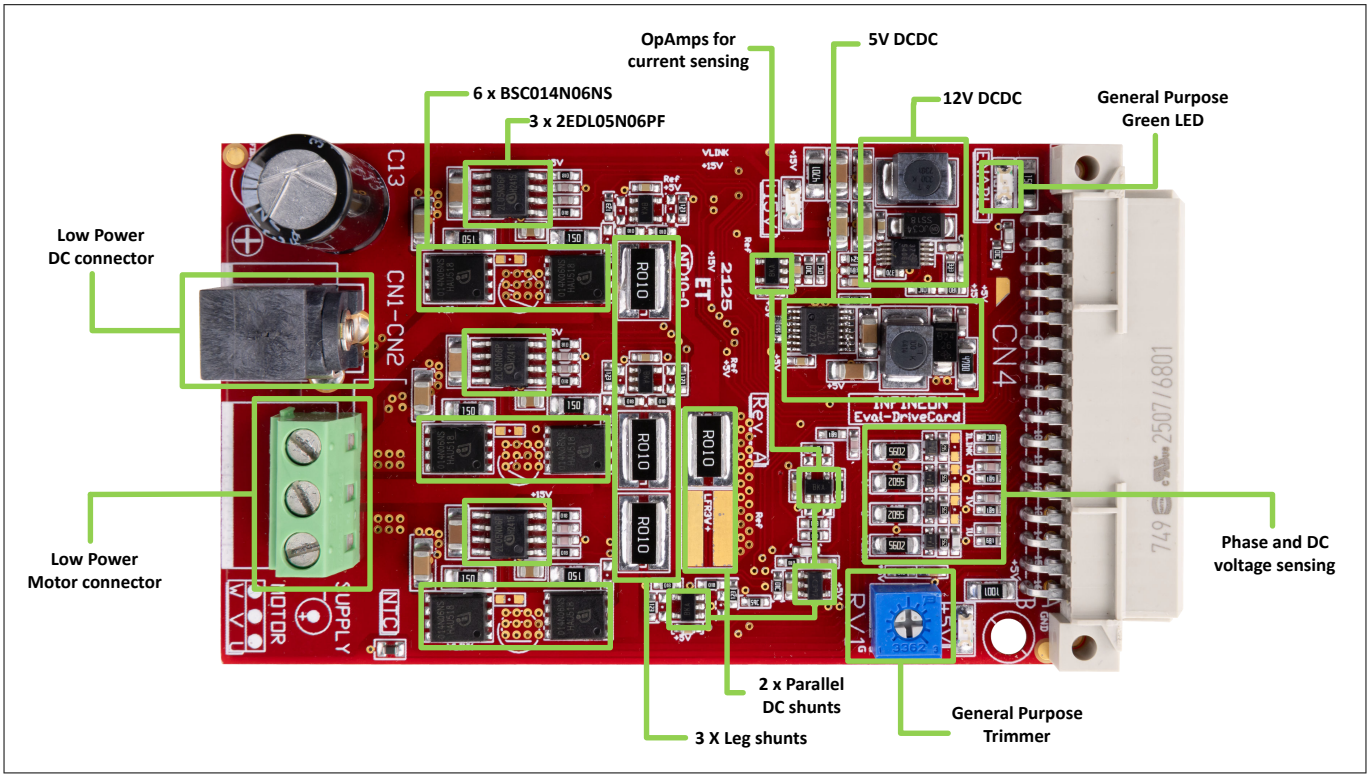

Figure 32 KIT_MOTOR_DC_250W_24V_T2G details

The KIT_MOTOR_DC_250W_24V_T2G features an MADK M5 interface, enabling it to drive a 24 V BLDC motor in three shunt or single shunt field-oriented control, as well as trapezoidal block commutation mode. For complete information about this kit, including schematics, and design files, see KIT_MOTOR_DC_250W_24V_T2G.

Table 16 Important board parameters when used with KIT_TRAVEO_T2G_B_H_DC_V1 motor control card

Parameter	Value
Zero current offset voltage	2.5 V
Shunt value	0.01 Ω
Overall current gain	12
Max measurable current	20.83 A
I_{TRIP} (Fault output trigger threshold)	25 A
Bus voltage attenuation factor	0.0909
Max measurable bus voltage	55 V
BEMF attenuation factor	0.0909

4 Production data

The schematics of KIT_TRAVEO_T2G_B_H_MC1 motor control evaluation kit can be downloaded from the kit webpage.

Revision history

Document revision	Date	Description of changes
**	2025-08-13	Initial release.

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