TriBoard TC4X7 COM

Hardware: TriBoard TC4X7 COM V3.0

About this document

Scope and purpose

The User Manual provide information about using, configuration and connecting the **TriBoard TC4X7 COM** with Infineon **AURIX™** TC4X7 (TC497A, TC4D7, TC4Z7, TC487, TC447) in the COM package.

This **TriBoard TC4X7 COM** Hardware Manual familiarizes you with the TriCore™ Evaluation Board and guides you through the initial configuration of the TriBoard.

Intended audience

Design, verification, test and software engineers will use this document to get an understanding of the functionality and connections of the **TriBoard TC4X7 COM**.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *The heat sink and device surfaces of the evaluation board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *The evaluation board contains parts and assembly's sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

This document describes the features and hardware details of the **TriBoard TC4X7 COM** equipped with a

32-Bit Single-Chip AURIX™ TriCore™-based Microcontroller TC4X7 in COM package from Infineon Technologies AG.

It can be used with a range of development tools including Infineon's free of charge Eclipse based IDE **AURIX™ Development Studio** (limited). AURIX™ Development Studio is a comprehensive environment, including C-Compiler and Multi-core Debugger, Infineon's low-level driver (iLLD), with no time and code-size limitations that enables editing, compiling and debugging application code.

Table 1 shows the overview specifications of the whole board.

Table 1 Overview of the Board Specification

CPU Core AURIX™	Usable devices	TC4D7 TC497A COM package TC487 COM package TC4Z7 TC447 COM package (planned, not yet tested, all information's are preliminary)
Power	• external powering 4 V…35 V (recommended 7 V...28 V)	
Features	• SD card slot for MicroSD • FlexRay™ [1)] Transceivers • High Speed CAN Transceivers (CAN-FD capable) • USB to UART bridge • 10/100/1000M/2.5 G Ethernet PHY • Semper® Flash with Hyperbus™ Interface • Serial Eeprom • LIN Transceiver • Crystal 25MHz • USB miniWiggler JDS for easy debugging • 8 Low Power Status LEDs • 4-DIP switches for configuration • access to all pins of controller • 100mm x 160mm (EURO-Board)	
Connectors	• Standard power connector • Micro USB connector for ASC Interface (ASC0) and miniWiggler • 2 x RJ45 connector for Ethernet • OcuLink connector for PCIe • USB C-type socket as HSTCU connector • 3 x 10-pin header for DAP, DAPE and DAP_SCR (DAPE only usable on Emulation Device) • 10pin (2x5) Header for LIN Transceiver (LIN)	

Table 1 Overview of the Board Specification

	• 2 x 10pin (2x5) Header for CAN High Speed Transceiver (CAN0 and CAN1) • 2 x 10pin (2x5) Header for FlexRay™ (ERAY-A and ERAY-B) • four 80-pin connectors (male) + four 80-pin connectors (female) with most I/O signals • optional ETK connector • optional 2 x 6pin (IEEE1394) Socket for HSCT
Components	• Infineon Functional Safety PMIC OPTIREG™ PMIC TLF4D985QKV03 • Three LEDs to validate power supply (VCORE / 1,8 Volt / QUC) • LED indicating safe state signal 2 from TLF4D985 • LED indicating RESET (/ESR0) active state • LED indicating active miniWiggler JDS (ACT) • LED switched via DAS software (RUN) • 2 x NXP FlexRay™ [1] Transceiver TJA1081BTS • 2 x Infineon High-Speed CAN-Transceiver TLE9371VSJ • Infineon LIN-Transceiver TLE 7259-3GE • FTDI USB to UART bridge FT2232HL • 2 x Realteks Integrated 10/100/1000M/2.5G Ethernet transceiver RTL8221B-CG • Cypress Semper® Flash S26HS512TGABHM000 • 8 general purpose LEDs (P33.0, P33.1, P33.4, P33.5, P13.0, P13.1, P13.2, P13.3) • 2 x Microchip 2K I2C Serial Eeprom with EUI-64™ [2] Node Identity • Reset push-button (PORST) • Enable push-button (ENA) • Generic push-button (P33.11) • 4-pin Dip switch (CONFIG)

1) *FlexRay™ is a trademark of FlexRay Consortium.*

2) *EUI-64™ is trademarked by IEEE*

These boards are neither cost nor size optimized and do not serve as a reference design.

1.1 Block diagram

- The block diagram in **Figure 1** shows the main components of the **TriBoard TC4X7 COM** and their interconnections.

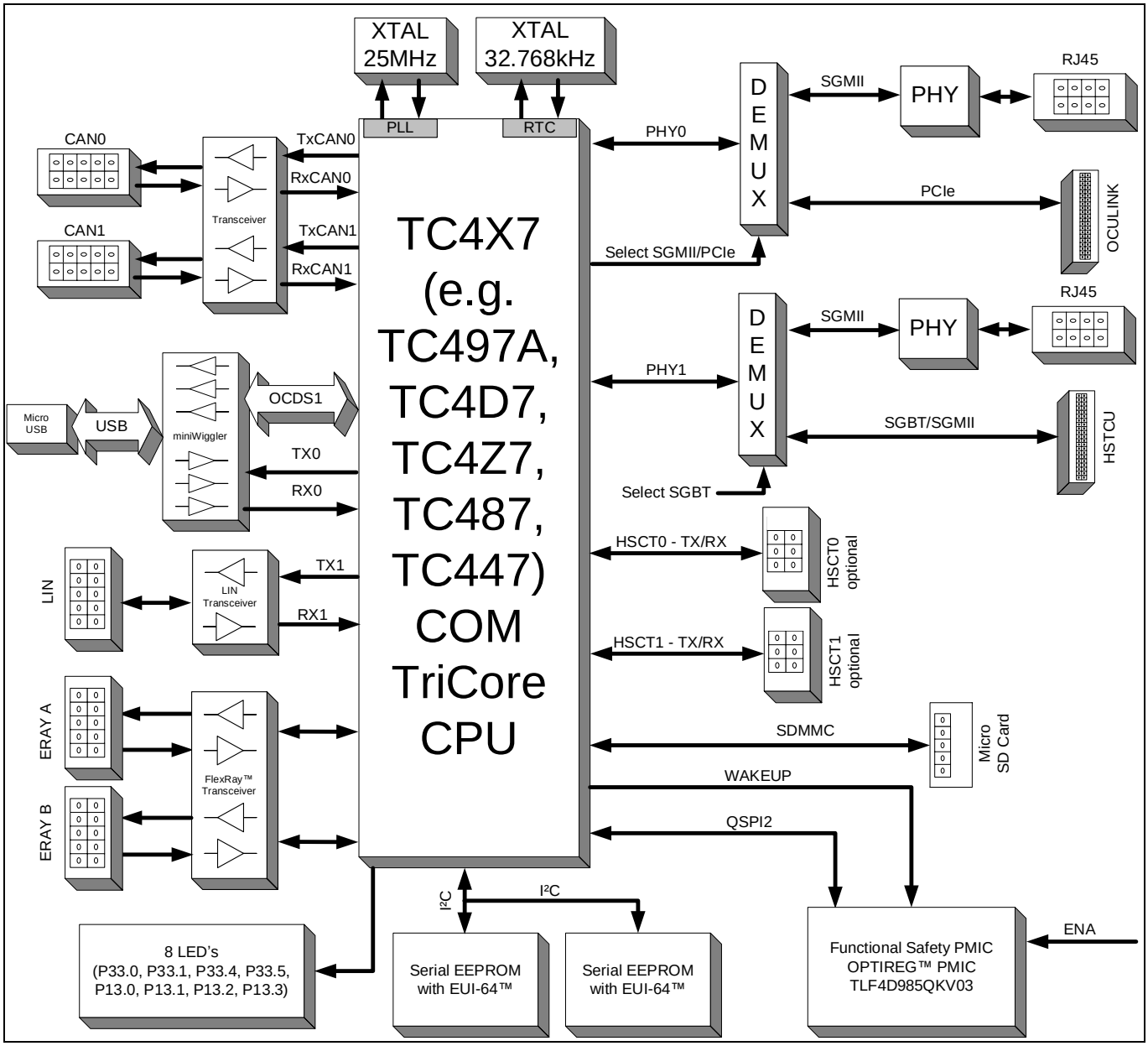


Figure 1 Block Diagram of the TriBoard TC4X7 COM

2 Hardware Description

The following chapters give a detailed description of the board hardware and how it can be used. The different parts of the TriBoard are shown in **Figure 2**.

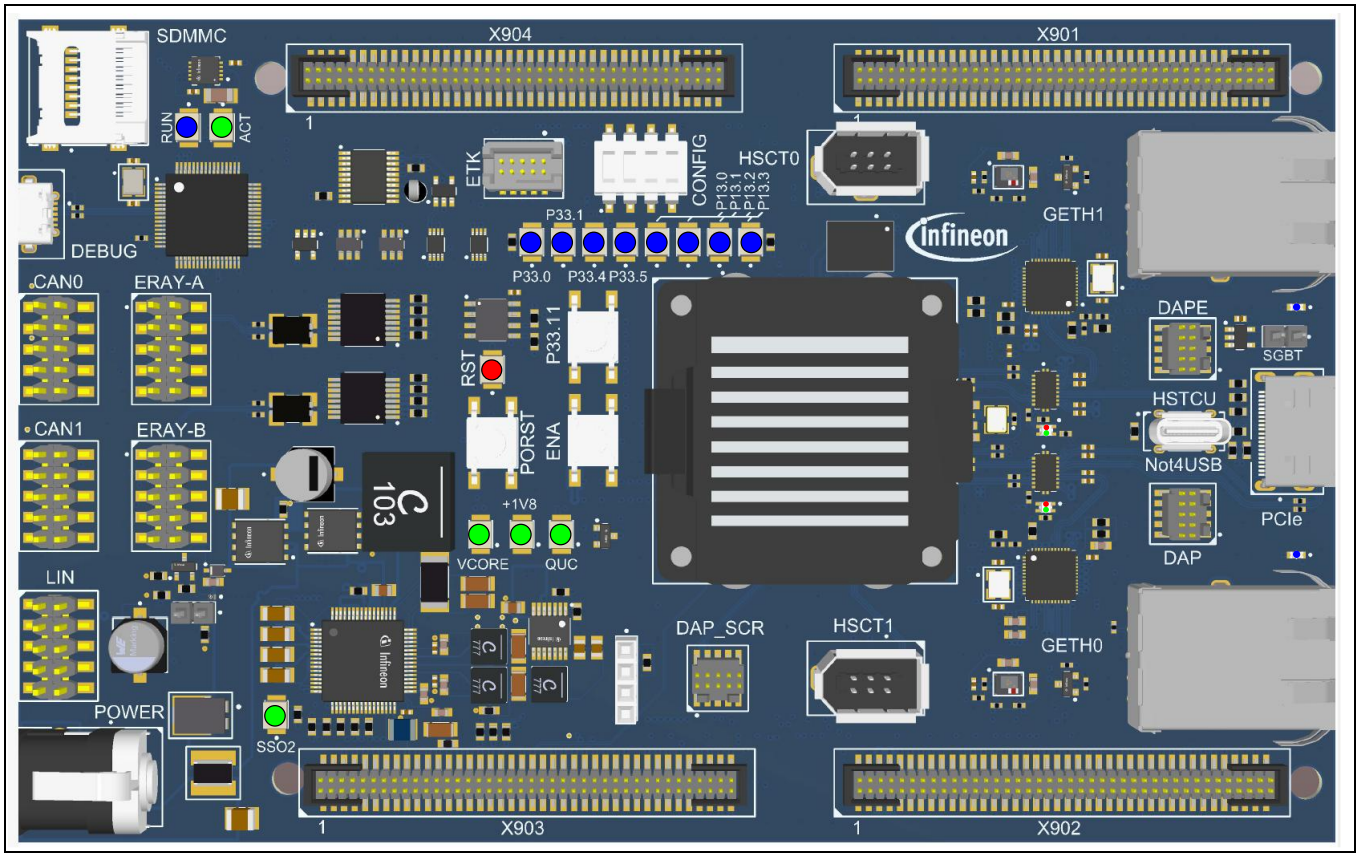


Figure 2 TriBoard TC4X7 COM Board View from the Top

2.1 Usable devices

The **TriBoard TC4X7 COM** is soldered with an **AURIX™** TC4X7 in the COM package or is a socketed board where the device can be easily exchanged. Because the socket is not soldered on the board it is possible to reuse the socket on another board or exchange the socket by a soldered device.

The socketed board can be used with the following devices (other devices will not be usable):

- **AURIX™** TC497A in the COM package
- **AURIX™** TC4D7
- **AURIX™** TC487 in the COM package
- **AURIX™** TC4Z7
- **AURIX™** TC447 in the COM package (planned, not yet tested, all information's are preliminary)

2.2 Power Supply

The **TriBoard TC4X7 COM** must be supplied by an external DC power supply, this can be done via the POWER DC plug X601. For X601 you can use a female DC supply plug with outside diameter of 5.5 mm and inside diameter of 2.1 mm or 2.5 mm. The inner contact is positive and the outer contact is ground. The pinout for the supply connector is shown in **Figure 21**.

The Board has to be connected to a +3,5V to +35V DC power supply.

The power consumption is not specified yet but a supply with 12V and 1A is recommended.

Applying a stable supply voltage causes the power on reset after a short period. The three LED's (VCORE, +1V8, QUC) indicate the status of the on-board generated voltages.

NOTE: ***Without TC4X7 device the TLF4D985QKV03 will go in FAILSAFE mode and the LEDs will be on only for some milliseconds. The board can't be used without AURIX™ TC4X7 device.***

A manual power on reset is executed by pressing the reset button (S202 – /PORST).

In case the TLF4D985QKV03 is switched off then PMIC can be waked up by the ENA button (S601) or via pin P33.6 (SCR: P0.6) from AURIX™.

Before switch off the TLF4D985, make sure that P33.6 (SCR: P0.6) has enable the internal pull-up or is driven high, otherwise the TLF4D985 will go to INIT state instead of going in STANDBY state.

All needed voltages are generated and supervised via Infineon's Functional Safety PMIC OPTIREG™ PMIC TLF4D985QKV03.

The TLF4D985QKV03 provide the following voltages:

+3,3V for standby (QST connected to VDDEVRSB)

+3,3V for TriCore (QUC connected to VDDEXT)

+5V communication supply (QCO used by CAN and FlexRay™ transceivers)

+5V voltage reference (QVR connected to VDDM and VAREFx)

+1,8V for TriCore and Flash (+1V8 connected to VDDPHPHY0, VDDPHPHY1, VDDHSIF and Flash)

+3,3V will be provided from VS via step down regulator controlled by voltage monitor 1 of TLF4D985QKV03 , used by the Ethernet Phys and LVDS demultiplexer.

+1V for TriCore (VCORE connected to VDD)

Table 2 TLF4D985 Signals and AURIX™ Pin Mapping

TLF Signal Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
SCS	P15.2, Master slave select output	QSPI2_SLSO0
SCL	P15.8, Master SPI clock output	QSPI2_SCLK
SDI	P15.6, Master SPI data output	QSPI2_MTSR
SDO	P15.7, Master SPI data input	QSPI2_MRSTB
WAK	P33.6, General-purpose output	P33.6 OUT

(table continues...)

TLF Signal Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
INT1	ESR1, General-purpose input	-
SYNC_IN/INT2	P33.11, ESR2 General-purpose input	SMM_ESR2_PORT_IN
RESOUT	PORST, Power on Reset Input	-
SSO1	P20.9, ERU channel 7 input A	SCU_E_REQ7A
ERR0	P33.12, FSP Output Signal	SMU_FSP1
ERR1	P32.2, FSP Output Signal	SMU_FSP2
WDI/ERR2	P20.3, General-purpose output	P20.3 OUT

2.2.1 Failsafe handling

In case that the device doesn’t contains a program, which disable or service the window watchdog and error pin monitor of the TLF4D985QKV03 then the TLF4D985QKV03 is going to a FAILSAFE state where all supplies are switched off.

This state can be left via reconnect the power plug or via the ENA button (S601). In this case you must connect a debugger which is able to disable the window watchdog and error pin monitor to reprogram the microcontroller.

In the default state of the board the switching to FAILSAFE state is switched off via resistor R614 (100K connected to HWCFG of TLF4D985QKV03).

If you will use/evaluate all safety features of the TLF4D985QKV03 then you should assemble connector X602 (2 pin header) and connect a jumper to X602. Make sure that you have a proper initialization of TLF4D985QKV03 in your software.

Connector X602 is marked in the following **Figure 3**:

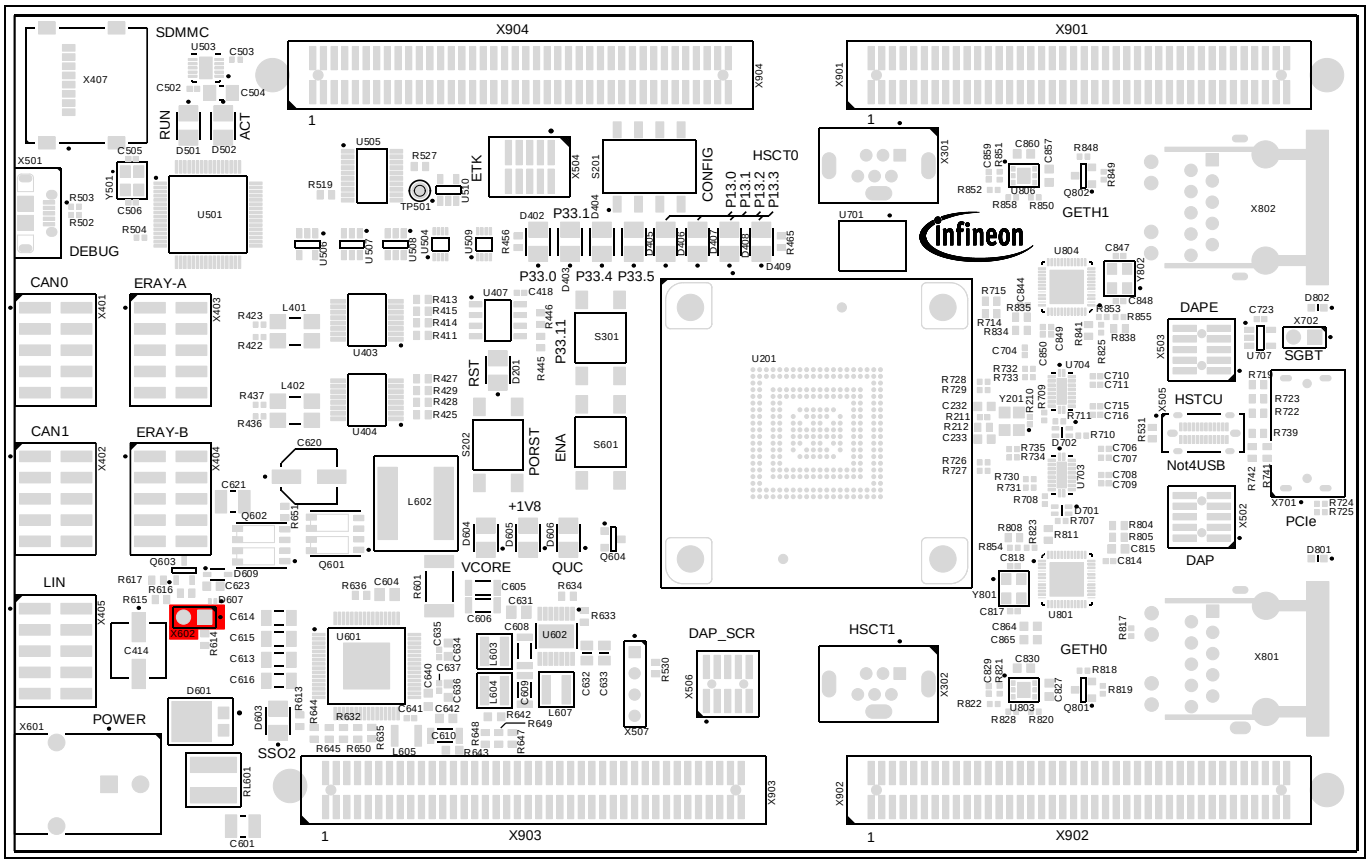


Figure 3 Jumper for switch on TLF4D985QKV03 Safety feature handling

2.3 LEDs

The **TriBoard TC4X7 COM** provides 19 LEDs:

Table 3 AURIX™ Pin Mapping for User LEDs

Name	AURIX™ Pin	Color	Active
D402	P33.0 (SCR: P0.0)	blue	Low-active (pull against GND)
D403	P33.1 (SCR: P0.1)	blue	Low-active (pull against GND)
D404	P33.4 (SCR: P0.4)	blue	Low-active (pull against GND)
D405	P33.5 (SCR: P0.5)	blue	Low-active (pull against GND)
D406	P13.0	blue	Low-active (pull against GND)
D407	P13.1	blue	Low-active (pull against GND)
D408	P13.2	blue	Low-active (pull against GND)
D409	P13.3	blue	Low-active (pull against GND)

Table 4 Miscellaneous LEDs

Name	Functionality	Color	Comment
D201	/ESR0 (RESET)	red	Low-active, device in reset
D501	miniWiggler RUN	blue	Debug RUN mode (switched by DAS Server)

(table continues...)

Table 4 Miscellaneous LEDs

Name	Functionality	Color	Comment
D502	miniWiggler ACTIV	green	on board miniWiggler JDS is ACTIV
D603	SSO2	green	Safe state control output 2 of TLF4D985, high-active
D604	VCORE	green	+1V power supply indication (VCORE)
D605	+1V8	green	+1V8 power supply indication (VDDPHPHYx, VDDHSIF, Flash)
D606	QUC	green	+5V power supply indication (VEXT)
D701	PCIe or SGMII selected	green red	SGMII selected (GETH0 will be used) PCIe selected (OcuLink connector used)
D702	SGMII or SGBT selected	red green	SGMII selected (GETH1 will be used) SGBT selected (PHY1 connected to HSTCU)
D801	PHY LED2	blue	LED2 of PHY RTL8221B-CG (U801 used as GETH0)
D802	PHY LED2	blue	LED2 of PHY RTL8221B-CG (U804 used as GETH1)

For location of the LEDs please see **Figure 2**.

2.4 Clock

2.4.1 Main crystal

On the board is a fixed crystal with 25MHz (CEC K-F-25.000M-08-15150-40125-80-A) assembled. You can change this by replacing Y201 (soldered). Per default XTAL1 and XTAL2 are not connected to X902/X1002. If the signals are needed on the 80 pin Samtec connectors (e.g., for measurement) then 0R resistors (size 0402) at R210 and R211 must be assembled. Please note that this can disturb the signal quality.

All mentioned parts are marked in the following **Figure 4**:

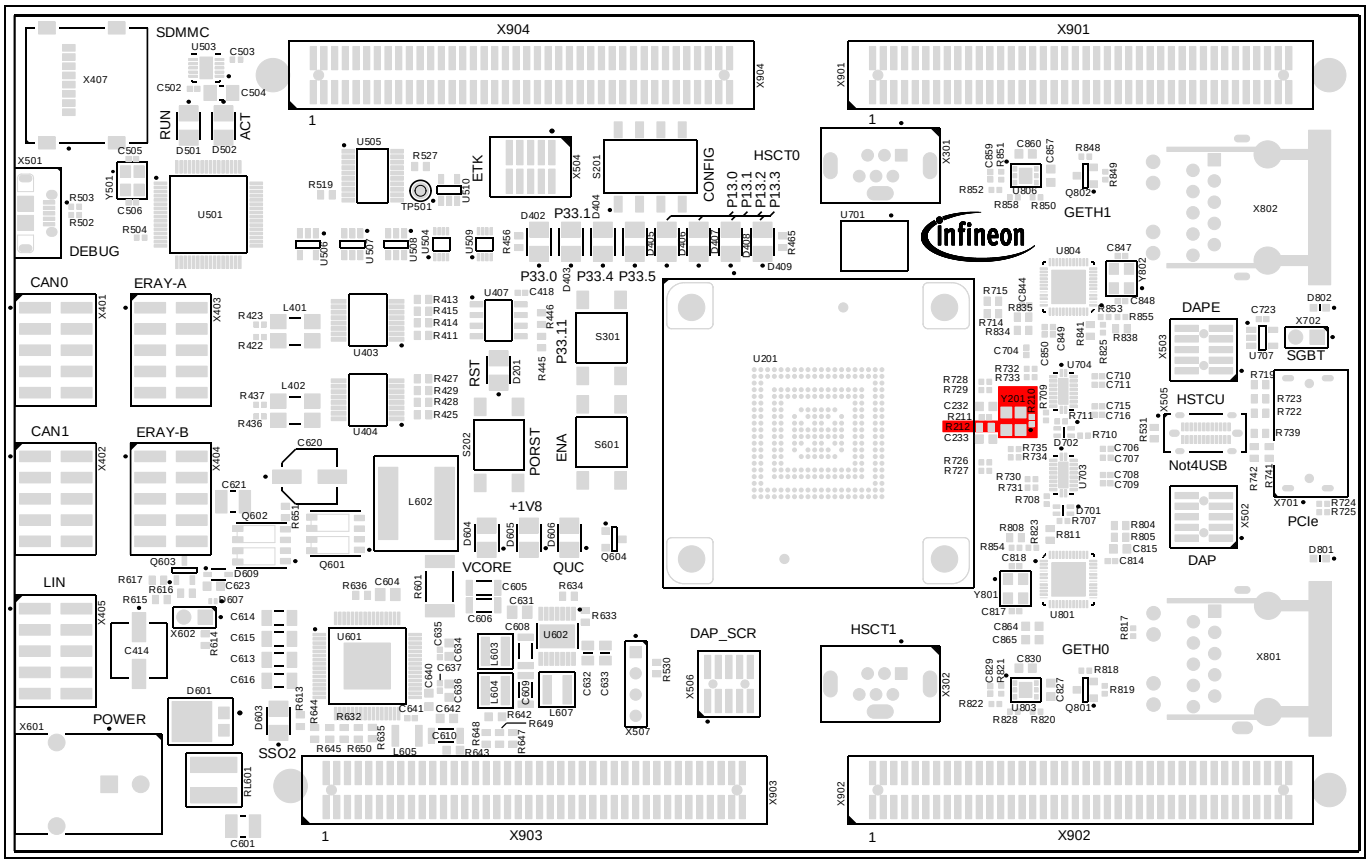


Figure 4 Main crystal location

2.4.2 RTC crystal

For RTC there is a 32,768kHz (DAISHINKU DST310S) crystal (Y301) assembled.

Per default XTAL3 (P33.9) and XTAL4 (P33.10) are not connected to X904/X1004. If the signals are needed on the 80 pin Samtec connectors (e.g., for measurement) then 0R resistors (size 0402) at R302 and R303 must be assembled. All mentioned parts are marked in the following **Figure 5**:

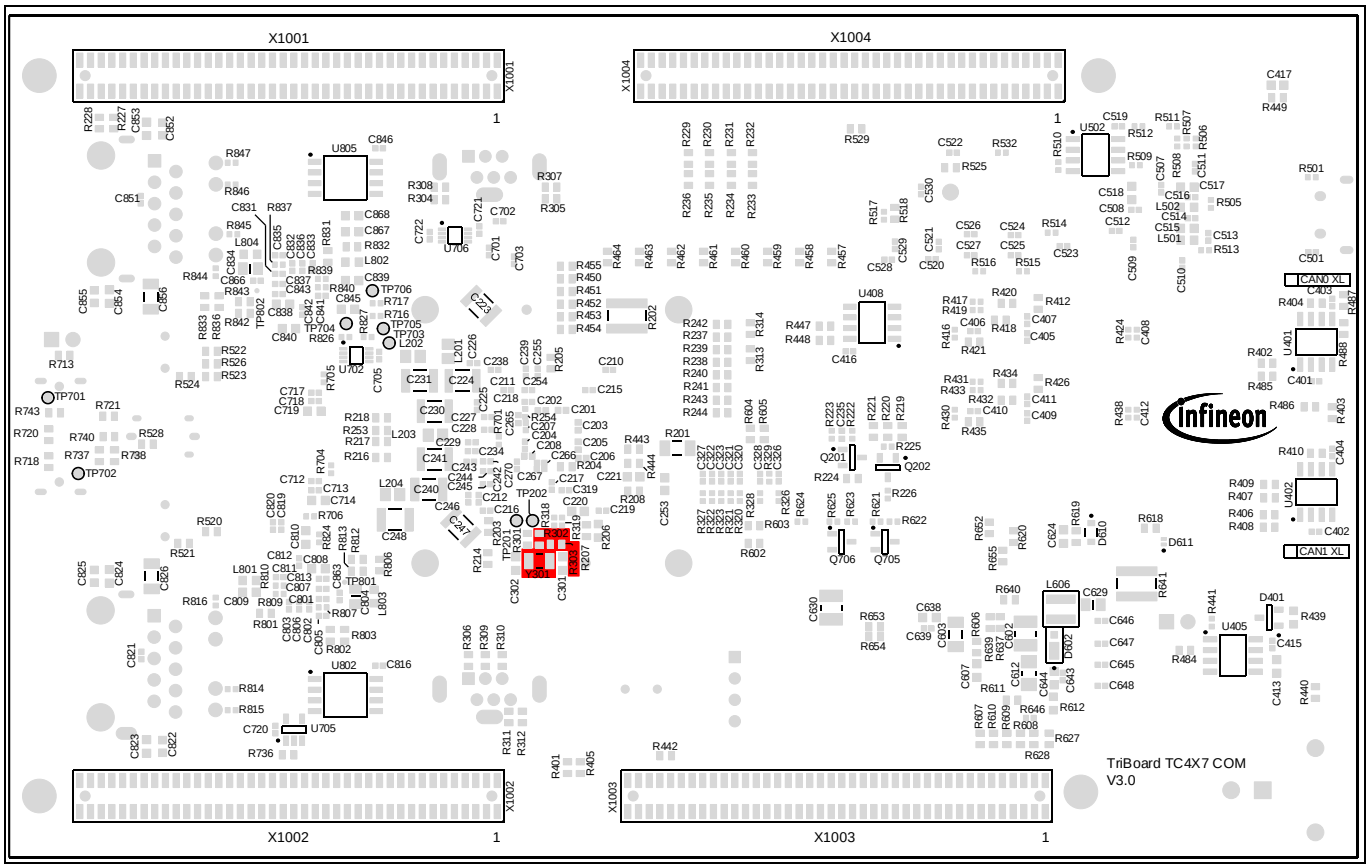


Figure 5 RTC crystal location

2.5 Reset

The power on reset input pin (/PORST) of the AURIX™ family is a bi-directional input/output intended for external triggering of power-related resets. If the /PORST pin remains asserted after a power event then the reset will be extended until it is deasserted. This does not replace the ESR pins functional reset. An external pull-up resistor (2.2 kΩ) keeps the /PORST pin high during normal operation. A low level at this pin will force a hardware reset. In case of an MCU internal reset the /PORST pin will drive a low signal.

A reset signal can be issued by

- the AURIX™ itself (U201.K20 - /PORST)
- the TLF4D985 (U601.26 – RESOUT)
- the on-board Reset Button (“PORST”)
- the on-board miniWiggler via FT2232HL (U501.27 – ACBUS1)
- the on-board DAP connector (X502.10 – /PORST)
- the on-board DAPE connector (X503.10 – /PORST)
- the optional ETK connector (X504.10 – /PORST)
- the on-board HSTCU connector (X505.A5 – /PORST)
- the Samtec connectors (X702.22/X802.22– /PORST)

An AURIX™ internal circuit always ensures a save Power-on-Reset. **TriBoard TC4X7 COM** does not require any additional external components to generate a reset signal during power-up. For more information’s, please refer to the datasheet or user manual of the assembled AURIX™ device.

2.6 Debugging and on board miniWiggler

The **TriBoard TC4X7 COM** supports debugging via different channels:

- On-board miniWiggler via the micro-USB connector X501
- 10-pin DAP connector X502
- 10-pin DAPE connector X503
- 10-pin DAP_SCR Connector X504
- 26-pin HSTCU connector X505
- Optional 10-pin ETK connector X506

2.6.1 Micro USB Connector

The Micro USB connector is used for connection to a PC. Via the USB it is possible to using the ASCLIN0 as serial connection via USB and Debugging via DAS. For the pinout of USB socket see Figure 22.

NOTE: Before connecting the board to the PC, make sure that the actual DAS software is installed on the PC.

For actual DAS software please contact your local FAE.
The software can also be found on:

DAS website

2.6.2 Serial Connection to PC

After the first connection of USB to a PC the needed driver will be installed automatically. During this there will be created a new COM port on PC. This COM port can be used to communicate with the board via ASCLIN0 of the device. Per default the ASCLIN0 is used on P14.0 and P14.1 (e.g., Generic Bootstrap Loader) .
In case you will use P14.0 and P14.1 as CAN or outside of the board then you must disable the voltage-level shifter U509. This can be done by assemble resistor R518 (size 0603) with a 0R resistor.

Table 5 FTDI Channel B Signals and AURIX™ Pin Mapping

FTDI Signal Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
BDBUS0	P14.1, Receive input	ASCLIN0_ARXA
BDBUS1	P14.0, Transmit output	ASCLIN0_ATX

The mentioned resistor R518 is red marked in following **Figure 6**:

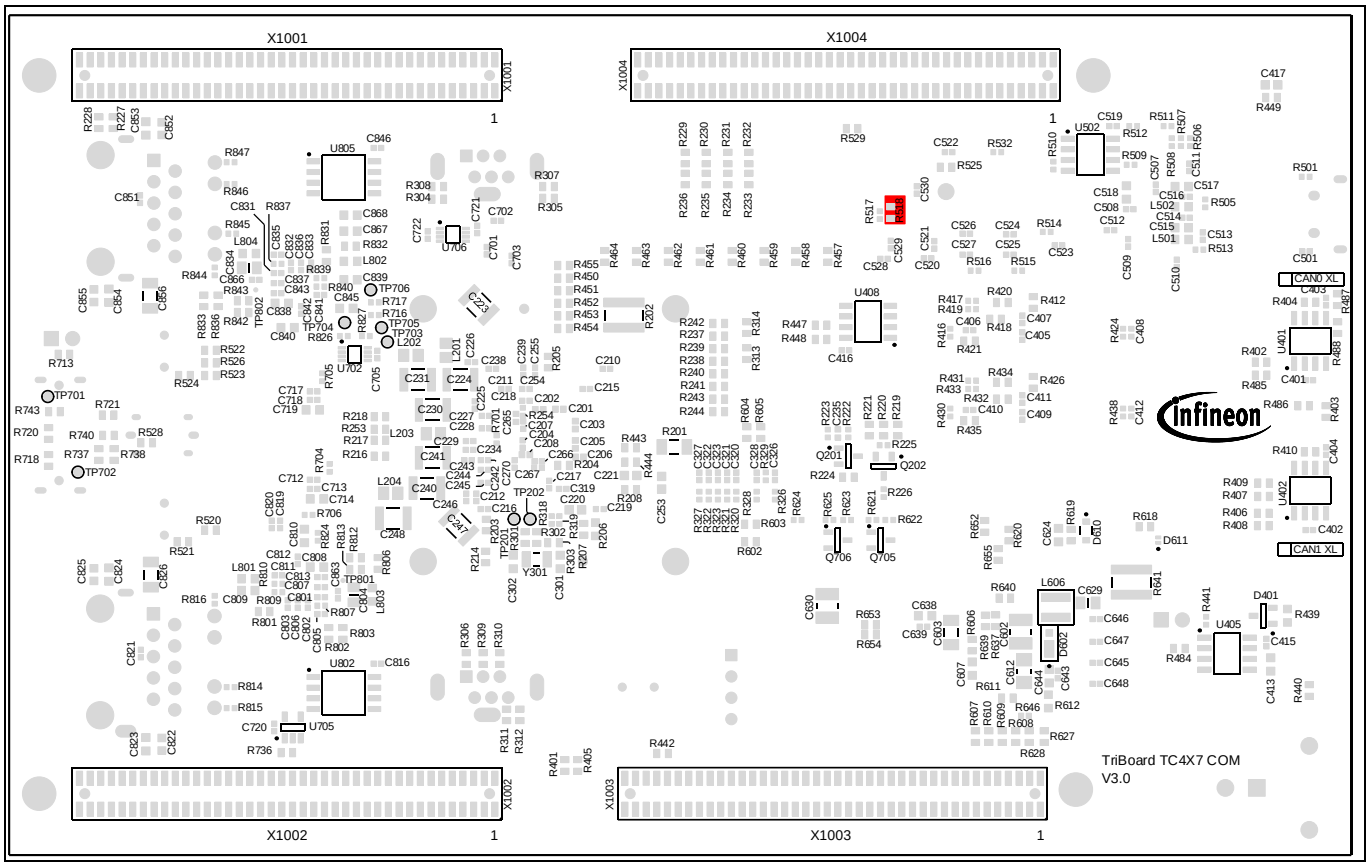


Figure 6 Resistor for disable level-shifter on ASC

2.6.3 miniWiggler JDS

The miniWiggler JDS is a low-cost debug interface which allows you access to the device via DAP. Make sure that you have the latest DAS release. Debugging is possible via the DAS Server ‘UDAS‘. Please contact your preferred debug vendor for support of DAS.

If you have connected the board to the PC and there runs the DAS server, then a working connection is visible via the green LED D502 (ACTIV). The blue status LED D501 (RUN) is switched on/off through the DAS Server, depending on the used debugger (client).

IMPORTANT: Make sure that there is no or a tristated connection on the DAP or HSTCU connector if the LED5 (miniWiggler in use) is on.

The miniWiggler is connected always via DAP to the **AURIX ™**. JTAG is not possible.

Table 6 FTDI Channel A Signals and AURIX™ Pin Mapping

FTDI Signal Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
ADBUS0	DAP0, DAP0 Clock Input	-
ADBUS2	DAP1, DAP1 Data I/O	-
ACBUS3	DAP2, DAP2 Data I/O	-
ACBUS1	/PORST, Power on Reset Input	-
ACBUS2	USR1, TESTMODE or /TRST	-

2.7 FlexRay™ (ERAY)

The board has 2 IDC10 plugs for FlexRay™ Communication (channel A and B) with up to 10 Mbit/s. For the pinout of the plugs see **Figure 23**. You can use an IDC female connector with crimp connector, flat cable and SUB-D 9 plug with crimp connector to have a 1:1 adapter to SUB-D 9.

The transceivers are connected to the **AURIX™** via zero-ohm resistors (R411 up to R415 and R425 up to R429) which must be removed to use the ports outside of the board.

Table 7 FlexRay™ (ERAY-A) Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
TXD	P02.0, Transmit Channel A	ERAY0_TXDA
RXD	P02.1, Receive Channel A2	ERAY0_RXDA2
TXEN	P02.4, Transmit Enable Channel A	ERAY0_TXENA
EN	P00.5, General-purpose output	P00.5 OUT
ERRN	P02.7, ERU channel 0 input F	SCU_E_REQ0F

Table 8 FlexRay™ (ERAY-B) Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
TXD	P02.2, Transmit Channel B	ERAY0_TXDB
RXD	P02.3, Receive Channel B2	ERAY0_RXDB2
TXEN	P02.5, Transmit Enable Channel B	ERAY0_TXENB
EN	P00.6, General-purpose output	P00.6 OUT
ERRN	P02.8, ERU channel 5 input G	SCU_E_REQ5G

For more information look in the user manual of **AURIX™**.

2.8 CAN/CANXL

The **TriBoard TC4X7 COM** provides two CAN connector connected to two CAN transceiver and to the CAN0 and CAN1 of **AURIX™**. The transceivers are connected to two IDC10 plug. For the pinout of IDC10 plug see **Figure 24**. You can use an IDC female connector with crimp connector, flat cable and SUB-D 9 plug with crimp connector to have a 1:1 adapter to SUB-D 9.

The used transceiver TLE9371VSJ is the latest Infineon high-speed CAN transceiver generation, used inside HS CAN networks for automotive and also for industrial applications. It is designed to fulfill the requirements of ISO 11898-2 (2016) physical layer specification and respectively also the SAE standards J1939 and J2284. The CAN buses (signals CANH, CANL) are terminated with by a 120 Ohm resistor.

The board also can be assembled with CAN XL transceiver **(not with TC497A)** instead of TLE9371VSJ. In this case the corresponding marker (CAN0 XL and CAN1 XL) on bottom silkscreen is marked and the marked CANx can be used in CAN XL mode. The corresponding resistors are set also in this case. See **Table 9** and **Table 10**Error! Reference source not found. the usable AURIX ™ Pins for CAN XL.

The transceiver is in stand-by mode per default. To switch the transceiver to normal operating mode the pin CAN_STB must be driven low from the CPU.

The transceivers are connected to the **AURIX™** via zero-ohm resistors (R401 up to R403 and R405 up to R409) which must be removed to use the ports outside of the board.

The transceiver of CAN0 is connected to the **AURIX™** CAN0 node 0 per default and can be changed to CAN0 node 2 by removing R402, R403 and assembling R485, R486. The transceiver is powered by the standby voltage provided from PMIC which is used on the selected **AURIX™** port. With this connection it is possible that the WCAN feature (Wake-up CAN filter) of the SCR can also be used and tested (when default CAN0 node 0 is selected).

The transceiver of CAN1 is connected to the **AURIX™** CAN0 node 2 per default and can be changed to CAN0 node 1 by removing R406, R407 and assembling R408, R409. In this case, please disable also the level-shifter on ASC, see chapter **Serial Connection to PC**.

Table 9 CAN0 Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
TXD	P33.8, CAN transmit output node 0 or P02.2, CAN transmit output node 2 or P02.2, CANXL transmit output node 1	CAN00_TXD CAN02_TXD CANXL01_TXD
RXD	P33.7, CAN receive input node 0 or P02.3, CAN receive input node 2 or P02.3, CANXL receive input node 1	CAN00_RXDE CAN02_RXDB CANXL01_RXDC
STB	P00.3, General-purpose output	P00.3 OUT

Table 10 CAN1 Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
TXD	P14.10, CAN transmit output node 2 or P14.0, CAN transmit output node 1 or P14.10, CANXL transmit output node 0	CAN02_TXD CAN01_TXD CANXL00_TXD
RXD	P14.8, CAN receive input node 2 or P14.1, CAN receive input node 1 or P14.8, CANXL receive input node 0	CAN02_RXDD CAN01_RXDB CANXL00_RXDA
STB	P00.2, General-purpose output	P00.2 OUT

2.9 LIN

On the board is one LIN transceiver connected to the ASCLIN4 on **AURIX™**. The transceiver is connected to one IDC10 plug. For the pinout of IDC10 plug see **Figure 25**. You can use an IDC female connector with crimp connector, flat cable and SUB-D 9 plug with crimp connector to have a 1:1 adapter to SUB-D 9.

The transceiver is in sleep mode per default (EN is low via pull-down R484). To switch the transceiver to normal operation mode the pin EN must be driven high from the CPU.

The transceiver is connected to the **AURIX™** via zero-ohm resistors (R442 up to R444) which must be removed to use the ports outside of the board.

Table 11 LIN Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
TXD	P00.9, Transmit output	ASCLIN4_ATX
RXD	P00.12, CAN receive input node 0	ASCLIN4_ARXA
EN	P00.7, General-purpose output	P00.7 OUT

The LIN can be used in master and in slave mode. For the master mode there is per default a pull-up of 1K (R439) and a capacitor of 1nF (C413) on the BUS assembled. For using the LIN in slave mode, the pull-up resistor R439 must be removed and maybe the capacitor changed to a smaller value (e.g., 220pF).

The mentioned resistor and capacitor are red marked in following **Figure 7**:

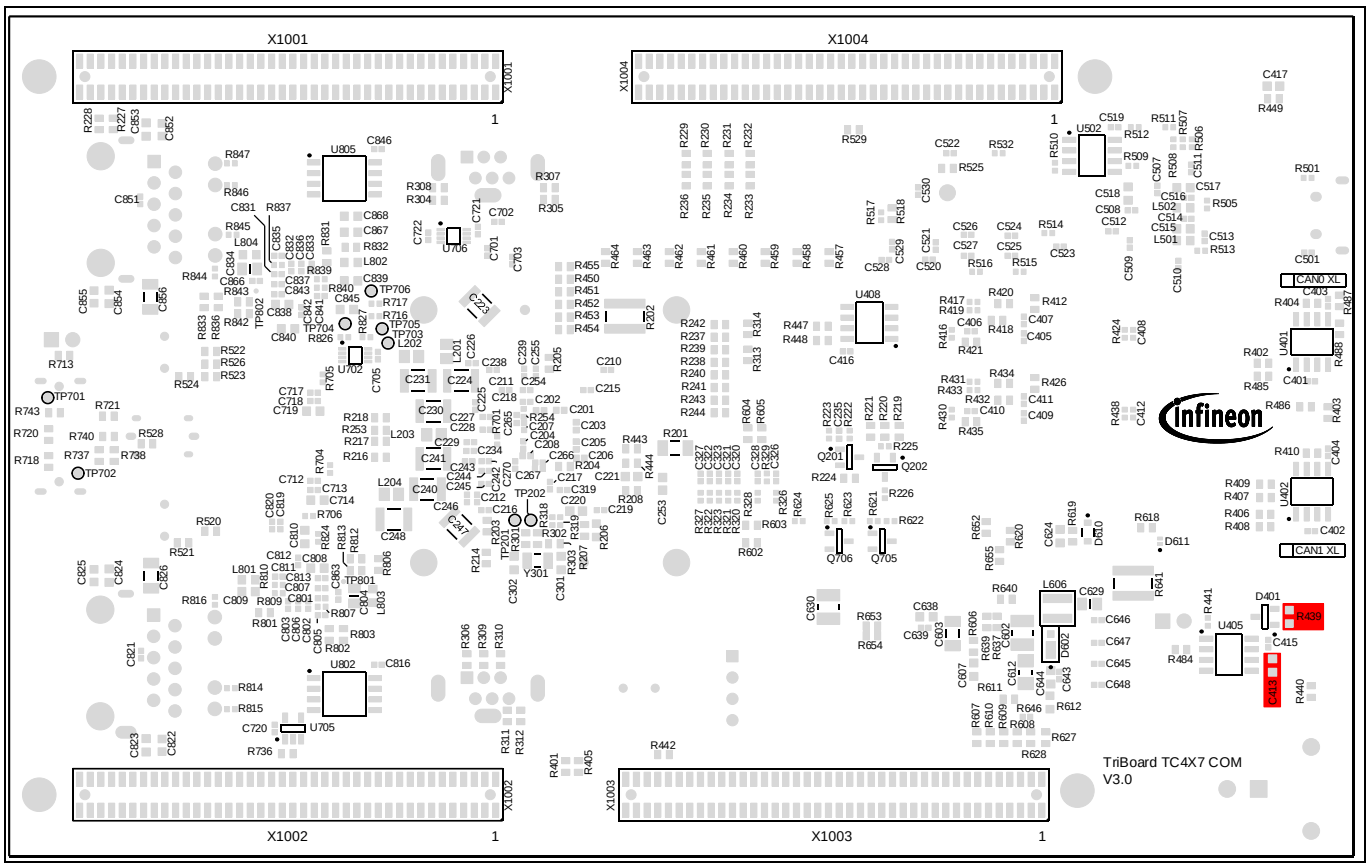


Figure 7 Components for LIN Master Mode

2.10 Serial Eeprom

The I2C via P15.4 and P15.5 of the **AURIX™** is connected to two serial EEPROMs with a size of 2KBit (2 x 128 x 8). The slave addresses of the EEPROMs are 0x50 and 0x51. The upper half of the array (80h-FFh) is permanently write-protected. Write operations to this address range are inhibited. Read operations are not affected. This upper half contains a preprogrammed EUI-64™ node address which can be used as MAC ID for Ethernet. The other 128 bytes are writable by customer.

To disconnect (disable) the EEPROMs remove resistor R445 and R446 (see **Figure 17**).

Table 12 Serial Eeprom Signals and AURIX™ Pin Mapping

Transceiver Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
SCL	P15.4, Serial Clock Output	I2C0_SCL
SDA	P15.5, Serial Data Input 2/Output	I2C0_SDAC/I2C0_SDA

2.11 High Speed Physical Layer (HSPHY)

The TC4X7 contains a functional block which provides communication capability according to the Ethernet IEEE 802.1 standard, the PCIe Gen 3 standard and the 8b/10b Aurora standard through MP8G PHY. HSPHY also provides controls for communication capability according to the JESD251 compliant xSPI interface and the Ethernet Interface RGMII.

The module consists of the following blocks:

- MP8G PHY (Multi-Protocol 8 Gigabit PHY)
- XPCS block (connects Ethernet MAC with the MP8G PHY with encoding)
- TPCS block (connects TRACE with the MP8G PHY)
- DLL and skew control block for xSPI, RGMII and GPIOs (connects xSPI)

Up to wwo MP8G PHYs (Multi-Protocol 8 Gigabit PHY, MP8G0 and MP8G1) are available in the HSPHY and they can be shared among the GETH MAC, TRACE and PCIe (TC4D7 only).

MP8G PHY0 and MP8G PHY1 connect to the two Ethernet MACs (MAC0 and MAC1) of GETH.

In addition, MP8GPHY0 can connect to PCIe (TC4D7 only) and MP8G PHY1 can connect to SGBT.

MP8G0 is not available with TC487 COM and TC447 COM therefore GETH0 can’t be used with th devices.

The board has the possibility to use all these interfaces but not at the same time. Therefore, the TriBoard contains demultiplexer connected to MP8G PHY0 and PHY1. PHY0 (if available) can be used as GETH0 or PCIe (only with TC4D7), PHY1 can be used as GETH1 or TRACE.

Selection between GETH0 and PCIe will be done via **AURIX™** port pin P00.4. After each reset P00.4 is at high level which connect PHY0 and GETH0, indicated by green light of LED 701. To switch to PCIe (OcuLink connector) P00.4 must be configured as output and driven low, indicated by red light of LED 701.

The second demultiplexer for PHY1 is per default assembling fixed configured to GETH1, indicated by green light of LED D702. If MP8G PHY1 should be used as TRACE then you must put a jumper on X702 (SGBT) to close the jumper. Then PHY1 is used as SGBT via USB-C, indicated by red light of LED D702.

Jumper X702 is red marked in the following **Figure 8**:

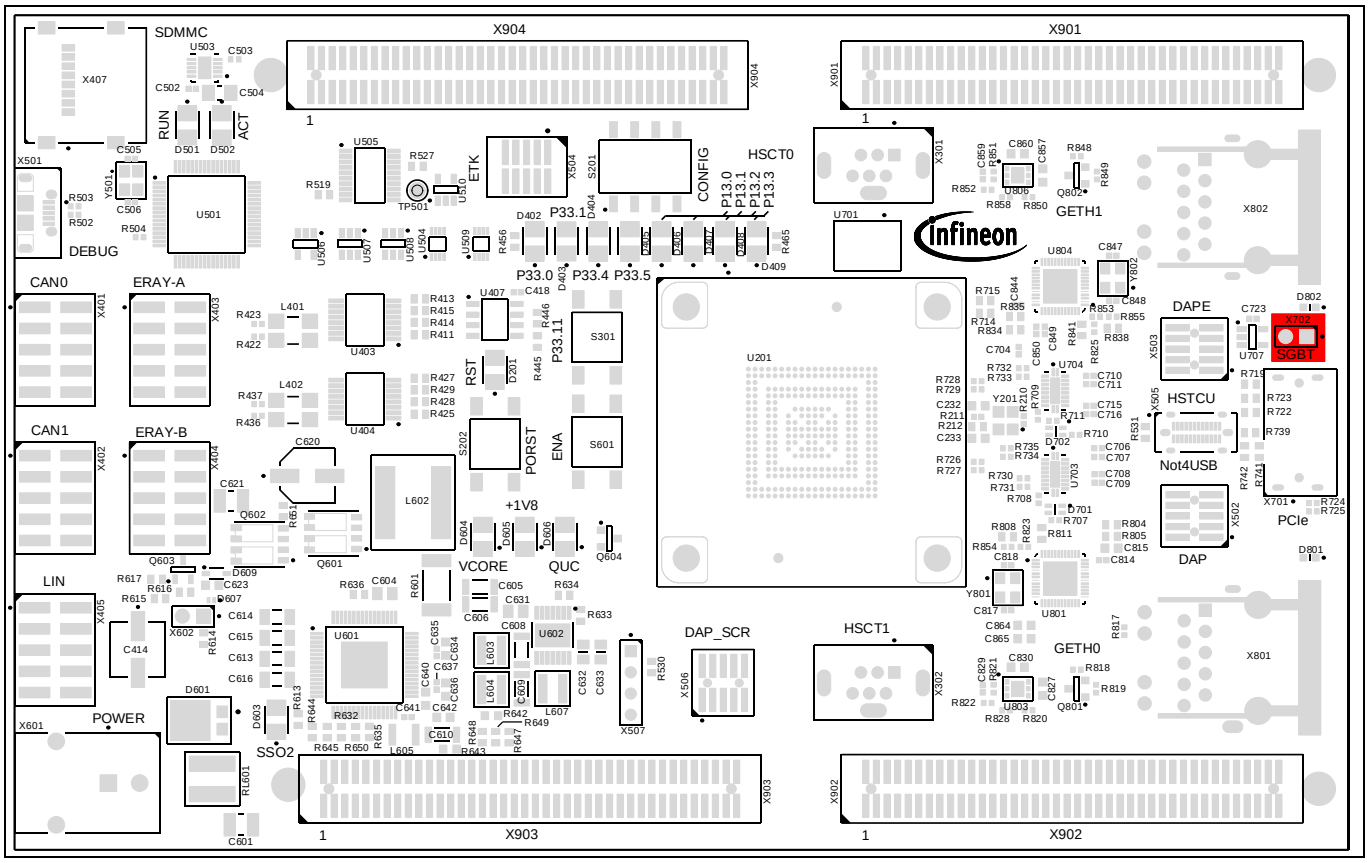


Figure 8 Jumper for SGBT selection

2.11.1 High-speed coupling

Using capacitors to AC-couple an LVDS data link provides many benefits, such as level shifting, removing common-mode errors, and protecting against input-voltage fault conditions.

The serial resistors in high-speed traces of the MP8G PHY0/MP8G PHY1 and the demultiplexer are placeholders for AC caps. These are subject to be adapted if needed.

Table 13 Coupling components

Component	Signal Name	Size	Comment
R724	PCIE_RX_S_P	0402	0R resistor, OcuLink connector to demultiplexer
R725	PCIE_RX_S_N	0402	0R resistor, OcuLink connector to demultiplexer
R734	PCIE_REFCLK_S_P	0402	0R resistor, TC4X7 to OcuLink connector
R735	PCIE_REFCLK_S_N	0402	0R resistor, TC4X7 to OcuLink connector
R726	PHY0TX_S_P	0402	0R resistor, TC4X7 to demultiplexer
R727	PHY0TX_S_N	0402	0R resistor, TC4X7 to demultiplexer
R728	PHY1TX_S_P	0402	0R resistor, TC4X7 to demultiplexer
R729	PHY1TX_S_N	0402	0R resistor, TC4X7 to demultiplexer
R730	PHY0RX_S_P	0402	0R resistor, demultiplexer to TC4X7
R731	PHY0RX_S_N	0402	0R resistor, demultiplexer to TC4X7
R732	PHY1RX_S_P	0402	0R resistor, demultiplexer to TC4X7

(table continues...)

Component	Signal Name	Size	Comment
R733	PHY1RX_S_N	0402	0R resistor, demultiplexer to TC4X7
C706	PCIE_TX_S_P	0402	220nF capacitor, demultiplexer to OcuLink connector
C707	PCIE_TX_S_N	0402	220nF capacitor, demultiplexer to OcuLink connector
C708	SGMII0TX_S_P	0402	100nF capacitor, demultiplexer to Ethernet PHY0
C709	SGMII0TX_S_N	0402	100nF capacitor, demultiplexer to Ethernet PHY0
C710	SGMII1TX_S_P	0402	100nF capacitor, demultiplexer to Ethernet PHY1
C711	SGMII1TX_S_N	0402	100nF capacitor, demultiplexer to Ethernet PHY1
C715	SGBT1TX_S_P	0402	100nF capacitor, demultiplexer to HSTCU connector
C716	SGBT1TX_S_N	0402	100nF capacitor, demultiplexer to HSTCU connector
C819	SGMII0RX_S_P	0402	100nF capacitor, Ethernet PHY0 to demultiplexer
C820	SGMII0RX_S_N	0402	100nF capacitor, Ethernet PHY0 to demultiplexer
C849	SGMII1RX_S_P	0402	100nF capacitor, Ethernet PHY1 to demultiplexer
C850	SGMII1RX_S_N	0402	100nF capacitor, Ethernet PHY1 to demultiplexer

The mentioned resistors and capacitors are red marked in following **Figure 9** and **Figure 10**:

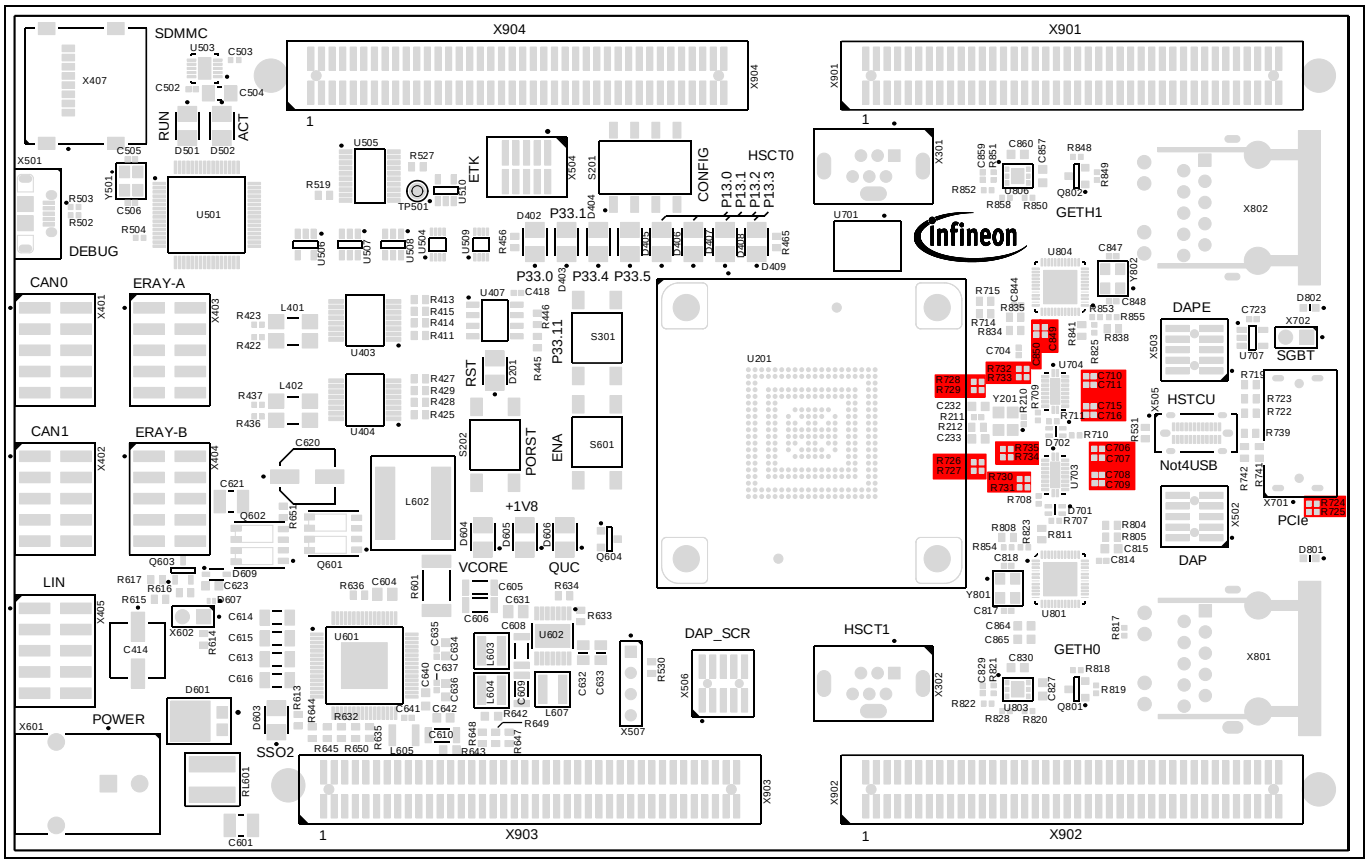


Figure 9 High-speed coupling capacitors and resistors Top side

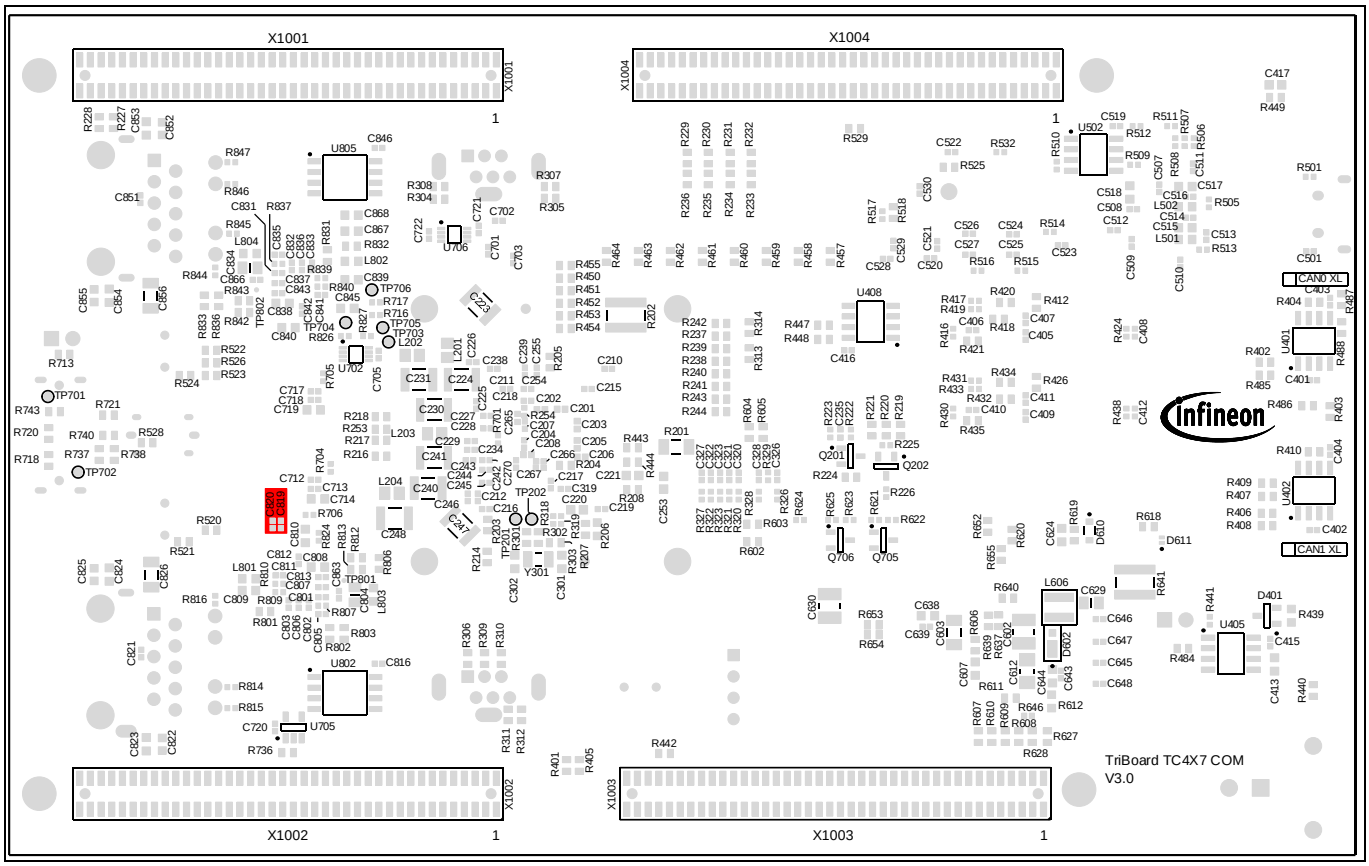


Figure 10 High-speed coupling capacitors and resistors Bottom side

2.11.2 Ethernet

The TriBoard provide two RJ45 connector (X801 and X802) for twisted pair ethernet connections. The TriBoard use a Realtek Integrated 10/100/1000M/2.5G ETHERNET Transceiver RTL8221B-CG as physical interface device. For more information about the ethernet module see TC4X7 User's Manual, about the PHY see the RTL8221B datasheet. Each PHY control the generation of the own needed 0,95V (+0V95_HS0 and +0V95_HS1) supply.

The PHYs are always in reset via pull-down resistor on PHYRSTB_N. To release the reset of the PHY the corresponding **AURIX™** pin must be configured as output and driven high.

For the connection between **AURIX™** and PHY is used SGMII. For the pinout of RJ45 see **Figure 27**.

Table 14 Ethernet Control Signals and AURIX™ Pin Mapping

PHY Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
PHYRSTB_N (GETH0)	P00.10, P00.10 General-purpose output	P00.10 OUT
INTB (GETH0)	P10.2, ERU channel 2 input A	SCU_E_REQ2A
PHYRSTB_N (GETH1)	P00.11, P00.11 General-purpose output	P00.11 OUT
INTB (GETH1)	P10.3, ERU channel 3 input A	SCU_E_REQ3A
MDC	P16.11, MDIO Clock	GETH0_MDC0 / MDC1
MDIO	P16.14, MDIO input / output	GETH0_MDIOB / MDIO1

2.11.3 PCIe (only with TC4D7)

For using the PHY0 with PCIe the **TriBoard TC4X7 COM** has a PCIe OcuLink connector. For pinout of this connector see **Figure 28**. For using PCIe please make sure that **AURIX™** pin P00.4 is configured as output and driven low. Two different pin mappings on Oculink usable:

Table 15 PCIe configurable Oculink Pin Mapping

PCIe Name	Signal name	Oculink pin number	Resistor	Assembly
PCIE_REFCLK_P	PCIE_REFCLKB_P PCIE_REFCLKA_P	B12 A12	R741 R737	yes no
PCIE_REFCLK_N	PCIE_REFCLKB_N PCIE_REFCLKA_N	B13 A13	R742 R738	yes no
PCIE_WAKE	PCIE_WAKEB PCIE_WAKEA	B10 A10	R743 R720	yes no
PCIE_PERST	PCIE_PERSTA PCIE_PERSTB	A12 B12	R740 R739	yes no

The sideband signals of PCIe are connected to **AURIX™** pins. Configure these two pins as input or output dependent of the use case of the pins.

Table 16 PCIe Control Signals and AURIX™ Pin Mapping

PCIe Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
PCIE_WAKE	P23.4, P23.4 General-purpose input/output	P23.4 IN/OUT
PCIE_PERST	P23.1, P23.1 General-purpose input/output	P23.1 IN/OUT

2.11.4 xSPI Flash

The Cypress Semper® Flash with HyperBus™ Interface (U701, S26HS512TGABHM000) is connected to port P16 of the **AURIX™** TC4X7 device and can be used as data flash memory with a size of 64 Mbyte. Please note that all port pins of P16 only be connected to the xSPI flash and the level shifter for MDC/MDIO used by GETH0 and GETH1. This port pins are not connected to any connector also not via a resistor.

Table 17 xSPI Flash Signals and AURIX™ Pin Mapping

Semper® Flash Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
CK	P16.1, Clock out	XSPI_CLK
CK#	P16.0, Clock out inverted	XSPI_CLK_INV
DS	P16.2, Data mask	XSPI_DM
DQ0	P16.7, Receive data/Transmit data	XSPI_RXD0/XSPI_TXD0
DQ1	P16.3, Receive data/Transmit data	XSPI_RXD1/XSPI_TXD1
DQ2	P16.5, Receive data/Transmit data	XSPI_RXD2/XSPI_TXD2
DQ3	P16.6, Receive data/Transmit data	XSPI_RXD3/XSPI_TXD3
DQ4	P16.8, Receive data/Transmit data	XSPI_RXD4/XSPI_TXD4

(table continues...)

Semper® Flash Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
DQ5	P16.9, Receive data/Transmit data	XSPI_RXD5/XSPI_TXD5
DQ6	P16.10, Receive data/Transmit data	XSPI_RXD6/XSPI_TXD6
DQ7	P16.12, Receive data/Transmit data	XSPI_RXD7/XSPI_TXD7
CS_N	P16.13, Chip Select 0	XSPI_CS0_N
RESET_N	P16.4, P16.4 General-purpose output	P16.4 OUT
INT_N	P14.8, P14.8 General-purpose input	P14.8 IN
RSTO_N	P14.7, P14.7 General-purpose input	P14.7 IN

2.12 Micro SD card slot

The board has a slot for a micro-SD card. To insert any SD card, push the lid of the slot to inside of the board and open the lid. After installing the SD card, close the lid and push to outside of the board to lock the SD card. Please see also the pictograms on the lid.

Table 18 SDMMC Signals and AURIX™ Pin Mapping

SD slot Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
CLK	P15.1, card clock output	SDMMC0_CLK
CMD	P15.3, command out	SDMMC0_CMD
DAT0	P20.7, read data in/ write data out	SDMMC0_DAT0_IN/ SDMMC0_DAT0
DAT1	P20.8, read data in/ write data out	SDMMC0_DAT1_IN/ SDMMC0_DAT1
DAT2	P20.10, read data in/ write data out	SDMMC0_DAT2_IN/ SDMMC0_DAT2
DAT3	P20.11, read data in/ write data out	SDMMC0_DAT3_IN/ SDMMC0_DAT3

The micro-SD card is connected to module SDMMC0 of the **AURIX™** device. If needed the connection to the SD card slot can be interrupted by removing resistor R450 up to R455.

2.13 HSCT (optional)

The TriBoard provide a footprint of IEEE 1394 socket (X301 and X302) for connection to other **AURIX™** via HSCT.

Note: *Don’t use X301 and X302 for connection to any IEEE 1394 device, this can destroy the board and/or the connected device.*

X301 is connected to HSCT0 and X302 to HSCT1 of the **AURIX™** device. Please note that HSCT1 is not available with TC447 COM and can’t be used.

For connect two TriBoards you need to assemble this socket (Lumberg 2415 01) on each board and connect the boards with a standard 6 pin IEEE 1394 cable. For the pinout of socket see **Figure 26**.

Table 19 HSCT Signals and AURIX™ Pin Mapping

Signal Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
SYSCLK	P20.0, Sys clock output P20.0, System clock input	HSCT0_SYSCLK_OUT CLOCK_CLKA_SYSCLK
RXD0_N	P21.2, RX data (LVDS N Line)	HSCT0_RXDN
RXD0_P	P21.3, RX data (LVDS P Line)	HSCT0_RXDP
TXD0_N	P21.4, TX data (LVDS N Line)	HSCT0_TXDN
TXD0_P	P21.5, TX data (LVDS P Line)	HSCT0_TXDP
RXD1_N	P21.0, RX data (LVDS N Line)	HSCT1_RXDN
RXD1_P	P21.1, RX data (LVDS P Line)	HSCT1_RXDP
TXD1_N	P22.2, TX data (LVDS N Line)	HSCT1_TXDN
TXD1_P	P22.3, TX data (LVDS P Line)	HSCT1_TXDP

2.13.1 High speed with HSCT

For use the HSCT connection between two boards you need to remove 9 resistors to have a very short connection between device and connector. On the TC4X7 TriBoard these 9 resistors are R304, R305, R306, R307, R308, R309, R310, R311 and R312 (red marked in **Figure 11**). These resistors need to be removed.

Important: When the resistors are removed then the port signals P20.0, P21.2, P21.3, P21.4, P21.5, P21.0, P21.1, P22.2 and P22.3 are no longer available on the 80 pin Samtec connectors.

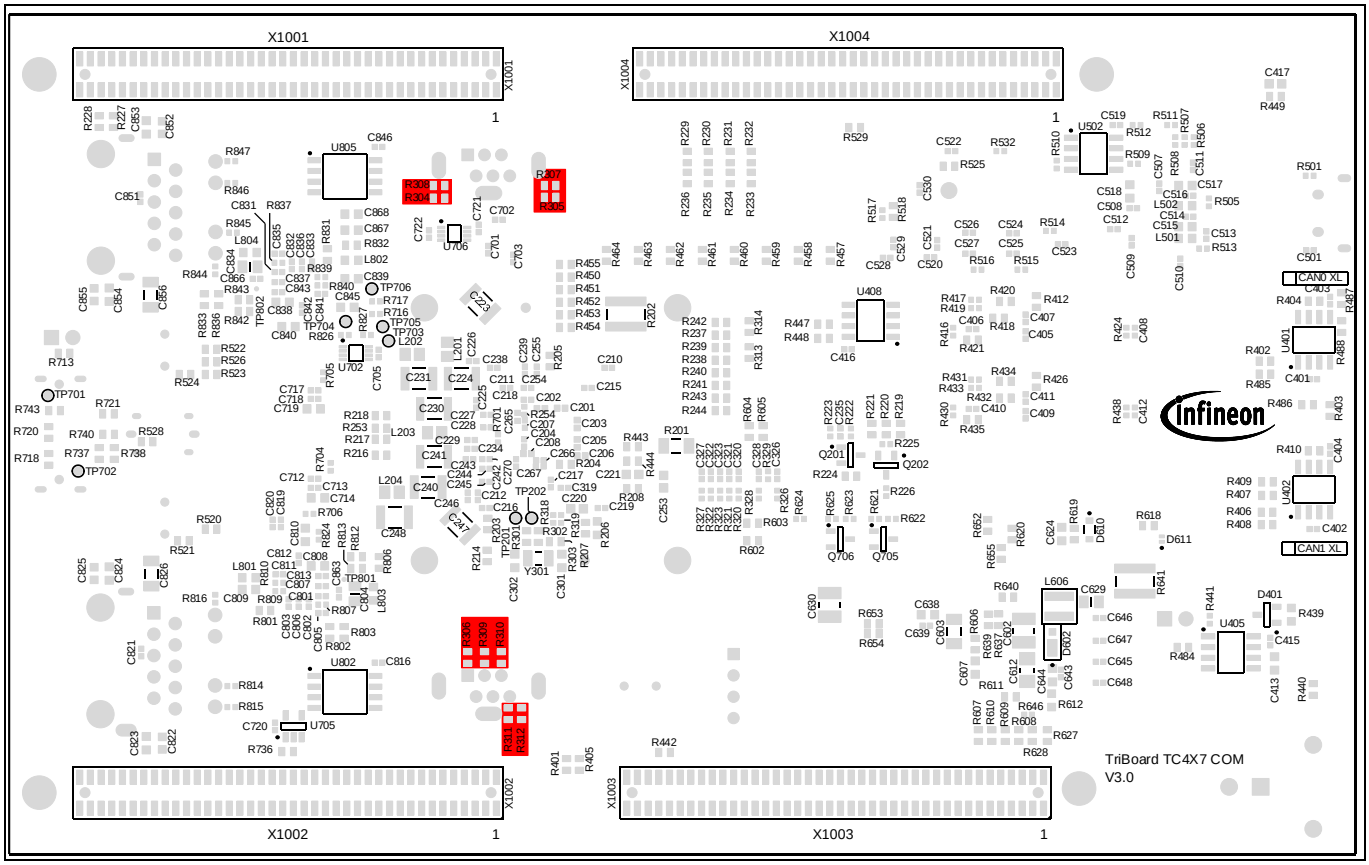


Figure 11 Resistors for high speed HSCT

2.14 ADC

On this boards are 4 ADC channels prepared with a low pass filter. On pin AN0, AN8, AN16 and AN24 is assembled a capacitor of 47nF and a serial resistor of 4,7K. The pins AN2 and AN3 are coupled together via a 6,8pF and connected to the Samtec connector via a serial resistor of 4,7K. This can be useful for using DSADC channel 0 input A.

Table 20 ADC Filter

Signal Name	AURIX ™Pin, AURIX™ Function	Default values and component name
AN0	AN0, Analog Input 0	4K7 (R320) and 47nF (C320)
AN8	AN8, Analog Input 8	4K7 (R321) and 47nF (C321)
AN16	AN16, Analog Input 16	4K7 (R322) and 47nF (C322)
AN24	AN24, Analog Input 24	4K7 (R323) and 47nF (C323)
AN2	AN2, Analog Input for DSADC0 Positive Input A	4K7 (R318) and 6,8pF (C319)
AN3	AN2, Analog Input for DSADC0 Negative Input A	4K7 (R319) and 6,8pF (C319)

The filter components are red marked in the following **Figure 12**.

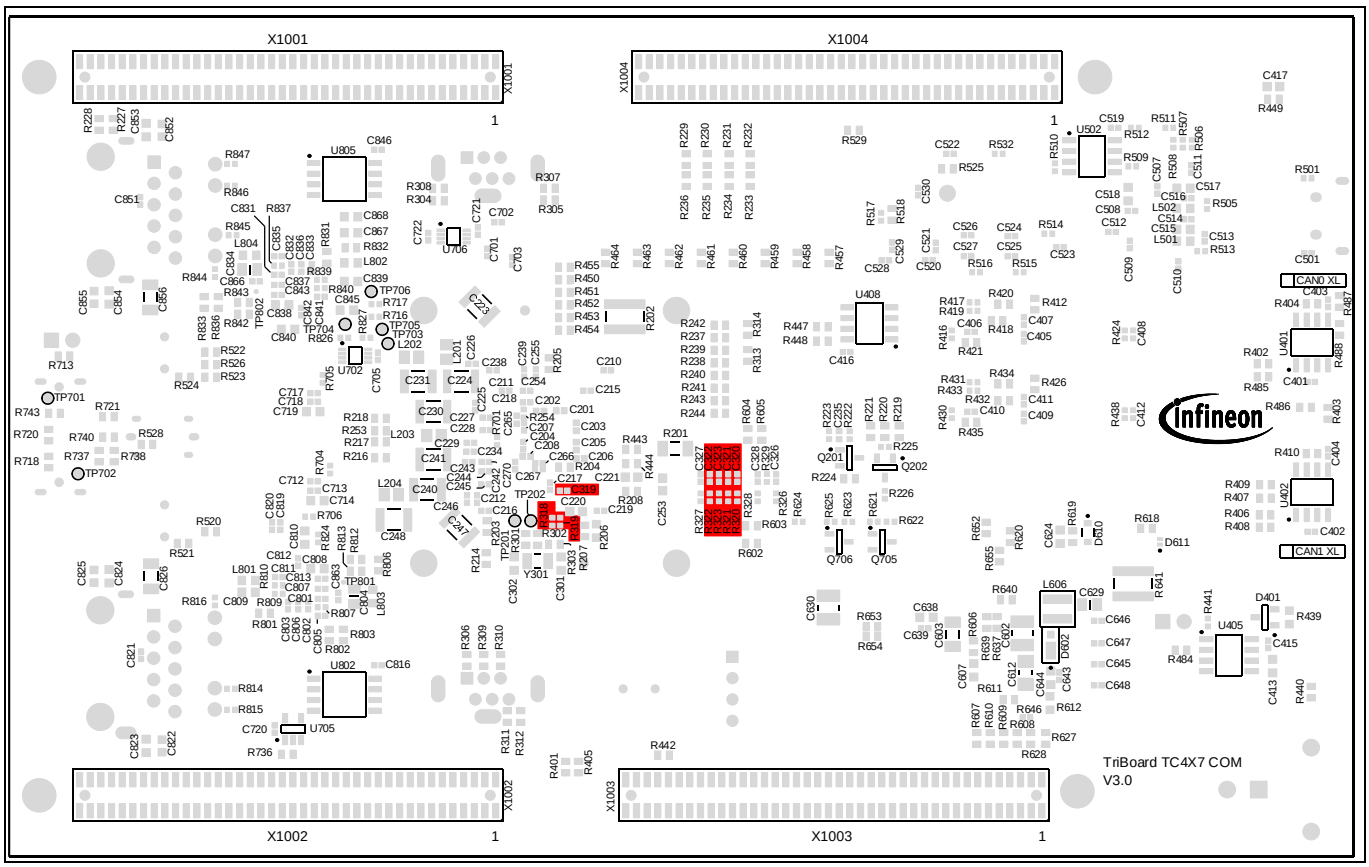


Figure 12 Filter components of ADC channels on Bottom Side

3 ADC channels are used on board directly for measurement, please see following **Table 21**:

Table 21 On board used ADC channels

Signal Name	AURIX ™Pin, AURIX™ Function	Measured voltage
AN29	AN29, Analog Input 29	+3V3 used for Ethernet Phys
AN30	AN30, Analog Input 30	+0,95V used/generated by Ethernet PHY 0 (U801)
AN31	AN31, Analog Input 31	+0,95V used/generated by Ethernet PHY 1 (U804)

2.15 Toggle LEDs

The status LEDs are low active and can be controlled by Software.

Port 13 pin 0 up to pin 3 are connected to single LED's (D406... D409) and powered by the normal microcontroller voltage.

Port 33 pin 0, 1, 4 and 5 are connected to single LED's (D402... D405) and powered by the standby voltage (QST). This means that this LED's can be used via SCR also when the board is in standby mode and only the standby voltage is available (port 33 is powered by VDDEVRSB pin which is connected to standby supply of TLF4D985). In this case the port pins are controlled by the standby controller.

Table 22 Toggle LEDs

LED Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line	Voltage
D402	P33.0 (SCR: P0.0), General-purpose output	P33.0 (SCR: P0.0) OUT	VDDEVRSB
D403	P33.1 (SCR: P0.1), General-purpose output	P33.1 (SCR: P0.1) OUT	VDDEVRSB
D404	P33.4 (SCR: P0.4), General-purpose output	P33.4 (SCR: P0.4) OUT	VDDEVRSB
D405	P33.5 (SCR: P0.5), General-purpose output	P33.5 (SCR: P0.5) OUT	VDDEVRSB
D406	P13.0, General-purpose output	P13.0 OUT	VDDEXT
D407	P13.1, General-purpose output	P13.1 OUT	VDDEXT
D408	P13.2, General-purpose output	P13.2 OUT	VDDEXT
D409	P13.3, General-purpose output	P13.3 OUT	VDDEXT

2.16 Buttons

On the board are three buttons.

The reset button (S202) will apply a warm power on reset to the device.

The ENA button (S601) will be used to enable/wakeup the TLF4D985.

The P33.11 button (S301) can be used by software as input. This button can be used also by the standby controller to react on an event when only standby supply is available (e.g., as wakeup the TLF4D985 via P33.10).

Table 23 Buttons and AURIX™ Pin Mapping

Button Name	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
ENA	-	-
RESET	PORST, Power on Reset Input	-
P33.11	P33.11, General-purpose input / ESR2 pin input	P33.11 IN / PMS_ESR2WKP

2.17 Other peripherals

For all other peripherals there are no special plugs on the board. The peripheral signals are available on the different connectors. See chapter **Connector Pin Assignment**.

2.18 Debug System

2.18.1 OCDS1

This TriBoard don't have any more the OCDS1 (IDC16 plug) connector. For use old debuggers with OCDS1 connector with this board ask your Infineon representative or debugger vendor for an adapter from OCDS1 to DAP or HSTCU.

2.18.2 DAP

The board comes with a DAP connector (X502). For pinout of this connector see **Figure 29**. You can connect a DAP hardware here.

If you use this connector, make sure that the miniWiggler JDS (see **miniWiggler JDS**) is not active (ACTIV LED is off) and a connected HSTCU hardware is disconnected or tristated.

If the ACTIV LED is on, then stop the active DAS Server 'UDAS' and/or remove the USB connection to the PC.

2.18.3 DAPE

The board comes also with another DAP connector (X503) which is connected to DAPE. For pinout of this connector see **Figure 29**. You can connect a DAP hardware here. If you use this connector, make sure that the miniWiggler JDS is not active (ACTIV LED is off) and a connected HSTCU hardware is disconnected or tristated.

Please note that in the case that DAPE will be use the standard DAP can't be used in 4-pin DAP mode. Also, in this case only DAP or DAPE can be used in 3-pin DAP mode, the other one can be used only in 2-pin DAP mode.

Note: *Due to multiplexing of signals DAPE1 and DAP3 on TC4x devices, the DAPE1 signal is connected also to pin 8 (USR1) of the DAP connector X502.*
With this connection any signal on pin 8 of the DAP connector can disturb the DAPE communication and DAPE will not work.
Solutions:
Make sure that a debugger connected to DAP (X502) does not drive pin 8 (USR1).
Otherwise zero ohm resistor R524 must be removed to use DAP and DAPE in parallel.
Please note that after this change unidirectional DAP wide mode does not work anymore.
The Infineon miniWiggler connected to DAP (X502) add a pull-up resistor to pin 8 (USR1) and will be disturb DAPE communication.
To avoid such conflict, the on-board wiggler may be used for DAP instead.

2.18.4 DAP_SCR

Additional DAP connector (X506) is connected to DAP_SCR. This DAP can be used only as private DAP connection to the standby controller. For pinout of this connector see **Figure 29**. You can connect a DAP hardware here. This DAP connector uses P33.2 (DAP0_1) and P33.3 (DAP1_1) of the SCR. SCRCFG must be set to 0x3 for OCDS Mode with SCR pins DAP0_1 or SCR DAP1_1 selected or to 0x5 for OCDS Mode with SCR pin SPD_1 selected (single pin dap via P33.3). The device completely can't be reseted via this connector.

2.18.5 HSTCU

Infineon's **AURIX™** TC4xx devices have a standardized set of tool interfaces (DAP, DAPE, trigger pins, SGBT, SGMII). With this new family **Infineon Technologies** specifies a standardized pinning for all these interfaces for the cost effective and small USB Type-C connector. This pinning is not compatible to regular USB devices, but ensures that there is no damage for any combination of regular USB hardware, HSTCU (High Speed Tool Connector USB-C) boards and tool HW.

The board contains also an Auxiliary power connector (not assembled per default) and mounting holes.

Please see Application Note AP32536 for more and detailed information.

For pinout of this connector see **Figure 30**.

2.18.6 High speed with DAP/DAPE/HSTCU

For use the DAP connection with 160 MHz you need to remove some resistors to have a very short connection between device and connector. On the **TriBoard TC4X7 COM** this are 4 resistors R520, R521, R522 and R523 for DAP and/or R522, R523 and R526 for DAPE (red marked in **Figure 13**). These resistors need to be removed.

Important: When the resistors are removed then only the DAP, DAPE and HSTCU connector on the board can be used. The on-board wiggler and the ETK connector couldn't be used in this case.

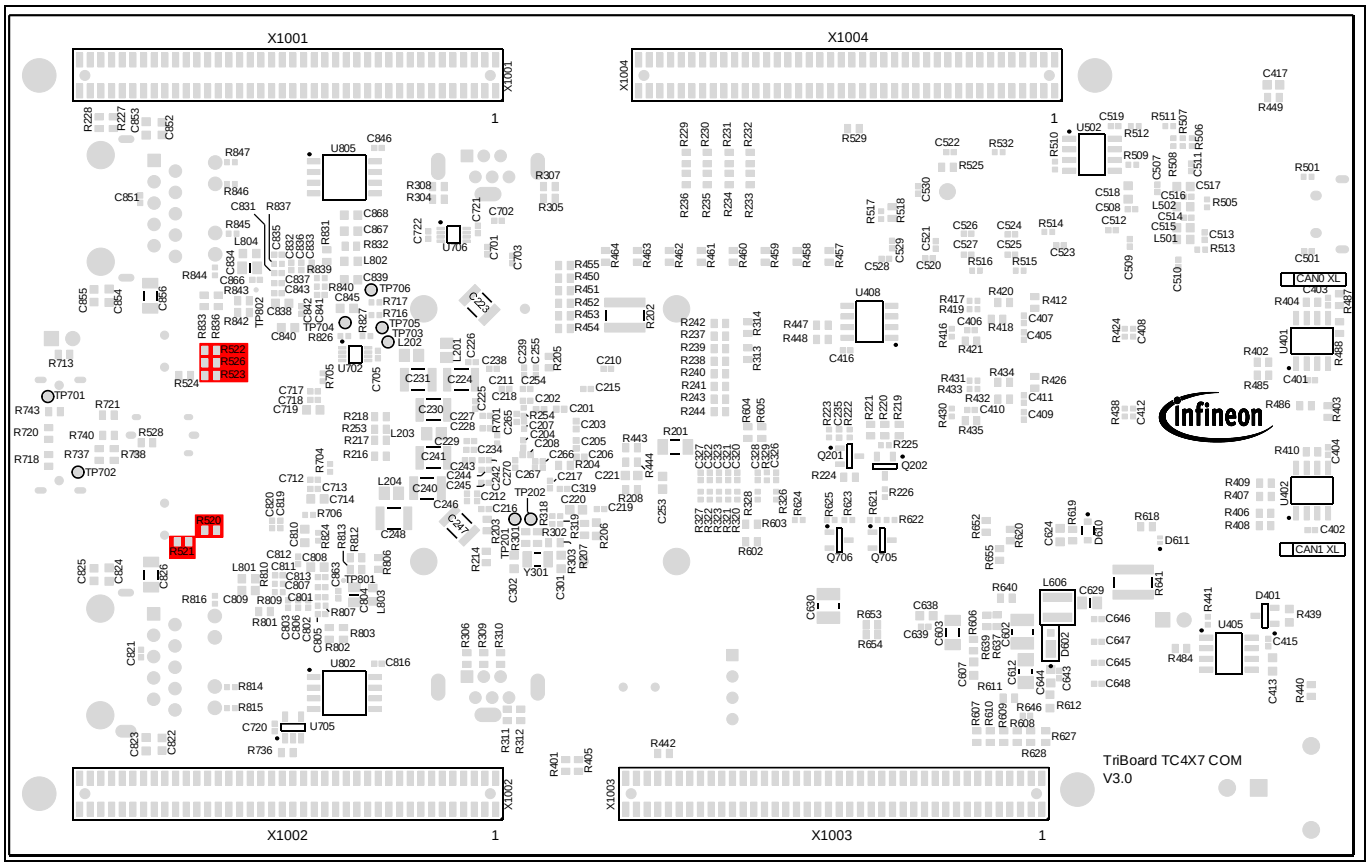


Figure 13 Location of DAP resistors

2.18.7 ETK connector (optional)

The **TriBoard TC4X7 COM** provide a 10 pin Samtec connector (X504) for connecting to an ETK. This connector should be assembled by yourself if needed.

For the pinout of connector see **Figure 31**.

The needed Samtec connector is: TFM-105-02-L-D.

3 TriBoard Configuration

3.1 HW Boot Configuration



Figure 14 HW Configuration DIP-Switches

The figure above shows the definition of the boot HW configuration switch. The meaning of the switches will be described in the following table (**Table 24**).

Note: *The ON position of the switch is equal to a logical LOW at the dedicated pin.*

3.1.1 Default Pad State

P14.4 / HWCFG6 is used to select the Default Pad State. Dipswitch 1 used to select this.

In case that Dispswitch 1 is set to ON then all I/O pins are in tristate otherwise the internal pull-up devices are enabled on the I/O pins. Please note that after change Dipswitch 1 you must make a power cycle (switch off -> switch on) to use the new configuration.

In case that Tristate is selected (Dipswitch 1 is set to ON) then the I/O pins are floating (High-Z). If you need a specific level on different pins during startup (e.g., driver pins) then you must add the needed pull device (up or down). Some pins (especially the HWCFG pins) haven always the needed external pull-up and/or pull-down resistor assembled on the board.

3.1.2 Startup Mode

The startup mode of the device must be defined with the Bootmode Header. Following boot options are possible:

- Internal start
- Bootstrap loader modes
- Alternate boot modes (ABM)

This will be defined in the Boot Mode Index (BMI) of the Boot Mode Header.

This bootmode can be overruled by HWCFG pins:

Table 24 User Startup Modes by HWCFG pins (all devices, expect TC497A and TC4D7) 1)2)3)4)

HWCFG[5...3]	Type of Boot	2	3	4
XX1	Start-up mode is selected by Boot Mode Index	OFF	X	X

1) The shadowed line indicates the default setting.
2) 'x' represents the don't care state.
3) 2 to 4 are the Dip Switch numbers.
4) HWCFG4 and 5 are not used, therefore DIP switch 3 and 4 haven no meaning for boot.

Table 25 User Startup Modes by HWCFG pins (only TC497A) 1)2)3)

HWCFG[5...3]	Type of Boot	2	3	4
XX1	Start-up mode is selected by Boot Mode Index	OFF	X	X
110	Internal Start from Flash	ON	OFF	OFF
100	Alternate Boot Mode, Generic Bootstrap Loader on fail (P14.0/P14.1)	ON	ON	OFF
000	Generic Bootstrap Loader (P14.0/P14.1)	ON	ON	ON

1) The shadowed line indicates the default setting.
2) 'x' represents the don't care state.
3) 2 to 4 are the Dip Switch numbers.

Table 26 User Startup Modes by HWCFG pins (only TC4D7) 1)2)3)4)

HWCFG[5...3]	Type of Boot	2	3	4
XX1	Start-up mode is selected by Boot Mode Index	OFF	X	X
X10	Internal Start from Flash	ON	OFF	X
X00	Generic Bootstrap Loader (P14.0/P14.1)	ON	ON	X

1) The shadowed line indicates the default setting.
2) 'x' represents the don't care state.
3) 2 to 4 are the Dip Switch numbers.
4) HWCFG5 is not used, therefore DIP switch 4 has no meaning for boot.

To start from internal flash, make sure that DIP switch 2 is not set to on and a valid BMHD for start from internal flash is programmed.

3.2 Config Signals

Table 27 Config Signals

Short Name	Description	Comment
P14.5	HWCFG [1]	HWCFG [2:1]: [0 0] – EVRCOFF (default via pull-downs R228 and R227) [0 1] – EVRCON (VDDEXT = 3.3V, 3.3V ≤ VDDEXTDC ≤ 5V) [1 0] – EVRCON (VDDEXT = 5V, 3.3V ≤ VDDEXTDC ≤ 5V) [1 1] – EVRCON (5.5V ≤ VDDEXTDC ≤ 6.5V)
P14.2	HWCFG [2]	
P14.3	HWCFG [3]	HWCFG [3] all devices except TC497A and TC4D7: [1] – Boot via BMI of first valid BMHD (see also **Table 24**) HWCFG [4] Reserved, not used HWCFG [5] Reserved, not used
P10.5	HWCFG [4]	HWCFG [5:3] TC497A: [0 0 0] – Generic Bootstrap (P14.0/1) [0 1 0] – ABM, ASC Bootstrap on fail (P15.2/3) [1 0 0] – ABM, Generic Bootstrap on fail (P14.0/1) [1 1 0] – Internal start from Flash [x x 1] – Boot via BMI of first valid BMHD (see also **Table 25**)
P10.6	HWCFG [5]	HWCFG [4:3] TC4D7: [0 0] – Generic Bootstrap (P14.0/1) [1 0] – ASC Bootstrap (P15.2/3) [x 1] – Boot via BMI of first valid BMHD (see also **Table 26**Table 24) HWCFG [5] Reserved, not used
P14.4	HWCFG [6]	All GPIOs in tri-state or input with pull-up active after reset (see chapter 3.1.1)

3.3 Assembly Options

Some resistors/bridges enable/disable or changing functions of specific signals in **Table 28** and **Table 29**.

To disable the signals, the resistors have to be removed. To enable, the resistor has to be assembled.

3.3.1 General optional resistors

Table 28 Signal mapping of the optional resistors

Resistor	Value	Assembled	Signal name	Size	Comment
R210	0 Ω	no	XTAL1	0402	Connect XTAL1 with X902/X1002
R211	0 Ω	no	XTAL2	0402	Connect XTAL2 with X902/X1002
R212	0 Ω	yes	XTAL2	0603	Serial resistor to reduce oscillator amplitude if needed.
R301	0 Ω	yes	XTAL4	0603	Serial resistor to reduce oscillator amplitude if needed.
R302	0 Ω	no	XTAL4, P33.10	0402	Connect XTAL4/P33.10 with X904/X1004
R303	0 Ω	no	XTAL3, P33.9	0402	Connect XTAL3/P33.9 with X904/X1004
R440	0 Ω	no	LIN, VCC_IN	0603	Connect VCC_IN to LIN connector
R456	0 Ω	yes	QST, LEDs	0603	Connect QST to toggle LEDs D402...D405
R465	0 Ω	yes	QUC, LEDs	0603	Connect QUC to toggle LEDs D406...D409
R524	0 Ω	yes	USR1, DAP3	0603	Connect DAP3 to USR1 of DAP
R525	0 Ω	no	USR1, P20.2	0603	Connect P20.2 to USR1 of miniWiggler JDS
R527	0 Ω	no	USR1, /TRST	0603	Connect /TRST to USR1 of miniWiggler JDS
R528	0 Ω	no	AUX, P20.2	0603	Connect P20.2 to AUX of HSTCU
R529	0 Ω	no	ETK, P20.1	0603	Connect P20.1 to ETK BRKIO
R530	0 Ω	no	+1V8	0603	Connect 1,8V from board to AUX power connector
R647	0 Ω	no	P33.11	0603	Connect P33.11 to INT2 of TLF4D985

Note: All resistors are red marked in the following figures.

3 TriBoard Configuration

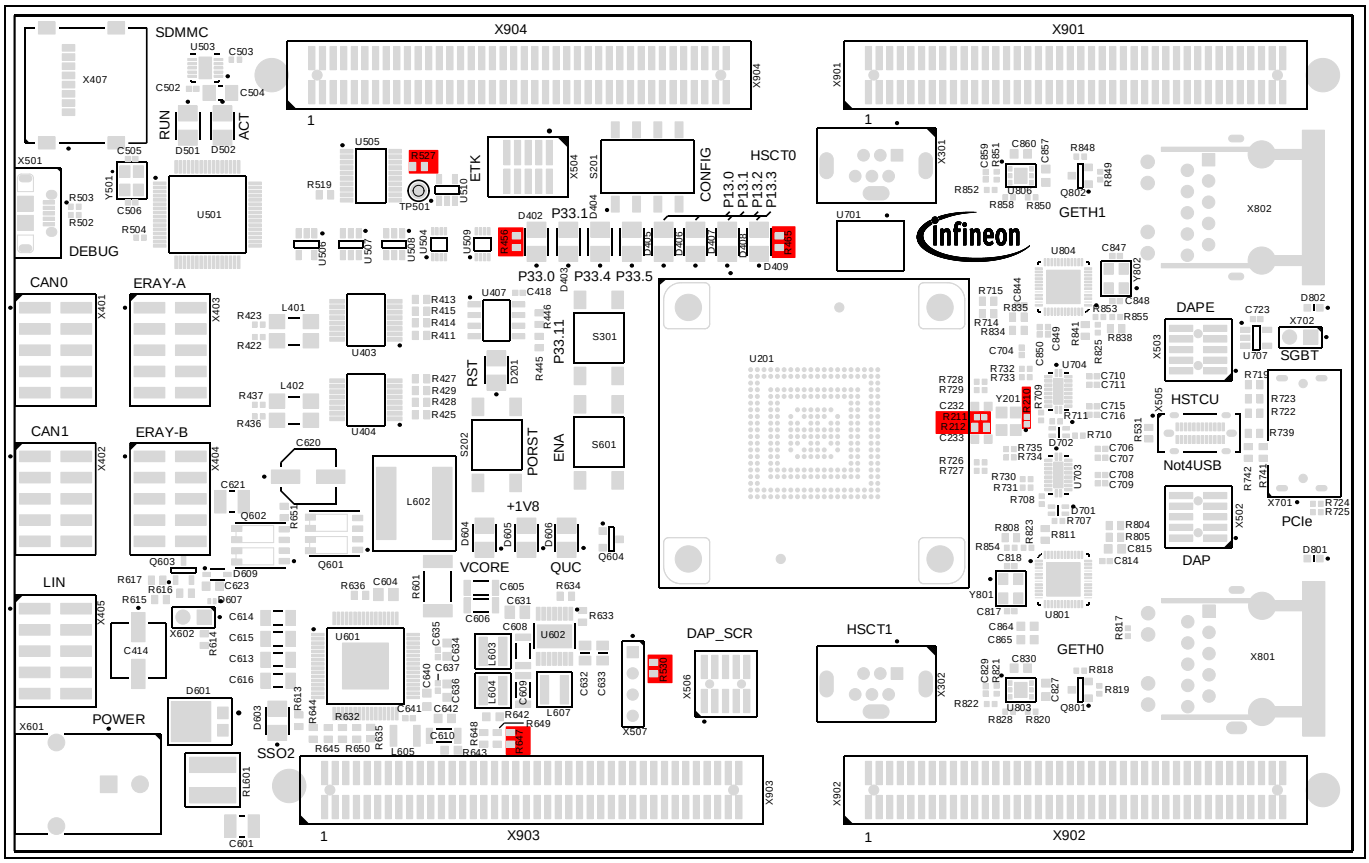


Figure 15 Location of general optional resistors on Top Side

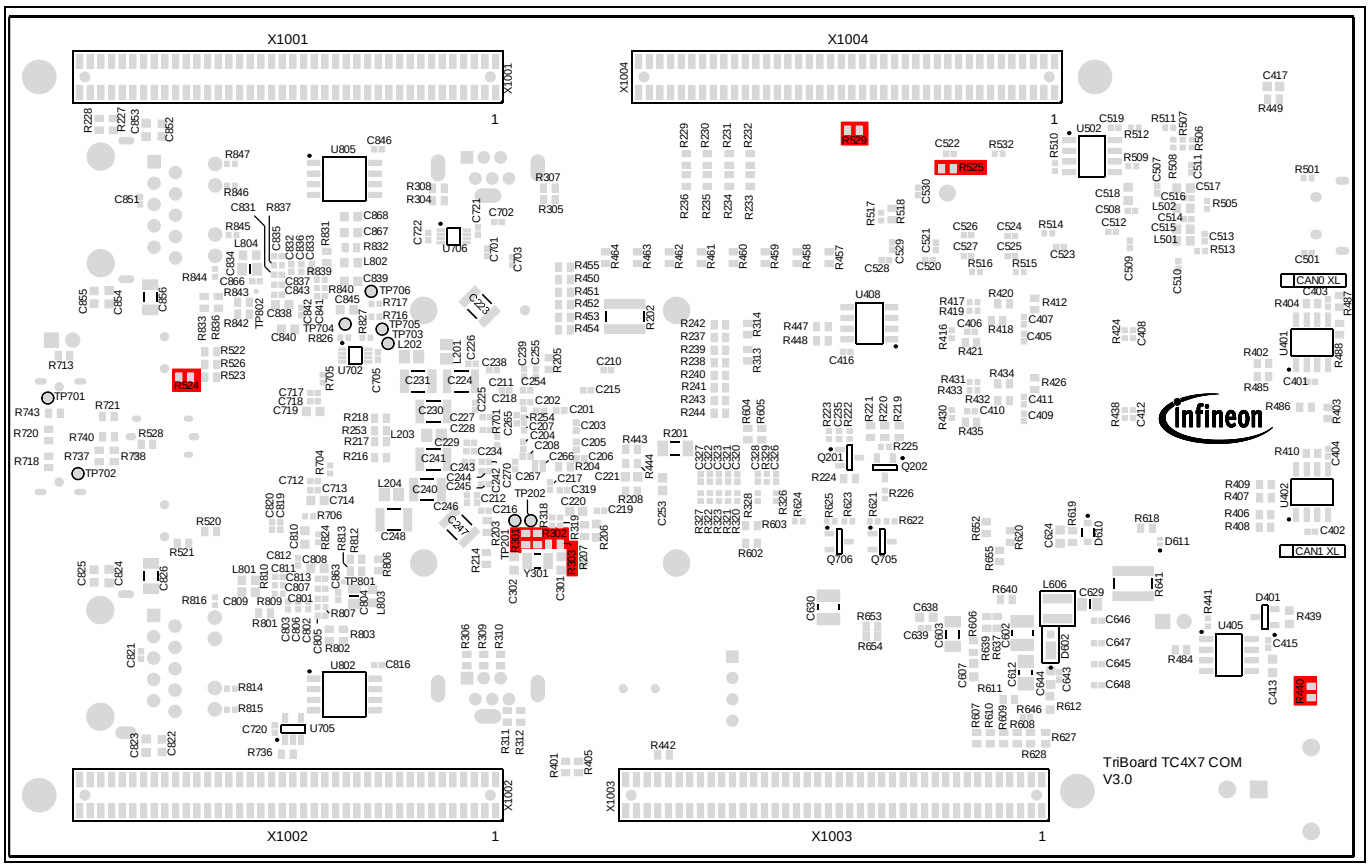


Figure 16 Location of general optional resistors on Bottom Side

3.3.2 Resistors for peripherals

Table 29 Signal mapping of the peripheral resistors

Resistor	Value	Assembled	Signal name	Size	Comment
R207	2,2 Ω	yes	VAREF1	0603	Connect VAREF1 to QVR
R208	2,2 Ω	yes	VAREF2	0603	Connect VAREF2 to QVR
R401	0 Ω	yes	CAN0 STB	0603	Connect P00.3 to STB of CAN0 transceiver
R402	0 Ω	yes	CAN0 TXD	0603	Connect P33.8 to TXD of CAN0 transceiver
R403	0 Ω	yes	CAN0 RXD	0603	Connect P33.7 to RXD of CAN0 transceiver
R405	0 Ω	yes	CAN1 STB	0603	Connect P00.2 to STB of CAN1 transceiver
R406	0 Ω	yes	CAN1 TXD	0603	Connect P14.10 to TXD of CAN1 transceiver
R407	0 Ω	yes	CAN1 RXD	0603	Connect P14.8 to RXD of CAN1 transceiver
R408	0 Ω	no	CAN1 TXD	0603	Connect P14.0 to TXD of CAN1 transceiver
R409	0 Ω	no	CAN1 RXD	0603	Connect P14.1 to RXD of CAN1 transceiver
R411	0 Ω	yes	ERAY-A EN	0603	Connect P00.5 to EN of ERAY-A transceiver
R412	0 Ω	yes	ERAY-A ERRN	0603	Connect P02.7 to ERRN of ERAY-A transceiver
R413	0 Ω	yes	ERAY-A RXD	0603	Connect P02.1 to RXD of ERAY-A transceiver
R414	0 Ω	yes	ERAY-A TXD	0603	Connect P02.0 to TXD of ERAY-A transceiver
R415	0 Ω	yes	ERAY-A TXEN	0603	Connect P02.4 to TXEN of ERAY-A transceiver
R425	0 Ω	yes	ERAY-B EN	0603	Connect P00.6 to EN of ERAY-B transceiver
R426	0 Ω	yes	ERAY-B ERRN	0603	Connect P02.8 to ERRN of ERAY-B transceiver
R427	0 Ω	yes	ERAY-B RXD	0603	Connect P02.3 to RXD of ERAY-B transceiver
R428	0 Ω	yes	ERAY-B TXD	0603	Connect P02.2 to TXD of ERAY-B transceiver
R429	0 Ω	yes	ERAY-B TXEN	0603	Connect P02.5 to TXEN of ERAY-B transceiver
R442	0 Ω	yes	LIN EN	0603	Connect P00.7 to EN of LIN transceiver
R443	0 Ω	yes	LIN TXD	0603	Connect P00.9 to TXD of LIN transceiver
R444	0 Ω	yes	LIN RXD	0603	Connect P00.12 to RXD of LIN transceiver
R445	0 Ω	yes	I2C SDA	0603	Connect P15.5 to SDA of serial Eeproms
R446	0 Ω	yes	I2C SCL	0603	Connect P15.4 to SCL of serial Eeproms
R450	0 Ω	yes	SDMMC DAT2	0603	Connect P20.10 to DAT2 of SDMMC slot
R451	0 Ω	yes	SDMMC DAT3	0603	Connect P20.11 to DAT3 of SDMMC slot
R452	0 Ω	yes	SDMMC CMD	0603	Connect P15.3 to CMD of SDMMC slot
R453	0 Ω	yes	SDMMC CLK	0603	Connect P15.1 to CLK of SDMMC slot
R454	0 Ω	yes	SDMMC DAT0	0603	Connect P20.7 to DAT0 of SDMMC slot
R455	0 Ω	yes	SDMMC DAT1	0603	Connect P20.8 to DAT1 of SDMMC slot
R485	0 Ω	no	CAN0 TXD	0603	Connect P02.2 to TXD of CAN0 transceiver
R486	0 Ω	no	CAN0 RXD	0603	Connect P02.3 to RXD of CAN0 transceiver

(table continues...)

Resistor	Value	Assembled	Signal name	Size	Comment
R714	0 Ω	yes	MDC_1V8	0603	Connect P16.11 to MDC via level shifter
R715	0 Ω	yes	MDIO_1V8	0603	Connect P16.14 to MDIO via level shifter
R720	0 Ω	no	PCIE_WAKEA	0603	Connect P23.4 to OcuLink connector pin A10
R721	0 Ω	yes	PCIE_PERST	0603	Connect P23.1 to signal PCIE_PERST
R737	0 Ω	no	PCIE_REFCLKA_P	0603	Connect signal PCIE_REFCLK_P to OcuLink connector pin A12
R738	0 Ω	no	PCIE_REFCLKA_N	0603	Connect signal PCIE_REFCLK_N to OcuLink connector pin A13
R739	0 Ω	no	PCIE_REFCLKB_P	0603	Connect signal PCIE_PERST to OcuLink connector pin B12
R740	0 Ω	yes	PCIE_REFCLKA_P	0603	Connect signal PCIE_PERST to OcuLink connector pin A12
R741	0 Ω	yes	PCIE_REFCLKB_P	0603	Connect signal PCIE_REFCLK_P to OcuLink connector pin B12
R742	0 Ω	yes	PCIE_REFCLKB_N	0603	Connect signal PCIE_REFCLK_N to OcuLink connector pin B13
R743	0 Ω	yes	PCIE_WAKEB	0603	Connect P23.4 to OcuLink connector pin B10
R808	0 Ω	yes	PHYRSTB_N	0603	Connect P00.10 to PHYRSTB_N of GETH0 PHY
R811	0 Ω	yes	INTB	0603	Connect P10.2 to INTB and GETH0 PHY
R812	0 Ω	yes	MDC	0603	Connect MDC to MDC of GETH0 PHY
R813	0 Ω	yes	MDIO	0603	Connect MDIO to MDIO of GETH0 PHY
R838	0 Ω	yes	PHYRSTB_N	0603	Connect P00.11 to PHYRSTB_N of GETH1 PHY
R841	0 Ω	yes	INTB	0603	Connect P10.3 to INTB and GETH1 PHY
R842	0 Ω	yes	MDC	0603	Connect MDC to MDC of GETH1 PHY
R843	0 Ω	yes	MDIO	0603	Connect MDIO to MDIO of GETH1 PHY

Note: All resistors are red marked in the following figures.

3 TriBoard Configuration

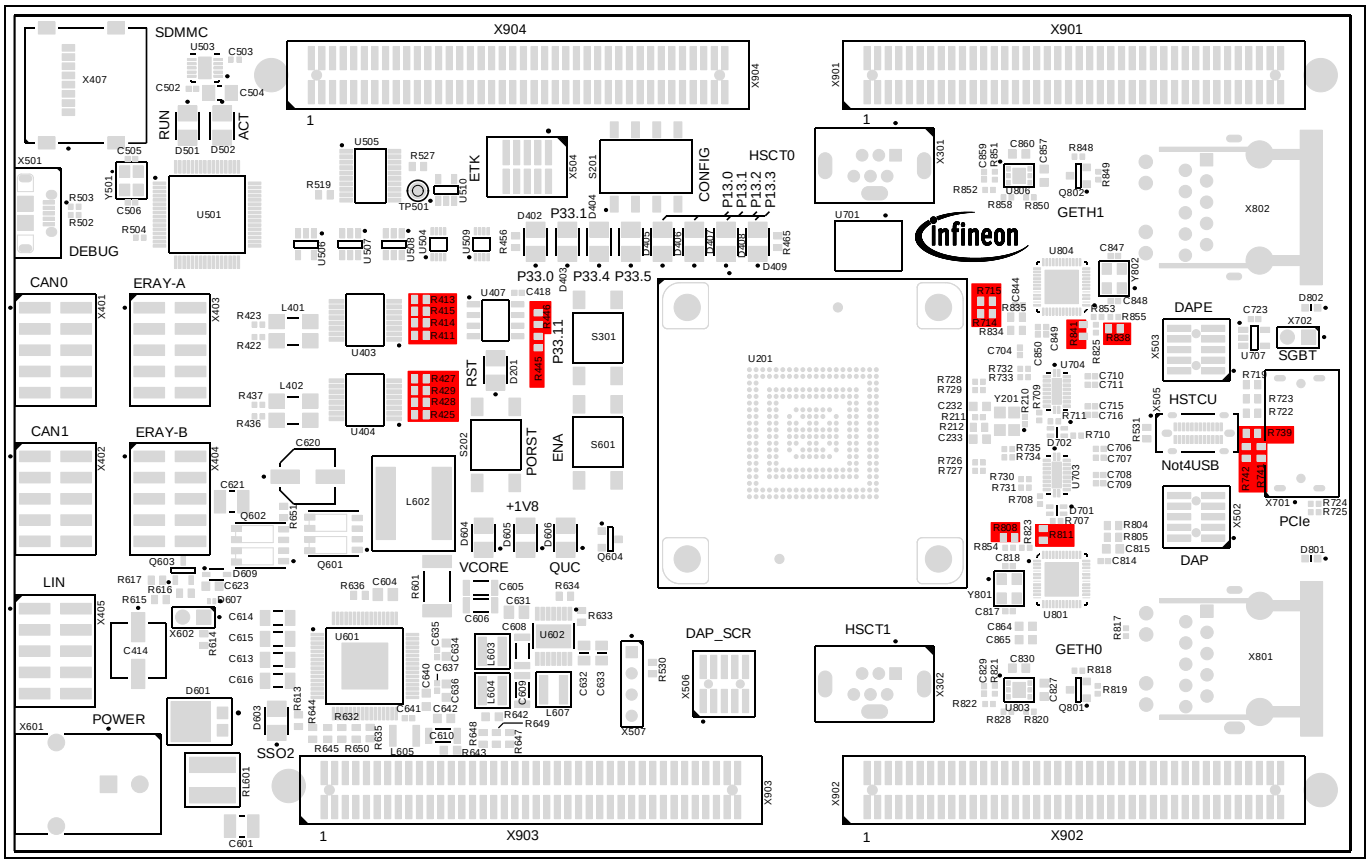


Figure 17 Location of peripheral resistors on Top Side

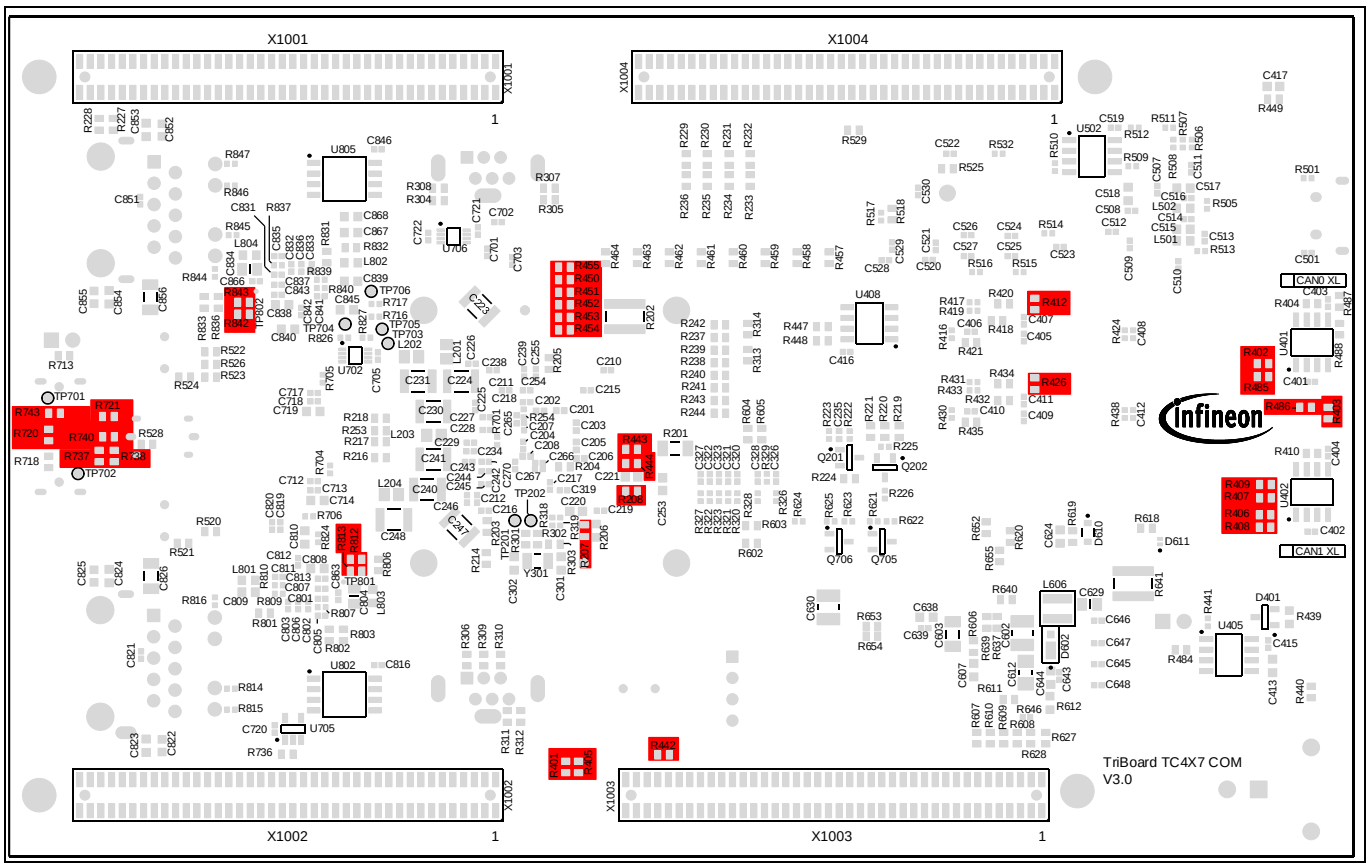


Figure 18 Location of peripheral resistors on Bottom Side

4 Connector Pin Assignment

The TriBoard will be shipped with four male (plug) connectors on top layer and four female (socket) connectors on bottom layer. The default connectors are 80-pol. Board to Board connectors from Samtec:

http://www.samtec.com

Plug:

FTSH-140-02-L-DV-ES-A

Socket:

FLE-140-01-G-DV-A

4.1 Not connected AURIX™ signals

Following **AURIX™** pins are not used on board and are not connected to any connector also not via resistor:

Table 30 Not connected AURIX™ signals

Short Name	Description
VGATE1P	DCDC P ch MOSFET gate driver output (EVRC not used, VDD supplied by TLF4D985)
VGATE1N	DCDC N ch MOSFET gate driver output (EVRC not used, VDD supplied by TLF4D985)

4.2 Only on board used AURIX™ signals

Following **AURIX™** pins are used on board only and are not connected to any connector also not via resistor:

Table 31 Only on board used AURIX™ signals

Short Name	Description
P16.0	XSPI_CLK_INV Clock out inverted
P16.1	XSPI_CLK Clock out
P16.2	XSPI_RWDS Data strobe
P16.3	XSPI_RXD1/XSPI_TXD1 Receive data/Transmit data
P16.4	Reset input from XSPI flash
P16.5	XSPI_RXD2/XSPI_TXD2 Receive data/Transmit data
P16.6	XSPI_RXD3/XSPI_TXD3 Receive data/Transmit data
P16.7	XSPI_RXD0/XSPI_TXD0 Receive data/Transmit data
P16.8	XSPI_RXD4/XSPI_TXD4 Receive data/Transmit data
P16.9	XSPI_RXD5/XSPI_TXD5 Receive data/Transmit data
P16.10	XSPI_RXD6/XSPI_TXD6 Receive data/Transmit data
P16.11	GETH0_MDC1 MDIO Clock
P16.12	XSPI_RXD7/XSPI_TXD7 Receive data/Transmit data
P16.13	XSPI_CS0_N Chip Select 0
P16.14	GETH0_MDIOB/GETH0_MDIO1 MDIO input/output

4.3 TC4X7 Connector / Top View

X901 and X1001				X902 and X1002			
GND	1	2	GND	GND	1	2	GND
GND	3	4	GND	GND	3	4	GND
	5	6	P21.6	VCC_IN	5	6	VCC_IN
	7	8	P21.7	VCC_IN	7	8	VCC_IN
	9	10		P22.4	9	10	P22.8
	11	12		P22.5	11	12	P22.9
	13	14		P22.6	13	14	P22.10
	15	16		/ESR1	15	16	/ESR0
	17	18		P22.7	17	18	P22.11
	19	20		GND	19	20	GND
	21	22		P14.4	21	22	/PORST
	23	24		P10.5	23	24	P23.3
	25	26		P10.4	25	26	P23.4
	27	28		P10.2	27	28	P23.1
	29	30		P13.1	29	30	P22.1
	31	32		P13.0	31	32	P22.0
	33	34		P13.3	33	34	P22.3
	35	36		P13.2	35	36	P22.2
	37	38		P20.9	37	38	P20.10
	39	40		P20.13	39	40	P00.4
	41	42		P33.5	41	42	P20.6
	43	44		P20.3	43	44	P20.2
	45	46		P00.0	45	46	P00.3
	47	48		P00.1	47	48	P00.2
	49	50	P21.2	GND	49	50	GND
	51	52	P21.3	XTAL1*	51	52	P32.4
	53	54	P21.4	XTAL2*	53	54	P14.6
	55	56	P21.5	P15.3	55	56	P15.5
	57	58		P15.2	57	58	P15.4
	59	60		P14.1	59	60	P15.1
	61	62		P14.0	61	62	P15.0
	63	64		P20.11	63	64	P00.12
	65	66		P20.14	65	66	P00.11
	67	68		P20.12	67	68	P00.5
	69	70		P20.7	69	70	P20.8
	71	72	P20.0	P15.8	71	72	P10.8
P14.2	73	74		P10.7	73	74	P10.3
P14.5	75	76		-	75	76	GND
	77	78		QUC	77	78	QUC (+3V3)
P21.0	79	80	P21.1	QUC	79	80	QUC (+3V3)

Figure 19 Connector for TC4X7 – Pinout (Part I, Top View)

Note: *Red marked signals are different compared with TriBoard TC3x7*
** XTAL1 and XTAL2 are only available when optional resistors R210 and R211 are assembled.*

4 Connector Pin Assignment

X903 and X1003					X904 and X1004				
GND	1	2	GND		GND	1	2	GND	
GND	3	4	GND		GND	3	4	GND	
AN0	5	6	AN16		P00.9	5	6	P03.14	
AN1	7	8	AN17		P00.10	7	8	P03.15	
AN2	9	10	AN18		P02.0	9	10		
AN3	11	12	AN19		P02.1	11	12		
AN4	13	14	AN20		P02.2	13	14		
AN5	15	16	AN21		P02.3	15	16		
AN6	17	18	AN22		P02.4	17	18	P14.7	
AN7	19	20	AN23		P02.5	19	20	P14.8	
AN8	21	22	AN24		P02.9	21	22	P14.9	
AN9	23	24	AN25		P02.10	23	24	P14.10	
AN10	25	26	AN26		P02.11	25	26	P15.6	
AN11	27	28	AN27		P01.3	27	28	P15.7	
AN12	29	30	AN28		P01.4	29	30	P20.1	
AN13	31	32	AN29		-	31	32	P01.5	
AN14	33	34	AN30		-	33	34	P01.6	
AN15	35	36	AN31		P10.6	35	36	-	
GND	37	38	GND		-	37	38	-	
VDDM	39	40	VAREF1		-	39	40	P23.5	
GND	41	42	VAREF2		P03.0	41	42	-	
GND	43	44	GND		P03.1	43	44	-	
-	45	46	-		P03.2	45	46		
-	47	48	-		P03.3	47	48		
-	49	50	-		P03.4	49	50	P32.2	
-	51	52	-		P03.5	51	52	-	
-	53	54	-		P03.6	53	54	P32.5	
-	55	56	-		P03.7	55	56	P33.8	
-	57	58	-		P03.8	57	58	P33.9*	
-	59	60	-		P03.9	59	60	P33.10*	
GND	61	62	GND		P03.10	61	62	P33.13	
P33.3	63	64	P33.6		P03.11	63	64	P33.14	
P33.2	65	66	P33.0		P03.12	65	66	P33.15	
P33.1	67	68	P33.4		P03.13	67	68	P32.6	
QUC	69	70	QUC (+3V3)		P34.1	69	70	P32.7	
P02.6	71	72	P00.6		P34.2	71	72	P34.4	
P02.7	73	74	P00.7		P34.3	73	74	P34.5	
P02.8	75	76	P00.8		QUC	75	76	P01.7	
P33.7	77	78	P14.3		QUC	77	78	QUC (+3V3)	
P33.11	79	80	P33.12		QUC	79	80	QUC (+3V3)	

Figure 20 Connector for TC4X7 – Pinout (Part II, Top View)

Note: *Red marked signals are different compared with TriBoard TC3x7*
** P33.9 and P33.10 are only available when optional resistors R303 and R302 are assembled.*

4.4 Power connector pinout

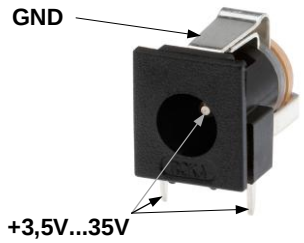


Figure 21 Power connector pinout (Roka 520 2550)

4.5 Micro USB connector pinout

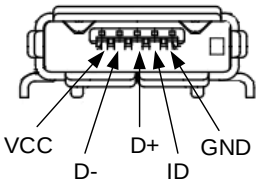


Figure 22 USB connector pinout (Micro USB B-type)

4.6 FlexRay™ (ERAY) connector pinout

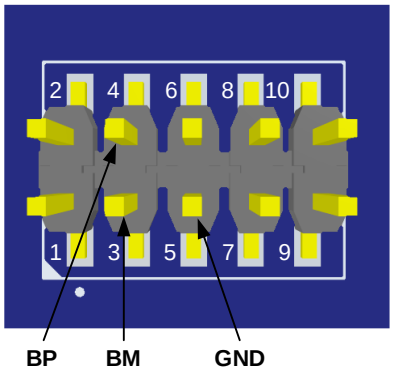


Figure 23 FlexRay™ (ERAY) connector pinout (IDC10)

4.7 CAN connector pinout

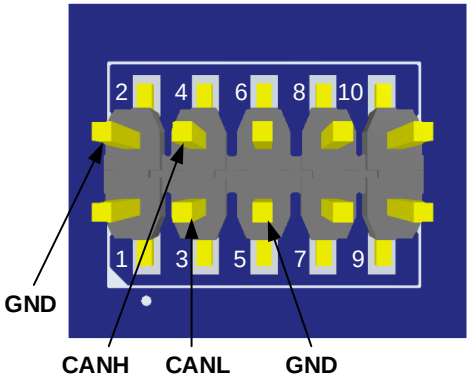


Figure 24 CAN connector pinout (IDC10)

4.8 LIN connector pinout

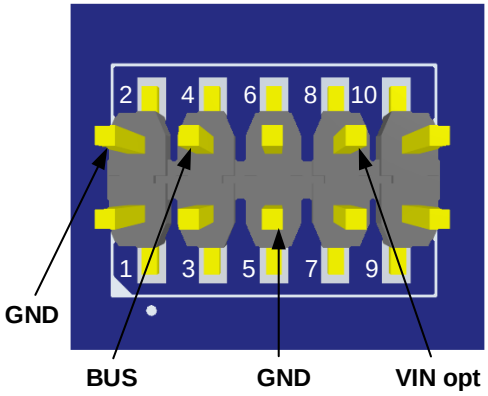


Figure 25 LIN connector pinout (IDC10)

4.9 HSCT connector pinout

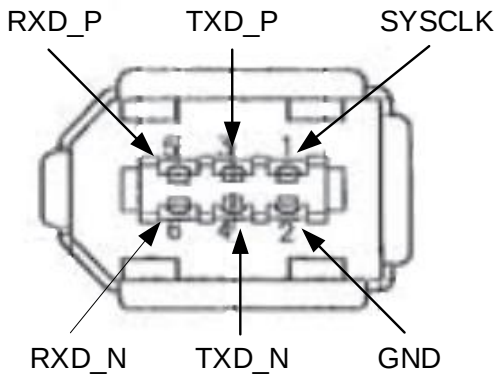


Figure 26 HSCT connector pinout (IEE1394 6-conductor)

4.10 Ethernet connector pinout

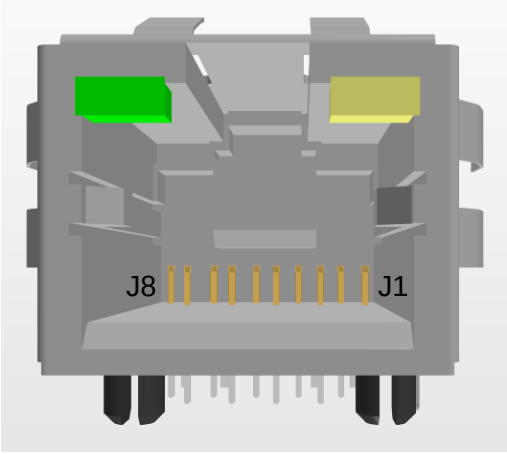


Figure 27 Ethernet connector pinout (RJ45)

4.11 PCIe connector pinout (OcuLink)

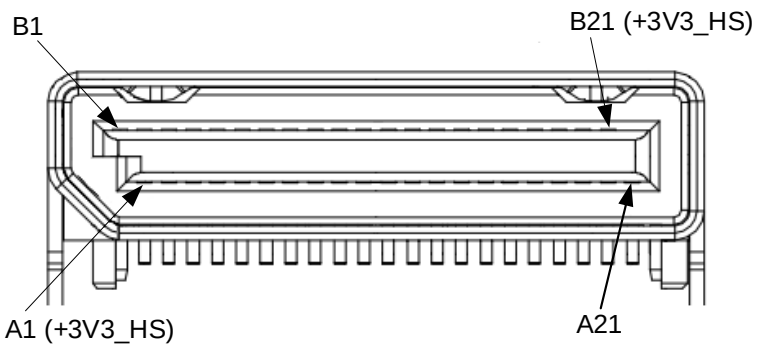


Figure 28 PCIe connector pinout (OcuLink)

4.12 DAP connector pinout

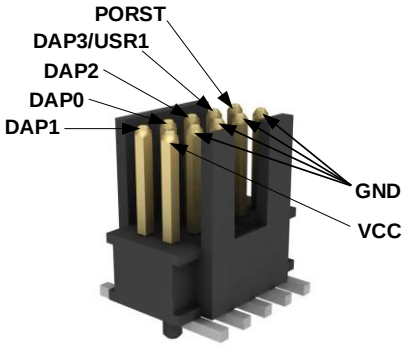


Figure 29 DAP connector pinout (Samtec FTSH10)

4.13 HSTCU connector pinout

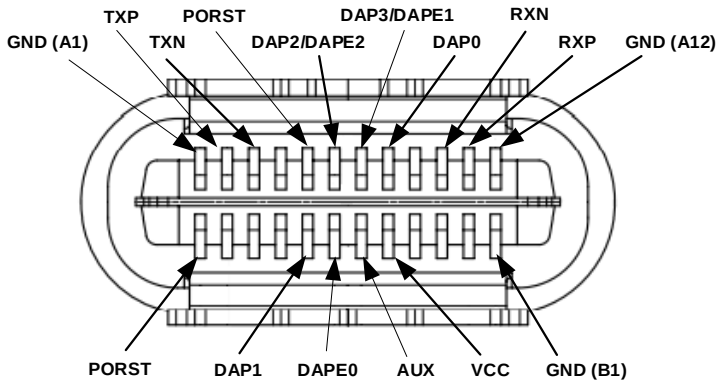


Figure 30 HSTCU connector pinout (USB C-type)

4.14 ETK connector pinout

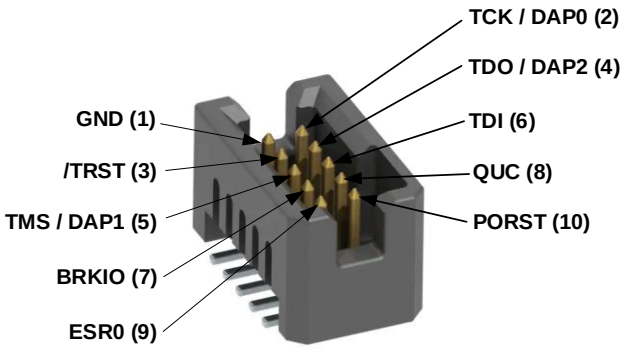


Figure 31 ETK connector pinout (Samtec TFM-105)

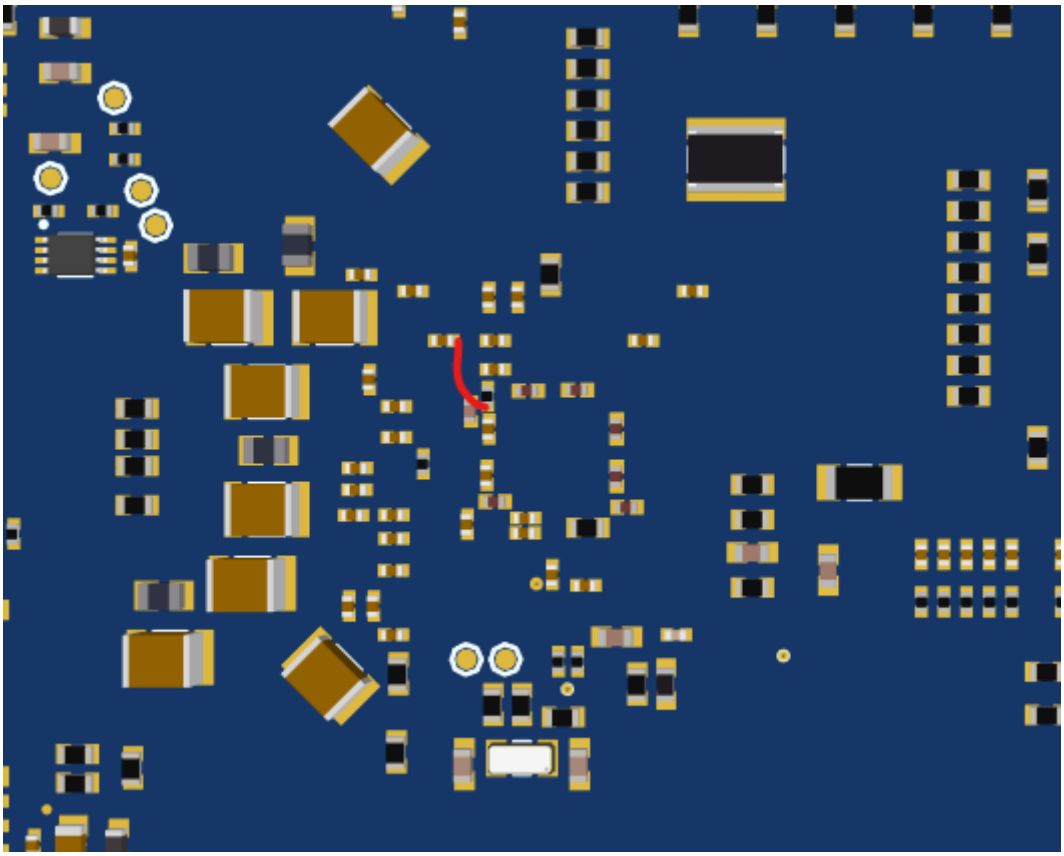
5 Schematics and Placement

5.1 Know problems

The usage of the device internal EVR3NVM regulator is changed (according to errata PMS_TC.034 for the devices TC4Zx, TC48x, TC46x, TC4Ex, TC4Px and TC44) for VDDEXT=3.3V.

For some corner cases e.g., low voltage at VDDEXT may impact access to the NVM memory banks.

In such a case a workaround is to connect VDDP3NVMx to VDDEXT (only for the case VDDEXT=3.3V) via a wire wrap. The needed wire connection is red marked in the following picture:



For productive designs please follow the errata PMS_TC.034 described in the device specific Errata Sheet. In case of a socket board first the socket needs to be disassembled before the wire connection can be placed. Please note in case the wire connection is made and the board has a socket then the board cannot be used with TC4D9 anymore.

5.2 Schematic

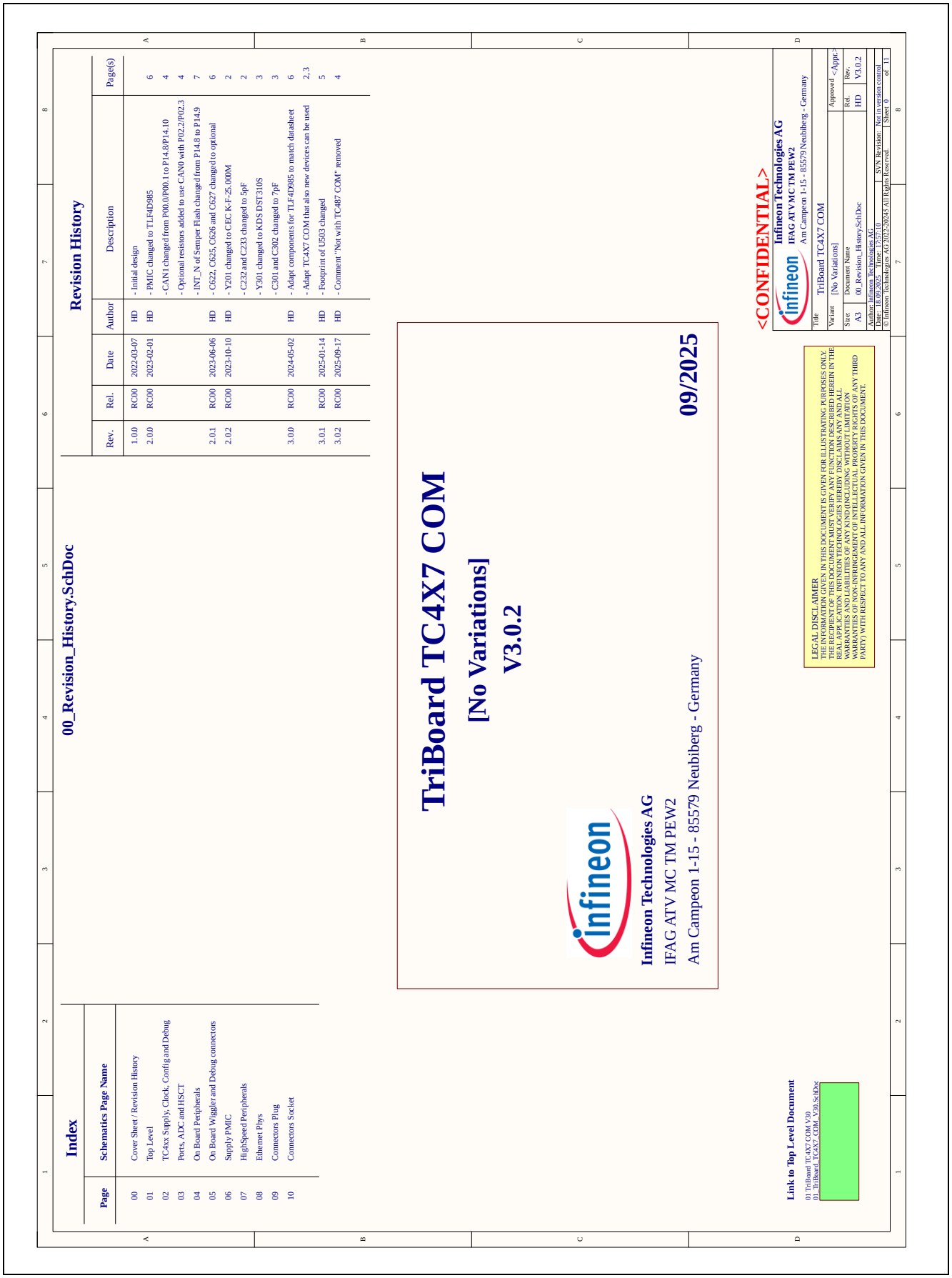


Figure 32 Schematic: Version History

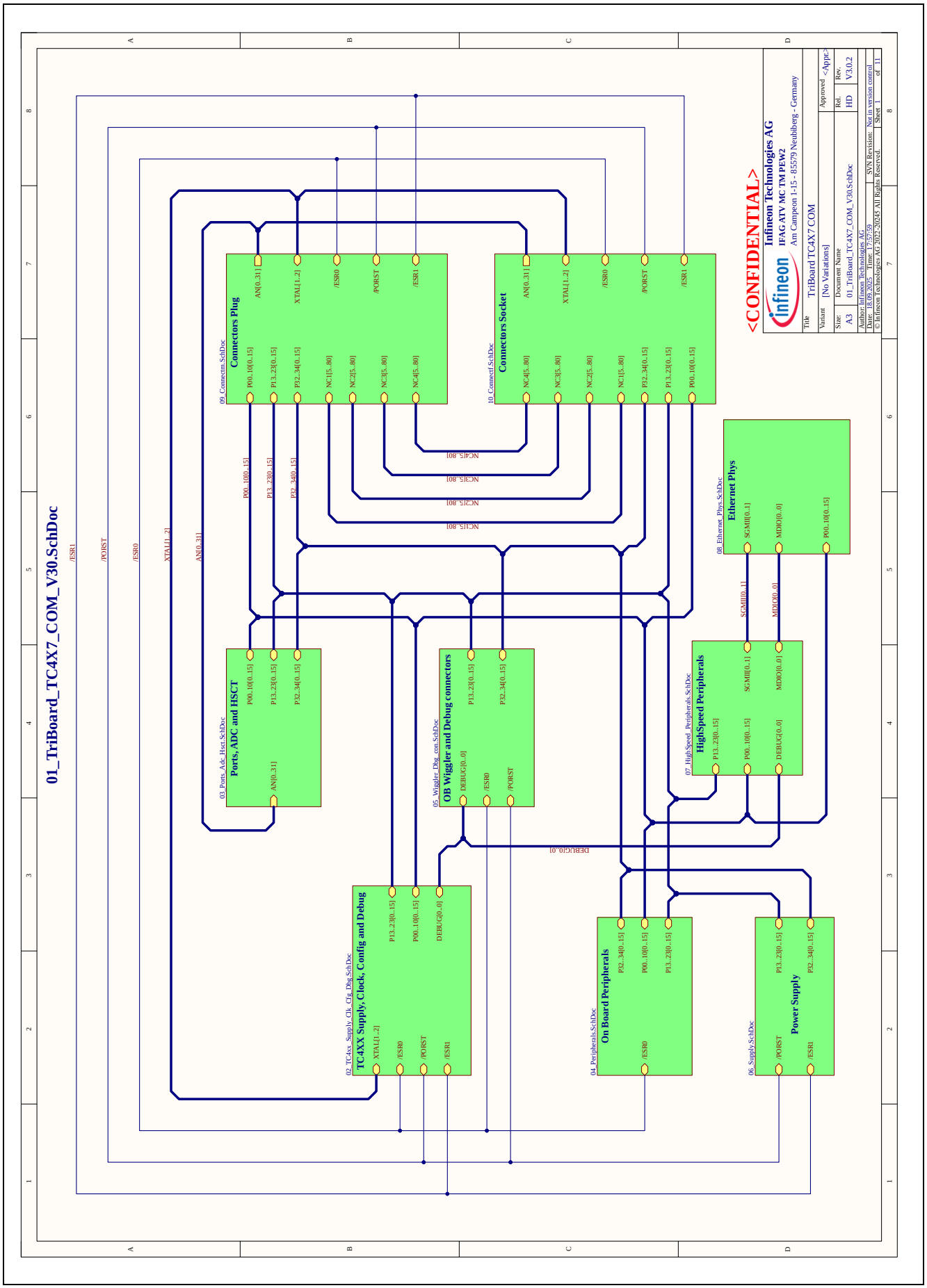


Figure 33 Schematic: Project

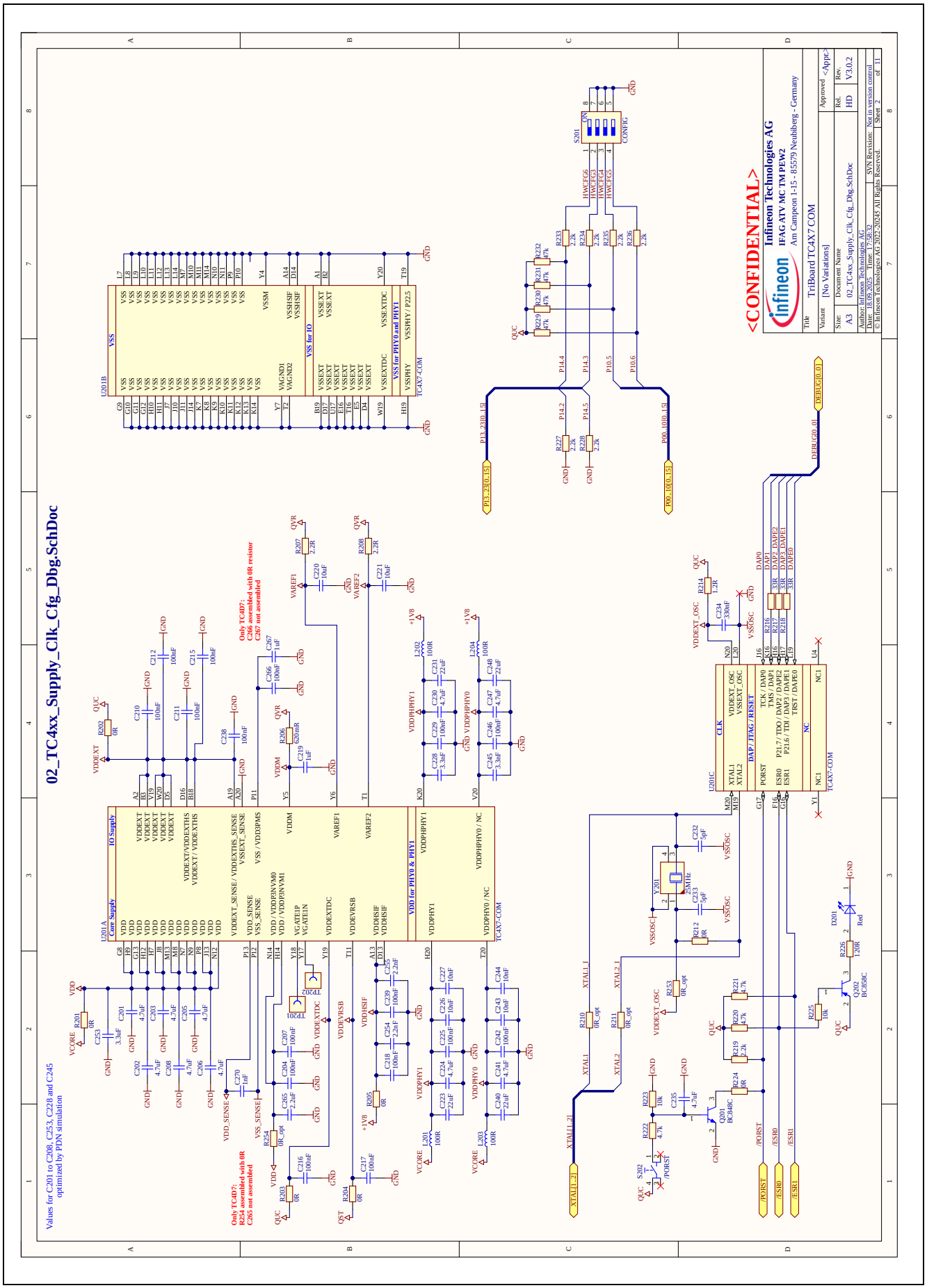


Figure 34 Schematic: TC4xx, supply, clock, config and debug

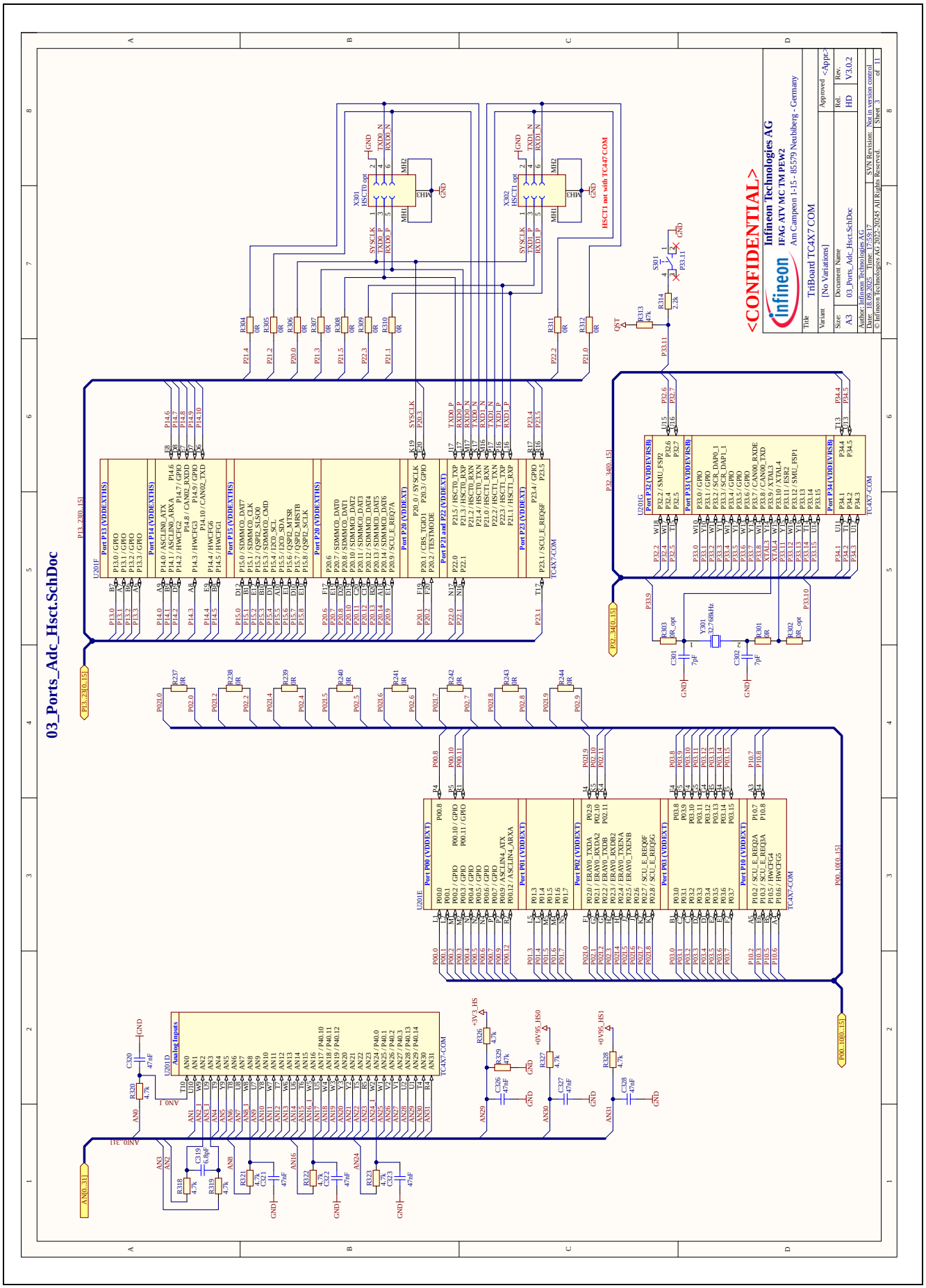


Figure 35 Schematic: TC4xx ports, ADC and HSCT

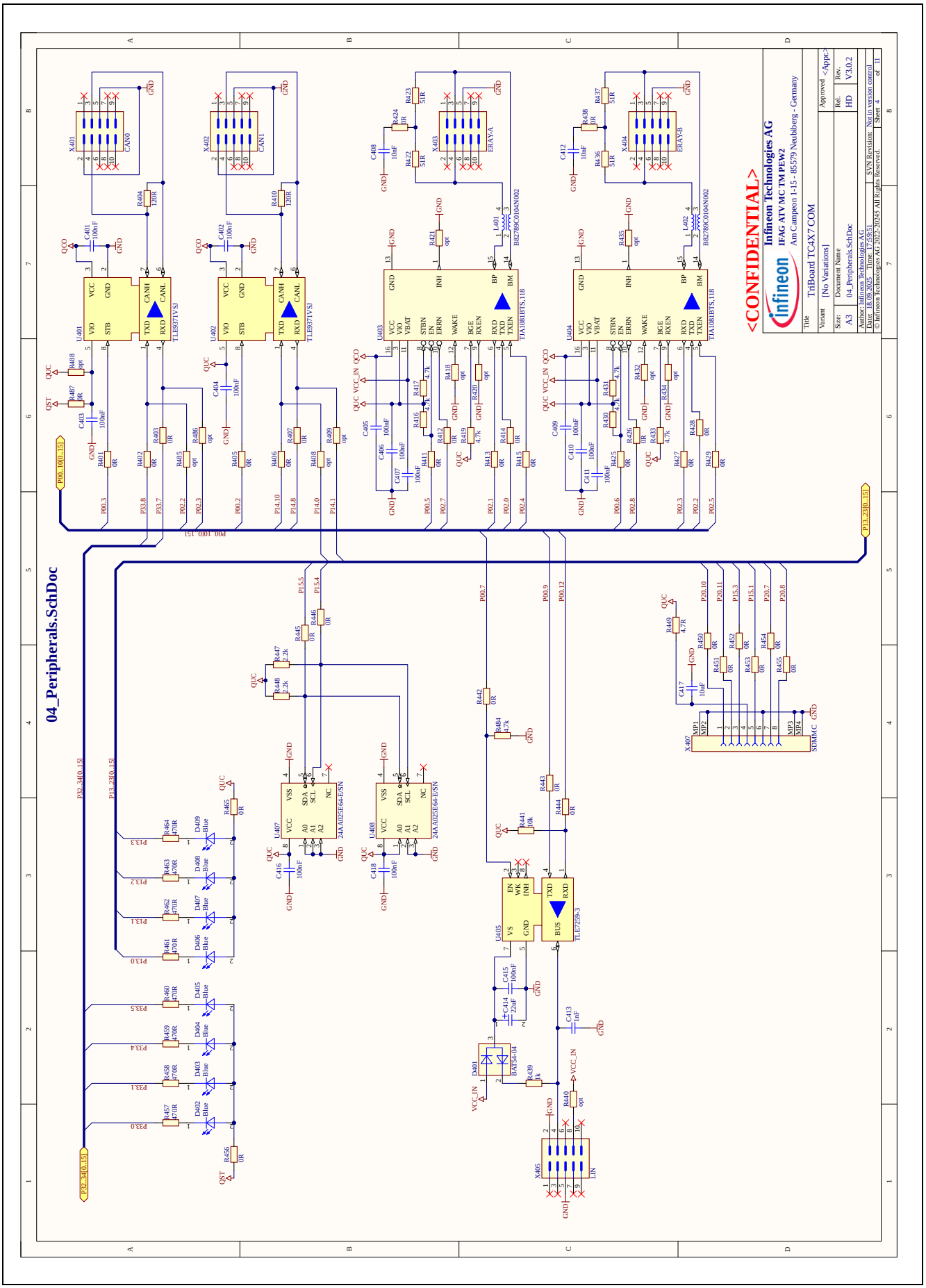


Figure 36 Schematic: On board peripherals

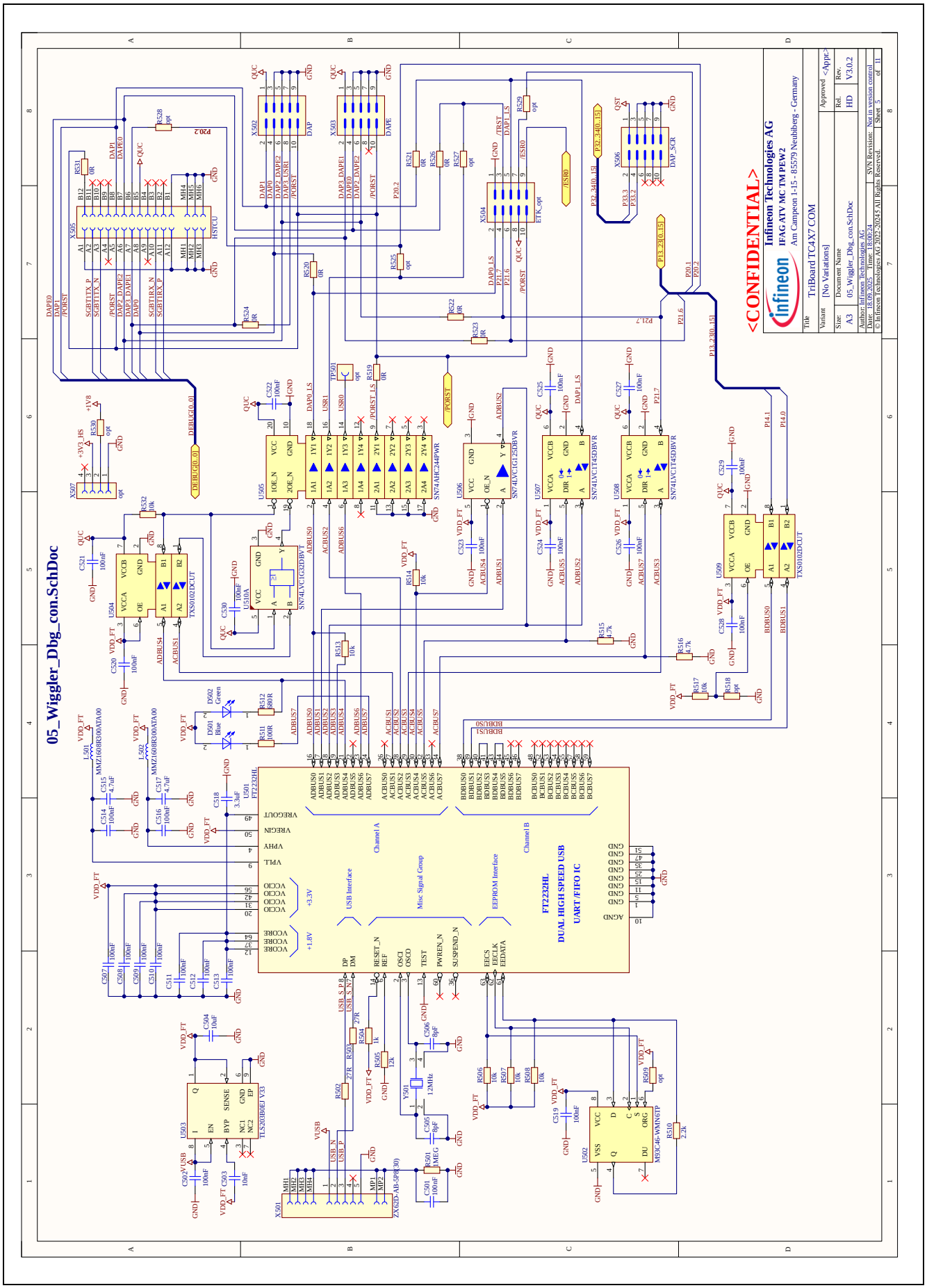


Figure 37 Schematic: On board wiggler and debug connectors

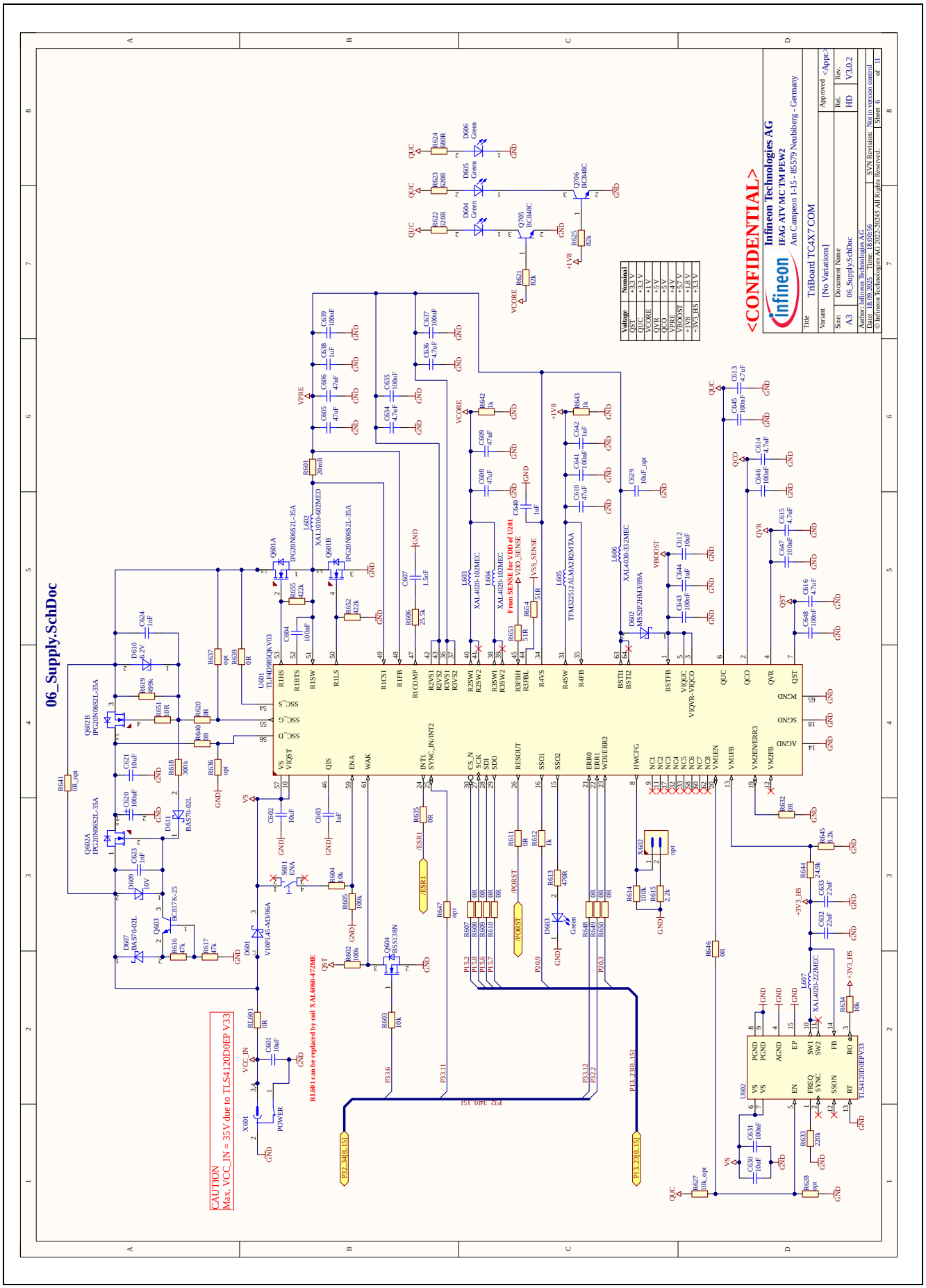


Figure 38 Schematic: Board power supply (PMIC)

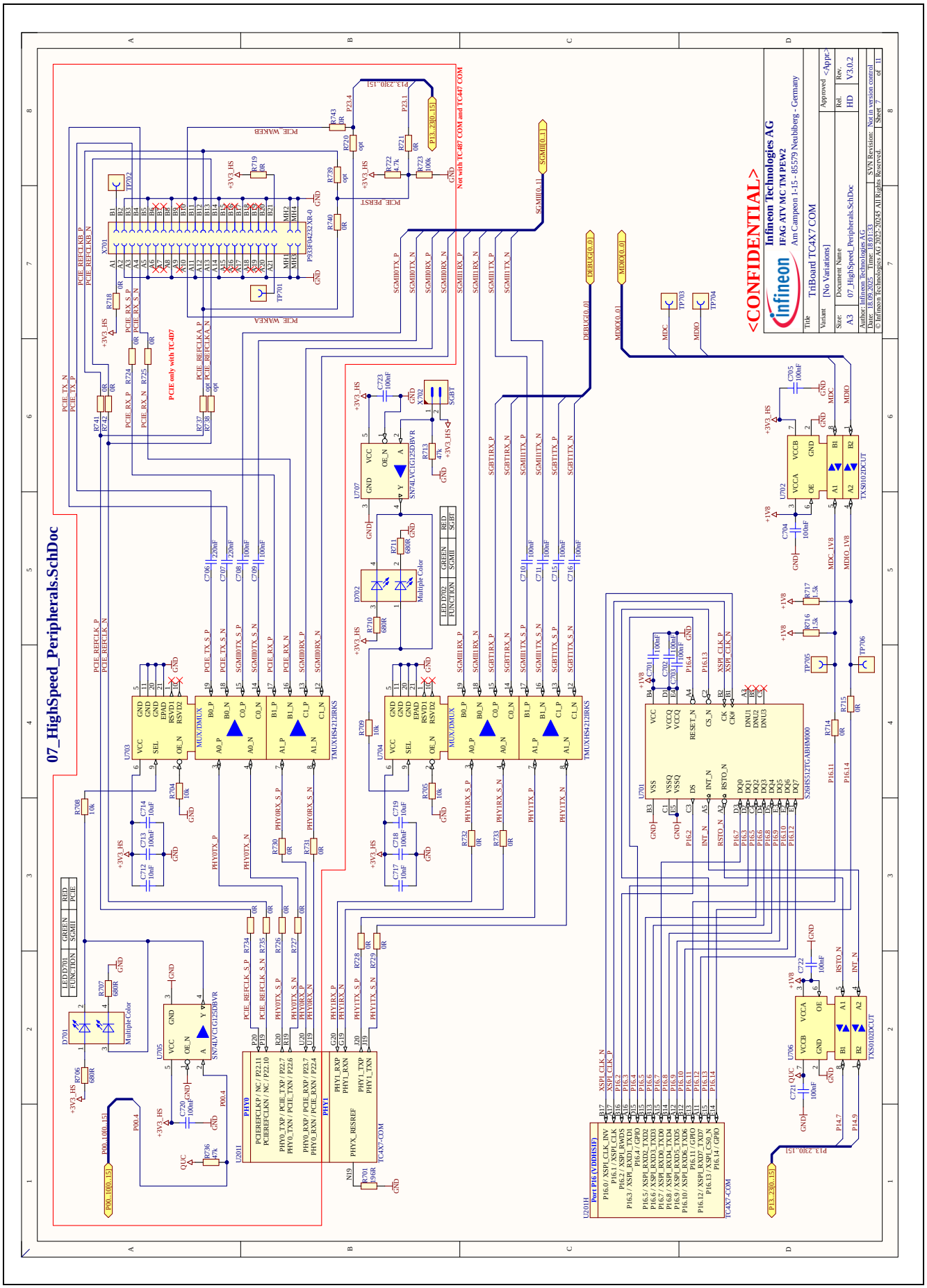


Figure 39 Schematic: High-Speed Peripherals

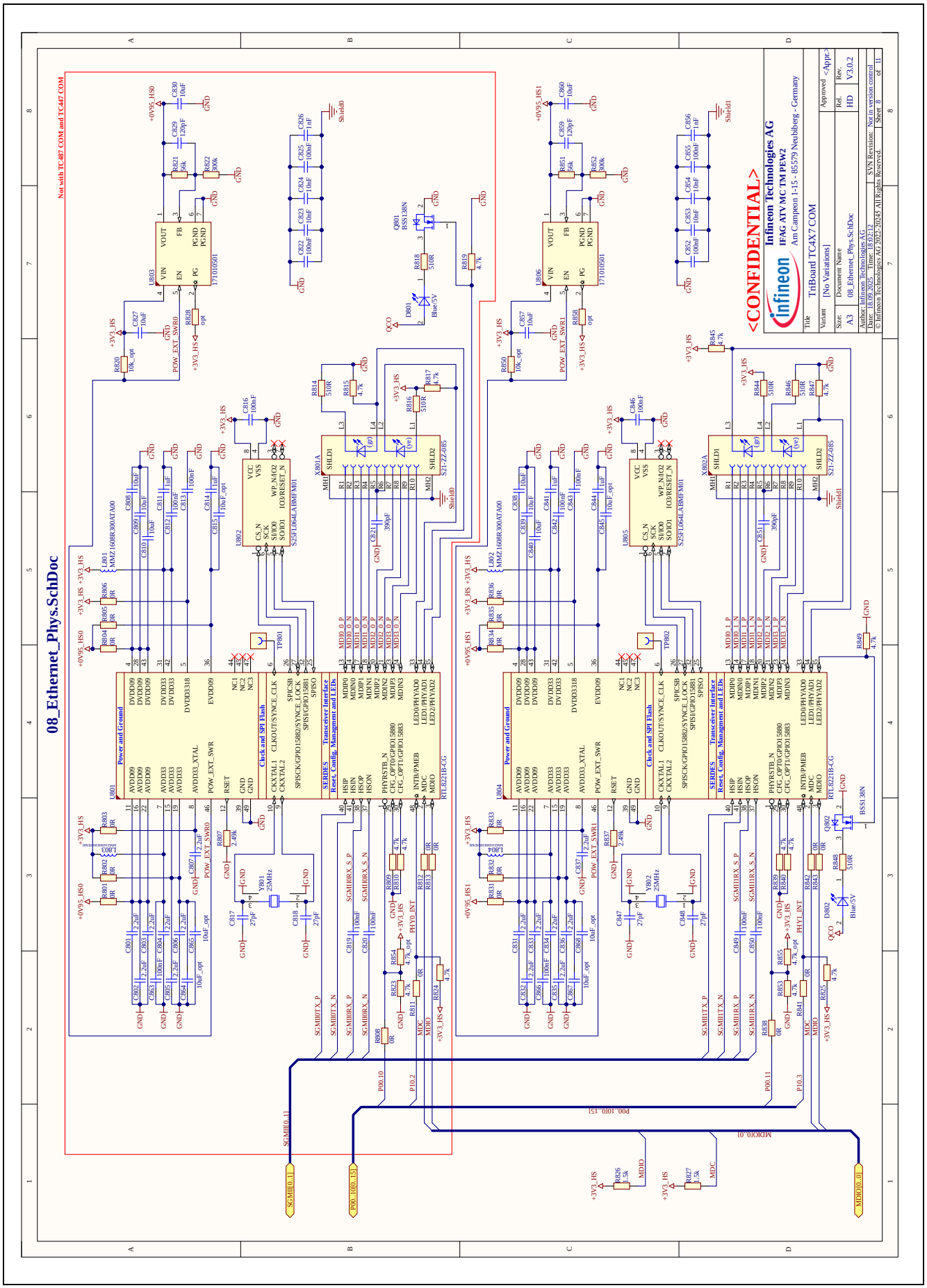


Figure 40 Schematic: Ethernet PHYs

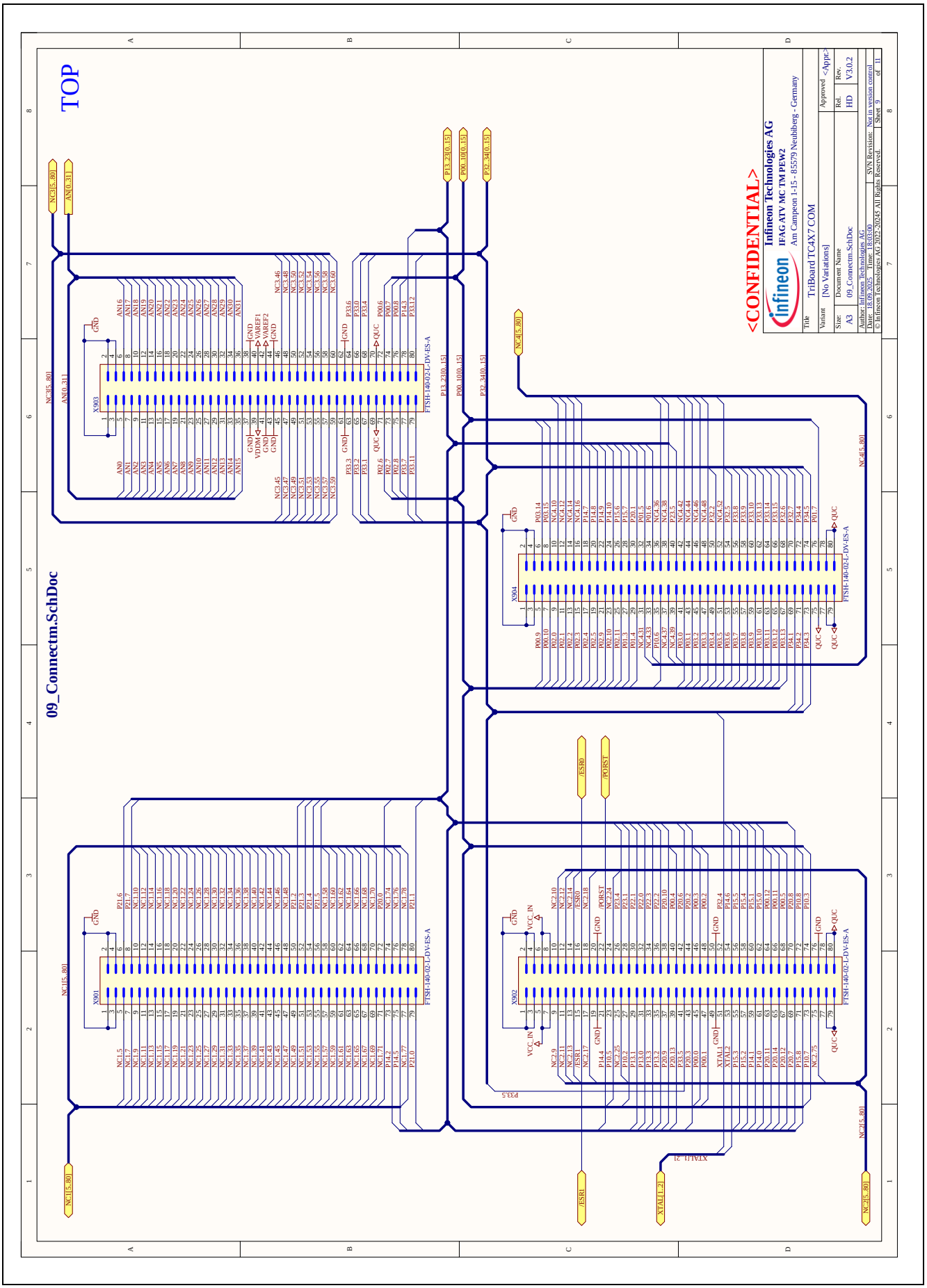


Figure 41 Schematic: Connectors (Plug)

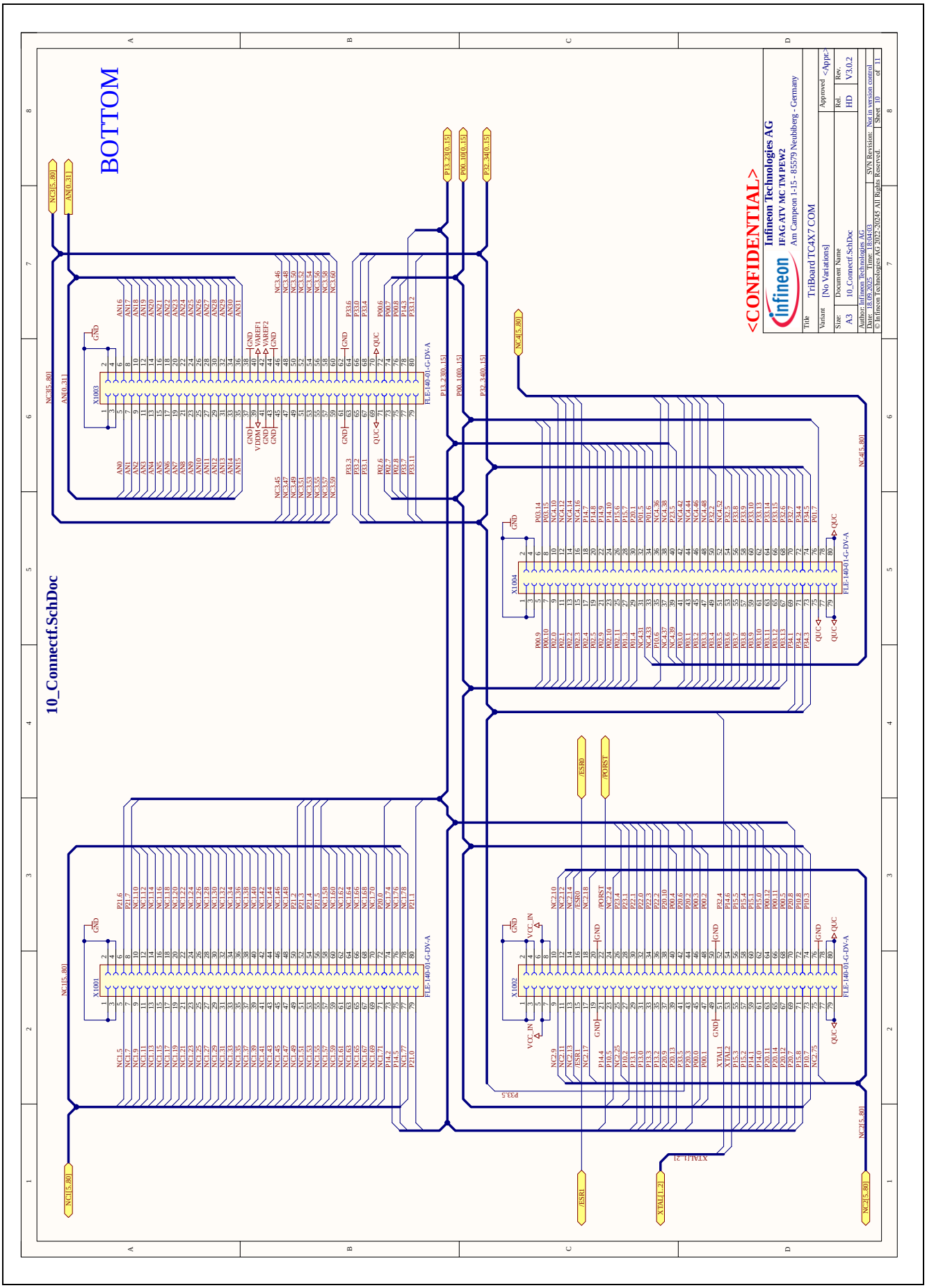


Figure 42 Schematic: Connectors (Socket)

5.3 Assembly

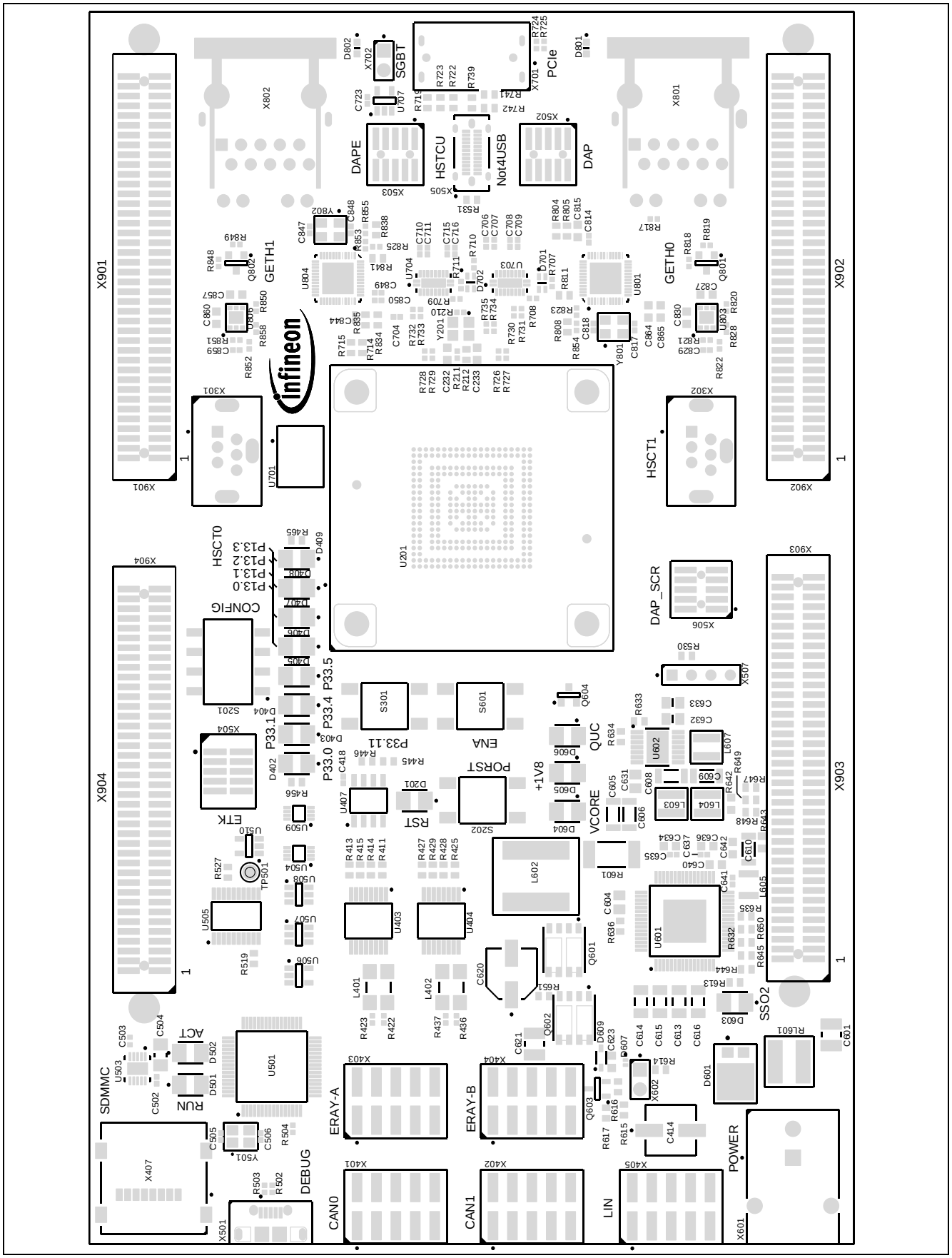


Figure 43 Assembly: Top View

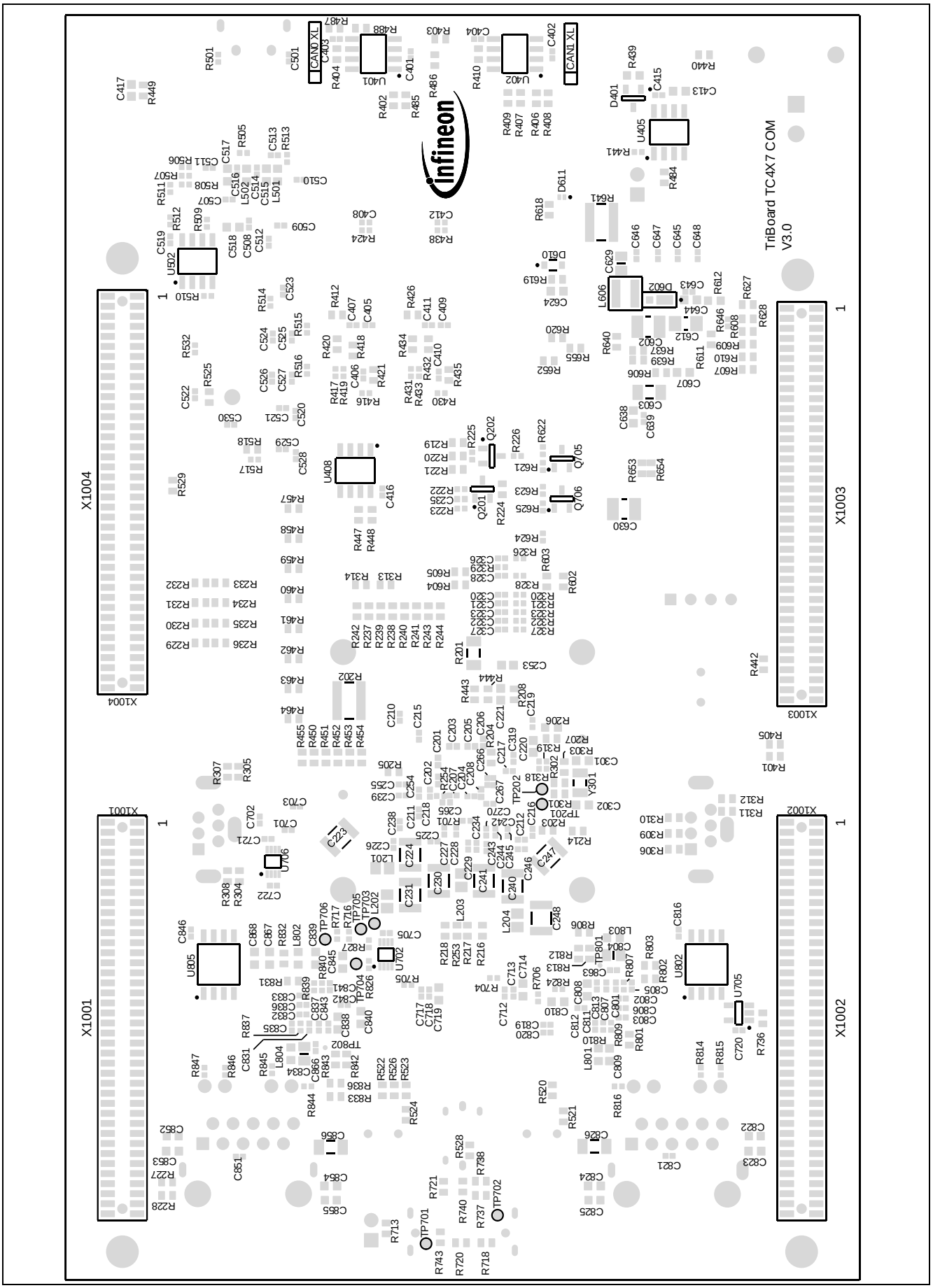


Figure 44 Assembly: Bottom View

5.4 Dimensioning

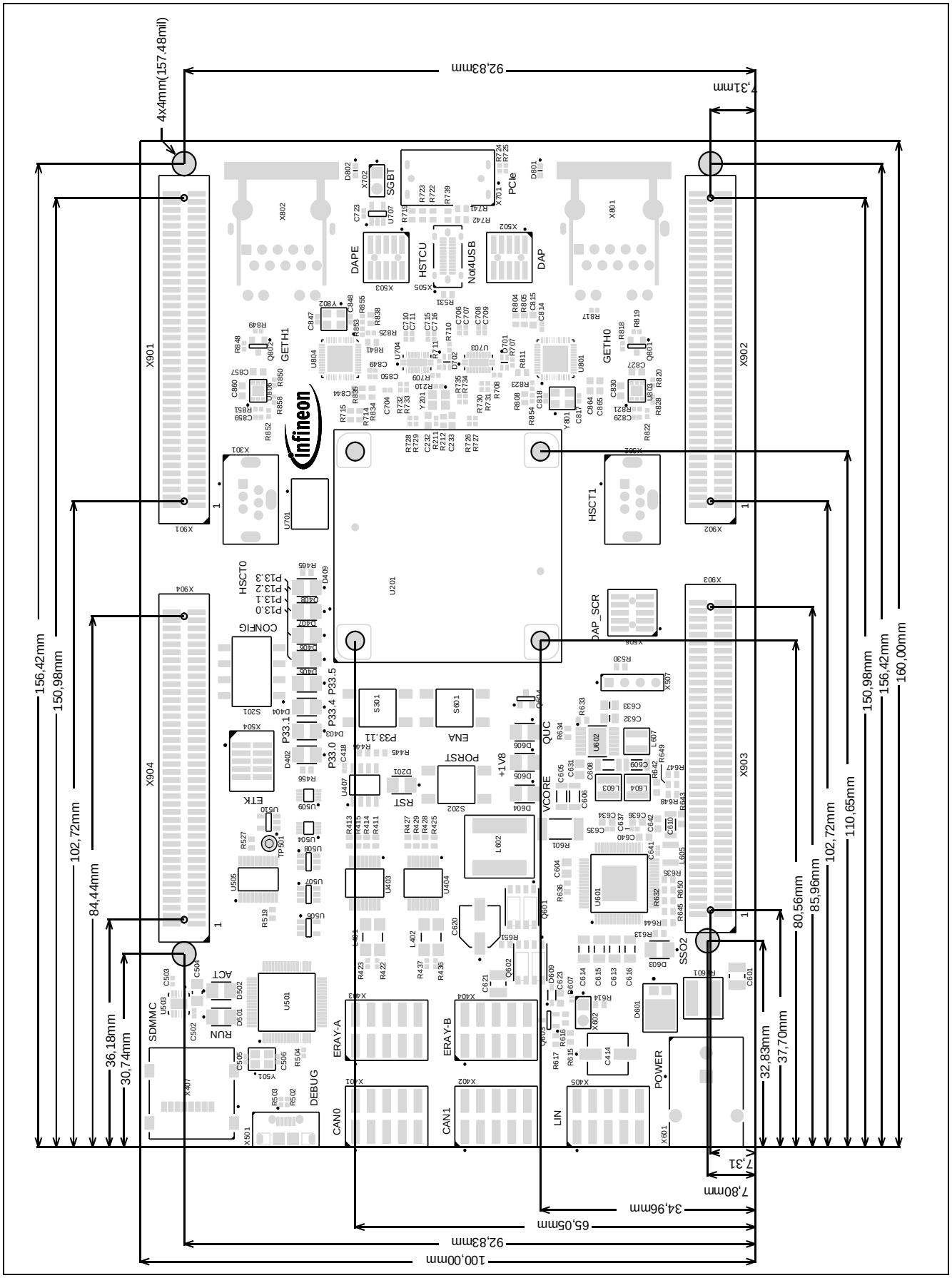


Figure 45 Dimensioning (mm)

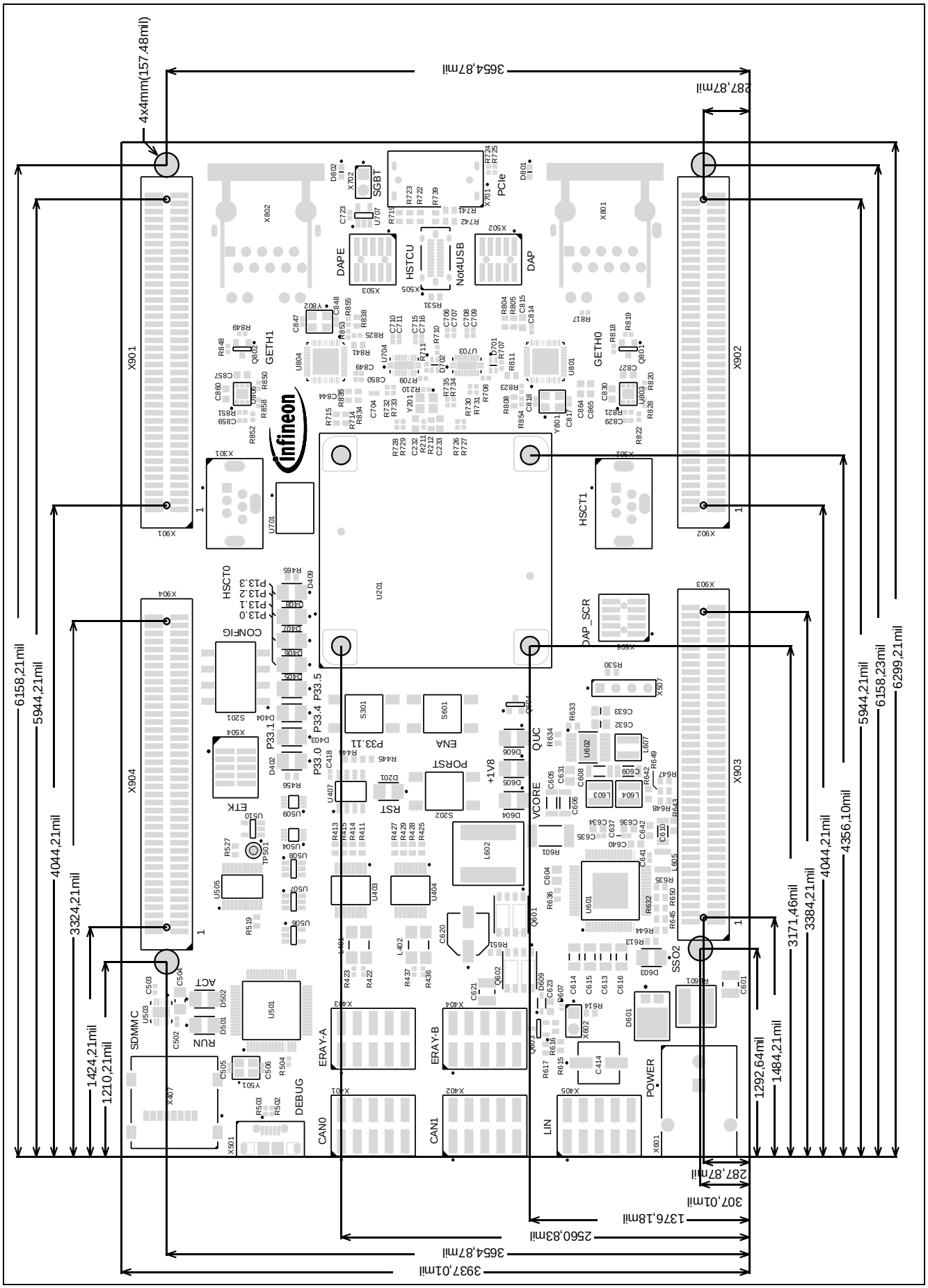


Figure 46 Dimensioning (mil)

6 Revision history

Document version	Date of release	Description of changes
V3.0	2025-01-07	Initial version for Hardware TriBoard TC4X7 COM V3.0
V3.0.1	2025-09-18	“planned, not yet tested, all information’s are preliminary” removed for TC487 Update schematic to V3.0.2 (footprint change of U503 and comment changed for SDMMC) FreeEntryToolchain removed in Introduction Note for DAPE updated Boot via HWCFG pins (defeatured for all TC4xx except TC4Dx) removed, separate table for TC4D7 added and adaptations in Table 24 “not with TC487 COM” removed from chapter 2.12 Micro SD card slot
V3.0.2	2025-12-12	“planned, not yet tested, all information’s are preliminary” removed for TC4Z7 Add description for changed VDDP3NVMx connection

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