# TLD7002-16ES hardware design guideline

## LITIX™ Pixel rear

Z8F80767398

## About this document

### Scope and purpose

This application note is intended to provide guidance on how to design schematic and *printed circuit board (PCB)* for a *light-emitting diode (LED)* driver unit based on the LITIX™ Pixel Rear TLD7002-16ES smart LED driver with *high-speed lighting interface (HSLI)* (*universal asynchronous receiver transmitter (UART)* over *controller area network (CAN)*) interface.

### Intended audience

The intended audiences for this document are hardware design engineers.

# Table of contents

**About this document** . . . 1
**Table of contents** . . . 2
**1 TLD7002-16ES hardware design guideline** . . . 3
**2 TLD7002-16ES external component selection** . . . 5
2.1 Reverse polarity protection (1) . . . 5
2.2 DC-DC input filter (2) . . . 5
2.3 VS capacitor, diode, and optional PI-filter (3) . . . 5
2.4 VDD capacitor (4) . . . 6
2.5 VLED and RVLED resistor (5) (16) . . . 7
2.6 COUTx and CVLED capacitors (6) . . . 8
2.7 GPIN0 NTC resistor divider (8) . . . 10
2.8 Unused OUT pins (9) . . . 10
2.9 GPINx as direct drive with 12V activation (10) . . . 10
2.10 GPIN binning resistors and unused GPINx (14)(15) . . . 11
2.11 HSLI related components . . . 12
2.11.1 HSLI Termination (12) . . . 13
2.11.2 HSLI filter capacitors (11) . . . 14
2.11.3 HSLI TVS diodes for ESD protection (13) . . . 14
2.11.4 HSLI TVS ferrite bead and common mode chokes . . . 15
2.11.5 DC-DC headroom control components (17) . . . 15
**3 ESD protection, general tips** . . . 18
**References** . . . 19
**Glossary** . . . 20
**Revision history** . . . 22
**Disclaimer** . . . 23

# 1 TLD7002-16ES hardware design guideline

The TLD7002-16ES is a 16-channel *LED* driver featuring integrated output stages with output current up to 76 mA as *linear current sink (LCS)*. A *HSLI* (up to 2 MBit/s) is used for control and diagnostic feedback. The device integrates a 40 MHz logic core in order to perform complex and flexible diagnostic operations.

In the following, some tips are provided for the external component selection to minimize the *electromagnetic compatibility (EMC)* emissions and improve design robustness.

The TLD7002-16ES external components are grouped in the figure below inside a blue bubble for functionality. Each group of external component is explained in detail in the following section.

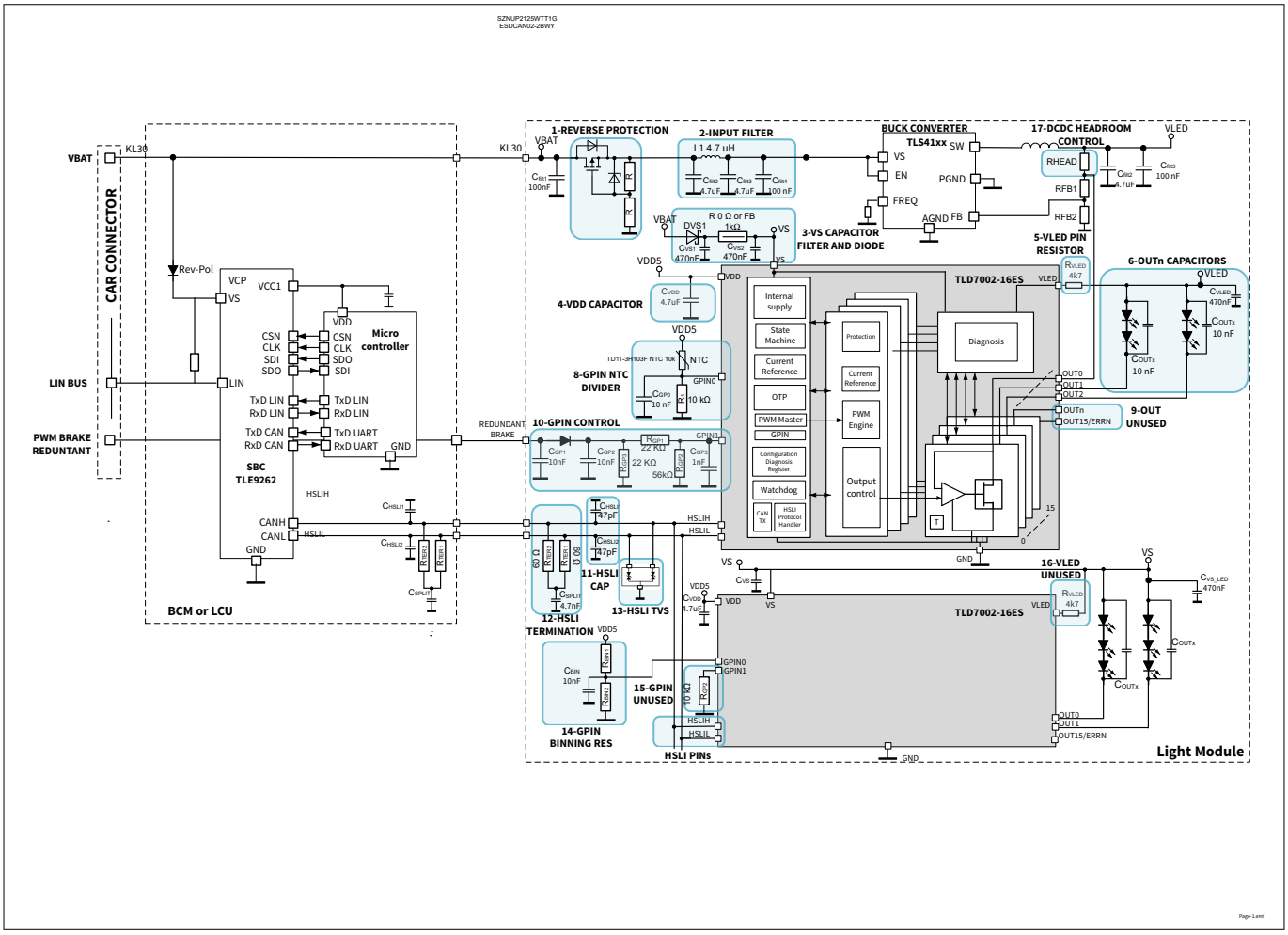



**Figure 1 LED driver unit (LDU) based on TLD7002-16ES schematic**

Here is a short summary of the TLD7002-16ES external components:

- $C_{VSmin}$ = 100 nF (X7R) typical value is $C_{VStyp}$ = 470 nF
- 4.7 µF ≤ $C_{VDD}$ ≤ 13 µF (X7R) typical value is $C_{VDDtyp}$ = 4.7 µF
- $C_{VLEDtyp}$ = 470 nF (X7R)
- $C_{OUTtyp}$ =10nF (X7R)
- 2 kΩ ≤ $R_{VLEDtyp}$ ≤ 5 kΩ connected between VLED pin and $C_{VLED}$
- 2 kΩ ≤ $R_{GPINx}$ ≤ 5 kΩ

Unused pin shall be connected as recommended

- Unused output pins (OUTn) shall be left open or connected to *ground (GND)* through 100 kΩ resistor
- Unused HSLI pins shall be left open

## 1 TLD7002-16ES hardware design guideline

- Unused GPINn pins shall be connected to GND via a resistor higher than 10 kΩ
- Unused VLED pin shall be connected to VS through 2 kΩ ≤ $R_{VLEDtyp}$ ≤ 5 kΩ

Details for each component are provided in the following pages.

# 2 TLD7002-16ES external component selection

## 2.1 Reverse polarity protection (1)

The TLD7002-16ES does not have internal protection for reverse battery at *voltage supply (VS)*, VLED and at the outputs pins, therefore external reverse protection is needed in order to prevent negative voltages at those pins.

MOSFET reverse polarity protection is providing better thermal performance especially when high current is present on the LDU (LED Driver Unit). A Schottky diode is often used as reverse polarity protection for modules where the *LED* current is low (e.g. < 2 A).

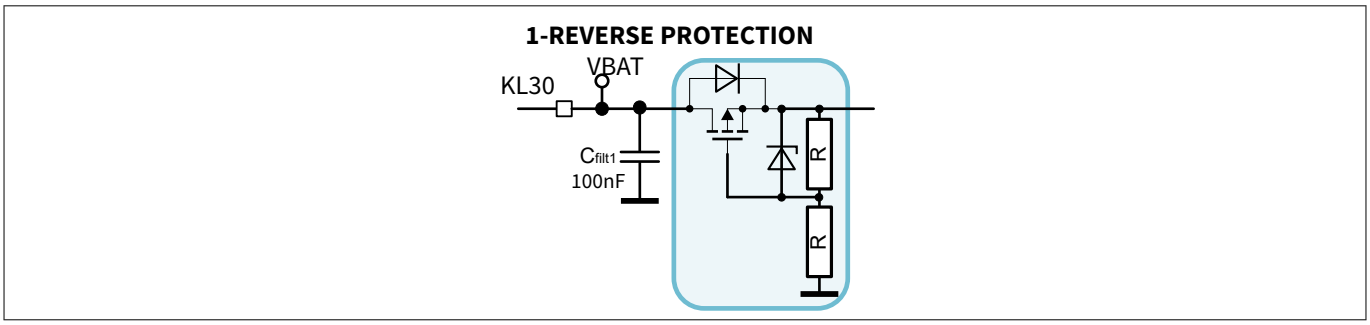



**Figure 2 Reverse battery protection for high current loads**

## 2.2 DC-DC input filter (2)

In case a *direct current to direct current (DC-DC)* converter (typically a Buck or a SEPIC converter) is present in the LDU as pre-regulator, then a PI-filter with a shielded inductor is often needed at the supply line to reduce conducted emission generated by the DC-DC switching activity. In case of SEPIC converters also an additional PI-filter at the DC-DC converter output could be needed due to the intermittent current for this topology.

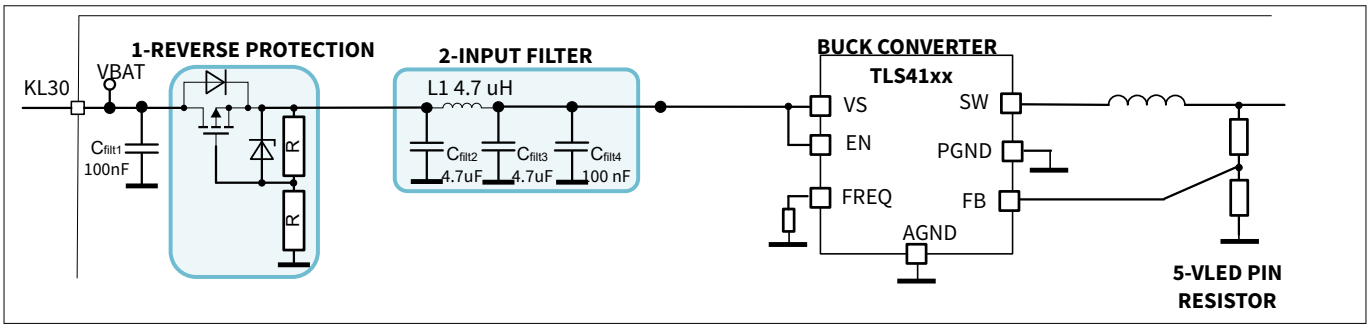



**Figure 3 Input Filter in case of DC-DC converter pre-regulator present on the LED driver PCB**

## 2.3 VS capacitor, diode, and optional PI-filter (3)

The TLD7002-16ES datasheet [1] requires a 100 nF min. to 470 nF typ. capacitor at the *VS* pin (PRQ-374).

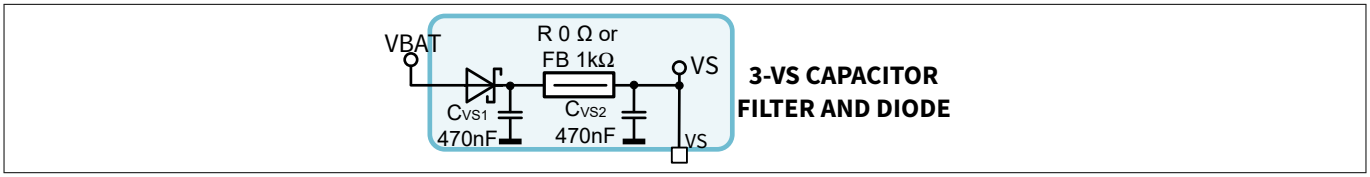



**Figure 4 VS pin input filter and diode**

A diode from the battery voltage to the VS pin is needed for standalone applications (without HSLI), in order to prevent the supply voltage drops to generate spurious IREF(internal reference voltage) warnings. Such IREF

warning in standalone applications may lead the device to remain in INIT mode, without emitting output currents. In addition, the diode before the VS pin and a capacitor at the VS pin in the range of 10 µF prevents the TLD7002-16ES to shut down during short interruption of the supply voltage. For applications with HSLI interface, the diode on the VS pin is less important because eventual IREF warning due to deep of VS ( between 5.5 V and 3.2V) can easily be cleared with and HWCR HSLI command.

In case the TLD7002-16ES is powered directly from the battery line, it is convenient to leave room for a PI-filter with 2 x 470 nF and 0 Ω resistor which act as a placeholder for a ferrite bead. Usually the ferrite bead is not needed and can be populated with a 0 Ω resistor. This resistor can later be swapped for a ferrite bead during *EMC* measurements if needed.

On the Layout suggestion for VS capacitor with a little loop from pin to pin, *GND* connections should be: Capacitor - GND pin - Cooling pad - other circuits.

The thermal pad is used as the ground star, so the cooling pad is also the central STAR for the GND in the *PCB*.

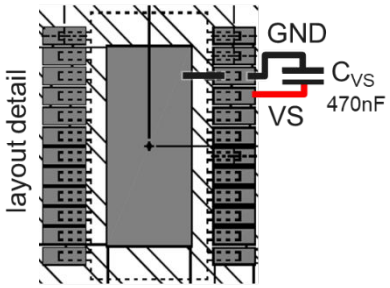



**Figure 5 Layout suggestion for VS capacitor**

With the above proposed solution, the noise coming from VS is sinked by the capacitor and the loop closes at the GND pin, without passing significant noise to the GND plane.

The TLD7002-16ES integrates a 40 MHz logic core therefore high frequency harmonics are present at the VS pin as shown in the TLD7002-16ES EMC test report. Those emissions are not a problem for the EMC qualification if small attentions are paid in the PCB layout. TLD7002-16ES EMC report is available on request.

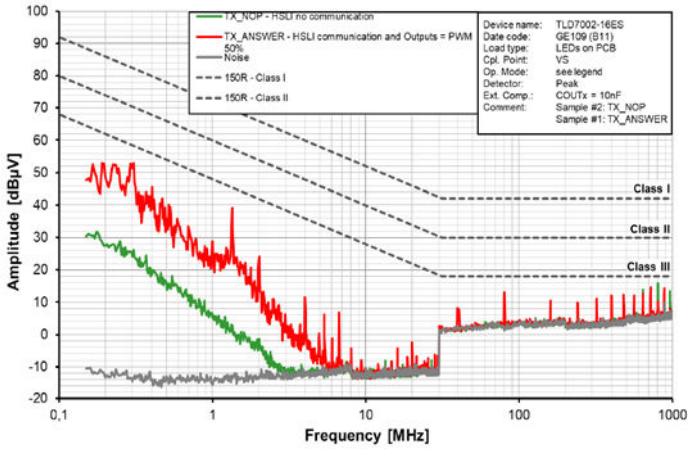



**Figure 6 TLD7002-16ES EMC test report, V1.0: RF emission from pin VS, 150Ω direct coupling method**

## 2.4 VDD capacitor (4)

The TLD7002-16ES datasheet [1] requires a 4.7 uF minimum to 13 uF maximum capacitor at the VDD pin (PRQ-375).

The possible value for the VDD capacitor is actually 1.8 uF minimum to 13 uF maximum.

Considering that:

- DC bias voltage leads to a decrease effective capacitance
  - low size cases has higher capacitance drops
  - higher % applied voltage toward the capacitor rated value leads to higher losses
- Temperature impact on capacitance for X7R materials
- Tolerance on the absolute capacitance value (for example 10%)

Then a 2.2 uF X7R 0805 10V could fit the VDD capacitor in case all the mentioned variations for the specific capacitor are still keeping the residual capacitance above 1.8uF.

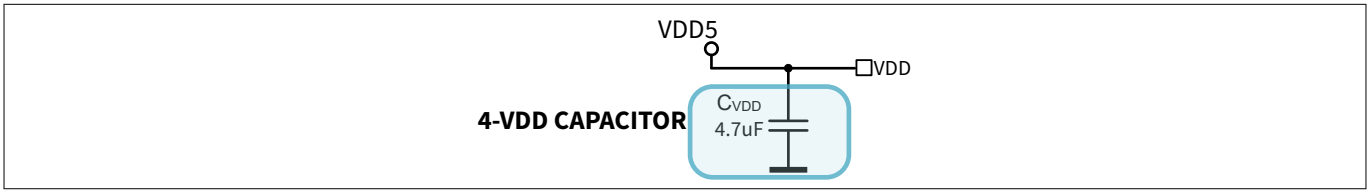



**Figure 7 VDD capacitor**

## 2.5 VLED and RVLED resistor (5) (16)

According to the TLD7002-16ES safety manual application assumption SA_03, a 2 kΩ to 5 kΩ resistor is required to limit the current on the PINs in case of short between GPIN1 and VLED. A 4.7 kΩ resistor is a typical choice for this component. This resistor is not mandatory for applications without ASIL requirements.

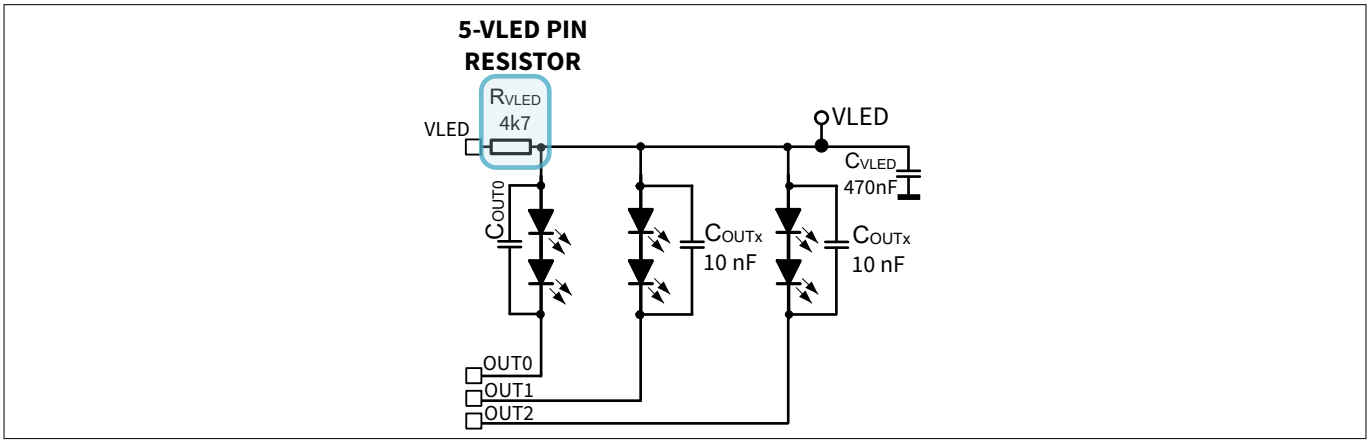



**Figure 8 VLED resistor**

Unused VLED pin shall be connected to *VS* through the previously mentioned resistor as shown in the picture below, otherwise a VS_VLED_UV undervoltage flag is produced.

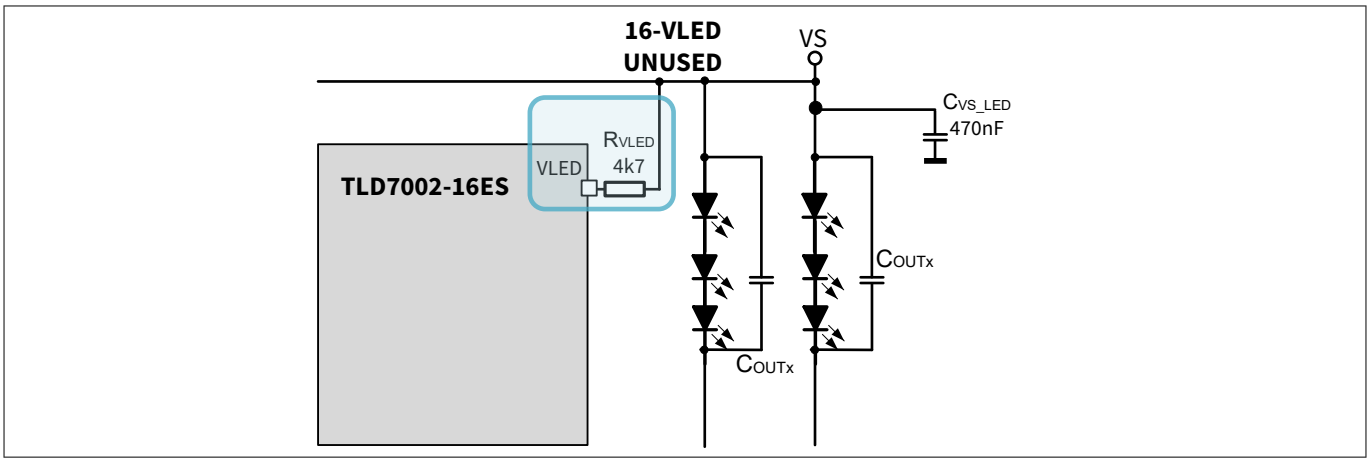



**Figure 9 Unused VLED pin**

## 2.6 COUTx and CVLED capacitors (6)

The TLD7002-16ES is a low-side current source; the datasheet [1] states that its output stages are stable even without a capacitor connected to them. A 10 nF COUT capacitor is usually used in parallel to the *LED* string to:

- Reduce *EMC* emissions
- Improve EMC robustness to injected noises
- Improve ESD robustness
- Improve effectiveness of the Short to adjacent pin feature (recommended in the TLD7002-16ES safety manual [2])

As shown on the figure below, the TLD7002-16ES output capacitors have to be placed so from OUTx net to VLED (or *VS*) net, and not from the output to *GND*.

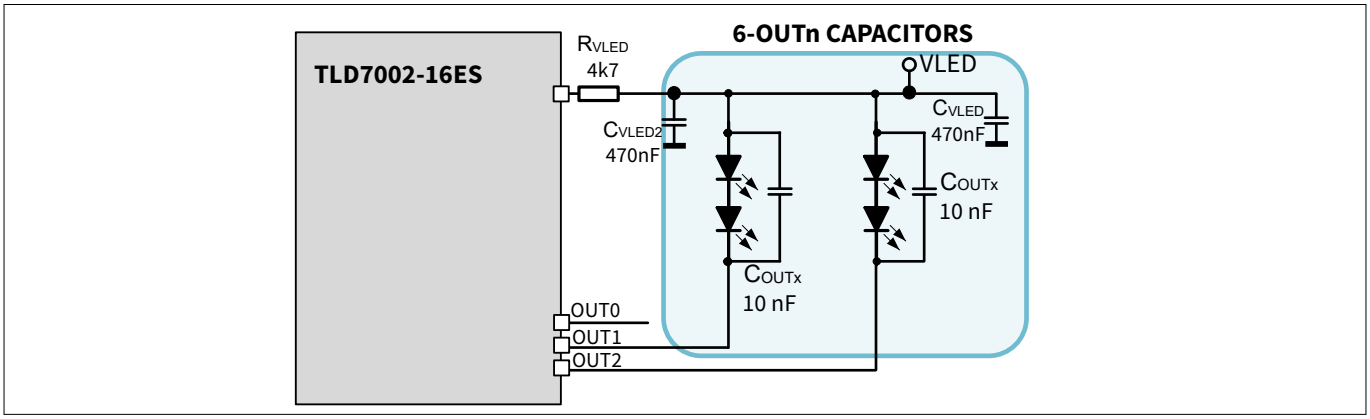



**Figure 10 $C_{OUTX}$ and $C_{VLED}$ capacitors**

The outputs of the TLD7002-16ES are often connected to large copper areas on the *PCB* for LEDs, which can act as a conduit for *electrostatic discharge (ESD)*. To improve ESD robustness and EMC performances 10 nF - 47 nF capacitors are often placed from the OUTx pin to VLED pins.

One or more capacitors from VLED to GND are needed to provide a low impedance path for the COUT capacitances, from the OUT pins to GND.

The VLED pin itself is only an ADC sensing pin. It would not need a capacitance from the TLD7002-16ES functioning point of view, and it is in fact decoupled with a 2k to 5k ohm resistor.

However, in most designs with the TLD7002-16ES, the VLED capacitances are placed to stabilize the DC-DC pre-regulator when present (e.g. 4.7 uF and 100 nF Cfilt2 and Cfilt3) and then some other VLED capacitances are placed close to the LEDs to improve EMC performances. On designs where the LEDs are distributed in large areas, 2 VLED capacitors (e.g. 2x470 nF) are placed at the sides of the LEDs to provide a lower impedance path for the COUT to GND and improve the EMC performances. In some cases, CVLED and COUT capacitances are placed close to the TLD7002-16ES instead of the LEDs.

Output capacitors can be placed close to the TLD7002-16ES OUT pin or close to the LEDs or even in both positions.

$C_{OUT_GND}$ capacitors: seldom used on the TLD7002-16ES designs, also a small capacitor (smaller than the one placed from VLED to OUTx, for instance 1 nF) is placed from the output to ground, in order to reduce even further EMC emissions. This capacitor must be small because in case of VLED transients, it would produce a current pulse on the connected LED string.

$R_{OUTX}$ pull up resistor: a resistor in parallel to the LED strings is recommended to increase the OUT_SHORT_WRN diagnostic coverage. According to the safety manual [2], the resistor has to be placed on OUTn and OUTn-1, the outputs where Short to adjacent pin feature is enabled. This resistor is important especially for small LED strings (1-2 LEDs in series). If the Short to adjacent features is not used, then the resistor in parallel to the LED string is not needed.

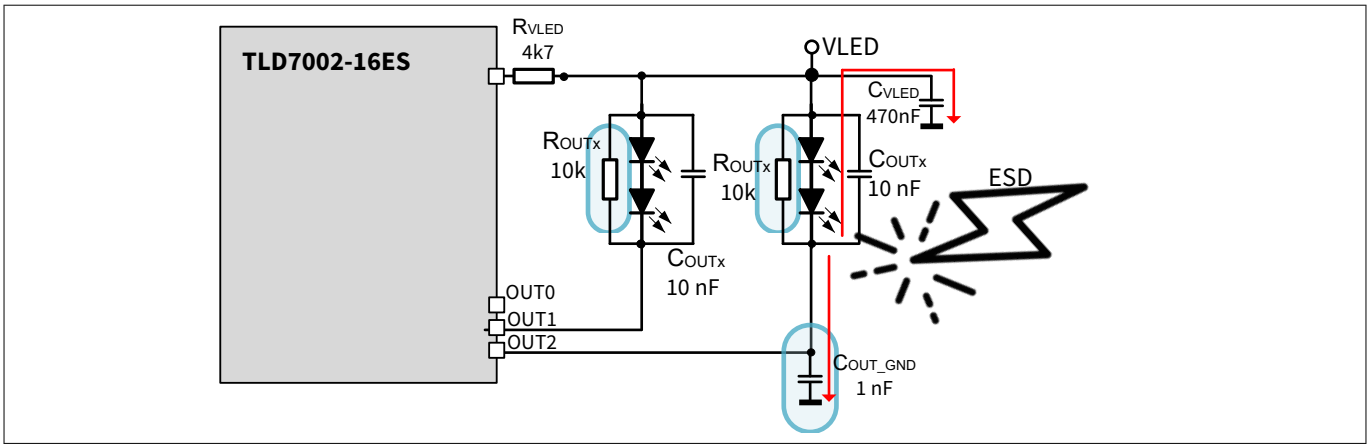



**Figure 11 Output Resistor and output capacitor to ground**

Seldom used small capacitors (e.g. 1 nF) from the output to GND are placed to improve the ESD robustness even further, and reduce EMC emissions.

***Note**: Output capacitors may introduce delays on the output voltage waveforms, impacting the diagnostic timings. In addition, a resistor in parallel to the* LED *will discharging the COUTx capacitance when pulse-width modulation (PWM) is off. This will further increase the before mentioned delay on the voltage waveforms. The delay introduced by the COUTx is bigger when the output current is set to low values (e.g. 20 mA).*

In order to perform diagnostic, the OUTx voltage is sampled by the TLD7002-16ES at Tdiag_DLY from the PWM start. Therefore, you must ensure that the output voltage in case of fault, is able to exceed the diagnostic thresholds. For instance, in the circuit below a circuit where a 22 nF capacitor connected from OUTx to VLED, in conjunction with a resistor in parallel to the LED and a high VLED voltage (e.g. 15 V). If an open load is present on the OUTx, it will produce the waveform shown in the picture below, where the OUTx ramps to 0 V slowly discharging the OUTx capacitance, and it is not able to reach the Open Load thresholds, preventing the TLD7002-16ES to detect the fault.

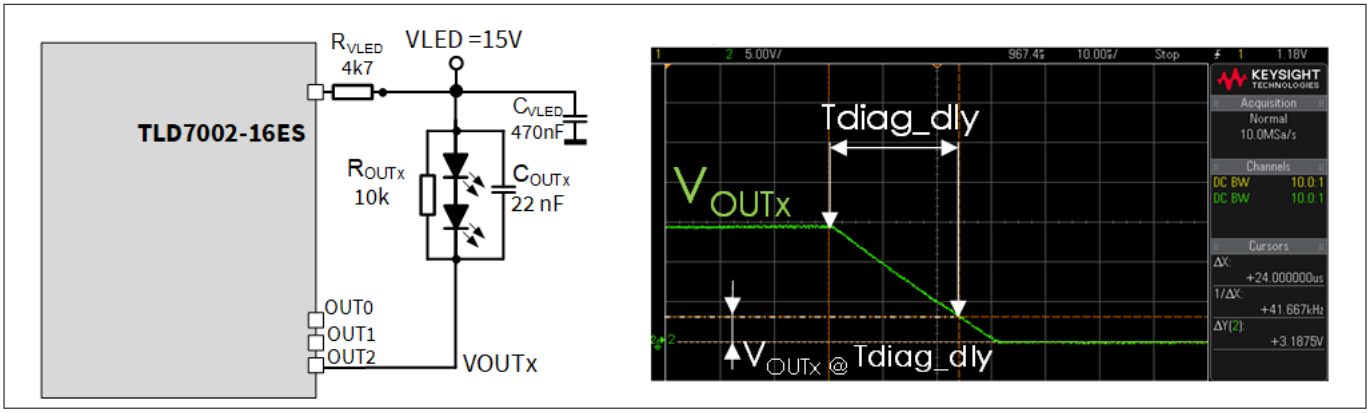



**Figure 12 Large $C_{OUTX}$ and $R_{OUTX}$ preventing open load detection with brief Tdiag_dly**

***Note**: With a Tdiag_DLY set to 24 us would be impossible to detect the open load, because the OUTx voltage is still above the open load threshold (400 mV typ) at 24 us from the* PWM *start. Tdiag_DLY has to be chosen in order to sample the output voltage when the waveforms are stable (on this example could be set to Tdiag_DLY = 48 us). Another solution could be to reduce the output capacitor to 10 nF making the waveform stable earlier.*

## 2.7 GPIN0 NTC resistor divider (8)

It is possible to connect a resistor divider with NTC to the GPINx of the TLD7002-16ES to calculate the temperature by reading back the GPINx voltage. If the NTC is connected to the GPIN0, and on the upper side of the voltage divider as shown in the picture below, it is also possible to implement configurable derating through GPIN0 (see TLD7002-16ES DS chapter 6.8.2).In alternative, it is possible to read back the NTC temperature with the TLD7002-16ES by using the GPIN0 as analog input (see TLD7002-16ES DS chapter 5.5). A 10 nF capacitor is usually connected to the GPINx to reduce the noise at the TLD7002-16ES GPIN0 input.

The TLD7002-16ES OTP has to be configured in order to have the GPIN0 as analog input, and eventually thermal derating has to be properly configured (see TLD7002-16ES OTP parameter settings application note [3]).

***Note**: GPINx are only 5 V tolerant (supply voltage (VDD) as absolute maximum rating).*

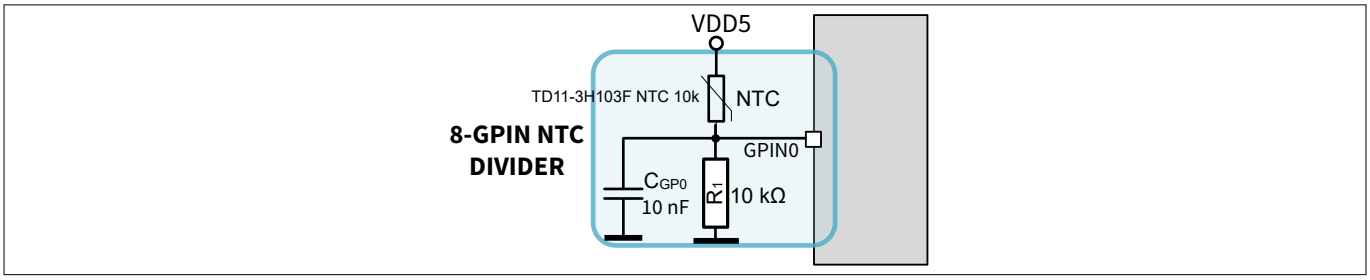



**Figure 13 GPIN0 NTC divider**

## 2.8 Unused OUT pins (9)

As suggested from the TLD7002-16ES datasheet [1], unused output pins (OUTn) shall be left open with duty cycle set to 0 or connected to *GND* via 100 kΩ. A single resistor can be shared for multiple unused outputs.

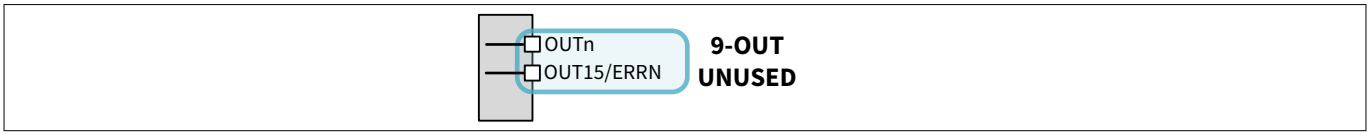



**Figure 14 Unused OUTx pins**

## 2.9 GPINx as direct drive with 12V activation (10)

GPINx can be used as redundant brake activation, controlled by a wire that goes outside the LCU to a 12 V battery line. It is safe to drive the GPIN1 directly by the battery line if the current is kept below the absolute maximum rating (Minimum 0 mA, Maximum 13.75 mA and the sum of current on GPIN0 and GPIN1 is below 20 mA, datasheet [1] PRQ-368). In addition, a reverse polarity protection and capacitors CGP1 and CGP2 for ESD protection are often adopted. An additional capacitor CGP3 in parallel to GPINx will filter eventual glitches.

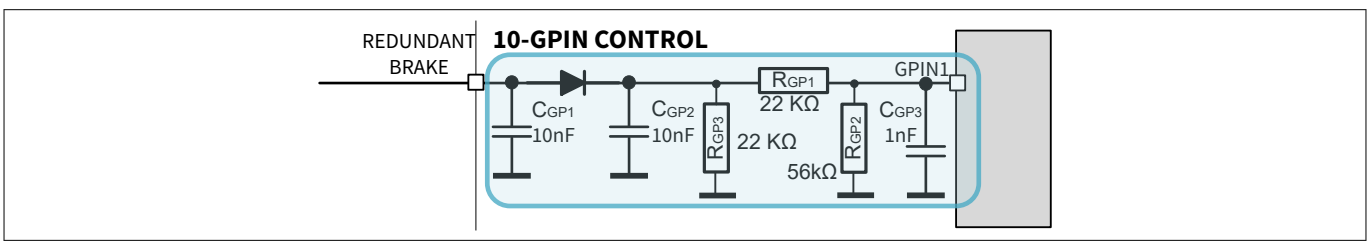



**Figure 15 GPINx used as direct drive with 12V lines**

In some design could be useful to “blank” the GPIN control signal for the TLD7002-16ES watchdog time, in order to blank spurious glitches on the GPINs when the vehicle is started.

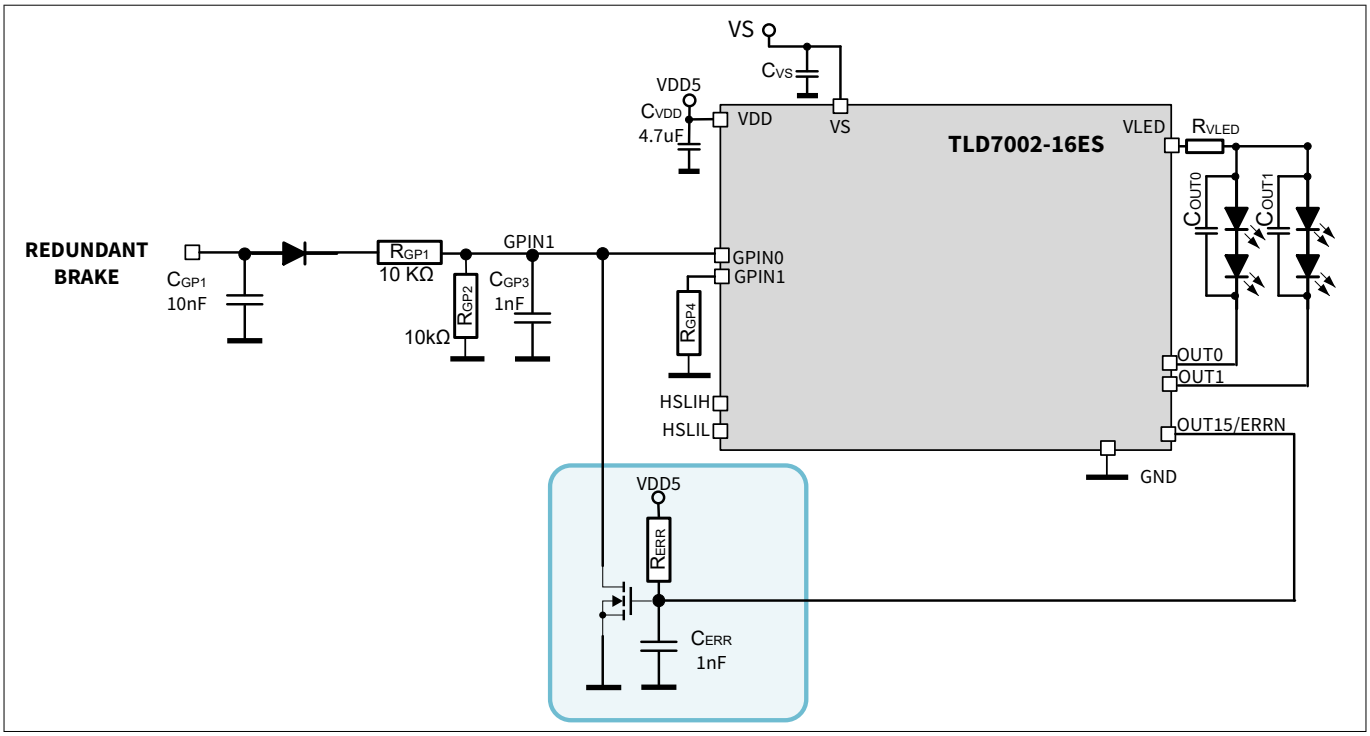



**Figure 16 GPINx direct control with blanking circuitry**

In the table below are shown all the conditions that the system may face during startup and running mode.

**Table 1 Possible operating modes for TLD7002-16ES with blanking circuitry**

| System status | External MOS status | OUT15 status | Stop function status |
|---|---|---|---|
| TLD7002 in off state or in reset mode | x | x | OFF |
| TLD7002 active but not controlled via HSLI and watchdog NOT triggered | ON | OFF | OFF |
| TLD7002 active but not controlled via HSLI and watchdog triggered | OFF | ON (OUT0 Fail safe with 100% duty saved in the OTP) | ON |
| TLD7002 active and controlled via HSLI | ON | OFF | OFF |

## 2.10 GPIN binning resistors and unused GPINx (14)(15)

TLD7002-16ES GPINs are often used to readback a BIN resistor value, by placing it on a resistor divider as shown in the picture below. A 10 nF capacitor is used to reduce the noise on the ADC conversion.

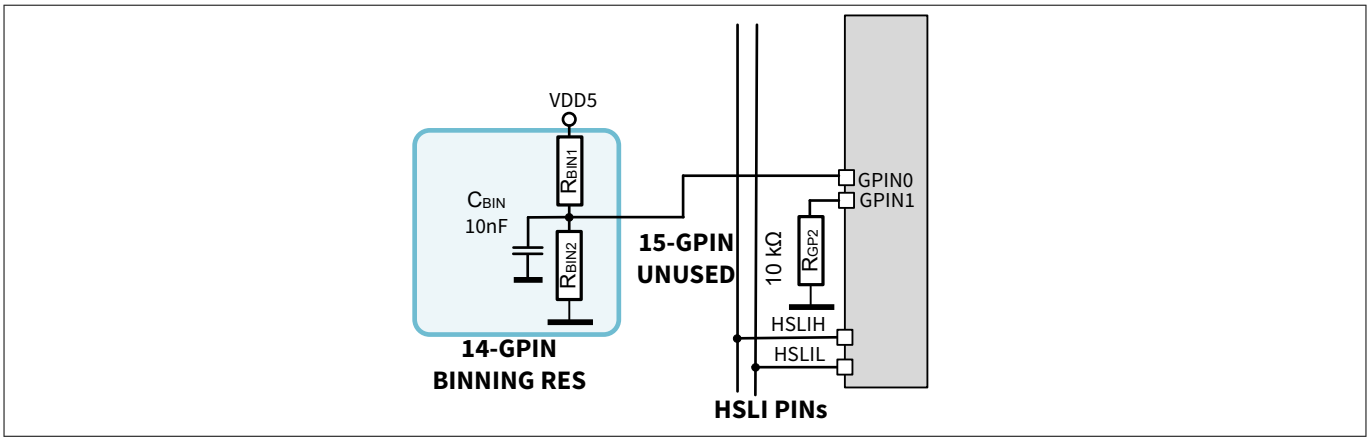



**Figure 17 GPIN0 binning resistor**

As suggested from the TLD7002-16ES datasheet [1], unused GPINx pins shall be connected to *GND* via a resistor higher than 10 kΩ. If left floating, coupled disturbance can rise it above the threshold setting the device in active mode. If the GPINx is connected directly to ground, in case of ground loss from the *integrated circuit (IC)*, the IC risk to get damaged because of the ground current from the GPINx to GND.

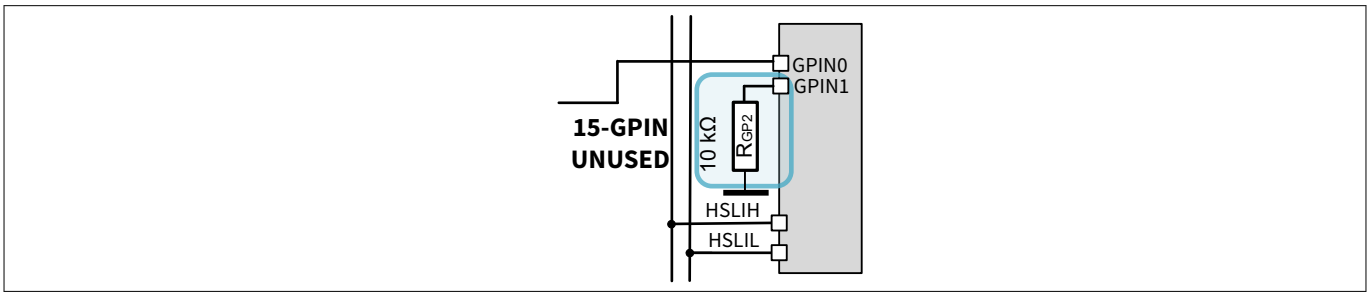



**Figure 18 GPINx unused**

## 2.11 HSLI related components

The *HSLI* interface it is based on a *UART* protocol over CAN-FD physical-layer up to 2 MBit/s.

The TLD7002-16ES integrates a CAN-FD transceiver, the external components for the TLD7002-16ES HSLI pins are similar to any other CAN-FD application, with the exceptions that there could be many transceiver (because of many TLD7002-16ES) in the same *PCB*. In the following chapters each HSLI pin external component is described.

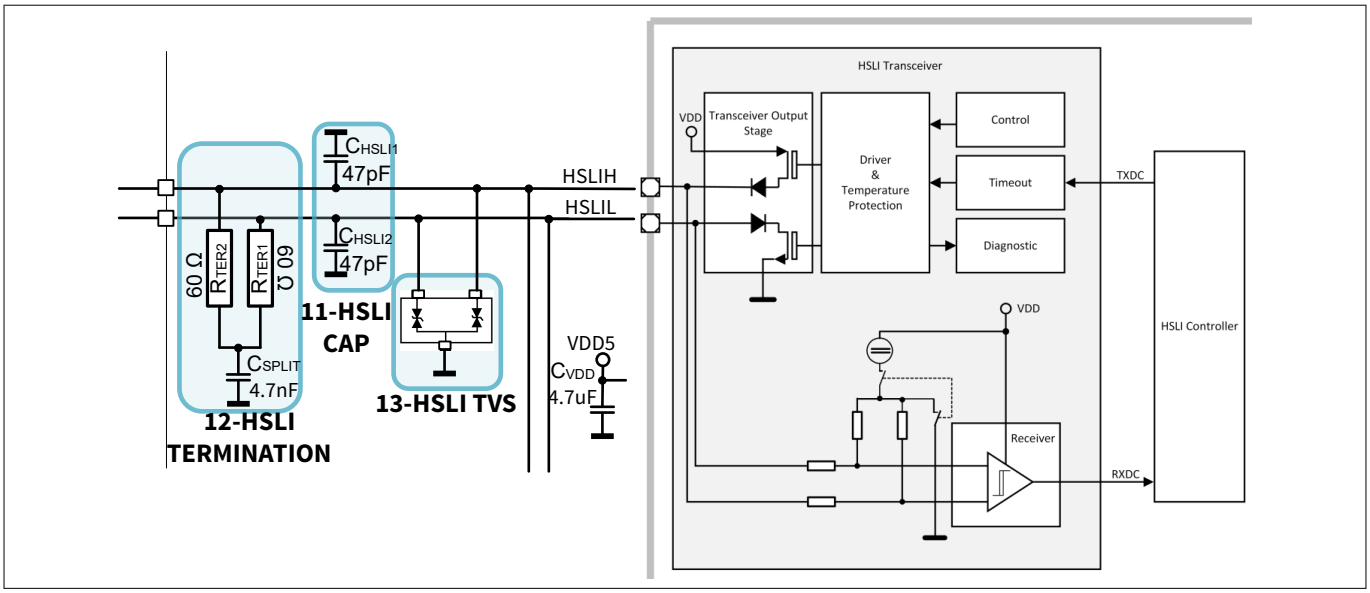



**Figure 19 HSLI related components**

## 2.11.1 HSLI Termination (12)

Termination shall be mounted only the 2 most distant *CAN* bus modules only. There are 2 types of termination resistors split termination and Standard termination. Split termination (2 x 60 Ω with central C split 4.7 nF) has better performance than standard termination.

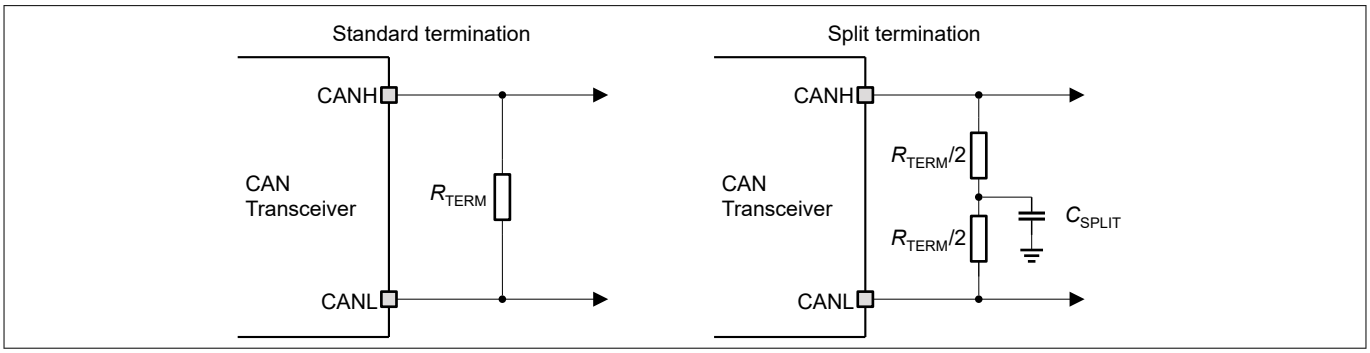



**Figure 20 HSLI termination resistors (preferred is Split termination)**

Termination shall be mounted only once per node (for example once per *PCB*), and not 1 per TLD7002-16ES device.

In case more than one receiver node (module/PCB) is connected to the same *HSLI* bus, some OEMs require secondary termination to be mounted on remaining HSLI nodes. Also, secondary termination resistors are mounted one per node (for example PCB), and not 1 per TLD7002-16ES device. Secondary terminations are identical to primary termination (split termination schematic) but they use 4.7 kΩ resistors instead of 60 Ω resistor.

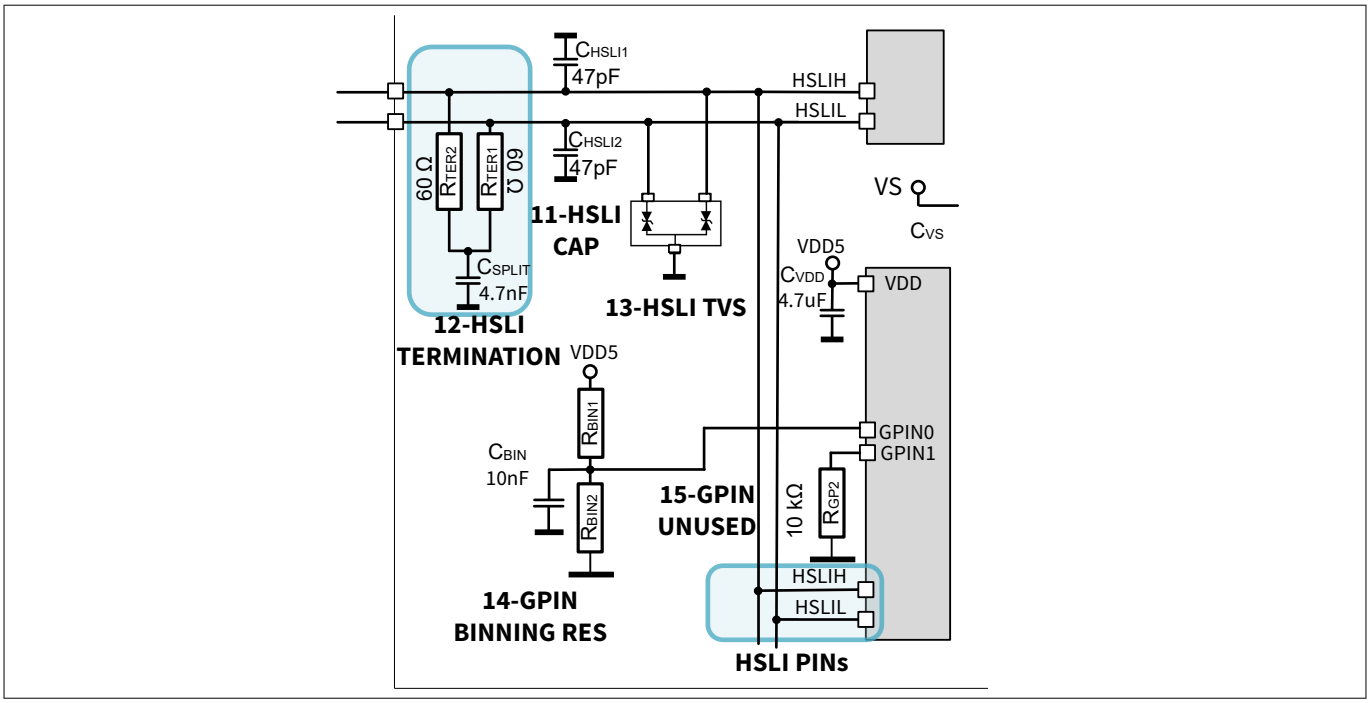



**Figure 21 HSLI termination, only one module, only on the 2 most distant modules in the BUS**

## 2.11.2 HSLI filter capacitors (11)

*HSLI* filtering capacitors are placed in parallel to CAN-H and CAN-l lines, they are usually not needed on TLD7002-16ES applications. Today there is no standard requirement for total capacitance of each HSLI(CAN) node. Usually an OEM requirement allow up to 50 pF differential or 100 pF CAN-H/CAN-L to GND, per node, including TLD7002-16ES HSLI pins capacitance, *ESD* protection diode parasitic capacitance, *PCB* traces.

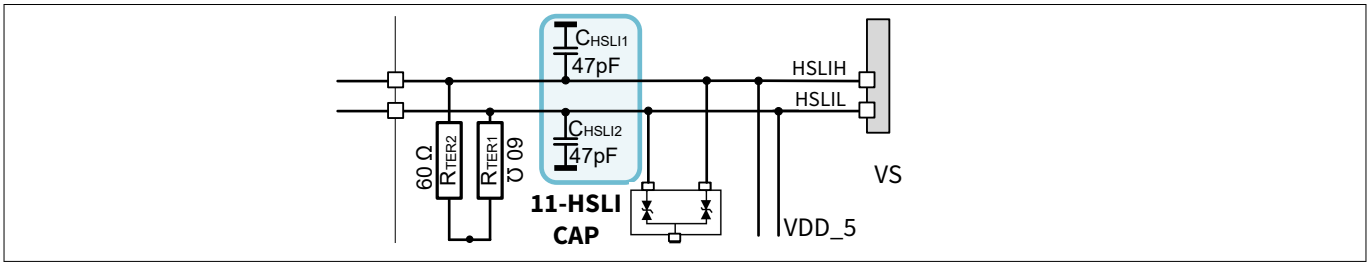



**Figure 22 HSLI filter capacitors**

HSLI filter capacitors are supposed to address *EMC* issues or to suppress *CAN* bus line transients high-frequency noise. In case they are really needed, then use only one HSLI filter capacitor couple per node, close to the HSLI connector, and not one per TLD7002-16ES device. Possible value for the HSLI filter capacitors is 47 pF.

***Note**: High filter capacitors value (E.G. 220 pF) could cause* CAN *wave reflections and ruin the communication.*

## 2.11.3 HSLI TVS diodes for ESD protection (13)

The TLD7002-16ES offers an 8 kV *ESD* susceptibility, *human body model (HBM)*but often *transient voltage suppressor (TVS)* diodes are placed in the LCU module to increase this protection. TVS diodes are placed one per module close to the *HSLI* connector pins.

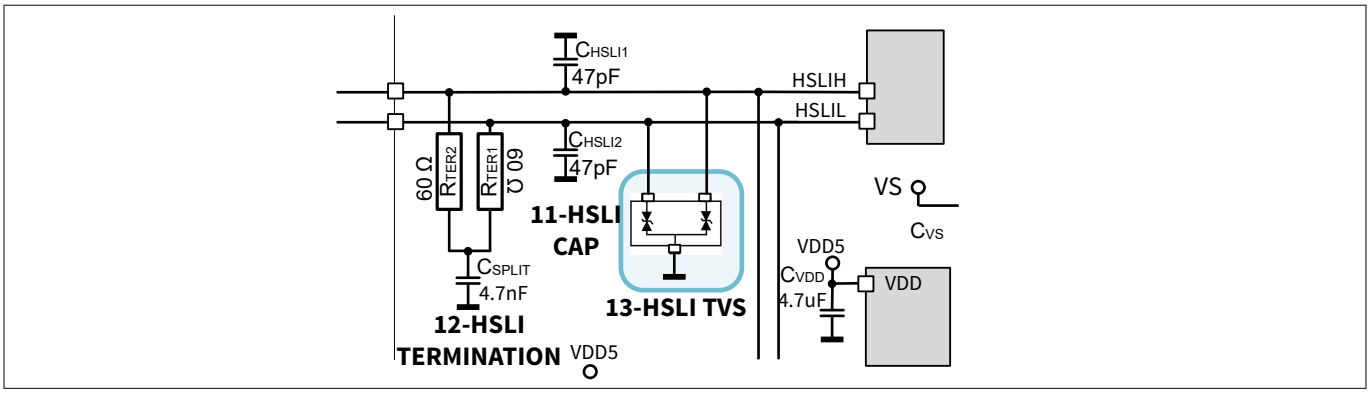



**Figure 23 HSLI TVS diodes for improved ESD protection**

## 2.11.4 HSLI TVS ferrite bead and common mode chokes

On some rare cases ferrite beads (for example 1 kΩ @ 100 MHz) at the *HSLI* pins are used to reduce *EMC* emissions. It is possible to design ferrite bead footprint placeholders close to the HSLI pins, and populate them with 0 Ω resistors on the first prototypes during EMC tests. While on the majority of the design common mode chokes are not needed on the HSLI lines.

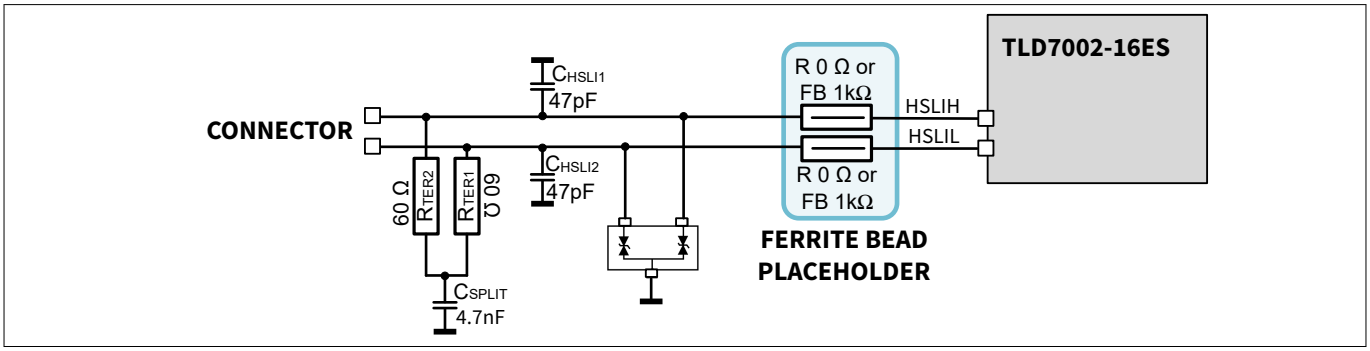



**Figure 24 HSLI ferrite beads**

## 2.11.5 DC-DC headroom control components (17)

The voltage regulator feedback feature (or *DC-DC* headroom control feature), allows the OUT0 to adjust an offset on the output of an external voltage regulator. This is used to implement a voltage head-room control in order to optimize power dissipation on linear *LED* drivers. The feature is described in detail in the User manual chapter 1.11.

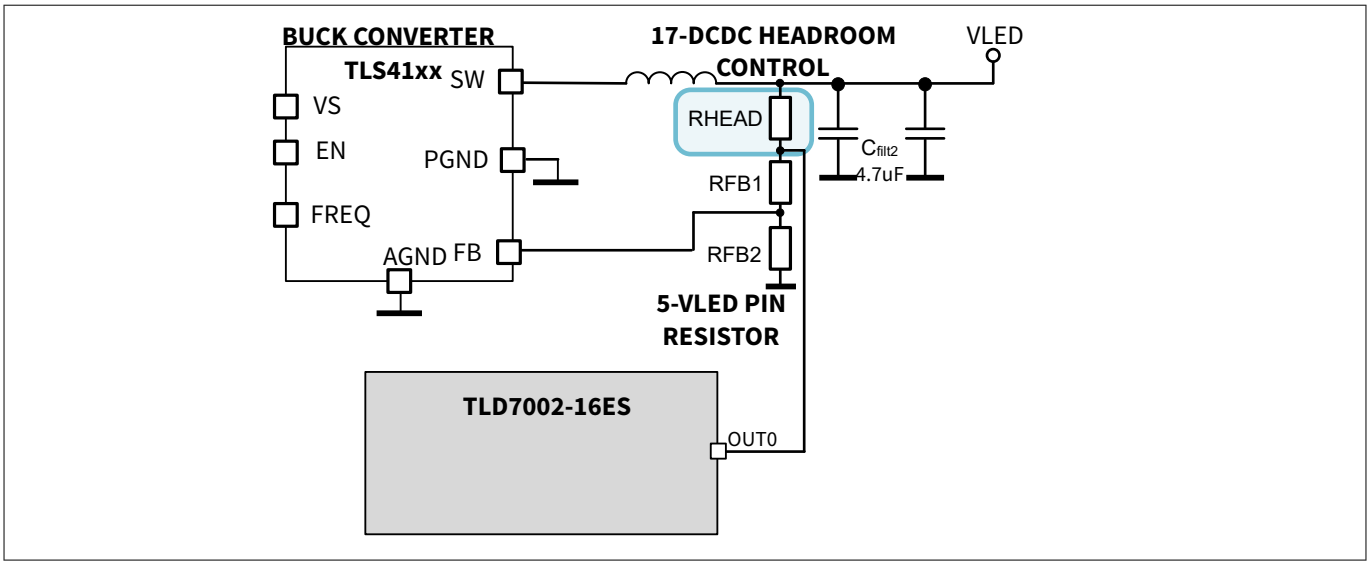



**Figure 25 DC-DC headroom control feature related components**

The DC-DC headroom control works only on output OUT0 of the TLD7002-16ES, because if the feature is enabled on the OTP, several diagnostic warnings are masked only on this output, and VOUTmin is not calculated on OUT0. In order to adjust the output voltage of the DC-DC pre-regulator, the TLD7002-16ES creates an offset on the default DC-DC regulator set point ( $V_{SET}$, defined by RFB1 and RFB2) by pulling a current on the resistor $R_{HEAD}$. Please note, this headroom adjustment it is not automatic, therefore the application has to read the VOUTmin of all the TLD7002-16ES outputs attached to this DC-DC pre-regulator, and adjusts the current on OUT0 to have the sufficient dropout on all the outputs (depends by the LED current), and to avoid the open load conditions in all the outputs (VOUT,OL_th = 500 mV max).

The current steps on OUT0, which are applicable in order to create the offset voltage, are equal to the standard LED driver mode steps (DS table 9). It is suggested to choose an RHEAD in order to keep offset current low and therefore reducing the power dissipation. In the example 50 mA offset current, sinked on a 10V DC-DC converter output would waste 500 mW of power.

**Headroom control dimensioning example:**

Let's dimension a DC-DC headroom control resistors in order to power LED strings (identical on all outputs to simplify the calculations), which are composed by a series of 2 x Osram LS E67B red LED at 50 mA.

Let's suppose that the string voltage for those LEDs, according to their datasheet, would span as show below:

$VFWD_{min(hot)}$ = 3,22 V to $VFWD_{max(cold)}$ = 5,44 V for the series of the 2 LEDs.

The DC-DC converter output voltage, in order to power this type of strings, has to be able to reach at least:

$VLED_{maxCold}$ = VFWD + TLD7002-16ES Vdropout at 50 mA

Considering that the maximum LED forward voltage (VFWD) is cold, then the TLD7002-16ES dropout also has to be considered at cold + self heat of the TLD7002-16ES (For example 65°). Therefore the VLED requirements are voltage generated by the DC-DC pre-regulator has to vary from:

$VLED_{maxCold}$ = $VFWD_{max}$at -40 Ta + VdropMax at 50 mA at (-40°Ta + 65°SelfHeat = 25°) = 5,44 V + 640 mV = 6,08 V

$VLED_{minHot}$ = $VFWD_{min}$ + Vdrop at 50 mA =3,22 V + 0,64 V = 3,86 V

***Note**: Considering the accuracy of the* DC-DC *pre-regulator and, the accuracy on the adjusting current on RHEAD, and also some load regulation margin (*DC-DC *pre-regulator voltage may vary during LED load steps or input voltage transients) it is convenient to set some margin on the* DC-DC *pre-regulation on the top of the required minimum voltages for instance PreRegMargin = 500 mV (depends by application condition).*

Now is possible to calculate the resistors for our DC-DC pre-regulator.

## 2 TLD7002-16ES external component selection

First, select **RFB1** and **RFB2** according to the DC-DC regulator datasheet, in order to have its default output voltage equal to:

VSETdcdc = minimum needed VLED voltage + PreRegMargin = 3,86 V + 500 mV

Where VSETdcdc is the DC-DC output voltage without TLD7002-16ES OUT0 contribution (IOUT0 = 0). Because, on this schematic, by pulling current on IOUT0 the output voltage can only increase.

Second, select **RHEAD** in order to have the needed maximum offset with a headroom control contribute of $IOUT0_{maxOffset}$ = 22 mA. This current level is high enough to have some headroom control granularity but low enough avoid dissipating too much power.

$V_{MaxOffset}$ = $VLED_{maxCold}$ - VSET + PreRegMargin = 6,08 V - 3,86 V +500 mV = 2,72 V

RHEAD = $V_{MaxOffset}/IOUT0_{maxOffset}$ = 2,72 V / 22 mA = 123 Ohm

# 3 ESD protection, general tips

TLD7002-16ES is protected against *ESD* levels as specified in the datasheet [1]: Output pins are protected against ESD up to 2 kV *HBM*. *HSLI* pins are even more robust than other pins because they are supposed to exit the *PCB*, 8 kV ESD susceptibility, HBM.

Infineon tested the TLD7002-16ES for ESD susceptibility. Often test levels are above the specified ones (Example: ESD classification 2 kV Test is executed at 2.5 kV), ESD test reports are available on request.

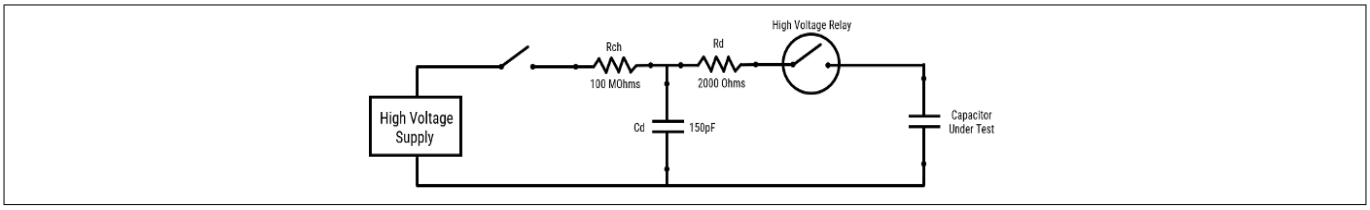



**Figure 26** **ESD *Discharge Network for ESD Testing per AEC-Q200***

***Note**:* *Wrap peeling*

ESD protection is often a concern on automotive *LED* driver units. LEDs are often positioned close to the transparent polycarbonate plastic, which could build up high amount of electrostatic charge due to triboelectric effect, or in the process of protection film/wrap peeling.

LED manufacturing processes are exposed to the ESD hazards during the detachment process of protective film. The peeling process of protective film, when it is being rubbed and separated from the tail-light plastic affects the amount of electrostatic charge generation. Modified surface treatment of a protective film showed significant effect to reduce the failure rate and the maximum friction charge (we do not have further details on this process). Lamp protective film removal (peeling) may cause severe ESD discharge damaging the LED driver unit, lamp failure is observed only after lamp plastic wrap removal (peeling).

***Note**:* *Reflectors*

Metalized reflectors are often placed close to the PCB to adjust the light pattern or help in the thermal management. The reflector could act as an antenna, increasing the ESD discharge coupling to the LEDs. Grounding (connecting) the Reflector to a *GND* potential would improve the ESD robustness. This connection can also impact on *EMC* performance.

***Note**:* *TLD7002-16ES output capacitors*

The TLD7002-16ES is a low side current source, its output stages are stable even without a capacitor connected to it, anyway a capacitor connected to each output toward VLED (or VS) could highly improve ESD robustness by mean of the charge sharing mechanism as shown in the picture below.

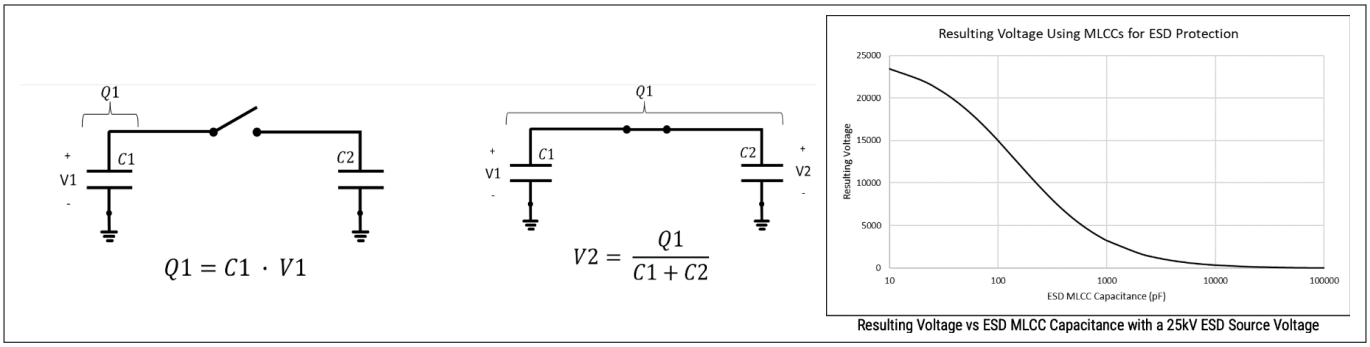



**Figure 27** **Charge sharing mechanism, source Kemet**

# References

**[1]** *Infineon-TLD7002-16ES-DS- EN device datasheet*; https://www.infineon.com/cms/en/product/power/led-driver-ic/litix-automotive-led-driver-ic/litix-pixel-rear/tld7002-16es/?redirId=287333#!documents

**[2]** *Infineon-TLD7002-16ES-SM-v01_00 Safety Manual* ; Some of the documents will require additional permission to be accessible (i.e. Safety Package), and they will be visible only on MyICP-LITIX please fill in the form to our Technical Assistance Center or contact support@infineon.com

**[3]** *Infineon-TLD7002-16ES-OTP-Parameter setting application note*; https://www.infineon.com/dgdl/Infineon-Z8F80497878-TLD7002-16ES-OTP-parameter-settings-ApplicationNotes-v01_00-EN.pdf?fileId=8ac78c8c8b6555fe018bf6824c505ef9&da=t

# Glossary

**CAN**

*controller area network (CAN)*

**DC-DC**

*direct current to direct current (DC-DC)*

**EMC**

*electromagnetic compatibility (EMC)*
The ability of electrical equipment and systems to function acceptably in their electromagnetic environment, by limiting the unintentional generation, propagation and reception of electromagnetic energy which may cause unwanted effects such as electromagnetic interference (EMI) or even physical damage in operational equipment.

**ESD**

*electrostatic discharge (ESD)*

A sudden and momentary flow of electric current between two electrically charged objects caused by contact, an electrical short or dielectric breakdown.

**GND**

*ground (GND)*

**HBM**

*human body model (HBM)*

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD) based on a human body.

**HSLI**

*high-speed lighting interface (HSLI)*

An Infineon-specific protocol for exchanging data among leaders and lighting-device followers.

**IC**

*integrated circuit (IC)*

A miniature electronic circuit built on the surface of a thin substrate of a semiconductor material.

**LCS**

*linear current sink (LCS)*

**LED**

*light-emitting diode (LED)*

A semiconductor circuit that emits light when activated.

**PCB**

*printed circuit board (PCB)*

A board that mechanically supports and electrically connects electronic components using conductive tracks, pads, and other features etched from copper sheets laminated onto a non-conductive substrate.

**PWM**

*pulse-width modulation (PWM)*

A technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

**TVS**

*transient voltage suppressor (TVS)*

An electronic component used to protect electronics from voltage spikes induced on connected wires.

**UART**

*universal asynchronous receiver transmitter (UART)*

A peripheral device or module for asynchronous serial communication in which the data format and transmission speeds are configurable.

**VDD**

*supply voltage (VDD)*

**VS**

*voltage supply (VS)*

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| Rev. 1.20 | 2025-10-30 | • Modified TLD7002-16ES hardware design guideline<br>• Modified COUTx and CVLED capacitors (6)<br>• Modified GPIN0 NTC resistor divider (8) |
| Rev. 1.10 | 2025-04-16 | • Modified VS capacitor, diode, and optional PI-filter (3)<br>• Modified VDD capacitor (4) |
| Rev. 1.00 | 2025-03-03 | • Initial document release |

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**Edition 2025-10-30**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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**Document reference**
**IFX-hhp1737018193669**

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