Integration of OBC and HV-LV DC-DC application using single AURIX™ TC4x MCU

Abstract

The key component of electric vehicle powertrain for re-fueling the energy is the On-board charger (OBC). It converts energy from the power grid to the battery, which delivers the energy required for powering the electrical motors and propelling the vehicle. The design of the OBC is becoming more challenging, especially when features like enabling faster charging time, higher power density or bi-directional energy flow without additional hardware must be implemented.

In this technical white paper, we will look at the topologies and the control of OBC and HV-LV DC-DC power converter, and how they are evolving over the trends of electric vehicles. We will also introduce the usage of the model-based design (MBD) for the implementation of the control algorithms, the benefits of the usage of AURIX™ TC4x microcontroller (MCU) in operating and efficient integration of the power converters. A feasibility study is successful done to prove that one TriCore™ and one parallel processing unit (PPU) in AURIX™ TC4x MCU can control three power stages (OBC and HV-LV DC-DC power converter) with cycle-by-cycle update.

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1 About this document

1.1 Scope and purpose

This white paper provides a study on efficient integration of OBC and HV-LV DC-DC converter using a single AURIX™ TC4x family MCU.

This document briefly describes the overview of OBC and HV-LV DC-DC converter topologies, the design and implementation of control algorithms for each of those topologies by means of AURIX™ Hardware Support Package (AHSP) using automated code generation. It also explains the verification of the operation of overall system.

1.2 Intended audience

This document is intended for the engineers with OBC and HV-LV DC-DC converter power electronics technical background, working on power electronics development tasks, system/solution/hardware/software architects, or concept engineers that are working on electronic power converters. This paper deals specifically with OBC and HV-LV DC-DC and the concepts or ideas presented in this paper are applicable on any other power converters like inverters or non-isolated DC-DC converters.

This document presumes the readers to have a basic knowledge on circuit design, topologies understanding and applying digital control in power converters.

1.3 Related definitions

Not applicable.

1.4 Related assets

- dSPACE® ControlDesk®
- MathWorks® (MATLAB®/Simulink®) and AURIX™ Hardware Support Package
- Infineon GUI Designer

2 Introduction to the following chapters

The following chapters will guide you through:

- An overview of the OBC and HV-LV DC-DC converter and their design trends
- The power converters stages inside the OBC and HV-LV DC-DC converter and the topologies
- The Hardware-in-the-Loop (HiL) approach, the reason behind and the benefits of using it
- Introduction of the AURIX™ TC4x MCU, the heart of the digital control of the power converters inside OBC and HV-LV DC-DC converter
- Implementation of the HiL approach and the results

2.1 Introduction to electric vehicles OBC and HV-LV DC-DC converters

An OBC is a battery charger inside an electric vehicle (Figure 1), with the functionality to control charging or discharging the high voltage battery from power grid. A HV-LV DC-DC converter is a power converter inside an electric vehicle, which converts the high voltage battery DC voltage to the low voltage battery (e.g. 12V battery) and supply power to the 12V loads present in the vehicle. They are the two major power converters of the electric vehicle drivetrain.

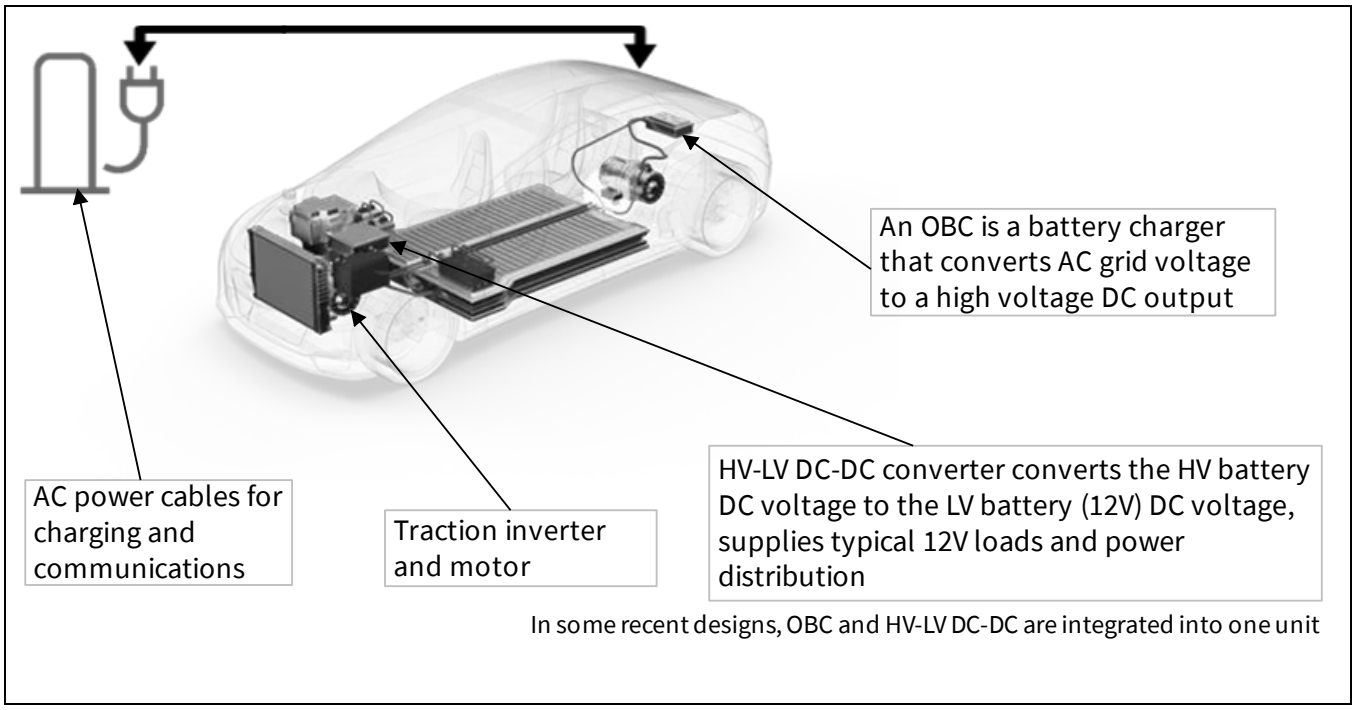

Figure 1 OBC and HV-LV DC-DC converter of an electric vehicle

2.2 Trends of battery electric vehicles with OBC

As shown in Figure 2, there are several trends about OBC design, focusing on:

- Performance increase
- New features like vehicle-to-load or vehicle-to-grid, supported by bi-directional conversion
- Battery voltage increase
- System integration (x-in-1)

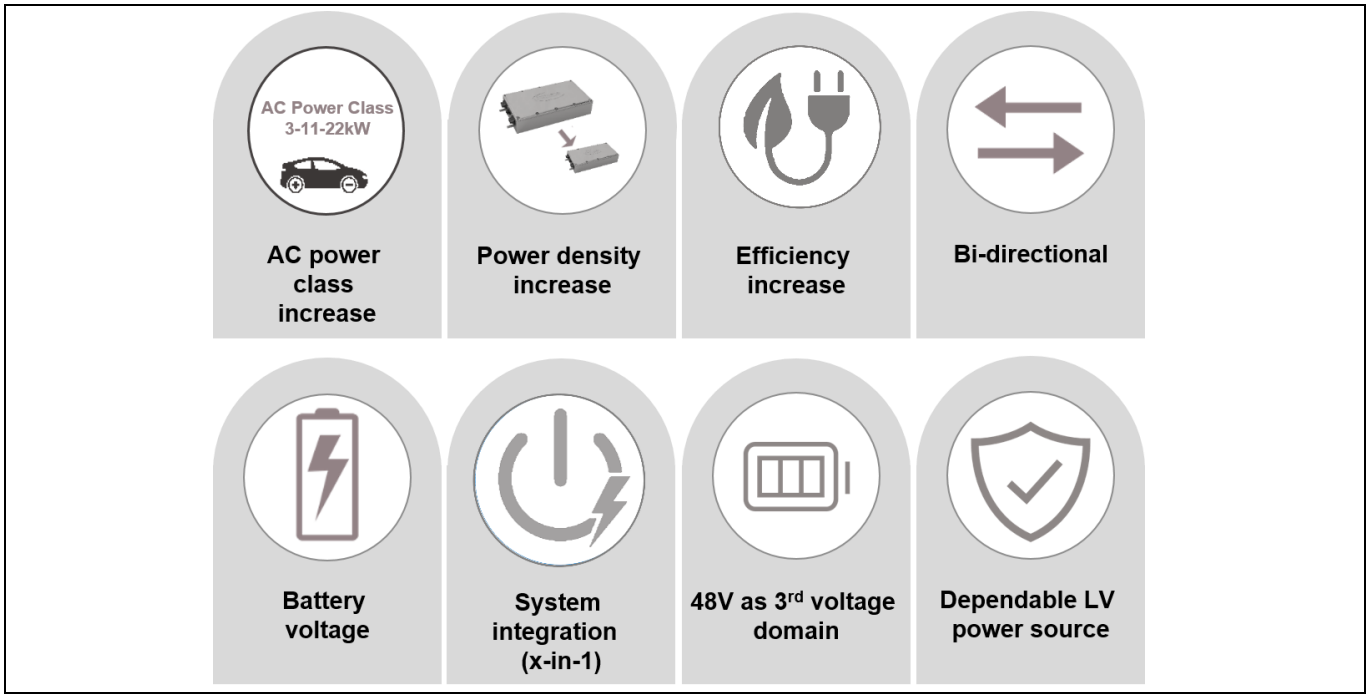

Figure 2 Trends overview of OBC and HV-LV DC-DC converter

A higher charging power would shorten the charging time, which is beneficial to the vehicle owner. Higher power also implies we need an efficient power converter to reduce the overall power loss and a compact design to reduce the size and weight of the OBC unit.

A state-of-the-art OBC design has a maximum efficiency of around 96% and a power rating ≤ 22 kW using 3-phase AC input. The AC power class is normally defined by the power grid type and standards / regulations of a specific country. Supported by high switching frequency hardware and digital control, the OBC is able to reach the power density of up to 3 to 4 kW/l.

If OBC is implemented as a bi-directional converter, the user is able to discharge the battery for:

- Powering an AC load: Vehicle-to-load
- Selling energy back to the power grid: Vehicle-to-grid

This creates more values and use cases for the same converter hardware and even unlocks a new business model. Nowadays, most of the OBC designs are ready for bi-directional power flow.

The high voltage battery voltage class has two mainstreams today: 400 V and 800 V class battery. A higher battery voltage can contribute to a faster charging power and shorten the time needed for the charging. Both battery voltage classes co-exist in the market. The OBC and HV-LV DC-DC converter designs need to adapt to different battery voltage classes.

Size and weight reduction are the key value drivers of any electronic control units (ECUs). Besides increasing the power density, it is also a trend to integrate multiple converters together.

Components like housing, cooling elements, wire harness and passive components can be integrated inside the single power conversion unit with both OBC and HV-LV DC-DC converter functionalities. The benefits of size and weight reduction make system integration easier and more convenient for assembly into the vehicle. In order to power-up more ECU loads, there is an increasing demand for the power at the low voltage domain and for

that reason HV-LV DC-DC converter design is moving towards higher output power ratings. Since there are different types of loads and the demand of the power over time is not always the same, the HV-LV DC-DC converter must be efficient over a wide range of output power, especially at light load conditions. Nowadays, the output current rating of the HV-LV DC-DC converter is in the range of 200-300 A, and the state-of-the-art peak efficiency is around 95%.

As power and current demand increases even above 300 A of current, due to very high ohmic losses a single HV-LV DC-DC converter cannot fulfill the power demand from the LV loads. In order to fulfil higher power demand, HV-LV DC-DC converter solutions with LV domain voltage increased to 48 V are developed. Introducing a 48 V power distribution voltage as a primary LV domain, reduction of the output current by a factor of 4 and reduction of the ohmic losses on the LV cables by a factor of 16 can be achieved.

2.3 Multiple MCUs as of today vs. one MCU for the future

Nowadays, the design of the OBC and the HV-LV DC-DC converter is using multiple MCUs. Due to the time critical tasks needed, the functionalities of the OBC and HV-LV DC-DC are separated into:

- Digital control of the power converters
- Communications
- Safety monitoring

Different types of MCUs are deployed for the different functionalities of the OBC and HV-LV DC-DC converter. Thanks to the capabilities of the AURIX™ TC4x MCU, the above-mentioned functionalities could be covered by one multi-core, faster clock speed AURIX™ TC4x MCU with a powerful parallel processing unit (PPU). This enables independent CPU usage for real-time critical use cases. It can also eliminate the needs of having multiple MCUs, multiple software source codes and even multiple toolchains for the software development. It helps to reduce development time, cost and increase the ease-of-use of the system components.

2.4 The need for inter-ECU communication and charging infrastructure security

A typical charging process consists of a hand-shaking communication between charging infrastructure to the electric vehicle, between OBC and some ECU like high voltage battery management system (BMS) and vehicle control unit (VCU). The MCU inside the OBC is very important to cover not only the power conversion tasks but also the off-board inter-ECU communications. MCU resources must support the time critical tasks like digital control loop and protections of a power converter. The communications to the charging infrastructure according to the latest ISO 15118-20 standard is fully supported by AURIX™ TC4x cyber security satellite (CSS) hardware accelerator.

3 Introduction to the OBC and HV-LV DC-DC converter functional blocks

There are two main electrical power converter stages working together in the OBC (Figure 3). The first stage is AC-DC converter which rectifies the power grid AC voltage into a DC voltage. This stage also performs the power factor correction (PFC) functionality to improve the power grid voltage quality (reducing harmonic distortions) by actively controlling the power factor to unity. This stage is therefore very often called PFC stage. The second stage is called HV-HV DC-DC converter stage. It converts the DC voltage output from the PFC stage into another DC voltage level to feed the high voltage battery with galvanic isolation provided by the high-frequency transformer.

Nowadays, the OBC design have bi-directional energy flow capability. During charging mode, the energy is fed from the power grid to the high voltage battery, while during discharging mode the energy is fed from the high voltage battery back to the power grid or fed to various types of AC loads. Implemented PFC stage will be described in Chapter 3.1 and isolated HV-HV DC-DC stage will be described in Chapter 3.2.

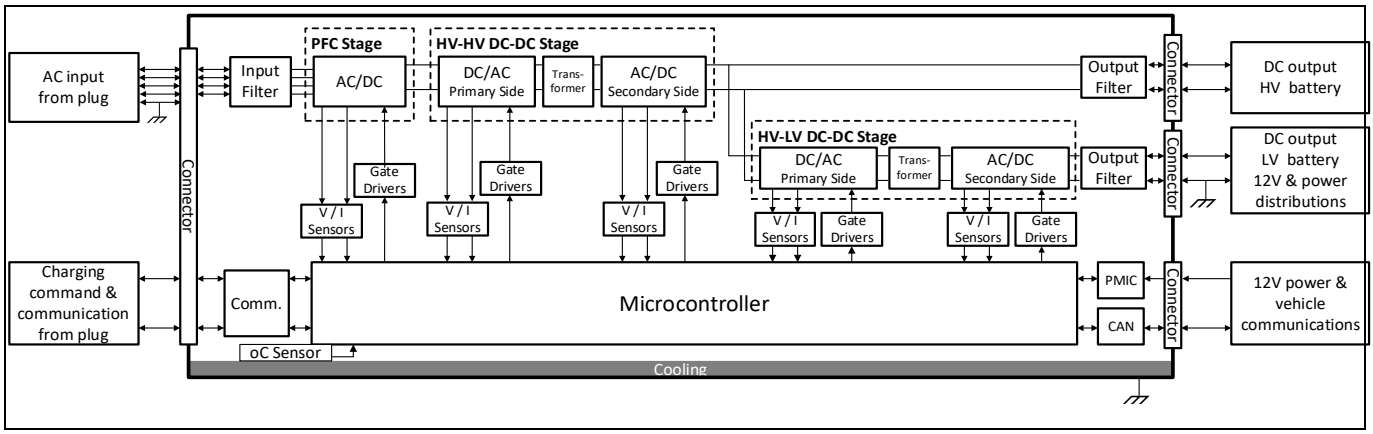

Figure 3 Block diagram of the power stages within OBC and HV-LV DC-DC converter

Typically, in electric vehicle, OBC works together with one HV-LV DC-DC converter (marked as “HV-LV DC-DC Stage” in Figure 3). This converter has only one stage which converts the HV battery voltage to the LV domain (12 V, 24 V or 48 V) and provides galvanic isolation between the two voltage domains.

HV-LV DC-DC converter can be unidirectional or bi-directional. For bi-directional case, the HV DC-link capacitor inside OBC or traction inverter could be charged up by the energy flow from LV domain to HV domain through this HV-LV DC-DC converter. Functionality of implemented HV-LV DC-DC converter is described in Chapter 3.3.

3.1 General description of 3-phase AC-DC PFC stage

As a state-of-the-art, PFC stage can be implemented either as a totem-pole or 3-phase bridge (B6) topology. Main advantages of the latter topology are:

- Smaller number of used components
- Versatile digital control which allows control of bi-directional power flow
- Near-unity power factor control using space vector modulation (SVM) scheme

Because of the above-mentioned reasons, the B6 topology is implemented in this project. During charging mode, power grid AC voltages (v_a, v_b and v_c shown in Figure 4) are rectified and boosted to supplying DC link

capacitor (C_{in}) with the DC current. The 3-phase bridge (B6 bridge, switches PFC_T1, 2…..6 shown in Figure 4) is driven by the gate pulses generated through the space vector modulation (SVM). PFC stage output DC link voltage (V_{DC}) is regulated depending on DC link voltage required by the HV-HV DC-DC converter stage and operating mode (either charging or discharging).

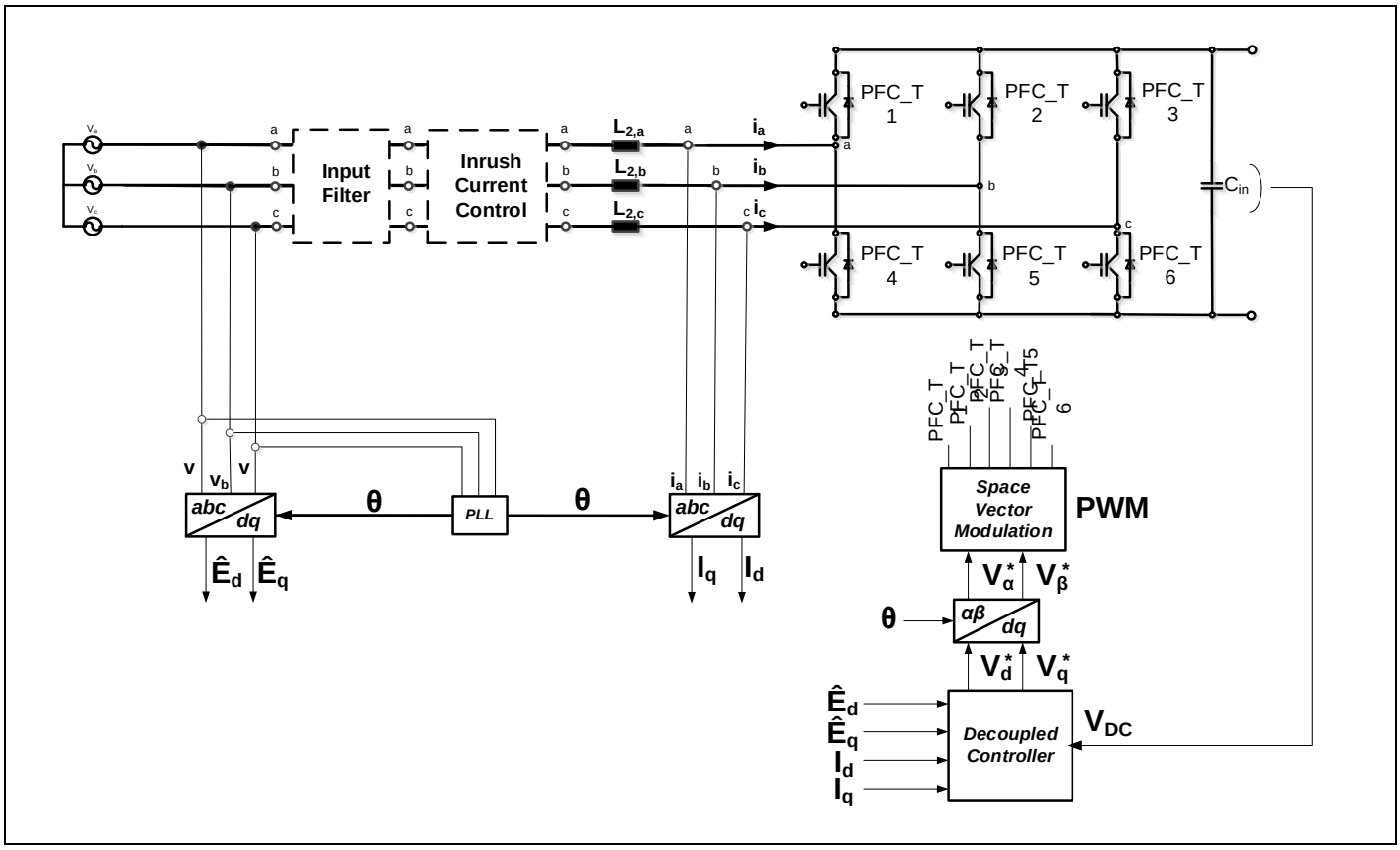

Figure 4 Block diagram of 3-phase B6 bridge PFC stage

PWM signals (PFC_T1, 2, … 6 shown in Figure 4) are generated by SVM pulse width modulation (PWM) block. Whole theory and mathematical apparatus used in field-oriented control (FOC) applied on electrical motor drives can be implemented in the case of PFC stage. AC-DC power conversion is analogues to braking mode, while the DC-AC power conversion is analogues to the motoring mode.

To calculate B6 duty cycles, 3-phase inductor currents and power grid voltages are measured (i_a, i_b, i_c, v_a, v_b, v_c shown in Figure 4). They are transformed by Clarke and Park transforms into two orthogonal components in rotating reference frame (dq), namely I_d, I_q, $\hat{E}_d$ and $\hat{E}_q$. Phase-locked-loop (PLL) is used to track the phase θ of the power grid voltage [1][2].

As shown in Figure 5, to linearize the control algorithm, the new variable $W = V_{DC}^2$ is introduced. Reference I^*_d is calculated by the voltage controller with current limiter, proportional to the difference of the measured W and the reference W*.

V^*_d/V^*_q and θ are fed to the inverse Park transform to get reference V^*_α/V^*_β. They are used as inputs for SVM PWM pattern generation to control the power switches of the PFC stage [3].

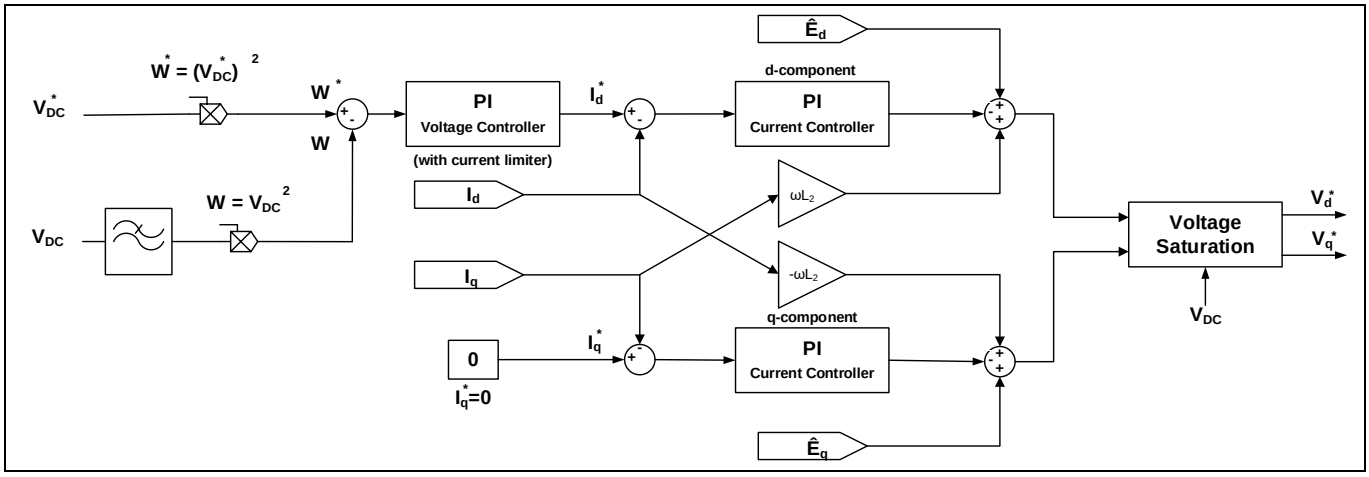

Figure 5 Control block diagram of 3-phase B6 bridge PFC stage

3.2 General description of isolated CLLC HV-HV DC-DC stage

An isolated resonant CLLC stage is used either to charge or discharge the HV battery at various DC link voltages (supplied from PFC stage) or load currents. It supports bi-directional energy flow as well as galvanic isolation between the primary voltage domain and the secondary voltage domain.

Purpose of the high frequency resonant network is to reduce semiconductors switching losses by enabling zero voltage switching (ZVS) and zero current switching (ZCS). The resonant frequency network shown in Figure 6 comprises of primary inductor (L_{r1}), primary capacitor (C_{r1}), secondary inductor (L_{r2}) and secondary capacitor (C_{r2}). In this design, resonant frequency (f_r) is set to be around 100 kHz. Comparing to other isolated non-resonant DC-DC topologies, presence of the resonant capacitors (C_{r1} and C_{r2}) blocks the flow of DC current and inherently protects the transformer from saturation because of the DC offset. Soft switching (ZVS/ZCS) can be achieved in a certain range of operating points that depend on the voltage conversion ratio and the output load current.

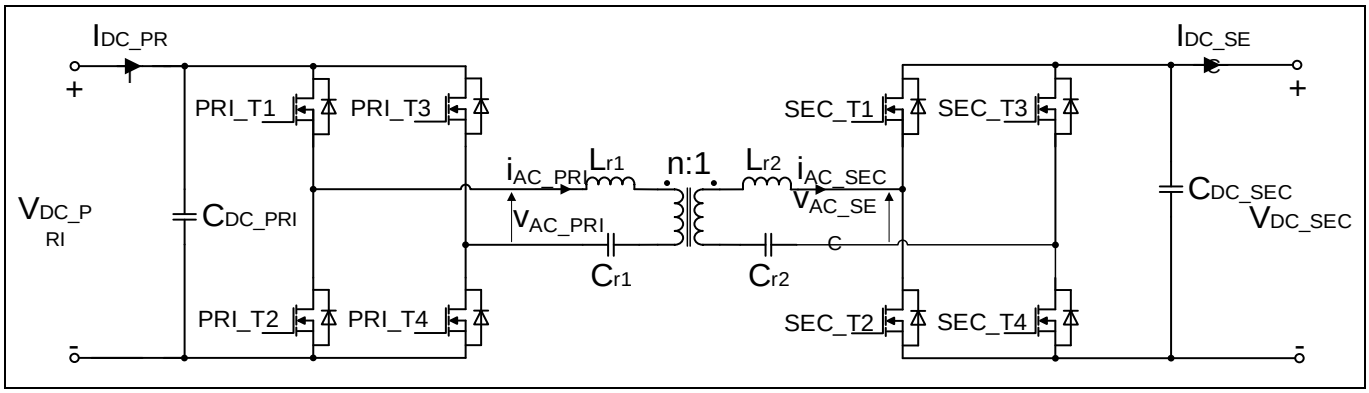

Figure 6 Isolated resonant CLLC converter topology

As shown in Figure 7, the pulse frequency modulation (PFM) is used to operate the converter, where the switching frequency (f_{sw}) is varying from 50 kHz up to a maximum 250 kHz. Maximum frequency is limited by the allowed maximum switching losses of the power switches and the system EMI limits. HV battery (typically 400 V or 800 V, connected to V_{DC_SEC} as shown in Figure 6) can be charged either in constant current (CC) or constant voltage (CV) operation mode. Discharging of HV battery is implemented in constant power (CP) operation mode. As shown in Figure 7, depending on the ratio of f_{sw} and f_r , the duty cycles and phase shift of secondary side switches are calculated differently for 3 operating regions ($f_{sw} > f_r$, $f_{sw} = f_r$ and $f_{sw} < f_r$) [4].

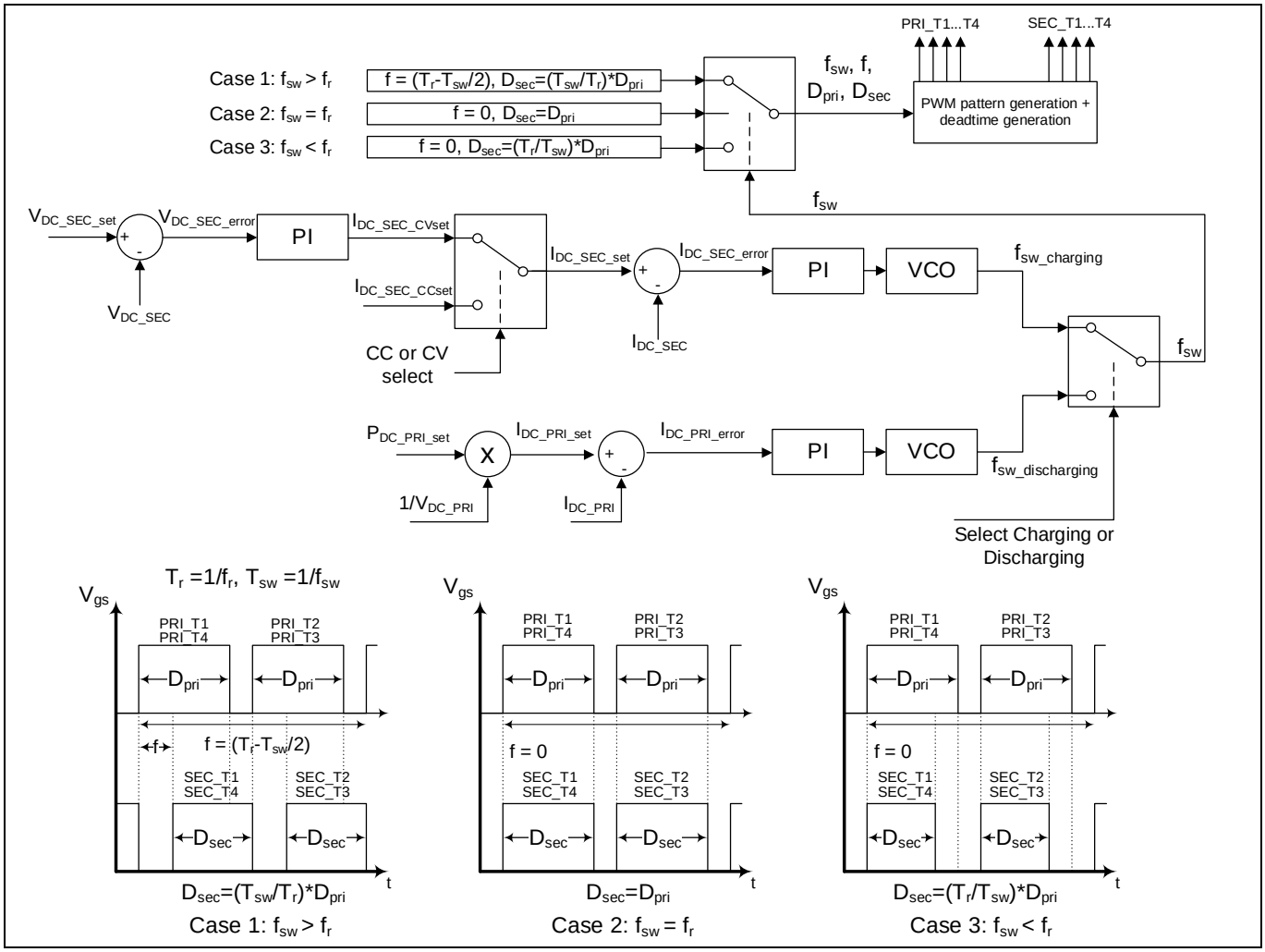

Figure 7 Isolated resonant CLLC converter control scheme

3.3 General description of isolated DAB in HV-LV DC-DC stage

Isolated DAB stage (shown in Figure 8) is used to charge or discharge the LV battery at various HV battery voltages or load currents [4]. It supports bi-directional energy flow and has galvanic isolation between the primary and secondary voltage domains.

Similar to the CLLC stage, LV battery can be charged either by operating in CC or in CV mode. The CP mode is used for battery discharging (see control scheme in Figure 8). Single phase shift (SPS) modulation scheme is implemented in this study. With SPS modulation, the DAB stage operates under ZVS conditions, minimizing the switching losses. Unlike the CLLC converter, ZVS operation region is narrow and depends on the voltage conversion ratio and on the output current.

Output of the DAB stage controller is the phase shift (φ) between primary and secondary side PWM signals (Figure 9). Amount of power that is being transferred between primary and secondary side is proportional to φ ($-\pi/2 \le \varphi \le \pi/2$). For $\varphi > 0$ LV battery is charged, and for $\varphi < 0$ LV battery is discharged.

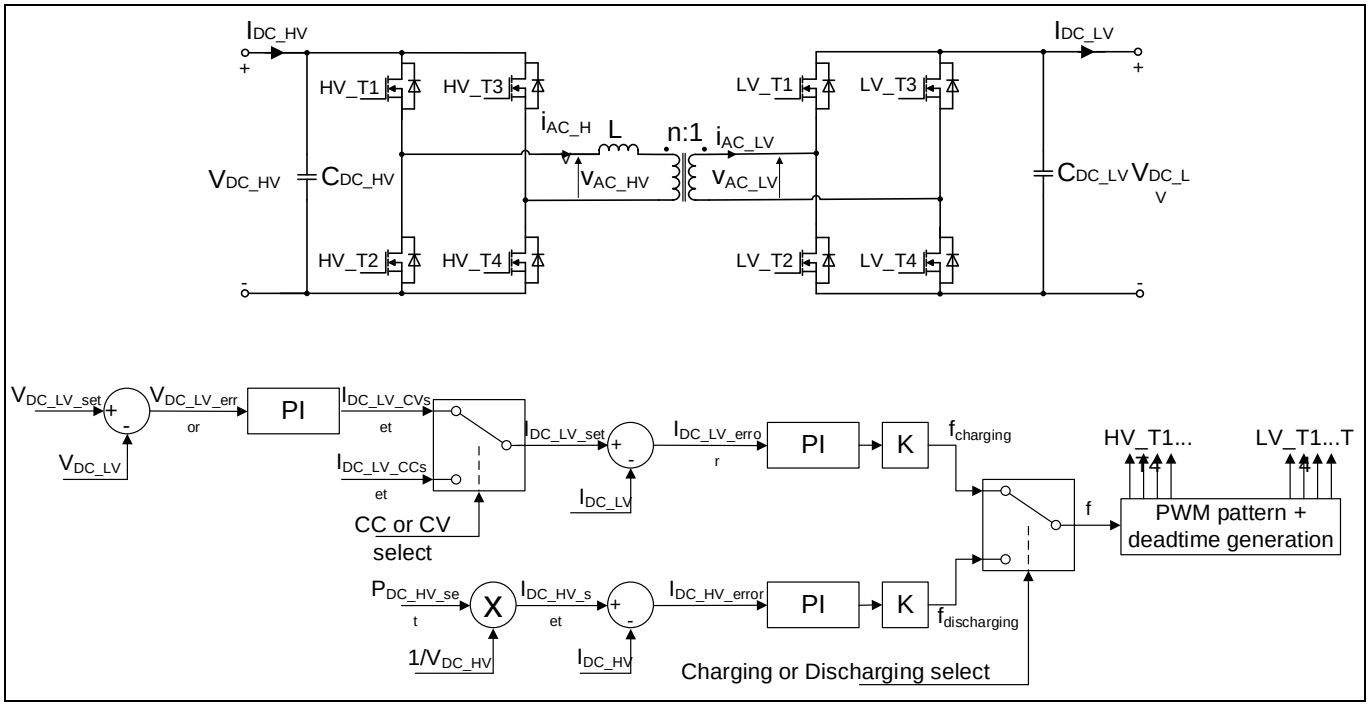

Figure 8 Isolated DAB converter topology and its control scheme

As shown in Figure 9, in the primary H-bridge HV_T1 and HV_T4 are driven by the same PWM signal with 50% duty cycle and similarly HV_T2 and HV_T3 are. HV_T1 and HV_T2 are complementary to each other and similarly HV_T3 and HV_T4 are. A dead-time is introduced between the two PWM signals driving HV_T1/HV_T2 and HV_T3/HV_T4 pairs to avoid current shoot-through in these H-bridges. Similar pulse patterns are used to drive the secondary H-bridge switches. To control the flow of the power between primary and secondary side, phase shift φ is introduced between corresponding PWM signals.

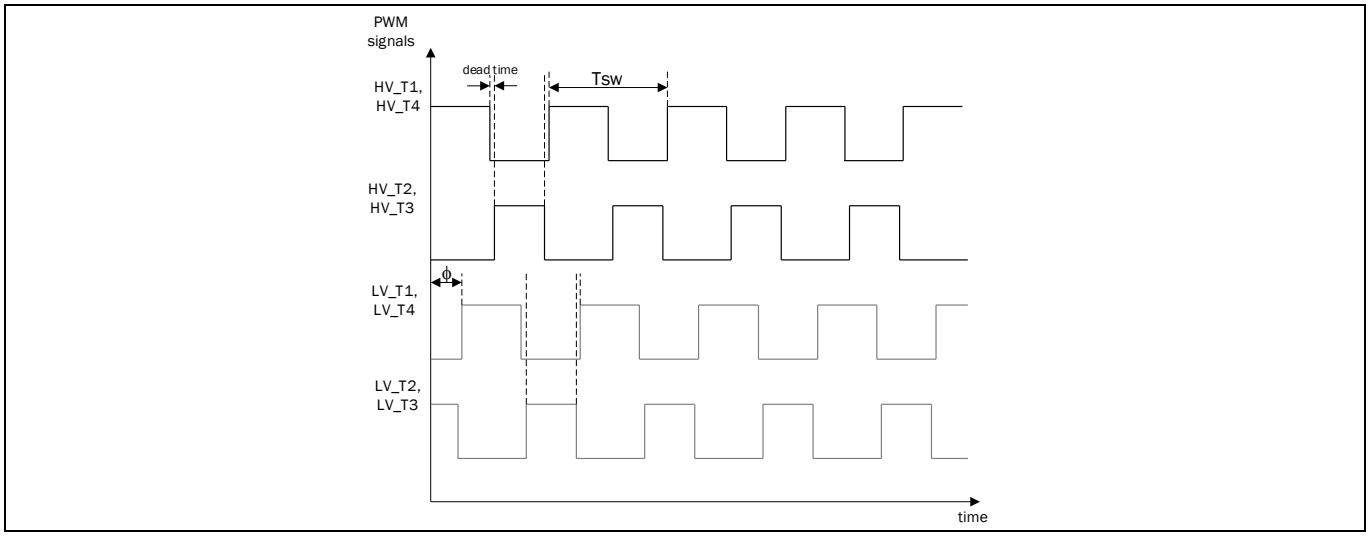

Figure 9 PWM signals for operating HV and LV bridges by means of SPS modulation

4 One AURIX™ TC4x providing high performance solution for full OBC and HV-LV DC-DC application

AURIX™ TC4x is designed to cover full OBC and HV-LV DC-DC application by single MCU, covering real-time control, communication security and auxiliary housekeeping functions. For real-time control, AURIX™ TC4x provides dedicated peripherals with state-of-the-art performance, and it also provides highly efficient bus architecture for fast accessing measurement results and updating driver signal. AURIX™ TC4x provides significant DMPIS improvement with TriCore™ 1.8, meanwhile computation of complex algorithms is dramatically reduced by parallel processing unit (PPU). In addition, newly added converter-DSP (CDSP) take over execution of simple control loops offloading main cores. From security perspective, AURIX™ TC4x provide cyber security satellite (CSS) for parallel hardware accelerating to satisfy latest ISO15118-20 standard and cyber security real-time module (CSRM) with embedded TriCore™ 1.8 with isolated NVM. Figure 10 illustrates the detailed AURIX™ TC4x real-time (RT) control unit.

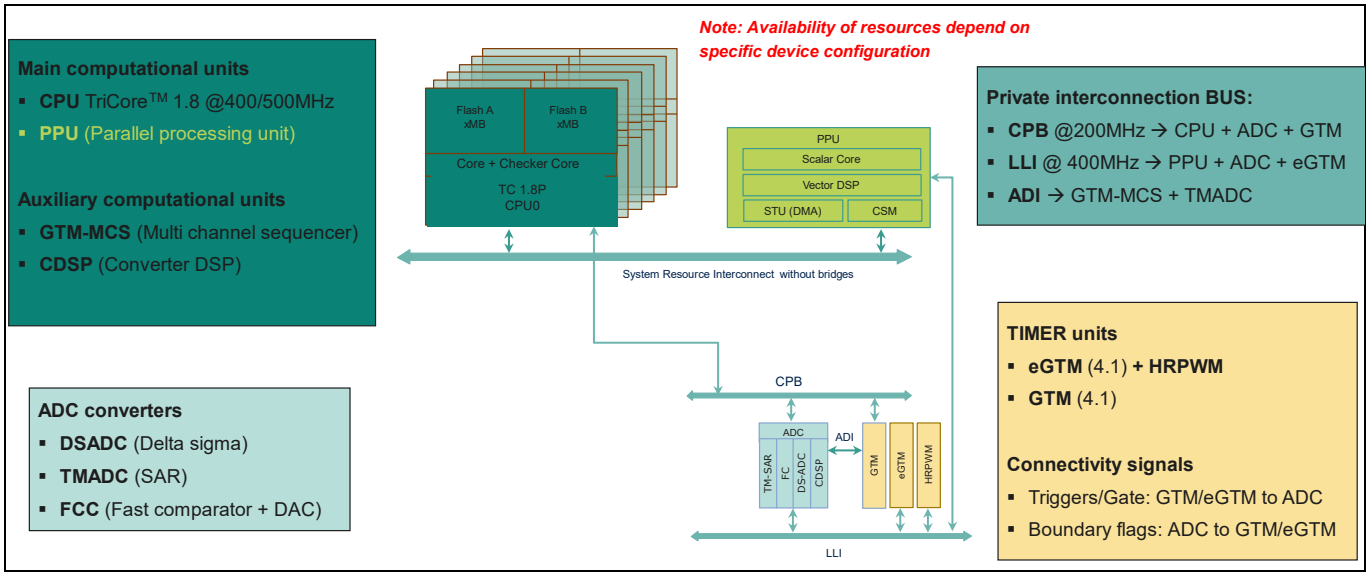

Figure 10 AURIX™ TC4x real-time control unit

Dedicated features from AURIX™ TC4x explain why AURIX™ TC4x is the best choice for OBC and HV-LV DC-DC application:

- TriCore™ 1.8, PPU, CDSP provide more DMIPS and flexibility for diversified control loops
- Dedicated low latency interface (LLI) and converter peripheral bus (CPB) enable ultra-fast peripherals access
- Analog peripherals time-multiplexed analog-to-digital converter (TMADC), delta-sigma ADC (DSADC), fast-compare comparator (FCC) and delta-sigma external modulation (DSEXTMOD) provide state-of-the-art measurement accuracy and necessary isolation for the power conversion applications
- Enhanced generic timer module (eGTM) with high-resolution PWM (HRPWM) provides the most efficient power conversion covering full operating range
- Security cluster increases throughput by parallel computation and supports upcoming security standards
- MathWorks® AURIX™ Hardware Support Package (AHSP) enables the fast prototyping and reduces the development efforts

4.1 TriCore™ 1.8, PPU, CDSP provide more DMIPS and flexibility for control algorithms

TriCore™ is the first unified, single-core, 32-bit microcontroller-DSP architecture optimized for RT embedded systems. The TriCore™ instruction set architecture (ISA) combines the RT capability of a MCU, the computational power of a DSP, and the high-performance features of a reduced instruction set computer (RISC) load/store architecture.

TriCore™ in AURIX™ TC4x are all with lock step for safe execution environment (native ASIL D). In addition, AURIX™ TC4x add PPU and add up to 12 CDSPs. The DMIPS comparison between AURIX™ TC3x and TC4x is illustrated in Figure 11.

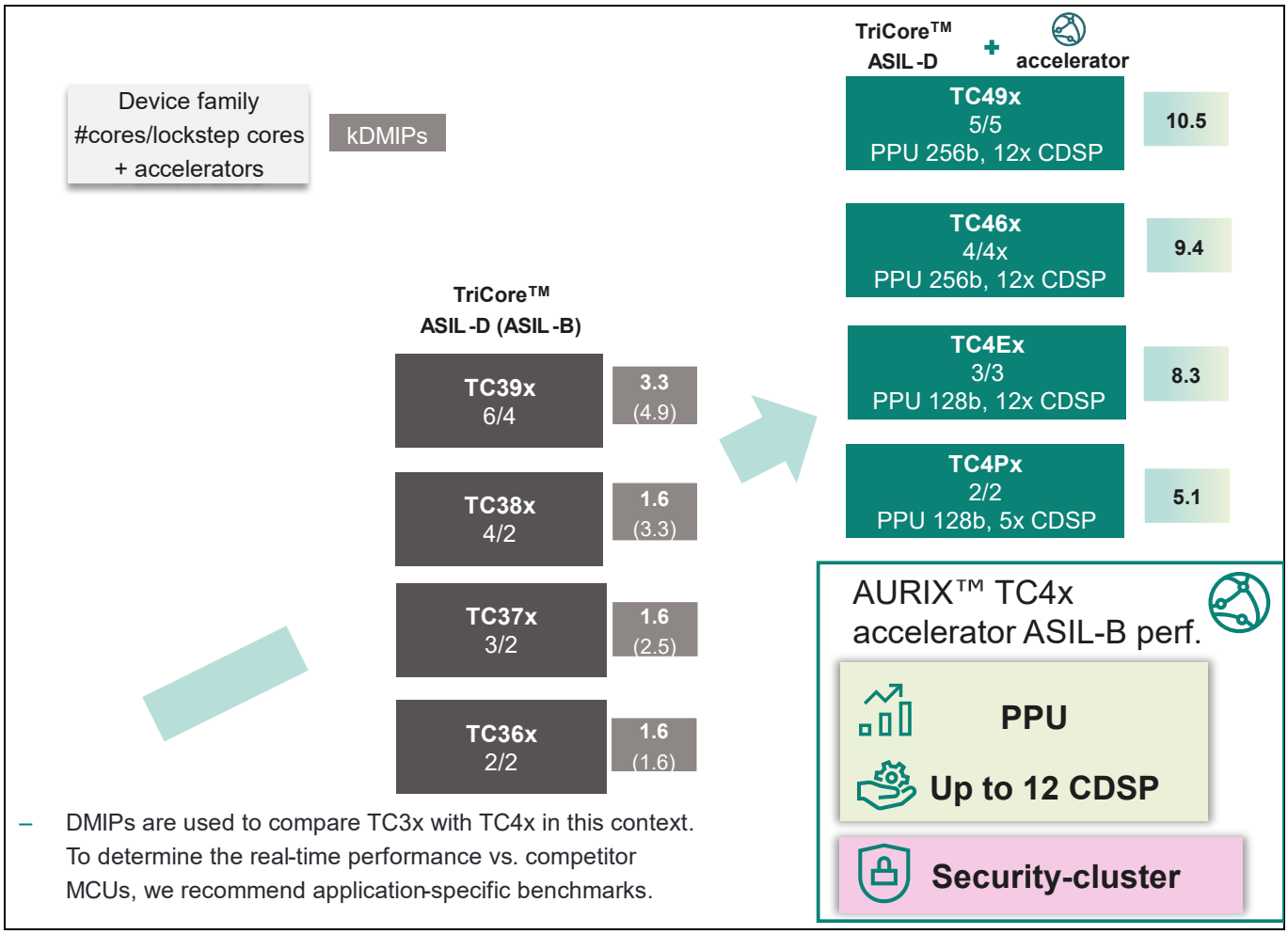

Figure 11 DMPIS comparison between AURIX™ TC3x and TC4x

PPU architecture is illustrated in Figure 12. It is a dedicated core with its own memory, doing vectorization for complex algorithms, named single instruction multiple data (SIMD). Inside PPU, scalar core is responsible for state machine-like operation and the vector core is responsible for executing complex algorithms. It can benefit multi-phases systems such as interleaved buck/boost converters, power stages requiring relatively complex algorithms such as PFC or three phases single-stage OBC.

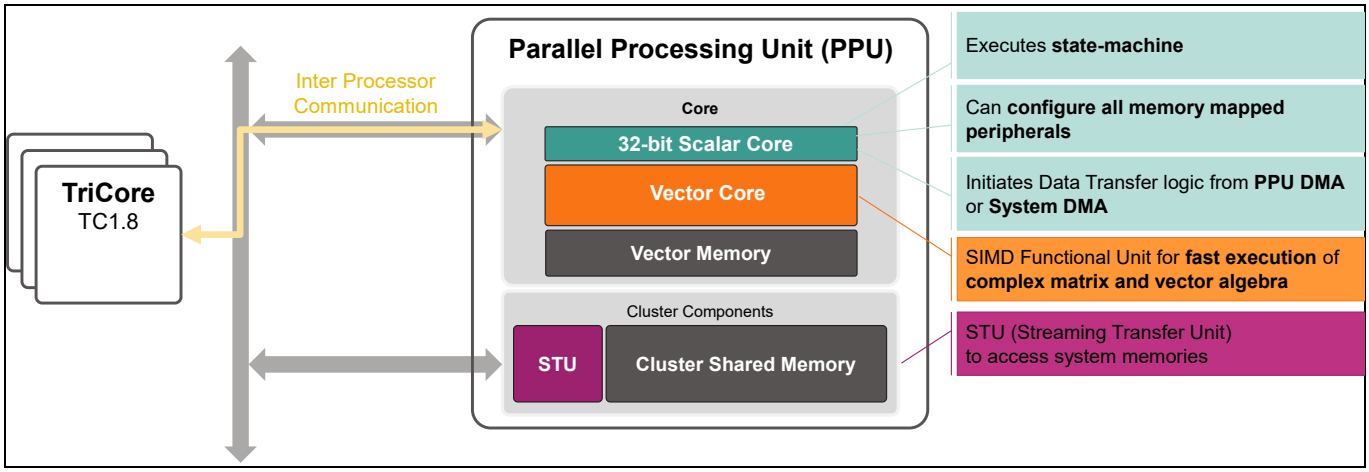

Figure 12 PPU architecture

Each CDSP consists of an Argonaut RISC core (ARC), around which the HW wrapper is made for enhanced functionality. On one hand, being part of ADC clusters, CDSP is used as the post-sampling filter before giving the ADC sampled value to the control loop. On the other hand, it can also be considered as a core executing digital controllers (e.g. proportional-integral controller or two-pole two-zero controller) to offload the TriCore™.

4.2 Dedicated LLI and CPB enable ultra-fast control loop and protection execution

CPB is connected to ADC clusters and generic timer module (GTM), which can be directly accessed by several TriCore™. In addition, a dedicated bus named LLI makes RT control needed peripherals, such as ADC, GTM, eGTM being very close to PPU (also very close to some of TriCore™). Hence, it provides PPU and TriCore™ extreme low latency accessing to ADC results and updating PWM.

In addition, RT responsiveness is largely determined by ultra-low best-in-class interrupt latency and context-switch time. The high-performance architecture minimizes interrupt latency by avoiding long multi-cycle instructions and by providing a flexible hardware-supported interrupt scheme. The architecture also supports fast-context switching.

4.3 Analog peripherals provide state-of-the-art accuracy and execution performance

Figure 13 illustrates that each analog channel has its own sample and hold stage which make parallel sampling possible within all the channels. For each TMADC kernel, it includes two ADC SAR cores and the conversion sequence is fully configurable, meanwhile there are 16 channels plus 2 internal monitor channels for on-chip signal supervision (for diagnostic usage). TMADC kernel provides sampling rate below 300 ns with 12 bits accuracy. Each channel can accept up to 3 triggers (two HW triggers, one SW trigger). The trigger could be from eGTM, GTM, GPIOs, and system control unit. In total, 64 hardware triggers are supported for all different kind of ADCs.

Each channel consumes in the worst case less than 3 picocoulomb on the input charge, which makes the ADC suitable for any kind of sensors supporting the next generation requirements for the applications like 48 V board nets.

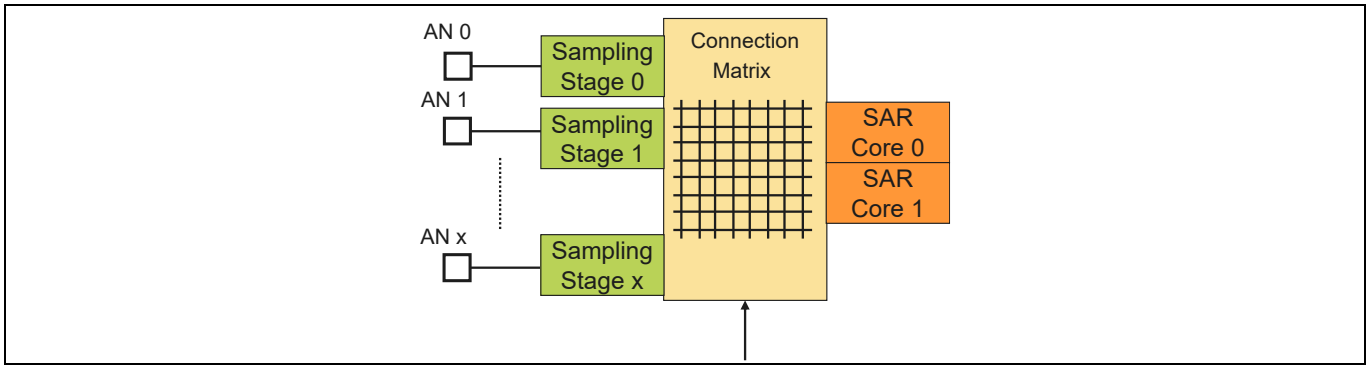

Figure 13 TMADC architecture for one TMADC instance

Another type of ADC called DSADC is used to satisfy higher accuracy requirements. DSADC can achieve more than 86 dB signal-to-noise ratio (SNR), meaning roughly 14 effective number of bits (ENOB) (for 5 V input, the LSB step is about 305 uV). Figure 14 illustrates the architecture of DSADC and DSEXTMOD. It can support either on-chip DSADC modulator up to 40MHz or external modulator. In both cases, CIC decimation filter and configurable filter chain are in the AURIX™. When the external modulator is used for several channels, the reinforced digital isolator can be used to replace several analog amplifiers, which can be one of options to save bill of materials (BOM) cost.

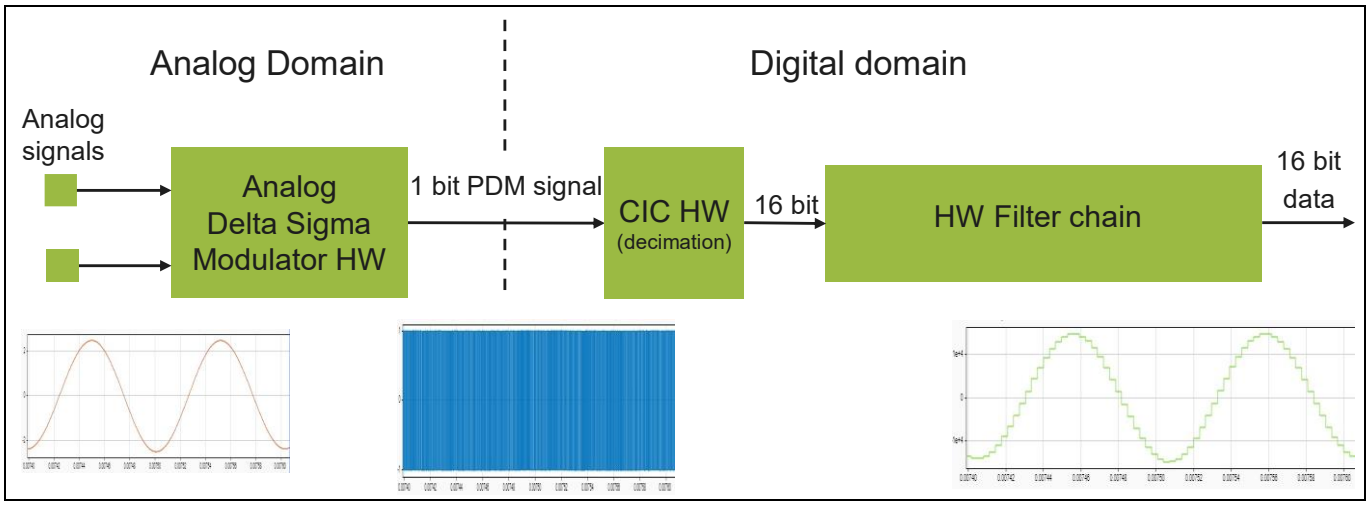

Figure 14 DSADC architecture

FCC with software configurable boundary value can perform below 50ns for finishing the comparison. Therefore, special control schemes such as peak-current mode control, executing necessary protection such as over-current protection and short circuit protection are supported.

4.4 eGTM with HRPWM provides the most efficient power conversion covering full operating range

eGTM provides 156 ps PWM resolution, which enables fine tuning of output voltages avoiding oscillations, especially at light load conditions for resonant converters. For interleaved topologies, the fine-tuning interleaved phase shift can significantly improve the current ripple which can reduce the size of magnetic components.

4.5 Security cluster of AURIX™ TC4x increases throughput by parallel computation and supports upcoming new security standard

For OBC and HV-LV DC-DC, the communication between a vehicle and a charger needs to be secured. Latest standard ISO15118-20 is published to mitigate any potential cybersecurity risks for any asset in vehicles. Effective cybersecurity development processes and measures need to be in place, otherwise it would be difficult to obtain approval certification.

By introducing the state-of-the-art next generation HW security module, comprising of a powerful CSS and CSRM, the security challenge can be solved. The architecture is illustrated in Figure 15. CSRM is developed to address the requirements of root-of-trust, public key cryptography, true random number generation, and a dedicated TriCore™ to perform all crypto related operations. Moreover, it also supports secure SW over-the-air updates. CSS is proposed to address the high-performance requirements of communication security, hence we present 'cyber security satellites' that will perform all crypto operations related to symmetric key cryptography and hashes. By using the satellite concept, it allows the application to directly access the satellites while making sure that the CSRM controls the access management of the crypto satellites, i.e. the embedded application areas cannot read keys stored in the satellites. To meet the performance requirements, the CSS supports hardware acceleration, such as: SHA-2-512, AES-256, and parallelization of crypto operations on multiple channels. Additionally, the satellites support safety for security requirements, including providing support for freedom from interference.

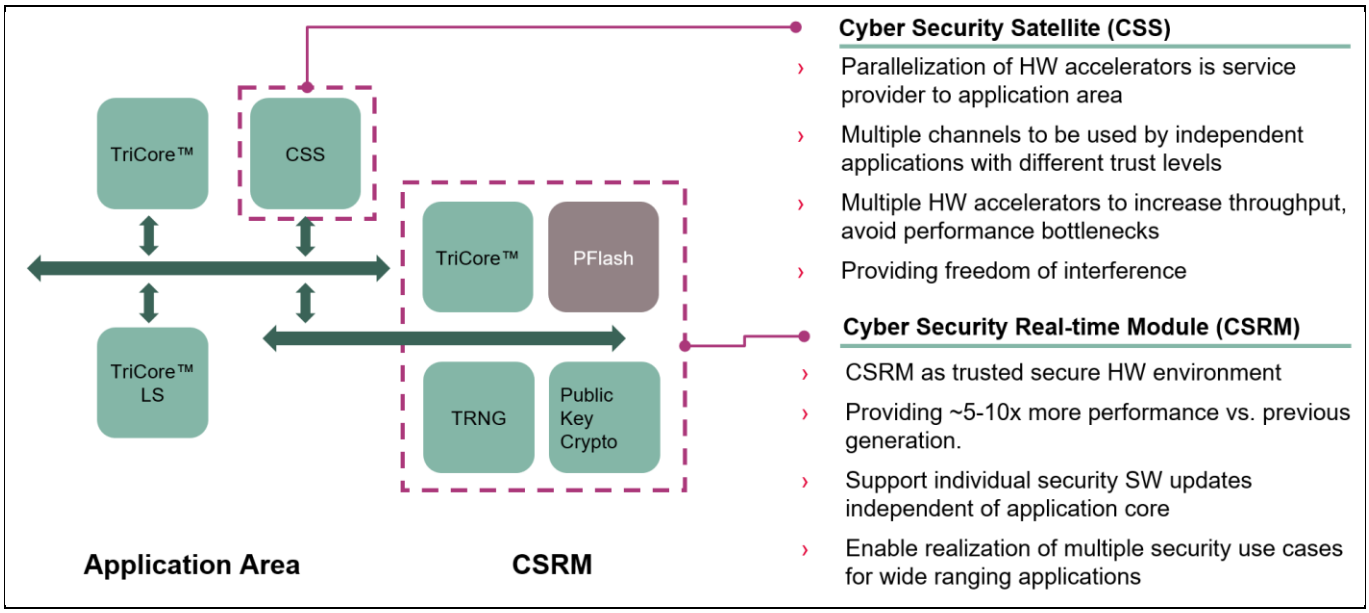

Figure 15 Next generation hardware security cluster

4.6 MathWorks® AURIX™ hardware support package (AHSP) enables the fast prototype

Infineon Technologies collaborate with MathWorks® to develop the HSP for AURIX™ MCUs. The AURIX™ HSP illustrated in Figure 16:

- Is a plugin to Embedded Coder® and SoC Blockset™
- Supports multicore application development

- Provides simulation support with target
- Aids to generate target specific optimized code
- Connects application to the peripherals → calls to driver APIs
- Provides HW mapping → Configuration GUI

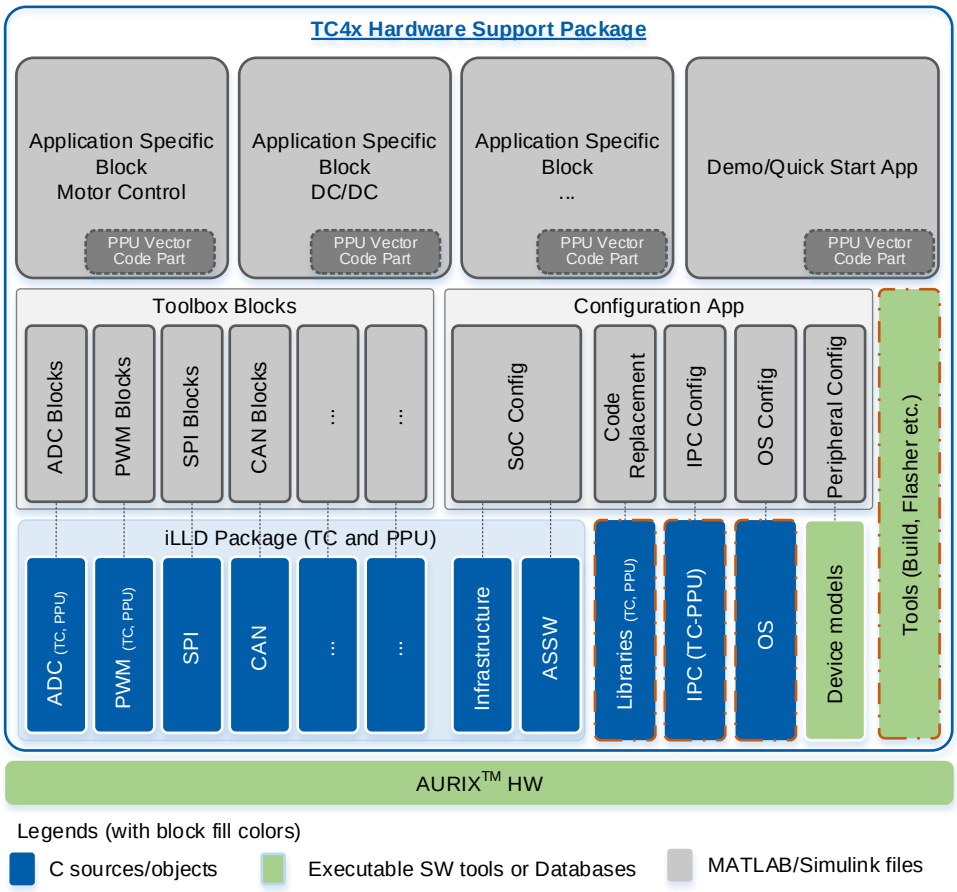

Figure 16 MathWorks® AURIX™ hardware support package

5 Hardware-in-the-loop (HiL) approach with real-time capable dSPACE plant

5.1 Introduction to model-based design (MBD)

The MBD in power electronics is an efficient approach to design and validate the control system of the power converters in simulation domain before the real hardware implementation. By modeling the “building blocks” of the converters into the plant, the plant and the controller behavior can be simulated and analyzed. Code generation could be supported with this approach. In automotive development, this is the state-of-the-art and becoming a standard.

The advantages of MBD approach are:

- Faster time-to-market
- Scalability and re-usability of the system
- Reduction of design errors and early detection of bugs and failures
- Lower cost of the development, by reducing the number of physical prototypes

5.2 Hardware-in-the-loop setup

In this study, the quasi-real time plant models of the three power converters (PFC stage, HV-HV DC-DC converter and HV-LV DC-DC converter) are implemented on the dSPACE® SCALEXIO® LabBox [5] real time platform (RTP) using the MBD approach. The entire system setup which integrates the AURIX™ TC4x MCU and the RTP system is shown in Figure 17.

The RTP system hardware is a System-on-Chip (SoC), which consists of a processor, a configurable field programmable gate array (FPGA) and input/output (I/O) boards. The FPGA base board houses the FPGA, interacts with the I/O as well as processor board, and the plant model’s binaries are executed here. The processor board facilitates the data exchange with each FPGA main board via buffer or register interface. Processor board also acts as a host computer, where a slow rate models (milliseconds range) can be implemented. Furthermore, it provides the interface for logged data and signal visualization on the ControlDesk® [6] graphical user interface (GUI).

The I/O board is synonymous with the peripheral hardware (HW) of MCU which hosts the ADC, digital-to-analog converter (DAC) and digital I/Os. In this implementation, the RTP system has three FPGA main boards. Each FPGA main board inter-connects to two I/O boards. To model the behavior of the OBC and the DAB, its overall electrical circuit is divided into different stages. Each stage is modelled separately and implemented on one of the three FPGA boards of the RTP.

The quasi-real time plant model runs at a small discrete time step on the FPGA. The input and output signals are sampled periodically at a pre-set sample rate. For a better emulation quality and achieving the quasi-real time behavior of the emulated plant, the plant model emulated is ensured to have 20 to 30 times higher sample rate compared to the converter’s switching frequency.

The plant model sample time (time step) for the emulated converters is:

- PFC converter: 320ns
- CLLC converter: 120ns
- DAB converter: 200ns

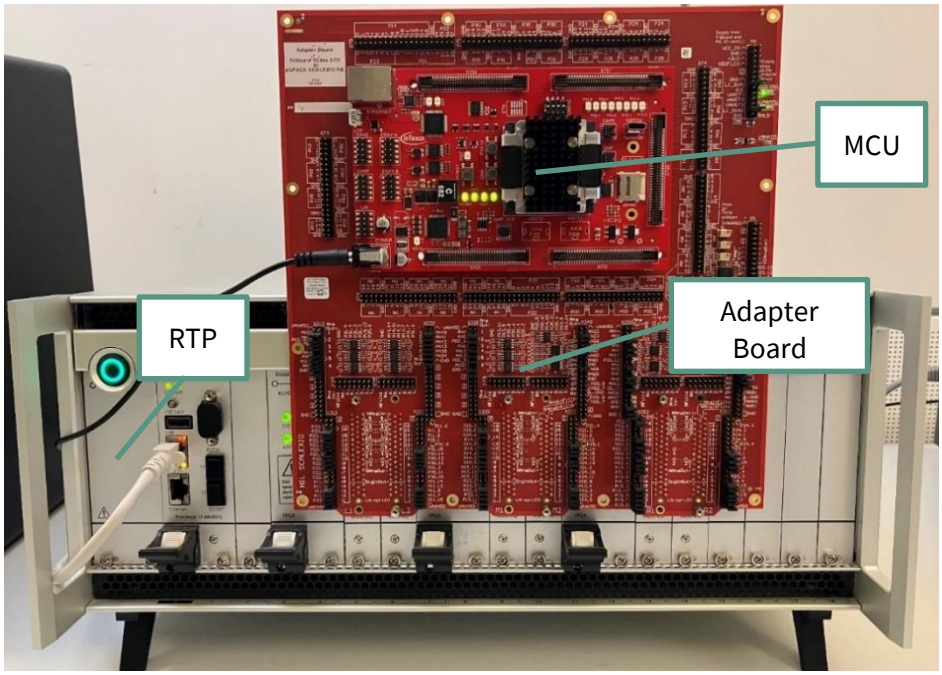

Figure 17 MCU and RTP FPGA and I/O board connection setup

To control and monitor the plant model, the analog and digital interface signals are defined for each converter. The analog interface signals are the current, voltage and temperature measurements from each converter. The digital input signals (input to AURIX™ TC4x MCU) are the emulated fault signals such as gate driver faults, over current faults and over temperature faults.

The analog signals are acquired by the time-multiplexed analog-to-digital converter (TMADC) of AURIX™ TC4x MCU and the digital signals are acquired by the general-purpose input output (GPIO) channels of AURIX™ TC4x MCU, pre-configured as the digital input channels. An adapter board is used to connect the MCU to RTP as shown in Figure 17.

Output signals from AURIX™ TC4x MCU are gate pulses for the switches of each converter's gate drivers and additional stimulus signals, e.g. to enable the gate drivers or to reset the faults. Parameterization, control, tuning and visualization of the plant model is carried out via the graphical user interface (GUI) created in dSPACE® ControlDesk® tool.

6 Implementation

To control three power converters with only one AURIX™ TriCore™ (TC) and one PPU as shown in Figure 18, a systematic approach is used to identify the overall execution time, to optimize model implementation to generate efficient code and to find out the optimal partitioning of the controllers combination on TC and PPU.

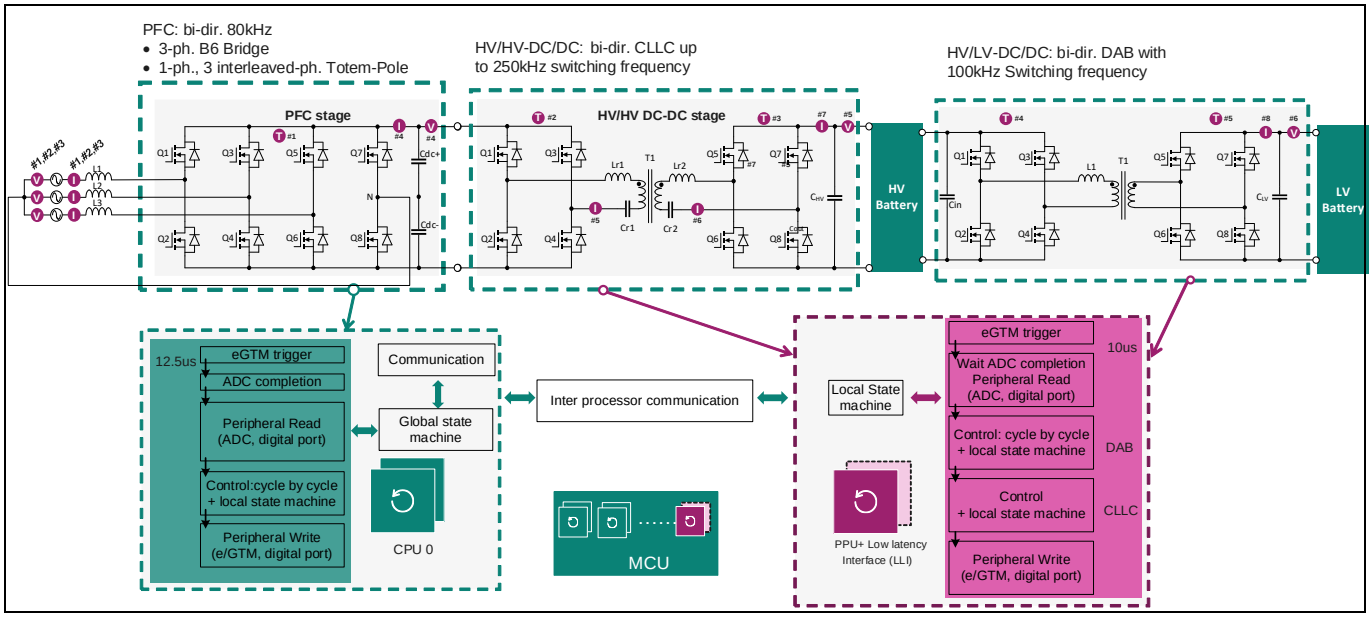

Figure 18 OBC and HV-LV DC-DC converter implementation overview

There are numerous methods available for measuring the execution times of tasks and multiple strategies can be employed to optimize code for achieving the best possible execution times. We will explore various optimization techniques in this chapter.

6.1 Optimization techniques

To attain shorter execution times, a variety of optimization techniques are applied within the model. These techniques include modifying the implementation or adjusting the code generation configuration settings. Additionally, altering the compiler optimization settings can also contribute to improved performance. These methods are outlined in detail below.

- In Matlab®/Simulink® Embedded coder® configuration settings
  - Optimization level option set to “maximize execution speed”
  - Removing unwanted operations/steps from the generated code
  - Inlining the parameters and code as much as possible
  - Selective usage of non-virtual buses, global signal and parameter objects
  - Using the code generation advisor from Simulink®
  - Avoiding the infinite and complex numbers in the generated code when possible
  - Using an efficient C99 language standard
- Simulink® model/modelling method
  - Usage of code friendly math operations and data types
  - Usage of only supported or code-efficient blocks

  - Minimization of redundant operations or redundant usage of blocks
  - Designing the model to smoothly support the vectorization and triggering the code replacement libraries (CRL) on PPU
  - Inlining the reusable C functions to avoid multiple calls/jumps
- Compiler settings
  - Compiler option being set to highest optimization level
  - Usage of tradeoff settings of compiler on TC
- Hardware features
  - Usage of data cache
  - Usage of multiple TMADC successive-approximation-register (SAR) cores

6.2 Code replacement libraries for AURIX™ TC4x™ and PPU

Indigenous CRL for TC named *TriCore_Float_Intrinsic* is developed. This CRL replaces the existing code with the efficient code for absolute, saturate, min, max functions and results in reduced execution time on TC. To activate this library, the custom header file and source file are added to the model path and “custom code” header and source file section of the model configuration settings. Usual modeling approach using the basic blocks such as min, max, abs or saturate from Simulink® library in the model canvas is identified by the MathWorks®/Embedded Coder® code replacement algorithm (CRA). Then, instead of a standard C code, more efficient instructions specified in the source file are added to the final code.

For the PPU, there are 5 CRLs which are available through Matlab®/Simulink® in the latest release of Matlab® (R2024b). Further details on how these libraries can be configured, prioritized using model configuration settings and which functions and data types are supported is available in [7]. In this work, *MetaWare TC4x PPU*, *MetaWare TC4x PPU SIMD* and *MetaWare TC4x PPU Veclib* libraries are used. The aforementioned CRLs support the code replacement for basic math functions such as add, sub, complex math, matrix operations as well as trigonometric functions.

The model should be designed in such a way that MathWorks® CRA identifies the blocks and block paths and replaces them automatically with the prioritized CRLs. The basic constraints are:

- The operations/functions should be vectorized (the higher the vector dimension the better)
- The inputs and outputs should obey the data type and signal complexity
- Avoidance of non-supported (for CRL) blocks altogether or in the path of supported blocks by making use of non-virtual subsystems.

In the context of this work, in two power converters many operations were parallelized and vectorized. Single instruction multiple data (SIMD) CRL tend to be the most efficient followed by the digital signal processing (DSP) library and followed by vector library. The efficiency of CRLs depend on many factors, mainly on the dimension of the vectors that are being used on the supported operations. Hence, it is important to identify the supported operations using the “crviewer” in Simulink® and assigning the most suited CRL the highest priority in the model’s configuration settings.

6.3 Model/software architectures

The AHSP supports code generation and development of embedded software targeting either single core or multicores in homogenous (two or more TCs only) or heterogeneous (minimum one TC and a PPU) architectures. The overview of possible model architecture/code generation hierarchy is shown in Figure 19. For targeting

multiple cores, a multicore homogenous or heterogeneous architecture is used. In this study, keeping the modularity in mind, the models are developed in such a way that application and peripherals layers are separated at the targeted converter level.

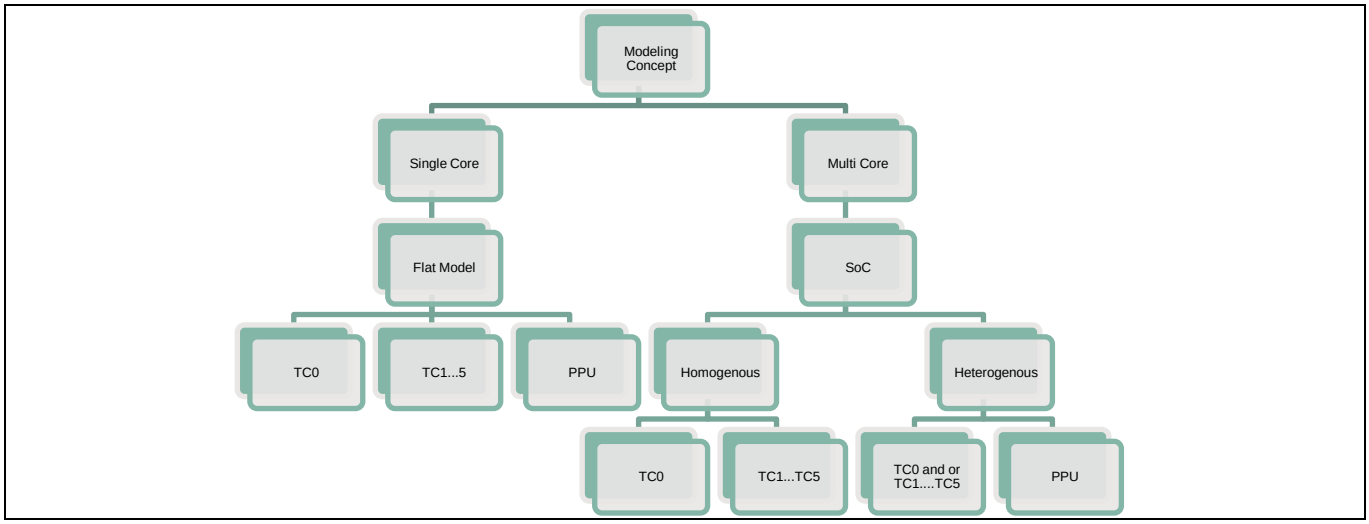

Figure 19 Modeling/Code generation hierarchy

With SoC workflow any core can be targeted independently or in combination with other cores, where the peripheral HW generated events (nested interrupt) are supported for TC and peripheral generated event (polling) is supported for PPU. The TriCore™ 0 is always required to enable the PPU or the other TCs. Implemented multicore architecture using SoC workflow is shown in Figure 20. The model architecture hierarchically consists of three models, namely, 'Top Model', 'Reference Model-1' and 'Reference Model-2'. The top model hosts the two reference models and the associated task managers through which the interrupt or polling tasks are configured. Each reference model has its own configuration set, with which required processing unit is targeted and required application is implemented. To exchange data between the used cores the inter-process data communication (IPC) blocks are used, which use the shared memory between the cores.

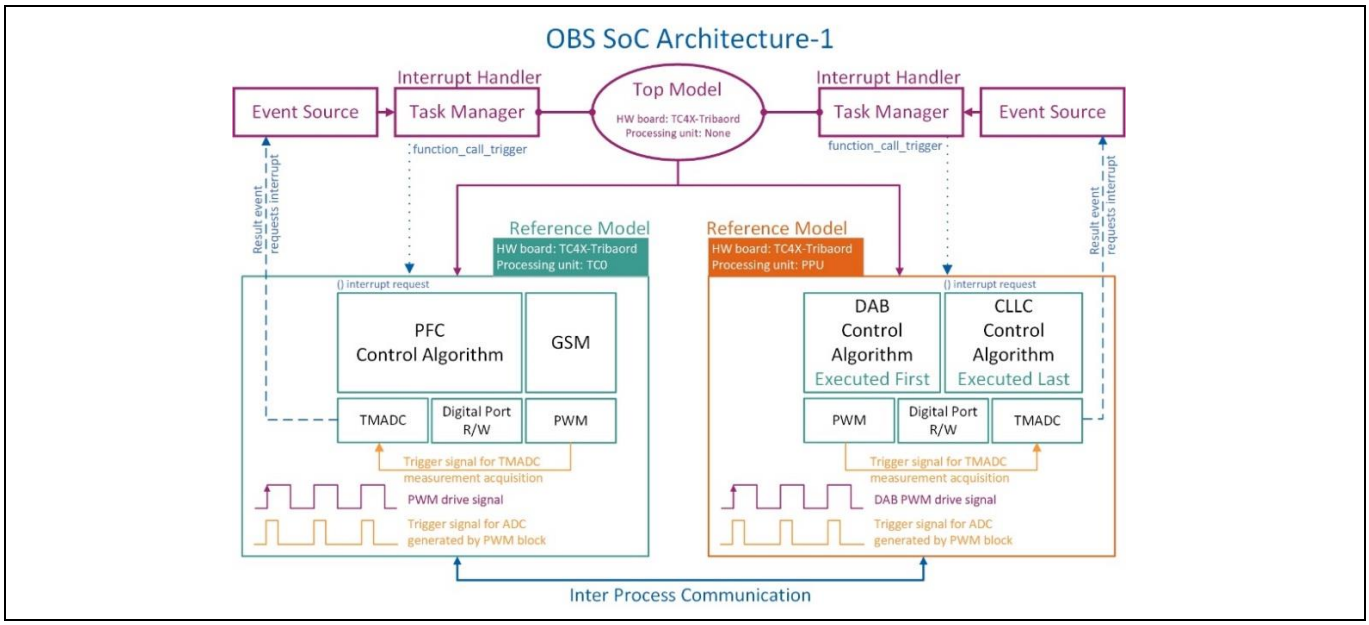

Figure 20 Implemented OBC + HV-LV DC-DC architecture

Implemented 'Top model' overview is shown in Figure 21 and the main components are listed in Table 1. The PFC stage controller is implemented on TriCore™ 0 along with the global state machine (GSM). The PFC stage controller consists of TMADC block to acquire the current, voltage and temperature measurements and two PWM blocks: one to drive the gates of MOSFETs and the other to trigger TMADC to start the analog signal measurement acquisition process. On completion of the result conversion, TMADC produces the result event, and this result event is used to request the interrupt on TC. The GSM monitors the states of all the power converters (PFC, CLLC and DAB) and it generates commands to start/stop individual power converter.

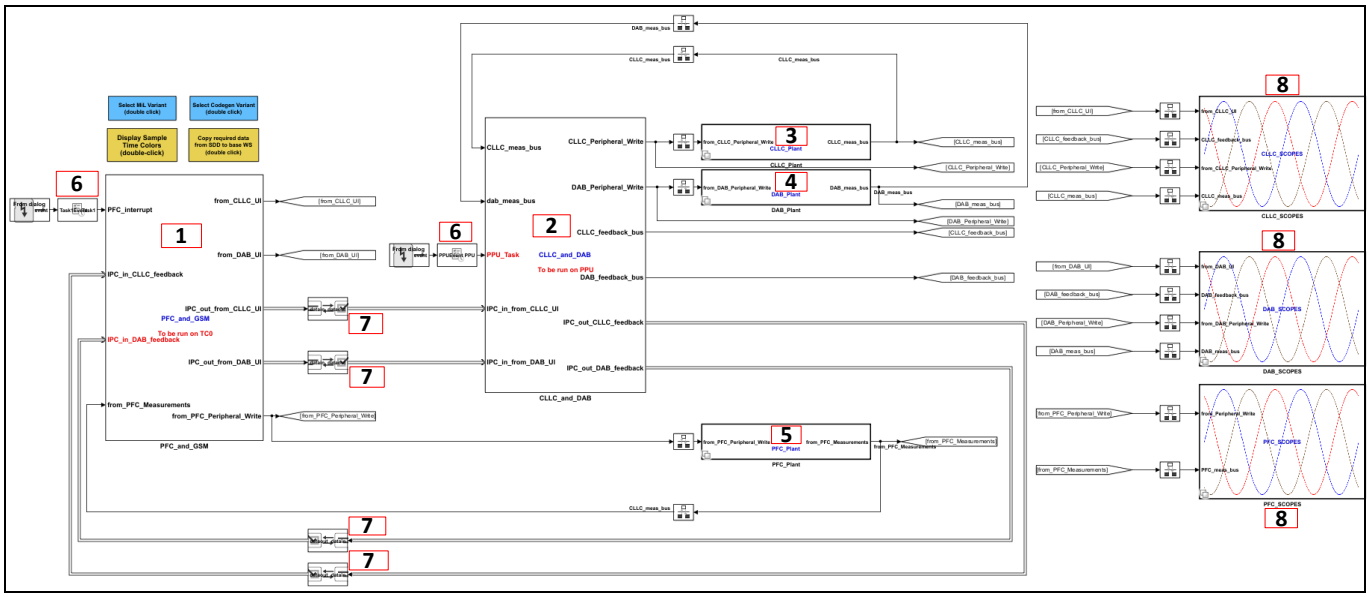

Figure 21 Implemented SoC top model overview

Table 1 OBC top model constituents

1	Model-Ref1 for TC: PFC control logic, GSM, IPC read/write, TMADC, PWM, Local State Machine (LSM)
2	Model-Ref2 for PPU: DAB+CLLC control logic, IPC read write, TMADC, PWM, LSM
3	Plant model of HV-HV DC-DC converter implemented using Simscape®
4	Plant model of HV-LV DC-DC converter implemented using Simscape®
5	Plant model of PFC implemented using Simscape®
6	Task Manager
7	Inter Process Data Communication Channel
8	Scopes for visualization

On PPU, control algorithms for both DAB and CLLC are implemented in a single task, with two different block execution priorities (first and last) [8]. Higher priority is given to the execution of the DAB control loop as compared to the CLLC. The TMADC present in the DAB control loop is triggered by the PWM block running at a fixed frequency (same as switching frequency of DAB), once all measurements for the DAB are done, a result event is produced (periodic in nature) which is used to poll the task on the PPU by means of the task manager or scheduler.

Once the DAB control loop execution is completed, the control loop of the CLLC is also executed within the same result event window produced by the TMADC of the DAB converter. Such a control loop execution (DAB first then CLLC) within the same event is achievable by making sure that within available control period (10 us), the DAB control loop executes as fast as possible. Remainder of the time is allocated to the CLLC control loop, thereby eliminating overlapping or preemption of the execution of the two control loops.

The key difference here is that, in TC the tasks are executed as interrupts (preemption is possible), whereas, on PPU tasks are executed as polled events. The controlled stimuli are:

- For PFC the duty of the PWM signal,
- For DAB inter full-bridge phase shift and
- For CLLC pulse frequency, duty and inter half-bridge phase shift on secondary side for synchronous rectification

Cycle-by-cycle update is achieved by executing the control loops within 12.5 us for PFC (switching frequency 80 kHz) and 10 us for DAB (switching frequency 100 kHz).

For the CLLC, if the operation point lies at or below the 100 kHz frequency, a cycle-by-cycle update is achieved. For above 100 kHz case only a sub-cycle update of the controlled stimuli is possible.

The final integration and HiL testing are carried out using two GUIs. Infineon GUI Designer is used to parametrize, tune and visualize the parameters and signals of AURIX™ TC4x MCU (TC and PPU) as shown in Figure 22. The dSPACE® ControlDesk® is used to parametrize the plant (grid emulation, PFC, CLLC and DAB power converters).

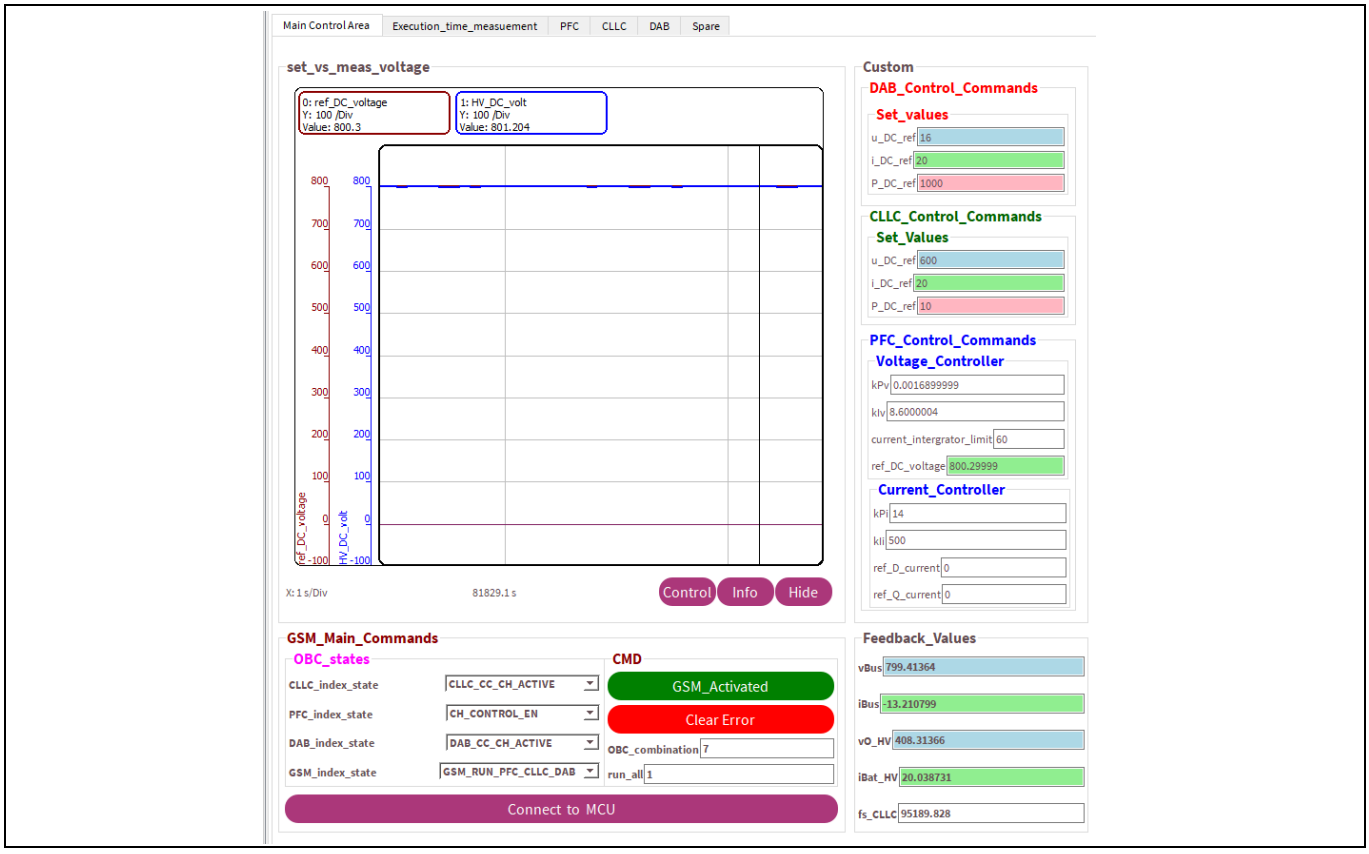

Figure 22 OBC and HV-LV DC-DC converter GUI overview from Infineon GUI Designer

7 Result

In this section the results obtained from the closed loop operation of the OBC and HV-LV DC-DC converter controllers with RTP are presented. Overview of the RTP GUI is shown in Figure 23 and emulated plant conditions are given in Table 2.

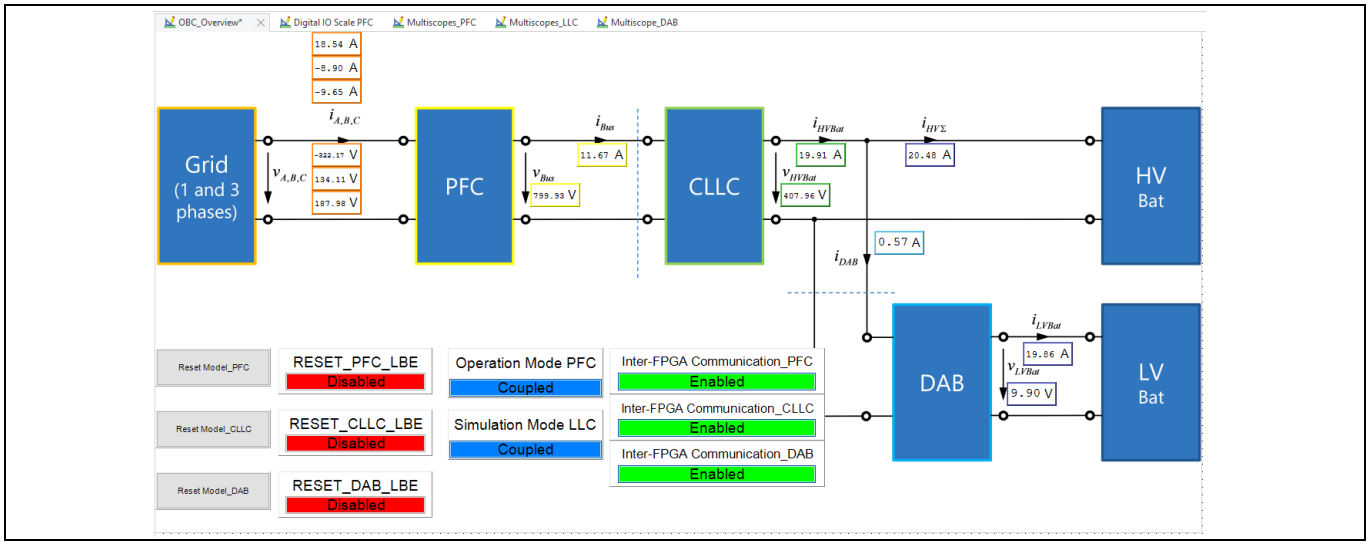

Figure 23 RTP plant model GUI on Control Desk

Table 2 Plant Conditions

Grid	3-ph balanced, 50 Hz, 325 V (peak)
PFC	Coupled to CLLC, Output (V_{Bus}) set voltage: 800 V
CLLC	Coupled to PFC, Constant Current Controlled Charging mode with synchronous rectification (SR), V_{Bat_HV} set to 400 V
DAB	Connected to HV Battery, Constant Current Controlled Charging mode with Synchronous SR, V_{Bat_LV} set to 9.5 V

At the above-mentioned plant conditions, a step change for charging current from 10A to 20A is commanded for OBC as well as HV-LV DC-DC converter and resulting voltages and currents are presented here. Figure 24 shows measured voltages and currents at the input and output of the PFC stage and HV-HV DC-DC converter stage.

From Figure 24 it can be seen that, the PFC is regulating the DC bus voltage at the set 800 V and the AC currents are balanced and are in phase with the AC phase voltages. Despite the step change in load current of the PFC stage, the voltage is well regulated at the set point. Figure 25 shows the v_A and i_A during the step change interval. Here it can be clearly seen that the PFC is operating at a unity power factor as the phase A voltage and current are in phase. The HV battery charging current's magnitude was changed from 10 to 20A with an imposed slew rate, such that overall step change is achieved within 40 ms. The same can be seen in Figure 24, accordingly the HV-HV DC-DC converter's DC output voltage has also changed to accommodate this demand as the battery voltage stays relatively constant at 400 V.

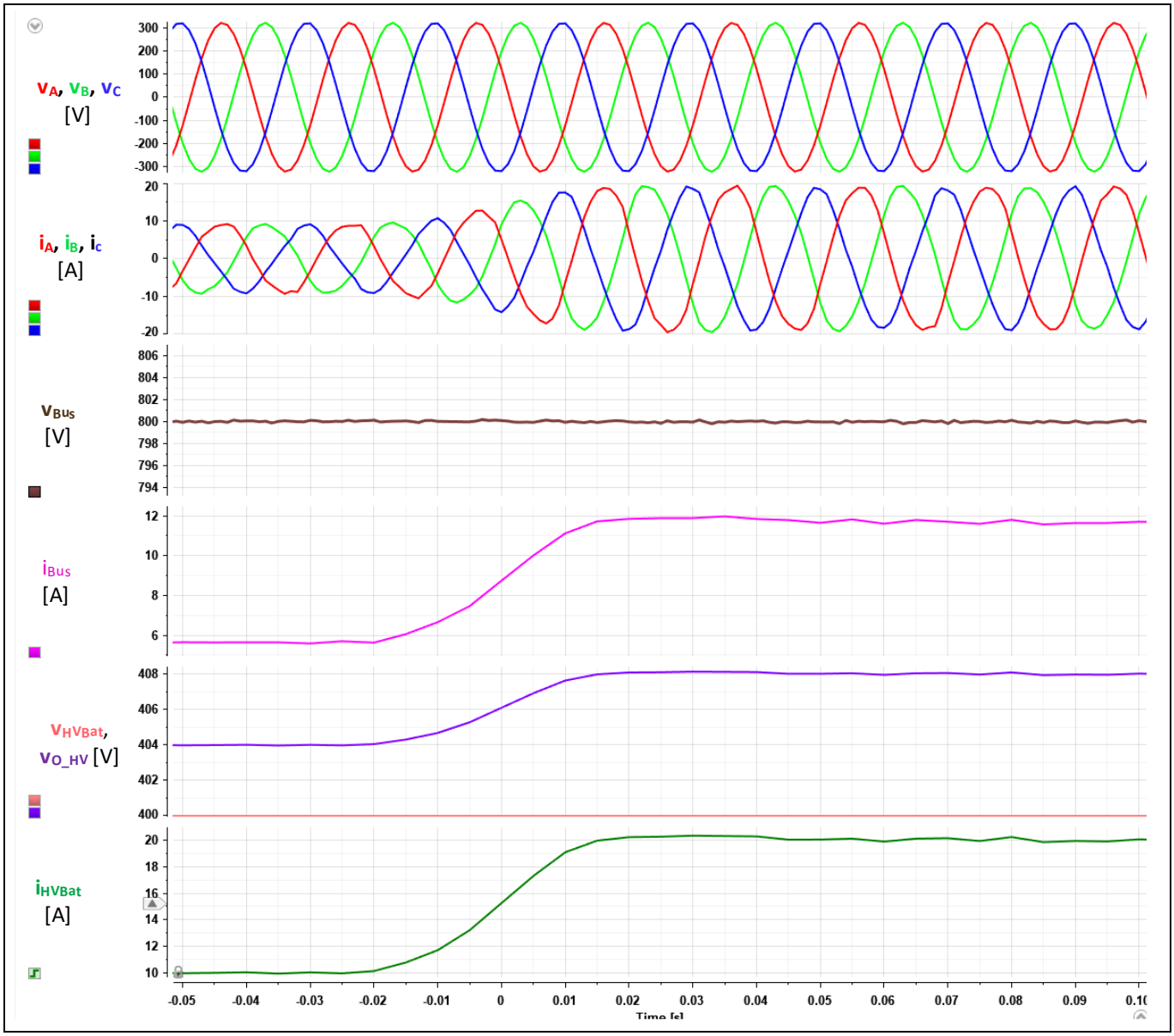

Figure 24 OBC response for a charging current step change from 10A to 20A

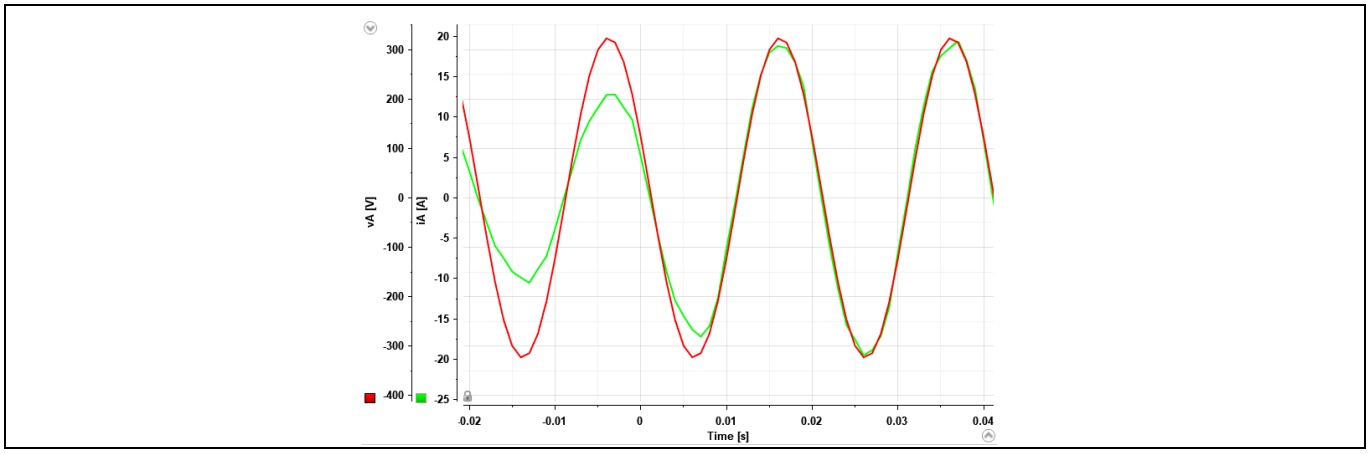

Figure 25 PFC working at unity power factor

Figure 26 shows measured voltages and currents at the HV and LV battery sides. The HV battery is being charged by the CLLC converter with a charging current of 20 A and DAB is charging the LV battery with a charging a current of 10 A. At this instance, the i_{DAB} current is around 0.35 A and the same can be seen reflected in the i_{HV_sigma}. At t = 0 s, the step change in LV battery charging current is commanded and the DAB changes the charging current magnitude to 20 A from the initial 10 A.

Figure 26 shows that the DC bus current has increased as well as the output DC voltage in order to accommodate this increase in the load demand. The DAB controller is able to achieve this step change within couple of milliseconds. From the step response it can be seen that there is an overshoot in both voltage as well as current responses, which is in the accepted controller design criteria and further it can be mitigated by imposing rate limit on the step change.

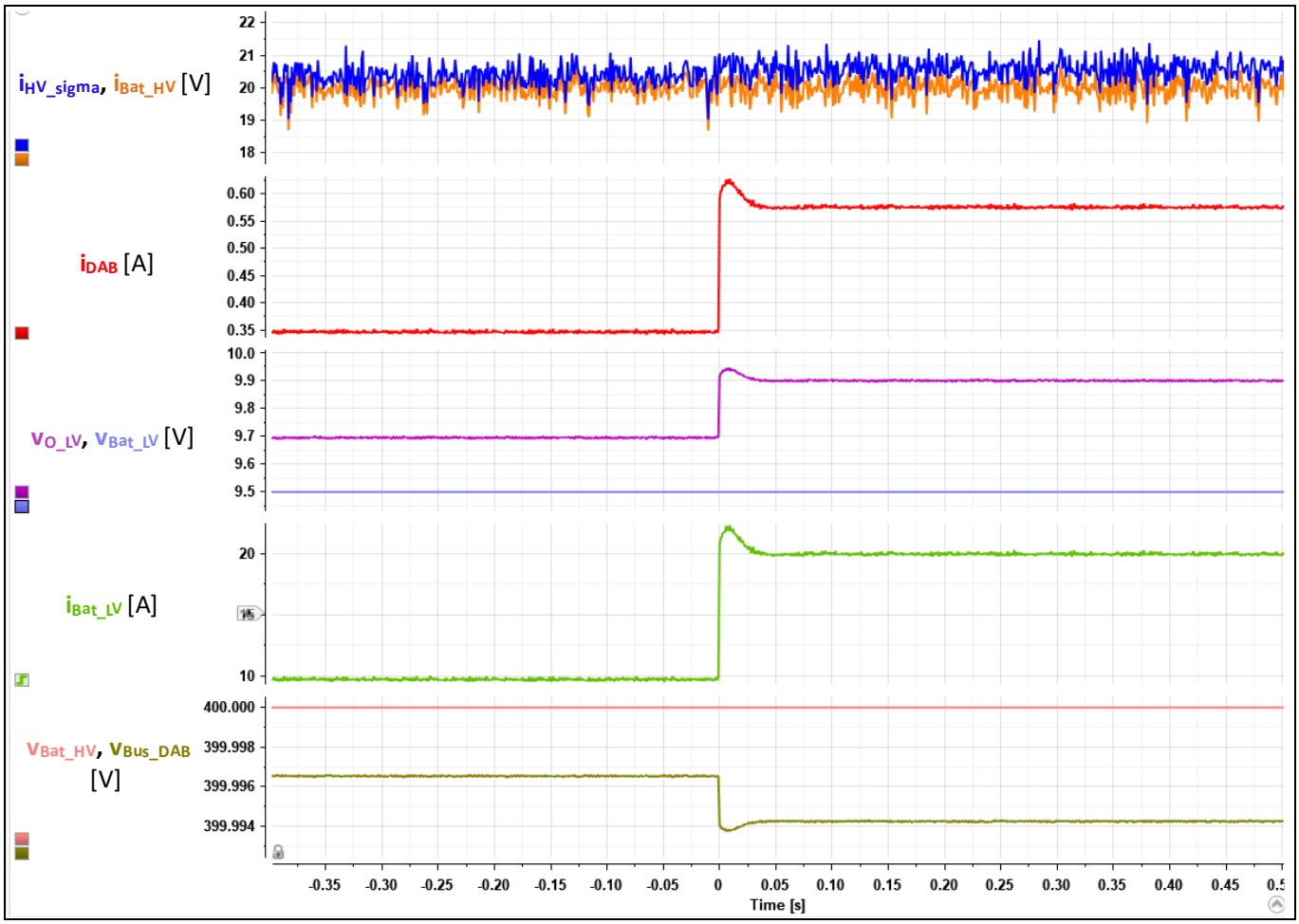

Figure 26 HV-LV DC-DC converter charging response for a step change from 10A to 20A

8 Conclusion and Summary

The goal of the feasibility study was to test the AURIX™ TC4x capabilities. Typically, many of our customers implement only the inner control loops (current) to be of a fast-executing type, while other control loops (voltage) and state machines are designed to be 5-10 times slower. With this feasibility study the needs of developers who are trying to accommodate three fast executing cascaded control loops and state machines in only two cores (one TriCore™ and one PPU) enabling high switching frequencies of power converters are met. As this was a feasibility study, code optimization was not the end goal, but rather to explore various software architectures leveraging AHSP and to show that the implementation of 3 converter control loops on one TriCore™ and one PPU is indeed possible. However, there is a potential for further architecture and code optimizations. This feasibility study has proven that by using latest AURIX™ TC4x, it does not only provide new ideas about OBC/HV-LV DC-DC implementation, but also enables further cost reduction with efficient integration by using single MCU for battery electric vehicles.

The results show that the versatile single AURIX™ TC4x microcontroller can execute all three digital control loops with one TriCore™ and one PPU core, fitting into the application requirements of the OBC and HV-LV DC-DC applications.

Additionally, the model-based design approach enables an ease-of-use method for the design and verification, supported by the RTP system.

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Glossary

AC
alternating current (AC)

AC-DC
alternating current – direct current converter (AC-DC)

ADC
analog-to-digital converter (ADC)

AHSP
AURIX™ Hardware Support Package (AHSP)

ARC
Argonaut RISC core (ARC)

BMS
battery management system (BMS)

BOM
bill of materials (BOM)

B6
three-phase six-switches bridge (B6)

CC
constant current (CC)

CDSP
converter-DSP (CDSP)

CLLC
capacitor-inductor-inductor-capacitor topology (CLLC)

CP
constant power (CP)

CPB
converter peripheral bus (CPB)

CRA
code replacement algorithm (CRA)

CRL
code replacement library (CRL)

CSS
cyber security satellite (CSS)

CSRM
cyber security real-time module (CSRM)

CV
constant voltage (CP)

DAB
dual active bridge topology (DAB)

DAC
digital–to-analog converter (DAC)

DC
direct current (DC)

DC-DC
direct current – direct current converter (DC-DC)

DSADC
delta-sigma ADC (DSADC)

DSEXTMOD
delta-sigma external modulation (DSEXTMOD)

ECU
electronic control unit (ECU)

eGTM
enhanced generic timer module (eGTM)

ENOB
effective number of bits (ENOB)

FCC
fast-compare comparator (FCC)

FPGA
field programmable gate array (FPGA)

FOC
filed-oriented control (FOC)

GUI
graphical user interface (GUI)

GPIO
general-purpose input/output (GPIO)

GSM
global state machine (GSM)

GTM
generic timer module (GTM)

HiL
hardware-in-the-loop (HiL)

HRPWM
high-resolution PWM (HRPWM)

HV
high voltage (HV)

HV-LV
high voltage – low voltage (HV-LV)

HW
hardware (HW)

ISA
instruction set architecture (ISA)

I/O
input/output (I/O)

IPC
inter-process data communication (IPC)

LLI
low latency interface (LLI)

LV
low voltage (LV)

MBD
model-based design (MBD)

MCU
microcontroller (MCU)

MiL
model-in-the-loop (MiL)

OBC
on-board charger (OBC)

PF
power factor (PF)

PFC
power factor correction (PFC)

PiL
processor-in-the-loop (PiL)

PI Controller
proportional-integral controller (PI Controller)

PID Controller
proportional-integral-derivative controller (PID Controller)

PLL
phased-locked-loop (PLL)

PPU
parallel processing unit (PPU)

PWM
pulse width modulation (PWM)

RCP
rapid control prototyping (RCP)

RISC
reduced instruction set computer (RISC)

RT
real-time (RT)

RTP
real-time platform (RTP)

SCU
system control unit (SCU)

SiL
software-in-the-loop (SiL)

SIMD
single instruction multiple data (SIMD)

SNR
signal-to-noise ratio (SNR)

SoC
system-on-chip (SoC)

SR
synchronous rectification (SR)

SVM
space vector modulation (SVM)

SW
software (SW)

TC
TriCore™ (TC)

TMADC
time-multiplexed analog-to-digital converter (TMADC)

VCO
voltage-controlled oscillator (VCO)

VCU
vehicle control unit (VCU)

ZCS
zero current switching (ZCS)

ZVS
zero voltage switching (ZVS)

Revision history

Date	Description of changes
19.02.2025	Initial version

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