Comprehensive electric and thermal evaluation of SiC high-power discrete packages for next generation power supplies

Josef Wildauer[1], Jon Azurza Anderson[1]

[1] Infineon Technologies Austria AG, Villach, Austria

Corresponding author: Josef Wildauer, josef.wildauer@infineon.com

Abstract

In modern power supplies, the use of SiC MOSFETs offers numerous advantages, including faster switching speeds and higher operating temperatures. However, to extract the largest benefit from discrete SiC MOSFETs, power electronics designers require a new understanding of the operating characteristics and their impact on power converter design. This article performs a quantitative and comprehensive electric and thermal evaluation of some of the most popular SiC MOSFET discrete packages, yielding that top-side-cooled devices offer a three-times lower parasitic loop inductance compared to through-hole and bottom-side-cooled devices, while offering an excellent thermal performance.

1 Introduction

To maximize system efficiency and leverage the full potential of SiC MOSFETs, proper electrical and thermal layout design is essential. Close attention has to be payed to system parasitics, and how these are influenced by the cooling. This is of particular importance when high switching speeds (dv/dt) are targeted. Most importantly, the impact from the stray inductances in the power and gate loop have to be minimized, to ensure optimal switching performance, while still complying with the mechanical constraints of the cooling system. While SiC MOSFETs offer notably high switching frequency (typically above 200 kHz), poor layout design can lead to voltage overshoots and associated problems, which might lead to the designer needing to artificially slow down the devices, thus increasing the losses (and the requirements of the cooling).

Top-side cooled (TSC) power packages offer an ideal solution from the system perspective, allowing to decouple the electric path (at the bottom) from the thermal path (through the top). Significant benefit can be therefore obtained by layout optimization and by closing the commutation loop below the devices, due to reduced mutual inductance. Additionally, the cooling system is located on the top side, making it possible to directly mount water cooling or a heatsink on the devices, which can improve heat dissipation [1].

On the other hand, bottom-side cooled power packages have always presented a challenge in finding a balance between thermal vias (or similar concepts, such as copper inlays) and the power loop design. This often requires additional PCB space to achieve the desired thermal performance, and the power loop suffers, as the loop cannot be closed below the device where the vias are placed, but closes around the devices. This last effect leads to more PCB area required, and a worse commutation loop, which can be a limitation.

2 Parasitic Loop Inductances

In this section, the power (or commutation) and gate loop inductances are analyzed in depth. For this purpose, a typical half bridge configuration (operated in double pulse mode) is used to analyze the power loop and gate inductances (**Fig. 1**).

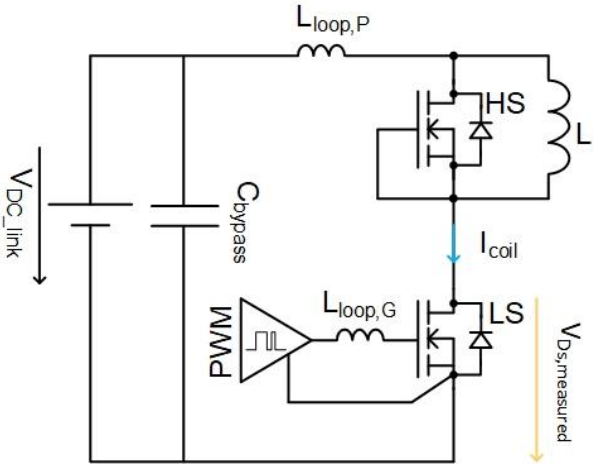


Fig. 1 Double pulse Setup for parasitic analysis.

The first part of the analysis focuses on the power inductance loop ($L_{loop,P}$). This loop comprises the

two SiC MOSFET devices, which handle the high-power operation, the decoupling capacitor (C_{bypass}), and the PCB layout. The power loop inductance has a signification impact on voltage overshoot, switching performance and electromagnetic interference (EMI).
The second part of the analysis focuses on the gate loop inductance ($L_{loop,G}$) of both the high- and low-side SiC MOSFETs. This inductance on the other hand has a large influence on the turn-on and turn-off performance of the SiC MOSFETs.

2.1 Power Loop Parasitic Inductance

The power (or commutation) loop inductance is a sum of parasitic inductances, which include the internal inductances from the power devices, which mainly originate from the bond wires and package, and additionally, it encompasses the inductance from the conductive tracks of the PCB design and the bypass capacitor. Reducing this power loop inductance is crucial for advanced power converters, as it significantly impacts the performance of the switching events. **Fig. 2** shows the schematic of a power switching loop in a half bridge configuration with two SiC MOSFETs, with the power loop inductance.

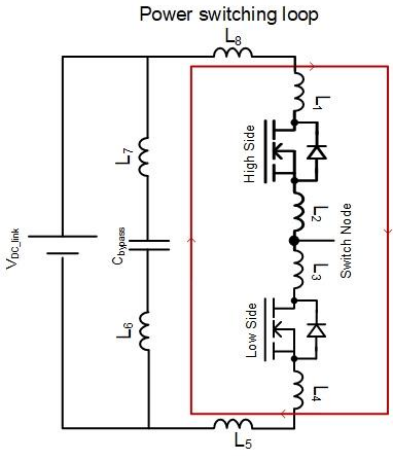


Fig. 2 Power loop parasitic inductances in a half-bridge setup.

2.1.1 Power Loop Design

For an optimal power loop PCB design, it is recommended to use advantage of the mutual inductance by utilizing a return path to reduce the total commutation inductance loop [2]. The magnetic field can be compensated when the field lines cancel each other, i.e., when the current flows in opposite direction in adjacent planes [3].
Fig. 3 presents two different power loop designs, one for the case of a top-side-cooled device, and one for the case of a bottom-side cooled device. For the case of the top-side-cooled device (**Fig. 3(a)**), the MOSFETs are placed as close as possible together, with the DC link decoupling capacitor on the top side (note that this capacitor should be lower in height than the Q-DPAK devices, which is minimum 2.35mm). To minimize power loop inductance, the return path is designed to follow the path of least magnetic resistance possible, which means going directly under the devices in the second PCB layer. In this case, the segment of the inductance is a sum of partial inductance, minus the effect of mutual inductance (**Eq. 1**).

On the other hand, for the bottom-side cooling devices (**Fig. 3(b)**), to design the return path directly under devices is not possible without a large compromise on the cooling capabilities, because the area on the opposite is used for cooling. In this case, the return path is routed back next to the devices. Consequently, the loop inductance is the sum of all parasitic inductances, as the mutual inductance is, to a practical effect, is insubstantial (**Eq. 2**).

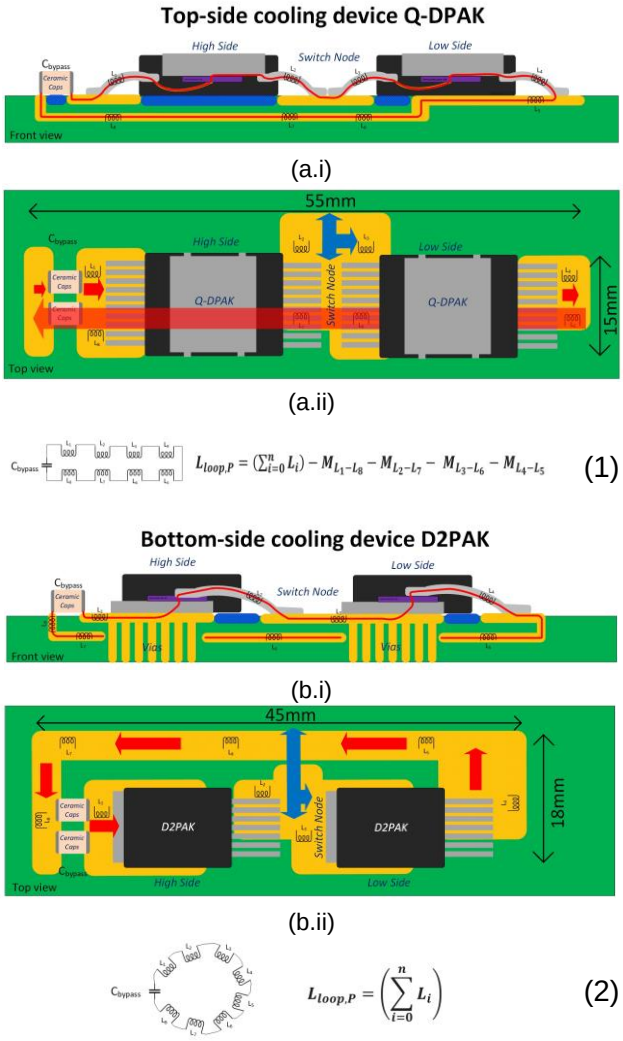


Fig. 3 Power loop design: top-side cooling device from (a.i) the side, and (a.ii) and top, and bottom-side cooling device from the (b.i) side, and (b.ii) top.

2.1.2 Multiphysics parasitic extraction of the power loop inductance

This section presents the results of the power loop inductance extraction conducted using 3D Finite Element Analysis (Ansys Q3D) for various discrete package solutions. **Fig. 4** shows the different types of package analyzed for the power loop inductance. All simulations utilize a half bridge design and all parasitic inductances were extracted at frequency of 100 MHz. For the bottom side cooling devices, the cooling area is located beneath the device, and hence, the PCB routing follows the approach shown in **Fig. 3(b)**.

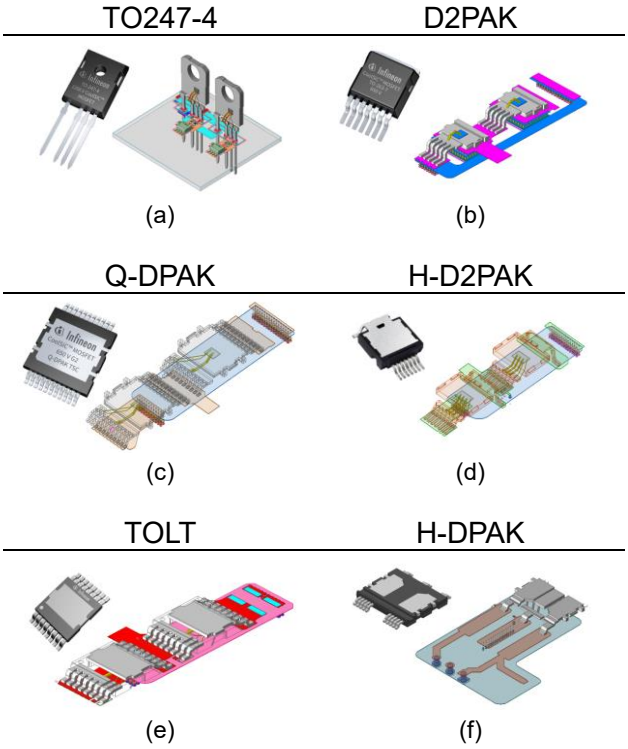


Fig. 4 Different power loop design by packages: a) TO247-4, b) D2PAK, c) Q-DPAK, d) H-D2PAK, e) TOLT, f) H-DPAK.

The first package is the through-hole package TO247-4, which is mainly used in perpendicular, resulting in an orthogonal current path, which makes it impossible to reduce mutual inductance beyond a certain degree. The next one is the D2PAK. In this case, the balancing between the cooling and layout design is challenging (**Fig. 3(b)**). This layout design uses the vias trough the PCB to cool device and the power path returns next to the device. In this case, the reduction of parasitic loop inductance by leveraging the mutual inductance is not effectively achieved. The next four packages are top-side-cooled devices. In these cases, the cooling occurs through the top-side, and the return path is directly under the device. From a package design perspective, the Q-DPAK and TOLT packages possess a more natural and symmetric current path, unlike the H-D2PAK package, where the current is on the drain tab forced to the sides. The last package is the H-DPAK. This is an integrated half bridge device containing two SiC MOSFETs within one package. In this case, the loop inductance can be optimized through chip design [4].

Another important factor impacting parasitic inductance is the number of bond wires from the die to the package leads. **Fig. 5** presents the Q-DPAK package with a different bond wire design (L_{DS} – package parasitic inductance from Drain to Source). In this case, a second bond wire reduces parasitic inductance by around 7%. Ultimately, this involves a compromise in technical mounting for small dies, as the SiC MOSFET die for higher ohmic devices becomes very small, making the technical mounting of additional bond wires not always feasible. Moreover, optimal chip positioning is a very challenging task. However, placing the chip as close as possible to the source pins can reduce the length of the bond wires, which particularly impacts the gate design, as it allows for the reduction of both the kelvin source and the gate wire parasitic inductances. The critical task here is to position the chip in such a way that it effectively transfers heat to the case, avoids isolation issues at the corners, and complies with production rules.

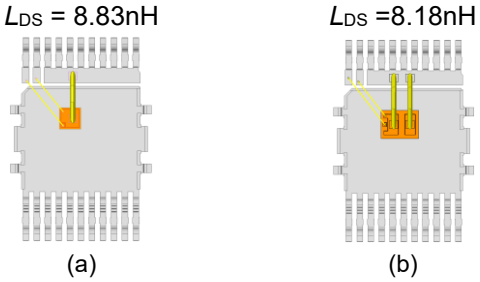
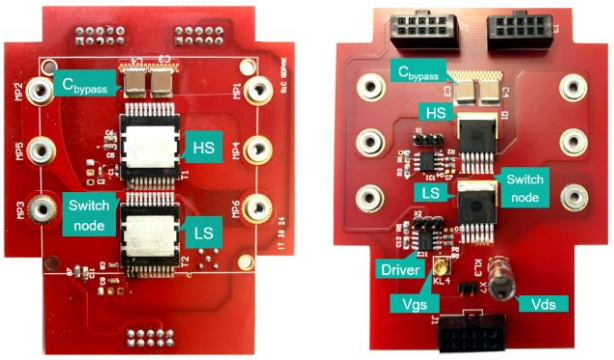


Fig. 5 Q-DPAK package layout for: (a) one source bond wire, and (b) two source bond wires, with a reduction of parasitic inductance on package level (L_{DS}).

2.1.3 Experimental Validation

To validate the parasitic extraction results, an experimental setup was constructed. The same PCB design with a half-bridge configuration that was used for the parasitic inductance extraction was used to experimentally validate the results, as shown in **Fig. 6** for the Q-DPAK and D2PAK. Similar PCBs were built for the rest of the packages. For this purpose, the half-bridge is operated in standard double pulse mode, with the high side SiC MOSFET functioning in diode mode. An air coil was connected parallel to the high-side device, like in **Fig. 1**. During first pulse, the low-side SiC MOSFET is switched on, and the inductor coil is

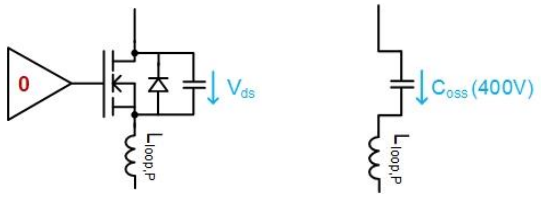
charged to a predetermined current level. After this period, the low-side SiC MOSFET is switched off. The turn-off event is employed to measure the power loop inductance, as when the SiC MOSFET turns off, the power loop inductance resonates with the C_{oss} of the switched off SiC MOSFET.



(a) (b)

Fig. 6 Test hardware for power loop inductance: (a) top-side-cooled Q-DPAK, and (b), bottom-side-cooled D2PAK.

Here, there are two things that have to be considered. Firstly, since the C_{oss} of the SiC MOSFET is non-linear, care has to be taken to use the C_{oss} at the right voltage for the calculation. As when the resonance occurs, the device is in off state, the value of the C_{oss} at the DC-link voltage (or blocking voltage, in this case) has to be considered, as shown in **Fig. 7**. With the turn-off waveforms taken on the D2PAK as an example in **Fig. 8**, since the blocking voltage is 400V, the C_{oss} has to be considered at 400V, i.e., C_{oss}(400V).



(a) (b)

Fig. 7 State of SiC MOSFET during the turn off: (a) SiC MOSFET circuit diagram, and (b), simplified equivalent circuit diagram.

Secondly, other capacitances that appear parallel to the C_{oss} of the switch have to be considered, as they can also affect the switching behavior. Most importantly, the parasitic capacitance of the PCB, C_{PCB}, has to be considered. This capacitance arises in the PCB between the copper planes of the switch node and the plane that is closing the commutation loop, which is shown in **Fig. 9**. This capacitance is the outcome of a trade-off in the PCB layout between $L_{loop,P}$ and C_{PCB}, i.e., to minimize the commutation loop inductance by routing it in a wide plane below the devices in the second layer, you inevitably increase the parasitic capacitance contribution of the PCB.

To calculate C_{PCB}, we assume that the copper planes on the PCB form a plate capacitor when simplified to the first order (**Eq. 3**).

$$C_{\mathrm{PCB}} = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{3}$$

The parameters for the estimation of the parasitic capacitance in the, e.g., D2PAK board, are given by:

$$\varepsilon_0 = 8.86e^{-15} \frac{\mathrm{As}}{\mathrm{V \cdot mm}};$$
$$\varepsilon_r = 4.6 \ (\mathrm{FR4\ material});$$
$$A_{D2PAK} = 65.3\ \mathrm{mm}^2\ ;$$
$$d = 0.127\ \mathrm{mm}.$$

C_{PCB} is in the range from smallest value of 10pF TO247-4, to the largest value of 21pF for D2PAK, which is an order of magnitude smaller than the C_{oss}(400V) of typical SiC MOSFETs. Hence, this shows, that for SiC MOSFETs in the 650 V / 750 V range, the parasitic PCB capacitance is a drawback that can be tolerated to reduce the parasitic loop inductance, particularly when it comes to hard-switched applications.

Note that there can also be other capacitances parallel to C_{PCB}, like the air core inductor inter-winding capacitance or the high-voltage probe capacitance, but these are lower than the C_{PCB} and can therefore be safely neglected for the purpose of this calculation.

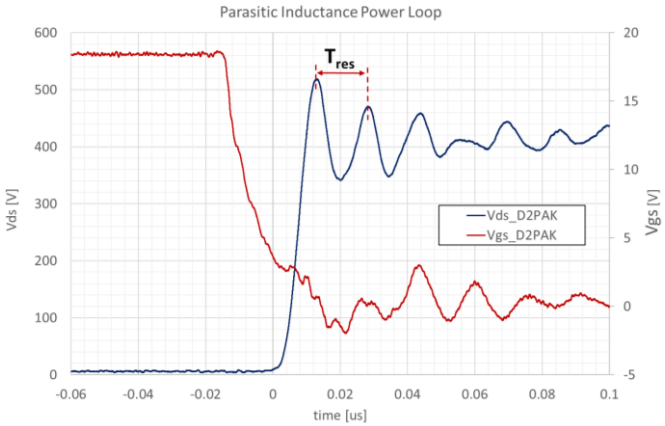


Fig. 8 Turn-off oscillation from SiC MOSFET (IMBG65R048M1H). Here, T_{res} = 13.5 ns, f_{res} =74 MHz, and C_{oss}(400V) = 129 pF.

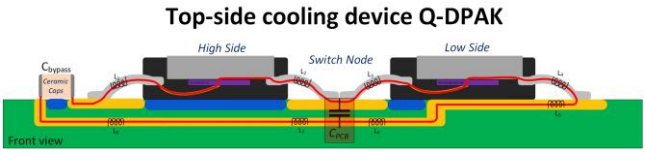


Fig. 9 Board capacity by switch node C_{PCB}.

Therefore, to calculate the parasitic loop inductance, the oscillation period arising at the turn off event must be measured (**Eq. 4**):

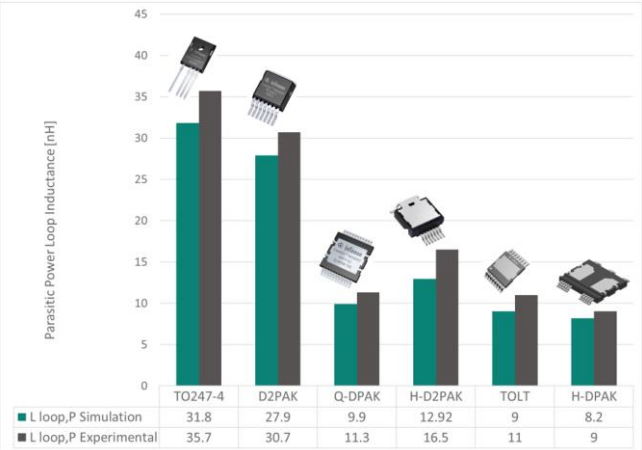
$$L_{\text{loop}} = \frac{\left(\frac{T_{\text{res}}}{2 \cdot \pi}\right)^2}{C_{\text{oss}} + C_{\text{PCB}}}, \qquad (4)$$

Where Tres is the period of the resonance, and the resonance frequency is given by $f_{res}=1/T_{res}$.

Following the D2PAK example, **Eq. 5** calculates the power loop inductance ($L_{loop,P}$) from the Bottom-Side Cooling "D2PAK" design,

$$L_{\text{loop,P,D2PAK}} = \frac{\left(\frac{13.5\ \text{ns}}{2 \cdot \pi}\right)^2}{129\ \text{pF} + 21\ \text{pF}} = 30.7\ \text{nH}. \qquad (5)$$

Fig. 10 presents the results for the power loop inductance with different packages. The D2PAK and TO247-4 exhibit the highest inductance values due to their design and package configuration. Top-side cooling devices are all in a similar range, where the H-DPAK, with the integrated half bridge, shows the best performance. The difference between the parasitic extraction and the measurements is minor, which leads to a large confidence in the values of the parasitic extraction.



	TO247-4	D2PAK	Q-DPAK	H-D2PAK	TOLT	H-DPAK
L loop,P Simulation	31.8	27.9	9.9	12.92	9	8.2
L loop,P Experimental	35.7	30.7	11.3	16.5	11	9

Fig. 10 Comparison of the power loop inductance values for different power packages.

Fig. 11 shows the impact of a larger parasitic loop inductance for different packages at turn-off for a current of 23A for SiC MOSFETs of similar R_{DSon} around $48m\Omega_{typ}$ at 25ºC. The TO247-4 has a higher overshoot compared to a similar SiC MOSFET in a D2PAK, and particularly, when compared to the Q-DPAK package. There are different methods to reduce the overshoot, the most prominent one being to slow down the switching speed (dv/dt) by increasing the gate resistor, but at the cost of increasing the switching losses. Therefore, driving this package with a higher switching frequency is more challenging compared to a Q-DPAK device. The D2PAK shows parasitic inductance levels that fall in between these two extremes, however, the challenge with the D2PAK is to achieve a good cooling performance. The TOLT and H-D2PAK also benefit by the design from a top-side cooling device design with small difference in the package size and design of the drain connection. In this last case, both chips of the half bridge are housed within a single package, minimizing the power loop inductance as much as possible.

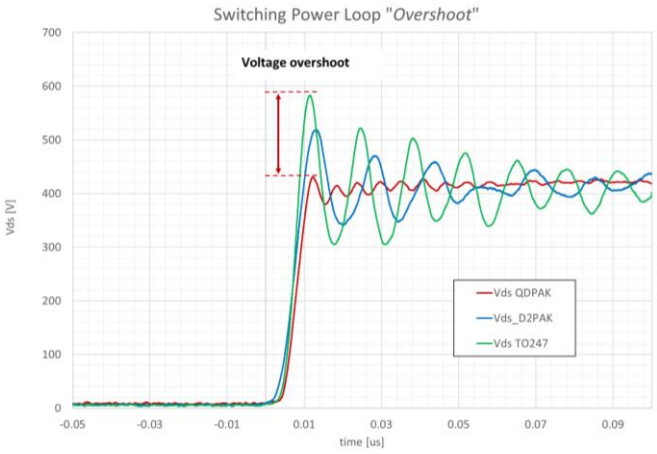


Fig. 11 Impact of parasitic power loop inductance for a turn off a current of 23A for all curves. For all cases, the external $R_{g,off}$ is 1Ω.

2.2 Gate Loop Inductance

In this section, the analysis of the gate loop inductance is presented. **Fig. 12** shows the parasitic gate loops, where L1, L2 and L3 can be lumped together as the high-side gate loop inductance, and L4, L5 and L6 can be lumped together as the low-side gate loop inductance.

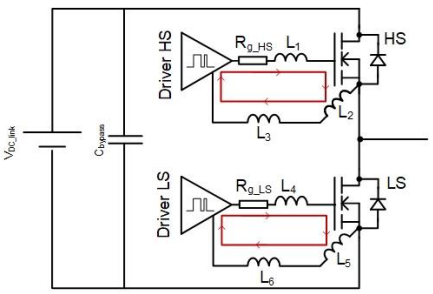
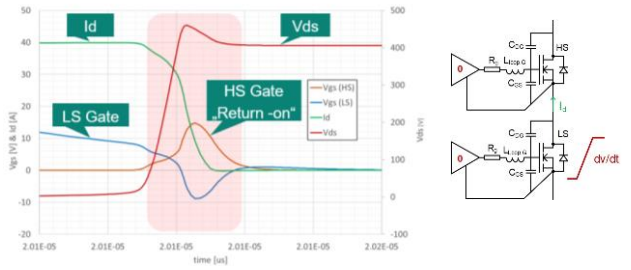


Fig. 12 Schematic of the gate loop inductance.

This is an important topic for investigation because of two risk factors, both occurring in the MOSFET of the half-bridge that is acting as the synchronous rectification device [6].
The first risk factor is, shown in **Fig. 13 (a)** for the low side device, that at a hard-switching event with a high turn-on dv/dt on the high-side device, the opposite (low-side, in this case) SiC MOSFET can experience a return-on (also known as parasitic turn-on or spurious turn-on). A return-on can cause several issues in the application, that can range from increased switching losses, up until destruction of the device.
The second risk factor concerning the gate loop parasitic effects is, that under conditions of a high turn-off dv/dt of the high-side, like shown in **Fig. 13(b)**, an undershoot can be generated in the opposite (low-side) device, which is still turned-off. This phenomenon pulls the gate voltage of the opposite device down, such that in high dv/dt conditions, it can violate minimum gate-source voltage datasheet specifications.
In order to mitigate these two risk factors, it is of paramount importance to reduce the gate loop inductance as much as possible, by having a good PCB layout.



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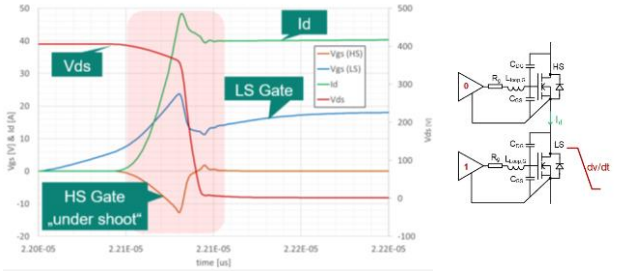
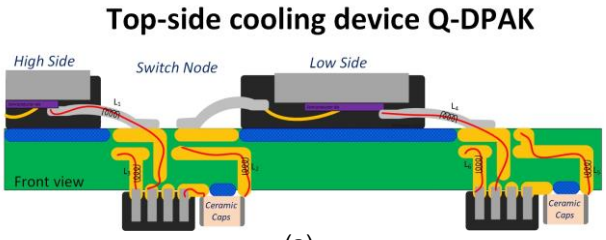


(b)

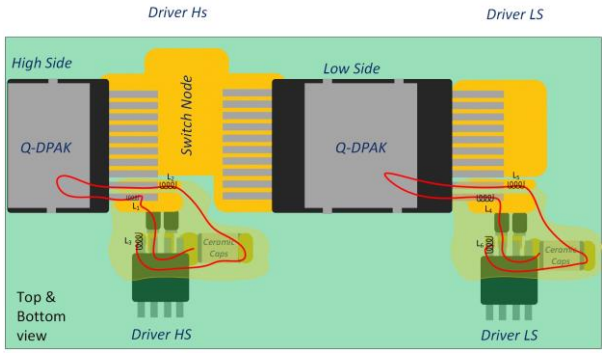
Fig. 13 Simulation from a critical impact of gate loop parasitic on a “synchronous mode” SiC MOSFET, for (a) high voltage rise speed (dv/dt) of the low-side device caused by a hard-turn-on of the high-side that causes a spike on the gate-source voltage of the low-side leading to a return-on, and (b) high voltage fall speed (dv/dt) of the low-side device caused by a high-current high-side device turn-off that causes a negative voltage spike on the gate-source voltage.

2.2.1 Gate loop design

Three guidelines are recommended for the gate loop design. Firstly, the switch node and the power path, if possible, should not be directly under the gate driver in order to preserve signal integrity [4]. Second, the Kelvin source (KS) pin should be used as the reference (or ground) of the gate driving circuit, as this separated pin does not carry high current and thus decouples the effect of the di/dt of the load current on the gate [5]. Finally, an important guideline is to have a plane connected to the KS as the “ground” of the gate driver circuit covering the whole gate driving circuit, that has the purpose of (a) shielding the gate signal, and (b) reducing the parasitic gate loop inductance. **Fig. 14** shows the gate loop design for a top-side cooling device.



(a)



(b)

Fig. 14 Gate loop design for Q-DPAK, shown from (a) the side view, and (b), the top view.

2.2.2 Multiphysics parasitic extraction of the gate loop inductance

The gate loop inductance of the different packages was again analyzed using 3D Finite Analysis (**Fig. 15**). For the TO247-4 and D2PAK devices, the gate driver is placed on the top side of the PCB, in the case of the latter due to the device cooling area. For the top-side-cooled devices, it is placed on the opposite side. The gate driver is positioned as close as possible to the gate pin, and the return path from the KS is under the gate path to reduce the gate parasitic inductance.

2.2.3 Experimental Validation

A double pulse setup was employed, following a similar procedure as described in the previous chapter. However, for this experiment, the DC link voltage was not applied. Only the gate drive circuit was powered, requiring it to charge or discharge the input capacitor C_{iss}. **Fig. 16** shows a simple schematic of the gate driver circuit. The input capacitance, C_{iss}, is a sum of Gate-Drain capacitance C_{GD} and Gate-Source capacitance C_{GS}, ($C_{iss} = C_{DG} + C_{GS}$).

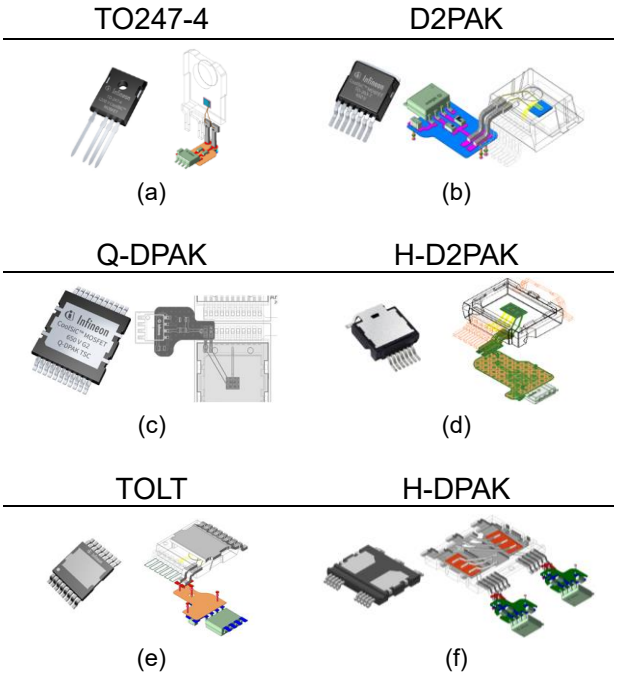


Fig. 15 Different gate loop design by packages: (a) TO247-4, (b) D2PAK, (c) Q-DPAK, (d) H-D2PAK, (e) TOLT, (f) H-DPAK.

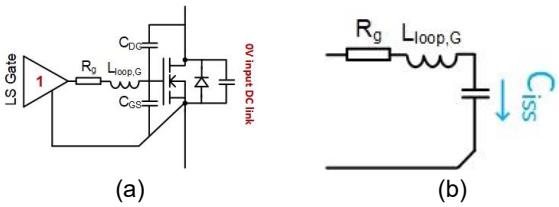


Fig. 16 State of the gate driving circuit at turn-on (a) SiC MOSFET circuit diagram, (b) simplified equivalent circuit diagram.

Fig. 17 shows the oscillation of the gate loop during a turn-on event of a TO247-4 SiC MOSFET without DC link voltage. The oscillation is very small, and hence, only half a period of the resonance is used for the analysis. Moreover, there is a certain error that comes from the interpretation of the peaks of the curve, but as showed for the commutation loop inductance parasitic extractions, we have a high confidence in the simulated values. The gate loop inductance was calculated using **Eq. 4**, replacing C_{oss} with C_{iss}, and without considering C_{pcb}, as with C_{iss} >> C_{pcb}, any parasitic capacitance contribution can be safely neglected.

Eq. 6 calculates the gate loop inductance ($L_{loop,G}$) from the TO247-4 package design.

$$L_{loop,G,TO247-4} = \frac{\left(\frac{25\ \text{ns}}{2 \cdot \pi}\right)^2}{800\ \text{pF}} = 19.8\ \text{nH} \qquad (6)$$

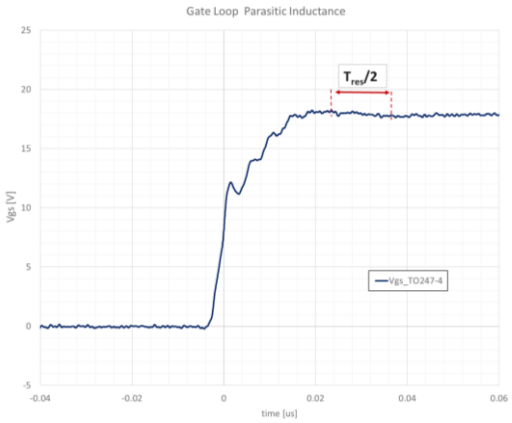
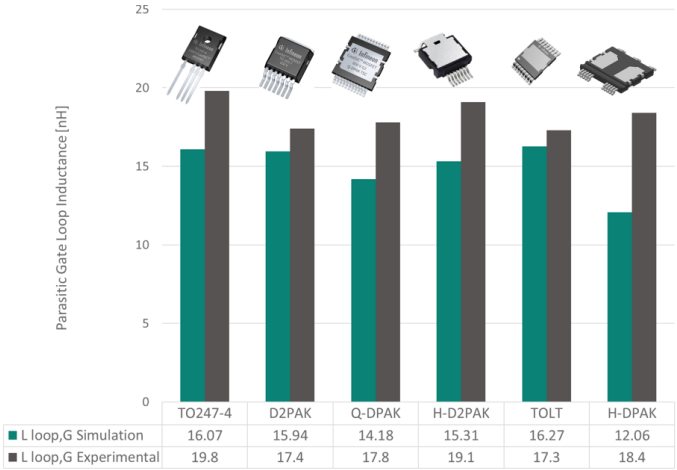


Fig. 17 Turn-on oscillation from gate loop, SiC-MOSFET (AIMZA75R060M1). In this curve, T_{res} = 25ns and f_{res} = 40 MHz, and C_{iss} = 800pF.

The results from the simulation and experimental analysis are presented in **Fig. 18**. Generally, the difference between the packages is smaller than for the case of the commutation loop inductance, because the driver concept and chip bonding are similar across all packages, i.e., one bond wire for the gate connection, and one bond wire for the kelvin source. In general, all the gate loop inductances are around $L_{loop,G}$ ≈ 15 nH, as long as the gate loop is correctly routed on the PCB.



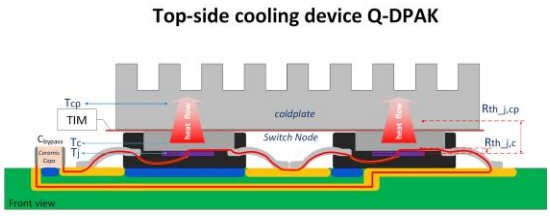
	TO247-4	D2PAK	Q-DPAK	H-D2PAK	TOLT	H-DPAK
L loop,G Simulation	16.07	15.94	14.18	15.31	16.27	12.06
L loop,G Experimental	19.8	17.4	17.8	19.1	17.3	18.4

Fig. 18 Comparison of gate loop inductances for different power packages.

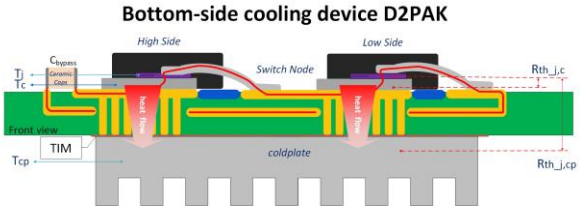
3 Thermal Behaviour

Another significant challenge of power converter design is the device cooling. When combined, an optimized power loop and thermal design, can lead to an increase in efficiency as the devices operate at a lower operation junction temperature [7].

To evaluate the thermal management of the analyzed power packages, a dedicated thermal measurement setup is used for investigations. **Fig. 19** illustrates the employed setup for top- and bottom-side cooling configuration, both of which are typical in real application use. In the top-side cooled configuration, cf., **Fig. 19(a)**, the lead frame is positioned on the top, and a heatsink or water-cooling system is connected to it, separated by a thermal isolation material (TIM), which is positioned between the device and heatsink [8]. For bottom-side cooled devices, cf., **Fig. 19(b)**, the heatsink is placed on the bottom, and the heat flow occurs through the PCB, where a TIM is also placed between the PCB and the heatsink.



(a)



(b)

Fig. 19 Thermal concept for (a) top-side cooling & (b) bottom side cooling device.

3.1 Thermal Simulation

To evaluate the heat flow with different TIM configurations, a simulation was conducted using a SiC MOSFET in a Q-DPAK package.
In steady-state operation, a specific power level is set, causing the device to heat up due to the internal resistance (R_{DSon}). **Fig. 20** depicts a thermal simulation of a Q-DPAK package, illustrating the different temperature states and the thermal resistances between the various materials. The primary challenge lies in achieving a good contact interface between the device and the heatsink or cold-plate, as the isolation material typically exhibits its poor thermal conductivity. The next challenge is to position the device as close as possible to the heatsink without violating the minimum distance required for high voltage clearance.

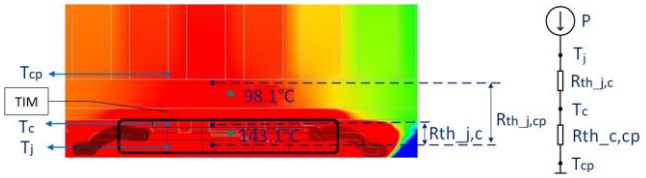


Fig. 20 Thermal Simulation of a SiC MOSFET die in a Q-DPAK.

Eq. 7 presents the calculation for the thermal resistance between the device and the heatsink or cold-plate ($R_{th\_j,cp}$).

$$R_{th_j,cp} = \frac{T_j - T_{cp}}{P} \tag{7}$$

In the simulation, a TIM with thermal conductivity of 1 W/m·K and a thickness of 1 mm was used. At nearly maximum power for this setup, with an R_{DSon} of 40 mΩ and a current of 15 A, the simulation yielded the following thermal resistance $R_{th\_j,cp}$ (**Eqs. 8 & 9**).

$$P = R_{dson} * I^2 = 0.04 * 15^2 = 9W \tag{8}$$

$$R_{th_j,cp} = \frac{143.1 - 98.1}{9} = 5.0\,\frac{K}{W} \tag{9}$$

To increase the power density, one potential approach is to either reduce the R_{DSon}, or to invest in improving the thermal stack.
Table 1 provides a comparison of different thermal stacks from the simulation setup. Various possibilities for thermal management are explored, such as using a TIM with better thermal conductivity or optimizing the distance between the heatsink and the device.

TIM [W/mK]	Thickness [mm]	$R_{th\_j,cp}$ [K/W]	P [W]
1	1.0	5.0	9
3	1.0	3.3	23
5	0.5	1.9	38

Table 1 Thermal stack comparison.

The inclusion of a fan or water-cooling system must be evaluated to optimize the thermal performance of the system. Ultimately, the simulation demonstrates the critical importance of thermal performance for modern power supplies, highlighting the necessity of investigating the thermal stack to achieve high power density.

3.2 Experimental Validation

In the experimental validation, different power packages with their according thermal stacks were realized. A typical stack configuration included a TIM with a thermal conductivity of 3 W/m·K and a thickness of 1 mm [9]. A current source was used to set the power level, and the device was operated in a steady-state mode with current flowing from source to drain (i.e., in 3rd quadrant operation). The diode voltage, which serves as an indicator of the chip temperature, was measured after the heatsink reached a temperature of 70°C. **Fig. 21** illustrates the experimental setup.

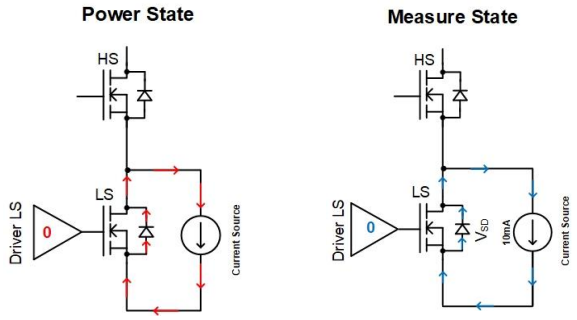


Fig. 21 Thermal measurement setup: (a) power state operated in steady-state mode (b) measure state with diode voltage measurement.

Prior to the experimental validation, the SiC MOSFET was calibrated at different temperature levels. During this calibration, the diode voltage drop was measured at a current of 10 mA, as shown in **Fig. 22**.

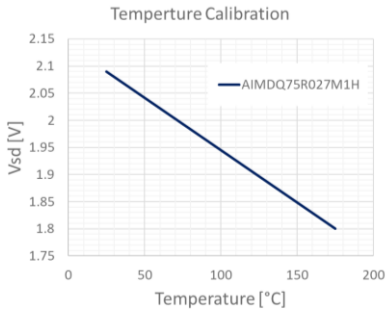


Fig. 22 SiC MOSFET temperature calibration for (AIMDQ75R027M1H).

Fig. 23 illustrates the thermal stack setup. In all cases the aforementioned TIM was placed between the device and the heatsink. A thermal camera was used to measure the temperature on the heatsink which is assured to be homogeneous in steady state. The size of the heatsink was the same for all packages.

This measurement was conducted for various types of packages within the same R_{DSon} class, approximately 27mΩ, to evaluate their thermal performance. **Fig. 24** presents a comparison of the thermal resistances for the various packages.

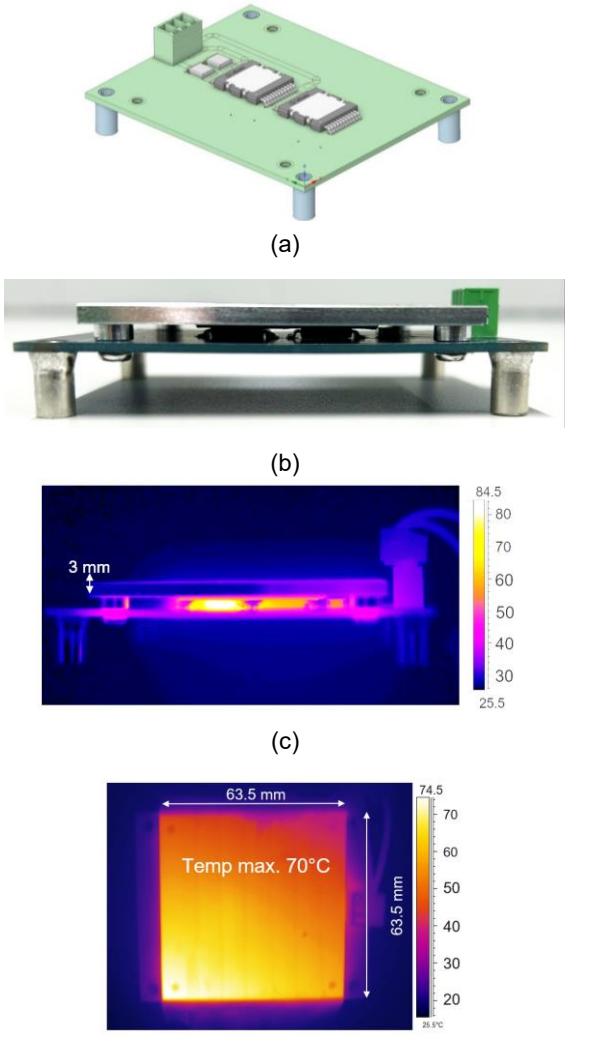


Fig. 23 Thermal measurement setup: (a) PCB used for the measurements, (b) side view of the setup, (c) side view with the thermal camera, and (d) top view with the thermal camera.

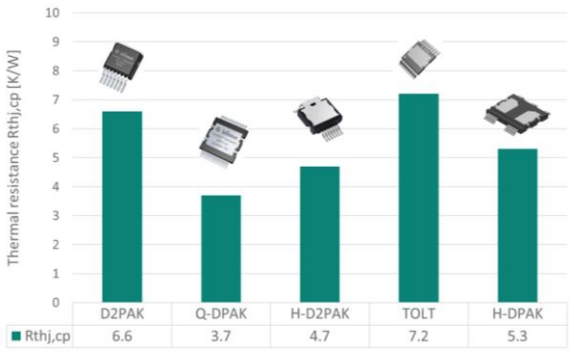


Fig. 24 Experimental thermal resistance values for the different packages with a TIM of 3 W/m·K & 1mm thickness. Note that for the H-DPAK, the power is per device of the half-bridge.

Fig. 25 presents the maximum power dissipation for the different power packages with the thermal stack from the experiment, assuming a cold-plate cooled at 65ºC, and a junction temperature of 130ºC.

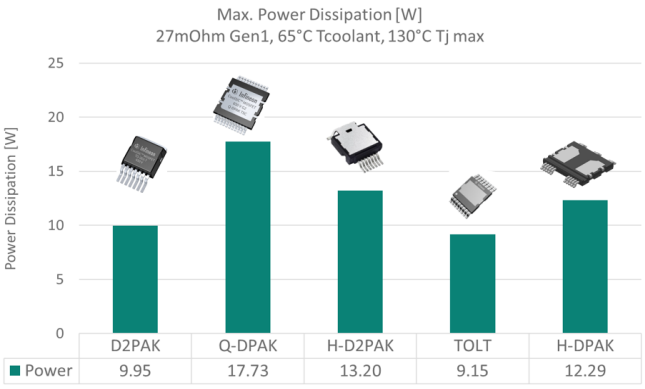


Fig. 25 Maximum power dissipation for different power packages with the thermal stack form the experiment. Note that for the H-DPAK, the power is per device of the half-bridge.

For a detailed thermal stack analysis with different TIM materials, please refer to the detailed analysis provided in [7].
An important factor that determines the cooling potential is the area of the lead frame, as a larger area can facilitate a larger heat transfer. Increasing the lead frame area enhances the thermal dissipation capabilities, which can help maintain lower temperatures on the device and improve overall thermal management. By comparing the results from TOLT and Q-DPAK with a similar thermal stack, it is evident that the Q-DPAK exhibits a 90% increase in power dissipation capability. This enhancement is attributable to the effective heat transfer area of the Q-DPAK, which is 2.7 times larger. The Q-DPAK also exhibits a 35% better thermal performance when compared to the H-D2PAK. The value for the H-DPAK is reported for one device, as in the measurement, power losses were only caused by the low-side device.
The performance of the bottom-side cooling device, D2PAK, is close to that of the TOLT. The primary challenge lies in achieving efficient thermal dissipation through the PCB, which may necessitate the utilization of advancements in modern PCB technology, such as copper inlay techniques, in order to increase its thermal dissipation.

Thermal management represents a perpetual balancing act between optimizing performance, maintaining adequate isolation, and meeting power density requirements. Designers must analyze the thermal resistance of the converter setup to ensure that the device does not reach excessively high temperatures and stays within limits specified in the manufacturer datasheet.

4 Conclusion

This paper offers a comprehensive summary of the electric and thermal characteristics of different SiC MOSFET high-power discrete packages.
Based on simulation and hardware measurements, this paper proposes optimal layout recommendations for power electronics systems designers to overcome two of the most challenging topics concerning the use of semiconductors: electrical and thermal performance. Best practice design examples are proposed, and based on those, quantitative data is obtained through state-of-the-art simulation methods, that are then validated on hardware for power packages readily available across the board for SiC MOSFETs.

5 References

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