Versatile I/O to interface S25FL-S SPI multi I/O flash in 1.8-V and 2.5-V systems

About this document

Scope and purpose

AN98518 discusses the versatile I/O (VIO) supply feature available in S25FL-S MIRRORBIT™ Serial Peripheral Interface (SPI) Multi-I/O Flash Memory family.

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1 Introduction

The S25FL-S MIRRORBIT™ Serial Peripheral Interface (SPI) Multi-I/O Flash Memory family has added the Versatile I/O (V_{IO}) supply feature as a model ordering option for the SOIC-16 and both 24-ball BGA packages.

Many embedded system applications have processors or chipsets operating at lower voltages even though a 3-V supply voltage is present in the system. As the voltage source for all flash device input receivers and output drivers, the Versatile I/O (V_{IO}) supply allows the host system to set the voltage levels that the device tolerates on all inputs and drives on outputs (control and I/O signals). The Versatile I/O (V_{IO}) supply range is from 1.65V to V_{CC} , and V_{IO} cannot be greater than the core SPI flash V_{CC} supply voltage which may range from 2.7V to 3.6V.

For example, a V_{IO} of 1.65V - 3.6V allows for I/O at the 1.8V, 2.5V, or 3V levels, driving and receiving signals to and from other 1.8V, 2.5V, or 3V devices on the same data bus.

2 V_{IO} package options

Versatile I/O (V_{IO}) is available for the following S25FL-S SPI Flash packages: the 300-mil 16-Lead SOIC, the 24-Ball BGA arranged as 5 x 5 balls (FAB024), and the alternative 24-Ball BGA arranged as 4 x 6 balls (FAC024). These S25FL-S SPI flash V_{IO} package models also support the Hardware Reset input signal on another dedicated pin. V_{IO} is not available for products offered in the WSON 8-contact 6 x 8 mm no-lead package since there are only six core Input/Output signals for Multi-I/O without V_{IO} or RESET#.

For package models that do not support V_{IO} , the V_{IO} supply is tied internally to V_{CC} inside the package for backward compatibility with the S25FL-P SPI Flash family. For 3V designs requiring a Hardware Reset pin, V_{IO} must be tied to V_{CC} so the interface signals operate at the same voltage as the core of the device.

Please refer to the specific S25FL-S SPI Multi-I/O Flash device data sheet for complete details on the V_{IO} model ordering options.

2.1 Package connection diagrams

The location of the V_{IO} and RESET# pins are shown in the following S25FL-S SPI Flash package connection diagrams.

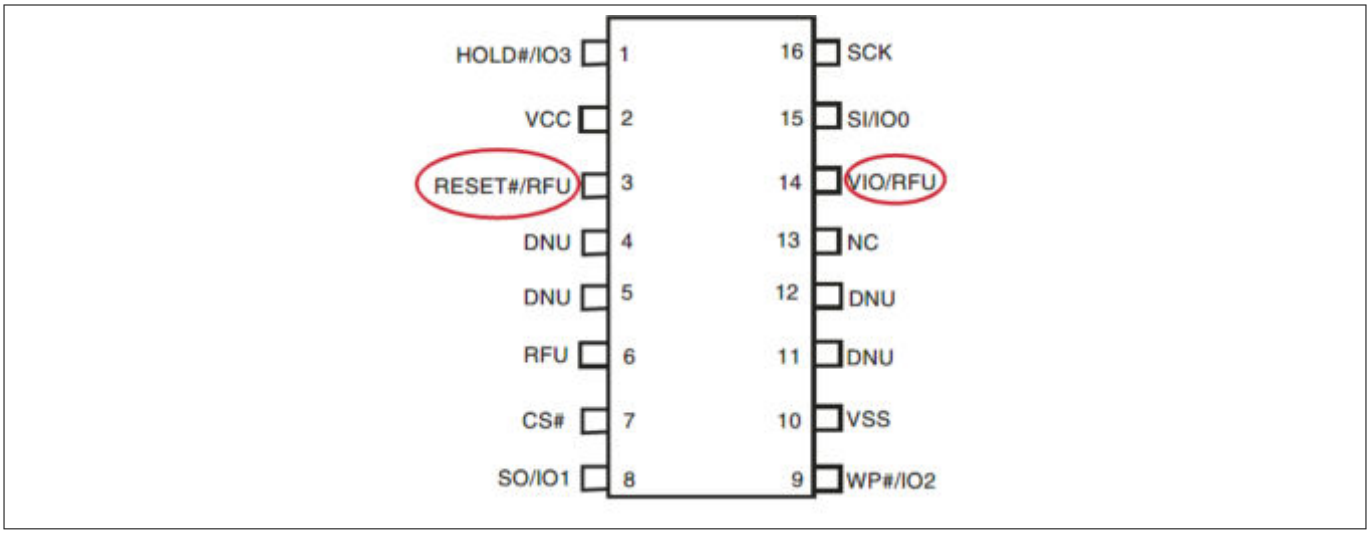

Figure 1 16-lead SOIC package, top view

2 V_{IO} package options

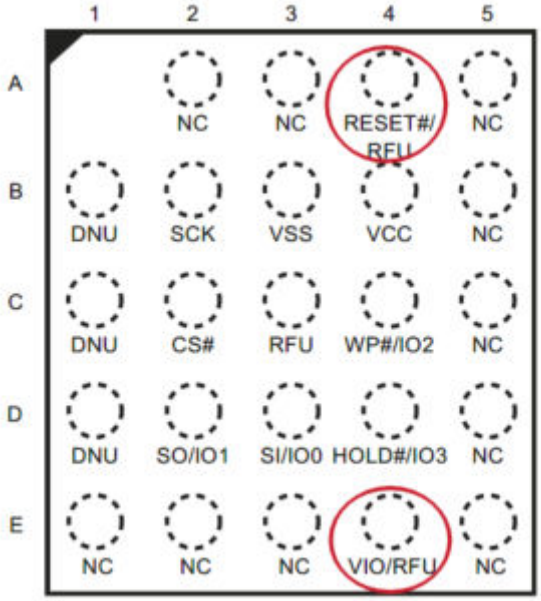

Figure 2 **24-ball BGA, 5 x 5 ball footprint (FAB024), top view**

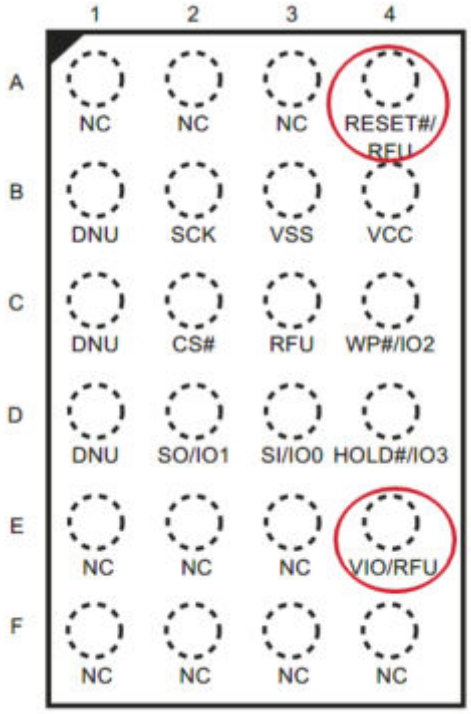

Figure 3 **24-ball BGA, 4 x 6 ball footprint (FAC024), top view**

3 V_{IO} interfacing examples

In Figure 4, the S25FL-S SPI Flash interface to a processor or chipset controller requiring 2.5V Input/Output signals is illustrated in a Quad Mode implementation. The SPI 2.5V V_{IO} signal is typically tied to the core V_{CC} of the controller. In this example, the controller also drives the SPI Hardware Reset signal with the timings compatible with the specific S25FL-S SPI Multi-I/O Flash device data sheet.

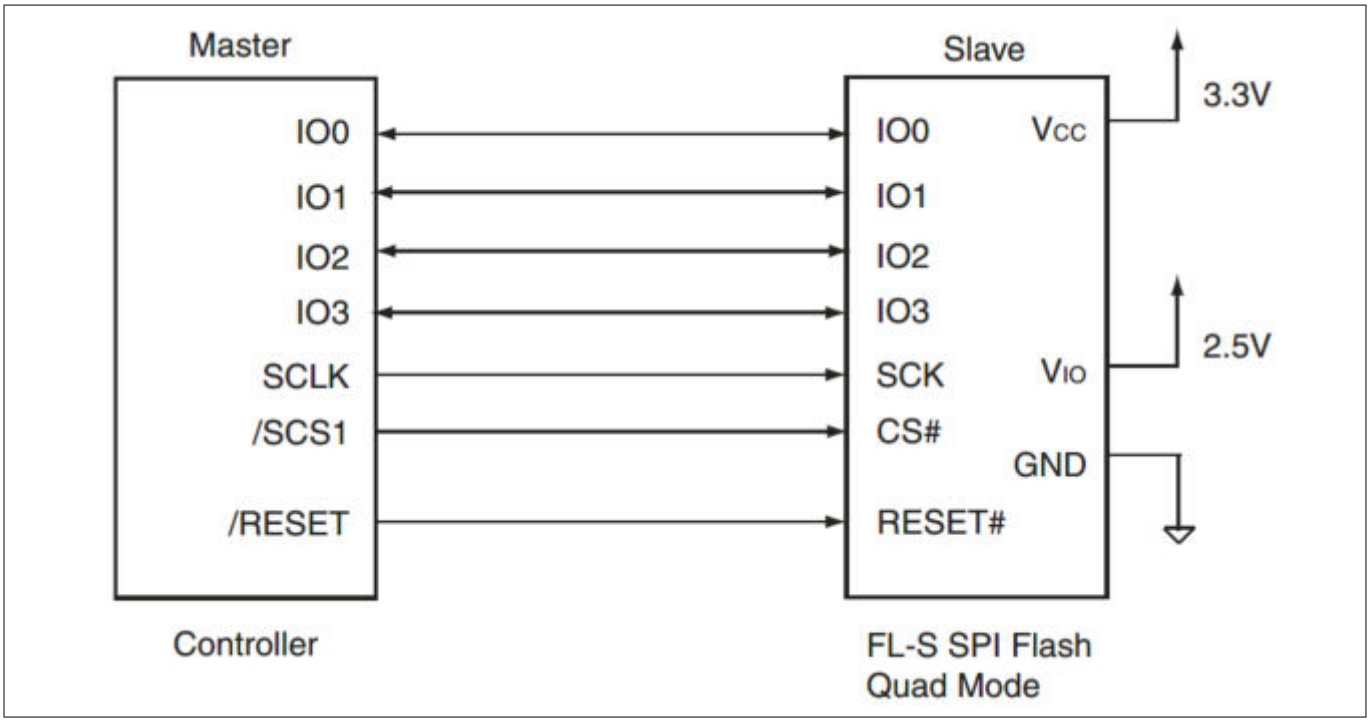

Figure 4 2.5V V_{IO} interface with RESET# example

In Figure 5, the S25FL-S SPI Flash interface to a processor or chipset controller requiring 1.8V Input/Output signals is illustrated in a Quad Mode implementation. Again, the SPI 1.8V V_{IO} signal is typically tied to the core V_{CC} of the controller. In this example, the controller does not drive the SPI Hardware Reset signal. The SPI RESET# input has an internal pull-up and may be left unconnected if the Hardware Reset feature is not used.

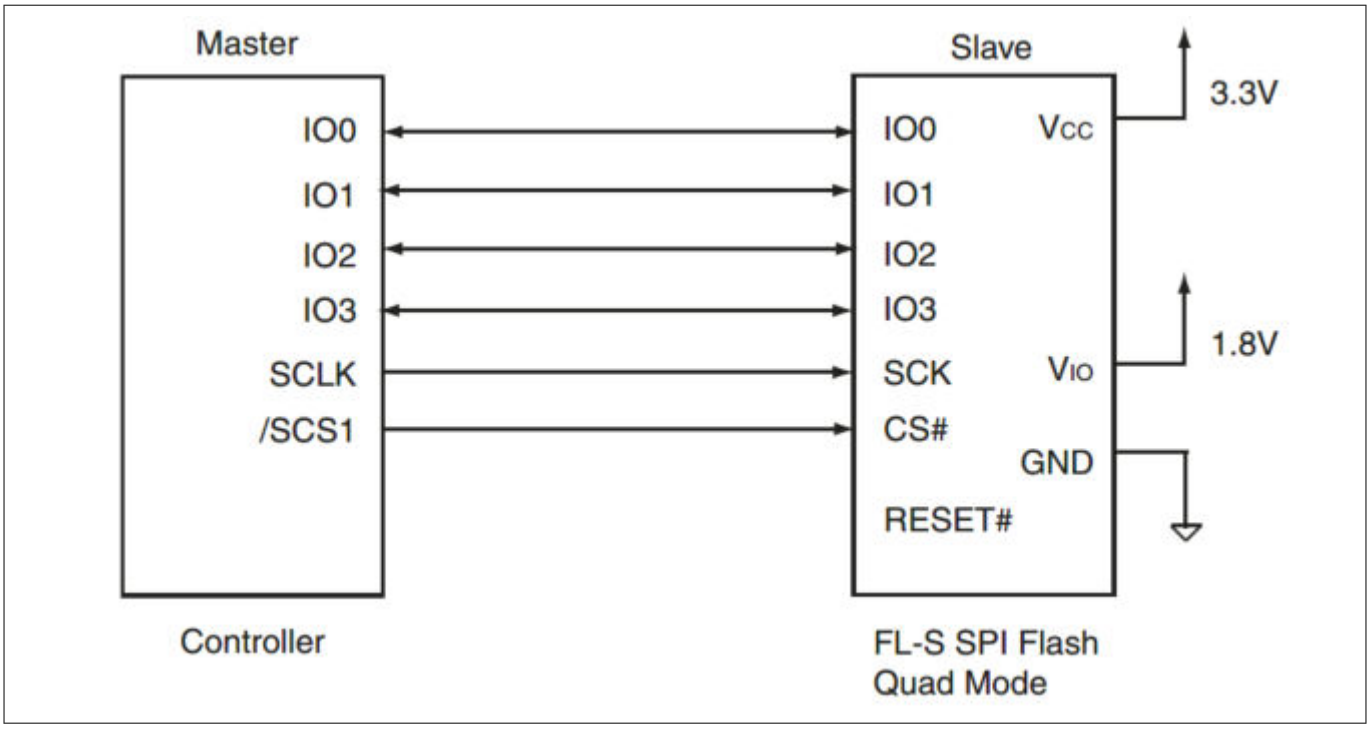

Figure 5 1.8 V V_{IO} interface without RESET# example

3.1 Power-up specifications

During the rise of power supplies at power-up, the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. However, the V_{IO} supply voltage must also be above V_{CC} -200 mV until the V_{IO} supply voltage is > 1.65V, i.e. the V_{IO} supply voltage must not lag behind the V_{CC} supply voltage by more than 200 mV during power up, until the V_{IO} supply voltage reaches its minimum operating level.

4 Summary

The Versatile I/O (V_{IO}) supply feature of the S25FL-S MirrorBit SPI Flash Memory family enables interfacing to system processor or chipset controllers requiring Input/Output levels between 1.65V and 3.6V, depending on the SPI core V_{CC} voltage, when a 3V supply voltage is present in the system.

The dedicated Hardware Reset input feature paired with the V_{IO} package options may be left unconnected if not used since the RESET# input has an internal pull-up. However, 3V designs requiring a Hardware Reset pin must tie V_{IO} to V_{CC} so the interface signals operate at the same voltage as the core V_{CC} of the SPI device.

5 References

- S25FL128S and S25FL256S Data sheet (S25FL128S_256S_00)
- Migration from FL-P to FL-S family SPI interface flash memories application note

Revision history

Document revision	Date	Description of Change
**	2012-03-27	Initial version
*A	2015-09-22	Updated in Infineon template
*B	2017-02-05	Updated logo and Copyright
*C	2026-07-14	Template update; no content change

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