# Replacing Everspin QSPI MRAM with Infineon QSPI nvSRAM

## About this document

AN96588 discusses the key differences between Everspin's 1-Mb Quad SPI (QSPI) MRAM and Cypress's 1-Mb QSPI nvSRAM devices. Note these differences when designing an application to enable drop-in replacement of MRAM with nvSRAM on the same footprint.

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# 1 Introduction

Infineon's 1-Mb QSPI nvSRAM is a high-performance nonvolatile SRAM product that offers truly random memory accesses (writes and reads). It is a monolithic integrated circuit with a quad serial peripheral interface (Quad SPI), which allows writing and reading the memory using a single (one I/O channel for one bit per clock cycle), dual (two I/O channels for two bits per clock cycle), or quad (four I/O channels for four bits per clock cycle) configuration via a function-rich command set. QSPI provides nvSRAM with a cost-effective, low-pin-count, nonvolatile memory solution.

The QSPI nvSRAM architecture incorporates Infineon's unique SRAM with silicon-oxide-nitride-oxide semiconductor (SONOS) nonvolatile elements. It blends the performance characteristics of a high-speed SRAM with a nonvolatile memory. The quad serial interface in quad SPI nvSRAM conforms to the de facto industry-standard QSPI interface. The instruction set includes standard QSPI opcodes along with nvSRAM-specific functions and performance-oriented new features. The QSPI nvSRAM signals include serial clock (SCK), SI, and SO (for command/response and data input/output) and control signals CS#, HOLD#, and WP#. This hardware interface creates a low-pin-count device that reduces package size, PCB area, and overall system cost.

A similar nonvolatile memory solution is Everspin's 1-Mb Quad SPI Magnetoresistive RAM (MRAM). MRAM storage elements require a localized magnetic field to change cell states during writes. Reads are done by measuring the resistance of the cell. The 1-Mb QSPI MRAM architecture also offers truly random accesses; however, QSPI is an expansion of the Extended SPI and does not conform to the de facto industry-standard. Moreover, MRAMs are susceptible to external magnetic fields, as exemplified during writes, causing potential incorrect bit programming. Hence, care must be taken in applications to ensure that MRAMs are not in close proximity to magnetic fields or current-carrying conductors.

Infineon's 1-Mb QSPI nvSRAM offers a nonvolatile solution with a standardized interface and none of the MRAM's magnetic field susceptibilities. It is immune to the magnetic fields that can be present in some commercial and industrial applications.

This application note discusses hardware and firmware (instruction opcodes) design with a focus on the option to replace the 1-Mb QSPI MRAM with the 1-Mb QSPI nvSRAM on the same socket without any hardware or opcode changes.

# 2 Replacing 1-Mb QSPI MRAM (MR10Q010) with 1-Mb QSPI nvSRAM (CY14B101QS)

This section highlights the differences between the 1-Mb QSPI nvSRAM and 1-Mb QSPI MRAM devices in terms of package and instruction set. It also discusses design considerations to enable seamless substitution.

## 2.1 Package compatibility

The 1-Mb QSPI nvSRAM and 1-Mb QSPI MRAM are both offered in 16-pin SOIC packages. The dimensions of the packages are similar and socket compatible, as shown in Table 1.

The primary differences are five pins– namely, pin 6, pin 11, pin 12, pin 13, and pin 14. Table 2 provides a detailed description of the pin differences and Infineon's PCB design connectivity preferences.

**Table 1 16-Pin SOIC package comparison**

| | Infineon 1-Mb Quad SPI nvSRAM (mm) | | Everspin 1-Mb Quad SPI MRAM (mm) | |
|---|---|---|---|---|
| **Package dimensions** | **Min.** | **Max.** | **Min.** | **Max.** |
| Length | 10.08 | 10.49 | 10.21 | 10.46 |
| Width | 7.39 | 7.59 | 7.42 | 7.59 |
| Height | 2.33 | 2.66 | 2.46 | 2.64 |
| Pitch | – | 1.27 | – | 1.27 |

**Table 2 Pin comparison details – Quad SPI nvSRAM and Quad SPI MRAM**

| PIN # | Infineon 1-Mb Quad SPI nvSRAM | Infineon connection | Everspin 1-Mb Quad SPI MRAM | Everspin connection | Infineon connection preference |
|---|---|---|---|---|---|
| 6 | NC | Not connected. | VDD/VCC (3.3 V) | Power supply voltage from +3.0 to +3.6 volts (VDD/VCC). | Can be biased to VDD/VCC. |
| 11 | NC | Not connected. | VSS (GND) | Ground pin (VSS/GND). | Can be biased to VSS/GND. |

**(table continues...)**

**Table 2 (continued) Pin comparison details – Quad SPI nvSRAM and Quad SPI MRAM**

| PIN # | Infineon 1-Mb Quad SPI nvSRAM | Infineon connection | Everspin 1-Mb Quad SPI MRAM | Everspin connection | Infineon connection preference |
|---|---|---|---|---|---|
| 12 | HSB# | Hardware STORE Busy.<br>Output: Indicates the busy status of nvSRAM when LOW.<br>Input: Hardware STORE implemented by pulling this pin LOW externally. | NC | Not connected. | The nvSRAM HSB# pin can be left floating (NC) if its functionality is not used in the design.<br>It is recommended to connect an external 4.7 kΩ to 10 kΩ pull-up resistor on the HSB# pin if it is connected to a controller I/O for control.<br>Refer to AN43380 for more details on HSB# operation in nvSRAMs. |
| 13 | $V_{CAP}$ | AutoStore capacitor.<br>Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, this pin must be left unconnected. It must never be connected to ground. | NC | Not connected.<br>**Note:** It is imperative that if MRAM is used in a design, that this pin be left unconnected to accommodate the $V_{CAP}$ capacitor. | The capacitor must be installed when using the AutoStore feature in nvSRAMs. |
| 14 | NC | Not connected. | VSS (GND) | Ground pin (VSS/GND). | Can be biased to VSS/GND. |

## 2.2 Pin compatibility

Figure 1 shows the pin function differences between the 1-Mb QSPI nvSRAM and 1-Mb QSPI MRAM.

## 2 Replacing 1-Mb QSPI MRAM (MR10Q010) with 1-Mb QSPI nvSRAM (CY14B101QS)

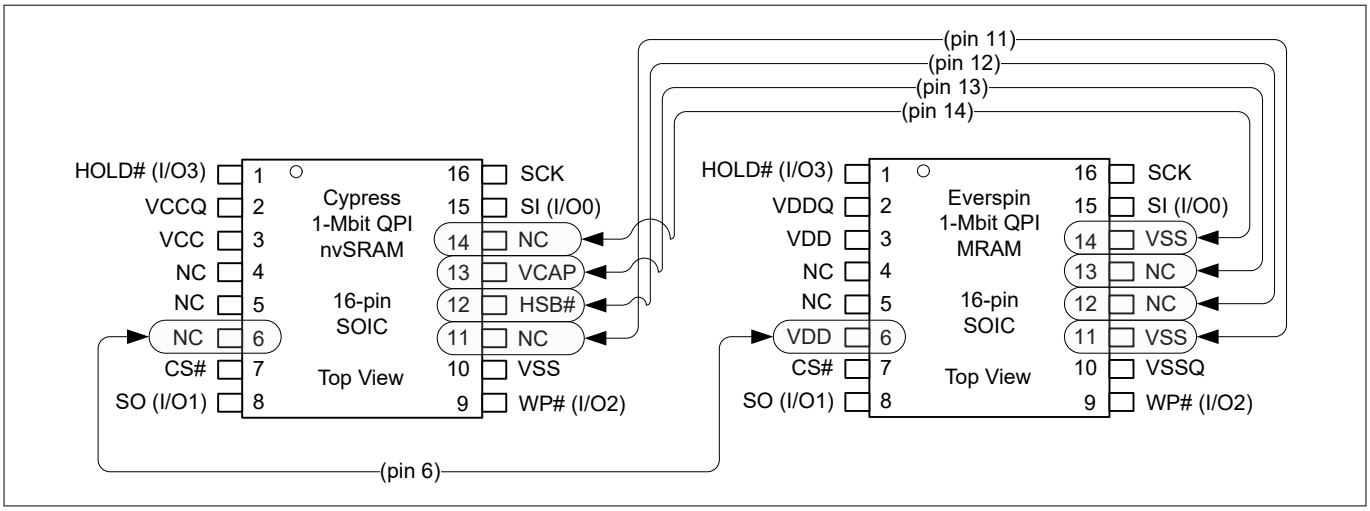



**Figure 1** **Pin comparison between 1-Mb QSPI nvSRAM and 1-Mb QSPI MRAM – 16-pin SOIC package**

## 2.3 Status register compatibility

The 1-Mb QSPI nvSRAM and 1-Mb QSPI MRAM both have 8-bit status registers. The bits in these registers provide a multitude of functions, ranging from the device busy status to the memory core write protect options. Table 3 provides a detailed comparison and Infineon's recommendations for use.

**Table 3** **Status register comparison details**

| Bit No. | Infineon 1-Mb Quad SPI nvSRAM | Infineon description | Everspin 1-Mb Quad SPIMRAM | Everspin description | Infineon recommendations |
|---|---|---|---|---|---|
| 0 | WIP | Work In progress | Reserved | Reserved Bit 0 | Read only (no conflict): Should be used to determine if the device is busy. |
| 1 | WEL | Write enable latch | WEL | Write enable latch | Identical functionality |
| 2 | BP0 | Block protection bits | BP0 | Block protection bits | Infineon's nvSRAM block protection is based on 1/64th device density whereas Everspin's MRAM is based on 1/4th device density. |
| 3 | BP1 | | BP1 | | |
| 4 | BP2 | | Reserved | Reserved bit 1 | |
| 5 | TBPROT | Configures start of block protection | Reserved | Reserved bit 2 | |
| 6 | SNL | Serial number lock | Quad SPI mode | Shows if the device is in Quad SPI mode | nvSRAM has a Quad SPI bit in the configuration register that is set by the QPIEN command. |
| 7 | SRWD | Status register write disable | SRWD | Status register write disable | Identical functionality |

## 2.4 Communications protocol (Instruction set) compatibility

The 1-Mb QSPI nvSRAM incorporates a rich instruction set, improving functionality and control over the 1-Mb QSPI MRAM. The nvSRAM communications protocol is a superset of that of the MRAM and supports higher data throughput. Table 4 provides a detailed overview of the instruction opcodes, as well as the opcodes that are compatible between the two devices.

**Table 4 Instruction set (Opcodes) comparison details**

| Instruction description | Instruction name | Opcode | SPI | DPI | QPI | SPI extended | MRAM SPI compatibility | MRAM QPI compatibility | MRAM SPI extended compatibility |
|---|---|---|---|---|---|---|---|---|---|
| **Control** | | | | | | | | | |
| Write disable | WRDI | 04h | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | Yes | Yes | |
| Write enable | WREN | 06h | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | Yes | Yes | |
| Enable DPI | DPIEN | 37h | [1,-,-,-] | | [4,-,-,-] | | NA | NA | |
| Enable QPI | QPIEN | 38h | [1,-,-,-] | [2,-,-,-] | | | Yes | Yes | |
| Enable SPI | SPIEN | FFh | | [2,-,-,-] | [4,-,-,-] | | | Yes | |
| **Memory read** | | | | | | | | | |
| Read | READ | 03h | [1,1,-,1] | [2,2,-,2] | [4,4,-,4] | | Yes | No | |
| Fast read | FAST_READ | 0Bh | [1,1,1,1] | [2,2,2,2] | [4,4,4,4] | | Yes | No | |
| Dual out (Fast) read | DOR | 3Bh | | | | [1,1,1,2] | | | NA |
| Quad out (Fast) read | QOR | 6Bh | | | | [1,1,1,4] | | | No |
| Dual IO (Fast) read | DIOR | BBh | | | | [1,2,2,2] | | | NA |
| Quad IO (Fast) read | QIOR | EBh | | | | [1,4,4,4] | | | Yes |
| **Memory write** | | | | | | | | | |
| Write | WRITE | 02h | [1,1,-,1] | [2,2,-,2] | [4,4,-,4] | | Yes | No | |
| Dual input write | DIW | A2h | | | | [1,1,-,2] | | | NA |
| Quad input write | QIW | 32h | | | | [1,1,-,4] | | | Yes |
| Dual IO write | DIOW | A1h | | | | [1,2,-,2] | | | NA |
| Quad IO write | QIOW | D2h | | | | [1,4,-,4] | | | Yes |

**(table continues...)**

**Table 4 (continued) Instruction set (Opcodes) comparison details**

| Instruction description | Instruction name | Opcode | SPI | DPI | QPI | SPI extended | MRAM SPI compatibility | MRAM QPI compatibility | MRAM SPI extended compatibility |
|---|---|---|---|---|---|---|---|---|---|
| **SR commands** | | | | | | | | | |
| Software reset enable | RSTEN | 66h | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| Software reset | RESET | 99h | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| Read RTC | RDRTC | 56h | [1,1,-,1] | [2,2,-,2] | [4,4,-,4] | | NA | NA | |
| Write RTC | WRRTC | 55h | [1,1,-,1] | [2,2,-,2] | [4,4,-,4] | | NA | NA | |
| Fast Read RTC | FAST_RDRTC | 57h | [1,1,-,1] | [2,2,-,2] | [4,4,-,4] | | NA | NA | |
| Enter Hibernate mode | HIBEN | BAh | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| Enter Sleep mode | SLEEP | B9h | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | Yes | Yes | |
| Exit Sleep mode | EXSLP | ABh | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | Yes | Yes | |
| **Register commands** | | | | | | | | | |
| Read status register | RDSR | 05h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | Yes | No | |
| Write status register | WRSR | 01h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | Yes | No | |
| Read configuration register | RDCR | 35h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | NA | NA | |
| Write configuration register | WRCR | 87h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | NA | NA | |
| Read ID register | RDID | 9Fh | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | No | No | |
| Fast Read ID register | FAST_RDID | 9Eh | [1,-,1,1] | [2,-,2,2] | [4,-,4,4] | | Yes | No | |
| Write serial number register | WRSN | C2h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | NA | NA | |

**(table continues...)**

**Table 4 (continued) Instruction set (Opcodes) comparison details**

| Instruction description | Instruction name | Opcode | SPI | DPI | QPI | SPI extended | MRAM SPI compatibility | MRAM QPI compatibility | MRAM SPI extended compatibility |
|---|---|---|---|---|---|---|---|---|---|
| Read serial number register | RDSN | C3h | [1,-,-,1] | [2,-,-,2] | [4,-,-,4] | | NA | NA | |
| Fast read serial number register | FAST_RDSN | C9h | [1,-,1,1] | [2,-,2,2] | [4,-,4,4] | | NA | NA | |
| **NV-specific commands** | | | | | | | | | |
| STORE | STORE | 8Ch | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| RECALL | RECALL | 8Dh | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| AutoStore enable | ASEN | 8Eh | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| AutoStore disable | ASDI | 8Fh | [1,-,-,-] | [2,-,-,-] | [4,-,-,-] | | NA | NA | |
| **Mode bits** | | | | | | | | | |
| Mode bit (Set, Reset) | | Axh, !Axh | | | | | | | |

***Note**: [1,1,1,1] = [instruction, address, mode, data] = Number of pins used during instruction cycles.*

***Note**: NA = Not available*

The MRAM supports the standard SPI and QSPI modes. It reconfigures the SPI pins to work in the QSPI mode by assigning the SI pin, SO pin, WP# pin, and HOLD# pin as the I/O0 pin, I/O1 pin, I/O2 pin, and I/O3 pin for opcode transfer in the instruction only. Address and/or data for the QSPI mode are controlled through the Quad Addr/Data or Quad Data instructions. Infineon recommends avoiding instructions in MRAM where the command is transferred in the QSPI mode and the address/data are transferred in the SPI mode. Using these MRAM instructions will impact performance when using the MRAM product and create noticeable coding differences between the MRAM and nvSRAM QSPI parts.

Table 5 provides a list of MRAM instructions in the QSPI mode that exhibit the above-mentioned behavior. As can be seen, data for these instructions is always transferred on a single pin and lacks throughput optimization.

**Table 5 MRAM Instruction Opcodes to avoid**

| Instruction description | Instruction name | Opcode | QPI |
|---|---|---|---|
| **Memory read** | | | |
| Read | READ | 03h | [4,1,-,1] |
| Fast read | FAST_READ | 0Bh | [4,1,1,1]] |

**(table continues...)**

**Table 5 (continued) MRAM Instruction Opcodes to avoid**

| Instruction description | Instruction name | Opcode | QPI |
|---|---|---|---|
| **Memory write** | | | |
| Write | WRITE | 02h | [4,1,-,1] |
| **Register commands** | | | |
| Read status register | RDSR | 05h | [4,-,-,1] |
| Write status egister | WRSR | 01h | [4,-,-,1] |
| **Read ID commands** | | | |
| Fast read ID register | FAST_RDID | 4Bh | [4,-,1,1] |

***Note**: [1,1,1,1] = [instruction, address, mode, data] = Number of pins used during instruction cycles.*

# 3 Power considerations

The 1-Mb QSPI nvSRAM includes robust power circuitry and is designed to maintain data integrity across all types of power ramp rates and brown-out conditions. However, nvSRAM requires data coherency between its internal nonvolatile elements and SRAM cells during different power modes, as explained in the following sections.

## 3.1 Power up

When the $V_{CC}$ power supply crosses the internal threshold ($V_{SWITCH}$), the 1-Mb QSPI nvSRAM starts its bootup sequence, followed by a memory Power-Up RECALL operation. The Power-Up RECALL process transfers data from the internal nonvolatile elements into the adjacent SRAM cells and readies the device for normal operation. The external capacitor, $V_{CAP}$, is also charged through the device to $V_{DD}$ during the power-up sequence and is maintained at that level during normal nvSRAM operation. The nvSRAM takes 20 ms ($t_{RECALL}$) to complete the bootup sequence. During this time, the device is inaccessible. The master QSPI controller that is connected to the QSPI nvSRAM needs to accommodate this 20 ms delay during power-up.

## 3.2 Power down

When the $V_{CC}$ or the $V_{CCQ}$ power supplies fall below the internal threshold ($V_{SWITCH}$), the 1-Mb QSPI nvSRAM initiates an AutoStore operation. During the AutoStore process, which simultaneously transfers all SRAM cell states to their adjacent nonvolatile elements, the nvSRAM switches off the collapsing $V_{DD}$ voltage and uses only the charge stored on the external $V_{CAP}$ capacitor to supply power. If a write cycle is in progress when the device loses $V_{CC}$/$V_{CCQ}$ power, it is allowed to finish before AutoStore is initiated. This ensures that the last data word is successfully written to the nvSRAM.

# 4 Summary

With forethought on PCB layout and care taken to avoid some Everspin MRAM instruction opcodes, the Infineon 1-Mb QSPI nvSRAM can be made pin-compatible with Everspin's 1-Mb QSPI MRAM. The two key actions required are adding $V_{CAP}$ on the nvSRAM $V_{CAP}$ pin (an NC pin for MRAM) and addressing the instruction opcode differences described in this application note.

Following the instructions in this application note will allow the 1-Mb QSPI nvSRAM to serve as a drop-in replacement for a 1-Mb QSPI MRAM.

# Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| ** | 2015-03-31 | Initial release. |
| *A | 2015-07-09 | Incorporated Instruction Opcode changes. |
| *B | 2026-09-04 | Template update; no content update |

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