Designing with I²C F-RAM

About this document

Scope and purpose

AN96578 provides design guidelines and example circuits to help you design with the I²C F-RAM device, a high-performance nonvolatile serial interface memory.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Associated part family

FM24xxx and CY15BxxxJ

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1 Introduction

Ferroelectric Random Access Memory (F-RAM) is a nonvolatile memory that uses ferroelectric technology to store data. The serial F-RAM device offers advantages over other nonvolatile serial memories due to its no-delay (or zero-delay) write. F-RAM can write hundreds of bytes in tens of microseconds. In comparison, EEPROM and flash memories take tens of milliseconds to write the same amount of data. The ability of F-RAM to write data quickly before losing power is particularly useful in systems that require preserving machine state information, parameter settings, or other vital data in a power-down event. F-RAM also has very high endurance over other nonvolatile solutions, allowing a large number of writes/reads to F-RAM without damaging its nonvolatile cells.

F-RAM is a true nonvolatile RAM since it combines the advantages of both RAM and nonvolatile memory. It is available in different interface options such as SPI, I²C, and parallel. This application note discusses the I²C interface in F-RAM. It describes the different I²C F-RAM configurations, shows I²C F-RAM interface in a typical system, and gives design guidelines for using it in a system and the data format for accessing it. For other details such as AC, DC, and timing parameters, refer to the specific I²C F-RAM datasheet.

2 I²C F-RAM configurations

The I²C F-RAM supports a data transfer rate up to 3.4 Mbps as well as all other lower frequency accesses as defined in the I²C-bus specification.

- Standard mode (Sm): Bit rate up to 100 Kbps
- Fast mode (Fm): Bit rate up to 400 Kbps
- Fast mode plus (Fm+): Bit rate up to 1 Mbps
- High-speed mode (Hs-mode): Bit rate up to 3.4 Mbps

The Sm, Fm, and Fm+ bus modes are offered in all device configurations. The Hs-mode is offered only FM24Vxx and CY15BxxxJ series devices.

2.1 Applicability of I²C bus protocol features

Table 1 summarizes the mandatory and optional features of the standard I²C slave bus specifications. The I²C F-RAM supports all the mandatory features of a standard I²C slave device.

Table 1 Applicability of I²C protocol

Feature	I²C spec standards	I²C F-RAM
START condition	Mandatory	Offered
STOP condition	Mandatory	Offered
Acknowledge	Mandatory	Offered
7-bit slave address	Mandatory	Offered
10-bit slave address	Optional	Not offered
Clock stretching	Optional	Not offered
General call address	Optional	Not offered
Device ID	Optional	Offered[1)]
Software reset	Optional	Not offered

1) Device ID feature is offered in FM24VXX and CY15BxxxJ devices only

2.2 I²C F-RAM device options

Infineon supports I²C F-RAM in different configurations and packages, as listed in Table 2.

Table 2 I²C F-RAM configurations

Part number	Status	Density	Operating voltage (Typical)	Package	WP pin	A0 pin	A1/A2 pin	No. of devices per I²C bus	Device ID	Serial number	Sleep mode	Hs-mode (3.4 MHz)
FM24C04B	In Production	4 Kb	5.0 V	8 SOIC	Yes	No	Yes	4	No	No	No	No

(table continues...)

2 I²C F-RAM configurations

Table 2 (continued) I²C F-RAM configurations

Part number	Status	Density	Operating voltage (Typical)	Package	WP pin	A0 pin	A1/A2 pin	No. of devices per I²C bus	Device ID	Serial number	Sleep mode	Hs-mode (3.4 MHz)
FM24CL04B	In Production	4 Kb	3.3 V	8 SOIC	Yes	No	Yes	4	No	No	No	No
FM24C16B	In Production	16 Kb	5.0 V	8 SOIC	Yes	No	No	1	No	No	No	No
FM24CL16B	In Production	16 Kb	3.3 V	8 SOIC 8 DFN	Yes	No	No	1	No	No	No	No
FM24C64B	In Production	64 Kb	5.0 V	8 SOIC	Yes	Yes	Yes	8	No	No	No	No
FM24CL64B	In Production	64 Kb	3.3 V	8 SOIC 8 DFN	Yes	Yes	Yes	8	No	No	No	No
FM24V01	NRND[1)]	128 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
FM24V01A	In Production	128 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
CY15B128J	In Production	128 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
FM24V02	NRND[1)]	256 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
FM24V02A	In Production	256 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
CY15B256J	In Production	256 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
FM24W256	In Production	256 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	No	No	No	No
FM24V05	In Production	512 Kb	3.3 V	8 SOIC	Yes	Yes	Yes	8	Yes	No	Yes	Yes
FM24V10	In Production	1 Mb	3.3 V	8 SOIC	Yes	No	Yes	4	Yes	No	Yes	Yes
FM24VN10	In Production	1 Mb	3.3 V	8 SOIC	Yes	No	Yes	4	Yes	Yes	Yes	Yes

1) Not recommended for new design

3 I²C F-RAM system – Typical configuration

Figure 1 shows a typical I²C single-master multi-slave configuration. The I²C master device can be any microcontroller or a programmable device that is capable of generating the I²C master protocols. The slave devices can be any standard I²C slave devices. In Figure 1, the slave devices are I²C F-RAM devices. Since the 512-Kb and lower density I²C F-RAM devices support three slave addressing bits (A0, A1, and A2), it is possible to connect up to eight devices on the same I²C bus. A typical I²C F-RAM slave device is shown in Figure 2. A unique slave ID is assigned to each slave device by configuring the slave select address lines (A2, A1, and A0). In packages where the slave select address, A0, is not available, such as the 4-Kb and 1-Mb I²C F-RAM, it is possible to connect only up to four slave devices sharing the same bus by configuring the slave select address pins A2 and A1. For 16-Kb F-RAM devices, the device select address pins (A0, A1, and A2) are not available; hence, only one device can be connected on the bus.

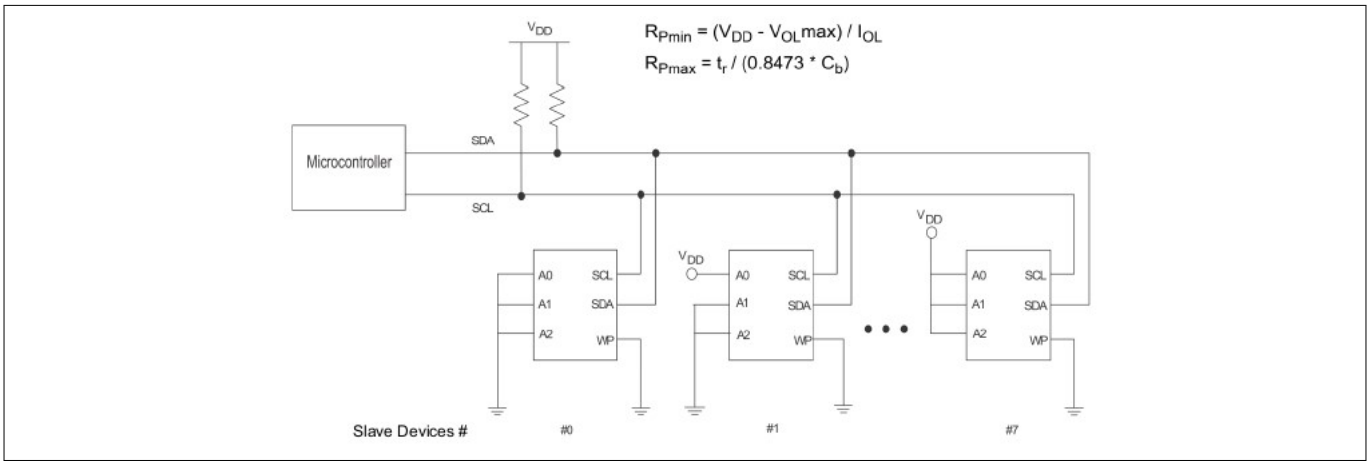


Figure 1 Single-master multi-slave I²C configuration

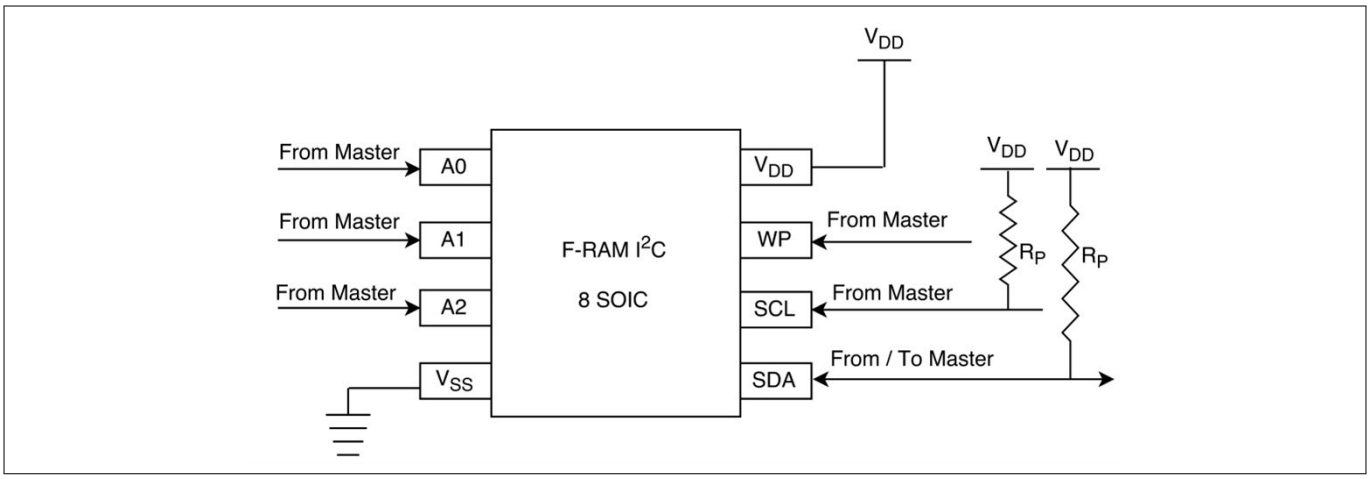


Figure 2 I²C F-RAM slave device

4 Design criteria for I²C F-RAM

I²C is a two-wire synchronous bus with an SCL line used for transmitting clock and an SDA line used for transmitting data. On the I²C F-RAM device, the SCL line is an input, while the SDA line is an open-drain output. The open drain allows easy arbitration over control of the bus to implement bidirectional communication on a single data line and multi-master support. The SCL line, though input at F-RAM, is an open-drain output at the master. Hence, both the SCL and SDA lines require an external resistor to V_{DD} to pull up the lines when they are released.

There are two considerations when determining the pull-up resistor values (R_P):

- Supply voltage (V_{DD})
- Total bus capacitance (C_B)

***Note**: The pull-up resistor value calculations in the following sections are for the I²C F-RAM SDA line. Based on the master I²C device, the calculation shown below should be repeated to determine the pull-up resistor value for the SCL line.*

4.1 Supply voltage (V_{DD})

Figure 3 shows the I²C logic levels. The I²C specification defines logic level low as the voltage below $V_{IL,}$ which is typically 30 percent of the supply voltage. Logic level high is defined as the voltage level above V_{IH}, which is typically 70 percent of the supply voltage. A voltage between these two levels is undefined.

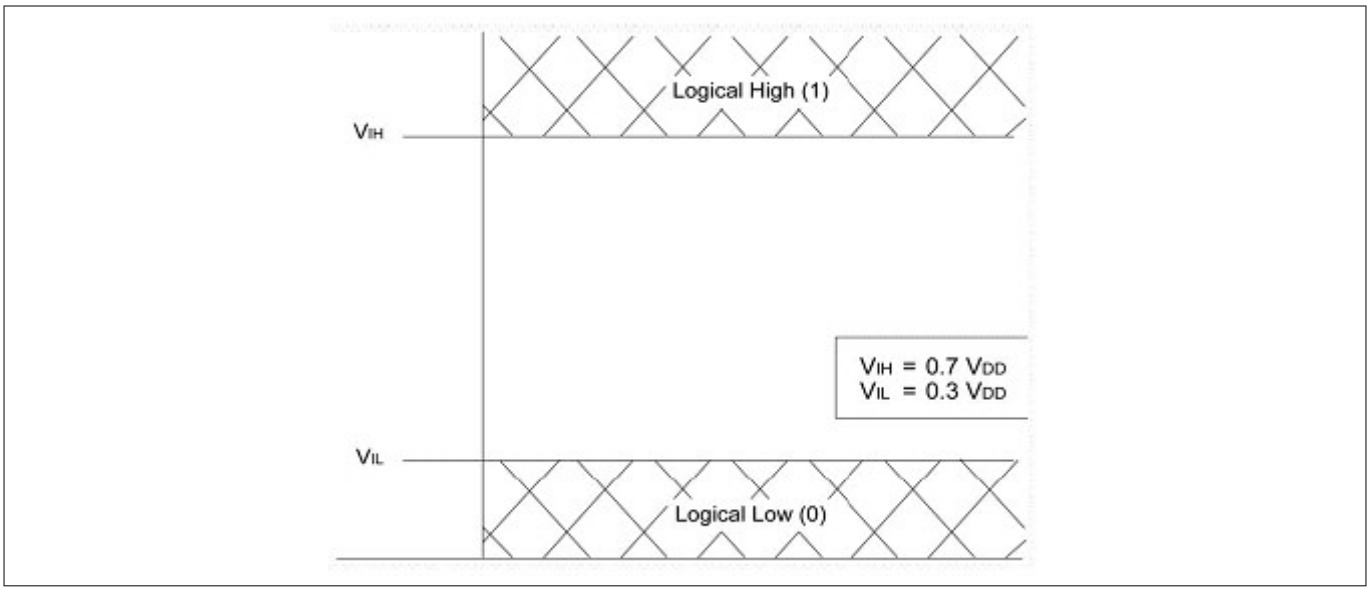


Figure 3 I²C bus logic levels

The supply voltage will limit the minimum value of the pull-up resistor (R_P). The pull-up resistor along with the ON resistance of the device transistor will form a potential divider network, as shown in Figure 4. A strong pull-up resistor will prevent the line from being sufficiently pulled low (below V_{IL}) to allow it to be detected as a logical low.

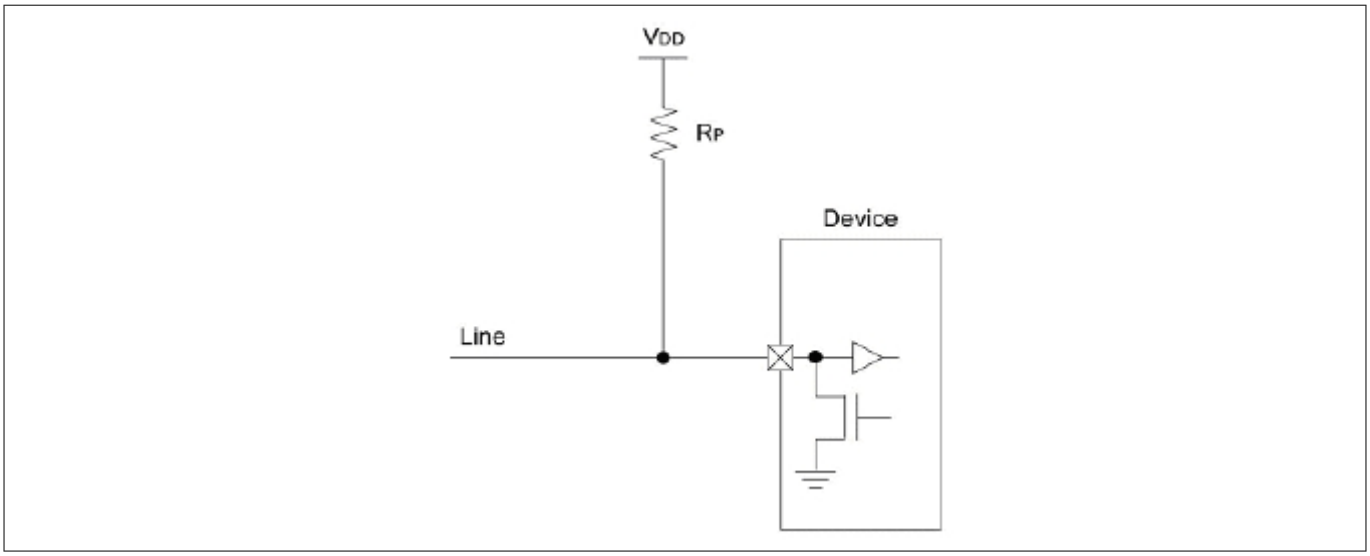


Figure 4 I²C bus line

The ON resistance of the transistor is typically not specified. Instead, a maximum sink current (I_{OL}) is specified, for which the voltage drop across the transistor should be below the output logical low-voltage level (V_{OL}).

$$V_{DD} - (I_{OL} \times R_P) \leq V_{OL}, \quad \text{that is,} \quad R_P \geq \frac{V_{DD} - V_{OL}}{I_{OL}} \tag{1}$$

For a typical 3.0-V I²C F-RAM part operating at the maximum V_{DD} voltage of 3.6 V, the V_{OL} specification is a maximum of 0.4 V at an I_{OL} of 2 mA. Hence

$$R_P \geq \frac{3.6 - 0.4}{2 \times 10^{-3}}, \quad \text{that is,} \quad R_P \geq 1.6\ \text{k}\Omega \tag{2}$$

4.2 Total bus capacitance (C_B)

Bus capacitance is the total capacitance contributed by all pins, connections, and PCB traces and wire. It can be significant for long traces and cabling of the SDA and SCL lines. When the SDA and SCL lines are released, it is pulled up by the external resistor (R_P). The pull-up resistor (R_P), along with the bus capacitance (C_B), forms an RC circuit and thus limits the rise time of the SDA and SCL lines. The rise time is critical in high-speed operations, and if the resistor value is too high, the line may not rise to a logical high in time. Therefore, the total bus capacitance limits the rise time and in turn the maximum value of the pull-up resistor.

For an RC circuit,

$$V(t) = V_{DD}\,(1 - e^{-t/RC}) \quad \text{i.e.} \quad t = -RC\,\ln\left(1 - \frac{V(t)}{V_{DD}}\right) \tag{3}$$

For I²C, the rise time (t_r) is defined as the time taken for the SDA or SCL line to rise from V_{IL} (0.3 × V_{DD}) to V_{IH} (0.7 × V_{DD}), as shown in Figure 5.

The time taken to charge to the V_{IL} level is

4 Design criteria for I²C F-RAM

$$t_1 = -R_P C_B \ln(1 - \frac{0.3 \times V_{DD}}{V_{DD}}) = 0.356675 \times R_P C_B \quad (4)$$

The time taken to charge to the V_{IH} level is

$$t_2 = -R_P C_B \ln(1 - \frac{0.7 \times V_{DD}}{V_{DD}}) = 1.203973 \times R_P C_B \quad (5)$$

Hence, the rise time

$$t_r = t_2 - t_1 = (1.203973 \times R_P C_B) - (0.356675 \times R_P C_B) = 0.8473 \times R_P C_B \quad (6)$$

For the I²C F-RAM in Fm-mode,the rise time t_r = 120 ns. Hence,

$$120 \times 10^{-9} = 0.8473 \times R_P C_B \quad (7)$$

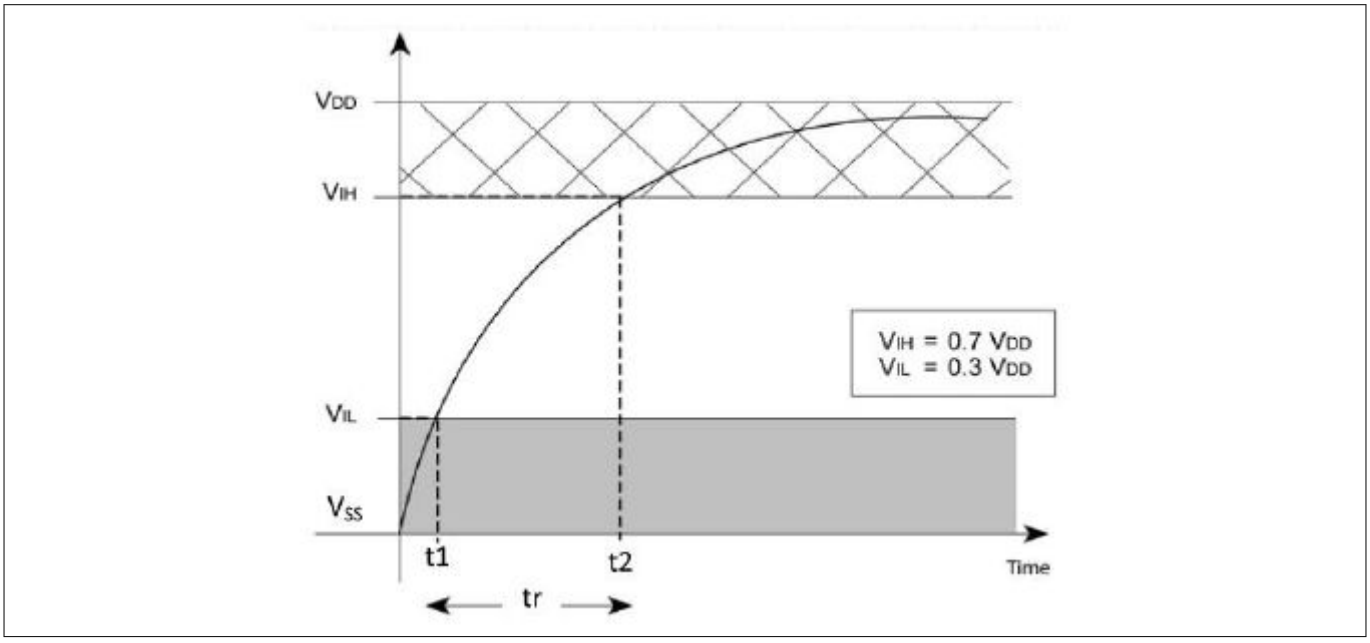


Figure 5 I²C line rise time

Low-power designs should prefer using a pull-up resistor (R_P) value towards the higher limit of the range to limit current consumption. Table 3 provides a list of the values of R_P (Min, Max) for a given bus load condition and operating voltage. Shaded regions indicate that R_P (Min) exceeds the R_P (Max) value for a few bus loads (C_B) under a given operating voltage condition. Since the R_P (Min) can never exceed the R_P (Max) value, this will put a limit on the maximum capacitive load (C_B) to be used on the I²C bus. For example, if a 3-V part is configured to operate at a minimum V_{DD} supply (V_{DD} = 2.7 V), then the system must not exceed the load (in picofarads) given in Table 3 for the SDA line. A similar calculation can be done on the SCL line for the I²C master.

Table 3 R_P (Min, Max) values for different bus loads and operating voltages

	R_P (Max) kΩ	
Freq	**1 MHz**	**3.4 MHz**
t_R (ps)	**120000**	**80000**
C_B (pF)		
V_{DD} = 3.6 V, R_P (min) = 1.6 kΩ		
10	14.16	9.44
20	7.08	4.72
30	4.72	3.15
40	3.54	2.36
50	2.83	1.89
60	2.36	1.57
70	2.02	1.35
80	1.77	1.18
90	1.57	1.05
100	1.42	0.94
125	1.13	0.76
150	0.94	0.63
175	0.81	0.54
200	0.71	0.47
250	0.57	0.38
300	0.47	0.31
350	0.40	0.27
400	0.35	0.24
450	0.31	0.21
500	0.28	0.19
550	0.26	0.17
V_{DD} = 3.0 V, R_P (min) = 1.3 kΩ		
10	14.16	9.44
20	7.08	4.72
30	4.72	3.15
40	3.54	2.36
50	2.83	1.89
60	2.36	1.57
70	2.02	1.35

(table continues...)

Table 3 (continued) R_P (Min, Max) values for different bus loads and operating voltages

	R_P (Max) kΩ	
Freq	**1 MHz**	**3.4 MHz**
t_R (ps)	**120000**	**80000**
C_B (pF)		
80	1.77	1.18
90	1.57	1.05
100	1.42	0.94
125	1.13	0.76
150	0.94	0.63
175	0.81	0.54
200	0.71	0.47
250	0.57	0.38
300	0.47	0.31
350	0.40	0.27
400	0.35	0.24
450	0.31	0.21
500	0.28	0.19
550	0.26	0.17
V_{DD} = 2.7 V, R_P (min) = 1.15 kΩ		
10	14.16	9.44
20	7.08	4.72
30	4.72	3.15
40	3.54	2.36
50	2.83	1.89
60	2.36	1.57
70	2.02	1.35
80	1.77	1.18
90	1.57	1.05
100	1.42	0.94
125	1.13	0.76
150	0.94	0.63
175	0.81	0.54
200	0.71	0.47
250	0.57	0.38

(table continues...)

Table 3 (continued) R_P (Min, Max) values for different bus loads and operating voltages

	R_P (Max) kΩ	
Freq	**1 MHz**	**3.4 MHz**
t_R (ps)	**120000**	**80000**
C_B (pF)		
300	0.47	0.31
350	0.40	0.27
400	0.35	0.24
450	0.31	0.21
500	0.28	0.19
550	0.26	0.17
V_{DD} = 2.0 V, R_P (min) = 0.8 kΩ		
10	14.16	9.44
20	7.08	4.72
30	4.72	3.15
40	3.54	2.36
50	2.83	1.89
60	2.36	1.57
70	2.02	1.35
80	1.77	1.18
90	1.57	1.05
100	1.42	0.94
125	1.13	0.76
150	0.94	0.63
175	0.81	0.54
200	0.71	0.47
250	0.57	0.38
300	0.47	0.31
350	0.40	0.27
400	0.35	0.24
450	0.31	0.21
500	0.28	0.19
550	0.26	0.17

5 I²C F-RAM operation

The following sections briefly explain the I²C F-RAM operation. For a detailed explanation, refer to the respective datasheets.

5.1 WP pin

The WP (Write Protect) pin protects the entire memory when pulled to V_{DD}. It can be controlled by the microcontroller through a GPIO. For an application that does not use the write protect feature, this pin can be left floating. An internal pull-down will make the pin LOW.

5.2 A0, A1, A2 pins

The A0, A1, A2 pins control the device address selection for the I²C F-RAM device. They are internally pulled to LOW, so the default device address is 000 when these pins are left unconnected (floating). With different combinations of A0, A1, A2 settings, a maximum of eight F-RAM devices can be connected to the same I²C bus. Most I²C F-RAM devices have all three device address select pins. The exceptions are the 4-Kb and 1-Mb devices, which do not have the A0 pin, and the 16-Kb devices, which have none of the address select pins.

5.3 Slave address

The I²C F-RAM slave address is a 7-bit ID that includes fixed 4-bit slave id 1010b and user-configurable 3-bit device select bits (determined by the A0, A1, and A2 pins).

5.4 Address bytes

Based on the memory density, the I²C F-RAM read/write has 1- or 2-byte addresses, as shown in Table 4.

Table 4 Address bits for different densities of I²C F-RAM

Density	Slave address byte								Address byte 2 (MSB)								Address byte 1 (LSB)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4 Kb	Slave device address				A2	A1[1)]	A8[1)]	R/$\overline{W}$	N/A[2)]								A7	A6	A5	A4	A3	A2	A1	A0
16 Kb	Slave device address				A10 [1)]	A9[1)]	A8[1)]	R/$\overline{W}$	N/A[2)]								A7	A6	A5	A4	A3	A2	A1	A0
64 Kb	Slave device address				A2	A1	A0	R/$\overline{W}$	X[3)]	X[3)]	X[3)]	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128 Kb	Slave device address				A2	A1	A0	R/$\overline{W}$	X[3)]	X[3)]	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
256 Kb	Slave device address				A2	A1	A0	R/$\overline{W}$	X[3)]	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512 Kb	Slave device address				A2	A1	A0	R/$\overline{W}$	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1 Mb	Slave device address				A2	A1	A16 [1)]	R/$\overline{W}$	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

1) This is the page select address bit.
2) 4-Kb and 16-Kb density F-RAMs have a 1-byte address.
3) Unused bits of the most significant address byte are don't care bits, and F-RAM ignores them. However, the best practice is to set the unused address bit locations to '0' in the firmware. This approach makes it easy to upgrade the firmware when moving to a higher density option in the future.

5.5 Write operation

All writes start with the master sending a slave address that identifies the device for communication on the I²C bus. The write operation is indicated by setting the least significant bit of the slave address (R/$\overline{W}$ bit) to a '0'. The slave address is then followed by a 2-byte or 1-byte address based on the density of the F-RAM device, as listed in Table 4. For 4-Kb, 16-Kb, and 1-Mb I²C F-RAM devices, the slave address contains a few of the most significant bits of the memory address. The address is followed by the data to be written. For each byte, the F-RAM slave generates an Acknowledge. The write operation is terminated with a STOP condition.

Figure 6 shows single-byte write, Figure 7 shows multi-byte write, and Figure 8 shows high-speed write. Hs-mode requires the Hs-mode command (0x08) before the write operation starts.

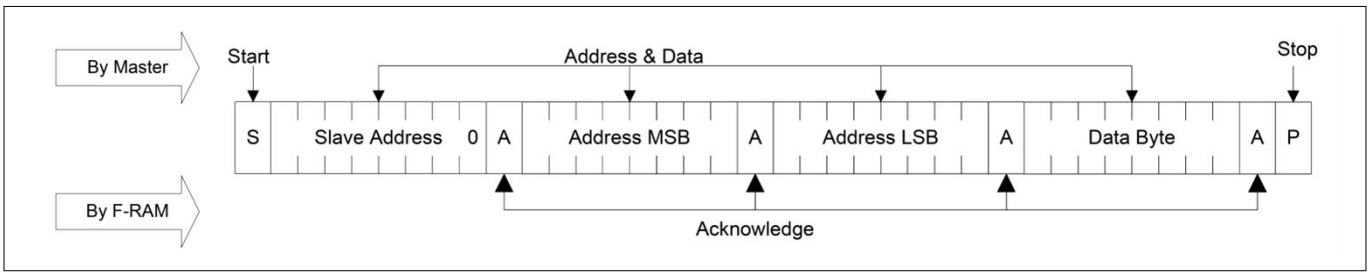


Figure 6 Single-byte write operation (256-Kb F-RAM)

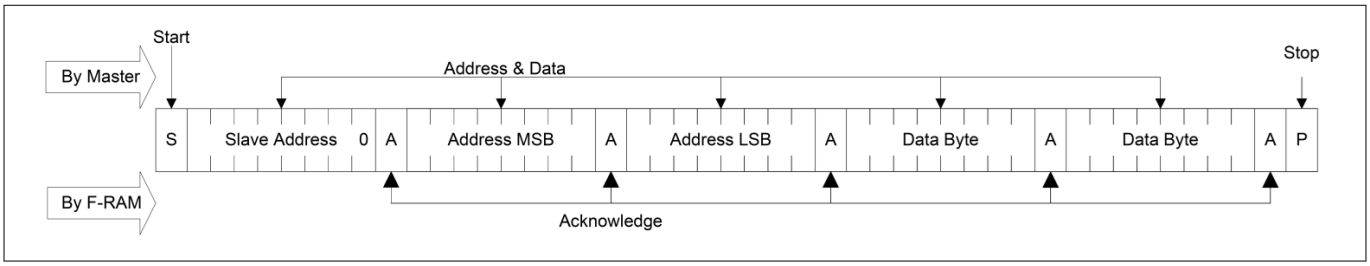


Figure 7 Multi-byte write operation (256-Kb F-RAM)

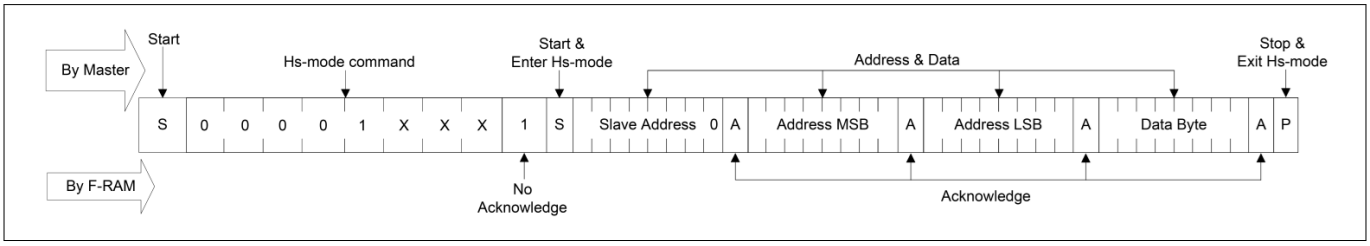


Figure 8 HS-mode single-byte write operation (256-Kb F-RAM)

5.6 Read operation

The read operation involves either current address or selective (random) address reads. In current address reads, shown in Figure 9, Figure 10, and Figure 11, the I²C F-RAM uses the address latched internally in the last read/write operation. In selective (random) address read, shown in Figure 12, the address from which the data is being read is specified.

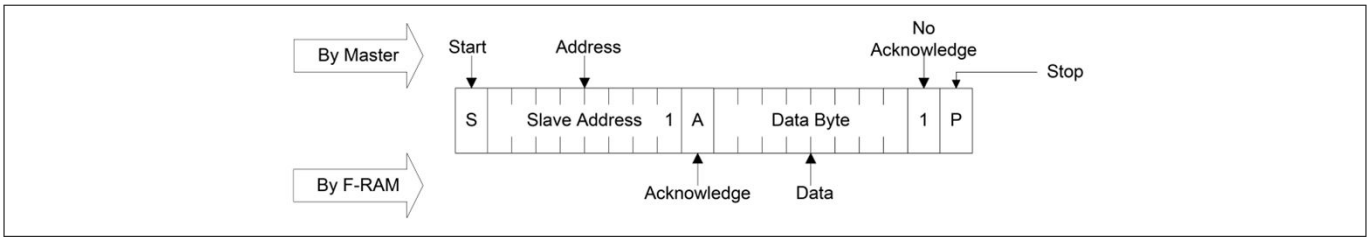


Figure 9 Single-byte current address read operation (256-Kb F-RAM)

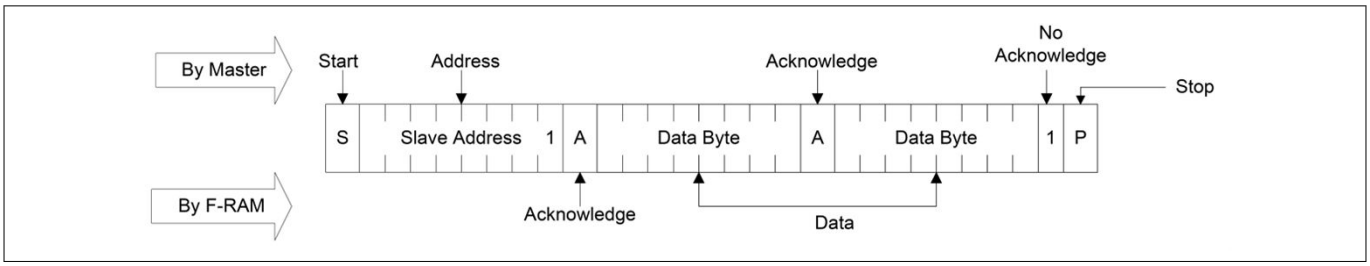


Figure 10 Multi-byte (Sequential) current address read operation (256-Kb F-RAM)

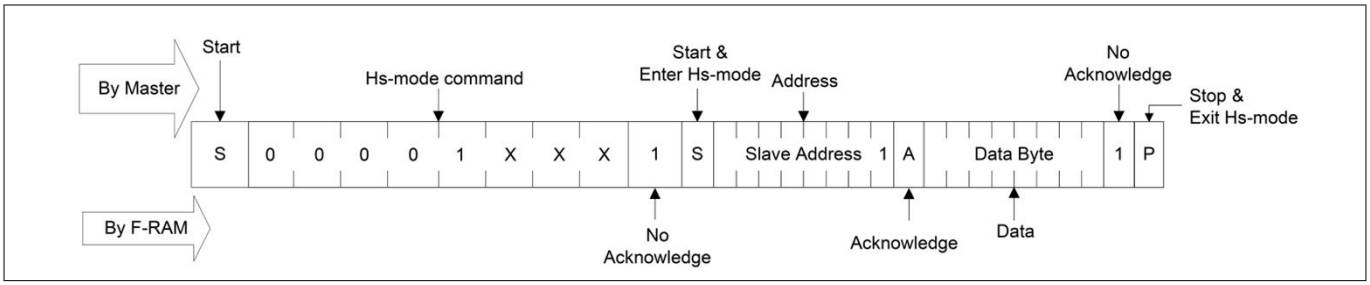


Figure 11 HS-mode single-byte current address read operation (256-Kb F-RAM)

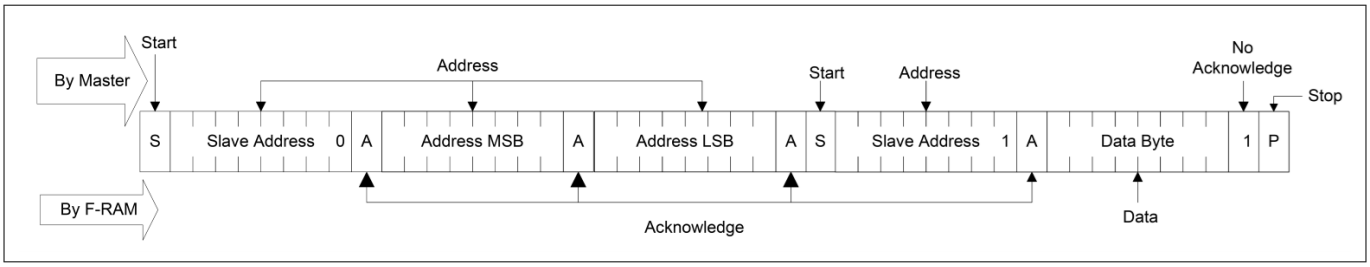


Figure 12 Single-byte selective (Random) address read operation (256-Kb F-RAM)

5.7 Sleep mode entry

A low-power mode called “sleep mode” is implemented in some I²C F-RAM devices, as listed in Table 2. The F-RAM device enters sleep mode through the command 0x86, as shown in Figure 13.

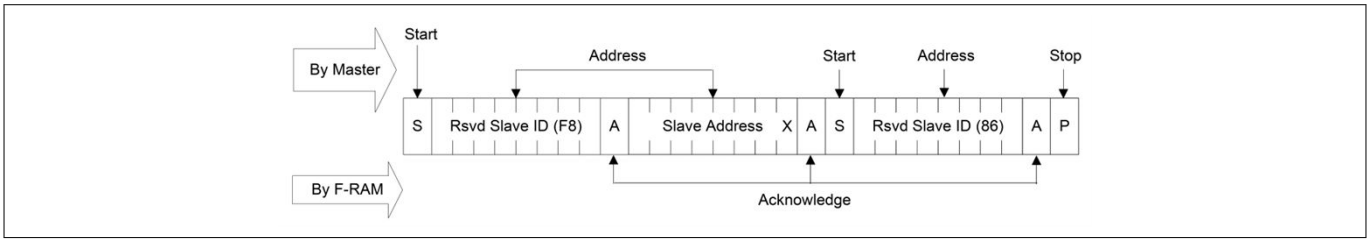


Figure 13 Sleep mode entry

5.8 Device ID

Most F-RAM products define a three byte Device ID, which consists of a Manufacturing ID and a Product ID. It can be read through the command 0xF9, as shown in Figure 14.

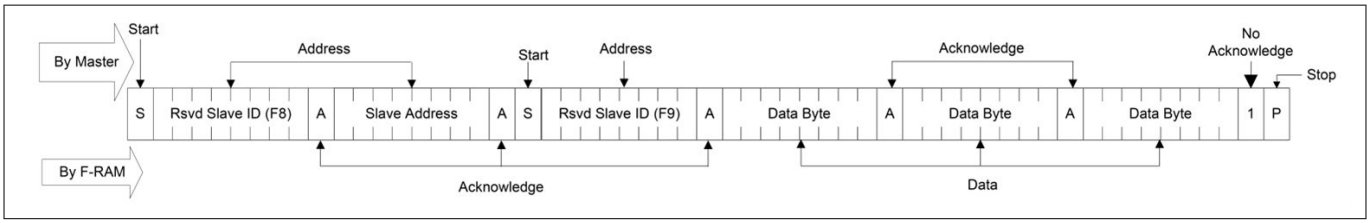


Figure 14 Read device ID

5.9 Serial number

FM24VN10 defines a serial number that is unique to each device and read only. It is an 8-byte number that can be read through the command 0xCD, as shown in Figure 15

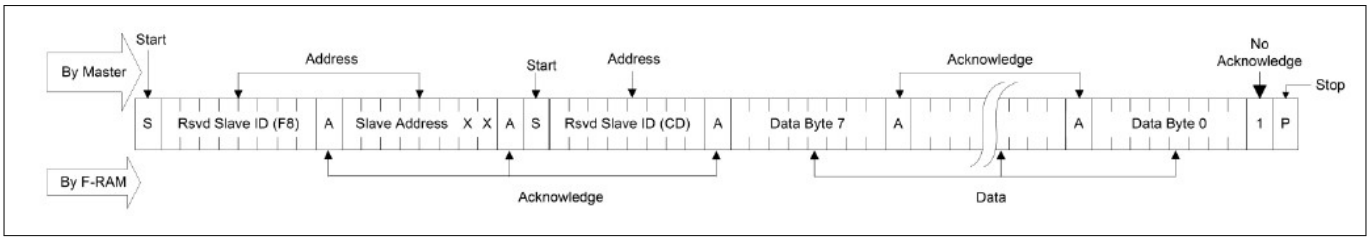


Figure 15 Read serial number

6 I2 C F-RAM Code Example

I²C F-RAM code example can be found in the application note “AN74875 - Designing with Serial I²C nvSRAM”. AN74875 provides an associated project, which has a PSOC™ Creator Component (nvRAM) for Infineon’s nonvolatile RAM products (nvSRAM and F-RAM). The PSOC™ Creator Component provides APIs to read and write from the memory. They also have APIs to execute device ID, serial number, and sleep mode entry.

7 Summary

This application note provides guidelines for designing applications with Infineon I²C F-RAM. The I²C F-RAM supports the standard I²C access protocols, similar to any other nonvolatile I²C memory products. This makes the F-RAM compatible with all I²C master controllers and reduces system development cycle time.

References

[1] *AN407 - A Design Guide to I²C F-RAM Processor Companions*; Available online
[2] *AN94901 - Migrating from FM24V02/FM24V01 to FM24V02A/FM24V01A*; Available online

Revision history

Document version	Date of release	Description of changes
**	2015-06-29	• Initial release
*A	2015-07-31	• Fixed formatting issues in Table 4
*B	2018-07-11	• Updated template
*C	2026-01-05	• Template update; no content update

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Edition 2026-01-05

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-tqy1752569418412

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