Designing with Infineon ONFI 1.0 nvSRAM

About this document

Scope and purpose

AN91206 provides details of the Open NAND flash Interface 1.0 (ONFI Version 1.0) nvSRAM command structure, command cycles, address cycles, and data cycles. These details will help you design with Infineon's ONFI 1.0 nvSRAM in a system. AN91206 also highlights the key differences between the ONFI 1.0 nvSRAM and ONFI 1.0 compliant NAND flash memory architecture, opcode, and functions to help you make necessary changes in the firmware program to allow you to access all features of the ONFI 1.0 nvSRAM using the standard ONFI 1.0 system bus.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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1 Introduction

The ONFI 1.0 nvSRAM follows the majority of the ONFI 1.0 standards which makes this device interoperable with all standard ONFI 1.0 host controllers. The ONFI 1.0 nvSRAM protocols are identical to the ONFI 1.0 standard, so can share the ONFI 1.0 bus with the other ONFI 1.0-compliant NAND flash devices in a system.

ONFI is an industry workgroup dedicated to simplifying NAND flash memory integration into consumer electronic products. ONFI defines standardized component-level interface specifications, standard command sets for device operation, and standard timing requirements. The nvSRAM integrates an SRAM cell and a silicon-oxide-nitride-oxide-silicon (SONOS)-based nonvolatile cell into a single nvSRAM cell.

The nvSRAM combines the best features of an SRAM and a nonvolatile memory, which makes it the fastest and the most reliable nonvolatile memory solution in the industry.

For more information on nvSRAM technology and functionalities, see the Infineon white paper. Refer to device datasheet the for more details on the ONFI 1.0 nvSRAM timing diagrams, and DC/AC specifications.

This application note describes the ONFI 1.0 nvSRAM architecture, protocols, and key differences from ONFI 1.0 standard. This application note also provides an example circuit for interfacing an ONFI 1.0 nvSRAM with a standard ONFI 1.0 controller.

2 nvSRAMs Versus NAND Flash

The nvSRAM differs from the NAND flash memory in design, cell architecture, and the process technology. Table 1 provides a high-level comparison between the nvSRAM and NAND flash memory technologies.

Table 1 nvSRAM Versus NAND Flash memory

Parameters	nvSRAM	NAND Flash
Nonvolatile memory cell	SONOS (Silicon-Oxide-Nitride-Oxide-Silicon)	Floating gate
Erase Cycle	Not applicable	Memory block must be erased before programming with new data
Page program cycle time	Not applicable. Data is always written to the SRAM array and is automatically saved to the nonvolatile memory at power down	Typically 200 µs to 300 µs
Endurance	1,000,000 cycles (nonvolatile cell)	100,000 cycles
Data retention	20 years @ 85 °C	10 years @ 85 °C
Page Write	Writes the entire memory array at bus speed	The Page Write operation writes in the page buffer at bus speed. However, every page write is followed by the page program cycle to transfer the data from the page buffer to the NAND flash memory.
Page Read	Reads the entire memory array at bus speed	The Page Read operation reads from the page buffer at bus speed. However, after every page read command, the system needs to wait for “t_R” time before the data is available for access.
Page size	Not applicable. The entire memory can be accessed as a single page when executing bulk write and bulk read operations	2 KB or above
Block size	Not applicable	64 pages or above

3 ONFI 1.0 nvSRAM architecture

ONFI 1.0 is a highly multiplexed x8 I/O (DQ[7:0]) and x16 I/O (DQ[15:0]) architecture to transmit the command, address, and data bytes over the same I/O bus. In the x8 interface, the command, address, and data bytes are transmitted over the same bus. In the x16 interface, the command and address bytes are always transmitted over the lower 8-bit bus, while the data words are transmitted over the 16-bit bus, but only for the main memory write and read operations. Other read operations such as Status Register, Device ID, and Parameter Page Transmit always occur over the lower 8-bit bus of the x16 I/O interface.

Figure 1 shows the ONFI 1.0 nvSRAM block diagram with I/Os (DQ[15:0]) interface details.

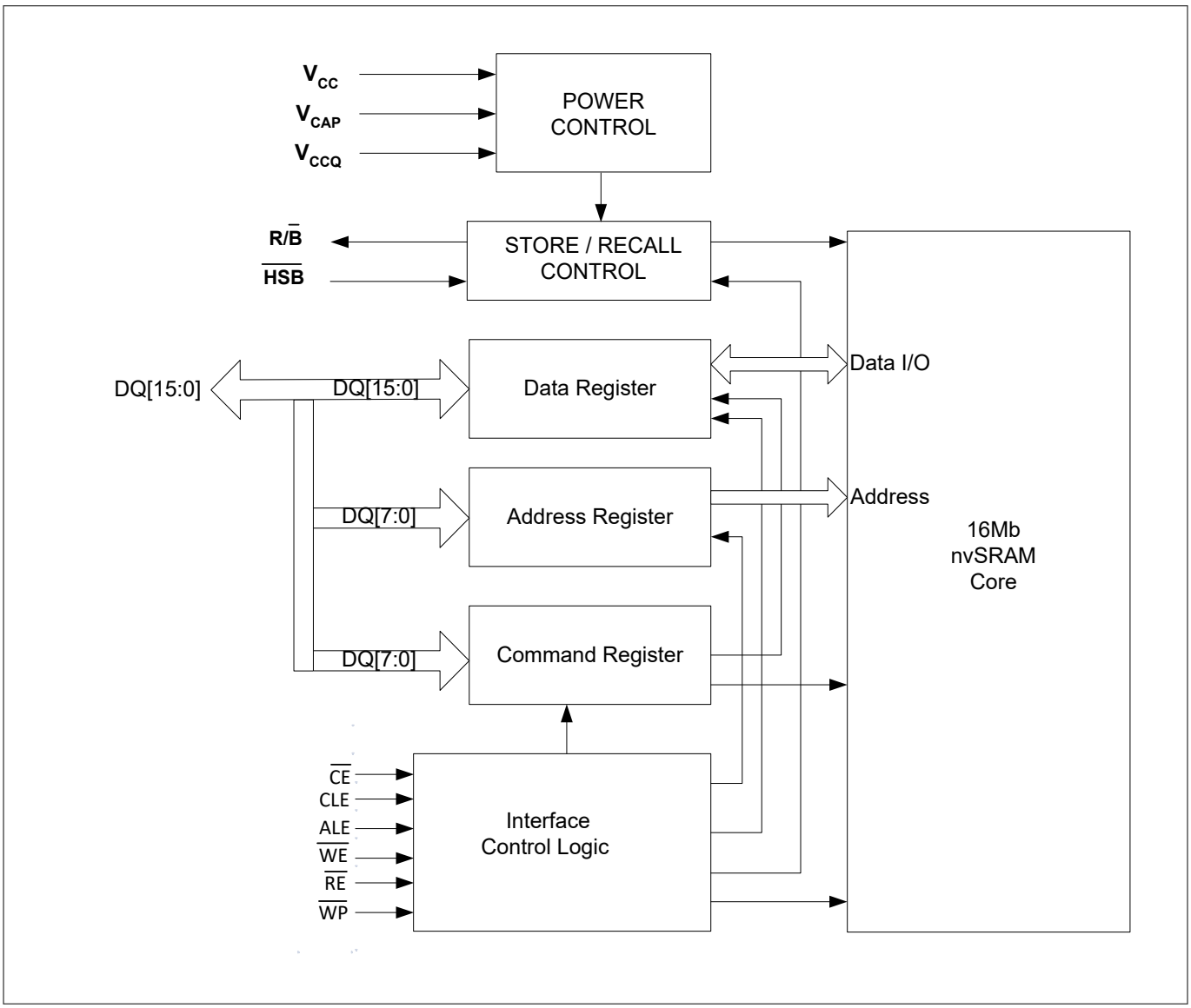


Figure 1 ONFI 1.0 nvSRAM Block diagram

3.1 Memory organization

The ONFI 1.0 NAND flash supports a hierarchal architecture, and the entire memory is divided into several pages, blocks, and planes. The ONFI 1.0 nvSRAM does not support the hierarchal architecture, so the entire memory array can be treated as a single page or a single block of memory.

Figure 2 illustrates the memory organization differences between the NAND flash and the nvSRAM architecture.

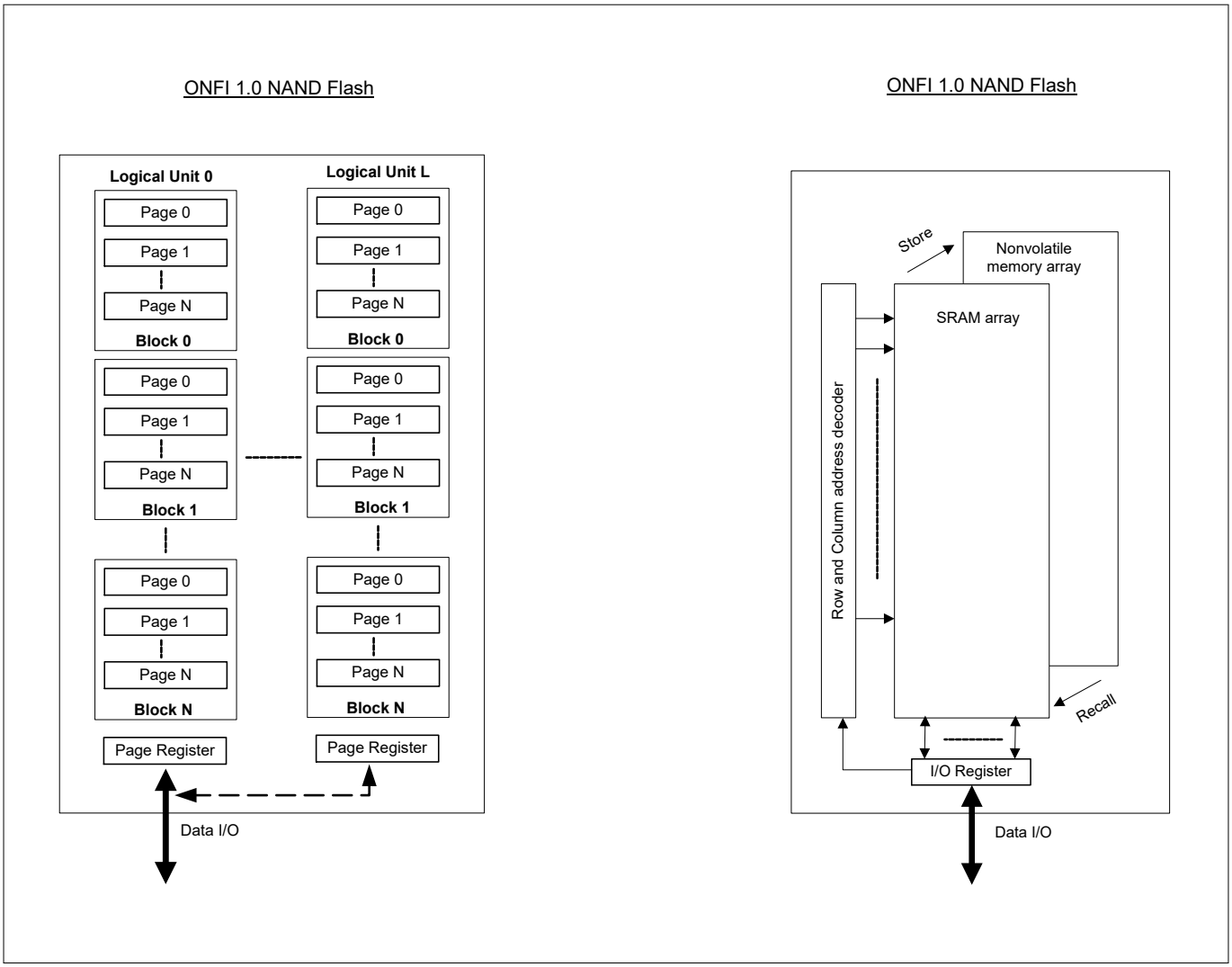


Figure 2 ONFI 1.0 NAND Flash and nvSRAM memory architecture

3.2 ONFI 1.0 nvSRAM Data Interface

The ONFI 1.0 control signals CLE, ALE, $\overline{WE}$, and $\overline{RE}$ are used to determine the command, address, data write, and data read accesses on the multiplexed I/O bus of the ONFI 1.0 nvSRAM. The write protect pin ($\overline{WP}$) enables or disables SRAM write in ONFI 1.0 nvSRAM. The $\overline{CE}$ control is used to select the device for access on the ONFI 1.0 bus. Table 2 shows the ONFI 1.0 nvSRAM bus state for different states of the input control signals.

Refer to the device datasheet for the AC/DC specifications and parameter details used in this application note.

Table 2 ONFI 1.0 nvSRAM Bus state

$\overline{CE}$	ALE	CLE	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	BUS STATE	COMMENTS
1	X	X	X	X	X	Standby	The nvSRAM enters the low-power standby mode when the device status is ready and R/$\overline{B}$ is pulled HIGH by the external pull-up resistor. When $\overline{CE}$ is disabled, all nvSRAM I/Os are disabled except $\overline{WP}$, R/$\overline{B}$, and $\overline{HSB}$.

(table continues...)

Table 2 (continued) ONFI 1.0 nvSRAM Bus state

$\overline{CE}$	ALE	CLE	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	BUS STATE	COMMENTS
0	0	0	1	1	X	Bus Idle	Bus is in the idle state. All inputs are enabled but the commands, addresses, and data bytes are ignored. There is also no data output from the device.
0	0	1	0	1	X	Command cycle	Latch the data byte as a command on the bus.
0	1	0	0	1	X	Address cycle	Latch the data byte as an address on the bus.
0	0	0	0	1	H	Write Cycle	Latch the data on the data bus for write.
0	0	0	1	0	X	Read Cycle	Send the data on bus for read.
0	1	1	X	X	X	Undefined	ONFI 1.0 doesn't specify the device state for this input signal condition; so, it is described as an undefined bus state in the ONFI 1.0 nvSRAM.
0	0	0	0	1	L	Write protect to SRAM	$\overline{WP}$ is toggled before initiating the SRAM write to prevent the write operation on the SRAM.

3.3 Command cycle

A command is written from DQ[7:0] to the command register on the rising edge of the $\overline{WE}$ control when $\overline{CE}$ is LOW, ALE is LOW, CLE is HIGH, and $\overline{RE}$ is HIGH. Figure 3 shows the command cycle timing.

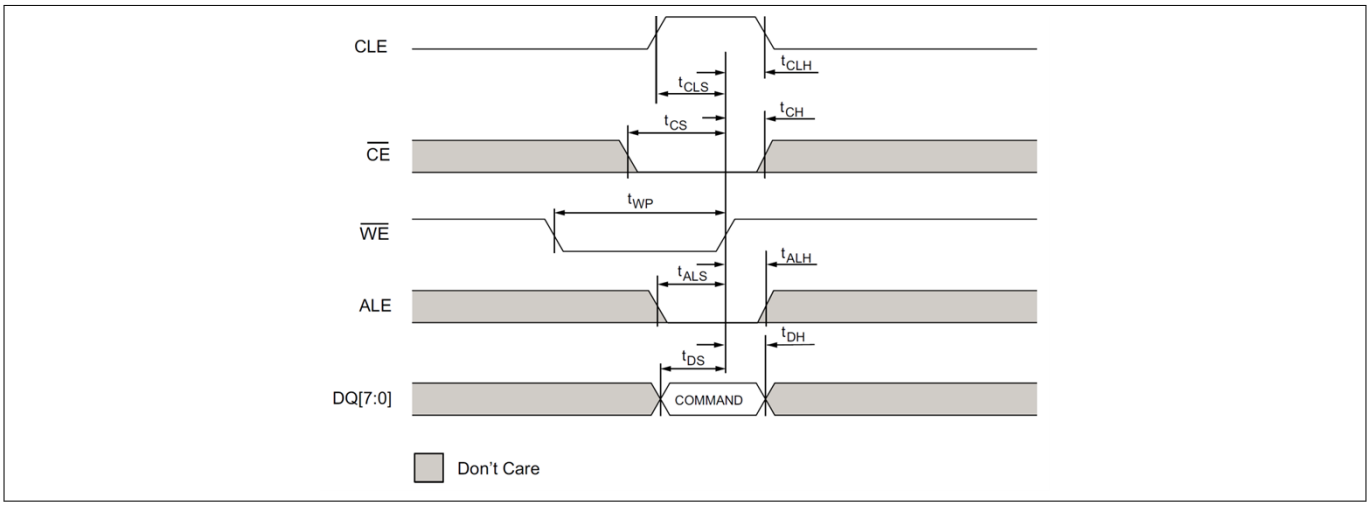


Figure 3 ONFI 1.0 nvSRAM Command cycle timing

3.4 Address cycle

An address is written from DQ[7:0] to the address register on the rising edge of the $\overline{WE}$ control when $\overline{CE}$ is LOW, ALE is HIGH, CLE is LOW, and $\overline{RE}$ is HIGH. In five-byte addressing, the least significant address byte is sent in the first address cycle and the most significant address byte is sent in the fifth address cycle. The nvSRAM requires only the first three address bytes to address its entire 16 Mb memory. The two extra MSBs are "Don't Care" address bytes. Figure 4 shows the address cycle timing.

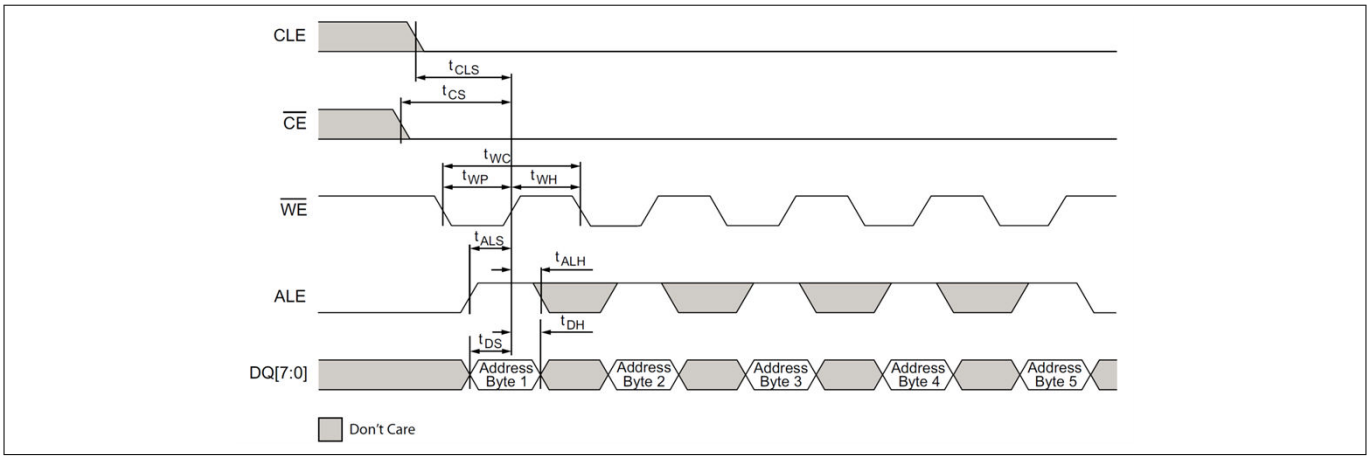


Figure 4 ONFI 1.0 nvSRAM Address cycle timing

3.5 Data input cycle (write cycle)

The data byte/word is written from DQ (DQ[7:0] or DQ[15:0]) to the data register of the nvSRAM on the rising edge of the $\overline{WE}$ control when $\overline{CE}$ is LOW, ALE is LOW, CLE is LOW, and $\overline{RE}$ is HIGH. Figure 5 shows the Data Input (Write) cycle timing.

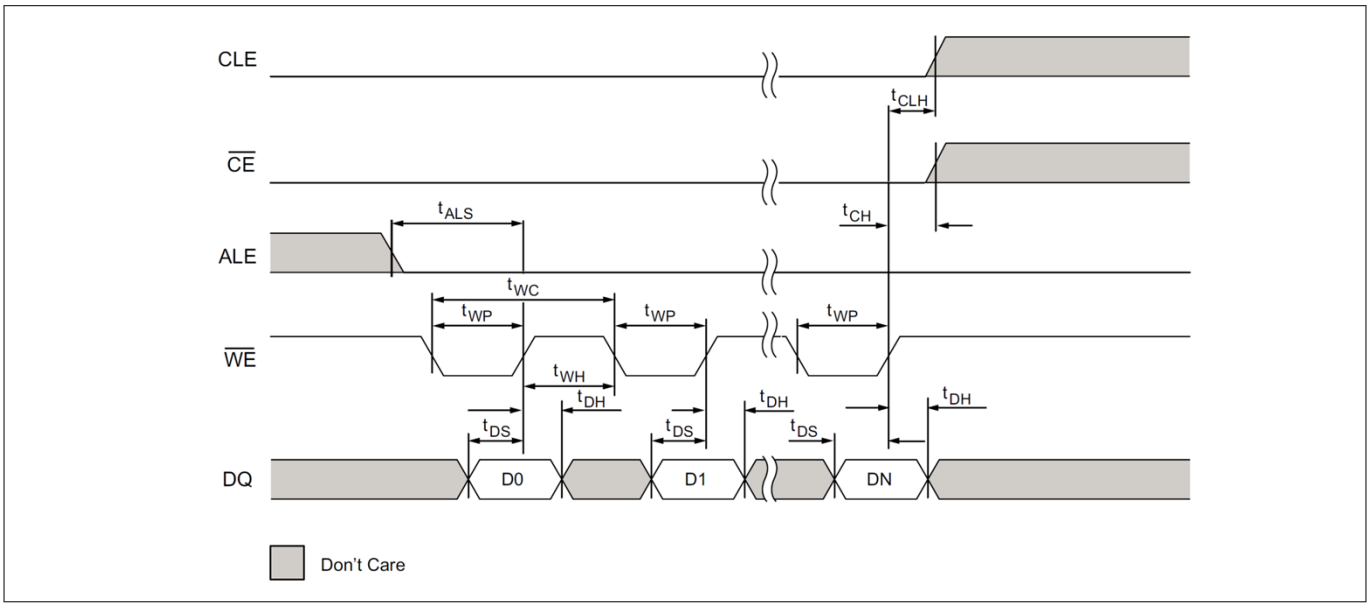


Figure 5 ONFI 1.0 nvSRAM Data input (write) cycle timing

3.6 Data output cycle (read cycle)

The data byte/word is sent out (during read) on the DQ bus (DQ[7:0] or DQ[15:0]) by the nvSRAM if its status is ready. Data is output from the data register on every falling edge of the $\overline{RE}$ control when $\overline{CE}$ is LOW, ALE is LOW, CLE is LOW, and $\overline{WE}$ is HIGH. Figure 6 shows the Data Output (Read) cycle timing.

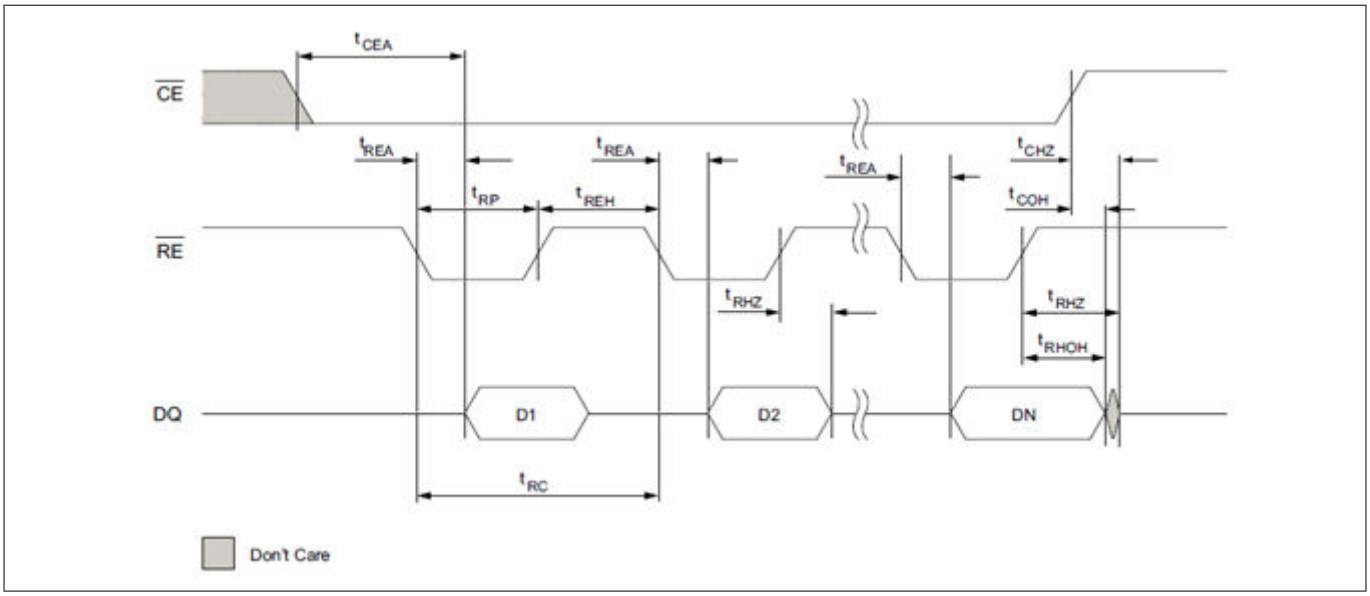


Figure 6 ONFI 1.0 nvSRAM Data output (read) cycle timing

3.7 ONFI 1.0 nvSRAM access op-codes and protocols

Table 3 lists the command, address, and data cycles for executing each of the following commands for ONFI 1.0 nvSRAM access.

Table 3 ONFI 1.0 nvSRAM commands

NVSRAM Function	Command Cycle1	Address Cycle/s	Data Cycle/s	Command Cycle 2	Description
Read from SRAM	00 h	Memory address (5 Bytes)	-	30 h	Reads the data from the SRAM address location transmitted in the five address bytes.
Write into SRAM	80 h,	Memory address (5 Bytes)	(1 to N)	10 h	Writes the data into the SRAM address location transmitted in the five bytes address. The length of the data bytes can be anywhere between 1 to N. The maximum value of N is the full-memory array.
Read Status Register	70 h	-	-	-	Reads the status of the device.
Read ID (ONFI Signature)	90 h	20 h (1 Byte)	-	-	Reads four bytes of the ONFI signature.
Read ID (Manufacturer ID and Device ID)	90 h	00 h (1 Byte)	-	-	Reads the four bytes of the manufacturer ID (two bytes MID and two bytes DID)

(table continues...)

Table 3 (continued) ONFI 1.0 nvSRAM commands

NVSRAM Function	Command Cycle1	Address Cycle/s	Data Cycle/s	Command Cycle 2	Description
Read Parameter Page	ECh	00 h (1 Byte)	-	-	The read parameter page function reads the data structure that describes the target's organization, features, timings, and other behavioral parameters.
Reset	FFh	-	-	-	Aborts the current operation (all writes and reads) and puts the NVSRAM into the default state. If a nonvolatile operation is in progress, it will be completed first and then the Reset request will be serviced.
ONFI 1.0 nvSRAM-Specific Commands, Not Applicable to NAND Flash					
Software Recall	FCh	-	-	-	This initiates the Recall operation to transfer data from the nonvolatile memory to the SRAM. This command is not an ONFI 1.0 standard command.
Software Store	84 h	-	-	A5h	This initiates the Store operation to transfer data from the SRAM to the nonvolatile memory. This command is not an ONFI 1.0 standard command.
AutoStore Disable	A3h	-	-	-	This command disables the AutoStore function in the ONFI 1.0 nvSRAM. This command is not an ONFI 1.0 standard command.
AutoStore Enable	ACh	-	-	-	This command enables the AutoStore function in the ONFI 1.0 nvSRAM. A capacitor of an appropriate value must be connected to the V_{CAP} pin to perform AutoStore on power loss. This command is not an ONFI 1.0 standard command.

(table continues...)

Table 3 (continued) ONFI 1.0 nvSRAM commands

NVSRAM Function	Command Cycle1	Address Cycle/s	Data Cycle/s	Command Cycle 2	Description
Reserved Commands					
Get Features	EEh	-	-	-	These are reserved commands in the ONFI 1.0 nvSRAM.
Set Features	EFh	-	-	-	

Table 4 ONFI 1.0 Flash commands not applicable to nvSRAM

NAND Flash Function	Command Cycle 1	Address Cycle/s	Data Cycle/s	Command Cycle 2	Description
Copyback Read	00h	5 Bytes	-	35 h	These commands are not applicable to the ONFI 1.0 nvSRAM.
Change Read Column	05 h		-	E0h	
Read Cache Enhanced	00 h	5 Bytes	-	31 h	
Read Cache	31 h	-	-	-	
Read Cache End	3 Fh	-	-	-	
Block Erase	60 h	3 Bytes	-	D0h	
Interleaved	60 h	3 Bytes	-	D1h	
Read Status Enhanced	78 h	3 Bytes	-	-	
Page Program Interleaved	80 h	5 Bytes	Yes	11 h	
Page Cache Program	80 h	5 Bytes	Yes	15 h	
Copyback Program	85 h	5 Bytes	Yes	10 h	
Copyback Program Interleaved	85 h	5 Bytes	Yes	11 h	
Change Write Column	85 h	2 Bytes	Yes		
Read unique ID	EDh	1 Bytes	-	-	

3.8 ONFI 1.0 Command description and timings

This section describes the ONFI 1.0 nvSRAM access command cycle timings. This also highlights differences from the ONFI 1.0 NAND flash wherever applicable. All commands except the status register read (70 h) and reset (FFh) are ignored when the nvSRAM is busy (RDY bit is set to ‘0’ in the status register).

3.8.1 Read (00 h, 30 h)

3.8.1.1 ONFI 1.0 nvSRAM

The ONFI 1.0 nvSRAM Read command reads the data-bytes (on the x8 interface) or data words (on the x16 interface). After receiving Read command cycles, the nvSRAM enters the data output mode (Read mode) and starts sending the data out on its data bus for every $\overline{RE}$ toggle ($\overline{CE}$ remains LOW) or $\overline{CE}$ toggle ($\overline{RE}$ remains LOW). The address counter advances to the next accessible location automatically. The device comes out of the Read mode only when a new command cycle is received (command or address cycle, either valid or invalid). The Read command can be used either for accessing a single byte/word or for burst access. The maximum length of the data burst in the ONFI 1.0 nvSRAM is the memory array size.

Figure 7 shows the ONFI 1.0 nvSRAM Read cycle timing.

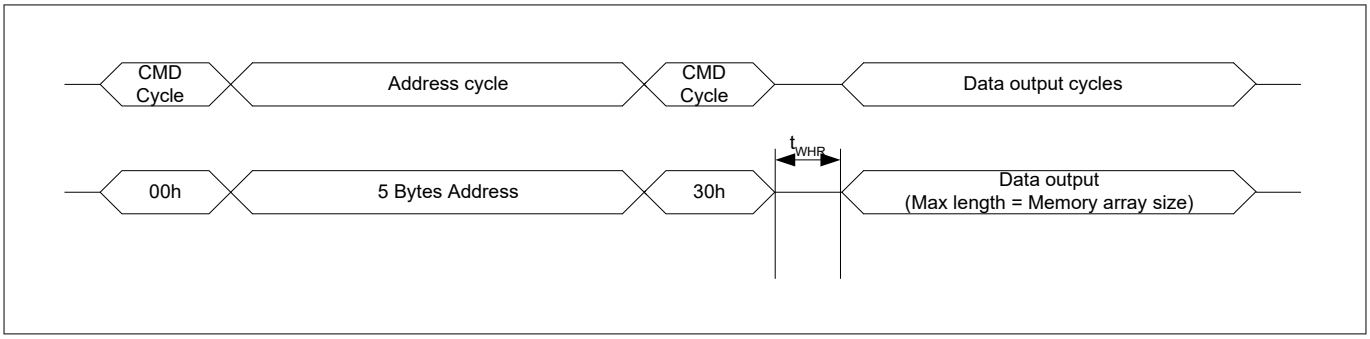


Figure 7 ONFI 1.0 nvSRAM Read cycle

3.8.1.2 ONFI 1.0 NAND Flash

The ONFI 1.0 NAND flash Page Read command is identical to the ONFI 1.0 nvSRAM except that the page data is available only $t_R$time after the 30 h command is transmitted. The t_R time is the wait time to transfer data from the flash array to the data memory register before it is available on the data bus.

The flash Read (Page Read) command is used either to access a single byte/word or a burst of data bytes/words. The maximum size of the data burst in the flash memory can be equal to its page size. Figure 8 shows the ONFI 1.0 NAND flash Read cycle timing.

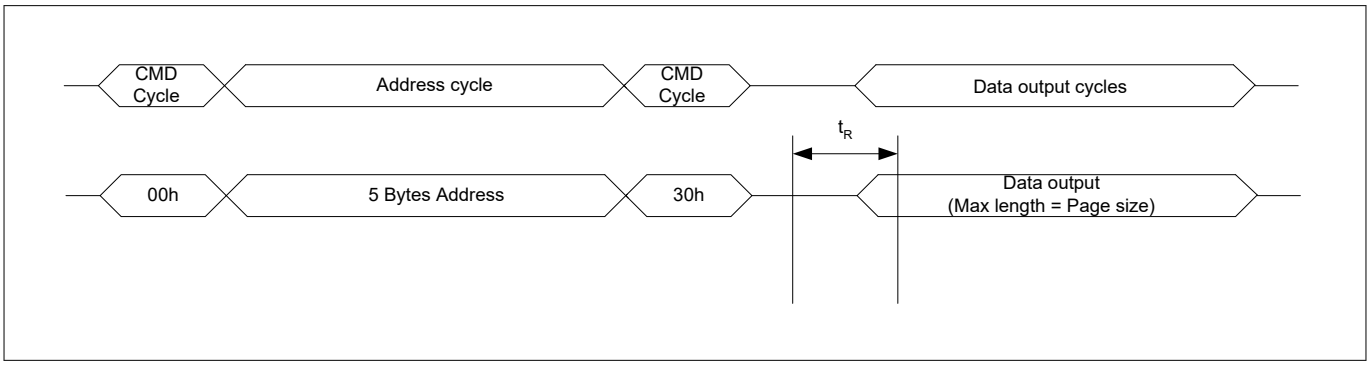


Figure 8 ONFI 1.0 NAND Flash read cycle

3.8.2 Write (80 h, 10 h)

3.8.2.1 ONFI 1.0 nvSRAM

The ONFI 1.0 nvSRAM Write command writes the data-bytes (on the x8 interface) or data words (on the x16 interface). After receiving a valid write command and address cycles, all subsequent data bytes or words are written directly in the SRAM of the nvSRAM. The device comes out of the Write mode only when a new command cycle is received (command or address cycle, valid or invalid).

The Write command can write either a single data word or a data burst. All data bytes are written to the SRAM array immediately and transferred to the nonvolatile memory array automatically on power down (AutoStore). The 10h command at the end of the write cycle is to make the ONFI 1.0 nvSRAM protocol compatible to the ONFI 1.0 standard, but this is an optional command for the ONFI 1.0 nvSRAM. The ONFI 1.0 nvSRAM write will be successful even without executing the 10 h command.

Figure 9 shows the ONFI 1.0 nvSRAM Write cycle timing.

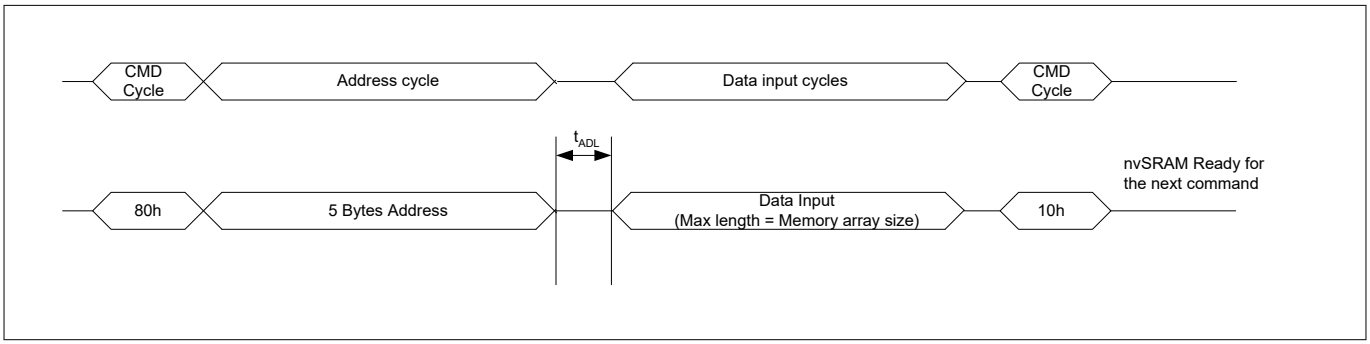


Figure 9 ONFI 1.0 nvSRAM Write cycle

3.8.2.2 ONFI 1.0 NAND Flash

The ONFI 1.0 NAND flash Page Write command is identical to the ONFI 1.0 nvSRAM write except that the page data is programmed into the nonvolatile memory only after the 10 h command is received. The NAND flash\ takes t_{PROG} time to complete the page program cycle before the flash is accessible for a new page write or read operation.

The NAND flash Write (Page Write) command is either used to write a single byte/word or a burst of data bytes/ words. The maximum size of the data burst in the flash memory can be equal to its page size.

Figure 10 shows the ONFI 1.0 NAND flash Write cycle timing.

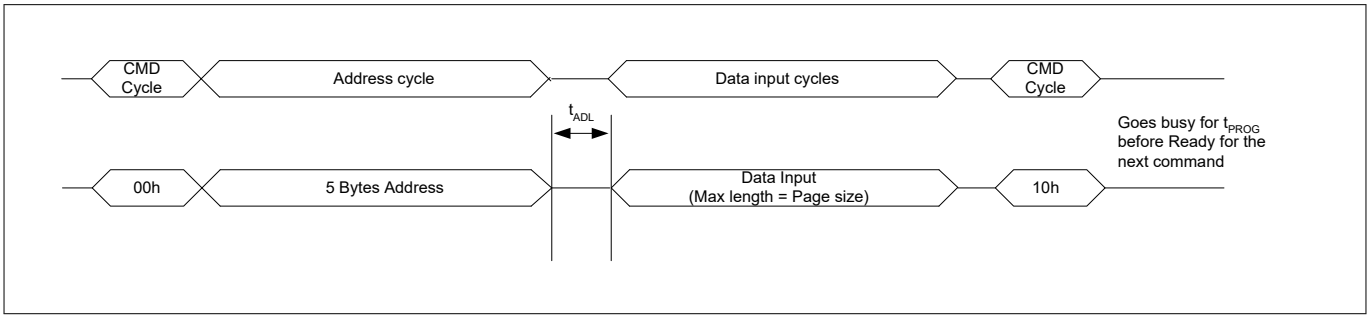


Figure 10 ONFI 1.0 NAND Flash Write cycle

3.8.3 Read parameter page (ECh)

3.8.3.1 ONFI 1.0 nvSRAM

The ONFI 1.0 nvSRAM Read Parameter Page command reads the parameter page data and outputs it on the 8-bit data bus for every $\overline{RE}$ toggle $\overline{CE}$ toggle. In x16 interface parts, the parameter page data outputs only on the lower 8-bit of x16 data bus; the upper 8-bit of the x16 data bus carries garbage data. The Parameter Page Read command always starts at the 00h address of the parameter page with an auto increment until the page boundary is reached. The Read Parameter Page command cannot access from the intermediate location of the Parameter Page. Figure 11 shows the ONFI 1.0 nvSRAM Parameter Page Read timing.

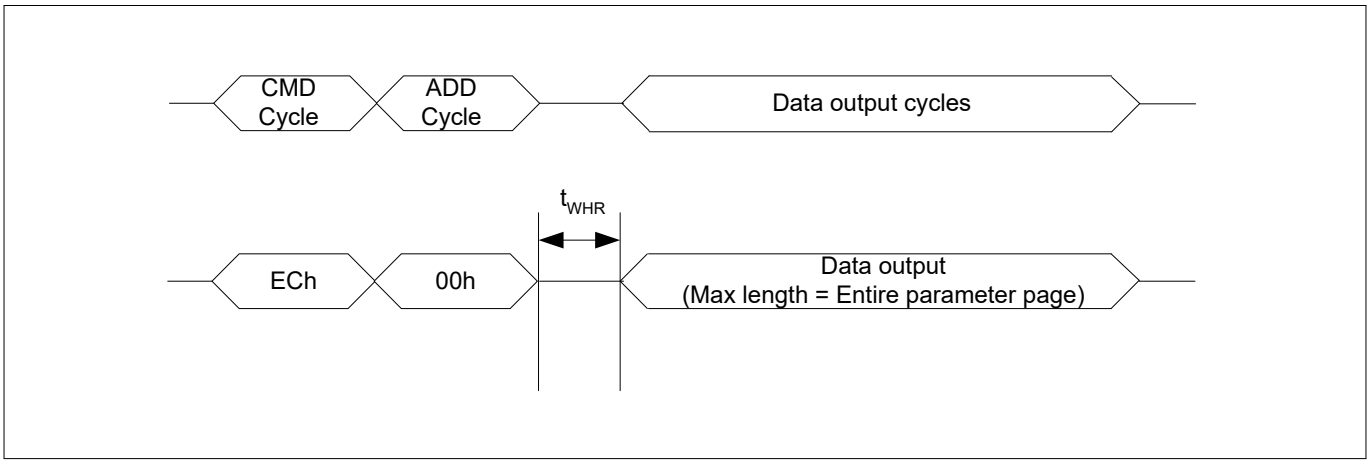


Figure 11 ONFI 1.0 nvSRAM Read Parameter Page cycle

3.8.3.2 ONFI 1.0 NAND Flash

The ONFI 1.0 NAND flash Read Parameter Page command is identical to the ONFI 1.0 nvSRAM except that the parameter page data is available only t_R time after the Read Parameter Page command is checked in.

The t_R time is the wait time to transfer the page data from the flash array to the data memory register. Figure 12 shows the ONFI 1.0 NAND flash Read Parameter Page timing.

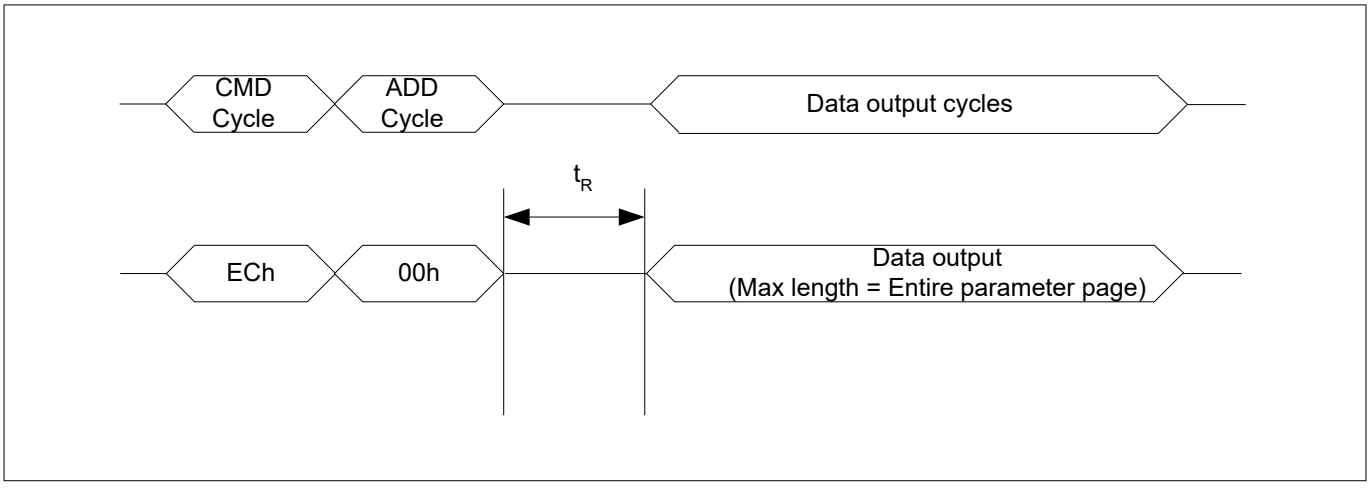


Figure 12 ONFI 1.0 NAND Flash Read Parameter Page cycle

3.8.4 Read status register (70 h)

3.8.4.1 ONFI 1.0 nvSRAM

The Read Status Register command reads the Status Register (SR) content on the 8-bit data bus. In x16 interface devices, the Status Register content is transmitted over the lower 8-bit of x16 data bus. Figure 13 shows the Read Status Register Cycle for the ONFI 1.0.

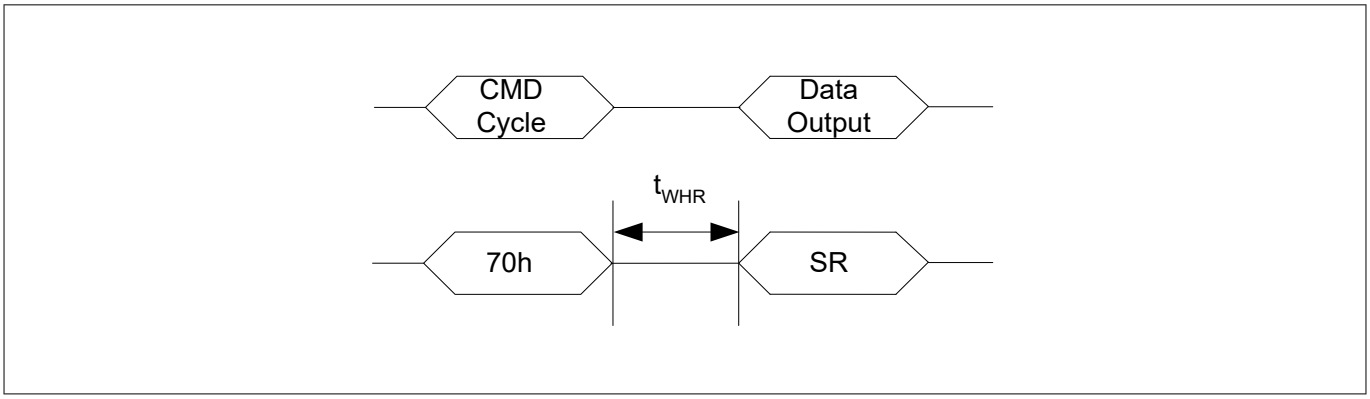


Figure 13 ONFI 1.0 Read Status register cycle

3.8.4.2 ONFI 1.0 NAND Flash

The timing diagram for the ONFI 1.0 NAND flash is the same as that of the ONFI 1.0 nvSRAM.

3.8.5 Read device ID (90 h) - Read ONFI signature

3.8.5.1 ONFI 1.0 nvSRAM

The Read Device ID command (90 h) with address byte 20 h reads the four-byte ONFI signature and outputs them on the 8-bit data bus. In x16 interface parts, the device outputs the signature bytes only on the lower 8-bit of the x16 data bus. Figure 14 shows the ONFI 1.0 Read Device ID cycle timing.

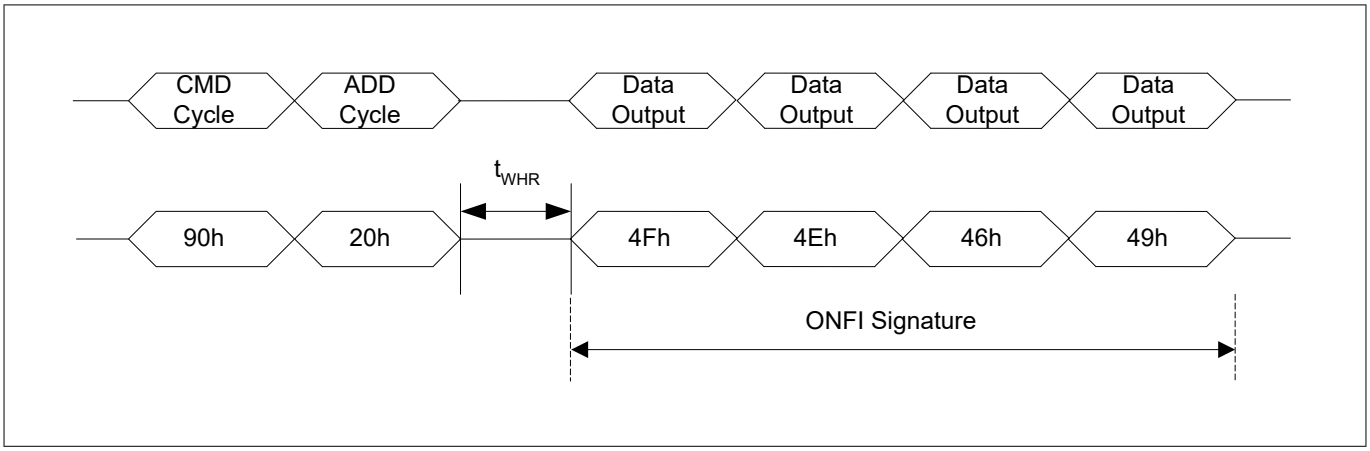


Figure 14 ONFI 1.0 Read Device ID (CMD = 90 h, ADD = 20 h) cycle

3.8.5.2 ONFI 1.0 NAND Flash

The timing diagram for the ONFI 1.0 NAND flash is the same as that of the ONFI 1.0 nvSRAM.

3.8.6 Read Device ID (90 h) - Read MID and DID

3.8.6.1 ONFI 1.0 nvSRAM

The Read Device ID command (90 h) with address byte 00 h reads the manufacturer ID (MID) and device ID (DID) and outputs them on the 8-bit data bus. In x16 interface parts, the device outputs the signature bytes only on the lower 8-bit part of the x16 data bus.

The ONFI 1.0 standard defines only the first two bytes for the MID and DID. Reading the device ID beyond the first two bytes yields values specified by the manufacturer datasheet.

The ONFI 1.0 nvSRAM returns four bytes as shown in Figure 15. The value for the MID and DID for x8 and x16 interface parts as follows:

ONFI 1.0 nvSRAM (x8):00 34 00 00h

ONFI 1.0 nvSRAM (x16):00 34 00 40h

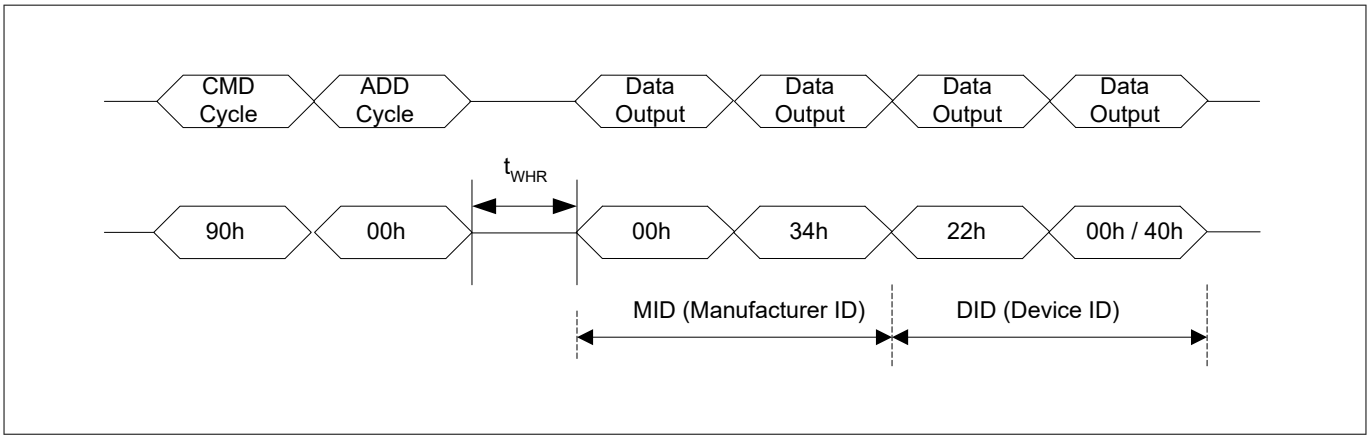


Figure 15 ONFI 1.0 Read Device ID (CMD = 90 h, ADD = 00 h) cycle

3.8.6.2 ONFI 1.0 NAND Flash

The ONFI 1.0 NAND flash behaves in an identical way to the ONFI 1.0 nvSRAM Read Device ID command except that the ONFI 1.0 NAND flash returns a 5-byte device ID.

3.8.7 Reset (FFh)

3.8.7.1 ONFI 1.0 nvSRAM

The Reset command puts the nvSRAM in its default power-up state. The Reset command can be executed when the device is in any state, except when ONFI 1.0 nvSRAM power-up RECALL cycle is in progress. During the power-up RECALL cycle, the Reset command should not be issued and the host must wait for the R/$\overline{B}$ to become HIGH, which indicates that the power up Recall cycle is complete and the ONFI 1.0 nvSRAM is ready for access. Figure 16 defines the Reset behavior and timings. For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are “Don’t Care” bits when transmitting the Reset command.

If the Reset (FFh) command is issued when a nonvolatile operation is in progress, then the reset request is executed only after the ongoing nonvolatile operation is completed. Depending upon the present state of the device, the t_{RSTT} timing varies based on the following:

- If the Reset command is executed when the device is ready, it takes t_{SS} time to process the reset request.

- If the Reset command is issued when the software Recall cycle is in progress, it takes t_{RECALL} time to process the Reset request.
- If the reset command is issued when a Software or $\overline{HSB}$ Store cycle is in progress

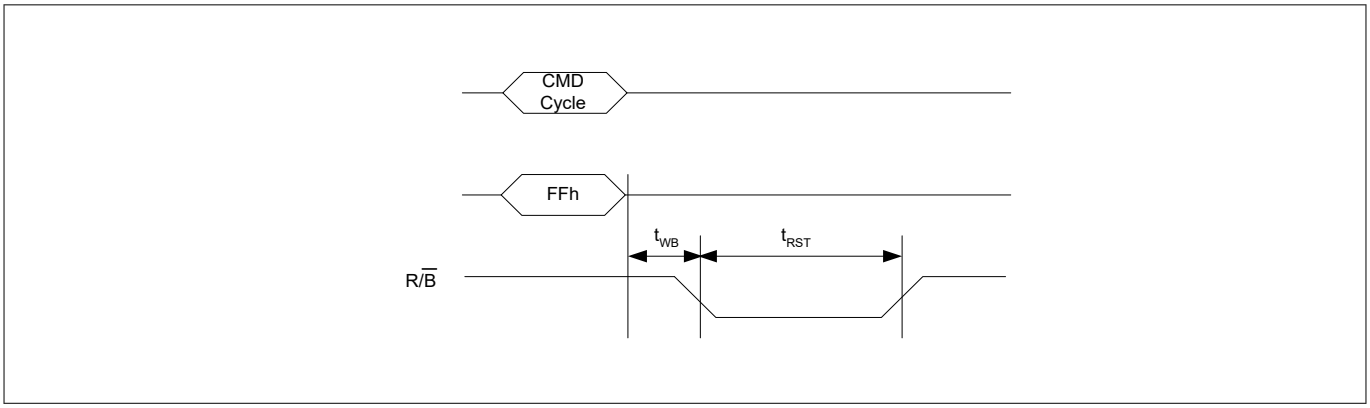


Figure 16 ONFI 1.0 nvSRAM Reset cycle

3.8.7.2 ONFI 1.0 NAND Flash

The ONFI 1.0 NAND flash Reset command is identical to the ONFI nvSRAM Reset command except that the ONFI 1.0 NAND flash aborts the command sequence in progress including the PROGRAM and ERASE commands. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed and is invalid.

3.8.8 Software store (84 h, A5h)

3.8.8.1 ONFI 1.0 nvSRAM

The Software Store command is specific to the ONFI 1.0 nvSRAM. This command is used to initiate the nonvolatile Store operation on demand. The nonvolatile Store operation saves the SRAM content into the nonvolatile memory and takes t_{STORE} time to complete the Software Store cycle.

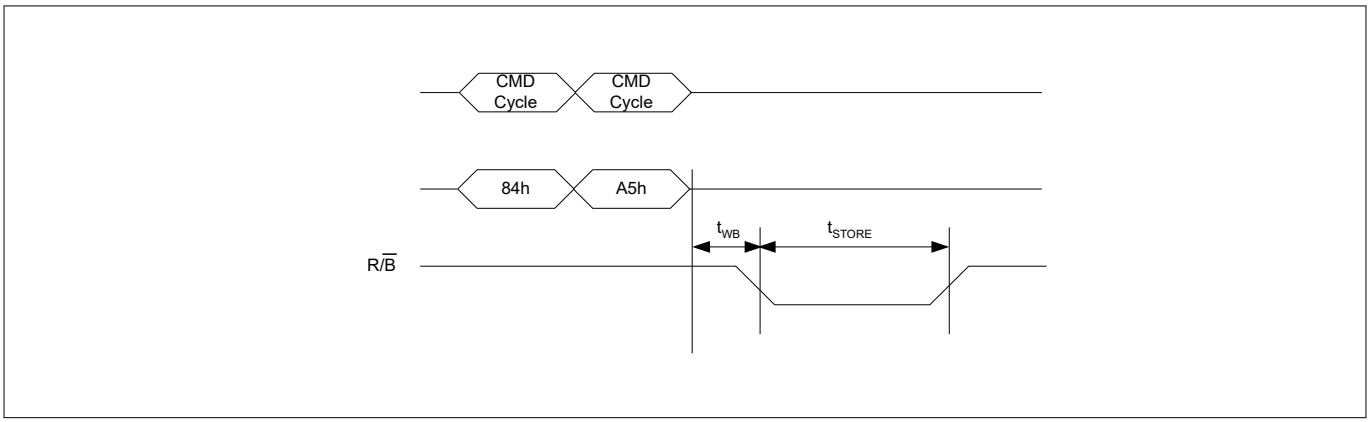


Figure 17 ONFI 1.0 nvSRAM Software Store cycle

3.8.8.2 ONFI 1.0 NAND Flash

This command is not applicable for the ONFI 1.0 NAND flash.

3.8.9 Software recall (FCh)

3.8.9.1 ONFI 1.0 nvSRAM

The Software Recall command is specific to the ONFI 1.0 nvSRAM. This command initiates a memory Recall operation and recalls the memory content from the nonvolatile memory to the SRAM. The ONFI 1.0 nvSRAM takes t_{RECALL} time to complete the Software Recall cycle.

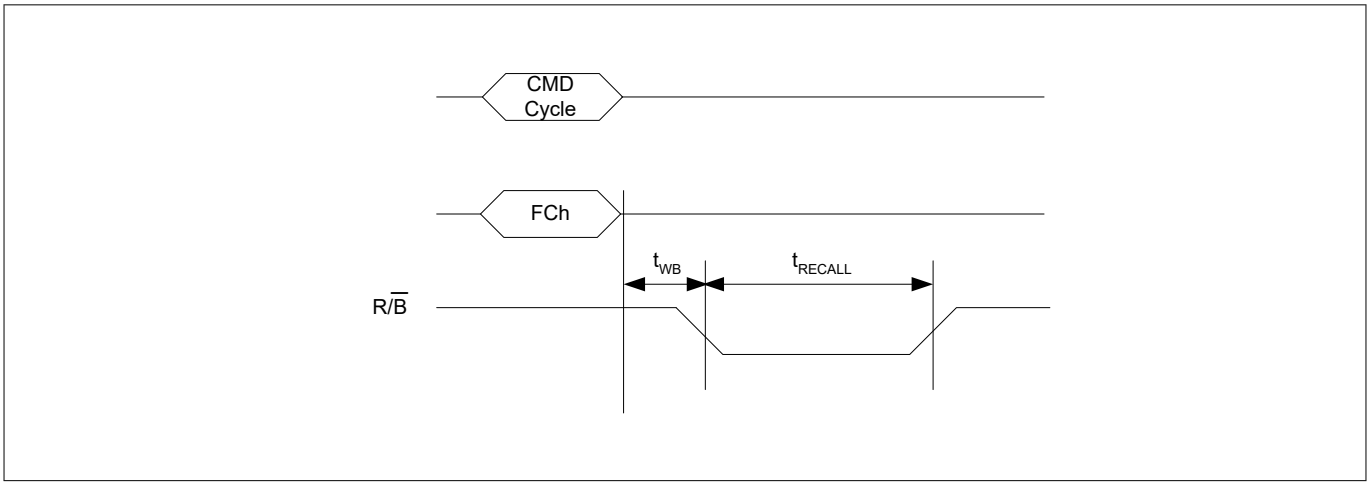


Figure 18 ONFI 1.0 nvSRAM Software Recall cycle

3.8.9.2 ONFI 1.0 NAND Flash

This command is not applicable for the ONFI 1.0 NAND lash.

3.8.10 AutoStore enable (A3h)

3.8.10.1 ONFI 1.0 nvSRAM

The AutoStore Enable command is specific to the ONFI 1.0 nvSRAM. This command is used to enable the AutoStore feature if it was disabled previously. All devices are shipped from factory with AutoStore enabled. The ONFI 1.0 nvSRAM takes t_{SS} time to process the AutoStore Enable command.

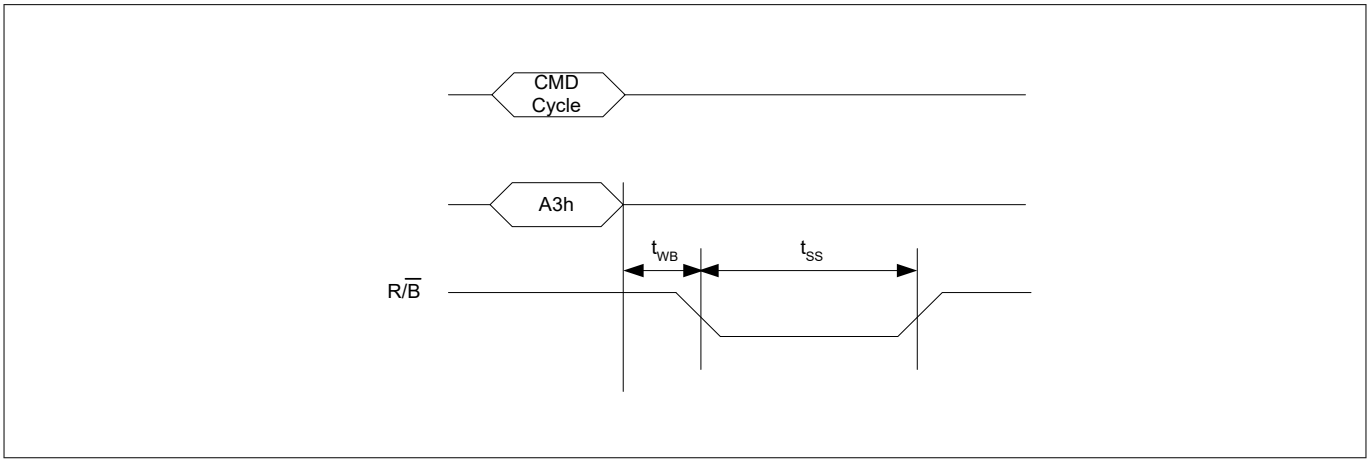


Figure 19 ONFI 1.0 nvSRAM AutoStore Enable cycle

3.8.10.2 ONFI 1.0 NAND Flash

This command is not applicable for the ONFI 1.0 NAND flash.

3.8.11 AutoStore disable (ACh)

3.8.11.1 ONFI 1.0 nvSRAM

The AutoStore Disable command is specific to the ONFI 1.0 nvSRAM and is used to disable the AutoStore feature. The nonvolatile Store (either $\overline{HSB}$ or software Store) should follow the AutoStore Disable command. Not executing the nonvolatile Store cycle following the AutoStore Disable command disables the AutoStore only for the current cycle; it does not survive for subsequent power cycles. The ONFI 1.0 nvSRAM takes t_{SS} time to process the AutoStore Disable command.

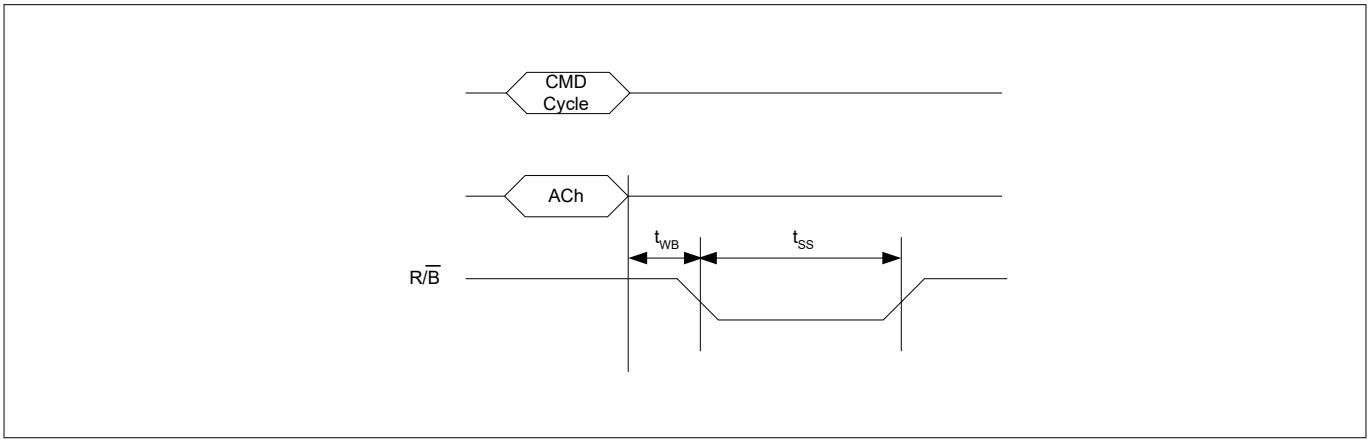


Figure 20 ONFI 1.0 nvSRAM AutoStore Disable cycle

3.8.11.2 ONFI 1.0 NAND Flash

This command is not applicable for the ONFI 1.0 NAND flash.

3.8.12 Reserved commands

3.8.12.1 ONFI 1.0 nvSRAM

The GetFeature (EEh) and SetFeature (EFh) commands are reserved for the ONFI 1.0 nvSRAM. These two commands are treated as valid commands and therefore do not set the FAIL flag bit in the status register unlike other invalid or not supported commands when they are executed.

3.8.12.2 ONFI 1.0 NAND Flash

The GetFeature (EEh) and SetFeature (EFh) commands are optional commands in the ONFI 1.0 standard.

4 ONFI 1.0 nvSRAM packages

The ONFI 1.0 nvSRAM is not package-compatible with ONFI 1.0 NAND flash devices. Table 5 lists the packages supported for ONFI 1.0 nvSRAM and NAND flash devices.

Table 5 ONFI 1.0 nvSRAM and NAND Flash packages

ONFI 1.0 nvSRAM	ONFI 1.0 NAND Flash
165-ball FBGA	48-TSOP 48-pin WSOP LGA-52 BGA-63

Refer to the ONFI 1.0 nvSRAM datasheet for the 165-ball FBGA package details.

5 Typical ONFI 1.0 nvSRAM interface in a system

This section provides an example circuit demonstrating the nvSRAM with a standard ONFI 1.0 host controller. Figure 21 shows a typical configuration of the ONFI 1.0 nvSRAM with the NAND host controller.

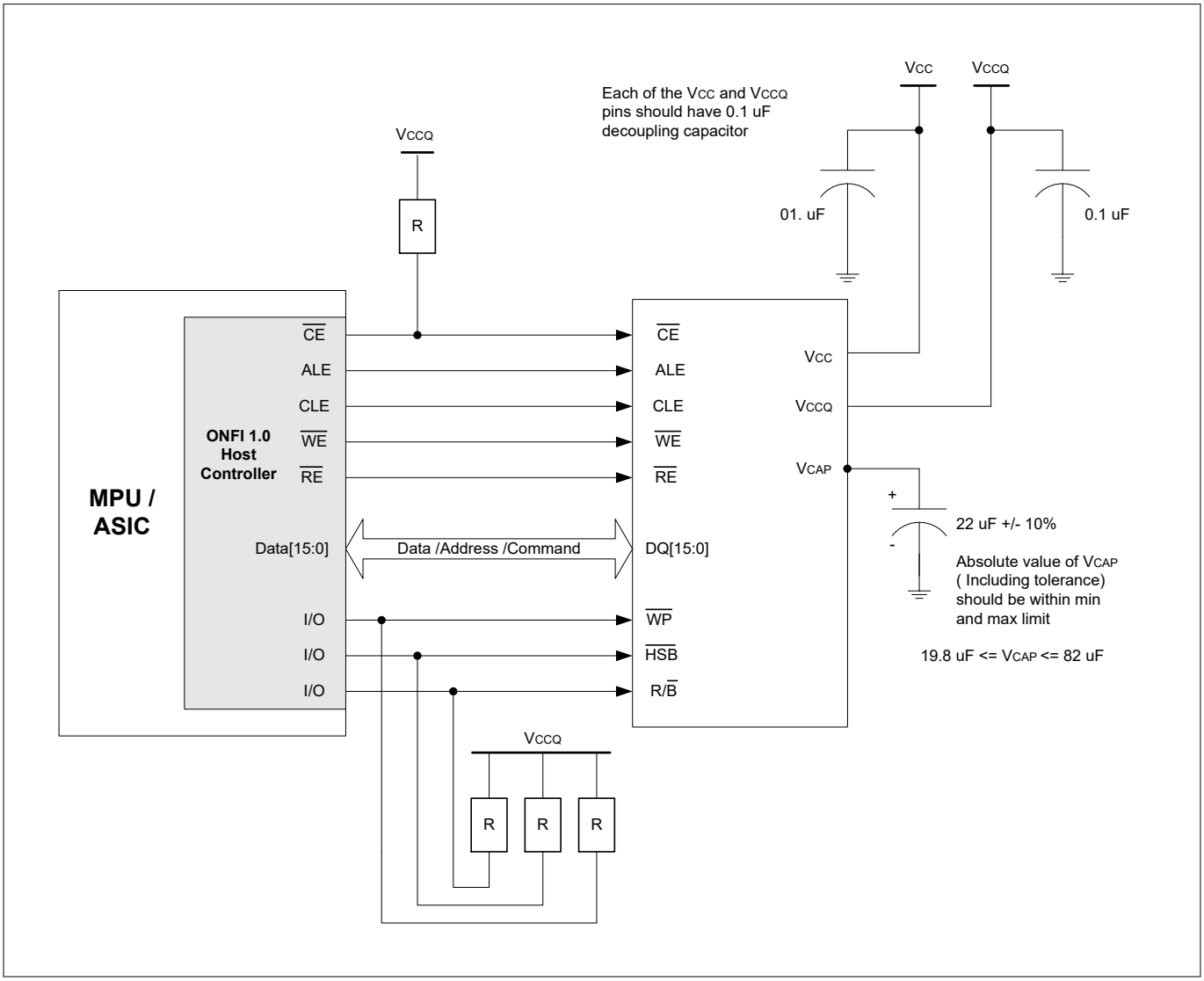


Figure 21 Typical ONFI 1.0 nvSRAM connection in a system

5.1 Design notes

1. The $\overline{WP}$ and $\overline{HSB}$ are active LOW input signals. If not used, these two control pins should be pulled to VCCQ using an external pull-up resistor of the value between 2.2 kΩ and 10 kΩ.
2. Each V_{CC} and V_{CCQ} pin should be connected to one 0.1 µF decoupling capacitor.
3. R/$\overline{B}$ is an active LOW, open-drain output driver and requires an external pull-up resistor to drive this pin to HIGH when the device is not busy. The R/$\overline{B}$ output can be tied to the other device R/$\overline{B}$ as a wired-OR logic. The value of the external pull-up resistor on R/$\overline{B}$ is determined based on multiple factors such as the sink current specification (I_{OL}), V_{OL} level, minimum rise time (t_R), and the total bus load on the pin.

6 Determining the pull-up value for R/$\overline{B}$

The combination of resistive pull-up (R_P) on the R/$\overline{B}$ and capacitive loading (C_B) of the R/$\overline{B}$ circuit determines the maximum rise time of the R/$\overline{B}$ signal. The actual value used for R_P depends on the system timing requirements. Large values of R_P cause the rise time to be delayed significantly. The rise time is approximately two time-constants (t_C) between the 10% and 90% points.

$$\text{Onetime} - \text{contact}\,(t_c) \;=\; R \times C \tag{1}$$

Where R = R_P (resistance of pull-up resistor), and C = C_B (total capacitive load).

$$\text{Rise time}\,(\max) \;= 2 \times (R_P \times C_B) \tag{2}$$

$$\text{Therefore,}\;\; \text{the}\;\; \max \text{value of}\; R_P = \frac{\text{Rise time}\;\;(\max)}{(2 \times C_B)} \tag{3}$$

The fall time of the R/$\overline{B}$ signal is determined mainly by the output impedance of the R/$\overline{B}$ signal and the total load capacitance C_B. The minimum value for Rp is determined by the output drive capability of the R/$\overline{B}$ signal (V_{OL}, I_{OL}) and the output voltage swing VCC (max).

$$R_p = \frac{V_{CC}(MAX) - V_{OL}(MAX)}{(I_{OL} + \Sigma_{IL})} \tag{4}$$

Where ΣI_L is the sum of the input leakage currents of all devices' R/$\overline{B}$ pins tied together.

7 Summary

The ONFI 1.0 nvSRAM follows the majority of access opcodes and timings specifications of the ONFI 1.0 standard. This allows interfacing Infineon's ONFI 1.0 nvSRAM to the ONFI 1.0 bus and sharing it with other ONFI 1.0 NAND flash memories. AN91206 provides a detailed description on ONFI 1.0 nvSRAM access opcodes, protocols, and cycle timings. This application note also highlights key differences between Infineon's ONFI 1.0 nvSRAM and the ONFI 1.0 NAND flash memory.

Users can refer to this application note to develop the design schematic and firmware code for ONFI 1.0 nvSRAM interfaces in a target system. A reference block diagram, design notes, and design schematic will help in designing with ONFI 1.0 nvSRAM quickly. Refer to the ONFI 1.0 nvSRAM datasheet for details on timing diagrams and AC parameters.

Revision history

Document revision	Date	Description of changes
**	2014-09-18	Initial release.
*A	2017-08-24	Updated to new template. Completing Sunset Review.
*B	2026-09-04	Template update. Updated the link for Nonvolatile SRAM (nvSRAM) Basics in Introduction.

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