Migrating from CY14B101P/CY14B512P/CY14B256P to CY14B101PA/CY14B512PA/CY14B256PA

About this document

Scope and purpose

AN72389 provides details for migrating from the CY14B101P/CY14B512P/CY14B256P nvSRAM parts to CY14B101PA/CY14B512PA/CY14B256PA parts in applications. This application note also lists the parameter differences between the parts and the design considerations for migration when converting applications to CY14B101PA/CY14B512PA/CY14B256PA.

Associated part family

Serial (SPI) nvSRAM

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1 Introduction

Infineon CY14B101PA is a 3 V, 1 Mbit (128K x 8) serial (SPI) nvSRAM with RTC in 0.13 micron technology. This part is functionally equivalent to the CY14B101P in the same technology with a few parameter enhancements and additional features. Due to these enhancements, there are a few differences in parameters. This application note highlights the differences between the CY14B101P and the CY14B101PA, and lists the parameters of significance that must be considered while migrating. These differences and considerations are applicable to CY14B512PA (3 V,

64K x 8, 512-Kbit) and CY14B256PA (3 V, 32K x 8, 256-Kbit) serial (SPI) nvSRAMs with RTC which are the replacement parts for CY14B512P and CY14B256P devices, respectively. This application note is described with respect to CY14B101P and CY14B101PA in the following sections. The same description applies to CY14B512P/ CY14B256P and CY14B512QPA/CY14B256PA.

2 Overview

The following tables compare the features and parameters of the two parts.

Table 1 Part number description

Description	Original Part number	Replacement Part number	Configuration
128 K x 8	CY14B101P	CY14B101PA	With AutoStore, Write Protect, Hardware STORE, RTC

3 Operating temperature range

The CY14B101P and CY14B101PA are offered in the industrial temperature range.

3.1 Feature Set

Both the parts share the same overall feature set. There are a few additional features in the new device. These are listed in Table 2.

Table 2 Feature Set Comparison

Feature Set	**CY14B101P**	**CY14B101PA**
SPI clock speed, SRAM access	40 MHz	40 MHz, 104 MHz
SPI clock speed, RTC access	25 MHz	25 MHz
AutoStore	Identical	
Hardware STORE	Identical	
Read/write instructions	Identical	
Special NV Instructions		
Software STORE	Identical	
Software RECALL		
AutoStore Enable/Disable		
Special instructions		
SPI Fast read	Not Available	104 MHz
SLEEP	Not Available	Available
Serial Number		
Device ID		
RTC		
Calibration	Identical	
Watchdog timer		
Alarm		
Capacitor or battery backup	Available	Available
RTC Backup time with 1 Farad	**30 days**	**25 days**
Backup power fail flag	Not Available	Available
Square wave output	Not Available	Available

4 Packages

CY14B101PA is pin compatible with CY14B101P and is available in the same 16-pin SOIC package.

5 Parameters

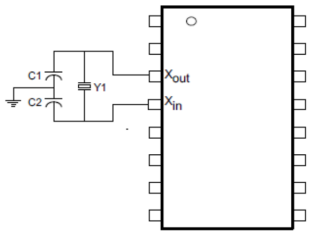
The CY14B101PA is a drop in replacement for CY14B101P and requires only minimal changes in the application board. However, the differences in parameters should be considered before replacing one part with the other. Table 3 lists the differences in parameters between CY14B101P and CY14B101PA.

Table 3 Parameter comparison

Parameter	Description	CY14B101P		CY14B101PA		Unit
		Min.	Max.	Min.	Max.	
DC Parameters						
I_{CC1}	Average V_{CC} current, f_{SCK} = 40 MHz	-	10	-	3	mA
	Average V_{CC} current, f_{SCK} = 104 MHz	104 MHz clock speed not available		-	10	mA
I_{CC2}	Average V_{CC} current during STORE	-	10	-	3	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	-	5	-	3	mA
I_{SB}	Average V_{CC} current	-	5	-	0.25	mA
I_{ZZ}	Sleep mode current	Feature not available		-	8	µA
V_{CAP}	Storage capacitor	61	180	42	180	µF
AC Switching Parameters						
All AC parameters are identical and additionally the CY14B101PA has 104 MHz specs						
Software Controlled Operations Parameters						
t_{RECALL}	RECALL duration	-	**200**	-	**600**	µs
t_{SS}	Soft sequence processing time	-	**100**	-	**500**	µs
RTC						
I_{BAK}	RTC backup current	-	**0.5**	-	**0.6**	µA

(table continues...)

Table 3 (continued) Parameter comparison

Parameter	Description	CY14B101P		CY14B101PA		Unit
		Min.	Max.	Min.	Max.	
DC Parameters						
t_{RTCp}	RTC processing time from end of 'W' bit set to '0'	-	**350**	-	**1,000**	µs
Figure 1. RTC recommended Component Configuration 		Y1 = 32.768 KHz (12.5 pF) **C1 = 10 pF** C2 = 68 pF		Y1 = 32.768 KHz (12.5 pF) **C1 = 12 pF** C2 = 68 pF		

5.1 Instruction set

The CY14B101PA has the same SPI instruction set as the CY14B101P for all functions. Hence, users do not need to make any changes to the opcodes. The CY14B101PA has additional features such as Fast Read, SLEEP, Serial Number, and Device ID, which are not available in the old part. Users interested in using these features can see datasheet for additional detail.

5.2 Status register bit definition

Bits 4, 5, and 6 in Status Register are Don't Care bits in CY14B101P while in CY14B101PA, bit 6 is the Serial Number Lock bit and Bits 4 and 5 are Don't Care bits. The differences in these bits is shown in Table 4.

Table 4 Status register bit definition

Bit	CY14B101P	CY14B101PA
Bit 0 (RDY)	Ready	
Bit 1 (WEN)	Write Enable	
Bit 2 (BP0)	Block protect bit '0'	
Bit 3 (BP1)	Block protect bit '1'	
Bit 4, Bit 5	Don't Care, Factory default is "0" These bits are writable. On power-up, these bits are written with "0"	Don't Care, Factory default is "0" These bits are non-writable. These bits always return "0" upon read

(table continues...)

Table 4 (continued) Status register bit definition

Bit	CY14B101P	CY14B101PA
Bit 6	**Don't Care** Bits are writable. On power-up, bits are written with "0"	**Serial Number Lock**, Factory default is "0" Set to "1" by user for locking serial number. When written with "1" and STORED, the bit will stay at "1" through power cycles and cannot be written with "0" subsequently
Bit 7 (WPEN)	Write protect enable bit	

6 Critical considerations

The impact of the differences in CY14B101PA with respect to the CY14B101P in existing applications is discussed below. Board designers are recommended to review the detailed datasheets when migrating to the new part.

6.1 DC and AC parameter differences

All the DC and AC parameters are the same or better in the CY14B101PA parts and hence these parts can directly replace the CY14B101P parts. Existing applications can directly benefit from the low power consumption in the CY14B101PA parts, such as 3 mA I_{CC1} and 250 µA I_{SB} compared to 10 mA I_{CC1} and 5 mA I_{SB} in the CY14B101P part. The CY14B101PA parts also have additional features such as 104 MHz operation and SLEEP mode which can be used by making suitable changes in the controller firmware.

6.2 Software controlled NV operation parameters

Due to the low power design, the processing time for the special NV operations (t_{RECALL} and t_{SS}) are higher in the CY14B101PA parts. These parameters could affect applications which use the special NV instructions for Software RECALL and AutoStore Enable/Disable. When these instructions are executed, the CY14B101PA parts take 400 µs longer to complete the execution and hence users should allow an additional controller wait time before accessing the nvSRAM again. This is shown in Table 5.

Table 5 NV operation timing comparison

Instruction category	Instruction name	Opcode	Duration	
			CY14B101P	CY14B101PA
Special NV Instructions				
Software STORE	STORE	0x3C	8 ms in both parts	
Software RECALL	RECALL	0x60	**200 µs**	**600 µs**
AutoStore Enable	ASENB	0x59	**100 µs**	**500 µs**
AutoStore Disable	ASDISB	0x19	**100 µs**	**500 µs**

6.3 Status register bits 4, 5, 6 (Don't care bits)

In the CY14B101P part, the Don’t Care bits 4-6 are writable and return “0” on power up. In the CY14B101PA part, only the Bit 6 is writable (being SNL bit) and will return “1” once written with “1”. This difference would not affect any application where the Don’t Care bits are left at “0”. If any application is writing into these bits, then the difference in these bits needs to be considered.

6.4 RTC

RTC performance with the CY14B101PA part is optimum with the recommended capacitors (C1 = 12 pF, C2 = 68 pF, 12.5 pF crystal).

The CY14B101PA parts have a Backup power fail detect feature because of which the back up current is higher than in the CY14B101P part. This higher I_{BAK} current in the CY14B101PA part means the backup capacitor is required to be higher (by 20%) to get the same back up time as in the CY14B101P part.

Also, the CY14B101PA part has higher RTC processing time because of its low power design and hence any application where a STORE is performed after an RTC register update requires a longer wait time of 1,000 µs compared to the 350 µs in the CY14B101P part for the updated data in the RTC registers to be saved.

6.5 PCB layout considerations

The CY14B101PA is available in the same 16-SOIC package as the CY14B101P and hence migrating from CY14B101P requires no change in the PCB forrprint. See the Infineon application notes, AN61546 – Non-Volatile Static Random Access Memory (nvSRAM) Real Time Clock (RTC) Design Guidelines and Best Practices, for detailed information on RTC layout considerations applicable to all low power RTC oscillators.

7 Details of improvement

This section describes the enhancement in $\overline{\text{HOLD}}$ operation in the CY14B101PA parts.

7.1 $\overline{\text{HOLD}}$ Function

The CY14B101P part required $\overline{\text{CS}}$ to remain LOW along with $\overline{\text{HOLD}}$ pin to pause communication. See Figure 1. In the CY14B101PA part, $\overline{\text{CS}}$ can toggle after $\overline{\text{HOLD}}$ is asserted and serial communication is paused by holding $\overline{\text{HOLD}}$ pin alone LOW. See Figure 2.

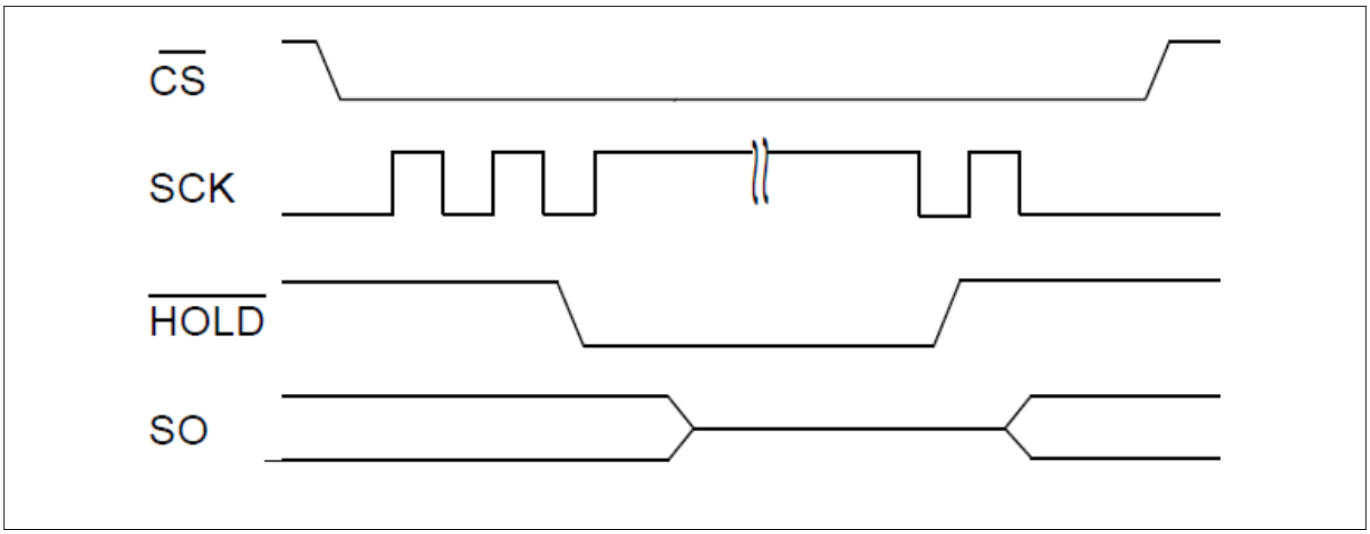


Figure 1 $\overline{\text{HOLD}}$ Operation in CY14B101P

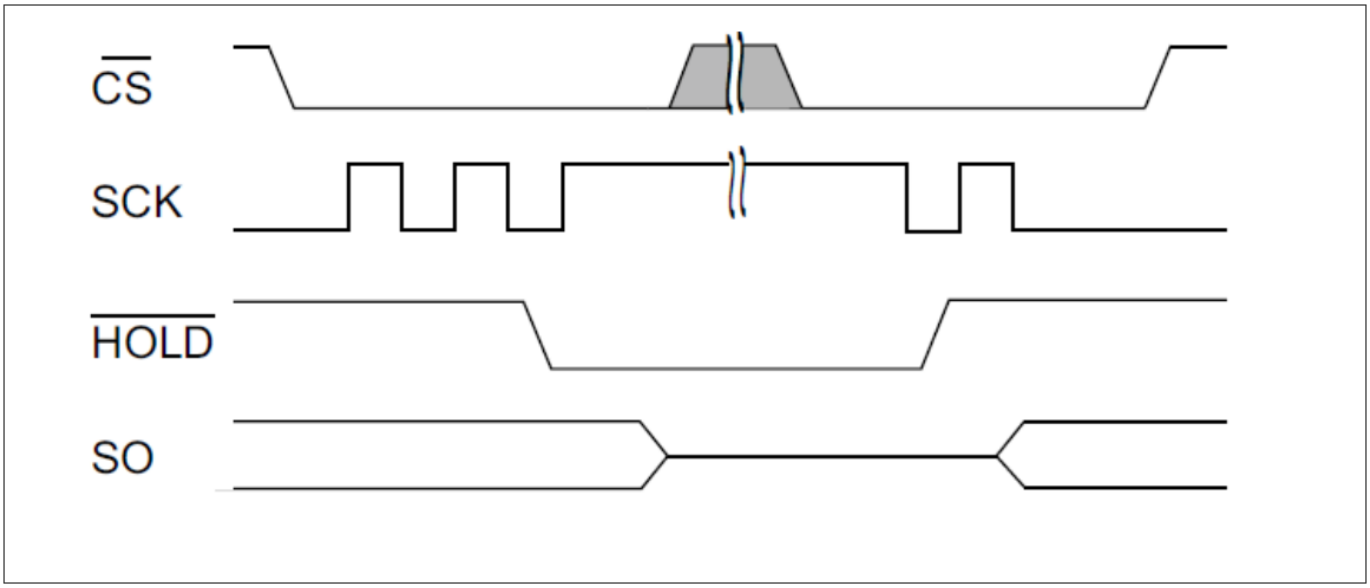


Figure 2 $\overline{\text{HOLD}}$ Operation in CY14B101PA

8 Summary

This application note discusses the differences between CY14B101PA, the new version SPI nvSRAM with RTC, and the older CY14B101P. CY14B101PA is pin compatible with and can replace the CY14B101P device with minimum changes in most applications. This application note is also applicable for CY14B512PA replacing CY14B512P and CY14B256PA replacing CY14B256P.

Revision history

Document version	Date of release	Description of changes
**	2011-11-25	New Spec.
*A	2012-06-05	Replaced “Converting” with “Migrating” in Document Title. Updated Abstract (Reworded for better understanding). Updated text for more clarity. No change in technical content. Updated to new template.
*B	2014-09-12	No change in technical content. Updated to new template. Completing Sunset Review.
*C	2017-08-17	Updated logo and copyright.
*D	2026-09-04	Template update; no content update

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