72-Mbit RHQDRII+ power modes

About this document

Scope and purpose

High speed source synchronous semiconductor devices rely on clock synthesis circuits (DLL - Delay Lock Loop/PLL - Phase Lock Loop) to mitigate on die clock skews. The 72-Mbit RHQDRII+ SRAM uses a DLL to ensure output data and echo clocks (Strobe) are edge aligned and de-skewed with respect to the source clock. However, all DLLs/PLLs require a certain number of clock cycles to attain “lock” during which the device will not reliably operate. This application note discusses the required steps necessary to effectively transition between maximum performance and power saving modes with proper DLL operation.

Associated part family

CYRS1542AV18, CYRS1543AV18, CYRS1544AV18, CYRS1545AV18

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1 Introduction

Infineon's Radiation Hardened 72-Mbit QDR™ II+ SRAM is a source synchronous pipelined Static RAM equipped with the 1.8-V QDR™ II+ architecture with RadStop technology. The QDR™ II+ architecture has separate data inputs and data outputs. To maximize data throughput, both read and write ports are equipped with DDR interfaces, which transfer data on both rising and falling edges of the clock signal.

Source synchronous interfaces remove the time-of-flight limit on interconnection between ICs and require no controlled clock skew. Another advantage of source synchronous interfaces is dramatically increased I/O frequencies. Because of the increased I/O frequencies, controlling data bit-to-bit timing skews and "eye patterns" are critical for proper interface operation. 72-Mbit RHQDRII+ SRAM's DLL effectively de-skews the internal clock network providing edge aligned data output signals.

72-Mbit RHQDRII+ SRAM is a high performance memory and supports two power modes, namely, maximum performance (MP) and power save (PS). The DLL has to be locked in the MP mode. Hence, proper DLL locking clock cycles have to be observed when switching between MP and PS modes. The following table lists the two power modes along with their supported operations.

Table 1 Power modes

Power mode	Device operations
Maximum Performance (MP)	Read, Write
Power Save (PS)	NOP, Standby

DLL basics shows the functional block diagram of the 72-Mbit QDR™ II+ SRAM physical input/output interface.

2 DLL basics

Infineon has designed a DLL in 72-Mbit RHQDRII+ SRAM to remove clock distribution delay associated with the clock network as shown in Figure 1.

2 DLL basics

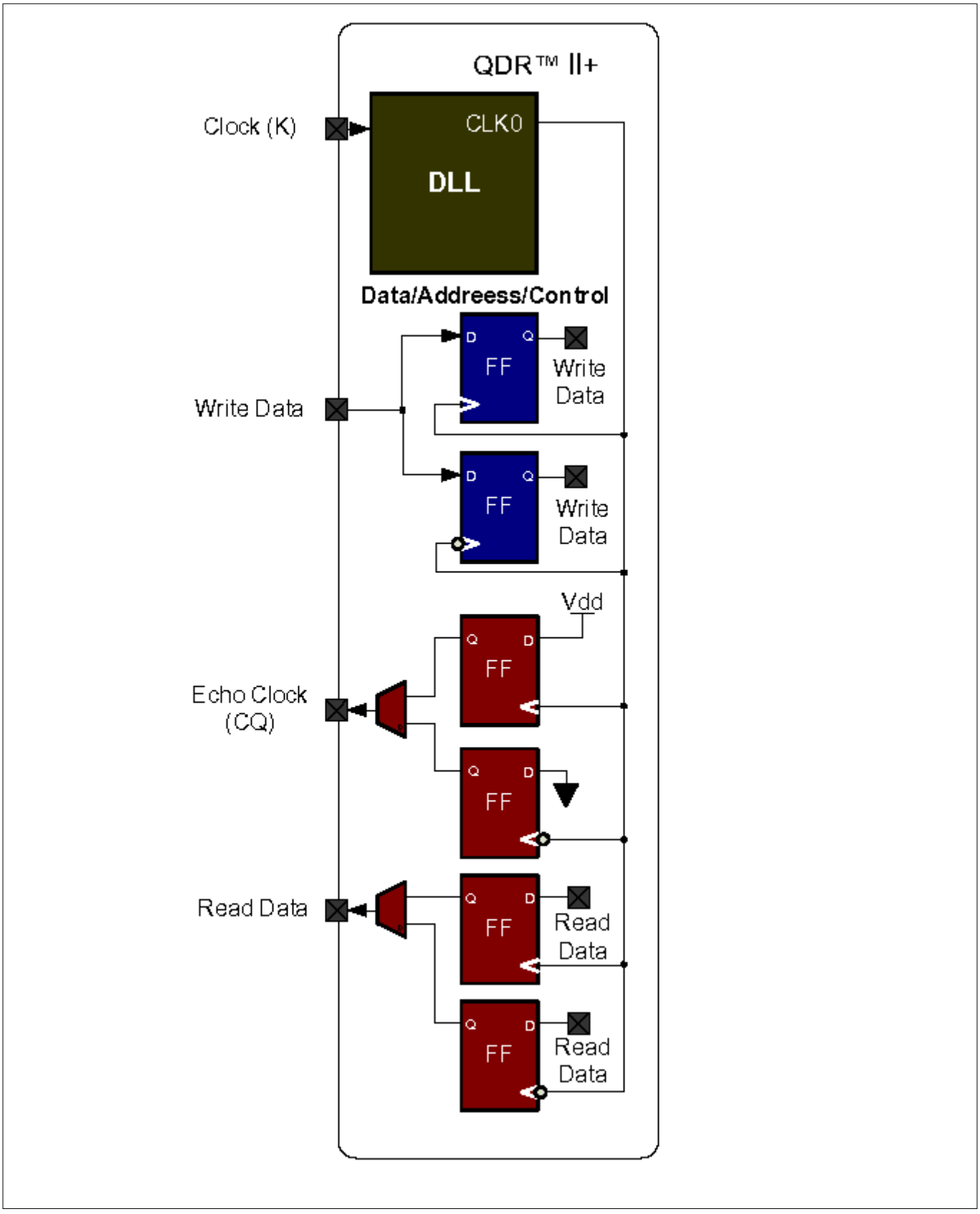

Figure 1 QDR™ II+ functional architecture

A DLL in its simplest form consists of variable delay line and control logic. Figure 2 shows a DLL functional block diagram. A DLL works by inserting delay between the input clock (REFCLK) and the feedback clock (FBCLK) until

2 DLL basics

the two rising edges align. After the edges line up, the DLL "locks." As long as the device is operated after the DLL locks, the two clocks have no discernible difference. Thus, the DLL output clock compensates for the delay in the clock distribution network, effectively removing the delay between the source clock and its loads.

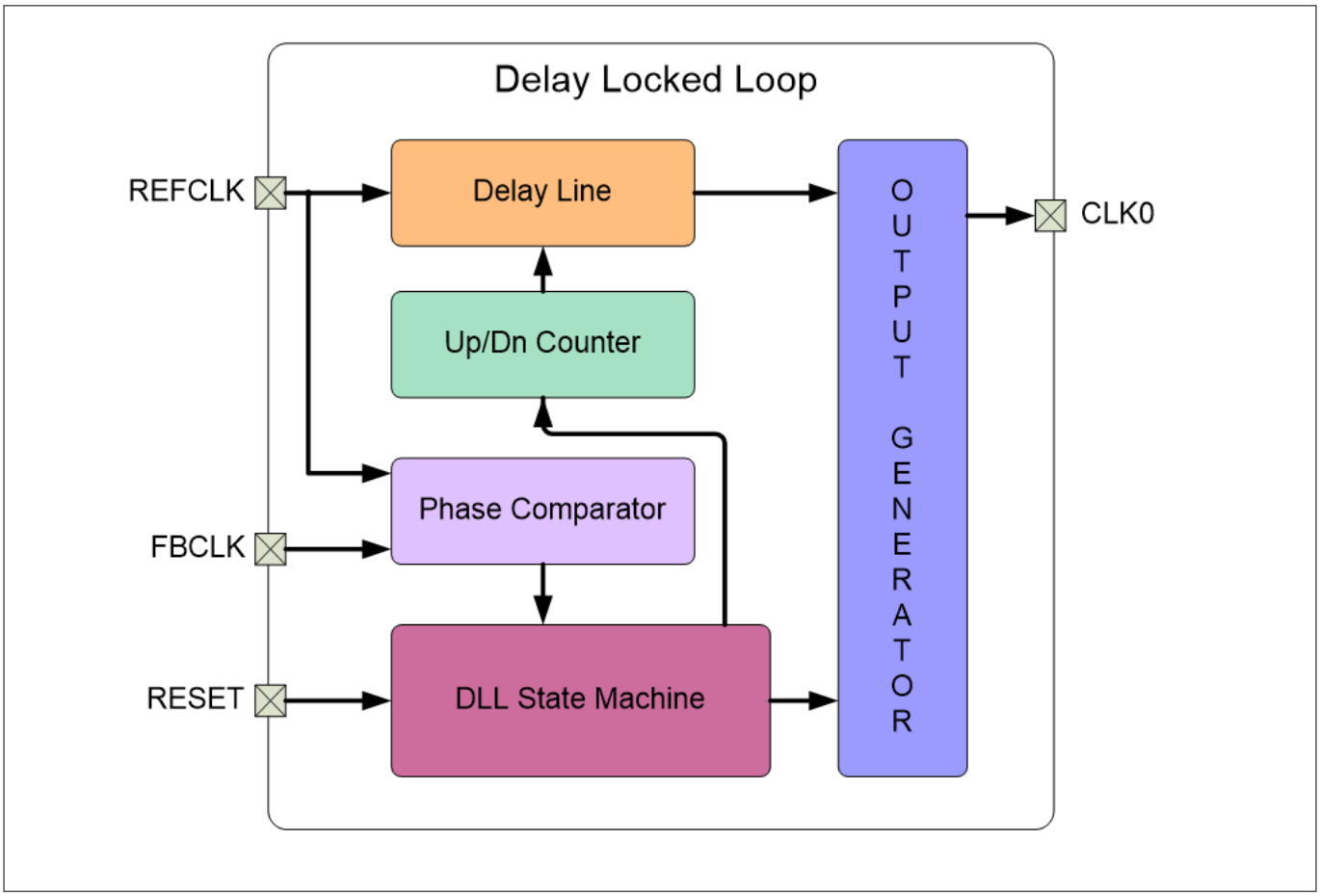

Figure 2 DLL functional architecture

To achieve lock, the DLL needs to sample several thousand stable clock cycles. The DLL timing parameter section of the CYRS154*AV18 data sheets provide the locking times (10,240 cycles). The system should not access data from 72-Mbit RHQDRII+ SRAM till the DLL lock is complete. Otherwise, the echo clocks (CQ, CQb) and read data are not valid and can exhibit glitches, spikes, or other spurious behavior.

3 Read timing

To fully appreciate the effects of DLL in 72-Mbit QDRII+ SRAM, Figure 3 shows typical read cycle timing. As can be seen, the echo clocks (CQ and CQb), which are the read strobe signals, are edge aligned with the read data (Q).

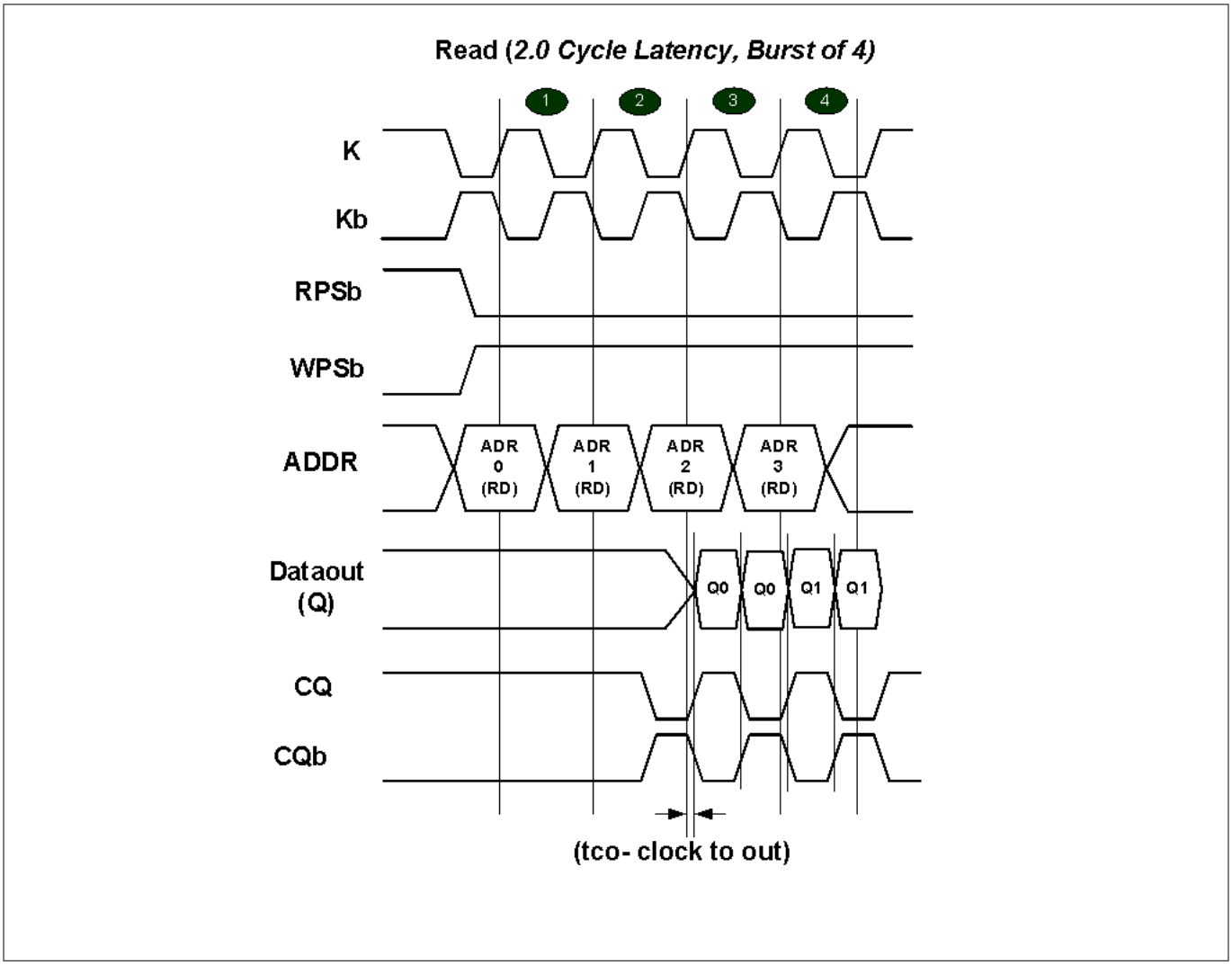

Figure 3 Read waveforms

4 Operational states

Table 2 lists all the different operations supported in
72-Mbit RHQDRII+ SRAM along with their respective current consumption.

Table 2 Table of operational modes

State	K(Clock)	RPSb	WPSb	Max. Current
Read (MP)	L→ H	L	X	1.65A
Write (MP)	L→ H	X	L	1.65A
NOP (PS)	L→ H	H	H	0.4A
Standby (PS)	Stopped	X	X	0.04A

4.1 Read

Read operations are initiated by asserting RPSb at the rising edge of the positive input clock (K). The address is also latched on the rising edge of the K clock. Following the correct clock latency, data is driven onto the Q bus. DLL should be locked when 72-Mbit RHQDRII+ SRAM is in the read mode so that echo clocks (CQ, CQb) can be used as strobe signals.

***Note**: Please refer to CYRS154*AV18 data sheets for signal details.*

4.2 Write

Write operations are initiated by asserting WPSb at the rising edge of the positive input clock (K) for burst of 4 or rising edge of negative input clock (Kb) for burst of 2. On the correct clock (K, Kb) edges, the data presented to D bus is latched in. After the address is decoded, the latched data (presented on the D bus) is stored in memory. DLL should be locked when 72-Mbit RHQDRII+ SRAM is in the write mode.

***Note**: Please refer to CYRS154*AV18 data sheets for signal details.*

4.3 No Operation (NOP)

NOP is initiated when both RPSb and WPSb are asserted HIGH on the rising edge of the positive input clock (K). DLL is not locked when 72-Mbit RHQDRII+ SRAM is in the NOP mode.

4.4 Standby

Standby is initiated when the input clocks (K, Kb) are stopped and DOFFb is deactivated (DLL Off signal). DLL is not locked when 72-Mbit RHQDRII+ SRAM is in the standby mode.

5 Power mode transitions

Having the DLL locked is critical for proper read and write operations. However, as mentioned above, NOP and standby states bring the DLL out of its locked state. Thus, to resume operations after NOP or standby, a wait period is required for the DLL to attain lock (10,240 cycles).

5.1 Standby/NOP to Read/Write

Read and write operations require DLL to be locked. Figure 4 shows the correct transition from standby/NOP to read/write for burst of 2. As mentioned, a wait period of 10,240 cycles is required.

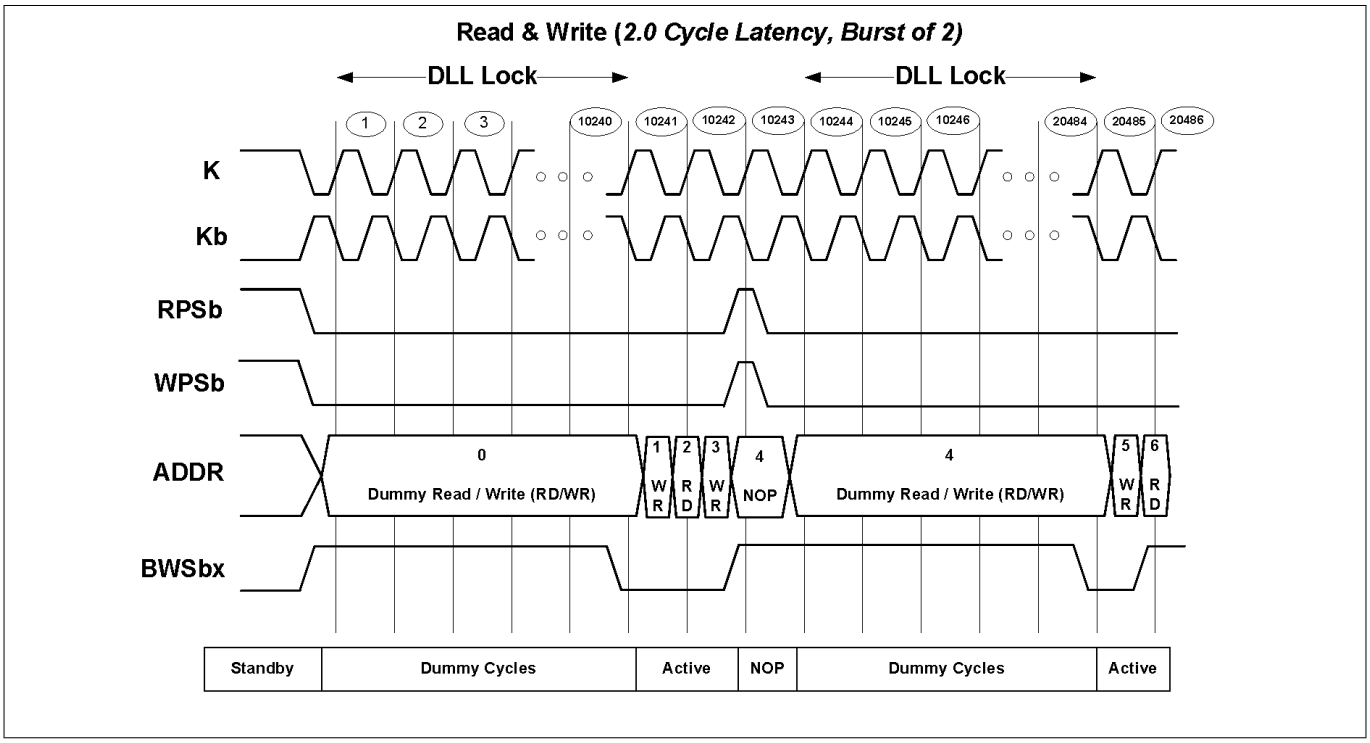

Figure 4 Standby to Read/Write – Burst of 2

Figure 5 shows the correct transition from standby/NOP to read/write for burst of 4.

5 Power mode transitions

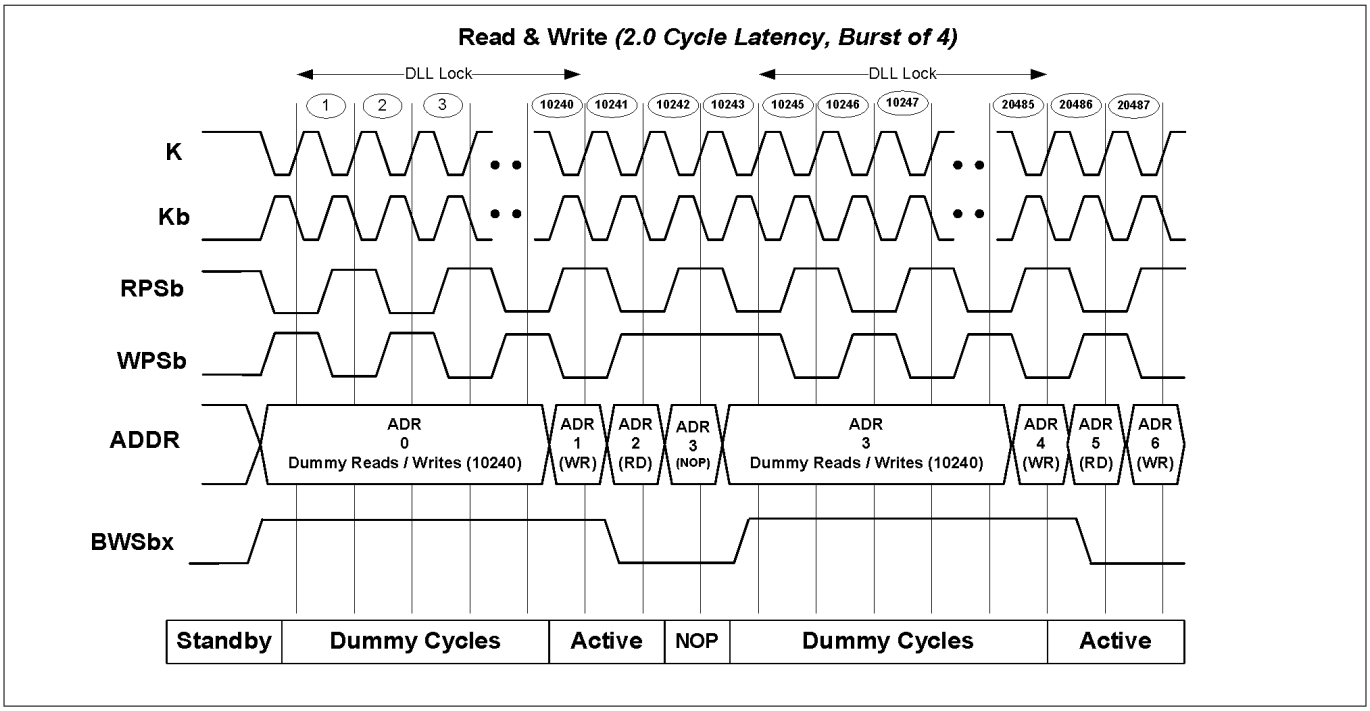

Figure 5 Standby to Read/Write – Burst of 4

6 System design consideration

NOP and standby states are principally designed in to significantly reduce device power consumption proper 72-Mbit RHQDRII+ SRAM read and write operations require a “locked” DLL and can take 10,240 clock cycles to achieve lock from power save mode. In order to maintain DLL lock, Infineon recommends the following for optimum 72-Mbit RHQDRII+ SRAM performance:

6.1 Maximum performance

In order to maintain DLL lock and avoid waiting, clock cycles that do not access data from the 72-Mbit RHQDRII+ SRAM memory core should contain dummy read/write cycles. This in shown in Figure 6 and Figure 7 for bursts of 2 and 4 respectively. Keep in mind that reads from the same address will not adversely affect the SRAM cells.

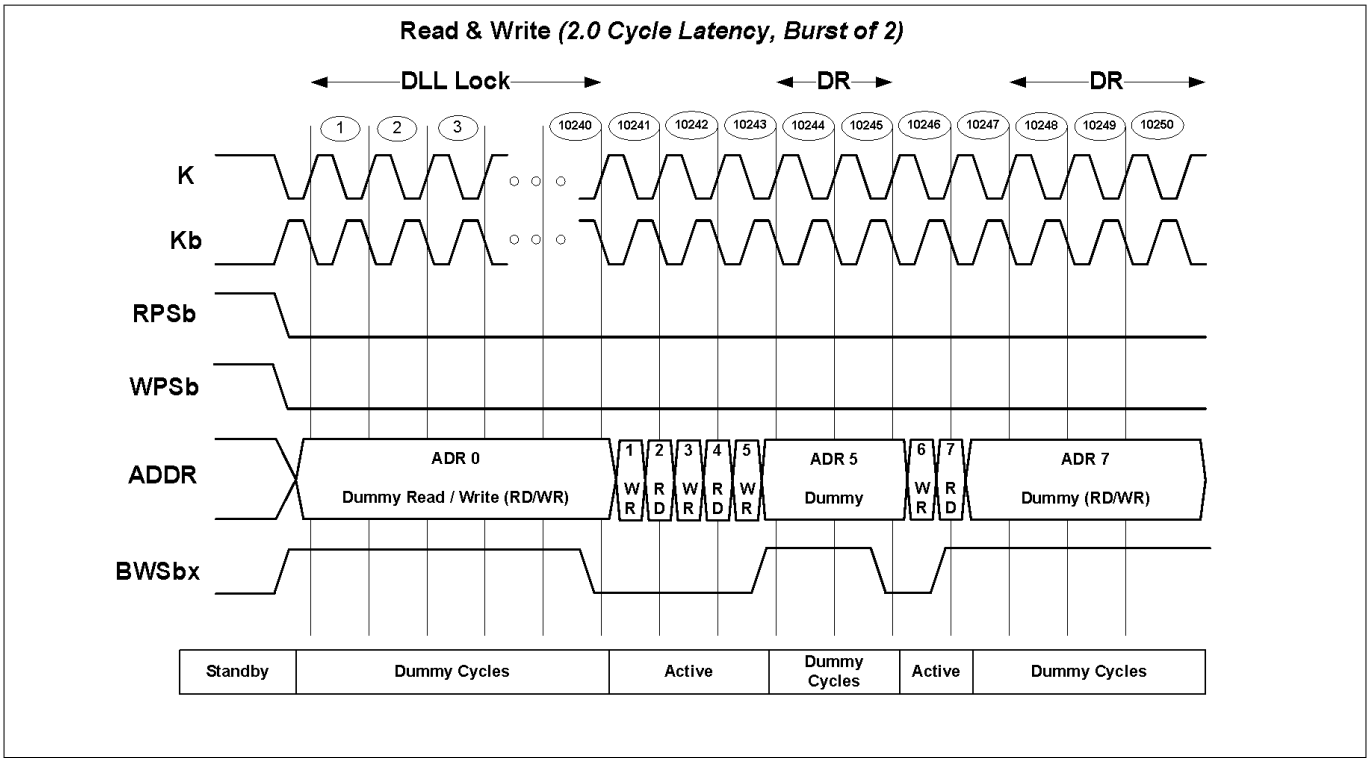

Figure 6 Maximum performance – Burst of 2

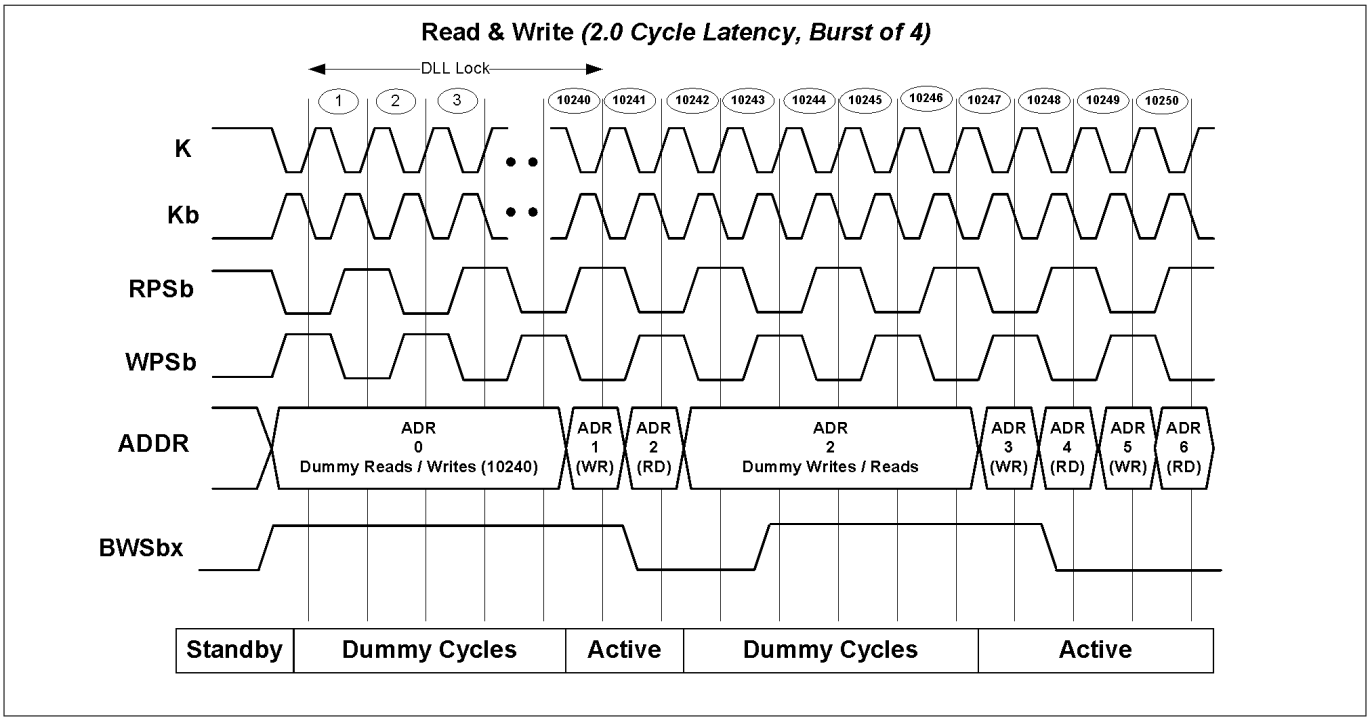

Figure 7 Maximum performance – Burst of 4

6.2 Power save

NOP and standby modes have significant power saving and can improve the overall system power performance if required. DLL is not locked in these modes and transiting out requires DLL lock before performing any memory access operations.

6.3 Data width expansion

If data width expansion is needed and multiple 72-Mbit RHQDRII+ are used in series, all operations are similar to a single device 72-Mbit RHQDRII+ operation.

6.4 Depth expansion

For depth expansion where multiple 72-Mbit RHQDRII+ are used in parallel, a multiplexer at the data output (Q) pins is required for maximum performance mode. The reason behind this is in maximum performance mode, the outputs from the two 72-Mbit RHQDRII+ devices will not tri-state since dummy read cycles are inserted.

7 Summary

PLLs and DLLs are essential to eliminating internal device clock delays. Infineon’s 72-Mbit RHQDRII+ has a DLL which requires lock for proper memory operations. NOP and standby modes bring the DLL out of lock state to save power. Resuming Read afterwards requires the DLL to achieve lock, meaning waiting for 10,240 clock cycles. For high performance system applications, dummy read/write cycles should be inserted during device idle clock cycles to maintain DLL in lock and avoid any wait states.

Revision history

Document version	Date of release	Description of changes
**	2011-05-24	New Application Note.
*A	2012-09-20	Added actual part numbers.
*B	2014-06-06	Updated to new template. Completing Sunset Review.
*C	2017-07-28	Updated to new template. Completing Sunset Review.
*D	2026-09-03	Template update; no content update.

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