Enabling Infineon HYPERFLASH™ with NXP S32G

About this document

Scope and purpose

This application note describes how to enable Infineon HYPERFLASH™ serial NOR flash memories with S32G Vehicle Network Processors from NXP, by showing working examples of hardware connection, boot configuration, programming, and flash driver integration for real-time applications.

Intended audience

This document is intended for hardware and software designers who plan to integrate Infineon S26KL-S/S26KS-S HYPERFLASH™ or S26HL-T/S26HS-T SEMPER™ NOR flash memories with NXP S32G family of devices. Readers are expected to have access to NXP documents as well as usage experience of NXP design tools.

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1 Introduction

1.1 Infineon HYPERFLASH™ NOR flash

Infineon S26KL-S/S26KS-S HYPERFLASH™ family is serial NOR flash memories with HYPERBUS™ interface that deliver the performance required for embedded systems in automotive applications. The key features of HYPERFLASH™ are:

- x8 interface operating up to 166 MHz DDR (333 MBps)
- 12-pin interface compatible with Octal SPI memories from various vendors
- Automotive qualified to AEC-Q100 Grade 1 (40°C to +125°C)
- 128 Mb to 512 Mb densities

Additionally, Infineon S26HL-T/S26HS-T SEMPER™ NOR flash with HYPERBUS™ family is a superset of S26KL-S/S26KS-S HYPERFLASH™ and has additional features as follows:

- Up to 200 MHz DDR (400 MBps)
- ASIL-D certified
- 256 Mb to 2 Gb densities

For basics of the HYPERBUS™ interface, such as signal descriptions and protocol, see HYPERBUS™ Specification.

1.2 External flash memory interface in NXP S32G

NXP S32G family of devices is a high-performance vehicle network processor, combining CAN/LIN/FlexRay networking with high data rate Ethernet, which targets automotive applications, such as central gateway, domain controllers, ADAS, and FOTA masters.

S32G does not have internal, on-chip flash memory where the processors can boot from. Therefore, external non-volatile memory is essential. S32G has an SDHC that can interface eMMC, SD card, and SDIO. It also has a QuadSPI controller to interface external flash memory. The key features of the QuadSPI controller are:

- x1 (single), x2 (dual), x4 (Quad), x8 (Octal) I/O SPI, and HYPERBUS™
- Single Data Rate (SDR) and Double Data Rate (DDR) sampling modes
- Up to 200 MHz serial clock speed

For an in-depth description about the QuadSPI controller, see AN13563 published from NXP.

1.3 Hardware and software setup

The following hardware and software are used to cover all the topics in this document.

- S32G Vehicle Networking Reference Design (S32G-VNP-RDB2) with flash memory replaced
- Infineon S26KS256S HYPERFLASH™ and S26HS512T SEMPER™ NOR flash
- S32 Design Studio v3.6 along with S32 Flash Tool and S32 Real-Time Drivers (RTD) 5.0.0

2 Hardware setup

2.1 HYPERFLASH™ pinout and signal description

HYPERFLASH™ devices are provided in Fortified Ball Grid Array (FBGA), 1 mm pitch, 24-ball, 5 x 5 ball array footprint (Figure 1). The footprint and pin assignment are compatible with x8 (Octal) SPI flash memories from different vendors. Table 1 describes input/output signals typically connected to S32G.

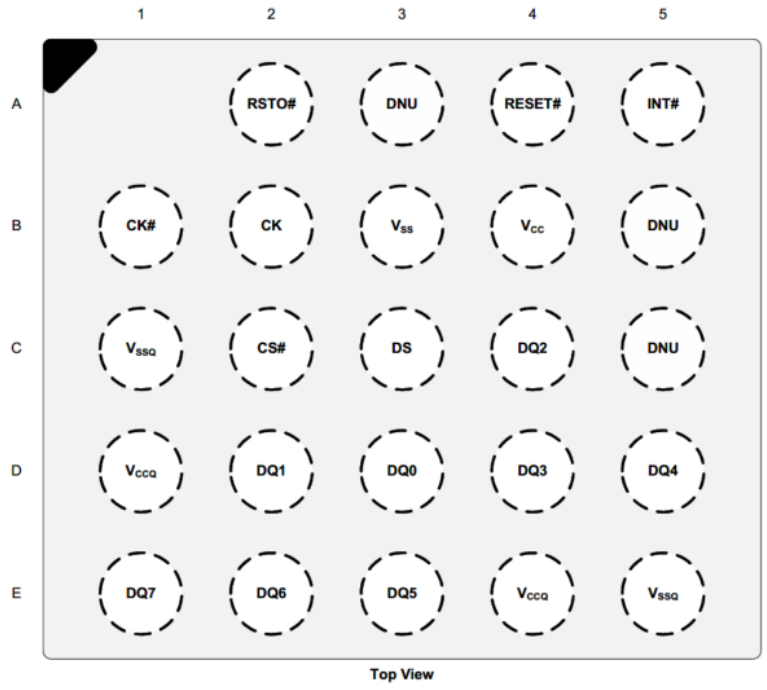


Figure 1 24-ball FBGA pinout

Table 1 Input/output signal description

Name	Type	Description
CS#	Input	**Chip Select:** Device is selected and in active state when CS# is LOW
CK	Input	**Clock:** Provides the timing of the serial interface
CK#	Input	**Differential Clock:** This signal is mandatory in S26KS-S, not used S26KL-S, and optional in S26HL-T and S26HS-T
DS	Output	**Data Strobe:** Used for data read operations only and indicates output data valid
DQ[7..0]	Input/output	**Serial Data:** Bidirectional signals that transfer command, address, and data information
INT#	Output (open drain)	**Interrupt:** An optional signal intended to be used to indicate an on-chip event has occurred
RESET#	Input	**Hardware Reset:** Resets device to default state

2.2 Connecting S32G QuadSPI controller and HYPERFLASH™

The S32G QuadSPI controller has two independent ports (A and B) and each port has two chip selects. Figure 2 is an example of a connection between S32G274A and S26KS256S HYPERFLASH™. In this example, QuadSPI port A (QSPI_A), Chip Select 0 (CS0) is used.

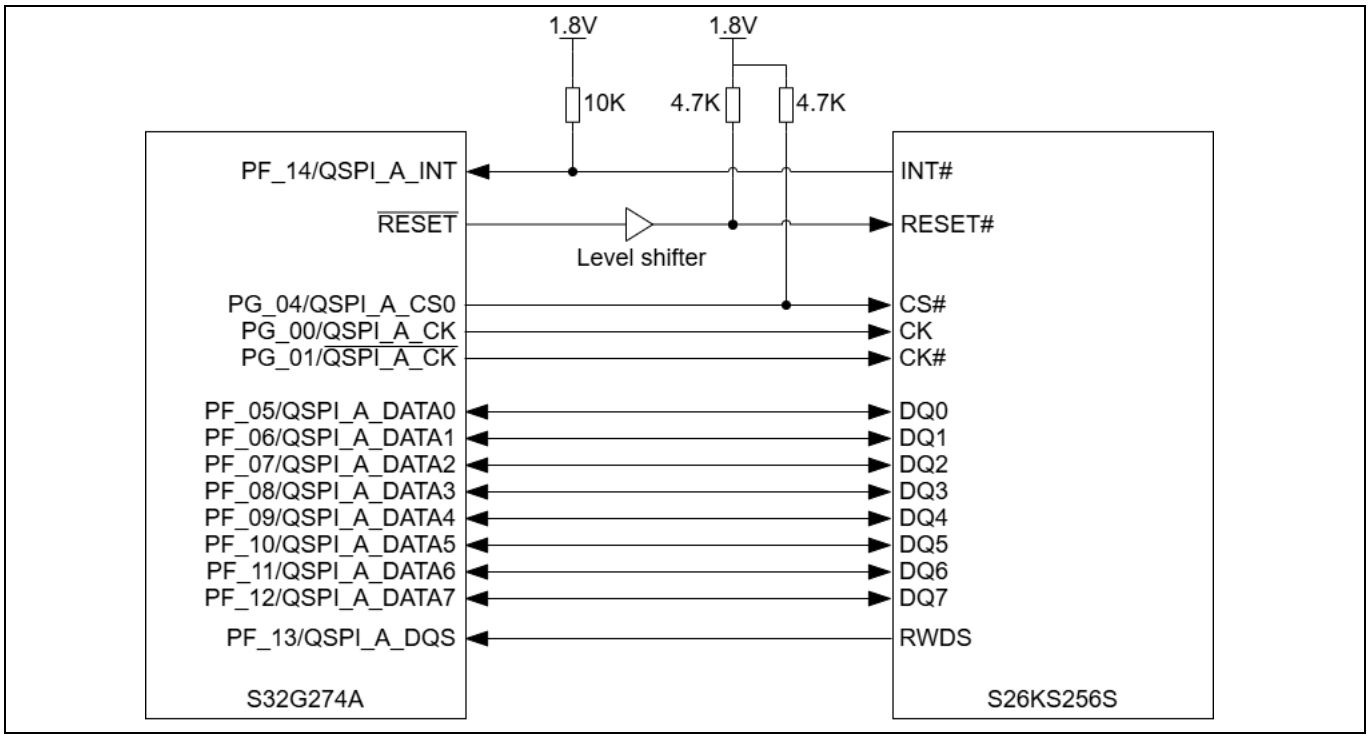


Figure 2 Connection between S32G274A and S26KS256S HYPERFLASH™

3 S32G boot configuration for HYPERFLASH™

S32G has BootROM firmware and it manages the boot sequence based on options specified through the boot configuration fuses. BootROM supports booting from external flash memory including HYPERFLASH™. This section describes the configuration required to boot from HYPERFLASH™ and boot performance optimization by maximizing read throughput of HYPERFLASH™.

3.1 Boot from HYPERFLASH™

Boot interface, device, and other options are controlled by boot configuration eFuse BOOT_CFGn. For the application development phase, boot configuration can be changed by 32 GPIOs named RCON[31:0], which corresponds bit by bit to BOOT_CFG1[31:0]. On S32G-VNP-RDB2, DIP switches are assigned to RCON/BOOT_CFG1. Table 2 shows the RCON/BOOT_CFG1 settings required for HYPERFLASH™ boot and corresponding DIP switches on S32G-VNP-RDB2. The configuration bits not described in the table are assumed to be '0'. See the S32G Reference Manual for the details of all boot configuration eFuse.

Table 2 Boot configuration for HYPERFLASH™

Fuse name	Fuse bit position	S32G-VNP-RDB2	Settings for HYPERFLASH™
Boot interface	BOOT_CFG1[7:5]	SW4[8:6]	**000:** QuadSPI as the boot interface
QuadSPI mode	BOOT_CFG1[4:2]	SW4[5:3]	**001:** HYPERFLASH™ mode
QuadSPI CAS	BOOT_CFG1[14:11]	SW5[7:4]	**0011:** Column address space in HYPERFLASH™
QuadSPI port	BOOT_CFG1[9]	SW5[2]	**0:** Port A
Time hold delay	BOOT_CFG1[23:22]	SW6[8:7]	**01:** Data aligned with 2X
Differential clock	BOOT_CFG1[19]	SW6[4]	**1:** Enable differential clock (for S26KS-S only)
DQS selection	BOOT_CFG1[30:29]	SW7[7:6]	**11:** External DQS
DLLSMPF	BOOT_CFG1[28:26]	SW7[5:3]	**100:** 4th tap

3.2 Boot performance optimization

With RCON/BOOT_CFG1 settings shown in Table 2, BootROM configures a QuadSPI controller for HYPERFLASH™ (x8 DDR mode) at 40 MHz, then reads reconfiguration parameters located at offset 200h in the HYPERFLASH™. Then BootROM reconfigures the QuadSPI controller with the reconfiguration parameters. Typically, reconfiguration parameters support higher clock frequency to optimize boot performance. Figure 3 shows the binary dump image of reconfiguration parameters generated by S32 Design Studio Configuration Tools. It is optimized for S26KS256S HYPERFLASH™ at 166 MHz. Table 3 and Table 4 are description of parameters and values.

```
$ hexdump -C s26ks256s-166.bin
00000000  5a 5a 5a 5a ec 00 00 07  03 03 01 00 00 00 00 00  |ZZZZ............|
00000010  0c 00 80 c2 00 00 00 00  03 00 01 00 00 00 00 04  |................|
00000020  ff 00 ff 00 00 00 00 02  00 00 00 02 00 00 00 00  |................|
00000030  00 00 00 00 00 00 00 00  00 00 00 00 00 00 01 00  |................|
00000040  a6 00 00 00 a0 47 18 2b  10 4f 0f 0f 40 3b 00 00  |.....G.+.O..@;..|
00000050  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00  |................|
*
00000200
```

Figure 3 Hex dump image of reconfiguration parameters

S32G boot configuration for HYPERFLASH™

Table 3 Reconfiguration parameters for HYPERFLASH™

Parameter	Value	Remarks
Header	0x5A5A5A5A	Fixed value
MCR	0x070000EC	CKN_FA_EN = 1, DQS_FA_SEL = 3, DDR_EN = 1, DQS_EN = 1, DQS_LAT_EN = 1
FLSHCR	0x00010303	TDH = 1, TCSH = 3, TCSS = 3
BFGENCR	0x00000000	–
DLLCR	0xC280000C	DLLEN = 1, FREQEN = 1, DLL_REFCNTR = 2, DLLRES = 8, SLAVE_AUTO_UPDT = 1, SLV_EN = 1
PARITYCR	0x00000000	–
SFACR	0x00010003	WA = 1, CAS = 3
SMPR	0x04000000	DLLFSMPFA = 4
DLCR	0x00FF00FF	–
SFLASH_1_SIZE	0x02000000	256 Mb (32 MB)
SFLASH_2_SIZE	0x02000000	Must be the same as above
DLPR	0x00000000	Data Learning Pattern is not used
SFAR	0x00000000	–
TBDR	0x00000000	–
DLL_BYPASS_EN	0x00	–
Reserved	0x00	–
DLL_AUTO_UPD_EN	0x01	–
IPCR_TRIGGER_EN	0x00	–
SFLASH_CLK_FREQ	0xA6	Max. 166 MHz for S26KS256S
Reserved	0x00 0x00 0x00	–
COMMAND_SEQ	0x47A0 0x2B18 0x4F10 0x0F0F 0x3B40 0x0000	See decoded read command sequence in Table 4
FLASH_WRITE_DATA	0x00 … 0x00	Not used (all 0)

Table 4 HYPERFLASH™ read command sequence

Instruction	Pad	Operand	Description
CMD_DDR	0x03	0xA0	Read command with continuous burst type
ADDR_DDR	0x03	0x18	24-bit row address
CADDR_DDR	0x03	0x10	16-bit column address (lower 3 bits are valid)
DUMMY	0x03	0x0F	15 dummy cycles
READ_DDR	0x03	0x40	64-bytes data read (size is overwritten by BootROM)
STOP	0x00	0x00	End of sequence

4 Programming to HYPERFLASH™

S32 Flash Tool is a flash programming software for NXP S32 devices. It can program external flash memories connected to a QuadSPI controller. The details about S32 Flash Tool are described in S32 Flash Tool User Guide in the install folder (*C:\NXP\S32DS.3.6.1\S32DS\tools\S32FlashTool\doc\S32_Flash_Tool_User_Guide.pdf*) and AN13563. The flash algorithm file for HYPERFLASH™ is available to use.

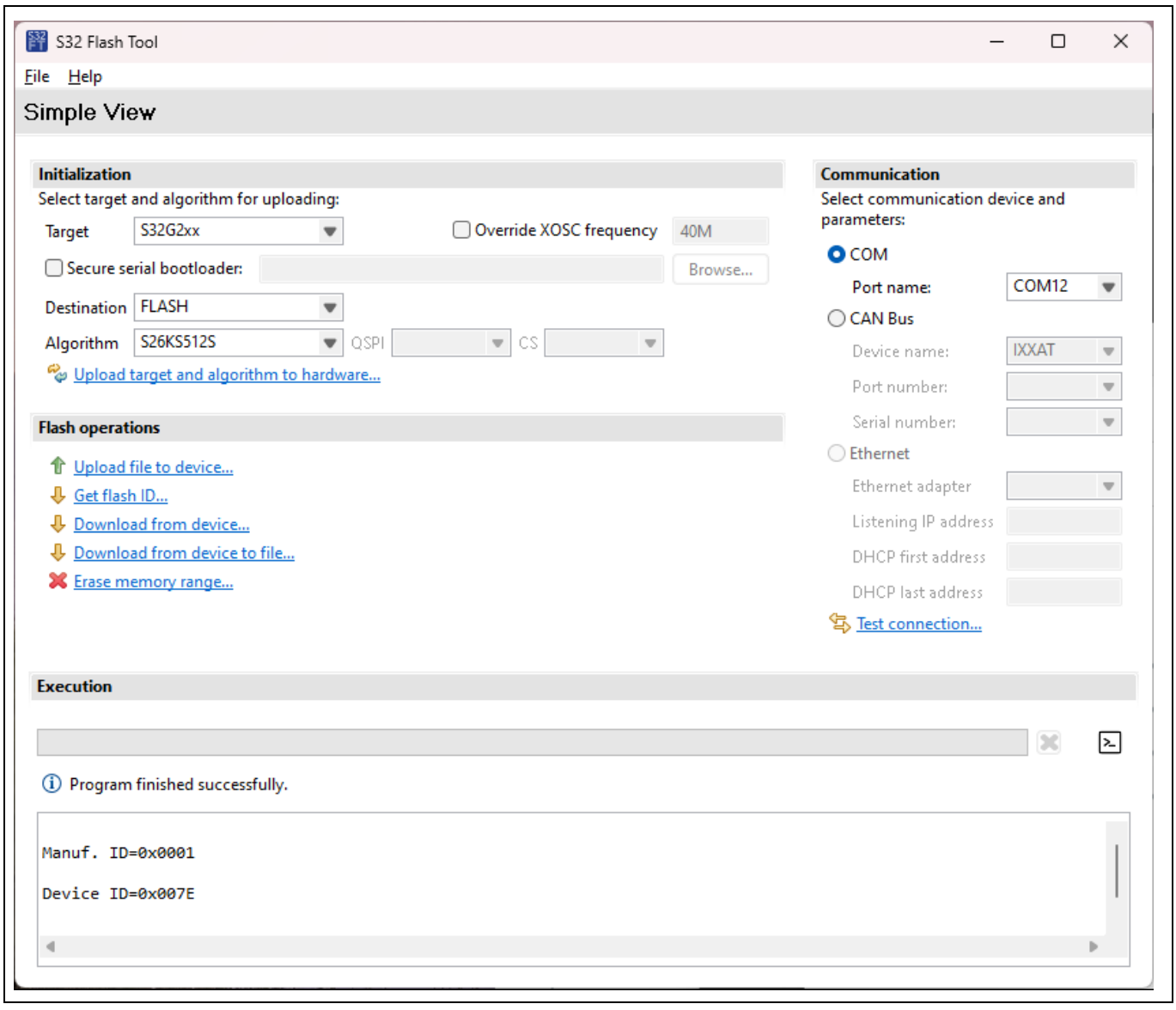


Figure 4 Reading HYPERFLASH™ ID in S32 Flash Tool

5 Flash driver configuration for HYPERFLASH™

The flash driver for real-time applications, FLS is a part of Real-Time Drivers (RTD) provided by NXP. RTD is bundled with S32 Design Studio along with example projects and a driver configuration tool. The following sections explain how to import an FLS example project to S32 Design Studio and configure it for HYPERFLASH™.

5.1 Import FLS example project

1. In S32 Design Studio, select **File** > **New** > **S32DS Project From Example**

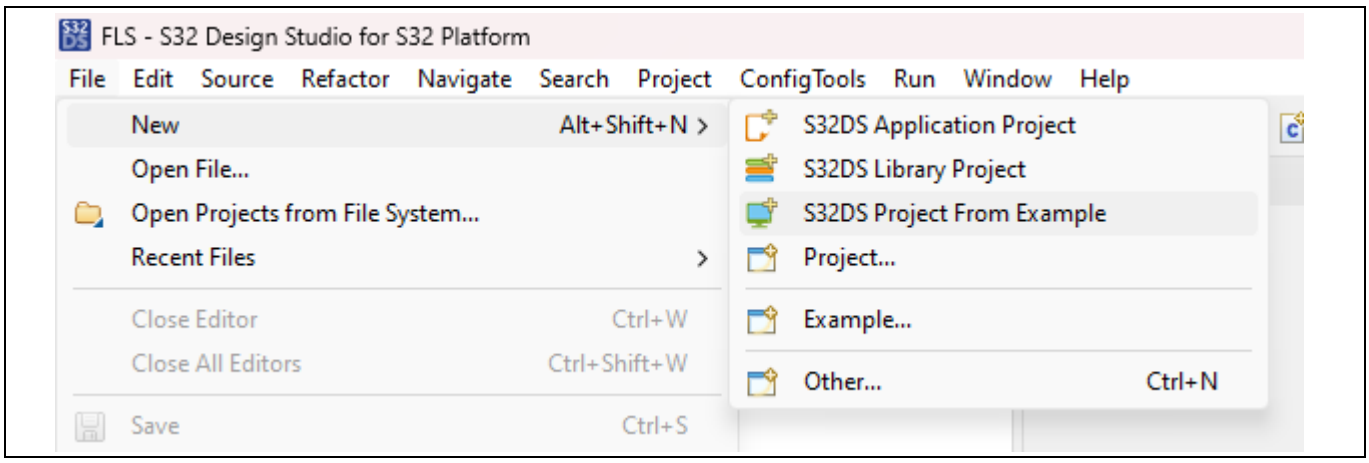


Figure 5 Create an S32DS project from example

2. In the selection dialog, select **Fls Examples** project then click the **Finish** button

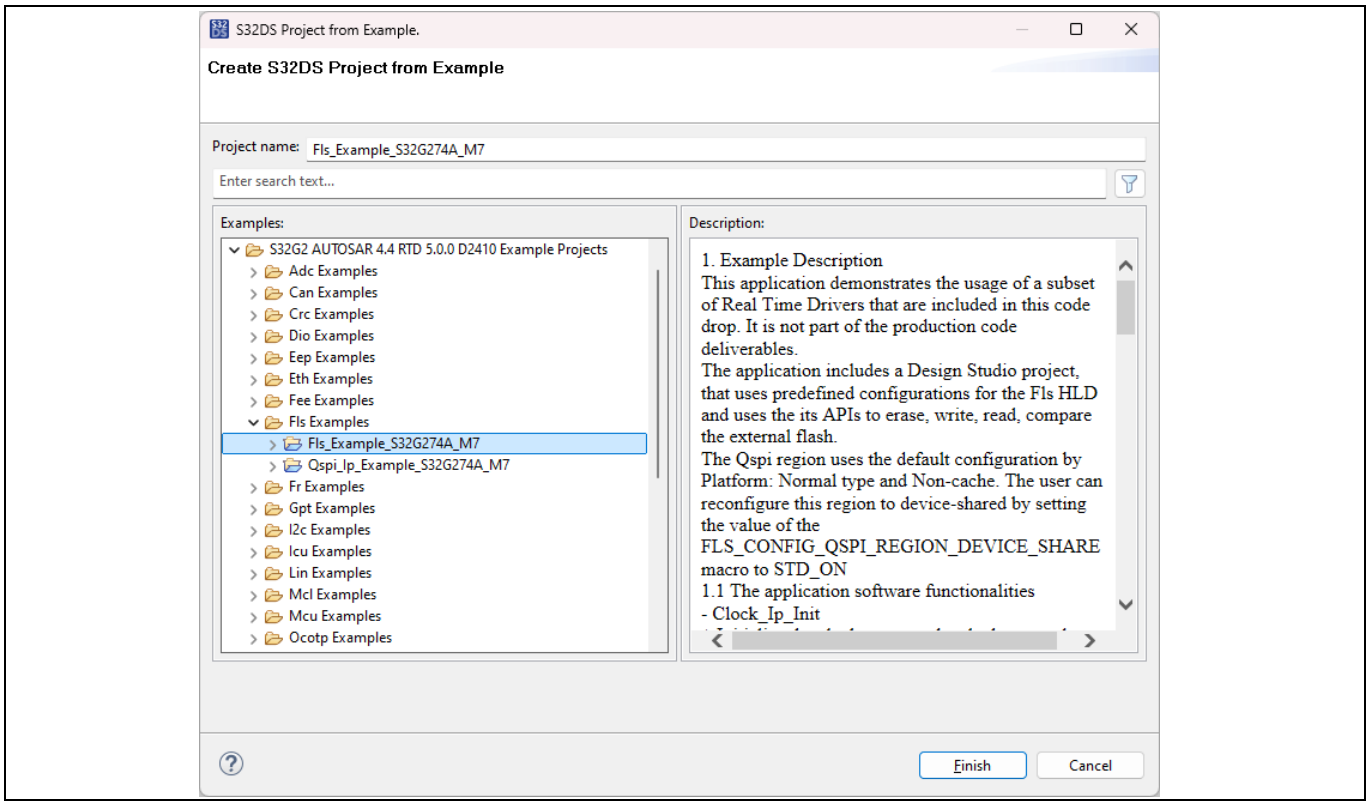


Figure 6 FLS example project in selection dialog

5.2 Clock configuration for QuadSPI controller

Clock for external flash can be configured by the clock configuration tool in S32 Design Studio. Select **ConfigTools** > **Clocks** menu to open the configuration tool. The clock for the external flash is named as *QSPI_1X_CLK*. By default, it is set to 200 MHz in the example project. To adjust QSPI_1X_CLK, modify the divisor for PERIPH_PLL_DFS1 and QSPI0_CLK. Figure 7 and Figure 8 show the clock path and divisor settings to generate a 166 MHz clock for S26KS256S HYPERFLASH™. In this case, the divisors for PERIPH_PLL_DFS1 and QSPI0_CLK are 3 and 2 respectively.

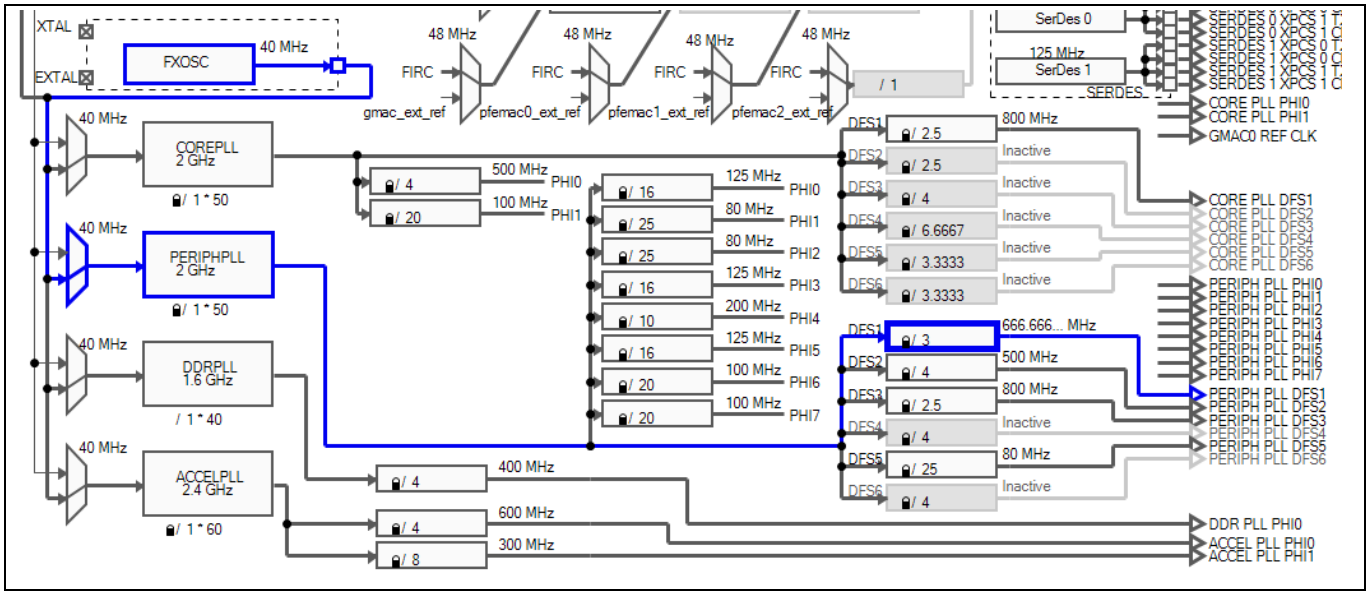


Figure 7 Clock divisor PERIPH_PLL_DFS1

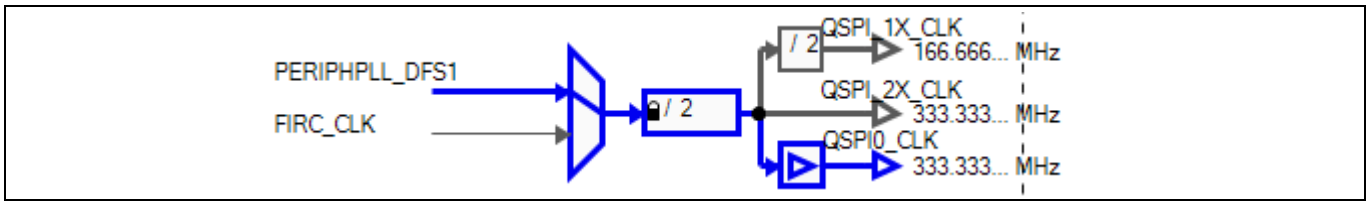


Figure 8 Clock divisor for QSPI0_CLK

5.3 FLS configuration for HYPERFLASH™

In S32 Design Studio, select **ConfigTools** > **Peripherals**, click the **Fls** pane in the Components tab, then Fls configuration window with containers and parameters appear (Figure 9). The following sections only describe about parameters in FlsSectorList and FlsExternalDriver containers that are specific for HYPERFLASH™. See the user manual for S32 FLS Driver in the install folder (*C:\NXP\S32DS.3.6.1\S32DS\software\PlatformSDK_S32XX_4_0_0\RTD\Fls_TS_T40D11M50I0R0\doc\RTD_FLS_UM.pdf*) for the details of all parameters and driver design.

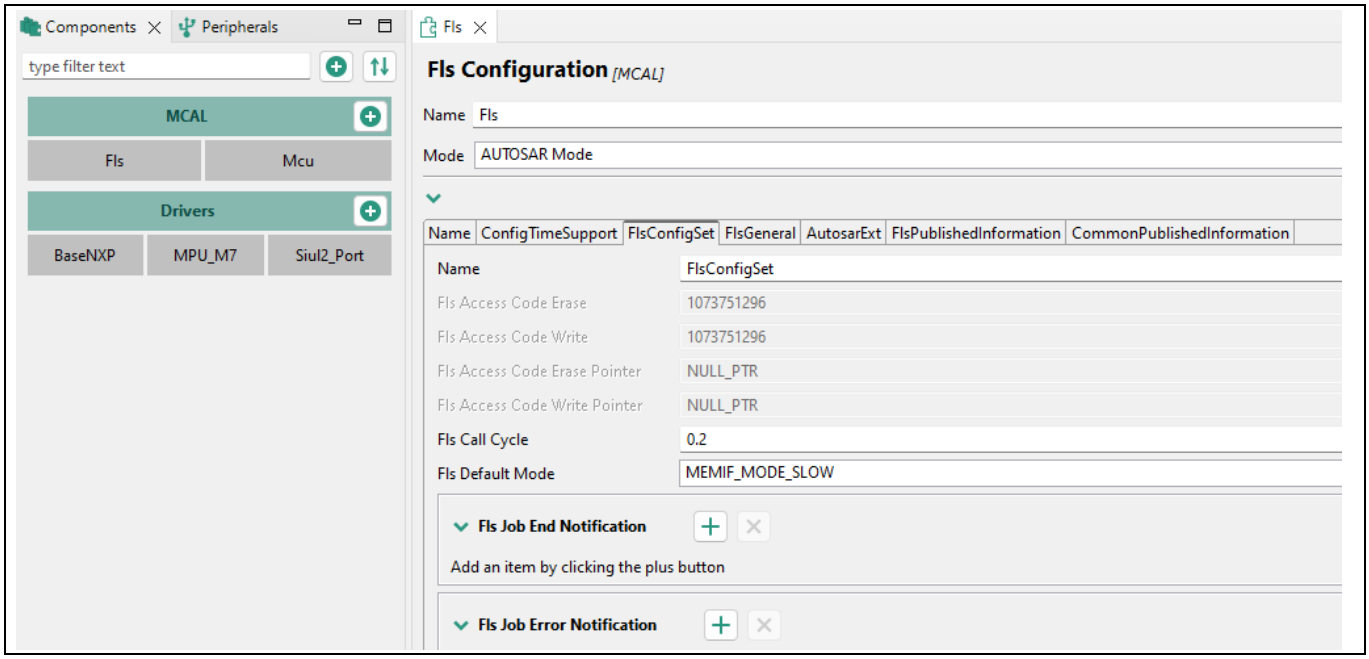


Figure 9 Fls configuration window

5.3.1 FlsSectorList

Figure 10 shows simple settings of FlsSectorList for HYPERFLASH™ as an example. Table 5 describes key parameters that need to be adapted for HYPERFLASH™.

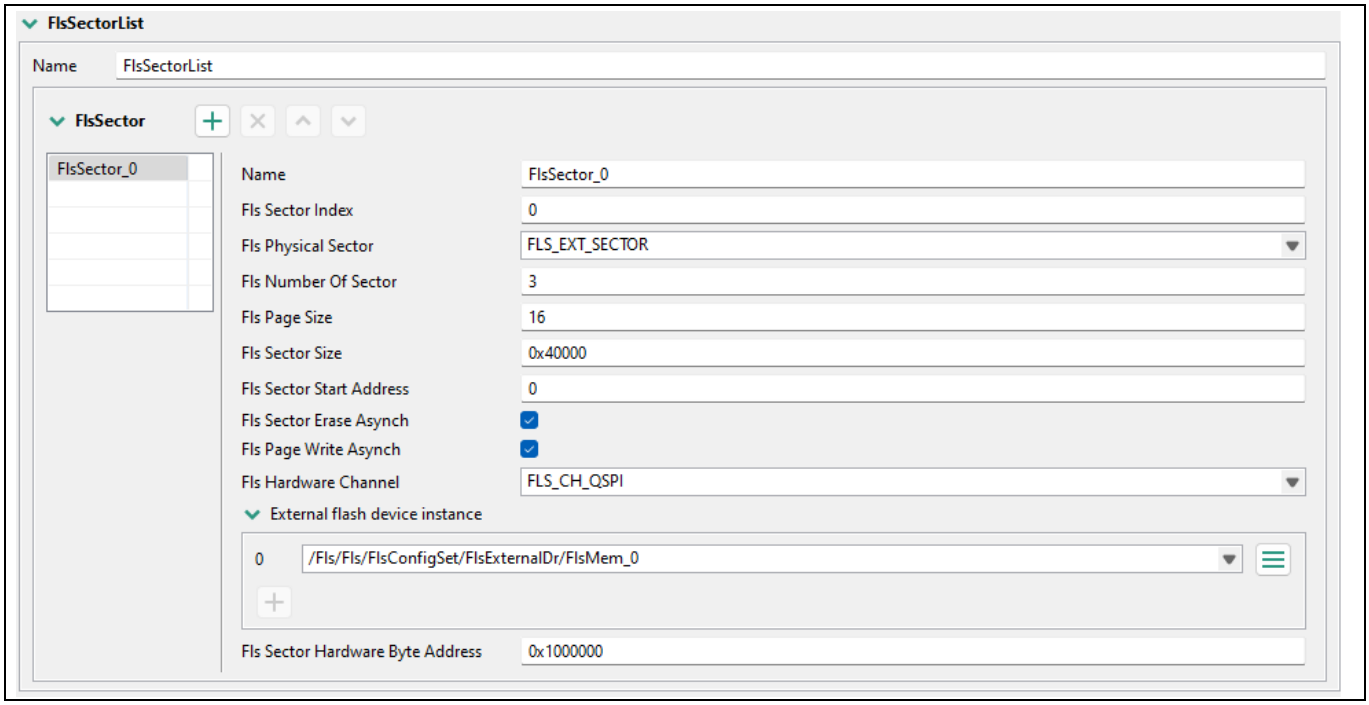


Figure 10 FlsSectorList window

Table 5 Key parameters in FlsSectorList

Parameter	Value	Comment
Fls Page Size	16	Must be a multiple of 16 bytes to align the ECC data unit
Fls Sector Size	0x40000	HYPERFLASH™ has 256 Kbytes uniform sectors (default)
Fls Sector Hardware Byte Address	Any	Must be aligned with the sector boundary

5.3.2 ControllerCfg

ControllerCfg is a set of configuration parameters specific to external flash controllers. In S32G, it defines parameters to configure the QuadSPI controller. Figure 11 and Table 6 show ControllerCfg example of S26KS256S HYPERFLASH™. Table 6 describes key parameters that need to be adapted. In this example, S26KS256S is connected to side A1 of the S32G QuadSPI controller. S32G reference manual, datasheet, and AN13563 suggest appropriate QuadSPI controller configuration for different use cases. Settings in this example follow the suggested configuration for DDR-200 MHz, which can cover S26KS256S HYPERFLASH™ (x8 DDR at 166 MHz).

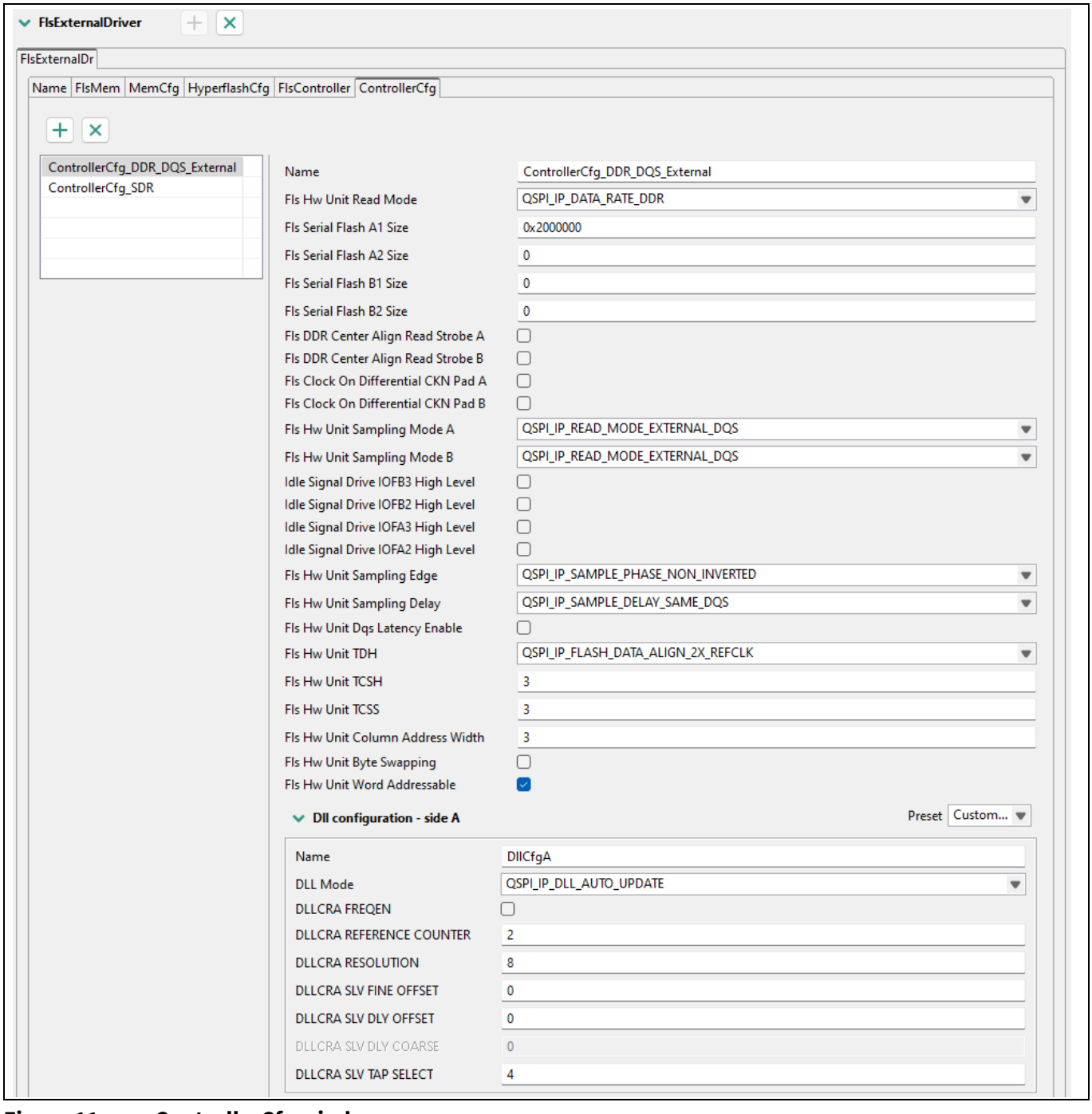


Figure 11 ControllerCfg window

Flash driver configuration for HYPERFLASH™

Table 6 Key parameters in ControllerCfg

Parameter	Value
Fls Hw Unit Read Mode	QSPI_IP_DATA_RATE_DDR
Fls Serial Flash A1 Size	0x2000000
Fls Clock On Differential CKN Pad A	Checked
Fls Hw Unit Sampling Mode A	QSPI_IP_READ_MODE_EXTERNAL_DQS
Fls Hw Unit TDH	QSPI_IP_FLASH_DATA_ALIGN_2X_REFCLK
Fls Hw Unit TCSH	3
Fls Hw Unit TCSS	3
Fls Hw Unit Column Address Width	3
Fls Hw Unit Word Addressable	Checked
DLL Mode	QSPI_IP_DLL_AUTO_UPDATE
DLLCRA REFERENCE COUTNER	2
DLLCRA RESOLUTION	8
DLLCRA SLV FINE OFFSET	0
DLLCRA SLV DLY OFFSET	0
DLLCRA SLV TAP SELECT	4

5.3.3 HyperflashCfg

HyperflashCfg is a set of parameters specific for HYPERFLASH™ devices. Figure 12 and Table 7 show HyperflashCfg example of S26KS256S HYPERFLASH™. Flash device size and Flash device page size must be set to 32 MB and 512 bytes respectively. Other parameters correspond to configuration register fields in HYPERFLASH™. In this example, those parameters are aligned with the factory default of the HYPERFLASH™ configuration register.

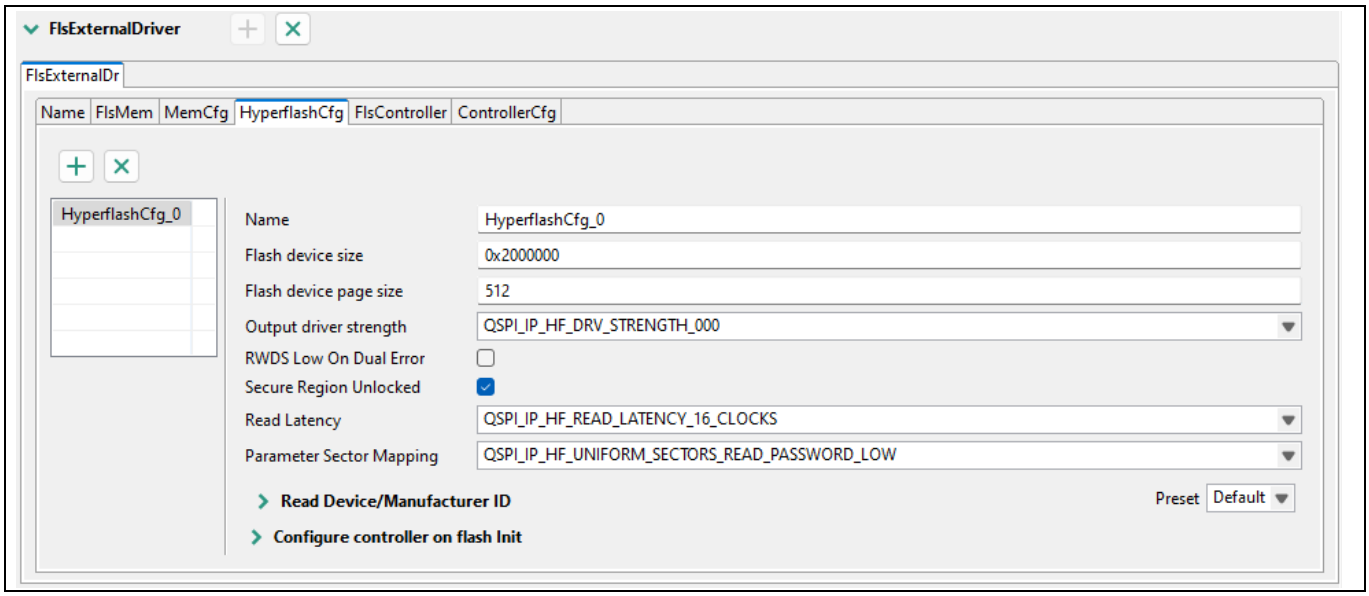


Figure 12 HyperflashCfg window

Table 7 Key parameters in HyperflashCfg

Parameter	Value
Flash device size	0x2000000
Flash device page size	512
Output driver strength	QSPI_IP_HF_DRV_STRENGTH_000
RWDS Low On Dual Error	Not checked
Secure Region Unlocked	Checked
Read Latency	QSPI_IP_HF_READ_LATENCY_16_CLOCKS
Parameter Sector Mapping	QSPI_IP_HF_UNIFORM_SECTORS_READ_PASSWORD_LOW

5.3.4 FlsController

Figure 13 shows the configuration example of FlsController parameters. It should look up the ControllerCfg defined in Section 5.3.2.

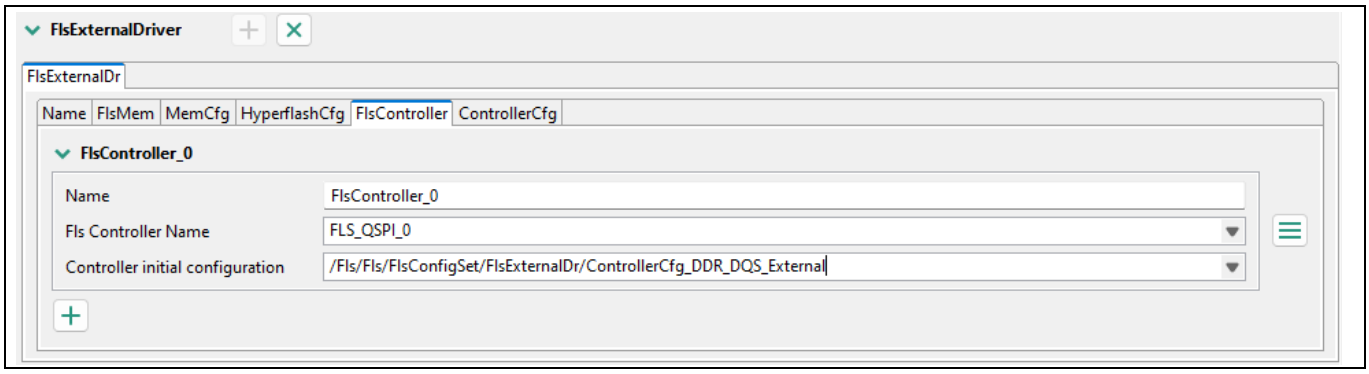


Figure 13 FlsController window

5.3.5 FlsMem

Figure 14 shows the configuration example of FlsMem parameters. The flash memory alignment must be 2 as HYPERFLASH™ is a word-aligned device.

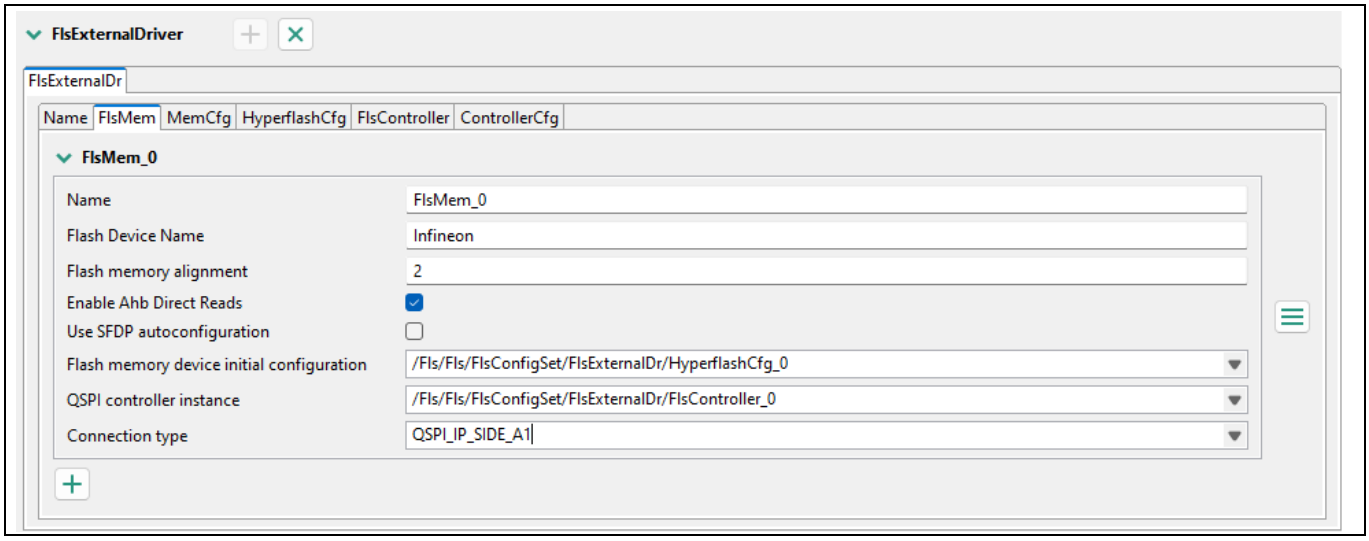


Figure 14 FlsMem window

6 Summary

Infineon S26KL-S/S26KS-S HYPERFLASH™ family of devices can be connected to QuadSPI controller in NXP S32G Vehicle Network Processors as external flash memory. The BootROM firmware in S32G can configure the QuadSPI controller and load user application from HYPERFLASH™ with optimized performance. S32 Flash Tool supports programming algorithm for HYPERFLASH™. Finally, Real-Time Driver (RTD) along with example project is available for HYPERFLASH™ with GUI-based configuration tool integrated in S32 Design Studio.

References

References

Contact Infineon support to obtain documents that are not available online.

[1] NXP Semiconductors: *S32G2 reference manual*; Available online

[2] NXP Semiconductors: *S32G2 datasheet*; Available online

[3] NXP Semiconductors: *AN13563: S32G QuadSPI Deep Dive application note*; Available online

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[5] Infineon Technologies AG: *SEMPER™ NOR flash webpage*; Available online

Revision history

Revision history

Document revision	Date	Description of changes
**	2025-07-09	Initial release

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